Errata

2Gb Parallel NAND with ECC off
MT29F2G08ABAGAWP-IT:G, MT29F2G08ABAGAH4-IT:G, MT29F2G08ABBGAH4-IT:G

Introduction

This document is an update to the specifications for the Micron® MT29F parallel NAND Flash memory data sheet. It is intended for hardware system manufacturers and software developers of applications, operating systems, and tools.

Scope

This document provides an explanation of device errata, including errata problem statement, implications, workaround, and status specific to the marketing part numbers (MPN) listed above.

This document may also contain information that was not previously published.

This document should be used with and may include updates to the specifications contained in 2Gb parallel NAND with ECC off data sheets. This erratum is applicable only when ECC is turned on.

Terminology

Errata: Design defects or errors in a published data sheet. Errata may cause product's behavior to deviate from published specifications. Hardware and software designed for use with any given stepping must assume that all errata documented for that stepping are present on all devices.

Device Identification

This section details how to identify a device affected by the errata defined in this document. The MPNs that identify an affected device begin with:

- MT29F2G08ABAGAWP-IT:G
- MT29F2G08ABAGAH4-IT:G
- MT29F2G08ABBGAH4-IT:G

Summary Table of Changes

Table below summarizes known issues in the current silicon revision.

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Table 1: Errata Summary

Erratum Number	Status[1]	Issue
1	Fix	If ECC is on, all page reads after a failed PROGRAM or ERASE cycle return fail status

Note: 1. Doc = Documentation changes only; Fix = This erratum is intended to be addressed; Fixed = This erratum has already been addressed; No Fix = There are no plans to address this erratum.

Errata List

Table 2: Known Issues, Workarounds, and Status

Erratum Number	Status	Issue
1	Problem	Status register bit 0 does not get reset after a failed PROGRAM or ERASE cycle.
	Implication	When the status bit 0 is set due to a failed PROGRAM or ERASE cycle, it does not get reset when a page read is initiated. This can be mis-interpreted as read failure due to uncorrectable ECC errors.
	Workaround	If the device encounters a program or erase failure, the host needs to do one of the items listed below to clear the status register fail bit: • Erase a block successfully or • Program a block successfully or • Program another block with 0xFF data or • Issue a reset command
	Status	A fix has been identified and will be enabled in the next silicon stepping.

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Revision History

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- Initial release

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