NAND Flash Memory

Serial Peripheral Interface (SPI)

MT29F2G01ABAGDSF, MT29F2G01ABAGD12, MT29F2G01ABAGDWB

Features

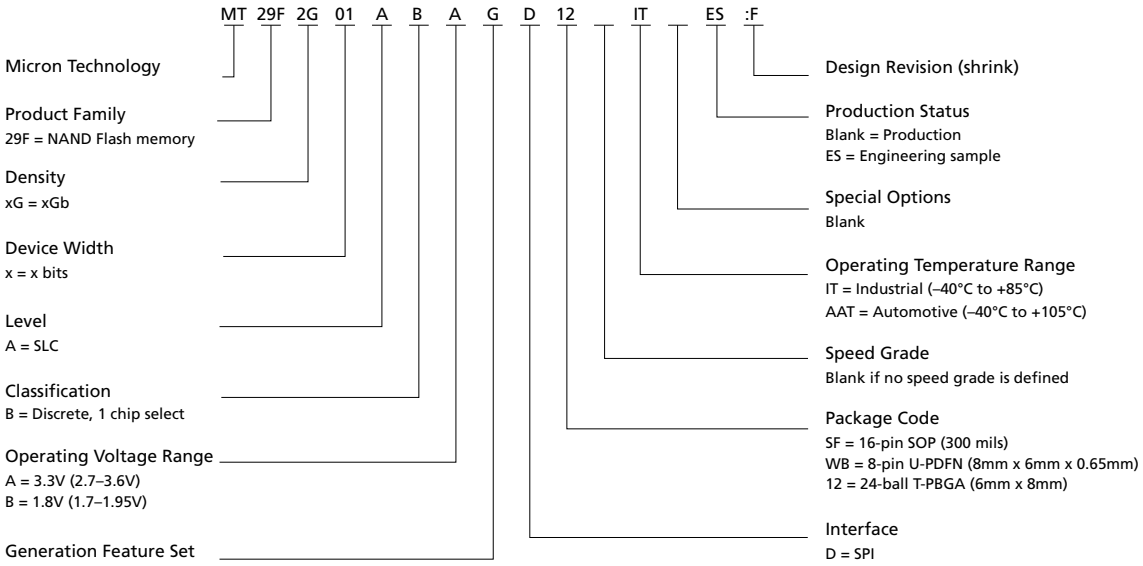
- Single-level cell (SLC) technology
- 2Gb density
- Organization
  - Page size x1: 2176 bytes (2048 + 128 bytes)
  - Block size: 64 pages (128K + 8K bytes)
  - Plane size: 2Gb (2 planes, 1024 blocks per plane)
- Standard and extended SPI-compatible serial bus interface
  - Instruction, address on 1 pin; data out on 1, 2, or 4 pins
  - Instruction on 1 pin; address, data out on 2 or 4 pins
  - Instruction, address on 1 pin; data in on 1 or 4 pins
- User-selectable internal ECC supported
  - 8 bits/sector
- Array performance
  - 133 MHz clock frequency (MAX)
  - Page read: 25µs (MAX) with on-die ECC disabled; 70µs (MAX) with on-die ECC enabled
  - Page program: 200µs (TYP) with on-die ECC disabled; 220µs (TYP) with on-die ECC enabled
  - Block erase: 2ms (TYP)
- Advanced features
  - Read page cache mode
  - Read unique ID
  - Read parameter page
- Device initialization
  - Automatic device initialization after power-up
- Security
  - Blocks 7:0 are valid when shipped from factory with ECC enabled
  - Software write protection with lock register
  - Hardware write protection to freeze BP bits
  - Lock tight to freeze BP bits during one power cycle
- Permanent block lock protection
  - OTP Space: 10 pages one-time programmable NAND Flash memory area
- Operating voltage range
  - V_{CC} = 2.7–3.6V
- Operating temperature
  - Industrial: –40°C to +85°C
- Quality and reliability
  - Endurance: 100,000 PROGRAM/ERASE cycles
  - Data retention: JESD47H-compliant; see qualification report
  - Additional: Uncycled data retention: 10 years 24/7 @85°C
- Package
  - 16-pin SOP, 300 mils (package code: SF)
  - 8-pin U-PDFN, 8mm x 6mm x 0.65mm (MLP8) (package code: WB)
  - 24-ball T-PBGA, 05/6mm x 8mm (5 x 5 array) (package code: 12)

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Part Numbering Information

Micron NAND Flash devices are available in different configurations and densities. Verify valid part numbers by using Micron's part catalog search at www.micron.com. To compare features and specifications by device type, visit www.micron.com/products. Contact the factory for devices not found.

Figure 1: Part Number Chart



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Contents

General Description 7
Architecture 8
Pin Assignments 9
Pin Descriptions 10
Memory Mapping 11
Array Organization 11
Bus Operation 12
SPI Modes 12
SPI Protocols 12
SPI NAND Command Definitions 13
RESET Operation 14
WRITE Operations 15
WRITE ENABLE (06h) 15
WRITE DISABLE (04h) 15
READ Operations 16
PAGE READ (13h) 16
READ FROM CACHE x1 (03h or 0Bh) 18
READ FROM CACHE x2 (3Bh) 19
READ FROM CACHE x4 (6Bh) 20
READ FROM CACHE Dual I/O (BBh) 21
READ FROM CACHE Quad I/O (EBh) 22
READ PAGE CACHE RANDOM (30h) 23
READ PAGE CACHE LAST (3Fh) 25
READ ID (9Fh) 25
Parameter Page 26
Parameter Page Data Structure Table 26
Unique ID Page 27
Program Operations 29
PAGE PROGRAM 29
PROGRAM LOAD x1 (02h) 29
PROGRAM EXECUTE (10h) 30
RANDOM DATA PROGRAM x1 (84h) 32
PROGRAM LOAD x4 (32h) and PROGRAM LOAD RANDOM DATA x4 (34h) 33
INTERNAL DATA MOVE 33
Block Erase Operations 34
Features Operations 36
GET FEATURES (0Fh) and SET FEATURES (1Fh) 36
Feature Settings 37
Security – Volatile Block Protection 38
Security – Block Protection Bits 38
Security – Hardware Write Protection 39
Security – Device Lock Tight (LOT) 39
Permanent Block Lock Protection 39
PROTECTION Command (2Ch) Details 40
Permanent Block Lock Protection Disable Mode 40
Security – One Time Programmable (OTP) 41
Enable OTP Access 41
OTP Configuration States 41
OTP Protection and Program Prevention 42
Exit OTP 42

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Status Register 43
ECC Protection 44
Error Management 46
SPI NOR Read Configuration 47
Power-Up and Power-Down 50
Electrical Specifications 52
Package Dimensions 57
  Package Dimensions 58
  Package Dimensions 59
Revision History 60
  Rev. F – 09/16 60
  Rev. E – 06/16 60
  Rev. D – 05/16 60
  Rev. C – 01/16 60
  Rev. B – 10/15 60
  Rev. A – 06/15 60

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List of Figures

Figure 1: Part Number Chart 2
Figure 2: Functional Block Diagram 8
Figure 3: 8-Pin, U-PDFN (Top View) 9
Figure 4: 16-Pin, SOP2 (Top View) 9
Figure 5: 24-Ball T-PBGA, 5 x 5 (Balls Down) 9
Figure 6: Memory Map 11
Figure 7: Array Organization 11
Figure 8: SPI Modes Timing 12
Figure 9: RESET (FFh) Timing 14
Figure 10: WRITE ENABLE (06h) Timing 15
Figure 11: WRITE DISABLE (04h) Timing 15
Figure 12: PAGE READ (13h) Timing 17
Figure 13: READ FROM CACHE (03h or 0Bh) Timing 18
Figure 14: READ FROM CACHE x2 19
Figure 15: READ FROM CACHE x4 20
Figure 16: READ FROM CACHE Dual I/O 21
Figure 17: READ FROM CACHE Quad I/O 22
Figure 18: READ PAGE CACHE RANDOM Sequence 24
Figure 19: READ ID (9Fh) Timing 25
Figure 20: PROGRAM LOAD (02h) Timing 30
Figure 21: PROGRAM EXECUTE (10h) Timing 31
Figure 22: PROGRAM LOAD RANDOM DATA (84h) Timing 32
Figure 23: PROGRAM LOAD x4 (32h) Timing 33
Figure 24: BLOCK ERASE (D8h) Timing 35
Figure 25: GET FEATURES (0Fh) Timing 36
Figure 26: SET FEATURES (1Fh) Timing 36
Figure 27: PROTECT Command Cycle 40
Figure 28: Read from Cache (03h) 48
Figure 29: Fast Read from Cache (0Bh) 49
Figure 30: SPI Power-Up 50
Figure 31: SPI Power-Up Timing 50
Figure 32: Alternative SPI Power-Up Timing 51
Figure 33: AC Measurement I/O Waveform 52
Figure 34: WP# Timing 55
Figure 35: Serial Input Timing 56
Figure 36: Serial Output Timing 56
Figure 37: 16-pin SOP (300 mils body width) – Package Code: SF 57
Figure 38: 8-pin U-PDFN (MLP8) 8mm x 6mm x 0.65mm – Package Code: WB 58
Figure 39: 24-Pin T-PBGA (5 x 5 Ball Grid Array) 6mm x 8mm – Package Code: 12 59

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List of Tables

Table 1: SPI Pin Descriptions 10
Table 2: SPI NAND Command Set 13
Table 3: READ ID Table 25
Table 4: Parameter Table 26
Table 5: Feature Address Settings and Data Bits 37
Table 6: Block Lock Register Block Protect Bits 38
Table 7: Configuration Registers for Security 42
Table 8: Status Register Bit Descriptions 43
Table 9: ECC Status Register Bit Descriptions 44
Table 10: ECC Protection 45
Table 11: Error Management Details 46
Table 12: Absolute Maximum Ratings 52
Table 13: Operating Conditions 52
Table 14: AC Measurement Conditions 52
Table 15: Capacitance 53
Table 16: DC Characteristics 53
Table 17: AC Characteristics 53
Table 18: PROGRAM/READ/ERASE Characteristics 54

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General Description

Serial peripheral interface (SPI) NAND is an SLC NAND Flash memory device that provides a cost-effective nonvolatile memory storage solution where pin count must be kept to a minimum. It is also an alternative solution to SPI NOR, offering superior write performance and cost per bit over SPI NOR. The hardware interface creates a low pin-count device with a standard pinout that remains the same from one density to another and supports future upgrades to higher densities without board redesign.

The serial electrical interface follows the industry-standard serial peripheral interface. New command protocols and registers are defined for SPI operation. The command set resembles common SPI-NOR command sets, modified to handle NAND specific functions and additional new features.

New features include user-selectable internal ECC and first page auto-load on power-up. SPI NAND Flash devices have six signal lines plus VCC and ground (GND). The signal lines are SCK (serial clock), SI, SO (for command/response and data input/output), and control signals CS, HOLD#, WP#. This hardware interface creates a low pin-count device with a standard pinout that remains the same from one density to another, supporting future upgrades to higher densities without board redesign.

Each block of the serial NAND Flash device is divided into 64 programmable pages, each page consisting of 2176 bytes. Each page is further divided into a 2048-byte data storage region and a 128-byte spare area. The 128-byte area is typically used for memory and error management functions.

With internal ECC enabled as the default after power on, ECC code is generated internally when a page is written to the memory core. The ECC code is stored in the spare area of each page. When a page is read to the cache register, the ECC code is calculated again and compared with the stored value. Errors are corrected if necessary. The device either outputs corrected data or returns an ECC error status. The internal ECC can be configured off after device initialization. Contact Micron representative if ECC is required to be default off after power on.

The first eight blocks are valid when shipped from factory. Security functions are also provided including software block protection: Lock tight and hardware protection modes avoid array data corruption.

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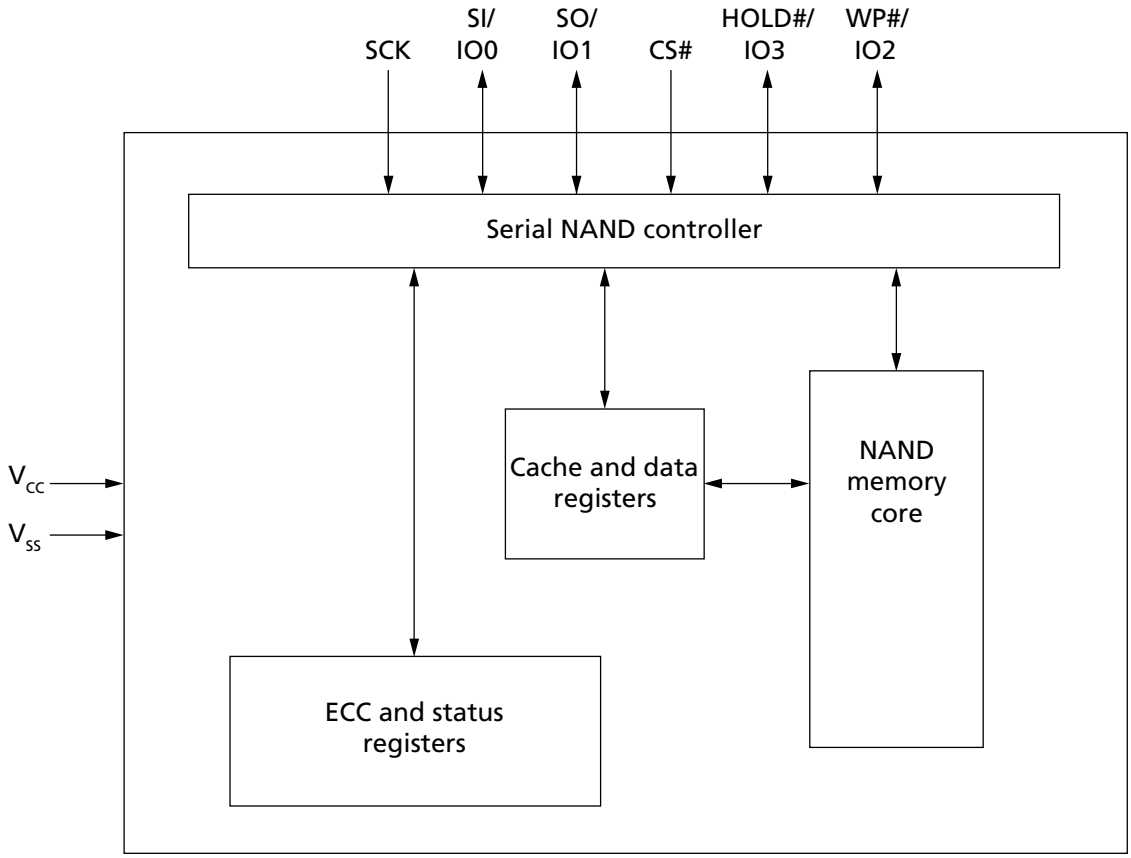
Architecture

The devices use an industry-standard NAND Flash memory core organized by page/block. The standard parallel NAND Flash electrical interface and I/O logic are replaced by an SPI interface. The new command protocol set is a modification of the SPI NOR command set available in the industry. The modifications are specifically to handle functions related to NAND Flash architecture. The interface supports page and random read/write and internal data move functions. The device also includes an internal ECC feature.

Data is transferred to or from the NAND Flash memory array, page-by-page, to a cache register and a data register. The cache register is closest to I/O control circuits and acts as a data buffer for the I/O data; the data register is closest to the memory array and acts as a data buffer for the NAND Flash memory array operation.

The NAND Flash memory array is programmed and read in page-based operations; it is erased in block-based operations. The cache register functions as the buffer memory to enable random data READ/WRITE operations. These devices also use a new SPI status register that reports the status of device operation.

Figure 2: Functional Block Diagram



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Pin Assignments

Figure 3: 8-Pin, U-PDFN (Top View)

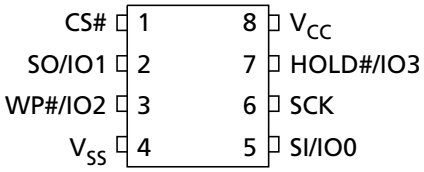


Figure 4: 16-Pin, SOP2 (Top View)

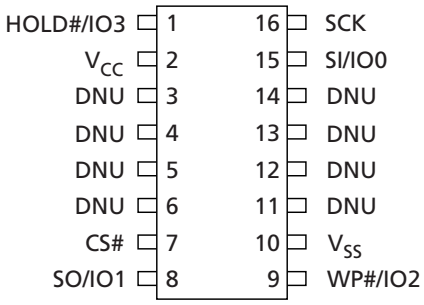
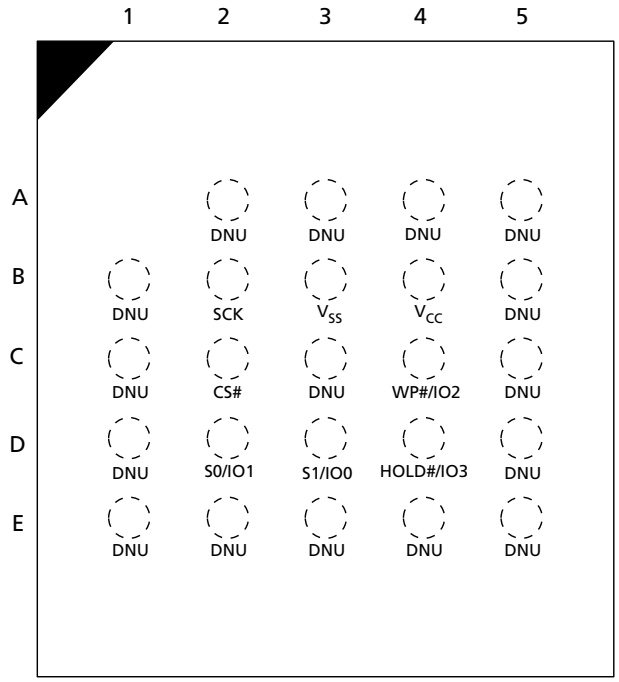


Figure 5: 24-Ball T-PBGA, 5 x 5 (Balls Down)



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Pin Descriptions

Table 1: SPI Pin Descriptions

Symbol	Type	Description
CS#	Input	**Chip select:** Places the device in active power mode when driven LOW. Deselects the device and places SO at High-Z when HIGH. After power-up, the device requires a falling edge on CS# before any command can be written. The device goes into standby mode when no PROGRAM, ERASE, or WRITE STATUS REGISTER operation is in progress. In the case of write-type instructions, CS# must be driven HIGH after a whole sequence is completed. Single command and address sequences and array-based operations are registered on CS#.
SCK	Input	**Serial clock:** Provides serial interface timing. Latches commands, addresses, and data on SI on the rising edge of SCK. Triggers output on SO after the falling edge of SCK. While CS# is HIGH, keep SCK at VCC or GND (determined by mode 0 or mode 3). Do not toggle SCK until CS# is driven LOW.
WP#	Input	**Write protect:** When LOW, prevents overwriting block lock bits (BP[3:0] and TB) if the block register write disable (BRWD) bit is set. WP# must not be driven by the host during a x4 READ operation. If the device is deselected, this pin defaults as an input pin.
HOLD#	Input	**Hold:** Hold functionality is disabled by default except the special part numbers. Contact Micron Sales representatives for details. When enabled, the external pull-up resistor is necessary to avoid accidental operation being placed on hold. HOLD# pauses any serial communication with the device without deselecting it. To start the HOLD condition, the device must be selected, with CS# driven LOW. During HOLD status (HOLD# driven LOW), SO is High-Z and all inputs at SI and SCK are ignored. Hold mode starts at the falling edge of HOLD#, provided SCK is also LOW. If SCK is HIGH when HOLD# goes LOW, hold mode is kicked off at the next falling edge of SCK. Similarly, hold mode is exited at the rising edge of HOLD#, provided SCK is also LOW. If SCK is HIGH, hold mode ends after the next falling edge of SCK. HOLD# must not be driven by the host during the x4 READ operation.
SI/IO0, SO/IO1, IO2, IO3	I/O	**Serial I/O:** The bidirectional I/O signals transfer address, data, and command information. The device latches commands, addresses, and data on the rising edge of SCK, and data is shifted out on the falling edge of the SCK. If the device is deselected, IO[0,2] defaults as an input pin and IO[1,3] defaults as an output pin. SI must not be driven by the host during x2 or x4 READ operations.
V_{CC}	Supply	**V_{CC}:** Supply voltage
V_{SS}	Supply	**V_{SS}:** Ground
DNU	–	**Do not use:** Must be left floating.
NC	–	**No Connect:** Not internal connection; can be driven or floated.

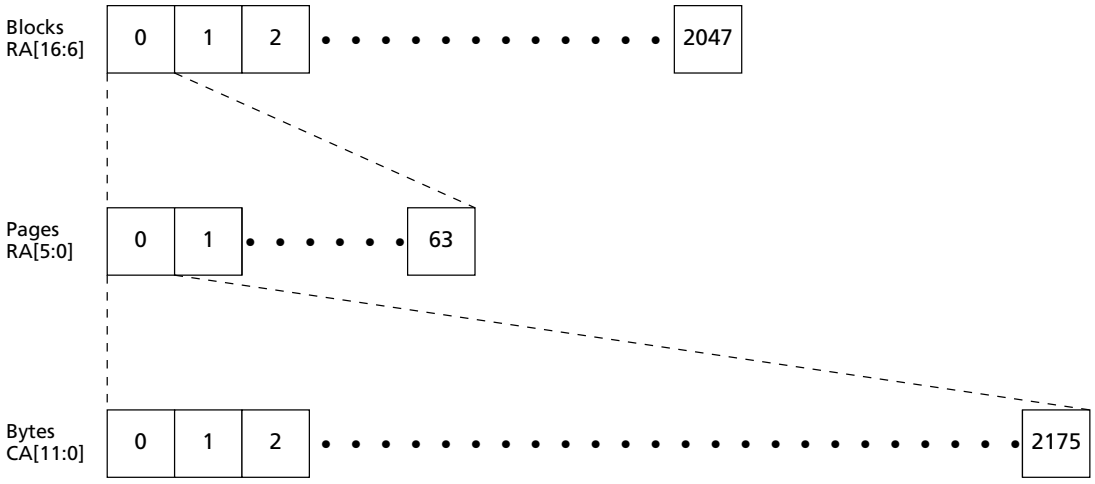
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Memory Mapping

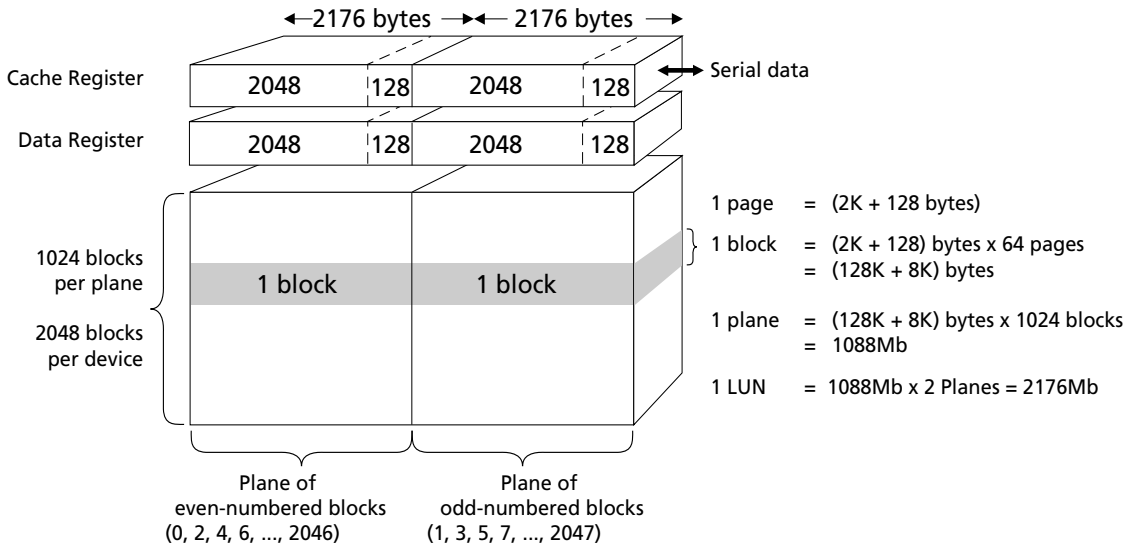
Figure 6: Memory Map



Notes:
1. The 12-bit column address is capable of addressing from 0 to 4095 bytes; however, only bytes 0 through 2175 are valid. Bytes 2176 through 4095 of each page are "out of bounds," do not exist in the device, and cannot be addressed.
2. Block RA6 controls the plane selection.

Array Organization

Figure 7: Array Organization



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Bus Operation

SPI Modes

The device can be driven by a microcontroller with its SPI running in either of two modes depending on clock polarity (CPOL) and clock phase (CPHA) settings:

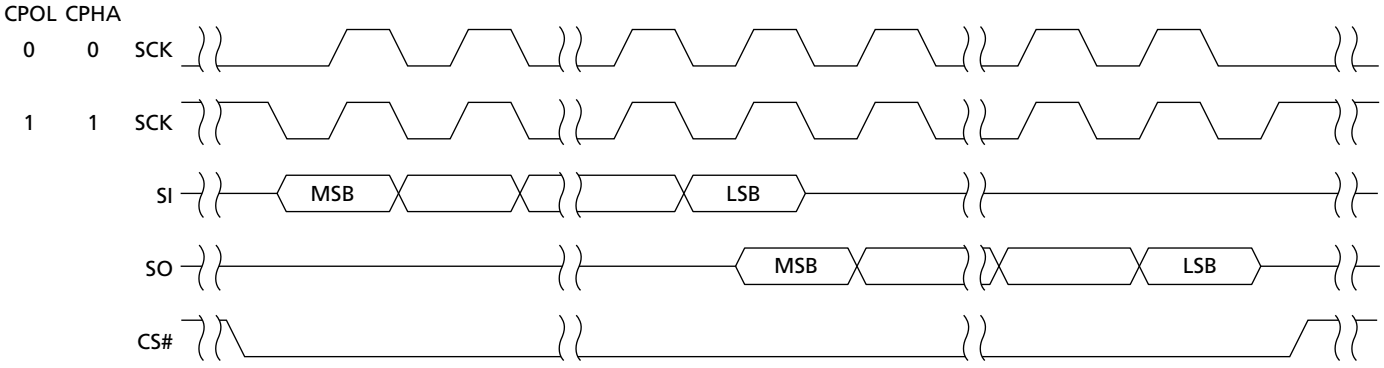
- CPOL = 0, CPHA = 0 (Mode 0)
- CPOL = 1, CPHA = 1 (Mode 3)

Input data is latched in on the rising edge of SCK, and output data is available from the falling edge of SCK for both modes.

The difference between the two modes, shown here, is the clock polarity when the bus master is in standby mode and not transferring data.

- SCK remains at 0 for CPOL = 0, CPHA = 0 (Mode 0)
- SCK remains at 1 for CPOL = 1, CPHA = 1 (Mode 3)

Figure 8: SPI Modes Timing



Notes:
1. While CS# is HIGH, keep SCK at V_{CC} or GND (determined by mode 0 or mode 3). Do not begin toggling SCK until after CS# is driven LOW.
2. All timing diagrams shown in this data sheet are mode 0.

SPI Protocols

Standard SPI: Command, address, and data are transmitted on a single data line. Input on SI is latched in on the rising edge of SCK. Output on SO is available on the falling edge of SCK.

Extended SPI: An extension of the standard SPI protocol. Command and address are transmitted on a single data line through SI. Data are transmitted on two or four data lines, IO[3:0], depending on the command.

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SPI NAND Command Definitions

Table 2: SPI NAND Command Set

Command	Op Code	Address Bytes	Dummy Bytes	Data Bytes	Comments
RESET	FFh	0	0	0	Reset the device
GET FEATURES	0Fh	1	0	1	Get features
SET FEATURES	1Fh	1	0	1	Set features
READ ID	9Fh	0	1	2	Read device ID
PAGE READ	13h	3	0	0	Array read
READ PAGE CACHE RANDOM	30h	3	0	0	Cache read
READ PAGE CACHE LAST	3Fh	0	0	0	Ending of cache read
READ FROM CACHE x1	03h, 0Bh	2	1	1 to 2176	Output cache data at column address
READ FROM CACHE x2	3Bh	2	1	1 to 2176	Output cache data on IO[1:0]
READ FROM CACHE x4	6Bh	2	1	1 to 2176	Output cache data on IO[3:0]
READ FROM CACHE Dual IO	BBh	2	1	1 to 2176	Input address/Output cache data on IO[1:0]
READ FROM CACHE Quad IO	EBh	2	2	1 to 2176	Input address/Output cache data on IO[3:0]
WRITE ENABLE	06h	0	0	0	Sets the WEL bit in the status register to 1; required to enable operations that change the content of the memory array
WRITE DISABLE	04h	0	0	0	Clears the WEL bit in the status register to 0; required to disable operations that change the content of the memory array
BLOCK ERASE	D8h	3	0	0	Block erase
PROGRAM EXECUTE	10h	3	0	0	Array program
PROGRAM LOAD x1	02h	2	0	1 to 2176	Load program data into cache register on SI
PROGRAM LOAD x4	32h	2	0	1 to 2176	Load program data into cache register on SO[3:0]
PROGRAM LOAD RANDOM DATA x1	84h	2	0	1 to 2176	Overwrite cache register with input data on SI
PROGRAM LOAD RANDOM DATA x4	34h	2	0	1 to 2176	Overwrite cache register with input data on SO[3:0]
PERMANENT BLOCK LOCK PROTECTION	2Ch	3	0	0	Permanently protect a specific group of blocks

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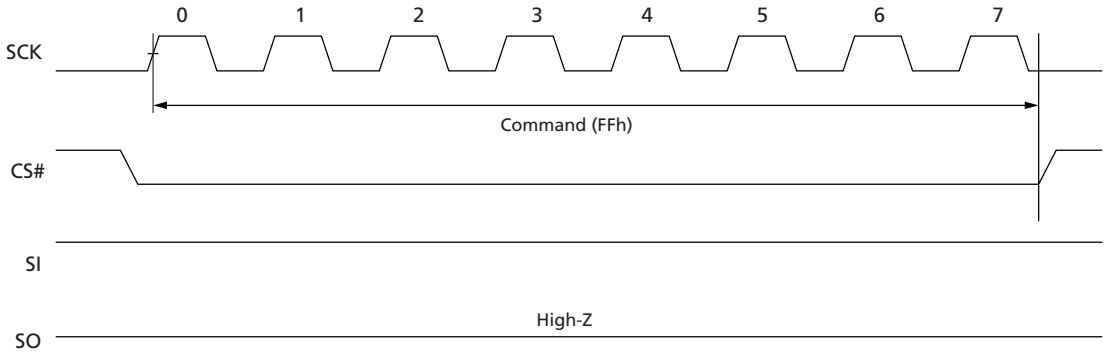
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RESET Operation

The RESET command (FFh) is used to put the memory device into a known condition and to abort the command sequence in progress. READ, PROGRAM, and ERASE commands can be aborted while the device is in the busy state. Once the RESET command is issued to the device, it will take t_{POR} to reset. During this period, the GET FEATURE command could be issued to monitor the status (OIP) except for 4Gb stacked device. For 4Gb stacked device, no command should be issued until t_{POR}. The contents of the memory location being programmed or the block being erased are no longer valid. The first page data of the first block is auto-loaded to the cache register.

All other status register bits will be cleared. The ECC status register bits will be updated after a reset. The configuration register bits CFG[2:0] will be cleared after a reset. All the other configuration register bits will not be reset. The block lock register bits will not be cleared after reset until the device is power cycled or is written to by SET FEATURE command.

Figure 9: RESET (FFh) Timing



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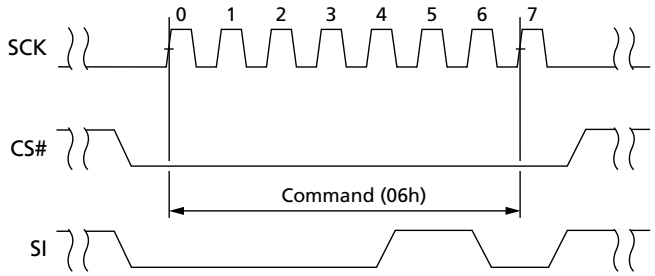
WRITE Operations

WRITE ENABLE (06h)

The WRITE ENABLE (06h) command sets the WEL bit in the status register to 1. Write enable is required in the following operations that change the contents of the memory array:

- PAGE PROGRAM
- OTP AREA PROGRAM
- BLOCK ERASE

Figure 10: WRITE ENABLE (06h) Timing

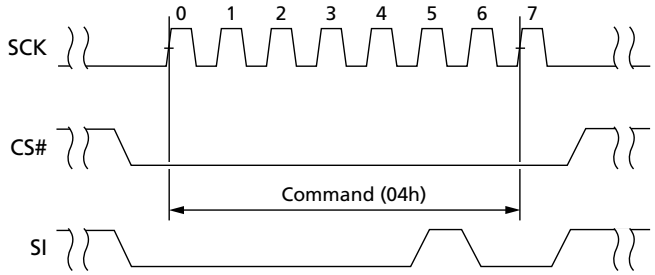


WRITE DISABLE (04h)

The WRITE DISABLE (04h) command clears the WEL bit in the status register to 0, disabling the following operations:

- PAGE PROGRAM
- OTP AREA PROGRAM
- BLOCK ERASE

Figure 11: WRITE DISABLE (04h) Timing



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READ Operations

PAGE READ (13h)

The PAGE READ (13h) command transfers data from the NAND Flash array to the cache register. It requires a 24-bit address consisting of 7 dummy bits and a 17-bit block/page address (8 dummy bits followed by an 16-bit block/page address for 1Gb). After the block/page address is registered, the device starts the transfer from the main array to the cache register. During this data transfer busy time of ^{t}RD, the GET FEATURES command can be issued to monitor the operation.

Following successful completion of PAGE READ, the READ FROM CACHE command must be issued to read data out of cache. The command sequence is as follows to transfer data from array to output:

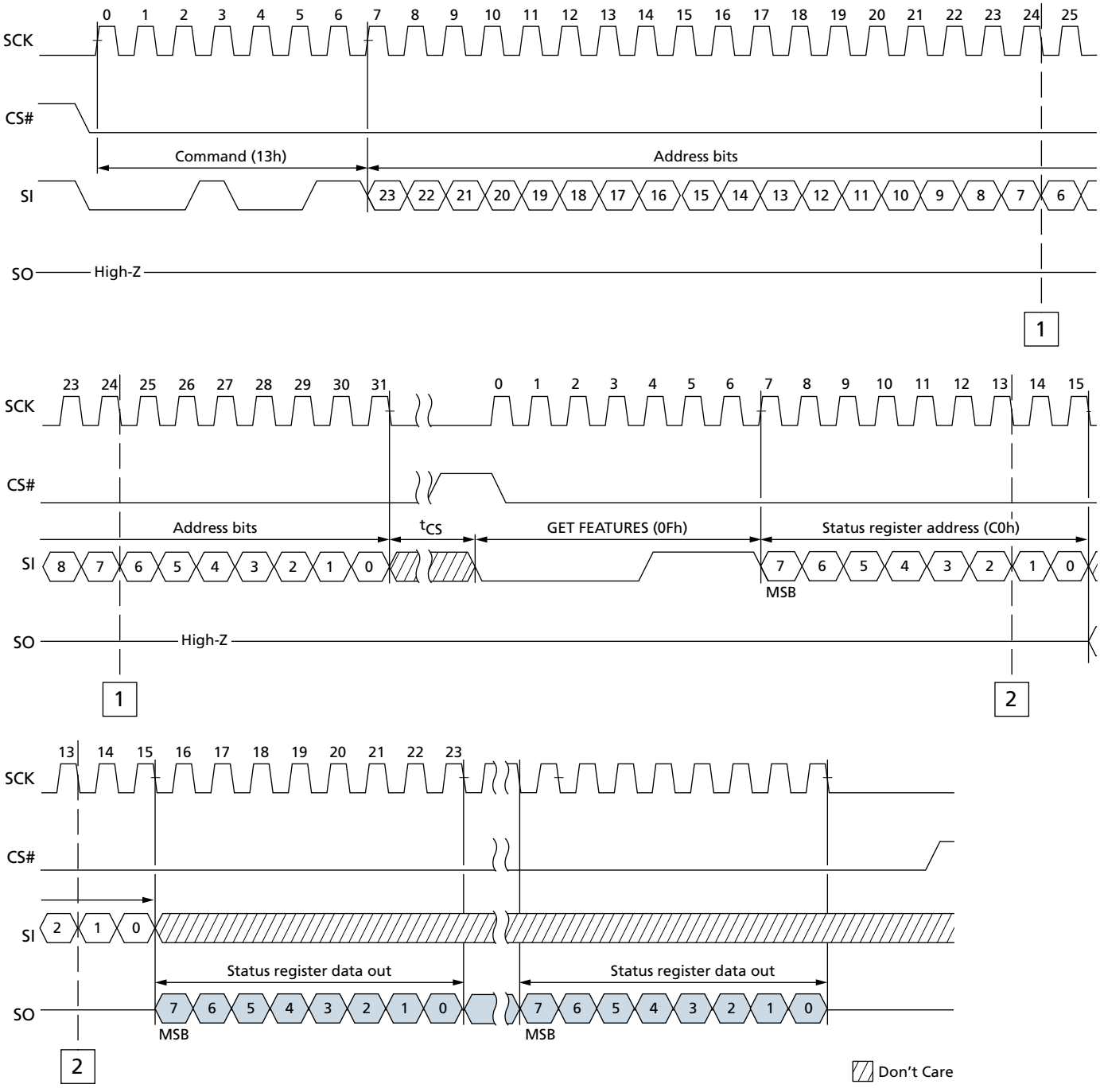
- 13h (PAGE READ command to cache)
- 0Fh (GET FEATURES command to read the status)
- 03h or 0Bh (READ FROM CACHE)
- 3Bh (READ FROM CACHE x2)
- 6Bh (READ FROM CACHE x4)
- BBh (READ FROM CACHE Dual I/O)
- EBh (READ FROM CACHE Quad I/O)

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Figure 12: PAGE READ (13h) Timing



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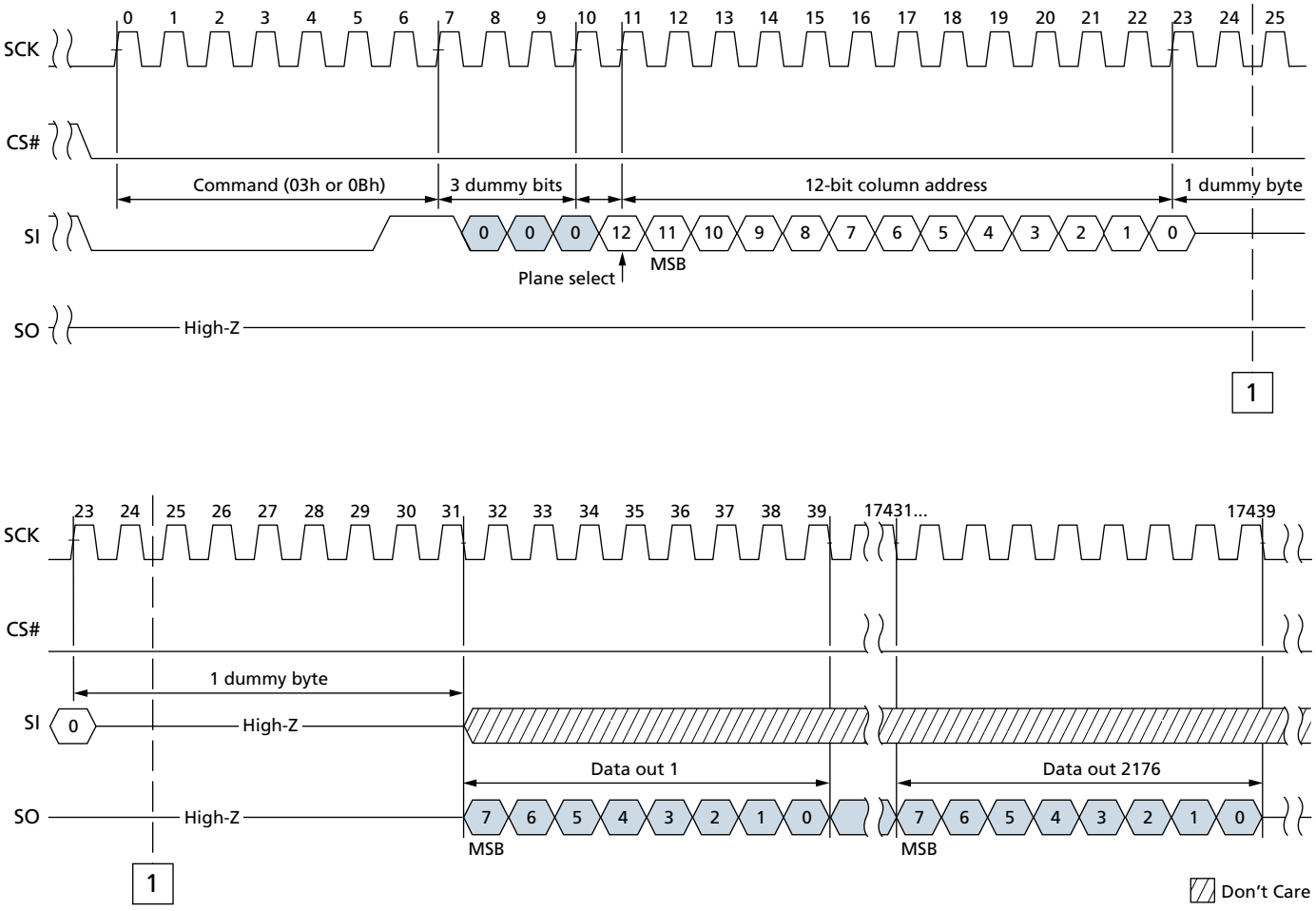
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READ FROM CACHE x1 (03h or 0Bh)

The READ FROM CACHE x1 command enables sequentially reading one or more data bytes from the cache buffer. The command is initiated by driving CS# LOW, shifting in command opcode 03h/0Bh, followed by a 16 bit column address and 8-bit dummy clocks. Both the commands run at fast mode.

Data is returned from the addressed cache buffer, MSB first, on SO at the falling edge of SCK. The address is automatically incremented to the next higher address after each byte of data is shifted out, enabling a continuous stream of data. This command is completed by driving CS# HIGH.

Figure 13: READ FROM CACHE (03h or 0Bh) Timing



Note: 1. Plane select is a dummy bit for 1Gb devices.

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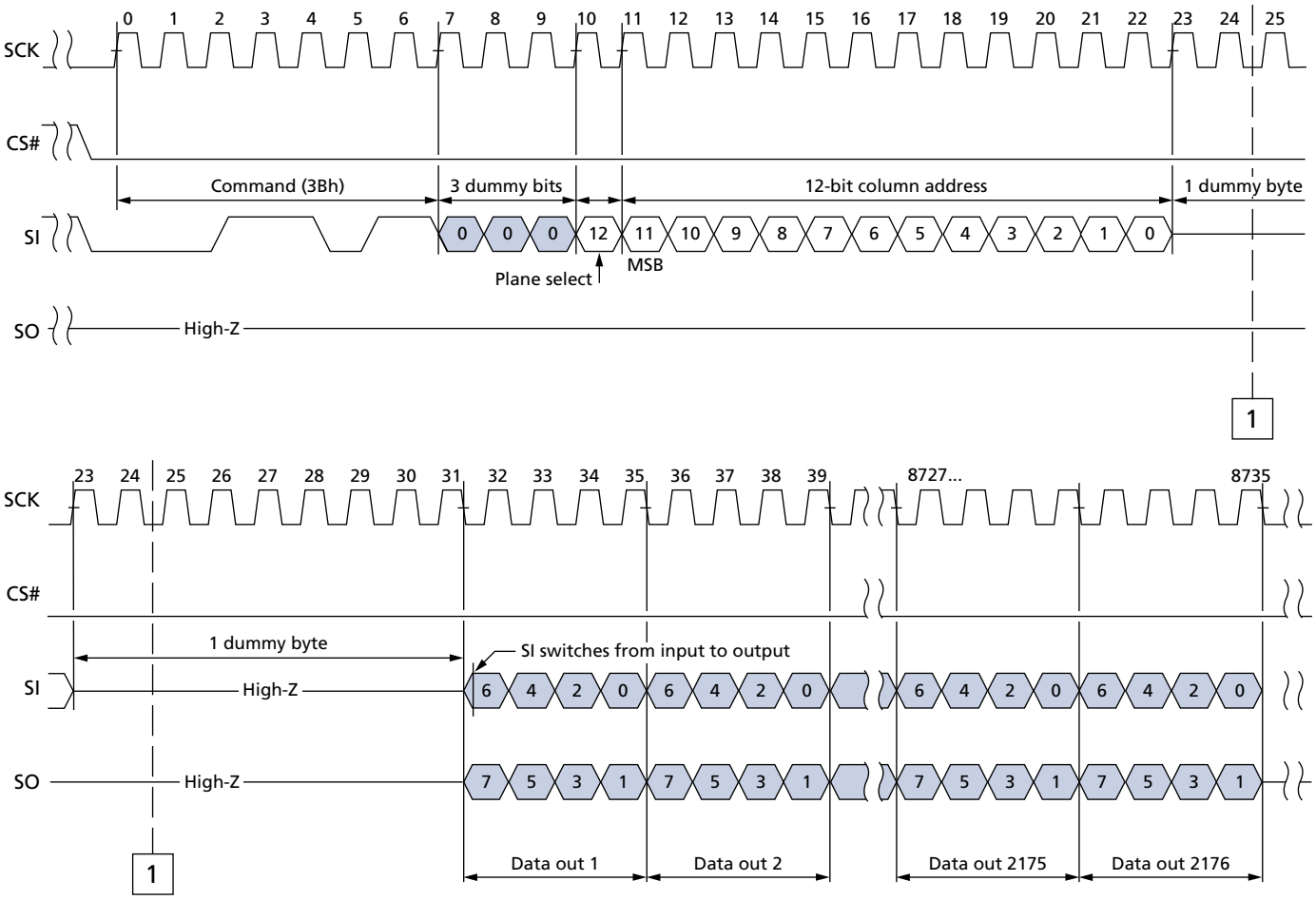
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READ FROM CACHE x2 (3Bh)

The READ FROM CACHE x2 (3Bh) command is similar to READ FROM CACHE x1 (03h or 0Bh) except that data is output on the following two pins, enabling data transfer at twice the rate: IO0(SI) and IO1(SO).

Figure 14: READ FROM CACHE x2



Note: 1. Plane select is a dummy bit for 1Gb devices.

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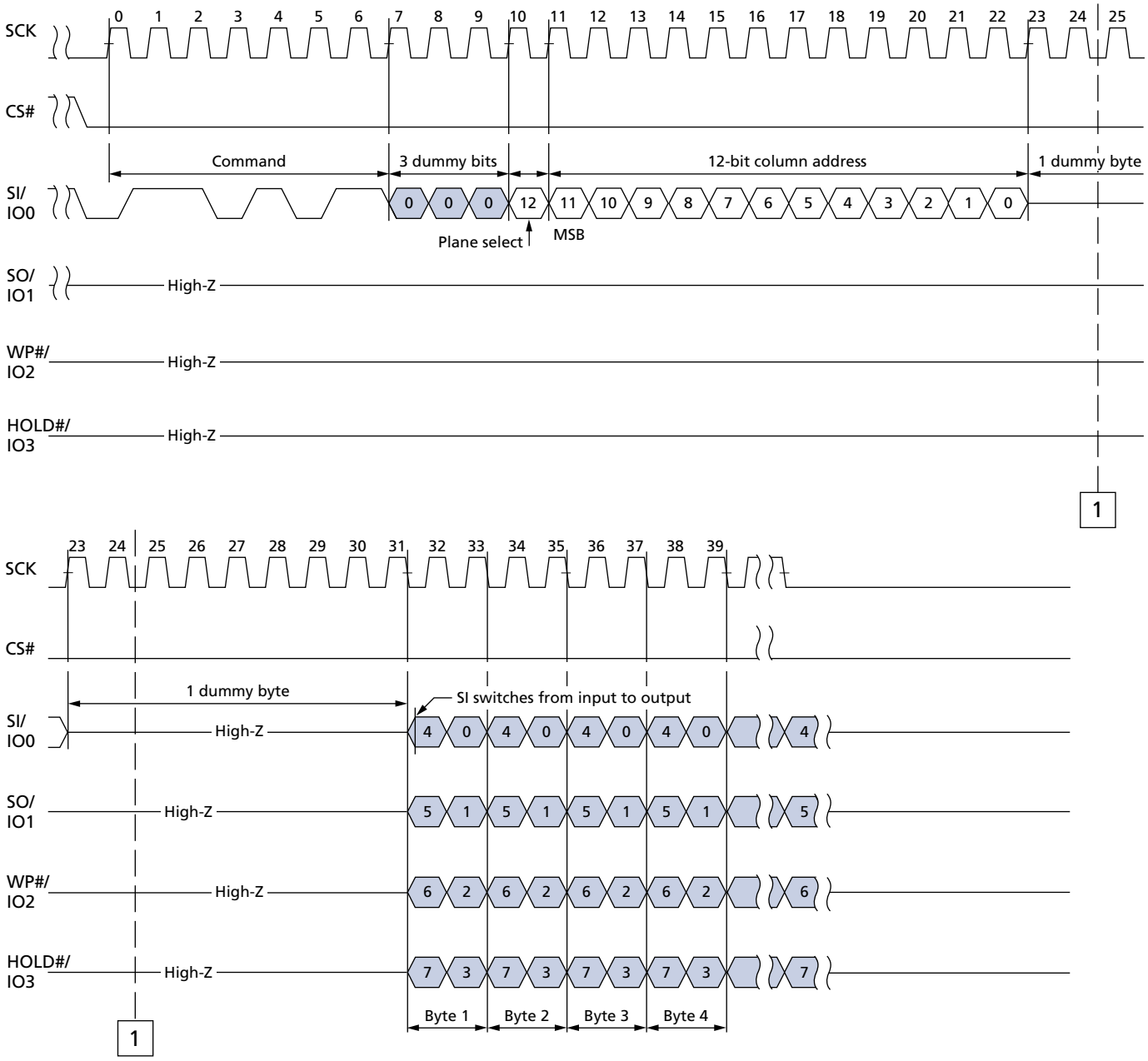
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READ FROM CACHE x4 (6Bh)

The READ FROM CACHE x4 (6Bh) command is similar to READ FROM CACHE x1 command, but with the capability to output data across four data lines.

Figure 15: READ FROM CACHE x4



Note: 1. Plane select is a dummy bit for 1Gb devices.

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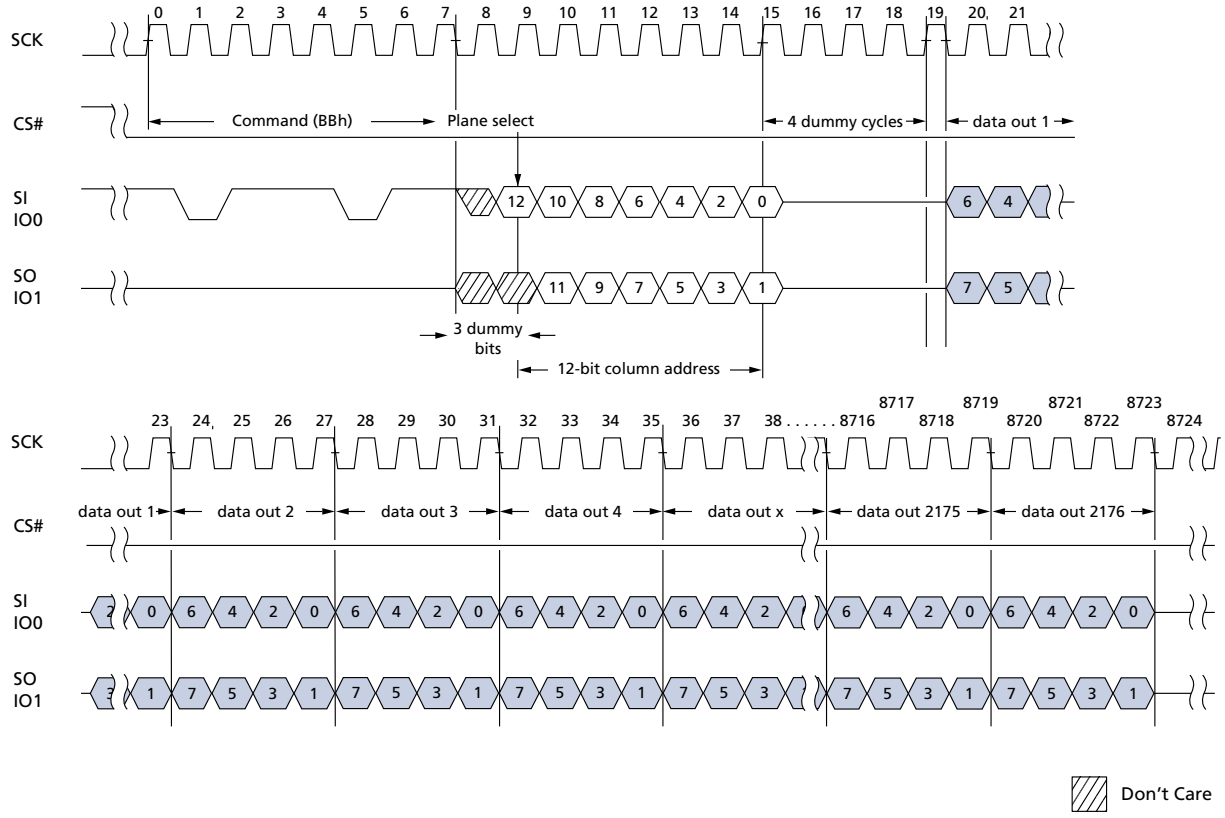
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READ FROM CACHE Dual I/O (BBh)

The READ FROM CACHE Dual IO (BBh) command enables improved random access while maintaining two IO pins, IO0 and IO1. It is similar to the READ FROM CACHE x2 (3Bh) command but with capability to input either the column address or the dummy clocks two bits per clock, thereby reducing command overhead. Refer to the Electrical Specifications for the supported frequency.

Figure 16: READ FROM CACHE Dual I/O



Note: 1. Plane select is a dummy bit for 1Gb devices.

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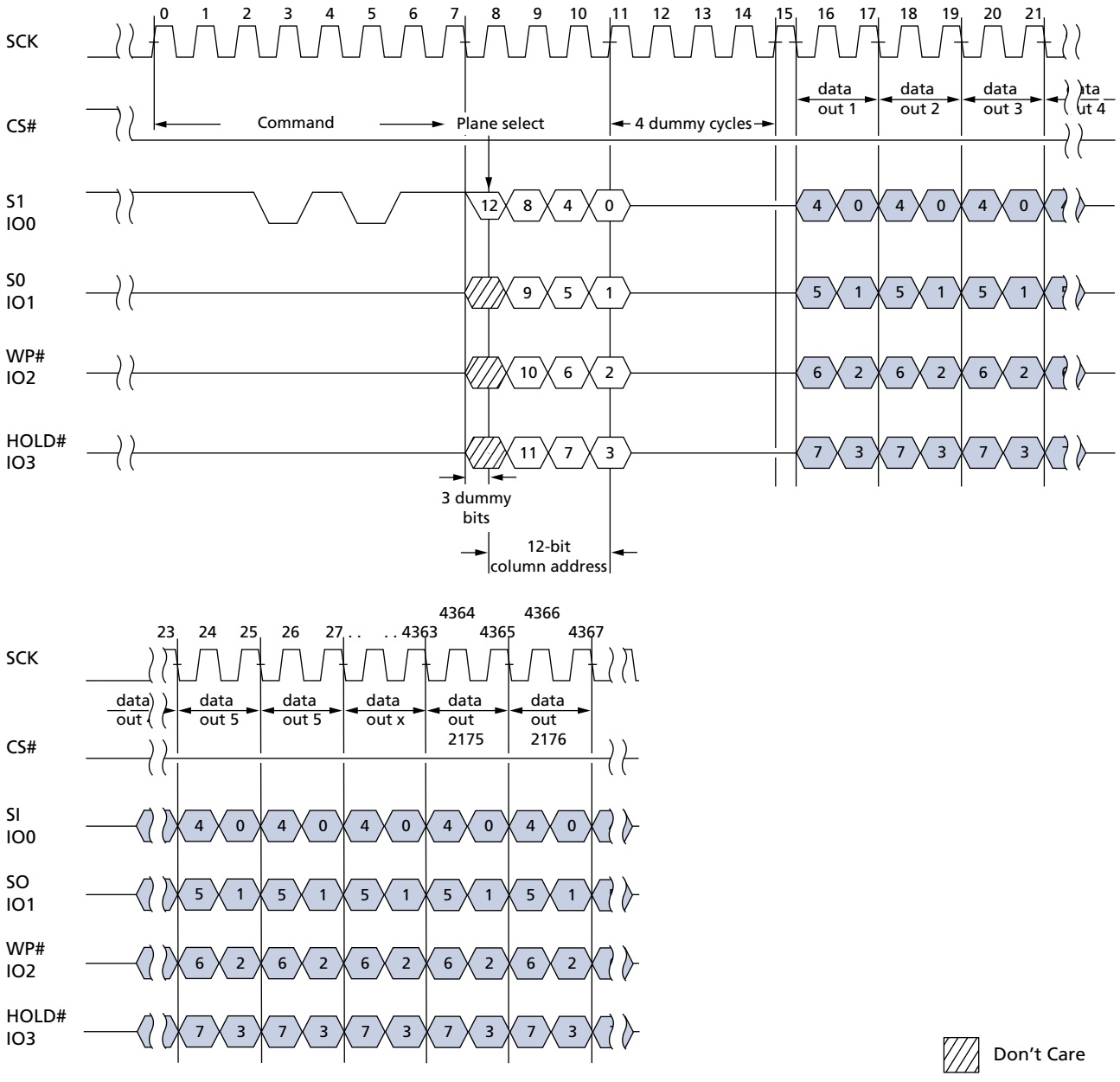
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READ FROM CACHE Quad I/O (EBh)

The READ FROM CACHE Quad I/O (EBh) command is similar to the READ FROM CACHE Dual I/O (BBh) command except that address and data bits are input and output through four pins: IO0, IO1, IO2, and IO3. The quad IO dramatically reduces command overhead, enabling faster random access to the cache buffer. Refer to the Electrical Specifications for the supported frequency.

Figure 17: READ FROM CACHE Quad I/O



Note: 1. Plane select is a dummy bit for 1Gb devices.

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READ PAGE CACHE RANDOM (30h)

The READ PAGE CACHE RANDOM (30h) command reads the specified block and page into the data register while the previous page is output from the cache register. This command is accepted by the die when it is ready (OIP = 0, CRBSY = 0). This command is used to improve the read throughput as follows:

1. 13h – PAGE READ to cache
2. 0Fh – GET FEATURE command to the read status until OIP status bit is changed from 1 to 0
3. 30h – READ PAGE CACHE RANDOM command to transfer data from data register to cache register and kick off the next page transfer from array to data register
4. 0Fh – GET FEATURE command to read the status until OIP status bit is changed from 1 to 0
5. 03h, 0Bh, 3Bh, 6Bh, BBh, or EBh – READ FROM CACHE TO OUTPUT command
6. 0Fh – GET FEATURE command to read the status until CRBSY = 0
7. Repeat step 3 to step 6 to read out all expected pages until last page
8. 3Fh – READ PAGE CACHE LAST command to end the read page cache sequence and copy a last page from the data register to the cache register
9. 0Fh – GET FEATURE command to read the status until OIP status bit is changed from 1 to 0
10. 03h, 0Bh, 3Bh, 6Bh, BBh, or EBh – READ FROM CACHE TO OUTPUT command to read out last page from cache register to output

The READ PAGE CACHE RANDOM command requires a 24 bit address consisting of 8 dummy bits followed by a 16-bit block/page address for 1Gb device or 7 dummy bits followed by a 17-bit block/page address for 2Gb or higher devices. After the block/page addresses are registered, the device starts to transfer data from data register to cache register for ^{t}RCBSY. After ^{t}RCBSY, OIP bit (through GET FEATURE command to check this status bit) goes to 0 from 1, indicating that the cache register is available and that the specified page in the READ PAGE CACHE RANDOM command is copying from the the Flash array to the data register. At this point, data can be output from the cache register beginning at the column address specified by READ FROM CACHE commands. The status register CRBSY bit value remains at 1, indicating that the specified page in READ PAGE CACHE RANDOM command is copying from the Flash array to the data register; CRBSY returns to 0 to indicating the copying from array is completed. During ^{t}RCBSY, the error check and correction is also performed.

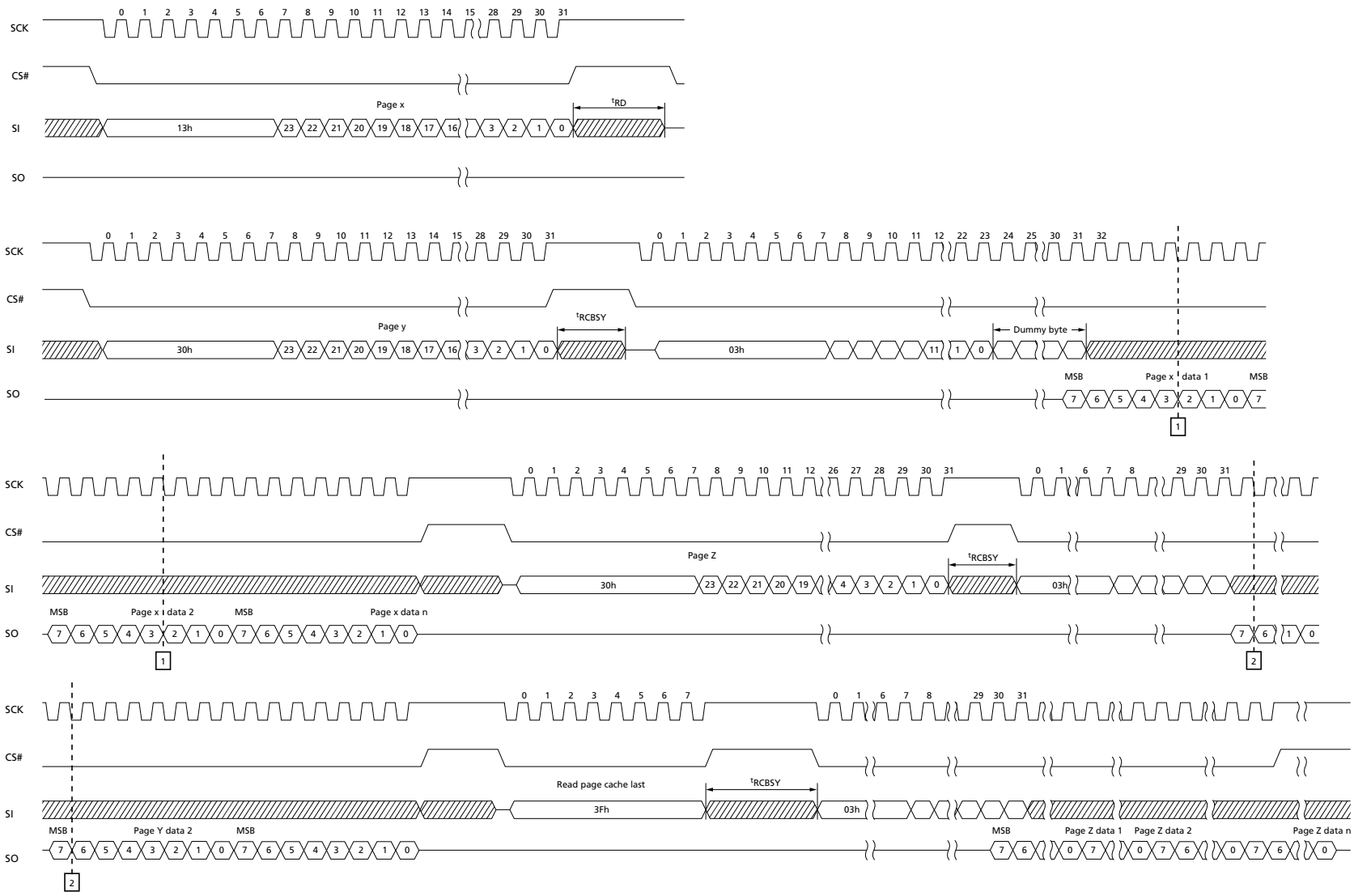
Note: With an on-die ECC-enabled die, ECC is executed after data is transferred from the data register to the cache register; therefore, ^{t}RCBSY includes this ECC time, which must be factored in when checking the OIP status.

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Figure 18: READ PAGE CACHE RANDOM Sequence



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READ PAGE CACHE LAST (3Fh)

The READ PAGE CACHE LAST (3Fh) command ends the READ PAGE CACHE RANDOM sequence and copies a page from the data register to the cache register. This command is accepted by the die when it is ready (OIP = 0, CRBSY = 0). After this command is issued, the status register bit OIP goes HIGH and the device is busy (CRBSY = 0, OIP = 1) for ^{t}RCBSY. Address is not applied in this command sequence. When data is completely copied to cache register, OIP goes LOW and READ FROM CACHE commands could be issued to output data.

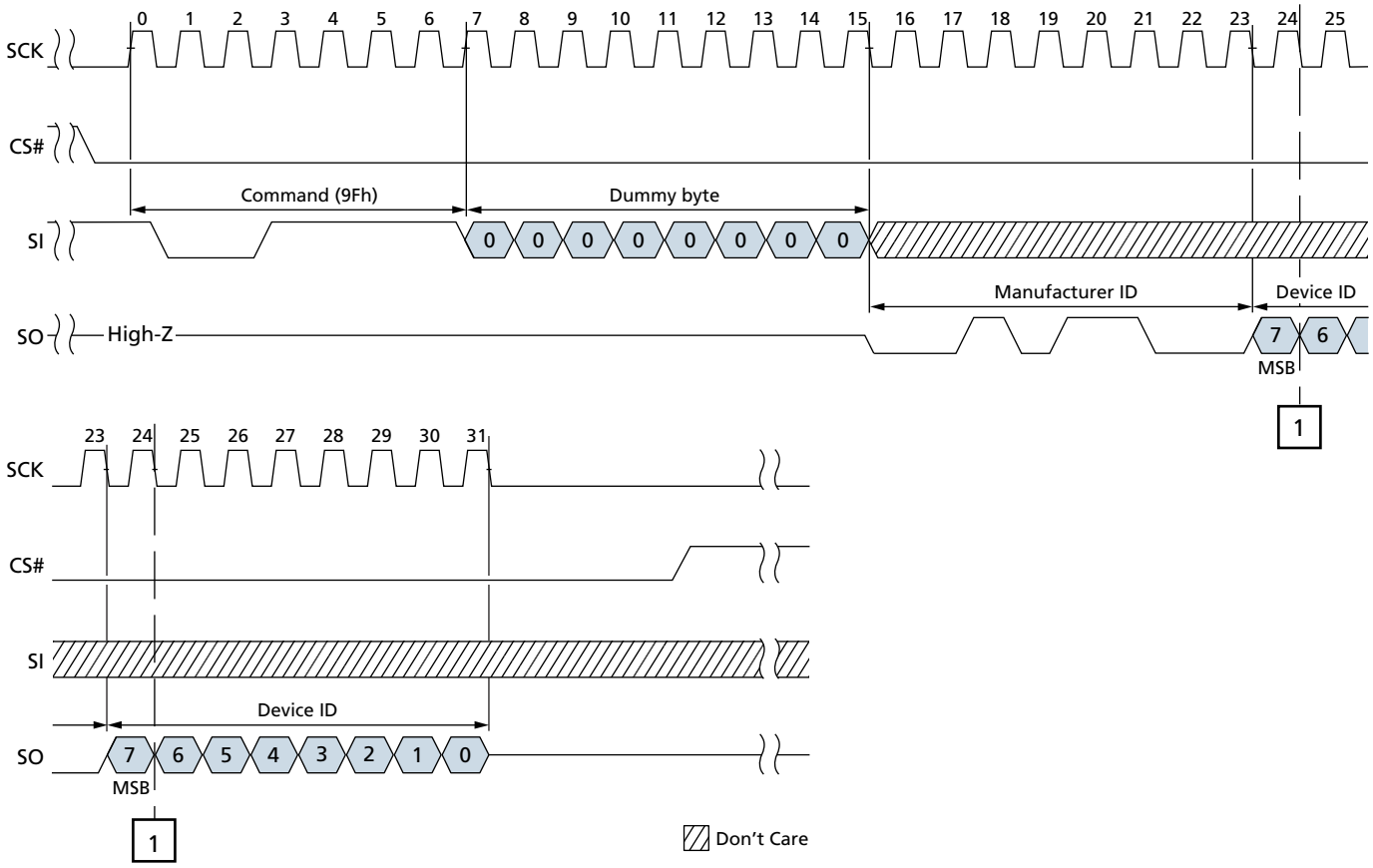
READ ID (9Fh)

READ ID reads the 2-byte identifier code programmed into the device, which includes ID and device configuration data as shown in the table below.

Table 3: READ ID Table

Byte	Description	7	6	5	4	3	2	1	0	Value
Byte 0	Manufacturer ID (Micron)	0	0	1	0	1	1	0	0	2Ch
Byte 1	2Gb 3.3V Device ID	0	0	1	0	0	1	0	0	24h

Figure 19: READ ID (9Fh) Timing



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Parameter Page

The following command flow must be issued by the memory controller to access the parameter page contained within Micron SPI devices:

1. 1Fh – SET FEATURES command with a feature address of B0h and data value for CFG[2:0] = 010b (to access OTP/Parameter/UniqueID pages).
2. 13h – PAGE READ command with a block/page address of 0x01h, and then check the status of the read completion using the GET FEATUR ES (0Fh) command with a feature address of C0h.
3. 03h – READ FROM CACHE command with an address of 0x00h to read the data out of the NAND device (see the following Parameter Page Data Structure table for a description of the contents of the parameter page.)
4. 1Fh – SET FEATURES command with a feature address of B0h and data value of 00h to exit the parameter page reading.

Parameter Page Data Structure Table

Table 4: Parameter Table

Byte	Description	Value (hex)
0-3	Parameter page signature	4Fh, 4Eh, 46h, 49h
4-5	Revision number	00h
6-7	Feature support	00h
8-9	Optional commands support	06h, 00h
10-31	Reserved	00h
32-43	Device manufacturer	4Dh, 49h, 43h, 52h, 4Fh, 4Eh, 20h, 20h, 20h, 20h, 20h, 20h
44-63	Device model: MT29F2G01ABAGDSF	4Dh, 54h, 32h, 39h, 46h, 32h, 47h, 30h, 31h, 41h, 42h, 41h, 47h, 44h, 53h, 46h, 20h, 20h, 20h, 20h
44-63	Device model: MT29F2G01ABAGD12	4Dh, 54h, 32h, 39h, 46h, 32h, 47h, 30h, 31h, 41h, 42h, 41h, 47h, 44h, 31h, 32h, 20h, 20h, 20h, 20h
44-63	Device model: MT29F2G01ABAGDWB	4Dh, 54h, 32h, 39h, 46h, 32h, 47h, 30h, 31h, 41h, 42h, 41h, 47h, 44h, 57h, 42h, 20h, 20h, 20h, 20h
64	Manufacturer ID	2Ch
65-66	Date code	00h
67-79	Reserved	00h
80-83	Number of data bytes per page	00h, 08h, 00h, 00h
84-85	Number of spare bytes per page	80h, 00h
86-89	Number of data bytes per partial page	00h, 02h, 00h, 00h
90-91	Number of spare bytes per partial page	20h, 00h
92-95	Number of pages per block	40h, 00h, 00h, 00h
96-99	Number of blocks per unit	00h, 08h, 00h, 00h
100	Number of logical units	01h
101	Number of address cycles	00h
102	Number of bits per cell	01h
103-104	Bad blocks maximum per unit	28h, 00h

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Table 4: Parameter Table (Continued)

Byte	Description	Value (hex)
105-106	Block endurance	01h, 05h
107	Guaranteed valid blocks at beginning of target	08h
108-109	Block endurance for guaranteed valid blocks	00h
110	Number of programs per page	04h
111	Partial programming attributes	00h
112	Number of ECC bits	00h
113	Number of interleaved address bits	00h
114	Interleaved operation attributes	00h
115-127	Reserved	00h
128	I/O pin capacitance	08h
129-130	Timing mode support	00h
131-132	Program cache timing	00h
133-134	^{t}PROG maximum page program time	58h, 02h
135-136	^{t}ERS maximum block erase time	10h, 27h
137-138	^{t}R maximum page read time	46h, 00h
139-140	^{t}CCS minimum	00h
141-163	Reserved	00h
164-165	Vendor-specific revision number	00h
166-179	Vendor specific	01h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 02h, 02h, B0h, 0Ah, B0h
180-247	Reserved	00h
248	ECC maximum correct ability	08h
249	Die select feature	00h
250-253	Reserved	00h
254-255	Integrity CRC	Set at Test
256-512	2nd copy of the parameter table	
513-768	3rd copy of the parameter table	
769-2048	Additional redundant parameter pages	

Unique ID Page

The following command flow must be issued by the memory controller to access the unique ID page contained within the device:

1. Issue a SET FEATURES (1Fh) command on a feature address of B0h and data value of 40h (Access to OTP, Parameter, UniqueID pages, ECC disable).
2. Issue a PAGE READ (13h) command on a block/page address of 0x00h, and then poll the status register OIP bit until device ready using the GET FEATURES (0Fh) command issued on a feature address of C0h.

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3. Issue a READ FROM CACHE (03h) command on an address of 0x00h to read the unique ID data out of the NAND device.
4. To exit reading the uniqueID page, issue a SET FEATURES (1Fh) command with a feature address of B0h and data value of 10h or 00h (main array READ, ECC enable/disable).

The device stores 16 copies of the unique ID data. Each copy is 32 bytes: the first 16 bytes are unique data, and the second 16 bytes are the complement of the first 16 bytes. The host should XOR the first 16 bytes with the second 16 bytes. If the result is 16 bytes of FFh, that copy of the unique ID data is correct. If a non-FFh result is returned, the host can repeat the XOR operation on a subsequent copy of the unique ID data.

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Program Operations

PAGE PROGRAM

A PAGE PROGRAM operation sequence enables the host to input 1 byte to 2176 bytes of data within a page to a cache register, and moves the data from the cache register to the specified block and page address in the array. Only four partial-page programs are allowed on a single page. If more than 2176 bytes are loaded, then those additional bytes are ignored by the cache register.

The page program sequence is as follows:

- 06h (WRITE ENABLE command)
- 02h (PROGRAM LOAD command)
- 10h (PROGRAM EXECUTE command)
- 0Fh (GET FEATURES command to read the status)

PROGRAM LOAD x1 (02h)

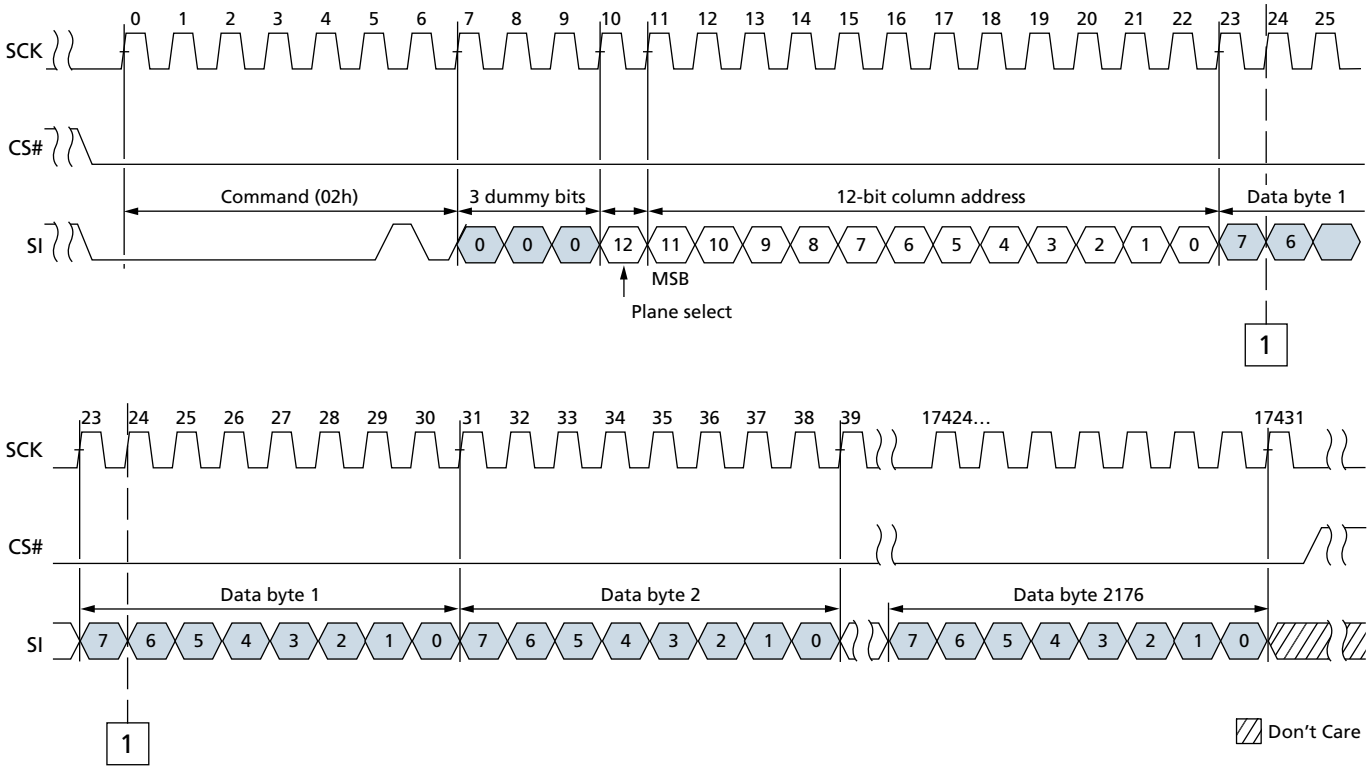
Prior to performing the PROGRAM LOAD operation, a WRITE ENABLE (06h) command must be issued. As with any command that changes the memory contents, the WRITE ENABLE command must be executed in order to set the WEL bit. WRITE ENABLE is followed by a PROGRAM LOAD (02h) command. The PROGRAM LOAD command consists of an 8-bit op code, followed by 3 dummy bits, followed by a plane select (if available) and a 12-bit column address, and then the data bytes to be programmed. The data bytes are loaded into a cache register that is 2176 bytes long. Only four partial-page programs are allowed on a single page. If more than 2176 bytes are loaded, those additional bytes are ignored by the cache register. The command sequence ends when CS# goes from LOW to HIGH.

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Figure 20: PROGRAM LOAD (02h) Timing



Note: 1. Plane select is a dummy bit in 1Gb device.

PROGRAM EXECUTE (10h)

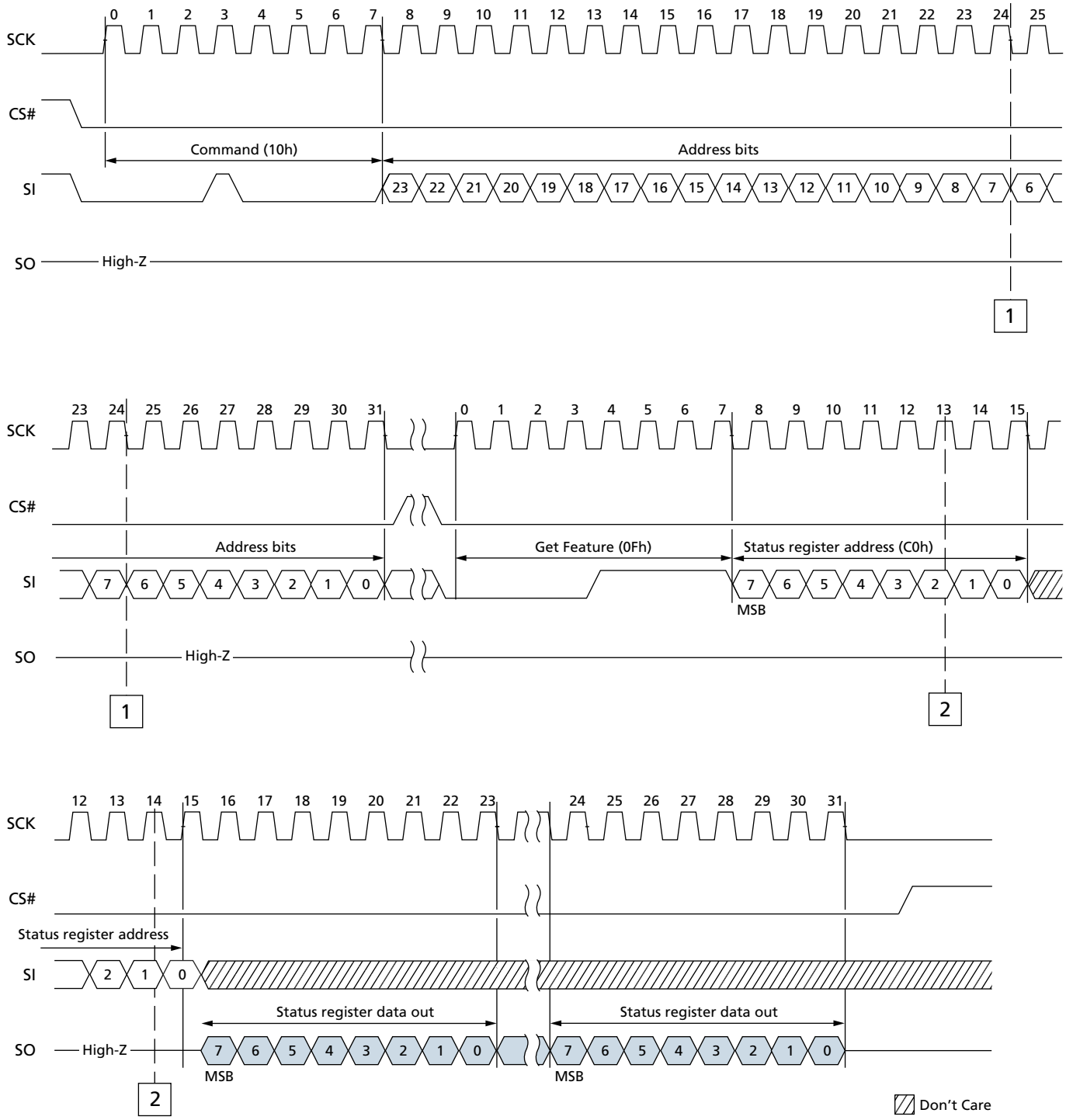
The PROGRAM EXECUTE command consists of an 8-bit op code, followed by a 24-bit address. After the page/block address is registered, the device starts the transfer from the cache register to the main array and is busy for ^{t}PROG time. During this busy time, the status register can be polled to monitor the status of the operation (refer to the status register section). When the operation completes successfully, the next series of data can be loaded with the PROGRAM LOAD command.

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Figure 21: PROGRAM EXECUTE (10h) Timing



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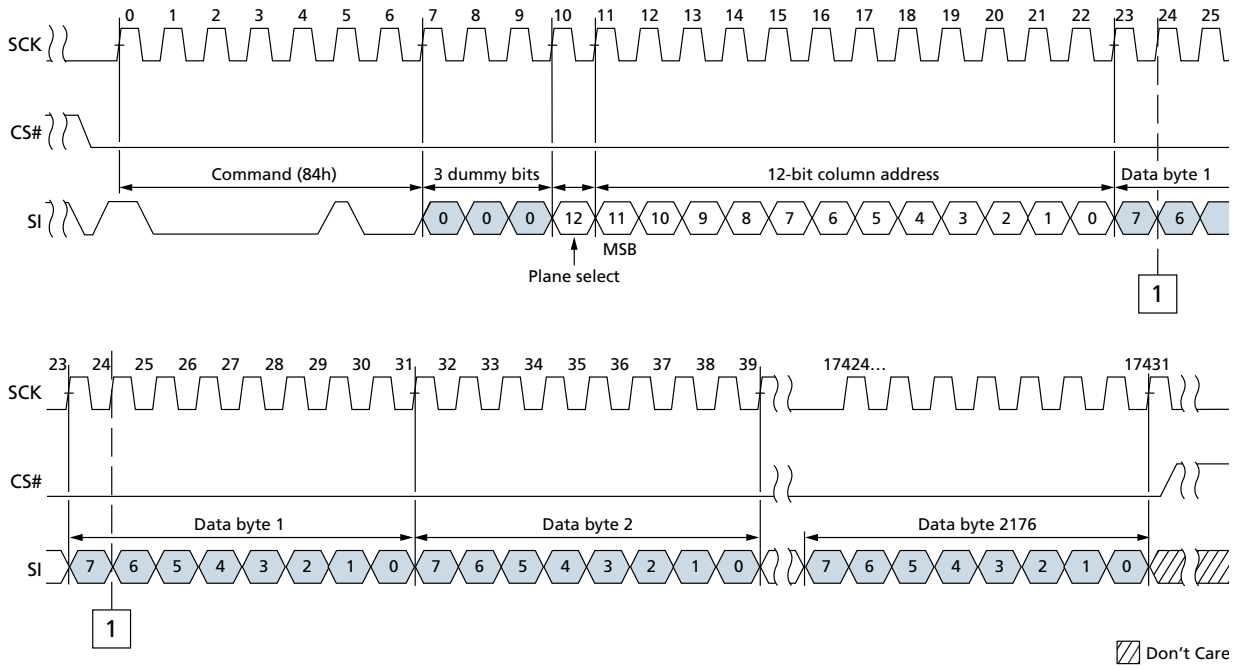
RANDOM DATA PROGRAM x1 (84h)

The RANDOM DATA PROGRAM operation programs or replaces data in a page with existing data. The random data program sequence is as follows:

- 06h (WRITE ENABLE command)
- 84h (PROGRAM LOAD RANDOM DATA command)
- 10h (PROGRAM EXECUTE command)
- 0Fh (GET FEATURES command to read the status)

The PROGRAM LOAD RANDOM DATA x1 (84h) operation is similar to PROGRAM LOAD x1 (02h). The difference is that PROGRAM LOAD X1command will reset the cache buffer to an all FFh value, while PROGRAM LOAD RANDOM DATA X1command will only update the data bytes that are specified by the command input sequence, and the rest of data in the cache buffer will remain unchanged. If the random data is not sequential, then another PROGRAM LOAD RANDOM DATA x1 (84h) command must be issued with a new column address. After the data is loaded, a PROGRAM EXECUTE (10h) command can be issued to start the programming operation.

Figure 22: PROGRAM LOAD RANDOM DATA (84h) Timing



Note: 1. Plane select is a dummy bit in 1Gb device.

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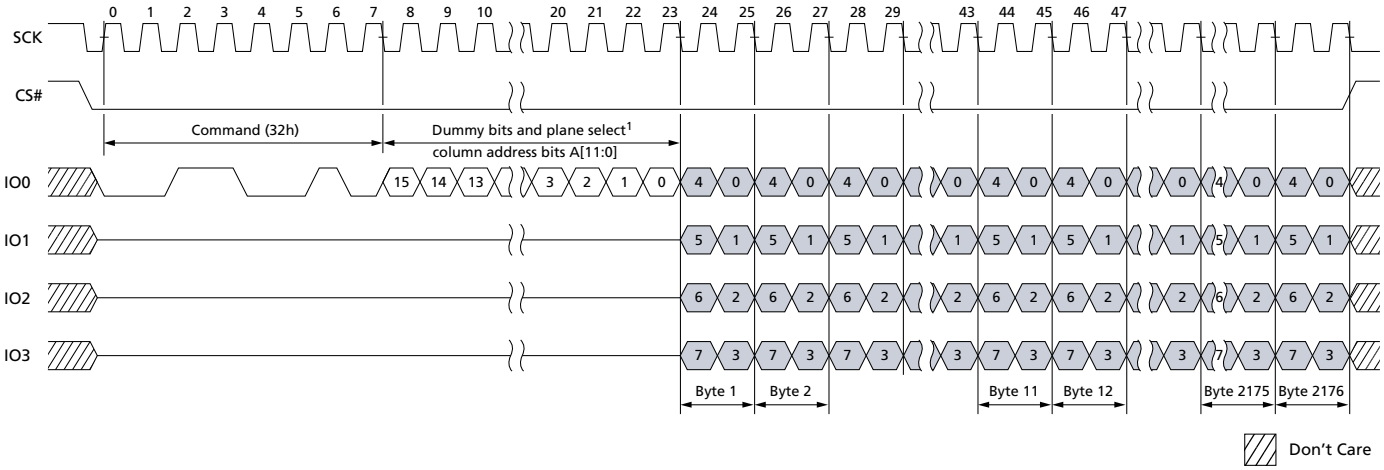
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PROGRAM LOAD x4 (32h) and PROGRAM LOAD RANDOM DATA x4 (34h)

The PROGRAM LOAD x4 (32h) and RANDOM DATA x4 (34h) is similar to PROGRAM LOAD x1 (02h) command and RANDOM DATA x1 (84h), but with the capability to input the data across four data lines.

Figure 23: PROGRAM LOAD x4 (32h) Timing



Note: 1. Number of dummy bits are different for the different densities, and plane select is not available in 1Gb. Plane select is a dummy bit in 1Gb device.

INTERNAL DATA MOVE

The INTERNAL DATA MOVE command programs or replaces data in a page with existing data. The internal data move command sequence is as follows:

- 13h (PAGE READ command to cache)
- 06h (WRITE ENABLE command)
- 84h (PROGRAM LOAD RANDOM DATA command)
- 10h (PROGRAM EXECUTE command)
- 0Fh (GET FEATURES command to read the status)

Note: If the random data is not sequential, another PROGRAM LOAD RANDOM DATA (84h) command must be issued with the new column address.

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Block Erase Operations

The BLOCK ERASE (D8h) command is used to erase at the block level. The blocks are organized as 64 pages per block, 2176 bytes per page (2048 + 128 bytes). Each block is 136KB. The BLOCK ERASE command (D8h) operates on one block at a time. The command sequence for the BLOCK ERASE operation is as follows:

- 06h (WRITE ENABLE command)
- D8h (BLOCK ERASE command)
- 0Fh (GET FEATURES command to read the status register)

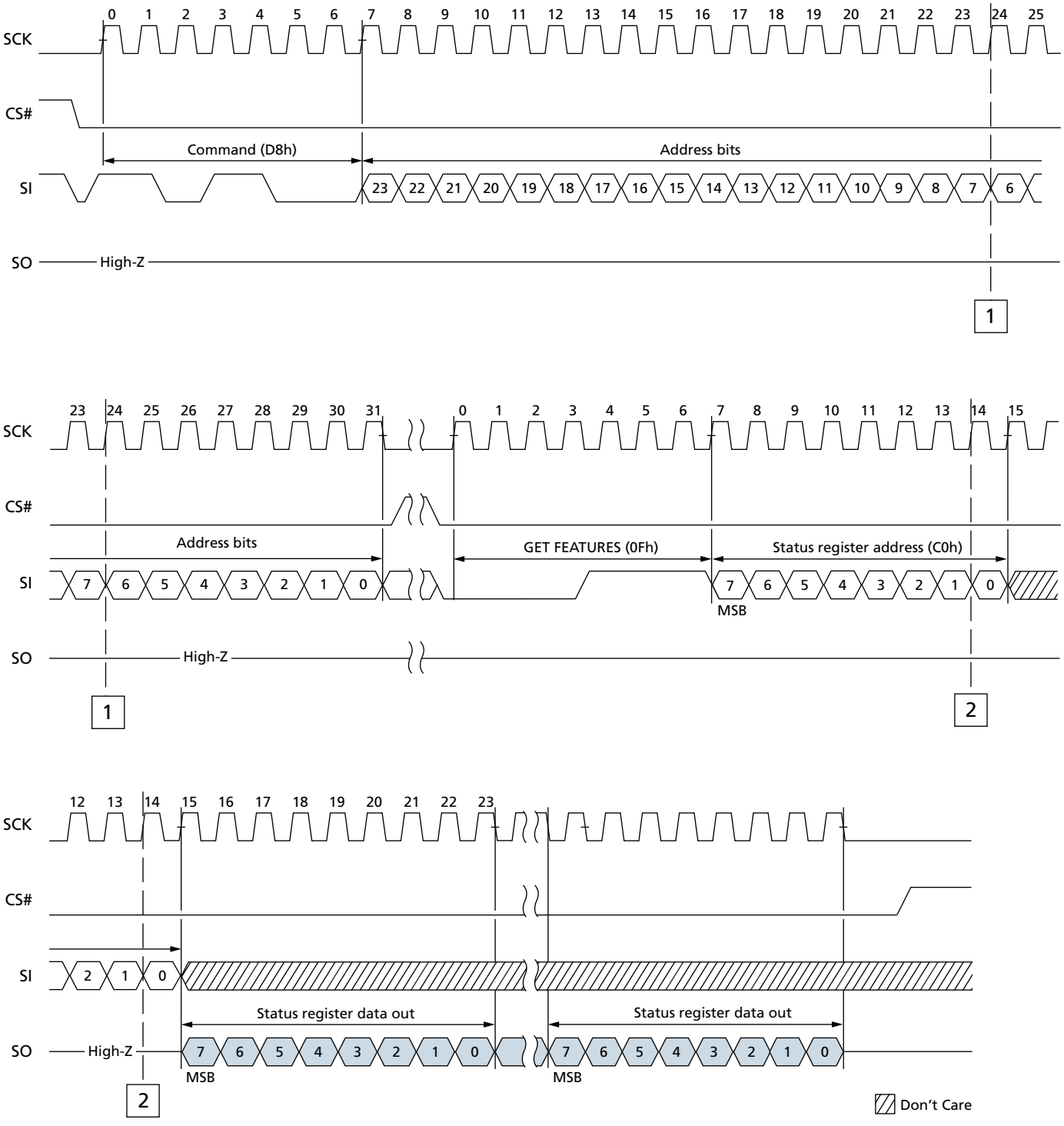
Prior to performing the BLOCK ERASE operation, a WRITE ENABLE (06h) command must be issued. As with any command that changes the memory contents, the WRITE ENABLE command must be executed in order to set the WEL bit. If the WRITE ENABLE command is not issued, then the rest of the erase sequence is ignored. A WRITE ENABLE command must be followed by a BLOCK ERASE (D8h) command. This command requires a 24-bit address consisting of dummy bits followed by a valid block address. After the address is registered, the control logic automatically controls timing and ERASE and VERIFY operations. The device is busy for t_{ERS} time during the BLOCK ERASE operation. The GET FEATURES (0Fh) command can be used to monitor the status of the operation. (See the following figure.)

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Figure 24: BLOCK ERASE (D8h) Timing



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Features Operations

GET FEATURES (0Fh) and SET FEATURES (1Fh)

The GET FEATURES (0Fh) and SET FEATURES (1Fh) commands either monitor the device status or alter the device configuration from the default at power-on. These commands use a 1-byte feature address to determine which feature is to be read or modified. Features such as OTP protect, block locking, SPI NOR like protocol configuration, and ECC correction can be managed by setting specific bits in feature addresses. Typically, the status register at feature address C0h is read to check the device status, except WEL, which is a writable bit with the WRITE ENABLE (06h) command.

When a feature is set, it remains active until the device is power cycled or the feature is written to. Unless specified otherwise, when the device is set, it remains set even if a RESET (FFh) command is issued. CFG[2:0] will be cleared to 000 after a reset and the device is back to normal operation.

Figure 25: GET FEATURES (0Fh) Timing

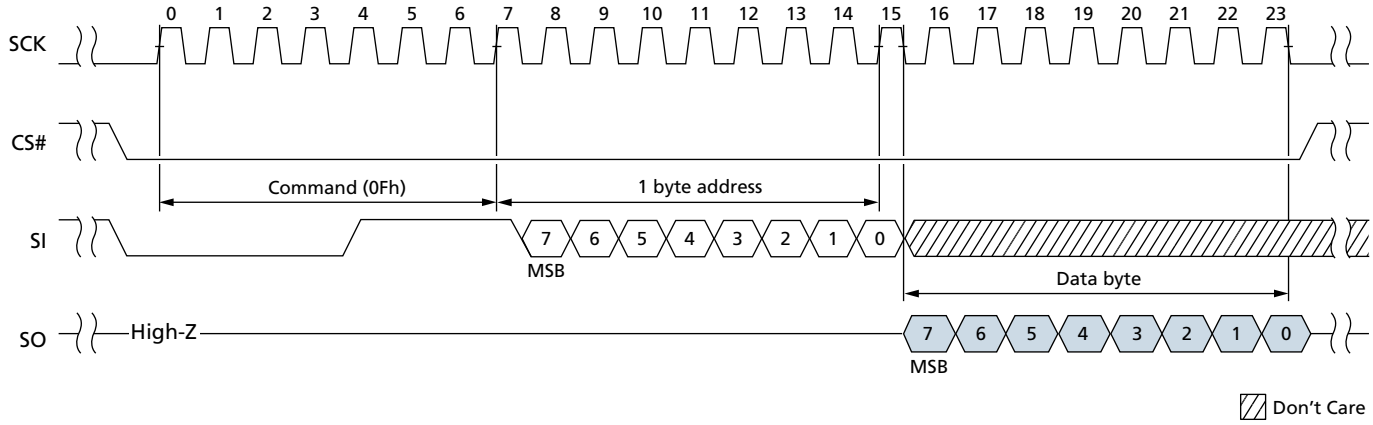
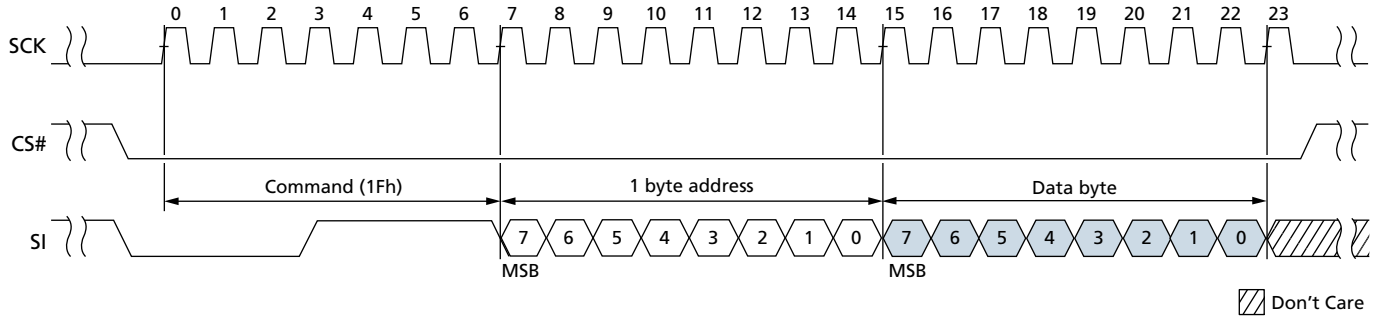


Figure 26: SET FEATURES (1Fh) Timing



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Feature Settings

Table 5: Feature Address Settings and Data Bits

Register	Feature Address	Feature Data Bits								Notes
		7	6	5	4	3	2	1	0	
Block lock	Address = A0h; Access = R/W	BRWD	BP3	BP2	BP1	BP0	TB	WP#/HOLD# Disable	–	1, 2
Configuration	Address = B0h; Access = R/W	CFG2	CFG1	LOT_EN	ECC_EN	–	–	CFG0	–	1
Status	Address = C0h; Access = R	CRBSY	ECCS2	ECCS1	ECCS0	P_Fail	E_Fail	WEL	OIP	1
Die select	Address = D0h; Access = R/W	–	DS0	–	–	–	–	–	–	1

Notes:
1. See the corresponding register bit description in Security Features, ECC Protection, Status Register, and Read Protocol – Similar to SPI NOR sections.
2. When the WP#/HOLD# disable bit is at the default value of 0, and with BRWD set to 1 and WP# LOW, block lock registers [7:2] cannot be changed.

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Security – Volatile Block Protection

The block lock feature protects the entire device or ranges of device blocks from the PROGRAM and ERASE operations. The SET FEATURE command must be issued to alter the state of block protection. After power-up, the device is in the locked state by default; block lock register bits BP[3:0] and TB are 1 . Reset will not modify the block protection state. When a PROGRAM/ERASE command is issued to a locked block, a status register P_Fail bit or E_Fail bit will be set to indicate the operation failure.

The following command sequence unlocks all blocks after power-up: The SET FEATURES register write (1Fh) operation is issued, followed by the feature address (A0h). Then, 00h is issued on data bits to unlock all blocks.

Security – Block Protection Bits

Table 6: Block Lock Register Block Protect Bits

TB	BP3	BP2	BP1	BP0	Protected Portion	Protected Blocks
0	0	0	0	0	None—all unlocked	None
0	0	0	0	1	Upper 1/1024 locked	2046:2047
0	0	0	1	0	Upper 1/512 locked	2044:2047
0	0	0	1	1	Upper 1/256 locked	2040:2047
0	0	1	0	0	Upper 1/128 locked	2032:2047
0	0	1	0	1	Upper 1/64 locked	2016:2047
0	0	1	1	0	Upper 1/32 locked	1984:2047
0	0	1	1	1	Upper 1/16 locked	1920:2047
0	1	0	0	0	Upper 1/8 locked	1792:2047
0	1	0	0	1	Upper 1/4 locked	1536:2047
0	1	0	1	0	Upper 1/2 locked	1024:2047
1	0	0	0	0	All unlocked	None
All others					All locked	0:2047
1	0	0	0	1	Lower 1/1024 locked	0:1
1	0	0	1	0	Lower 1/512 locked	0:3
1	0	0	1	1	Lower 1/256 locked	0:7
1	0	1	0	0	Lower 1/128 locked	0:15
1	0	1	0	1	Lower 1/64 locked	0:31
1	0	1	1	0	Lower 1/32 locked	0:63
1	0	1	1	1	Lower 1/16 locked	0:127
1	1	0	0	0	Upper 1/8 locked	0:255
1	1	0	0	1	Lower 1/4 locked	0:511
1	1	0	1	0	Lower 1/2 locked	0:1023
1	1	1	1	1	All locked (default)	0:2047

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Security – Hardware Write Protection

Hardware write protection prevents the block protection state from hardware modifications.

The following command sequence enables hardware write protection: The SET FEATURE command is issued on feature address A0h. Then, the WP#/Hold# disable bit state is set to 0 as the default after power up.

The BRWD bit is operated in conjunction with WP#/Hold# disable bit. When BRWD is set to 1 and WP# is LOW, none of the other block lock register bits [7:2] can be set. The block lock state cannot be changed, regardless of what is unlocked or locked. Also, when the WP#/Hold# disable bit is set to 1, the hardware protected mode is disabled. The default value of BRWD and WP#/Hold# disable bits = 0 after power up.

Security – Device Lock Tight (LOT)

The lock tight mode prevents the block protection state from software modifications. After it is enabled, this mode cannot be disabled by a software command. Also, BP, TB, and BRWD bits are protected from further software changes. Only another power cycle can disable the lock tight mode.

The following command sequence enables the lock tight mode: The SET FEATURES register write (1Fh) operation is issued, followed by the feature address (B0h). Then, data bits are set to enable LOT (LOT_EN bit = 1).

When the hardware write protection mode is disabled during quad or x4 mode, lock tight can be used to prevent a block protection state change.

Permanent Block Lock Protection

48 blocks per die (0 to 47) can be permanently locked using PROTECT command. The PROTECT command provides nonvolatile, irreversible protection of up to twelve groups (48 blocks). Implementation of the protection is group-based, which means that a minimum of one group (4 blocks) is protected when the PROTECT command is issued. Because block protection is nonvolatile, a power-on or power-off sequence does not affect the block status after the PROTECT command is issued. The device is shipped from the factory with no blocks protected so that users can program or erase the blocks before issuing the PROTECT command. Block protection is also irreversible in that when protection is enabled by issuing the PROTECT command, the protected blocks can no longer be programmed or erased. If permanent lock is disabled, PROTECT command would be ignored. As with any command that changes the memory contents, the WRITE ENABLE must be executed. If this command is not issued, then the protection command is ignored. WRITE ENABLE must be followed by a PROTECTION command (2Ch).

The following PROTECT sequence is used:

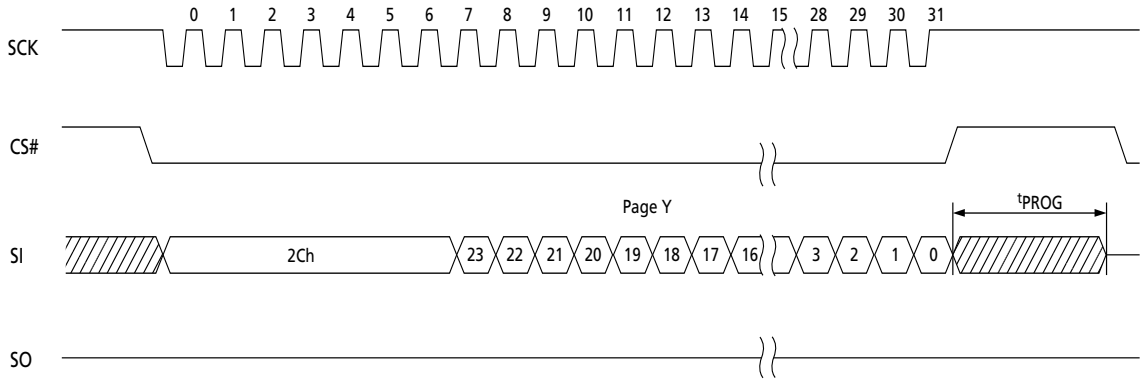
- 06h (WRITE ENABLE)
- 2Ch (permanent block lock protection)
- 24-bit address (see the PROTECTION Command Details)
- After ^{t}PROG time, use GET FEATURE command (0Fh) with feature address C0h to verify P_Fail bit

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Figure 27: PROTECT Command Cycle



PROTECTION Command (2Ch) Details

To enable protection, the PROTECTION command consists of an 8-bit command code, followed by a 24-bit address (8 dummy bits and an 16-bit page/block address for 1Gb or 7 dummy bits and an 17-bit page/ block address for 2Gb die). Row address bits 11, 10, 9, 8 (named as Y) input the targeted block group information. Where Y defines the group of blocks to be protected. There are 12 Groups Y where Y = 0000b-1011b:

- Y = 0000 protects Group0 = blks 0, 1, 2, 3.
- Y = 0001 protects Group1 = blks 4, 5, 6, 7.
- .....
- Y = 1011 protects Group11 = blks 44, 45, 46, 47.

After ^{t}PROG, the targeted block groups are protected. Upon PROTECT operation failure, the status register reports a value of 0Ch (P_FAIL = 1 and WEL = 1). Upon PROTECT operation success, the status register reports a value of 00h.

Note: There is no status register to check the PROTECT status of a block or a group. A permanent blocks table should be maintained and updated after a group is protected.

Permanent Block Lock Protection Disable Mode

This mode disables the ability to accept the PROTECTION command. Running this command sequence ensures no more groups can ever be permanently locked.

The following disable PROTECT sequence is used

- SET FEATURE command (1Fh) with B0h mode and data value C2h
- 06h (WRITE ENABLE)
- 10h (Execute with block/page address as '0')
- After ^{t}PROG time, use GET FEATURE command (0Fh) with feature address C0h to verify P_Fail bit

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Security – One Time Programmable (OTP)

This device offers a protected, one-time programmable NAND Flash memory area. Ten full pages (10 x 2176 bytes per page) per die are available, and the entire range is guaranteed. Customers can choose how to use the OTP area, such as programming serial numbers or other data for permanent storage. The OTP area can't be erased. When ECC is enabled, data written in the OTP area is ECC protected. Besides some additional configuration bits are described in this section.

Enable OTP Access

OTP access needs to be enabled in order to read and write to the OTP region. When the die is in OTP operation mode, all subsequent page program or page read commands are applied to the OTP area. SET FEATURES command (1Fh) with feature address B0h and data 50h (OTP operation mode with ECC enabled) or 40h (OTP operation mode with ECC disabled) are used to enable the OTP access.

After OTP access is enabled, the following sequence is used to program one or more pages

- WRITE ENABLE command (06h)
- PROGRAM EXECUTE command (10h) with the row address of page (OTP page address range 02h-0Bh)
- Verify until OIP bit not busy using GET FEATURE command (0Fh) with feature address C0h
- Using GET FEATURE command (0Fh) with feature address C0h, verify if P_FAIL bit is 0 for the successful operation.

After OTP access is enabled, the following sequence is used to read one or more pages

- PAGE READ command (13h) with the page address (02h-0Bh)
- Verify until OIP bit is not busy using GET FEATURE command (0Fh) with feature address C0h
- Page data using READ FROM CACHE command (03h).

OTP Configuration States

To check the status of OTP data protect, SPI NOR read enable, or permanent block Lock protection, the following sequence is used

- SET FEATURES command (1Fh) with feature address B0h and data (C0h for OTP data protect bit, 82h for NOR read protocol enable bit, C2h for permanent block lock disable bit)
- PAGE READ command (13h) with address 0
- Verify until OIP bit not busy using GET FEATURE command (0Fh) with feature address C0h
- READ FROM CACHE command (03h) with address 0
- Expect the read from cache data all 1 for the mode disabled or all "0" for enabled.

Note: Configuration status of CFG[2:0] can be read using GET FEATURE command (0Fh) with feature address B0h.

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OTP Protection and Program Prevention

This mode is used to prevent further programming of the pages in the OTP area. To protect and prevent programming the OTP area, the following sequence is used

- SET FEATURES command (1Fh) with feature address B0h and data C0h (CFG[2:0] = 110b)
- WRITE ENABLE command (06h)
- PROGRAM EXECUTE command (10h) with the row address 00h
- Verify until OIP bit not busy and P_FAIL bit 0 using GET FEATURE command (0Fh) with status register address C0h.

Exit OTP

To exit from OTP operation mode and return the device to normal array operation mode, the SET FEATURES command (1Fh) is issued. This is followed by setting the feature address = B0h and data CFG[2:0] = 000b. Last, the RESET (FFh) command is issued.

Table 7: Configuration Registers for Security

CFG2	CFG1	CFG0	State
0	0	0	Normal operation
0	1	0	Access OTP area/Parameter/Unique ID
1	1	0	Access to OTP data protection bit to lock OTP area
1	0	1	Access to SPI NOR read protocol enable mode
1	1	1	Access to permanent block lock protection disable mode

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Status Register

The device has an 8-bit status register that software can read during the device operation. All bits are read-only register except WEL, which could be changed by WRITE DISABLE (04h) and WRITE ENABLE (06h) commands. None of bits can be changed by SET FEATURE command (1Fh).The status register can be read by issuing the GET FEATURES (0Fh) command, followed by the feature address (C0h). The status register will output the status of the operation.

Table 8: Status Register Bit Descriptions

Bit	Bit Name	Description
7	Cache read busy (CRBSY)	This bit is set (CRBSY = 1) when READ PAGE CACHE RANDOM command is executing; this bit remains a 1 until the page specified at READ PAGE CACHE RANDOM command is transferred from array to data register. When the bit is 0, the device is in the ready state and background read page cache operation is completed. RESET command is acceptable during CRBSY = 1 and could halt background read page cache operation and download first page at block 0 into cache register at default.
6	ECC status register (ECCS2)	See ECC Protection for the ECC status definition. ECC status is set to 000b either following a RESET or at the beginning of the READ. It is then updated after the device completes a valid READ operation. ECC status is invalid if ECC is disabled (via a SET FEATURES command to get access the configuration register). After a power-up RESET, ECC status is set to reflect the contents of block 0, page 0.
5	ECC status register (ECCS1)	
4	ECC status register (ECCS0)	
3	Program fail (P_Fail)	Indicates that a program failure has occurred (P_Fail = 1). This bit will also be set if the user attempts to program an invalid address or a locked or protected region, including the OTP area. This bit is cleared during the PROGRAM EXECUTE command sequence or a RESET command (P_Fail = 0).
2	Erase fail (E_Fail)	Indicates that an erase failure has occurred (E_Fail = 1). This bit will also be set if the user attempts to erase a locked region or if the ERASE operation fails. This bit is cleared (E_Fail = 0) at the start of the BLOCK ERASE command sequence or a RESET command.
1	Write enable latch (WEL)	Indicates the current status of the write enable latch (WEL) and must be set (WEL = 1) prior to issuing a PROGRAM EXECUTE or BLOCK ERASE command. It is set by issuing the WRITE ENABLE command. WEL can also be cleared (WEL = 0) by issuing the WRITE DISABLE command or a successful PROGRAM/ERASE operation.
0	Operation in progress (OIP)	This bit is set (OIP = 1) when a PROGRAM EXECUTE, PAGE READ, READ PAGE CACHE LAST, BLOCK ERASE, READ PAGE CACHE RANDOM (within ^{t}RCBSY to wait for cache register readiness) or RESET command or a power-up initialization is executing; the device is busy. When the bit is 0, the interface is in the ready state.

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ECC Protection

The device offers an 8-bit data corruption protection by offering internal ECC to obtain the data integrity. The internal ECC can be enabled or disabled by setting the ECC_EN bit in the configuration register. ECC is enabled after device power-up by default. The READ and PROGRAM commands operate with internal ECC by default. Reset will not change the existing configuration. To enable/disable ECC after power on, perform the following command sequence:

- Issue the SET FEATURES command (1Fh)
- Issue configuration register address (B0h)
- Then: To enable ECC, set bit 4 (ECC enable) to 1; To disable ECC, clear bit 4 (ECC enable) to 0

During a PROGRAM operation, the device calculates an expected ECC code on the ECC-protected bytes in the cache register, before the page is written to the NAND Flash array. The ECC code is stored in the spare area of the page.

During a READ operation, the page data is read from the array to the cache register, where the ECC code is calculated and compared with the expected ECC code value read from the array. If a 1–8-bit error is detected, the error is corrected in the cache register. Only corrected data is output on the I/O bus. The ECC status register bit indicates whether or not the error correction is successful. The table below describes the ECC protection scheme used throughout a page.

Note: The unique ID and parameter page are not ECC-protected areas. Multiple copies are provided for parameter page to obtain the data integrity. XOR method is provided for unique ID to verify the data.

With internal ECC, users must accommodate the following (details provided in table below):

- Spare area definitions
- WRITEs are supported for main and spare areas (user meta data I and II). WRITEs to the ECC area are prohibited

When using partial-page programming, the following conditions must both be met:

- In the main user area and user meta data area I, single partial-page programming operations must be used
- Within a page, a maximum of four partial-page programming operations can be performed

Table 9: ECC Status Register Bit Descriptions

Bit 2	Bit 1	Bit 0	Description
0	0	0	No errors
0	0	1	1-3 bit errors detected and corrected
0	1	0	Bit errors greater than 8 bits detected and not corrected
0	1	1	4-6 bit errors detected and corrected. Indicates data refreshment might be taken
1	0	1	7-8 bit errors detected and corrected. Indicates data refreshment must be taken to guarantee data retention
Others			Reserved

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Table 10: ECC Protection

Max Byte Address	Min Byte Address	ECC Protected	Area	Description
1FFh	000h	Yes	Main 0	User Main data 0
3FFh	200h	Yes	Main 1	User Main data 1
5FFh	400h	Yes	Main 2	User Main data 2
7FFh	600h	Yes	Main 3	User Main data 3
803h	800h	No	Spare 0	Reserved (bad block data)
807h	804h	No	Spare 1	User meta data II
80Bh	808h	No	Spare 2	User meta data II
80Fh	80Ch	No	Spare 3	User meta data II
813h	810h	No	Spare 0	User meta data II
817h	814h	No	Spare 1	
81Bh	818h	No	Spare 2	
81Fh	81Ch	No	Spare 3	
827h	820h	Yes	Spare 0	User meta data I
82Fh	828h	Yes	Spare 1	
837h	830h	Yes	Spare 2	
83Fh	838h	Yes	Spare 3	
84Fh	840h	Yes	Spare 0	ECC for Main/Spare 0
85Fh	850h	Yes	Spare 1	ECC for Main/Spare 1
86Fh	860h	Yes	Spare 2	ECC for Main/Spare 2
87Fh	870h	Yes	Spare 3	ECC for Main/Spare 3

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Error Management

This NAND Flash device is specified to have the minimum number of valid blocks (N_{VB}) of the total available blocks per die shown in the table below. This means the devices may have blocks that are invalid when shipped from the factory. An invalid block is one that contains at least one page that has more bad bits than can be corrected by the minimum required ECC. Additional bad blocks may develop with use. However, the total number of available blocks will not fall below N_{VB} during the endurance life of the product.

Although NAND Flash memory devices may contain bad blocks, they can be used reliably in systems that provide bad-block management and error-correction algorithms. This ensures data integrity.

Internal circuitry isolates each block from other blocks, so the presence of a bad block does not affect the operation of the rest of the NAND Flash array.

NAND Flash devices are shipped from the factory erased. The factory identifies invalid blocks before shipping by attempting to program the bad-block mark into every location in the first page of each invalid block. It may not be possible to program every location in an invalid block with the bad-block mark. However, the first spare area location in each bad block is guaranteed to contain the bad-block mark. This method is compliant with ONFI factory defect mapping requirements. See the following table for the bad-block mark.

System software should initially check the first spare area location for non-FFh data on the first page of each block prior to performing any program or erase operations on the NAND Flash device. A bad-block table can then be created, enabling system software to map around these areas. Factory testing is performed under worst-case conditions. Because invalid blocks may be marginal, it may not be possible to recover the bad-block marking if the block is erased.

Table 11: Error Management Details

Description	Requirement
Minimum number of valid blocks per die (N_{VB})	2008
Total available blocks per die	2048
First spare area location in the first page of each block	Byte 2048
Value programmed for bad block at the first byte of spare area	00h
Minimum required ECC	8-bit ECC per sector (544) bytes of data
Minimum ECC with internal ECC enabled	8-bit ECC per 512 bytes (user data) + 8 bytes (Spare) + 16 bytes (ECC data)

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SPI NOR Read Configuration

Some chipset vendors may have already designed in SPI NOR IP to support system boot; address allocation on clock cycle in SPI NAND read from cache protocol will cause incompatibility. To be drop-in compatible to SPI NOR read protocol, this device offers an alternative solution to implement 03h/0Bh commands, as are done with SPI NOR. Refer to the Electrical Specifications for detail timing requirement. This solution would be enabled using the following command sequence:

- SET FEATURE command (1Fh) with feature address B0h and CFG bits[2:0] = 101b (access SPI NOR read protocol enable mode)
- WRITE ENABLE command (06h)
- PROGRAM EXECUTE command (10h) with block/page address all 0
- GET FEATURE command (0Fh) with status register address C0h to check until device is ready (OIP bit clear) and verify that P_FAIL bit is not set
- SET FEATURE command (1Fh) with feature address B0h and CFG bits[2:0] = 000b (return to normal operation mode)
- GET FEATURE command (0Fh) at address B0h and CFG bits[2:0] = 101b to verify all 0; all 1 indicates SPI NOR mode not enabled.

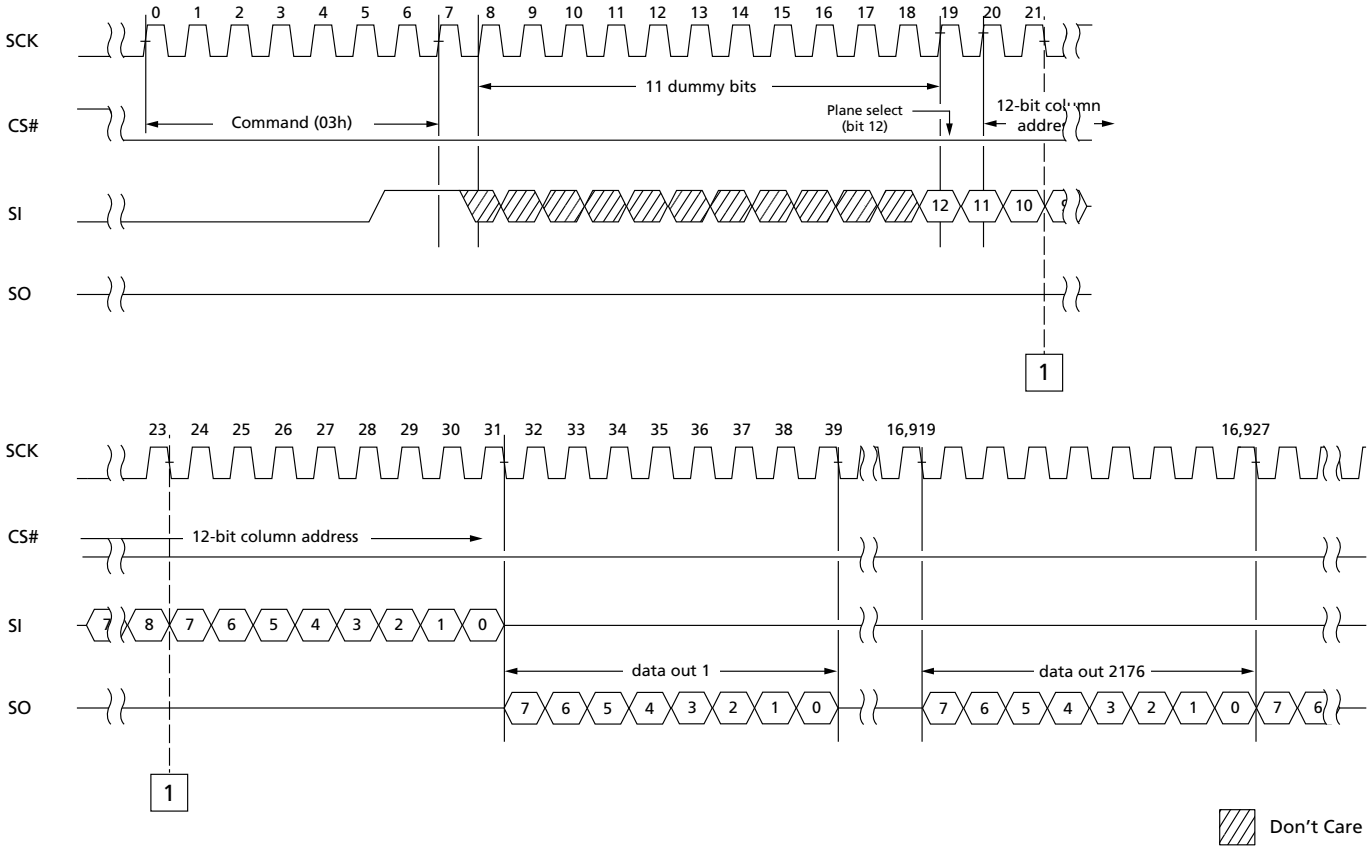
It is a nonvolatile configuration setting and power cycle will not recover it back to SPI NAND default mode. The rest of the SPI NAND commands still work in this configuration.

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Figure 28: Read from Cache (03h)



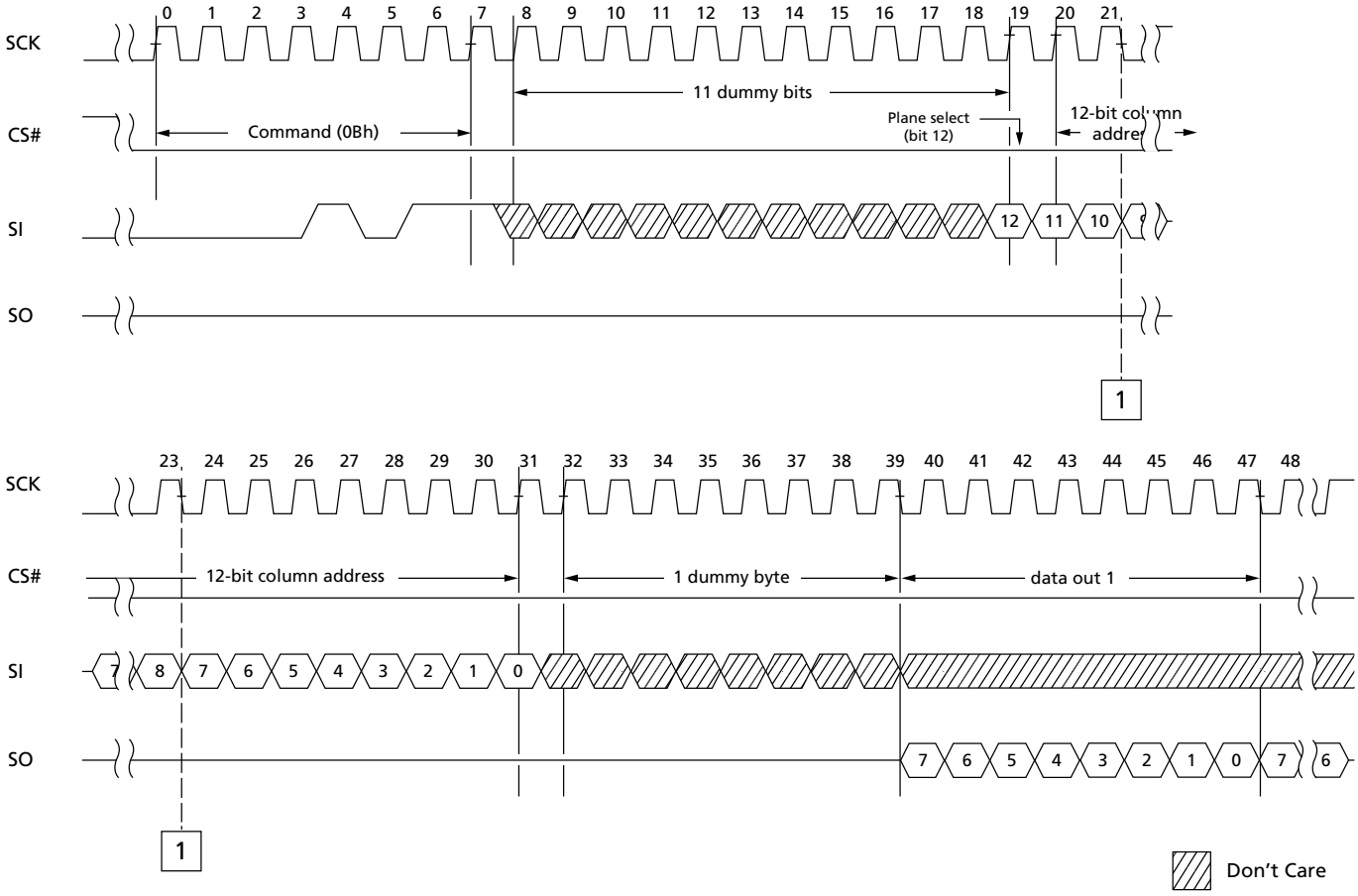
Note: 1. SPI NOR compatible. Plane select bit not available in 1Gb device and can be used as a dummy bit.

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Figure 29: Fast Read from Cache (0Bh)



Note: 1. SPI NOR compatible. Plane select bit not available in 1Gb device and can be used as a dummy bit.

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Power-Up and Power-Down

At power-up and power-down, the device must not be selected; that is, CS# must follow the voltage applied on V_{CC} until V_{CC} reaches the correct values: $V_{CC,\,min}$ at power-up and V_{SS} at power-down. Micron NAND Flash devices are designed to prevent data corruption during power transitions. V_{CC} is internally monitored and when V_{CC} reaches the write inhibit voltage V_{WI}, a minimum of 250µs must elapse before issuing a RESET (FFh) command. After issuing the RESET command, 1.25ms must elapse before issuing any other command. GET FEATURE command could be issued to poll the status register (OIP) before the first access. Normal precautions must be taken for supply line decoupling to stabilize the V_{CC} supply. Each device in a system should have the V_{CC} line decoupled by a suitable capacitor (typically 100nF) close to the package pins.

> **Note:** For power cycle testing, the system must not initiate the power-up sequence until V_{CC} drops down to 0V.

Figure 30: SPI Power-Up

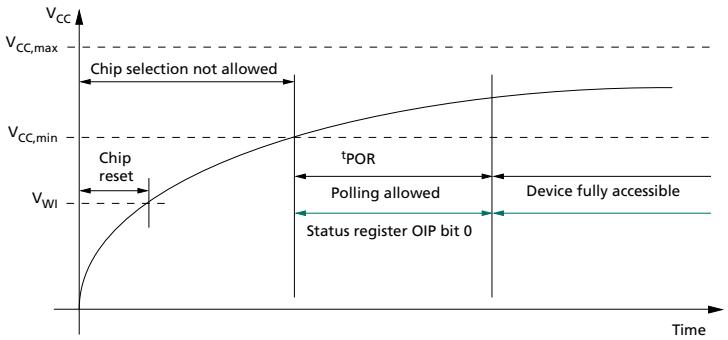
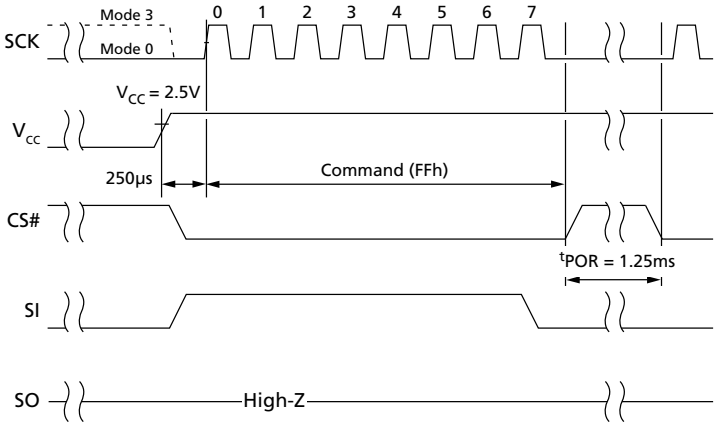


Figure 31: SPI Power-Up Timing



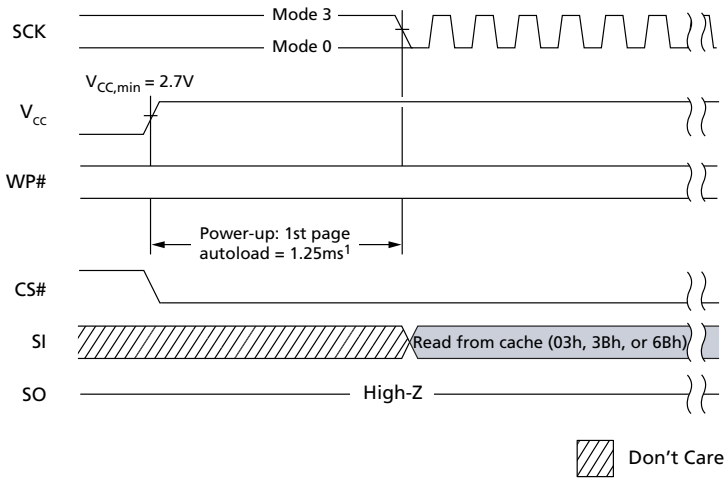
Micron has developed an alternative SPI NAND sequence that does not require issuing an explicit RESET (FFh) command upon power-up. This is default device initialization setting. When device V_{CC} has reached the write inhibit voltage, the device automatically kicks off the initialization. At default setting, first page data would be automatically loaded into cache register. During the initialization, GET FEATURE command could be issued to poll the status register (OIP) before the first access; Or, the first access can occur 1.25ms after V_{CC} reaches $V_{CC,min}$.

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Figure 32: Alternative SPI Power-Up Timing



Note: 1. Poll status register OIP bit is allowed during device initialization.

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Electrical Specifications

Stresses greater than those listed can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above values in this specification is not guaranteed. Exposure to absolute maximum rating conditions for extended periods can affect reliability.

Table 12: Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply voltage (SPI)	V_{CC}	–0.6	4.6	V
I/O voltage	V_{CC}	–0.6	4.6	V
Operating temperature (ambient)	T_A	–40	85	°C
Storage temperature	T_S	–65	150	°C

Note: 1. During infrequent, nonperiodic transitions and for periods less than 20ns, voltage potential between V_{SS} and V_{CC} may undershoot to –2.0V or overshoot to V_{CC_MAX} + 2.0V.

Table 13: Operating Conditions

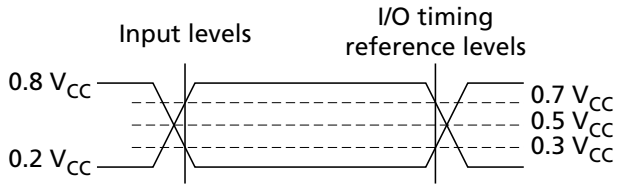
Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	2.7	3.3	3.6	V
Ambient operating temperature (industrial)	T_A	–40	25	85	°C

Table 14: AC Measurement Conditions

Parameter	Symbol	Min	Max	Unit
Load Capacitance	C_L	30/10		pF
Input rise and fall time	–	–	5	ns
Input rise and fall time (>100 MHz)	–	–	1.5	ns
Input pulse voltage[1]	–	0.2 V_{CC}	0.8 V_{CC}	V
Input timing reference voltages	–	0.3 V_{CC}	0.7 V_{CC}	V
Output timing reference voltages	–	V_{CC}/2		V

Note: 1. These are Min/Max specifications for dual/quad operations.

Figure 33: AC Measurement I/O Waveform



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Table 15: Capacitance

Description	Symbol	Test Conditions	Min	Max	Unit
Input/output capacitance (IO0, IO1, IO2, IO3)	C_{IN}	V_{OUT} = 0V	–	9	pF
Input capacitance (other pins)	C_{IN}	V_{IN} = 0V	–	9	pF

Notes:
1. These parameters are verified in device characterization and are not 100% tested.
2. The value includes the silicon and package together.

Table 16: DC Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input high voltage	V_{IH}	–	0.7 × V_{CC}	–	V_{CC} + 0.4	V
Input low voltage	V_{IL}	–	–0.5	–	0.3 × V_{CC}	V
Output high voltage	V_{OH}	I_{OH} = –100µA	V_{CC} - 0.2	–	–	V
Output low voltage	V_{OL}	I_{OL} = 1.6mA	–	–	0.4	V
Input leakage current	I_{LI}	–	–	–	±10	µA
Output leakage current	I_{LO}	–	–	–	±10	µA
Page read current	I_{CC3}	–	–	25	35	mA
Program current	I_{CC4}	–	–	20	25	mA
Erase current	I_{CC5}	–	–	20	25	mA
Standby current	I_{CC1}	CE# = V_{CC}; V_{IN} = V_{SS} or V_{CC}	–	15	50	µA

Notes:
1. Typical values are given for T_A = 25 °C.
2. These parameters are verified in device characterization and are not 100% tested.

Table 17: AC Characteristics

Parameter	Symbol	Min	Max	Unit
Clock frequency[1, 2]	^{f}C	–	133	MHz
Clock LOW time	^{t}WL	3.375	–	ns
Clock HIGH time	^{t}WH	3.375	–	ns
Clock LOW time (SPI NOR read 03h mode at 20 MHz)	^{t}WL	22.5	–	ns
Clock HIGH time (SPI NOR read 03h mode at 20 MHz)	^{t}WH	22.5	–	ns
Clock rise time	^{t}CRT	1.3	–	V/ns
Clock fall time	^{t}CFT	1.3		V/ns
Command deselect time	^{t}CS	30	–	ns
Chip select# active setup/hold time relative to SCK	^{t}CSS/^{t}CSH	3.375	–	ns
Chip select# non-active setup/hold time relative to SCK	^{t}CSH	2.5	–	ns
Output disable time	^{t}DIS	–	6	ns
Data input setup time	$^{t}SUDAT$	2.5	–	ns
Data input hold time	$^{t}HDDAT$	1.75	–	ns
Clock LOW to output valid (30pF)	^{t}V	–	6	ns

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Table 17: AC Characteristics (Continued)

Parameter	Symbol	Min	Max	Unit
Clock LOW to output valid (10pF)	^{t}V	–	5	ns
Clock LOW to output valid (similar to SPI NOR 20 MHz read 30pF)	^{t}V	–	30	ns
Clock LOW to output valid (similar to SPI NOR 20 MHz read 10pF)	^{t}V	–	28	ns
Output hold time (30pF)	^{t}HO	2	–	ns
Output hold time (10pF)	^{t}HO	1.5	–	ns
Output hold time (SPI NOR similar to 20 MHz read 30pF)	^{t}HO	0	–	ns
Output hold time (SPI NOR similar to 20 MHz read 10pF)	^{t}HO	0	–	ns
WP# hold time	^{t}WPH	100	–	ns
WP# setup time	^{t}WPS	20	–	ns

Notes:
1. Read from Cache Dual I/O (BBh) and Quad I/O (EBh) can run up to 108 MHz.
2. When read protocol similar to SPI NOR is enabled, Read from Cache 03h command can run up to 20 MHz, while read from Cache 0Bh command can run up to 133 MHz.

Table 18: PROGRAM/READ/ERASE Characteristics

Parameter	Symbol	Typ	Max	Unit
BLOCK ERASE operation time (128KB)	^{t}ERS	2	10	ms
PROGRAM PAGE operation time (ECC disabled)	$^{t}PROG$	200	600	µs
PROGRAM PAGE operation time (ECC enabled)		220	600	
Page read time (ECC disabled)	^{t}RD	–	25	µs
Page read time (ECC enabled)		46	70	
Data transfer time from data register to cache register (internal ECC disabled)	$^{t}RCBSY$	–	5	µs
Data transfer time from data register to cache register (internal ECC enabled)		40	50	µs
Power-on reset time (device initialization) from V_{CC} MIN	^{t}POR	–	1.25	ms
Write inhibit voltage	V_{WI}	–	2.5	V
Reset time for READ, PROGRAM, and ERASE operations (internal ECC disabled)	^{t}RST[1]	–	30/35/525	µs
Reset time for READ, PROGRAM, and ERASE operations (internal ECC enabled)		–	75/80/570	µs
Number of partial-page programming operations supported	NOP[2]	–	4	–

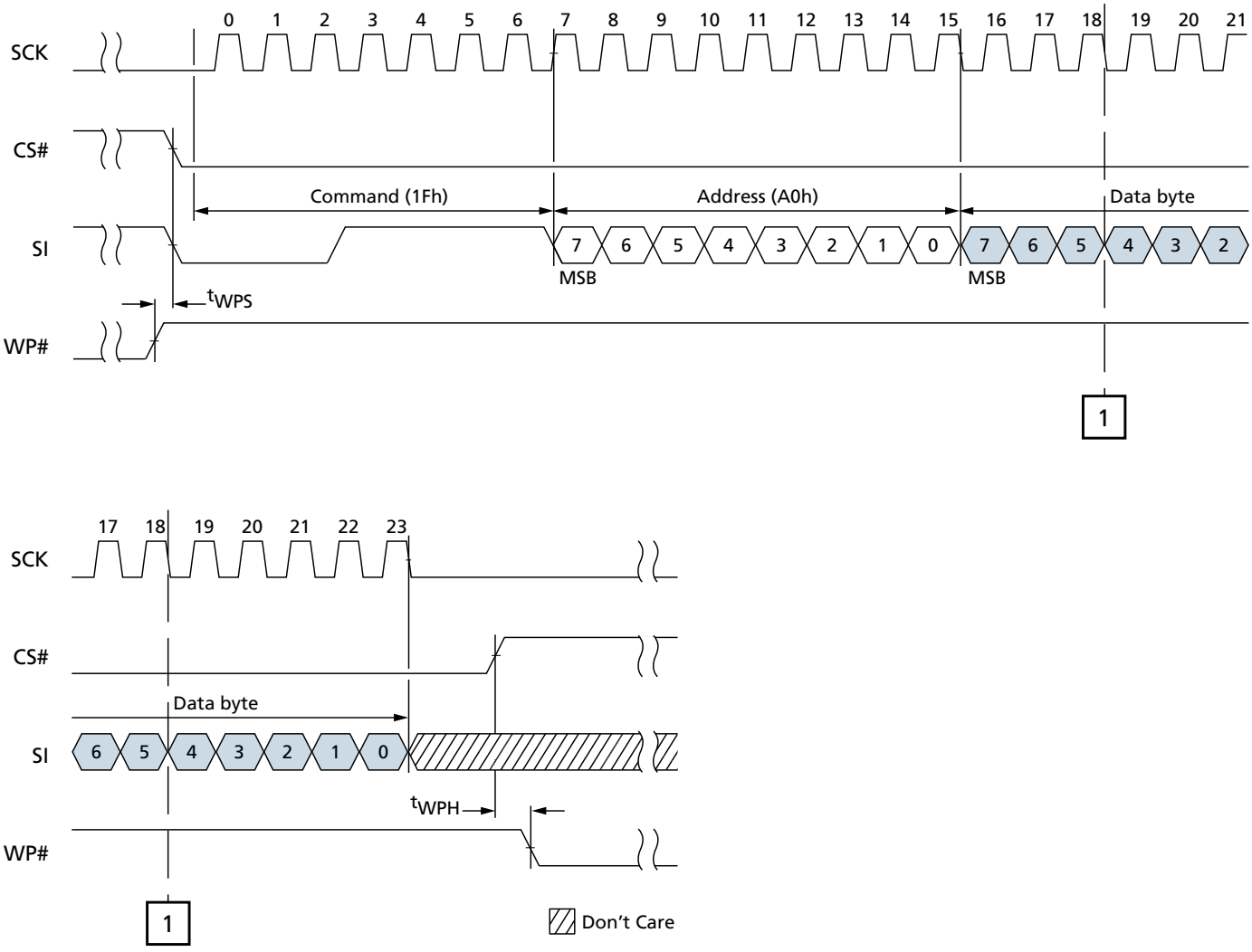
Notes:
1. For first RESET condition after power-up, ^{t}RST will be 1.25ms maximum. For stacked die, no command should be issued during this time.
2. In the main user area and in user meta data area I, single partial-page programming operations must be used. Within a page, the user can perform a maximum of four partial-page programming operations.

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Figure 34: WP# Timing



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Figure 35: Serial Input Timing

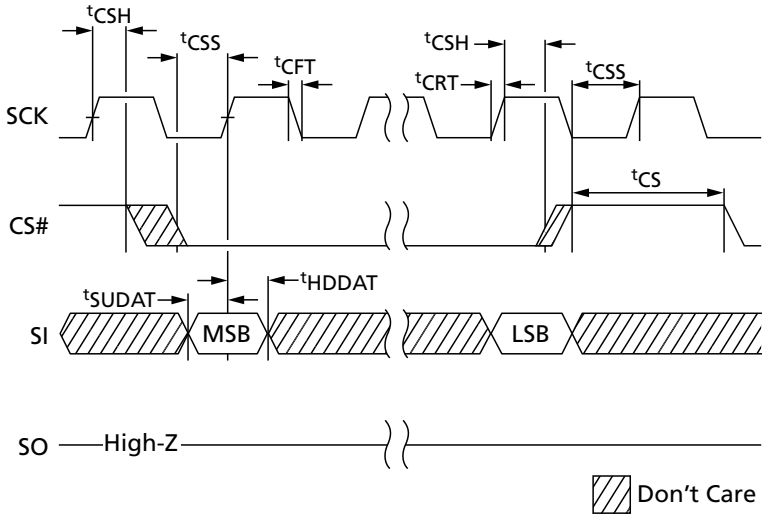
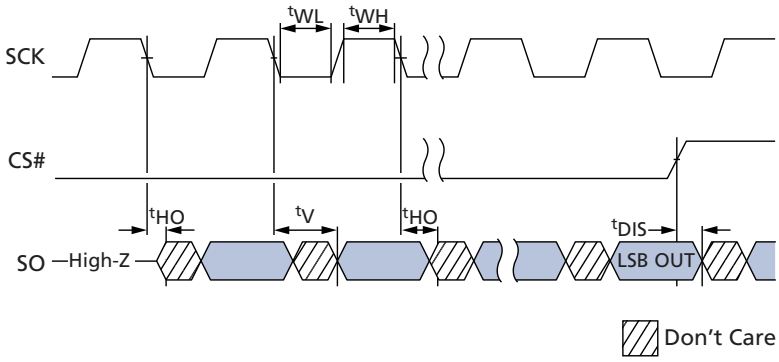


Figure 36: Serial Output Timing



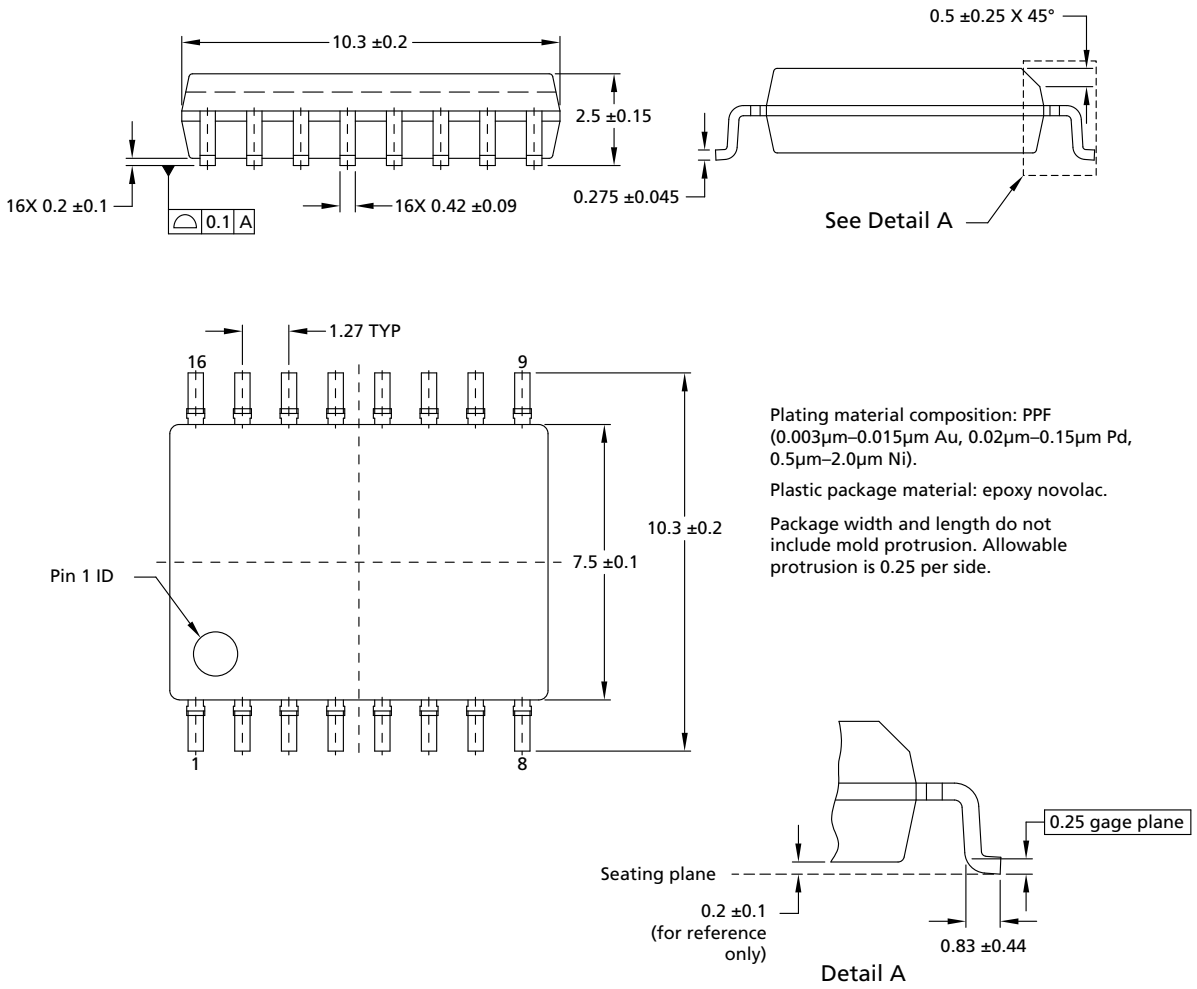
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Package Dimensions

Figure 37: 16-pin SOP (300 mils body width) – Package Code: SF



Note: 1. All dimensions are in millimeters.

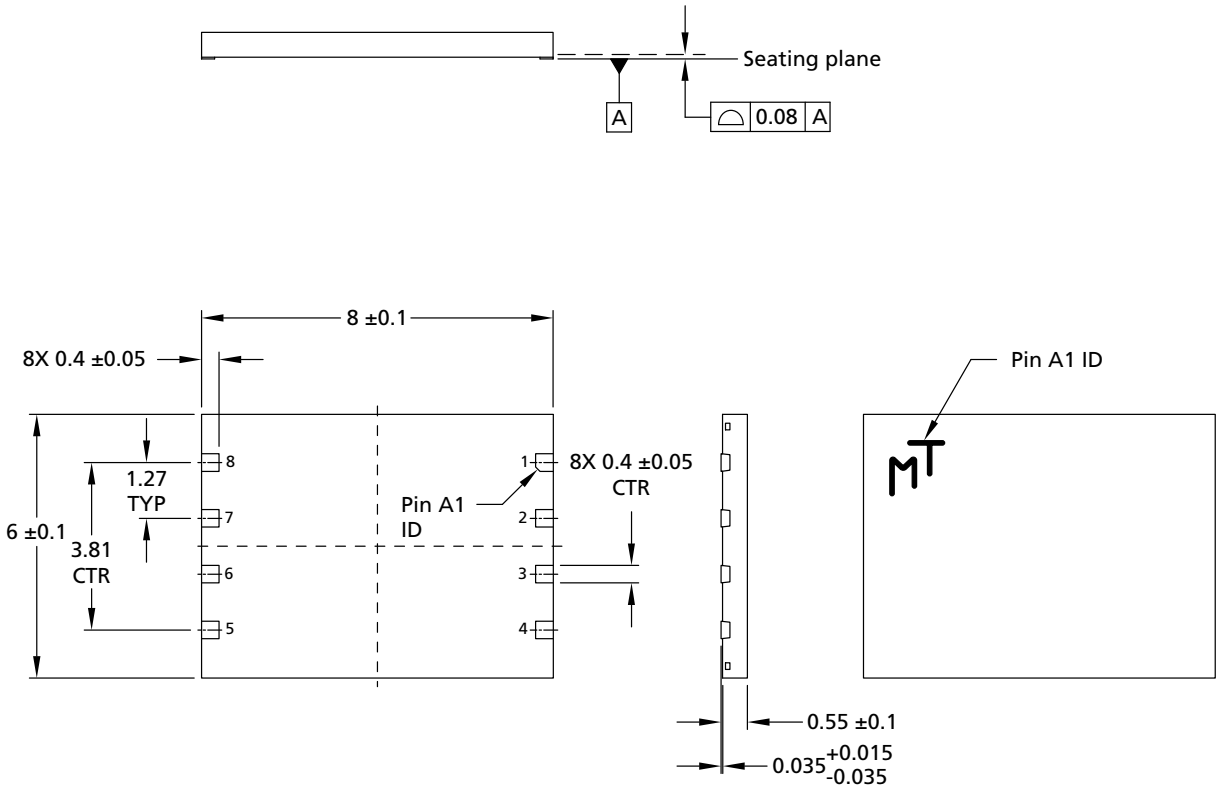
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Package Dimensions

Figure 38: 8-pin U-PDFN (MLP8) 8mm x 6mm x 0.65mm – Package Code: WB



Note: 1. All dimensions are in millimeters.

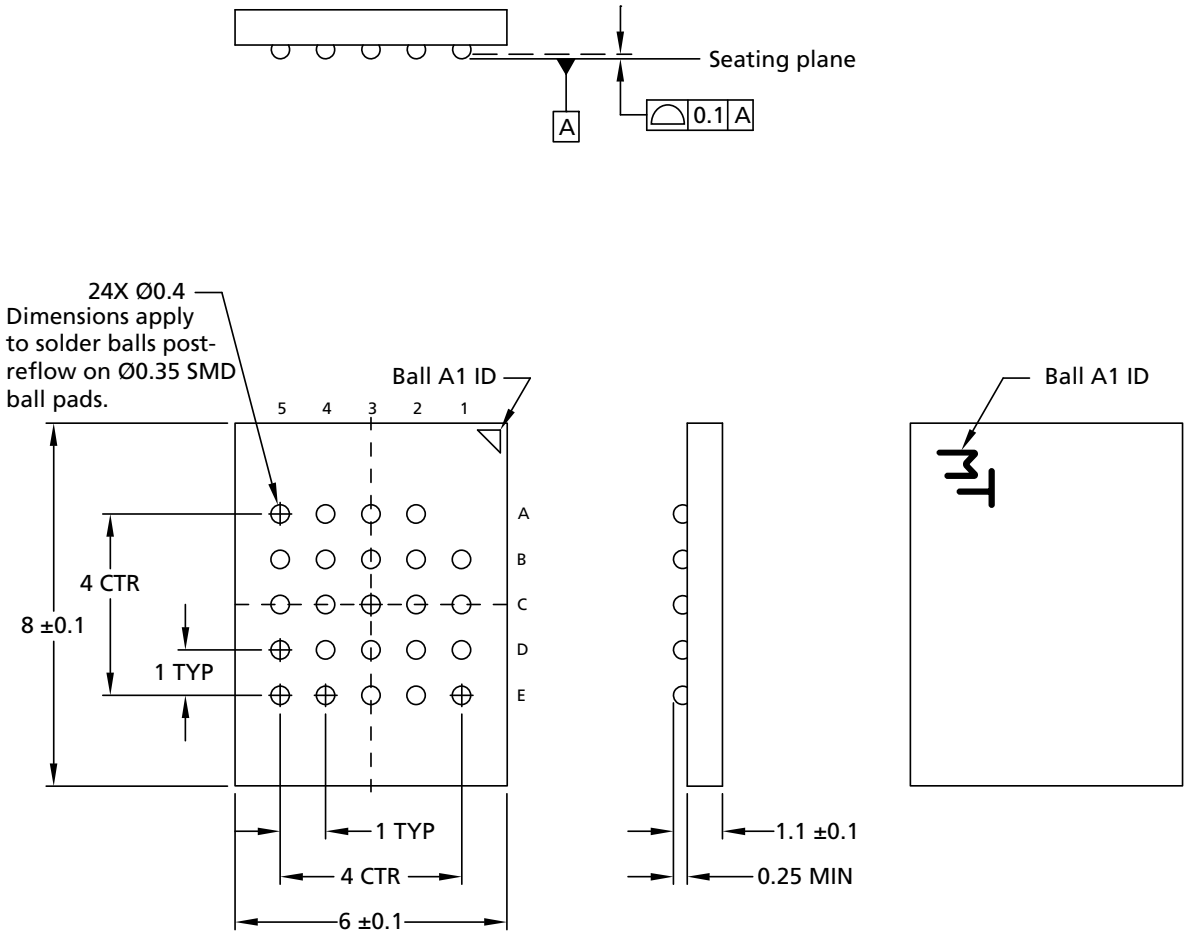
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Package Dimensions

Figure 39: 24-Pin T-PBGA (5 x 5 Ball Grid Array) 6mm x 8mm – Package Code: 12



Note: 1. All dimensions are in millimeters.

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Revision History

Rev. F – 09/16

- Updated legal status to Production
- Updated AC Characteristics table for NOR 03h cache read mode

Rev. E – 06/16

- Added uncycled data retention
- Updated PROGRAM/ERASE cycle to 100,000
- Updated byte 105 and 106 of the parameter table for P/E of 100,000
- Added permanent block lock
- Revised OTP section

Rev. D – 05/16

- Clarified 8-bit ECC per sector
- Replaced W9 package with WB UDFN
- Updated the parameter page data
- Updated I/O capacitance to 9pF

Rev. C – 01/16

- Updated functional block diagram
- Updated the parameter table
- Updated electrical specifications per characterization data
- Updated read x4 timing diagram
- Updated read and program timing diagrams to reflect 2Gb and 1Gb dummy bits

Rev. B – 10/15

- Updates to ensure consistency with NAND technology

Rev. A – 06/15

- Initial release

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Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.

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