FUJITSU SEMICONDUCTOR
DATA SHEET

DS501-00012-6v0-E

*Memory FRAM*

# 64 K (8 K × 8) Bit SPI

# MB85RS64

## ■ DESCRIPTION

MB85RS64 is a FRAM (Ferroelectric Random Access Memory) chip in a configuration of 8,192 words × 8 bits, using the ferroelectric process and silicon gate CMOS process technologies for forming the nonvolatile memory cells.
MB85RS64 adopts the Serial Peripheral Interface (SPI).
The MB85RS64 is able to retain data without using a back-up battery, as is needed for SRAM.
The memory cells used in the MB85RS64 can be used for $10^{12}$ read/write operations, which is a significant improvement over the number of read and write operations supported by Flash memory and $E^2$PROM.
MB85RS64 does not take long time to write data like Flash memories or $E^2$PROM, and MB85RS64 takes no wait time.

## ■ FEATURES

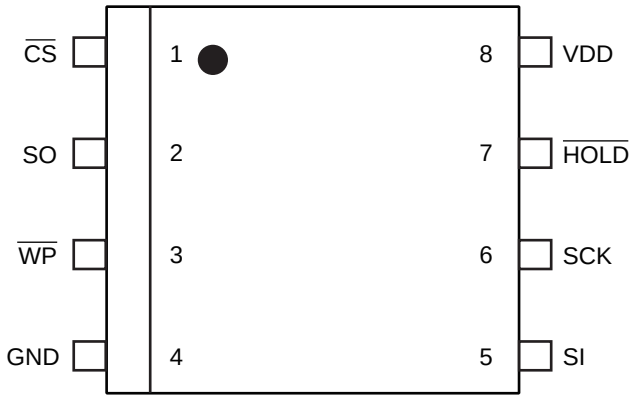
- Bit configuration : 8,192 words × 8 bits
- Serial Peripheral Interface : SPI (Serial Peripheral Interface)
  Correspondent to SPI mode 0 (0, 0) and mode 3 (1, 1)
- Operating frequency : 20 MHz (Max)
- High endurance : $10^{12}$ times / byte
- Data retention : 10 years ( + 85 °C), 95 years ( + 55 °C), over 200 years ( + 35 °C)
- Operating power supply voltage : 2.7 V to 3.6 V
- Low power consumption : Operating power supply current 1.5 mA (Typ@20 MHz)
  Standby current 5 μA (Typ)
- Operation ambient temperature range : − 40 °C to +85 °C
- Package : 8-pin plastic SOP (FPT-8P-M02) RoHS compliant

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扫码查规格书

## ■ PIN ASSIGNMENT

(TOP VIEW)



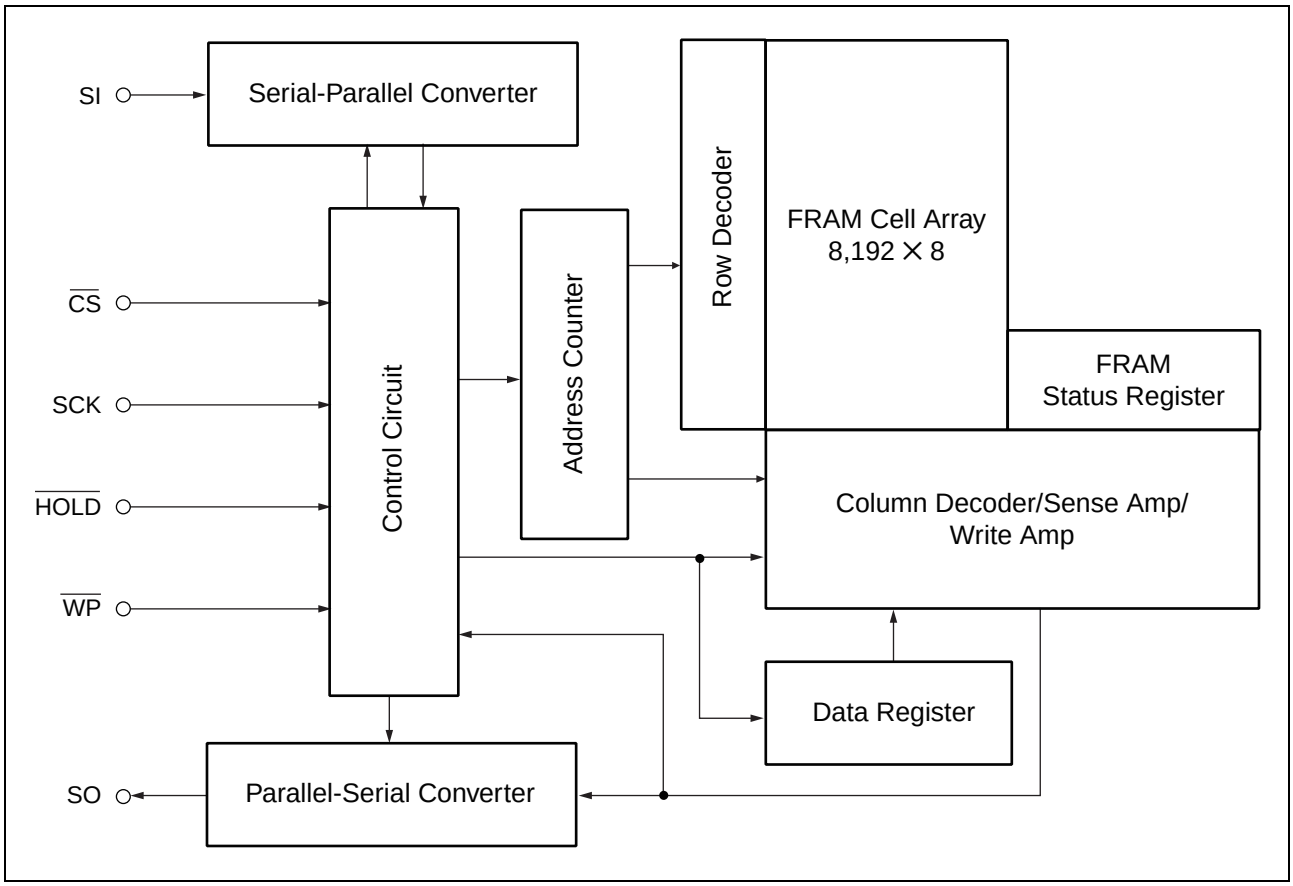

(FPT-8P-M02)

## ■ PIN FUNCTIONAL DESCRIPTIONS

| Pin No. | Pin Name | Functional description |
|---|---|---|
| 1 | $\overline{CS}$ | Chip Select pin<br>This is an input pin to make chip select. When $\overline{CS}$ is the “H” level, device is in deselect (standby) status and SO becomes High-Z. Inputs from other pins are ignored at this time. When $\overline{CS}$ is the “L” level, device is in select (active) status. $\overline{CS}$ has to be the “L” level before inputting op-code. The Chip Select pin is pulled up internally to the VDD pin. |
| 3 | $\overline{WP}$ | Write Protect pin<br>This is a pin to control writing to a status register. The writing of status register (see “■ STATUS REGISTER”) is protected in related with $\overline{WP}$ and WPEN. See “■WRITING PROTECT” for detail. |
| 7 | $\overline{HOLD}$ | Hold pin<br>This pin is used to interrupt serial input/output without making chip deselect. When $\overline{HOLD}$ is the “L” level, hold operation is activated, SO becomes High-Z, and SCK and SI become don’t care. While the hold operation, $\overline{CS}$ shall be retained the “L” level. |
| 6 | SCK | Serial Clock pin<br>This is a clock input pin to input/output serial data. SI is loaded synchronously to a rising edge, SO is output synchronously to a falling edge. |
| 5 | SI | Serial Data Input pin<br>This is an input pin of serial data. This inputs op-code, address, and writing data. |
| 2 | SO | Serial Data Output pin<br>This is an output pin of serial data. Reading data of FRAM memory cell array and status register are output. This is High-Z during standby. |
| 8 | VDD | Supply Voltage pin |
| 4 | GND | Ground pin |


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## ■ BLOCK DIAGRAM

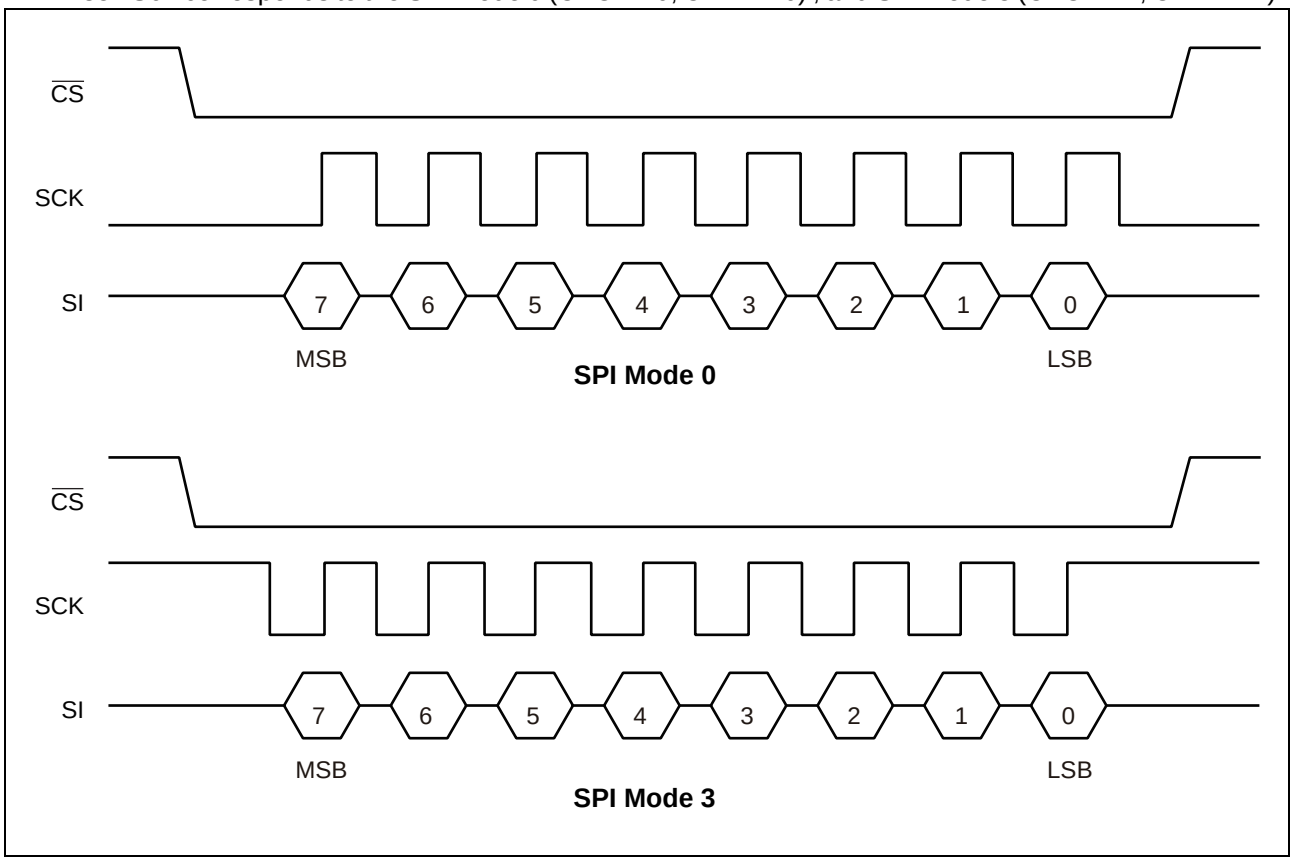




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## ■ SPI MODE

MB85RS64 corresponds to the SPI mode 0 (CPOL = 0, CPHA = 0) , and SPI mode 3 (CPOL = 1, CPHA = 1) .

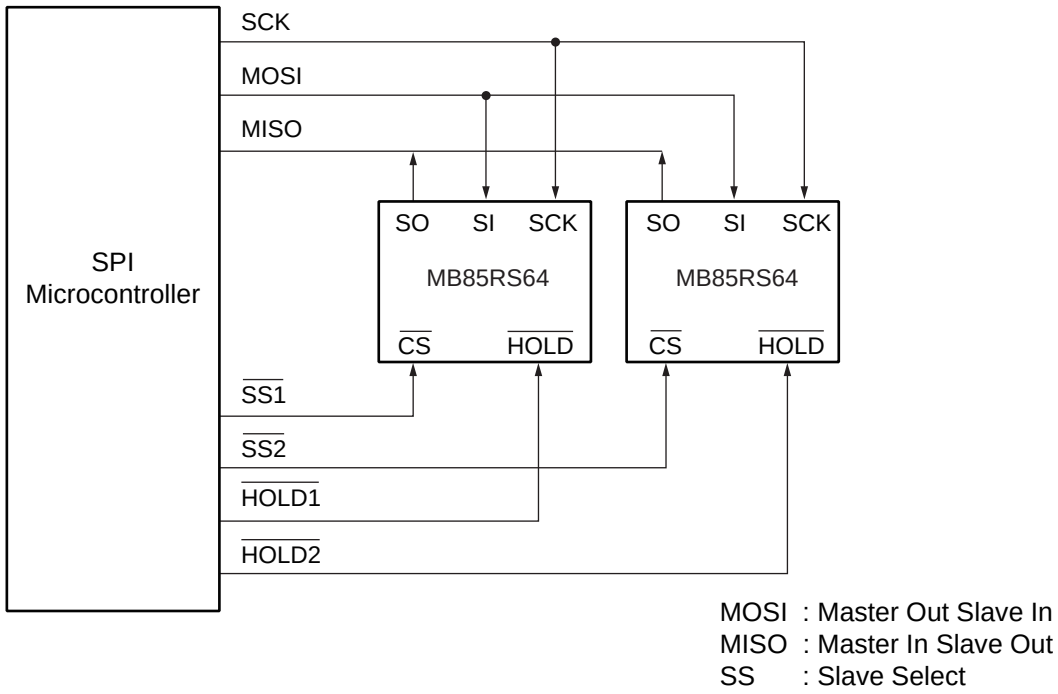




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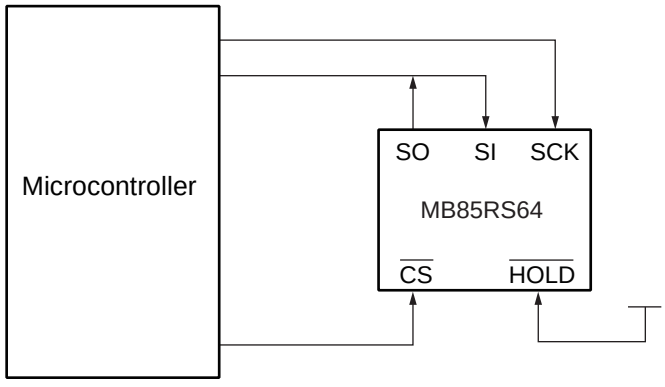
## ■ SERIAL PERIPHERAL INTERFACE (SPI)

MB85RS64 works as a slave of SPI. More than 2 devices can be connected by using microcontroller equipped with SPI port. By using a microcontroller not equipped with SPI port, SI and SO can be bus connected to use.




MOSI : Master Out Slave In
MISO : Master In Slave Out
SS : Slave Select

**System Configuration with SPI Port**




**System Configuration without SPI Port**


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## ■ STATUS REGISTER

| Bit No. | Bit Name | Function |
|---|---|---|
| 7 | WPEN | Status Register Write Protect<br>This is a bit composed of nonvolatile memories (FRAM). WPEN protects writing to a status register (see "■ WRITING PROTECT") relating with $\overline{WP}$ input. Writing with the WRSR command and reading with the RDSR command are possible. |
| 6 to 4 | — | Not Used Bits<br>These are bits composed of nonvolatile memories, writing with the WRSR command is possible, and "000" is written before shipment. These bits are not used but they are read with the RDSR command. |
| 3 | BP1 | Block Protect<br>This is a bit composed of nonvolatile memory. This defines size of write protect block for the WRITE command (see "■ BLOCK PROTECT"). Writing with the WRSR command and reading with the RDSR command are possible. |
| 2 | BP0 | |
| 1 | WEL | Write Enable Latch<br>This indicates FRAM Array and status register are writable. The WREN command is for setting, and the WRDI command is for resetting. With the RDSR command, reading is possible but writing is not possible with the WRSR command. WEL is reset after the following operations.<br>After power ON.<br>After WRDI command recognition.<br>At the rising edge of $\overline{CS}$ after WRSR command recognition.<br>At the rising edge of $\overline{CS}$ after WRITE command recognition. |
| 0 | 0 | This is a bit fixed to "0". |

## ■ OP-CODE

MB85RS64 accepts 6 kinds of command specified in op-code. Op-code is a code composed of 8 bits shown in the table below. Do not input invalid codes other than those codes. If $\overline{CS}$ is risen while inputting op-code, the command are not performed.

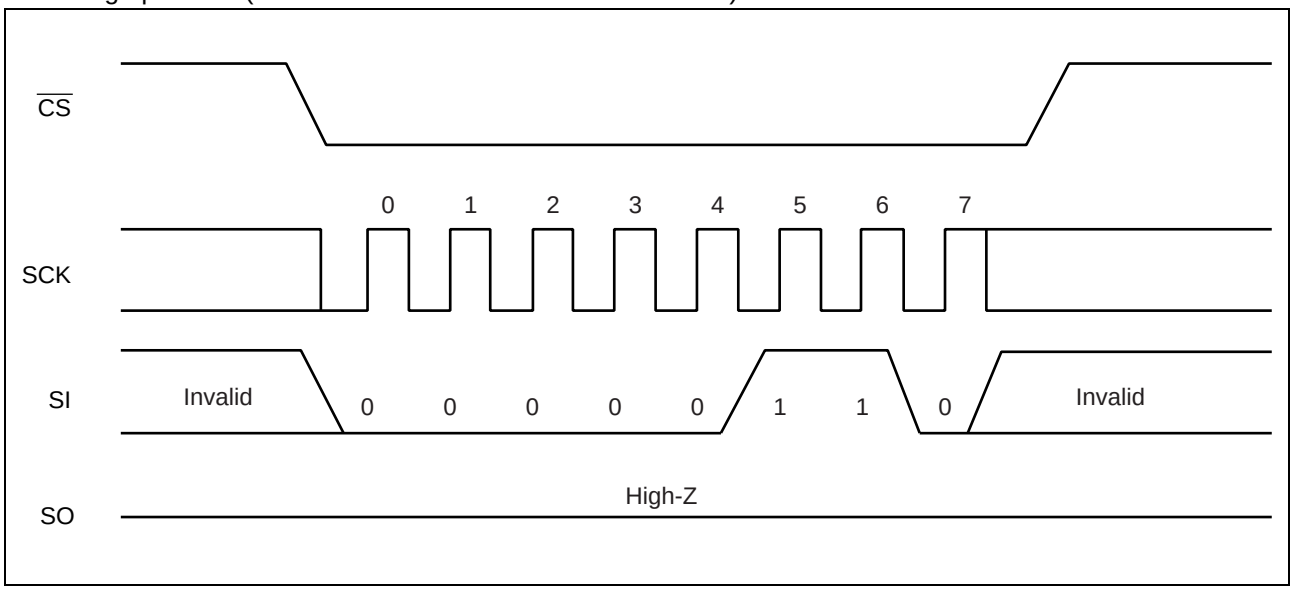
| Name | Description | Op-code |
|---|---|---|
| WREN | Set Write Enable Latch | $0000\ 0110_B$ |
| WRDI | Reset Write Enable Latch | $0000\ 0100_B$ |
| RDSR | Read Status Register | $0000\ 0101_B$ |
| WRSR | Write Status Register | $0000\ 0001_B$ |
| READ | Read Memory Code | $0000\ 0011_B$ |
| WRITE | Write Memory Code | $0000\ 0010_B$ |


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## ■ COMMAND

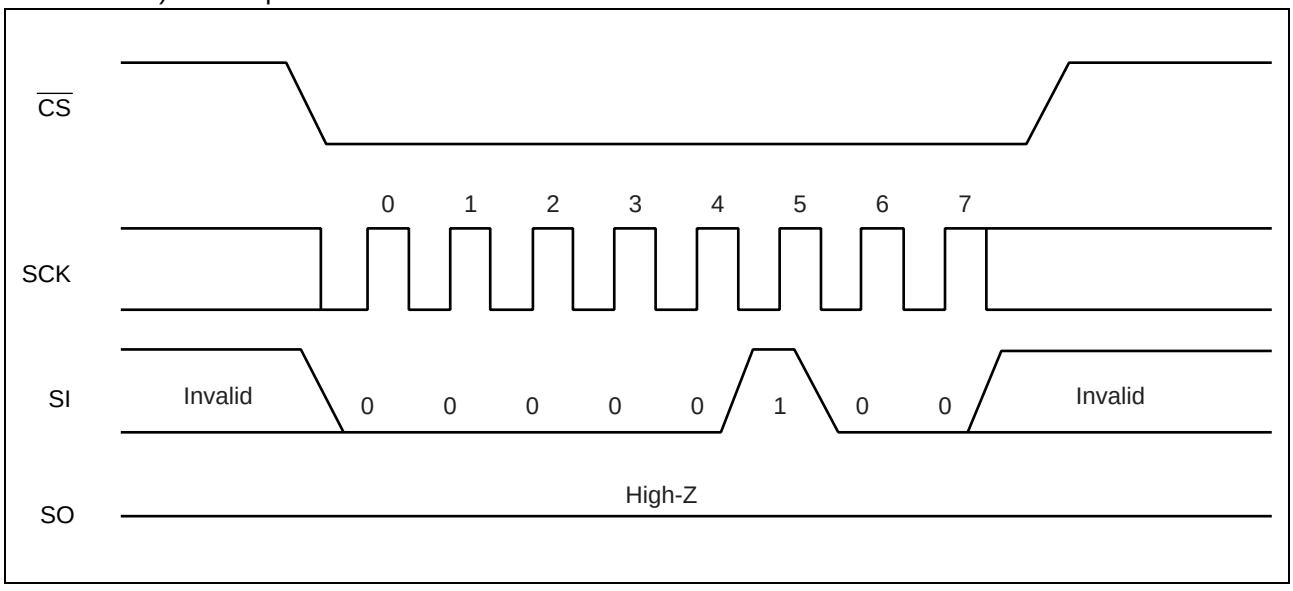
**• WREN**

The WREN command sets WEL (Write Enable Latch) . WEL shall be set with the WREN command before writing operation (WRSR command and WRITE command) .




**• WRDI**

The WRDI command resets WEL (Write Enable Latch) . Writing operation (WRITE command and WRSR command) are not performed when WEL is reset.

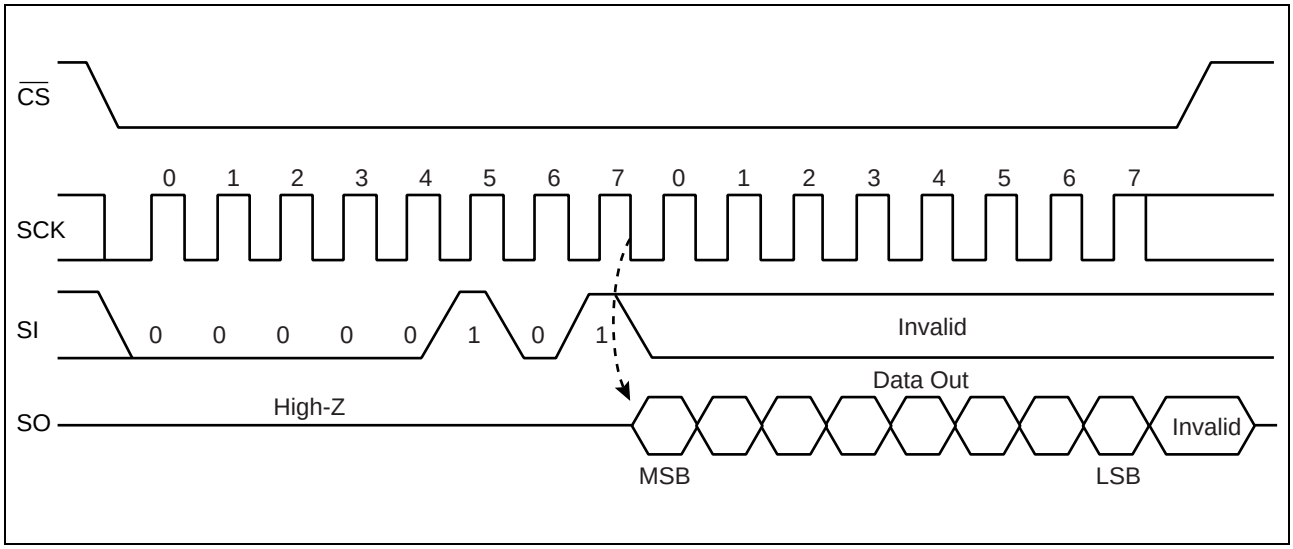




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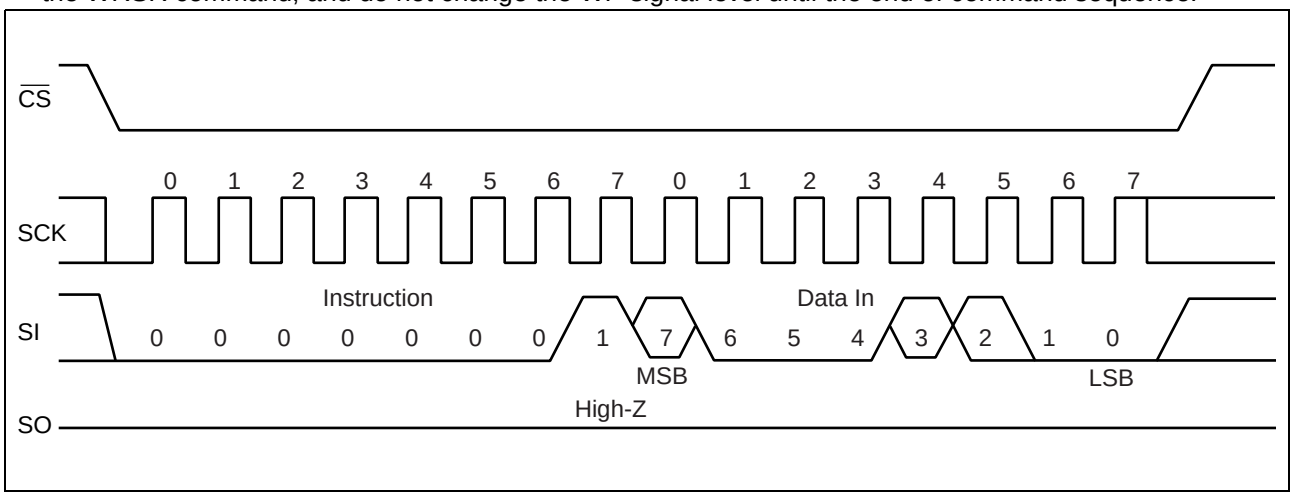
• **RDSR**

The RDSR command reads status register data. After op-code of RDSR is input to SI, 8-cycle clock is input to SCK. The SI value is invalid during this time. SO is output synchronously to a falling edge of SCK. In the RDSR command, repeated reading of status register is enabled by sending SCK continuously before rising of $\overline{CS}$.




• **WRSR**

The WRSR command writes data to the nonvolatile memory bit of status register. After performing WRSR op-code to a SI pin, 8 bits writing data is input. WEL (Write Enable Latch) is not able to be written with WRSR command. A SI value correspondent to bit 1 is ignored. Bit 0 of the status register is fixed to “0” and cannot be written. The SI value corresponding to bit 0 is ignored. The $\overline{WP}$ signal level shall be fixed before performing the WRSR command, and do not change the $\overline{WP}$ signal level until the end of command sequence.

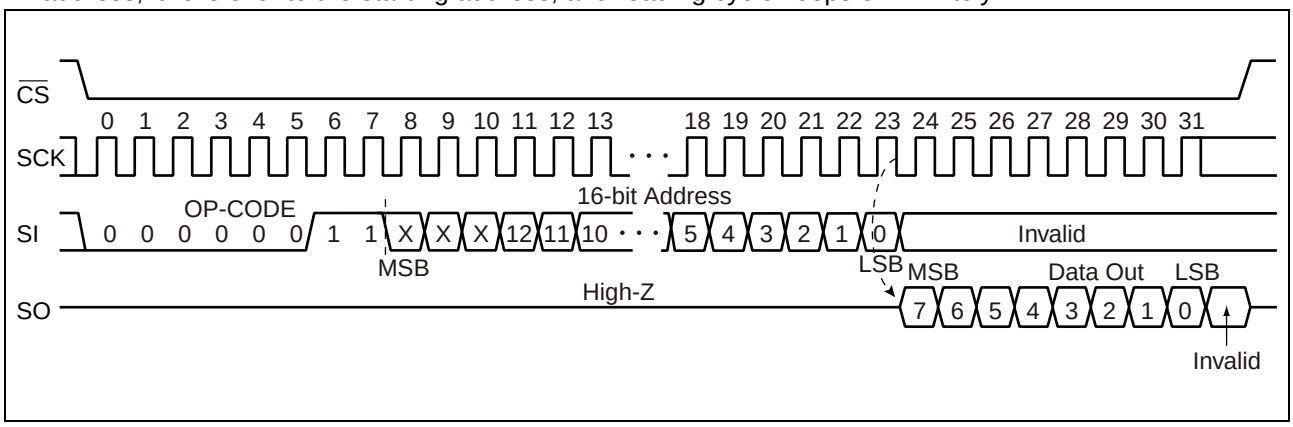




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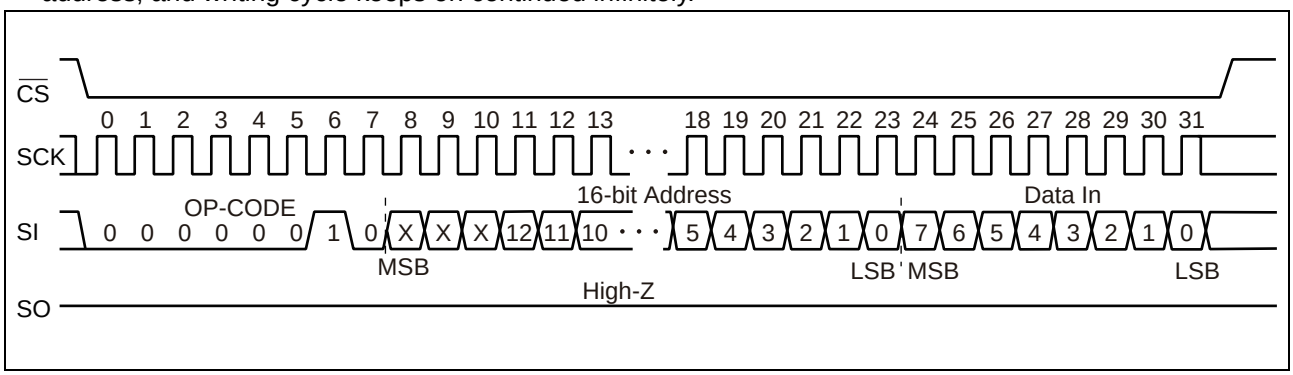
• **READ**

The READ command reads FRAM memory cell array data. Arbitrary 16 bits address and op-code of READ are input to SI. The 3-bit upper address bit is invalid. Then, 8-cycle clock is input to SCK. SO is output synchronously to the falling edge of SCK. While reading, the SI value is invalid. When $\overline{CS}$ is risen, the READ command is completed, but keeps on reading with automatic address increment which is enabled by continuously sending clocks to SCK in unit of 8 cycles before $\overline{CS}$ rising. When it reaches the most significant address, it rolls over to the starting address, and reading cycle keeps on infinitely.




• **WRITE**

The WRITE command writes data to FRAM memory cell array. WRITE op-code, arbitrary 16 bits of address and 8 bits of writing data are input to SI. The 3-bit upper address bit is invalid. When 8 bits of writing data is input, data is written to FRAM memory cell array. Risen $\overline{CS}$ will terminate the WRITE command. However, if you continue sending the writing data for 8 bits each before $\overline{CS}$ rising, it is possible to continue writing with automatic address increment. When it reaches the most significant address, it rolls over to the starting address, and writing cycle keeps on continued infinitely.





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## ■ BLOCK PROTECT

Writing protect block for WRITE command is configured by the value of BP0 and BP1 in the status register.

| BP1 | BP0 | Protected Block |
|---|---|---|
| 0 | 0 | None |
| 0 | 1 | $1800_H$ to $1FFF_H$ (upper 1/4) |
| 1 | 0 | $1000_H$ to $1FFF_H$ (upper 1/2) |
| 1 | 1 | $0000_H$ to $1FFF_H$ (all) |

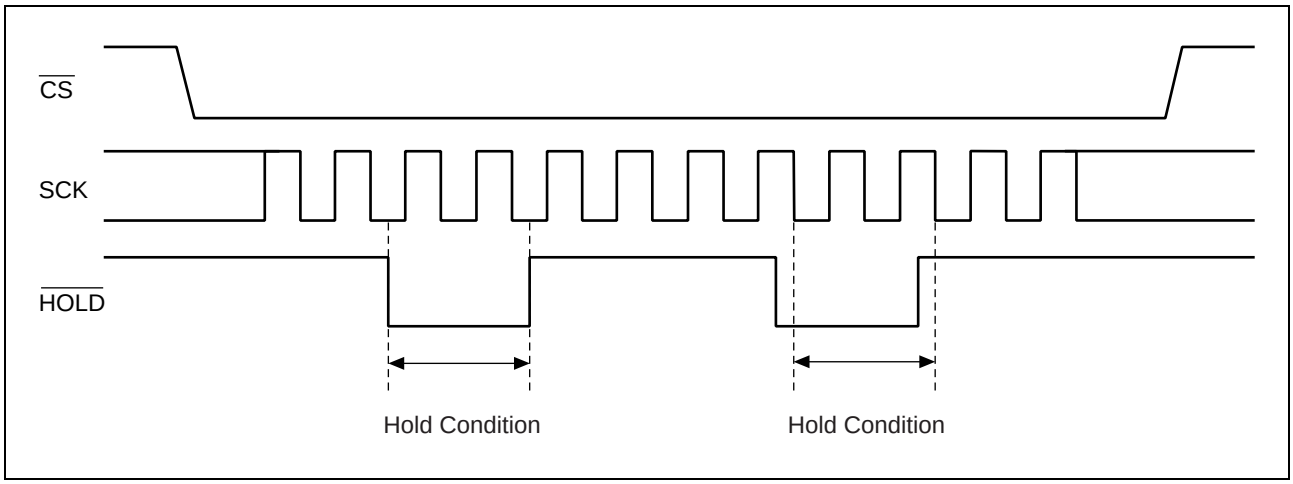
## ■ WRITING PROTECT

Writing operation of the WRITE command and the WRSR command are protected with the value of WEL, WPEN, $\overline{WP}$ as shown in the table.

| WEL | WPEN | $\overline{WP}$ | Protected Blocks | Unprotected Blocks | Status Register |
|---|---|---|---|---|---|
| 0 | X | X | Protected | Protected | Protected |
| 1 | 0 | X | Protected | Unprotected | Unprotected |
| 1 | 1 | 0 | Protected | Unprotected | Protected |
| 1 | 1 | 1 | Protected | Unprotected | Unprotected |

## ■ HOLD OPERATION

Hold status is retained without aborting a command if $\overline{HOLD}$ is the “L” level while $\overline{CS}$ is the “L” level. The timing for starting and ending hold status depends on the SCK to be the “H” level or the “L” level when a $\overline{HOLD}$ pin input is transited to the hold condition as shown in the diagram below. In case the $\overline{HOLD}$ pin transited to “L” level when SCK is “L” level, return the $\overline{HOLD}$ pin to “H” level at SCK being “L” level. In the same manner, in case the $\overline{HOLD}$ pin transited to “L” level when SCK is “H” level, return the $\overline{HOLD}$ pin to “H” level at SCK being “H” level. Arbitrary command operation is interrupted in hold status, SCK and SI inputs become don’t care. And, SO becomes High-Z while reading command (RDSR, READ). If $\overline{CS}$ is rising during hold status, a command is aborted. In case the command is aborted before its recognition, WEL holds the value before transition to hold status.





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## ■ ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Rating | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| Power supply voltage* | $V_{DD}$ | – 0.5 | + 4.0 | V |
| Input voltage* | $V_{IN}$ | – 0.5 | $V_{DD}$ + 0.5 | V |
| Output voltage* | $V_{OUT}$ | – 0.5 | $V_{DD}$ + 0.5 | V |
| Operation ambient temperature | $T_A$ | – 40 | + 85 | °C |
| Storage temperature | Tstg | – 55 | + 125 | °C |

*:These parameters are based on the condition that $V_{SS}$ is 0 V.

WARNING: Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings.
Do not exceed any of these ratings.

## ■ RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Value | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| Power supply voltage*1 | $V_{DD}$ | 2.7 | 3.3 | 3.6 | V |
| Operation ambient temperature*2 | $T_A$ | – 40 | — | + 85 | °C |

*1: These parameters are based on the condition that $V_{SS}$ is 0 V.

*2: Ambient temperature when only this device is working. Please consider it to be the almost same as the package surface temperature.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.

Any use of semiconductor devices will be under their recommended operating condition.
Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure.

No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.


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## ■ ELECTRICAL CHARACTERISTICS

### 1. DC Characteristics

(within recommended operating conditions)

| Parameter | Symbol | Condition | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| Input leakage current | $\|I_{LI}\|$ | $0 \le \overline{CS} < V_{DD}$ | — | — | 200 | µA |
| | | $\overline{CS} = V_{DD}$ | — | — | 10 | |
| | | $\overline{WP}$, $\overline{HOLD}$, SCK, SI = 0 V to $V_{DD}$ | — | — | 10 | |
| Output leakage current | $\|I_{LO}\|$ | SO = 0 V to $V_{DD}$ | — | — | 10 | µA |
| Operating power supply current | $I_{DD}$ | SCK = 10 MHz | — | 0.75 | — | mA |
| | | SCK = 20 MHz | — | 1.5 | 2.4 | mA |
| Standby current | $I_{SB}$ | SCK = SI = $\overline{CS}$ = $V_{DD}$ | — | 5 | 15 | µA |
| Input high voltage | $V_{IH}$ | $V_{DD}$ = 2.7 V to 3.6 V | $V_{DD} \times 0.8$ | — | $V_{DD} + 0.3$ | V |
| Input low voltage | $V_{IL}$ | $V_{DD}$ = 2.7 V to 3.6 V | – 0.5 | — | $V_{DD} \times 0.2$ | V |
| Output high voltage | $V_{OH}$ | $I_{OH}$ = –2 mA | $V_{DD}$ – 0.5 | — | $V_{DD}$ | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 2 mA | $V_{SS}$ | — | 0.4 | V |
| Pull up resistance for $\overline{CS}$ | RP | — | 18 | 33 | 80 | kΩ |


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## 2. AC Characteristics

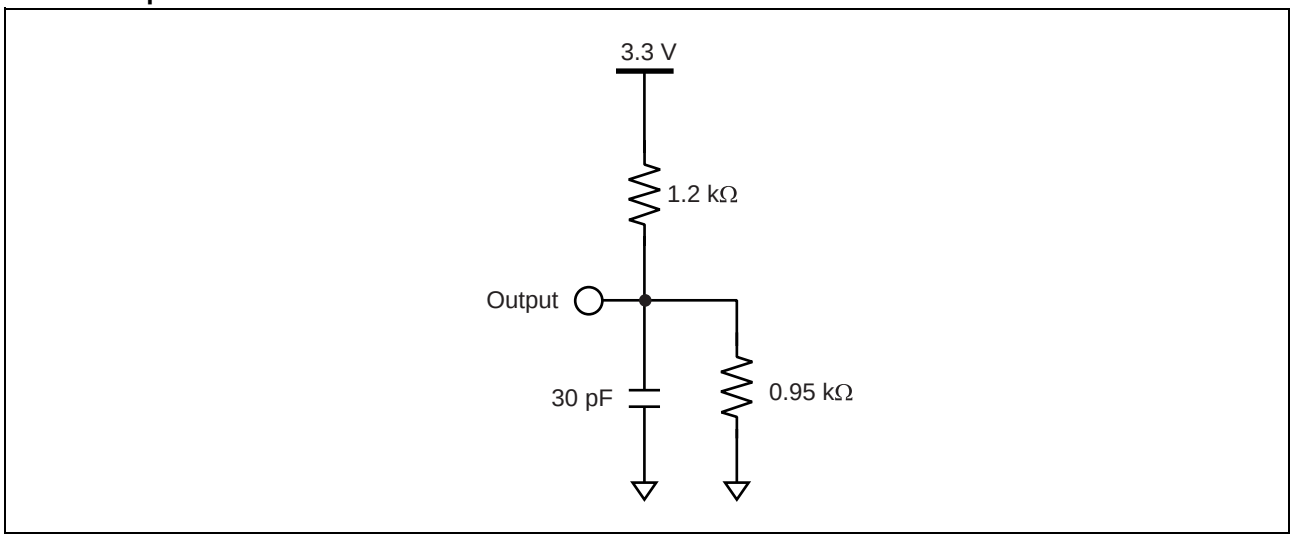
| Parameter | Symbol | Value | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| SCK clock frequency | $f_{CK}$ | 0 | 20 | MHz |
| Clock high time | $t_{CH}$ | 25 | — | ns |
| Clock low time | $t_{CL}$ | 25 | — | ns |
| Chip select set up time | $t_{CSU}$ | 10 | — | ns |
| Chip select hold time | $t_{CSH}$ | 10 | — | ns |
| Output disable time | $t_{OD}$ | — | 20 | ns |
| Output data valid time | $t_{ODV}$ | — | 18 | ns |
| Output hold time | $t_{OH}$ | 0 | — | ns |
| Deselect time | $t_{D}$ | 60 | — | ns |
| Data rising time | $t_{R}$ | — | 50 | ns |
| Data falling time | $t_{F}$ | — | 50 | ns |
| Data set up time | $t_{SU}$ | 5 | — | ns |
| Data hold time | $t_{H}$ | 5 | — | ns |
| $\overline{\text{HOLD}}$ set up time | $t_{HS}$ | 10 | — | ns |
| $\overline{\text{HOLD}}$ hold time | $t_{HH}$ | 10 | — | ns |
| $\overline{\text{HOLD}}$ output floating time | $t_{HZ}$ | — | 20 | ns |
| $\overline{\text{HOLD}}$ output active time | $t_{LZ}$ | — | 20 | ns |

### AC Test Condition

Power supply voltage : 2.7 V to 3.6 V
Operation ambient temperature : − 40 °C to + 85 °C
Input voltage magnitude : 0.3 V to 2.7 V
Input rising time : 5 ns
Input falling time : 5 ns
Input judge level : $V_{DD}/2$
Output judge level : $V_{DD}/2$


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**AC Load Equivalent Circuit**



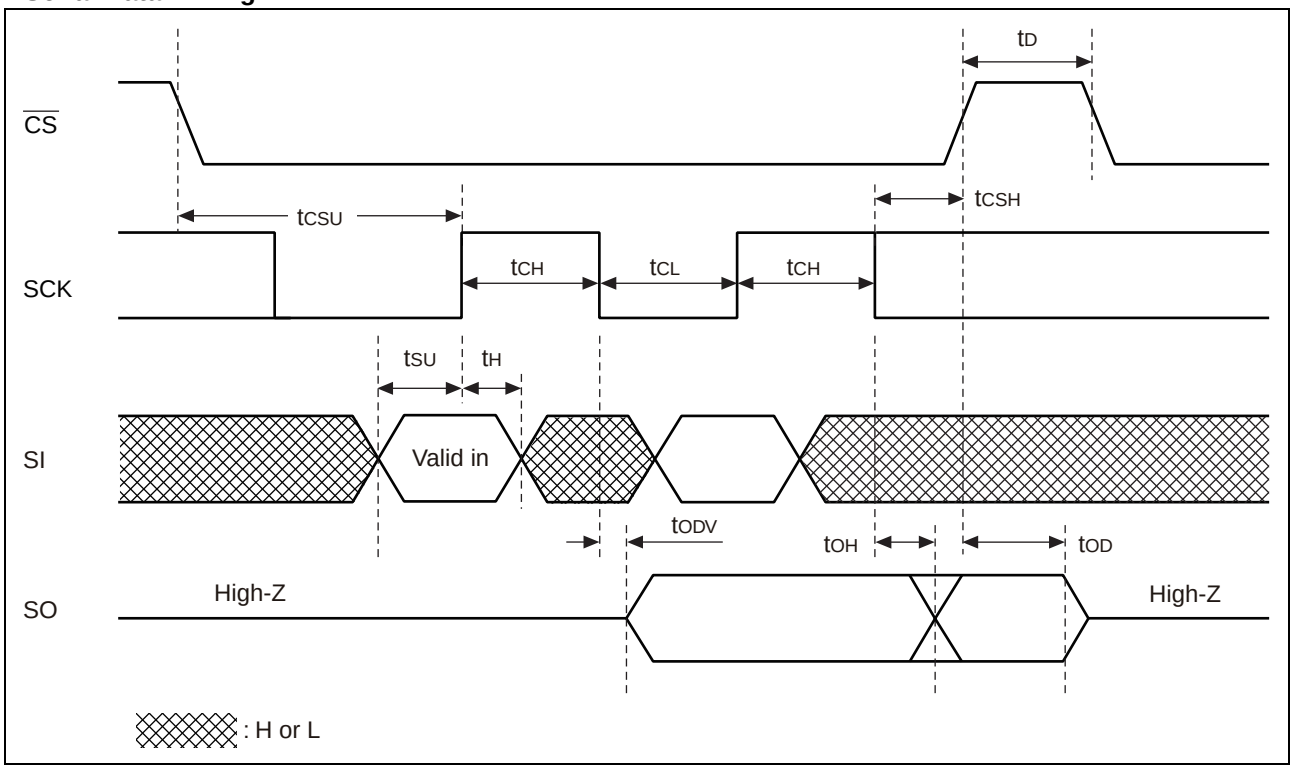

## 3. Pin Capacitance

| Parameter | Symbol | Conditions | Value | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| Output capacitance | $C_O$ | $V_{DD} = V_{IN} = V_{OUT} = 0$ V<br>f = 1 MHz, $T_A$ = + 25 °C | — | 10 | pF |
| Input capacitance | $C_I$ | | — | 10 | pF |

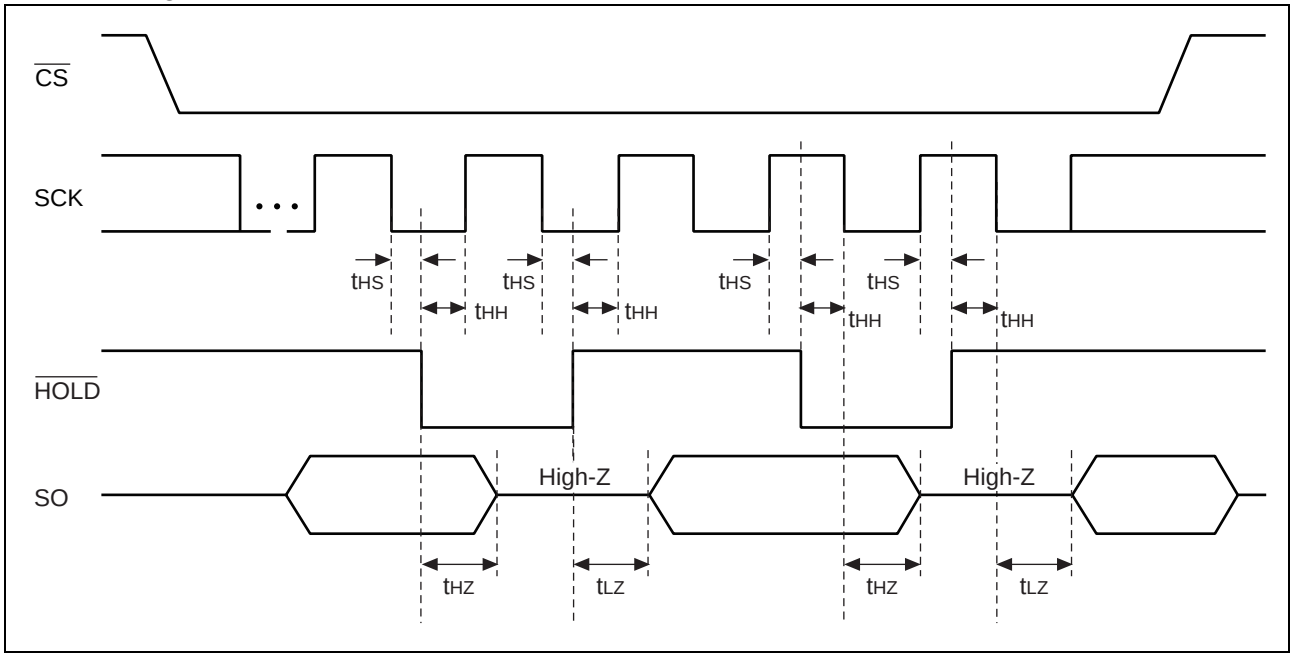

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## ■ TIMING DIAGRAM

**• Serial Data Timing**



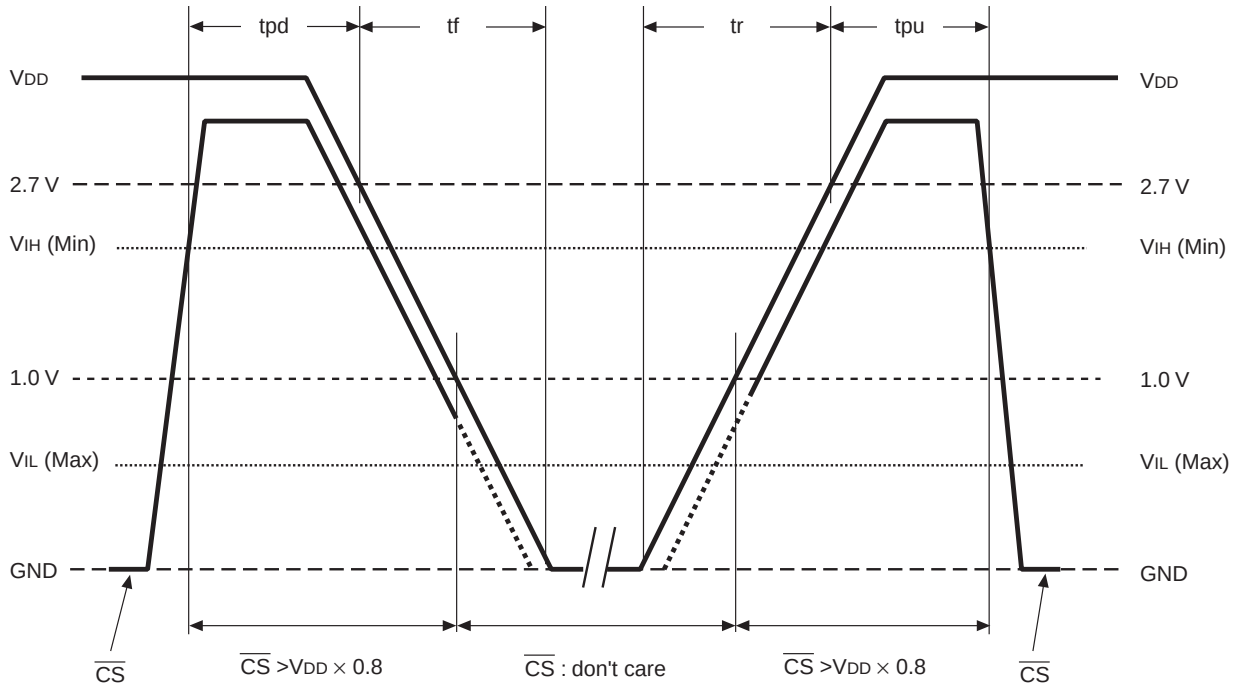

**• Hold Timing**





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## ■ POWER ON/OFF SEQUENCE




* : $\overline{CS}$ (Max) < $V_{DD}$ + 0.3 V

| Parameter | Symbol | Value | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| $\overline{CS}$ level hold time at power OFF | tpd | 400 | — | ns |
| $\overline{CS}$ level hold time at power ON | tpu | 0.1 | — | ms |
| Power supply falling time | tf | 100 | — | µs/V |
| Power supply rising time | tr | 30 | — | µs/V |

If the device does not operate within the specified conditions of read cycle, write cycle or power on/off sequence, memory data can not be guaranteed.

## ■ FRAM CHARACTERISTICS

| Item | Min | Max | Unit | Parameter |
|---|---|---|---|---|
| Read/Write Endurance*1 | $10^{12}$ | — | Times/byte | Operation Ambient Temperature $T_A$ = + 85 °C |
| Data Retention*2 | 10 | — | Years | Operation Ambient Temperature $T_A$ = + 85 °C |
| | 95 | — | | Operation Ambient Temperature $T_A$ = + 55 °C |
| | ≥ 200 | — | | Operation Ambient Temperature $T_A$ = + 35 °C |

*1 : Total number of reading and writing defines the minimum value of endurance, as an FRAM memory operates with destructive readout mechanism.

*2 : Minimum values define retention time of the first reading/writing data right after shipment, and these values are calculated by qualification results.

## ■ NOTE ON USE

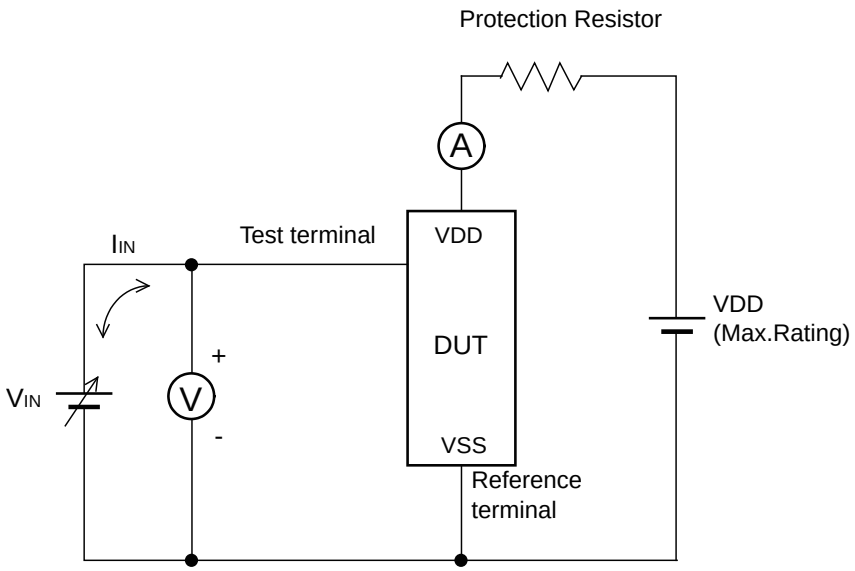
We recommend programming of the device after reflow. Data written before reflow cannot be guaranteed.


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## ■ ESD AND LATCH-UP

| Test | DUT | Value |
|---|---|---|
| ESD HBM (Human Body Model)<br>JESD22-A114 compliant | MB85RS64PNF-G-JNE1 | ≥ \|2000 V\| |
| ESD MM (Machine Model)<br>JESD22-A115 compliant | | ≥ \|200 V\| |
| ESD CDM (Charged Device Model)<br>JESD22-C101 compliant | | ≥ \|1000 V\| |
| Latch-Up (I-test)<br>JESD78 compliant | | — |
| Latch-Up ($V_{supply}$ overvoltage test)<br>JESD78 compliant | | — |
| Latch-Up (Current Method)<br>Proprietary method | | — |
| Latch-Up (C-V Method)<br>Proprietary method | | ≥ \|200 V\| |

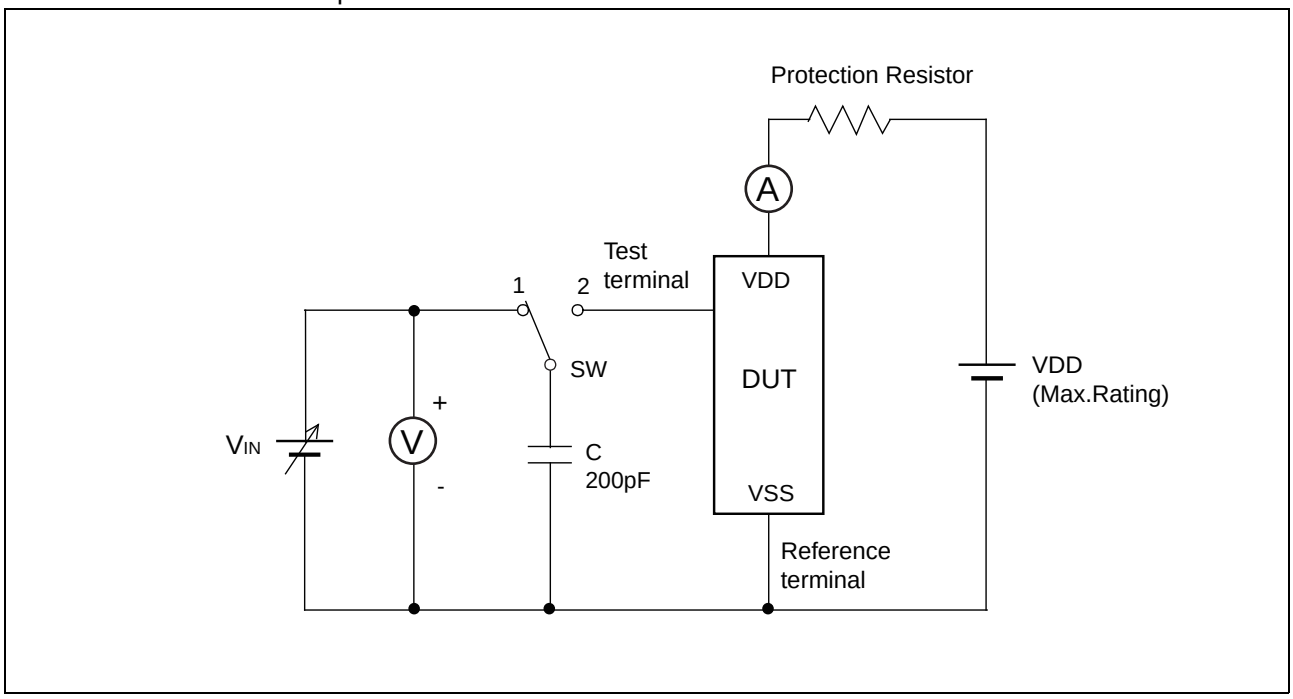
- Current method of Latch-Up Resistance Test




Note : The voltage $V_{IN}$ is increased gradually and the current $I_{IN}$ of 300 mA at maximum shall flow.
Confirm the latch up does not occur under $I_{IN}$ = ±300 mA.
In case the specific requirement is specified for I/O and $I_{IN}$ cannot be 300 mA, the voltage shall be increased to the level that meets the specific requirement.


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• C-V method of Latch-Up Resistance Test




Note : Charge voltage alternately switching 1 and 2 approximately 2 sec interval. This switching process is considered as one cycle.
Repeat this process 5 times. However, if the latch-up condition occurs before completing 5 times, this test must be stopped immediately.

## ■ REFLOW CONDITIONS AND FLOOR LIFE

[ JEDEC MSL ] : Moisture Sensitivity Level 3 (ISP/JEDEC J-STD-020D)

## ■ CURRENT STATUS ON CONTAINED RESTRICTED SUBSTANCES

This product complies with the regulations of REACH Regulations, EU RoHS Directive and China RoHS.


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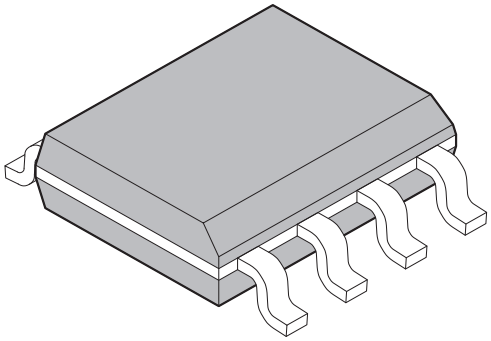
## ■ ORDERING INFORMATION

| Part number | Package | Shipping form | Minimum shipping quantity |
|---|---|---|---|
| MB85RS64PNF-G-JNE1 | 8-pin plastic SOP (FPT-8P-M02) | Tube | —* |
| MB85RS64PNF-G-JNERE1 | 8-pin plastic SOP (FPT-8P-M02) | Embossed Carrier tape | 1500 |

*: Please contact our sales office about minimum shipping quantity.

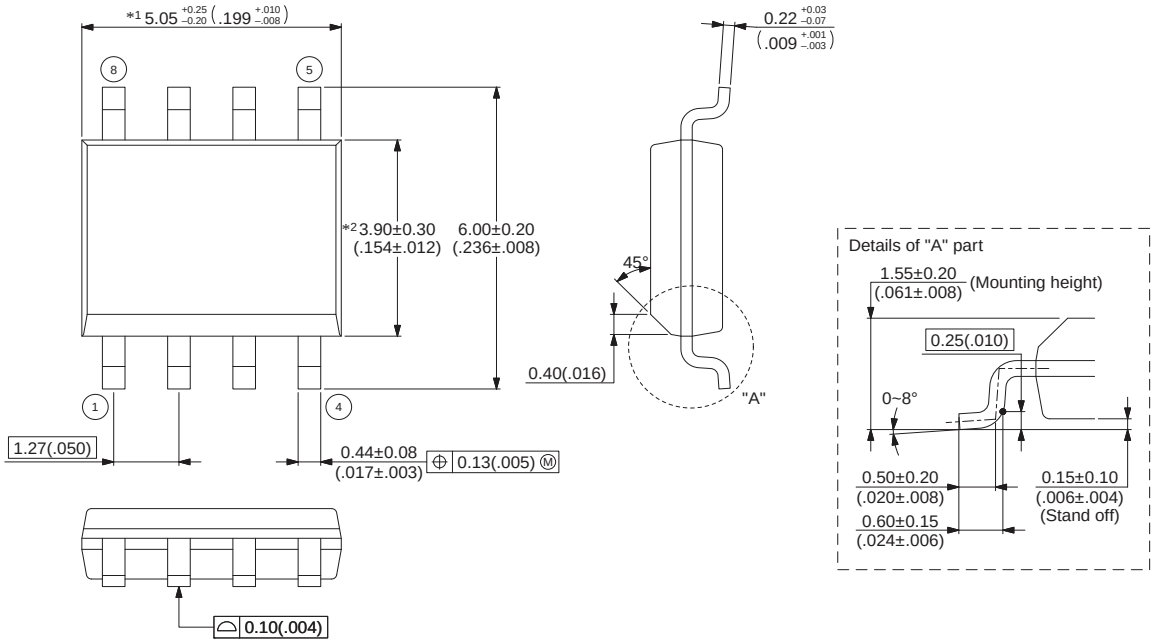

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## ■ PACKAGE DIMENSION

| 8-pin plastic SOP | | |
|---|---|---|
|  (FPT-8P-M02) | Lead pitch | 1.27 mm |
| | Package width × package length | 3.9 mm × 5.05 mm |
| | Lead shape | Gullwing |
| | Sealing method | Plastic mold |
| | Mounting height | 1.75 mm MAX |
| | Weight | 0.06 g |
| | | |

8-pin plastic SOP
(FPT-8P-M02)

Note 1) *1 : These dimensions include resin protrusion.
Note 2) *2 : These dimensions do not include resin protrusion.
Note 3) Pins width and pins thickness include plating thickness.
Note 4) Pins width do not include tie bar cutting remainder.




Dimensions in mm (inches).
Note: The values in parentheses are reference values.

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## ■ MARKING

[MB85RS64PNF-G-JNE1]
[MB85RS64PNF-G-JNERE1]




[FPT-8P-M02]

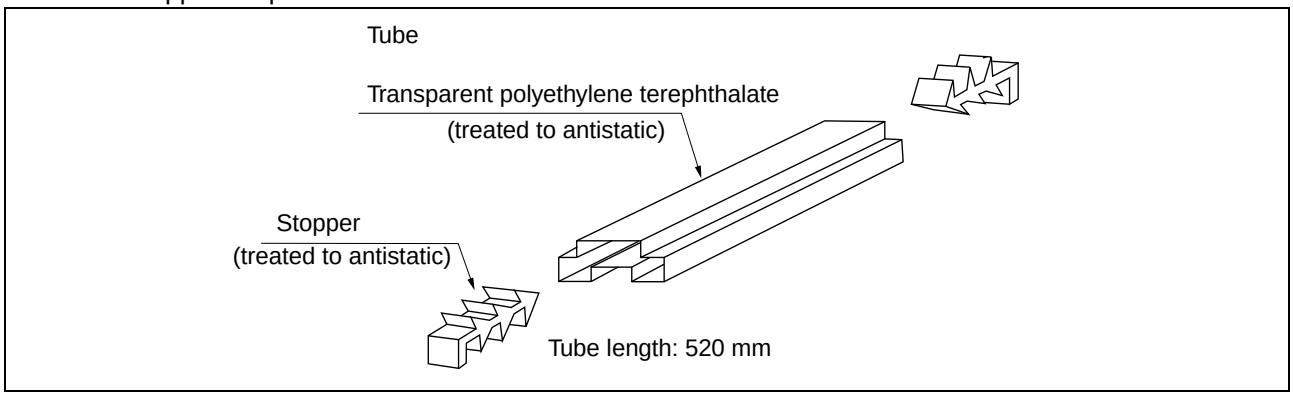

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## ■ PACKING INFORMATION

### 1. Tube

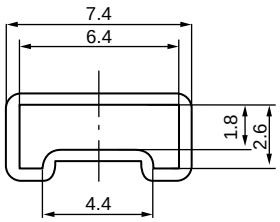
#### 1.1 Tube Dimensions

- Tube/stopper shape




**Tube cross-sections and Maximum quantity**

| Package form | Package code | Maximum quantity | | |
|---|---|---|---|---|
| | | pcs/ tube | pcs/inner box | pcs/outer box |
| SOP, 8, plastic (2) | FPT-8P-M02 | 95 | 7600 | 30400 |



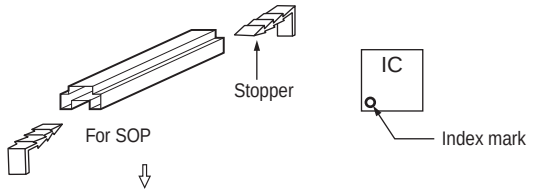
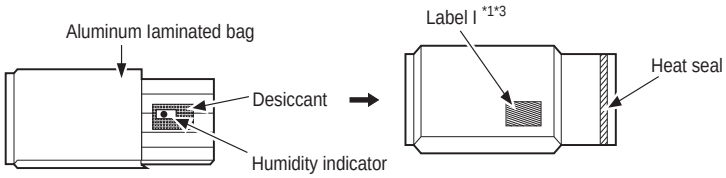
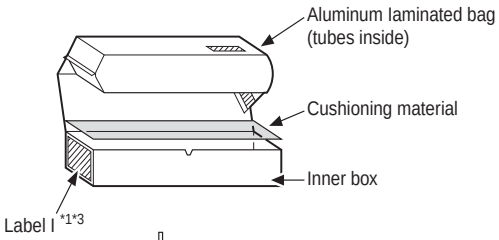
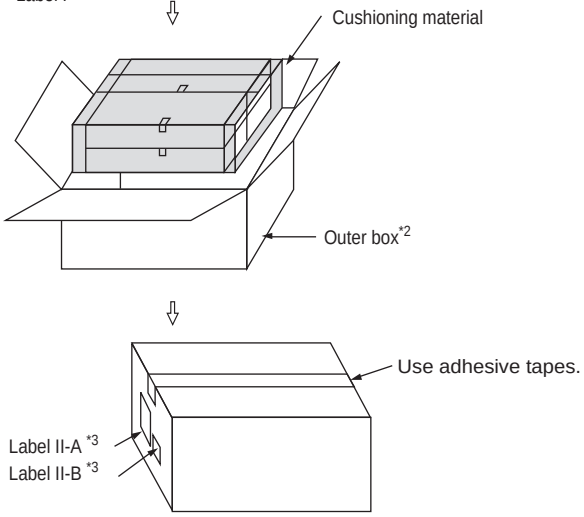

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F08008-SET1-PET:FJ99L-0022-E0008-1-K-3

t = 0.5
Transparent polyethylene terephthalate

(Dimensions in mm)


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### 1.2 Tube Dry pack packing specifications

| | |
|---|---|
| Tube |  |
| Dry pack |  |
| Inner box |  |
| Outer box |  |

*1: For a product of witch part number is suffixed with “E1”, a “ G Pb ” marks is display to the moisture barrier bag and the inner boxes.

*2: The space in the outer box will be filled with empty inner boxes, or cushions, etc.

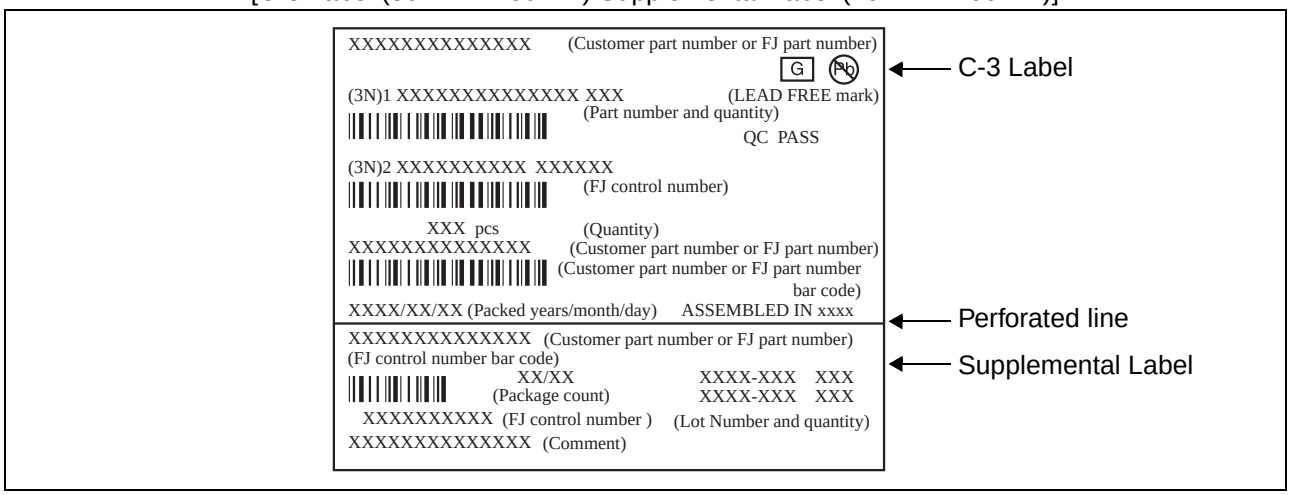
*3: Please refer to an attached sheet about the indication label.

Note: The packing specifications may not be applied when the product is delivered via a distributor.

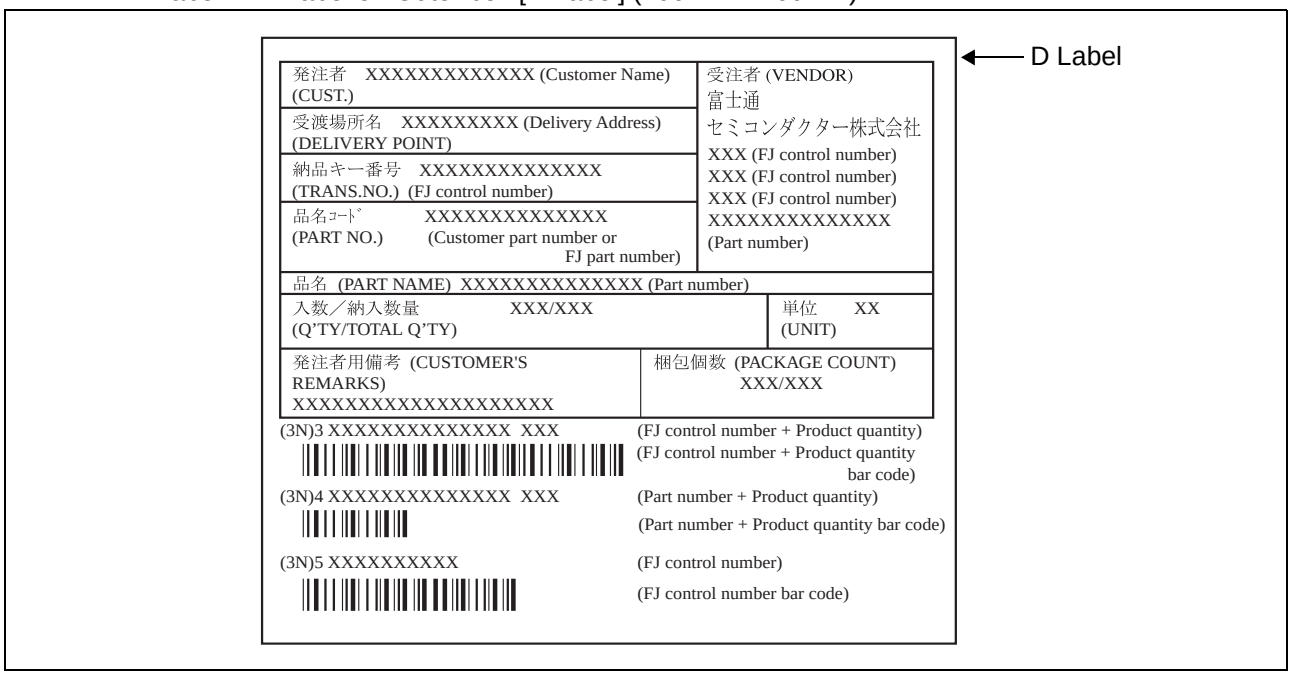

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### 1.3 Product label indicators

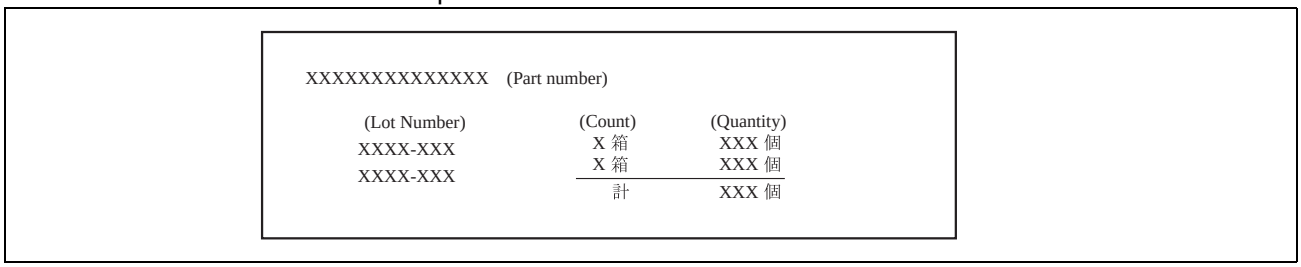
Label I: Label on Inner box/Moisture Barrier Bag/ (It sticks it on the reel for the emboss taping)
[C-3 Label (50mm × 100mm) Supplemental Label (20mm × 100mm)]




Label II-A: Label on Outer box [D Label] (100mm × 100mm)




Label II-B: Outer boxes product indicate

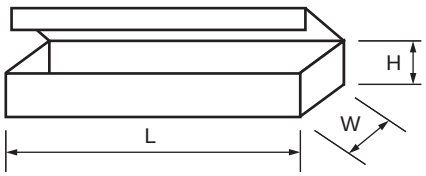



Note: Depending on shipment state, “Label II-A” and “Label II-B” on the external boxes might not be printed.


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### 1.4 Dimensions for Containers

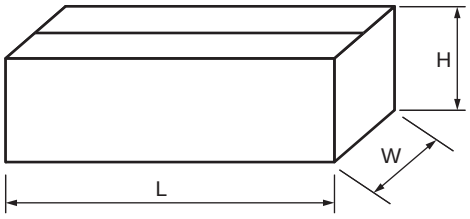
**(1) Dimensions for inner box**




| L | W | H |
|---|---|---|
| 540 | 125 | 75 |

(Dimensions in mm)

**(2) Dimensions for outer box**




| L | W | H |
|---|---|---|
| 565 | 270 | 180 |

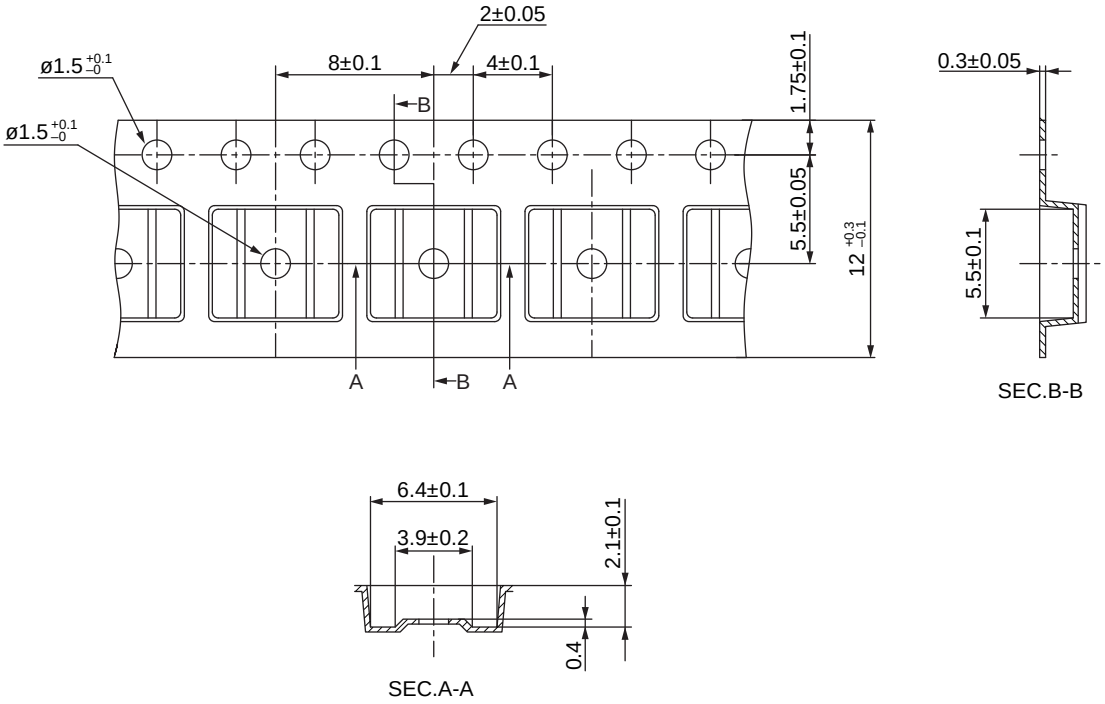
(Dimensions in mm)


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## 2. Emboss Tape

### 2.1 Tape Dimensions

| PKG code | Reel No | Maximum storage capacity | | |
|---|---|---|---|---|
| | | pcs/reel | pcs/inner box | pcs/outer box |
| FPT-8P-M02 | 3 | 1500 | 1500 | 10500 |



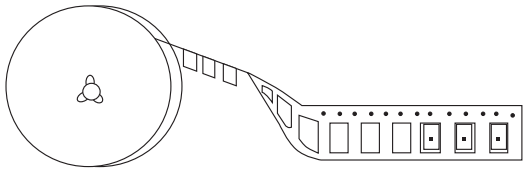

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(Dimensions in mm)

Material : Conductive polystyrene
Heat proof temperature : No heat resistance.
Package should not be baked by using tape and reel.

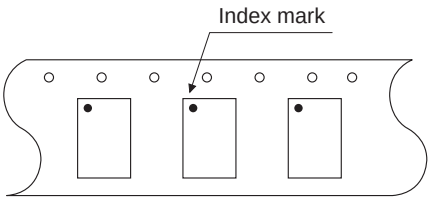

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## 2.2 IC orientation



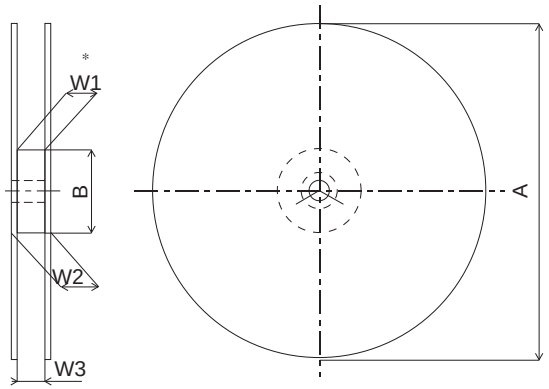
(User Direction of Feed)

• ER type

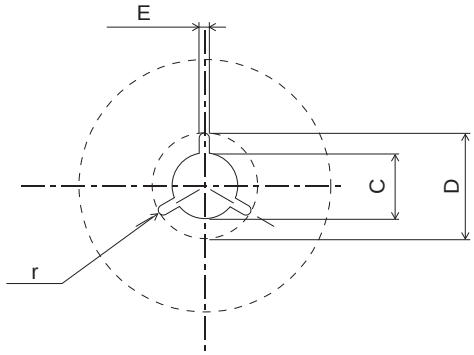



(Reel side) (User Direction of Feed)

## 2.3 Reel dimensions




Reel cutout dimensions



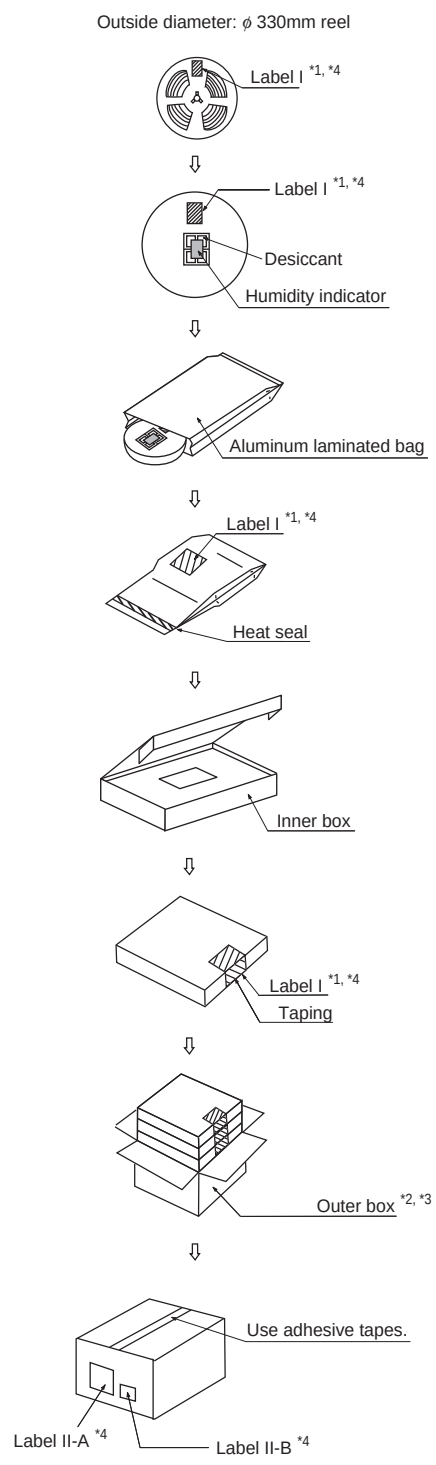

*: Hub unit width dimensions

Dimensions in mm

| Reel No | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Tape width / Symbol | 8 | 12 | | 16 | | 24 | | 32 | | 44 | | 56 | 12 | 16 | 24 |
| A | 254 ± 2 | 254 ± 2 | 330 ± 2 | 254 ± 2 | 330 ± 2 | 254 ± 2 | 330 ± 2 | 330 ± 2 | | | | | | | |
| B | $100^{+2}_{-0}$ | | | | | | | $100^{+2}_{-0}$ | $150^{+2}_{-0}$ | $100^{+2}_{-0}$ | $150^{+2}_{-0}$ | $100^{+2}_{-0}$ | 100 ± 2 | | |
| C | 13 ± 0.2 | | | | | | | | | | | | $13^{+0.5}_{-0.2}$ | | |
| D | 21 ± 0.8 | | | | | | | | | | | | $20.5^{+1}_{-0.2}$ | | |
| E | 2 ± 0.5 | | | | | | | | | | | | | | |
| W1 | $8.4^{+2}_{-0}$ | $12.4^{+2}_{-0}$ | | $16.4^{+2}_{-0}$ | | $24.4^{+2}_{-0}$ | | $32.4^{+2}_{-0}$ | | $44.4^{+2}_{-0}$ | | $56.4^{+2}_{-0}$ | $12.4^{+1}_{-0}$ | $16.4^{+1}_{-0}$ | $24.4^{+0.1}_{-0}$ |
| W2 | less than 14.4 | less than 18.4 | | less than 22.4 | | less than 30.4 | | less than 38.4 | | less than 50.4 | | less than 62.4 | less than 18.4 | less than 22.4 | less than 30.4 |
| W3 | 7.9 ~ 10.9 | 11.9 ~ 15.4 | | 15.9 ~ 19.4 | | 23.9 ~ 27.4 | | 31.9 ~ 35.4 | | 43.9 ~ 47.4 | | 55.9 ~ 59.4 | 12.4 ~ 14.4 | 16.4 ~ 18.4 | 24.4 ~ 26.4 |
| r | 1.0 | | | | | | | | | | | | | | |


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### 2.4 Taping (ϕ330mm Reel) Dry Pack Packing Specifications

| | |
|---|---|
| Embossed tapes |  |
| Dry pack | |
| Inner box | |
| Outer box | |



*1: For a product of witch part number is suffixed with “E1”, a “ G Pb ” marks is display to the moisture barrier bag and the inner boxes.

*2: The size of the outer box may be changed depending on the quantity of inner boxes.

*3: The space in the outer box will be filled with empty inner boxes, or cushions, etc.

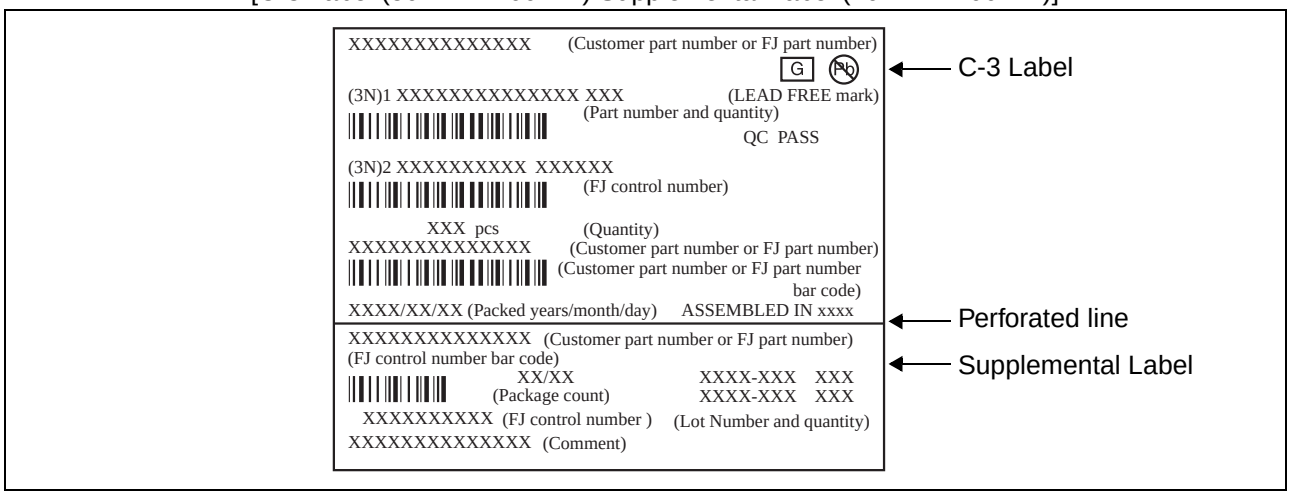
*4: Please refer to an attached sheet about the indication label.

Note: The packing specifications may not be applied when the product is delivered via a distributor.

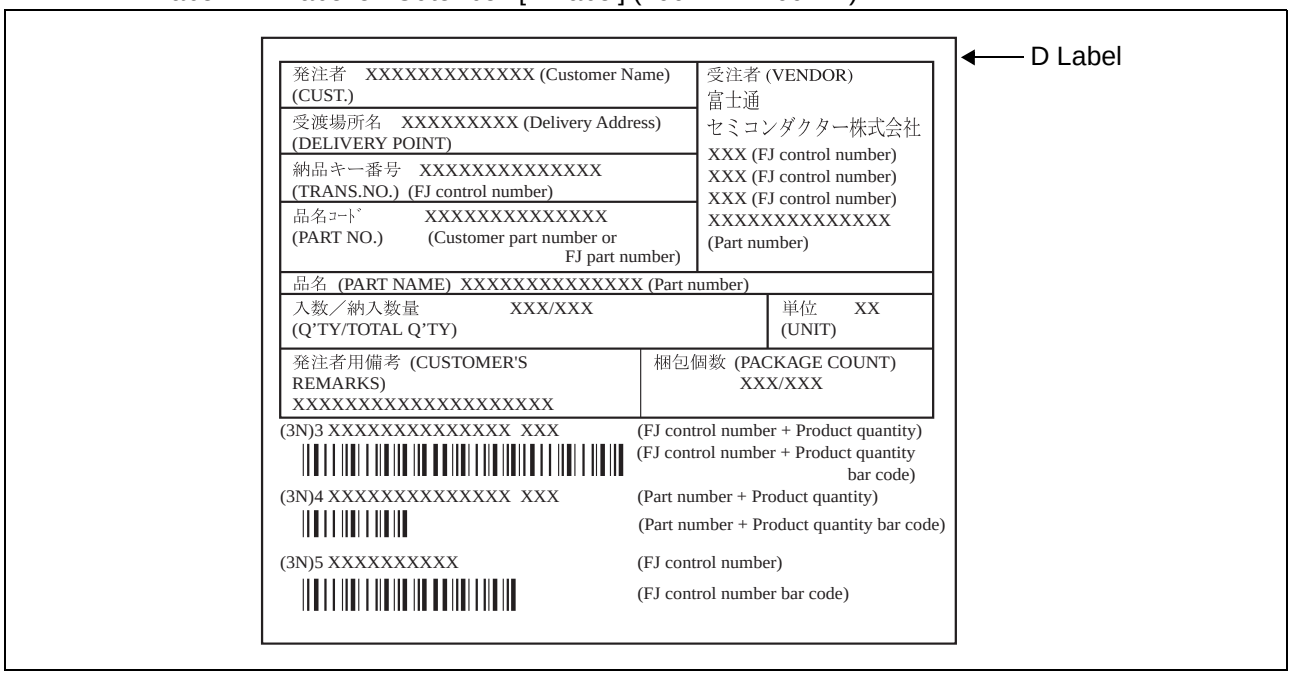

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## 2.5 Product label indicators

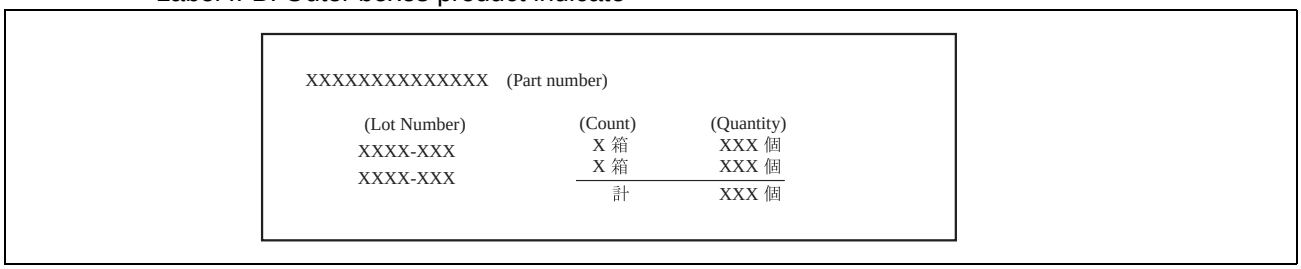
Label I: Label on Inner box/Moisture Barrier Bag/ (It sticks it on the reel for the emboss taping)
[C-3 Label (50mm × 100mm) Supplemental Label (20mm × 100mm)]




Label II-A: Label on Outer box [D Label] (100mm × 100mm)




Label II-B: Outer boxes product indicate

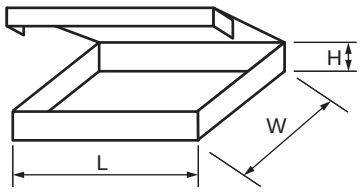



Note: Depending on shipment state, “Label II-A” and “Label II-B” on the external boxes might not be printed.


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### 2.6 Dimensions for Containers

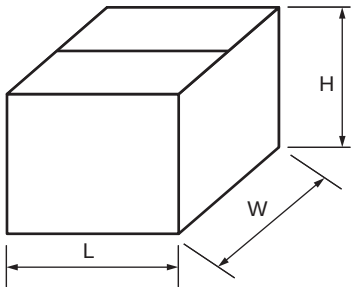
**(1) Dimensions for inner box**




| Tape width | L | W | H |
|---|---|---|---|
| 12, 16 | 365 | 345 | 40 |
| 24, 32 | | | 50 |
| 44 | | | 65 |
| 56 | | | 75 |

(Dimensions in mm)

**(2) Dimensions for outer box**




| L | W | H |
|---|---|---|
| 415 | 400 | 315 |

(Dimensions in mm)


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## ■ MAJOR CHANGES IN THIS EDITION

A change on a page is indicated by a vertical line drawn on the left side of that page.

| Page | Section | Change Results |
|---|---|---|
| 11 | ■ RECOMMENDED OPERATING CONDITIONS | Added note on the Operation Ambient Temperature.<br>Moved the “High Level Input Voltage” and “Low Level Input Voltage” to DC Characteristics. |
| 12 | 1. DC Characteristics | Added Operating power supply current (typ) of lower frequency. |
| | | Moved the “High Level Input Voltage” and “Low Level Input Voltage” from RECOMMENDED OPERATING CONDITIONS. |
| 18 | ■ CURRENT STATUS ON CONTAINED RESTRICTED SUBSTANCES | Deleted the URL info. |
| 20 | ■ PACKAGE DIMENSION | Deleted the URL info. |


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Edited: System Memory Business Division

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