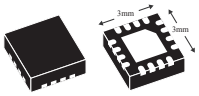
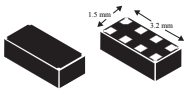
M41T62, M41T64, M41T65

Datasheet

Low-power serial real-time clocks (RTCs) with alarm



QFN16 3 x 3 mm



Embedded crystal LCC8 1.5 x 3.2 mm

No external crystal required

Maturity status link
M41T62
M41T64
M41T65

Features

- Serial real-time clock (RTC) with alarm functions
  - 400 kHz I²C serial interface
  - Memory mapped registers for seconds, minutes, hours, day, date, month, year, and century
  - Tenths/hundredths of second register
- 350 nA timekeeping current at 3 V
- Time keeping down to 1.0 V
- 1.3 V to 4.4 V I²C bus operating voltage
  - 4.4 V max. V_{CC} suitable for lithium-ion battery operation
- Low operating current of 35 µA (at 400 kHz I²C speed)
- 32 kHz square wave output is on at power-up. Suitable for driving a microcontroller in low-power mode. Can be disabled. (M41T62/64)
- Programmable 1 Hz to 32 kHz square wave output (M41T62/64)
- Programmable alarm with interrupt function (M41T62/65)
- 32 kHz crystal oscillator integrates crystal load capacitors, works with high series resistance crystals
- Oscillator stop detection monitors clock operation
- Accurate programmable watchdog
  - 62.5 ms to 31 minutes timeout
- Software clock calibration. Timekeeping can be adjusted within ± 2 parts per million (± 5 seconds per month)
- Automatic leap year compensation
- – 40 to + 85 °C operation
- Two package options
  - Very small 3 x 3 mm, lead-free and halogen-free (ECOPACK2) 16-lead QFN
  - Ultra small 1.5 x 3.2 mm, lead-free and halogen-free (ECOPACK2) 8-pin ceramic leadless chip carrier with embedded 32 kHz crystal - no external oscillator components required (M41T62)

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1 Description

The M41T6x is a low-power serial real-time clock (RTC) with a built-in 32.768 kHz oscillator. Eight registers are used for the clock/calendar function and are configured in binary-coded decimal (BCD) format. Further eight registers provide status/control of alarm, 32 kHz output, calibration, and watchdog functions. Addresses and data are transferred serially via a two-line, bidirectional I²C interface. The built-in address register is incremented automatically after each WRITE or READ data byte.

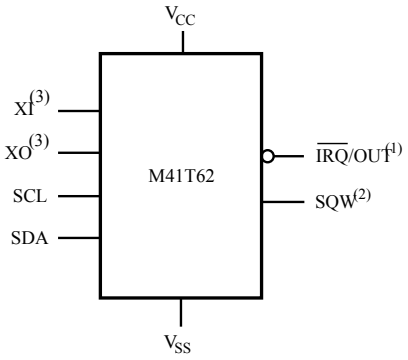
Functions available to the user include a time-of-day clock/calendar, an alarm interrupt (M41T62/M41T65), a 32 kHz output (M41T62/M41T64), a programmable square wave output (M41T62/M41T64), and a watchdog output (M41T65). The eight clock address locations contain the century, year, month, date, day, hour, minute, second and tenths/hundredths of a second in 24-hour BCD format. Corrections for 28-, 29- (leap year), 30- and 31-day months are made automatically.

The M41T6x is supplied in two very small packages: a tiny, 3 x 3 mm 16-pin QFN which requires a user-supplied 32 kHz crystal, and an ultra-small 1.5 x 3.2 mm LCC with embedded crystal - no external crystal is required.

Table 1. Device summary

Device	Basic RTC	Alarms	OSC fail detect	Watchdog timer	Calibration	SQW output	$\overline{\text{IRQ}}$ output	$\overline{\text{WDO}}$ output	F_{32K} output
M41T62	✓	✓	✓	✓	✓	✓	✓		
M41T64	✓	✓	✓	✓	✓	✓			✓
M41T65	✓	✓	✓	✓	✓		✓	✓	

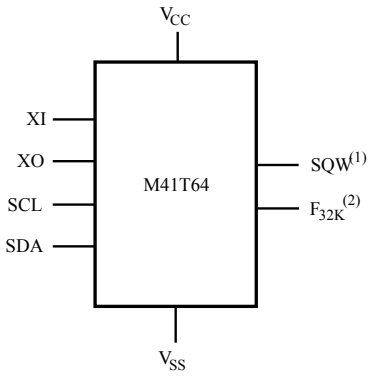
Figure 1. M41T62 logic diagram



1. Open drain.
2. Defaults to 32 kHz on power-up.
3. Not bonded on LCC package.

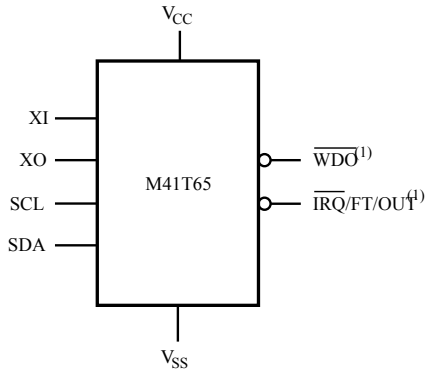
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Figure 2. M41T64 logic diagram



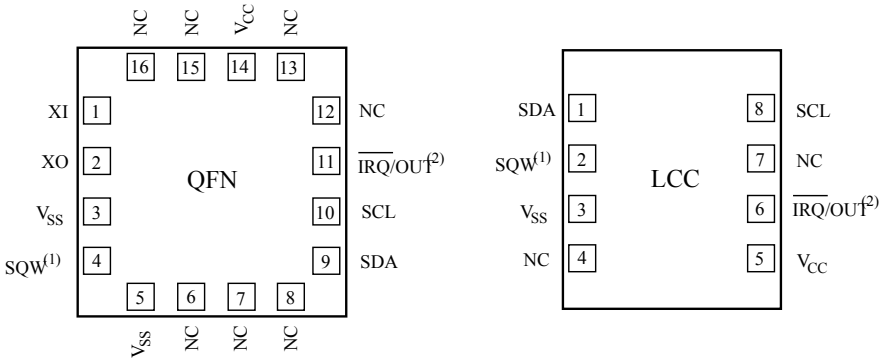
1. Open drain.
2. Defaults to 32 kHz on power-up.

Figure 3. M41T65 logic diagram



1. Open drain.

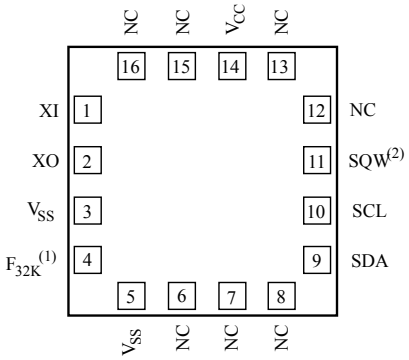
Figure 4. M41T62 connections



1. SQW output defaults to 32 kHz upon power-up.
2. Open drain.

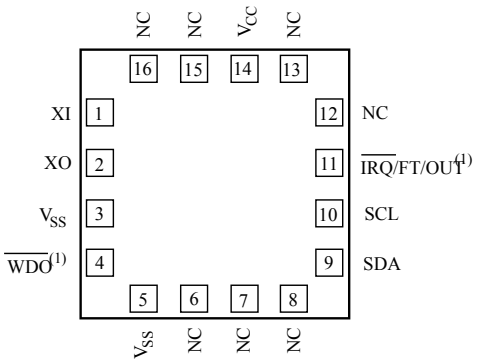
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Figure 5. M41T64 connections



1. Enabled on power-up.
2. Open drain.

Figure 6. M41T65 connections



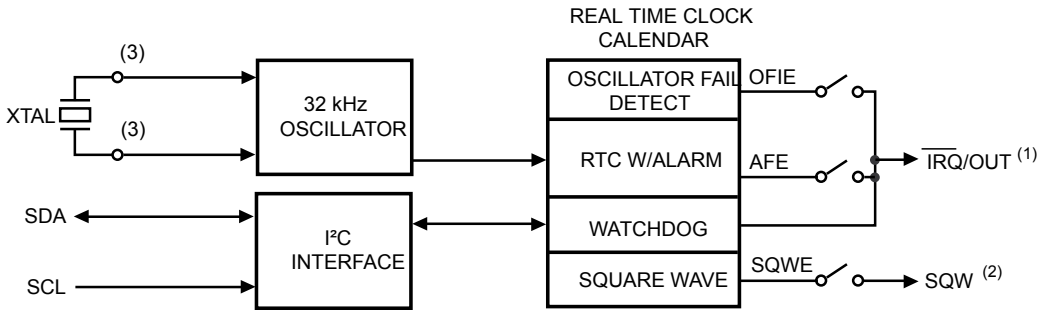
1. Open drain.

Table 2. Signal names

XI	Oscillator input
XO	Oscillator output
SDA	Serial data input/output
SCL	Serial clock input
$\overline{IRQ}$/OUT	Interrupt or OUT output (open drain)
$\overline{IRQ}$/FT/OUT	Interrupt, frequency test, or OUT output (open drain)
SQW	Programmable square wave - defaults to 32 kHz on power-up (open drain for M41T64 only)
F_{32K}	Dedicated 32 kHz output (M41T64 only)
$\overline{WDO}$	Watchdog timer output (open drain)
V_{CC}	Supply voltage
V_{SS}	Ground

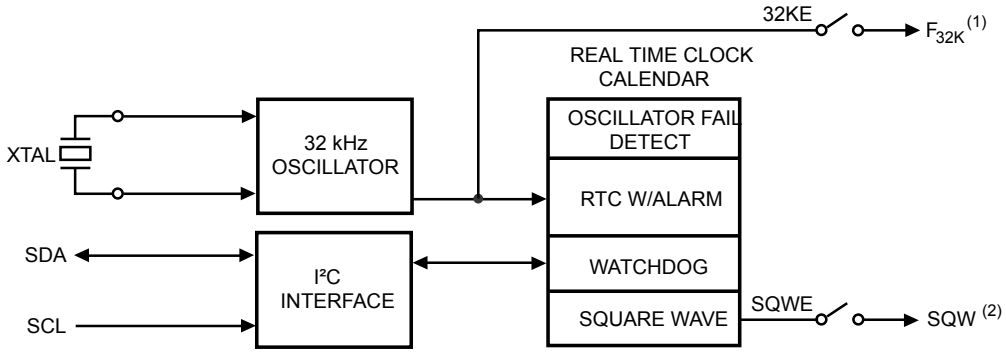
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Figure 7. **M41T62 block diagram**



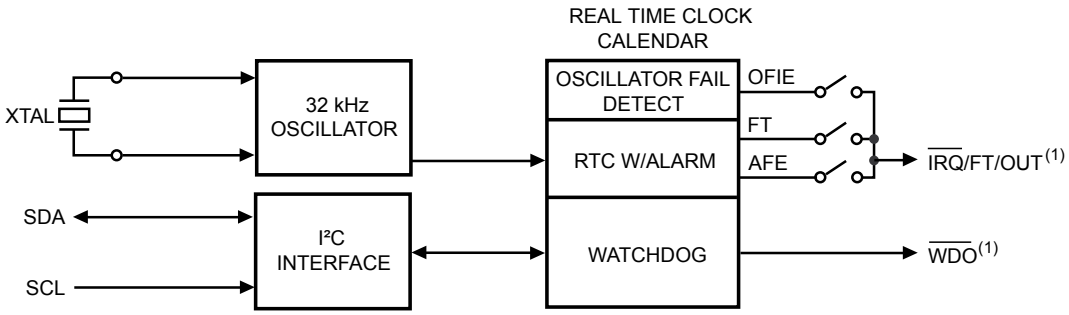
1. Open drain.
2. Defaults to 32 kHz on power-up.
3. Not bonded on embedded crystal (LCC) package.

Figure 8. **M41T64 block diagram**



1. Defaults enabled on power-up.
2. Open drain.

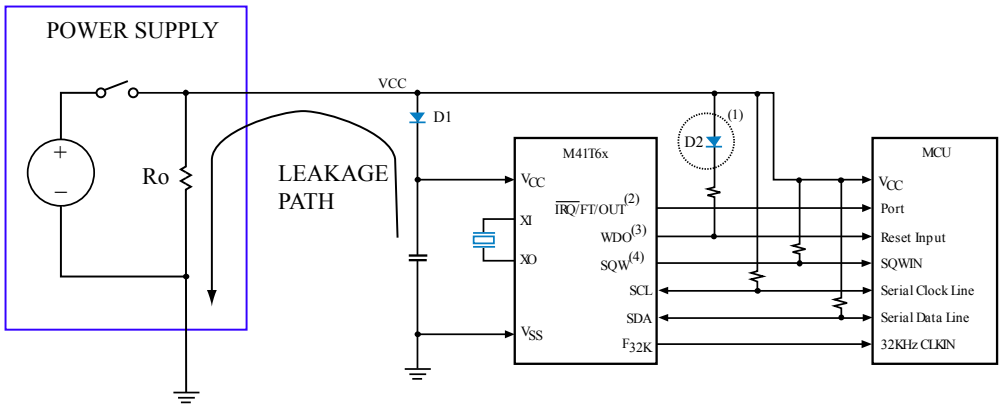
Figure 9. **M41T65 block diagram**



1. Open drain.

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Figure 10. Hardware hookup for SuperCap™ backup operation



1. Diode D2 is required on open drain pin (M41T65 only) when SuperCap (or battery) backup is being used. Low threshold BAT42 Schottky diode is recommended (see note below). D1 and D2 should be of the same type.
2. For M41T62 and M41T65 (open drain).
3. For M41T65 (open drain).
4. For M41T64 (open drain).

Note: Some power supplies, when shut off, can present a leakage path to ground, which shortens the backup time provided by the SuperCap (or battery). In such cases, a very low leakage diode is recommended for D1 (and D2).

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2 Operation

The M41T6x clock operates as a slave device on the serial bus. Access is obtained by implementing a start condition followed by the correct slave address (D0h). The 16 bytes contained in the device can then be accessed sequentially in the following order:

- 1st byte: tenths/hundredths of a second register
- 2nd byte: seconds register
- 3rd byte: minutes register
- 4th byte: hours register
- 5th byte: square wave/day register
- 6th byte: date register
- 7th byte: century/month register
- 8th byte: year register
- 9th byte: calibration register
- 10th byte: watchdog register
- 11th - 15th bytes: alarm registers
- 16th byte: flags register

2.1 2-wire bus characteristics

The bus is intended for communication between different ICs. It consists of two lines: a bi-directional data signal (SDA) and a clock signal (SCL). Both the SDA and SCL lines must be connected to a positive supply voltage via a pull-up resistor.

The following protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high.
- Changes in the data line, while the clock line is high, will be interpreted as control signals.

Accordingly, the following bus conditions have been defined.

2.1.1 Bus not busy

Both data and clock lines remain high.

2.1.2 Start data transfer

A change in the state of the data line, from high to low, while the clock is high, defines the START condition.

2.1.3 Stop data transfer

A change in the state of the data line, from low to high, while the clock is high, defines the STOP condition.

2.1.4 Data valid

The state of the data line represents valid data when after a start condition, the data line is stable for the duration of the high period of the clock signal. The data on the line may be changed during the Low period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a start condition and terminated with a stop condition. The number of data bytes transferred between the start and stop conditions is not limited. The information is transmitted byte-wide and each receiver acknowledges with a ninth bit.

By definition a device that gives out a message is called “transmitter,” the receiving device that gets the message is called “receiver.” The device that controls the message is called “master.” The devices that are controlled by the master are called “slaves.”

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2.1.5 Acknowledge

Each byte of eight bits is followed by one acknowledge bit. This acknowledge bit is a low level put on the bus by the receiver whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is a stable Low during the high period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master receiver must signal an end of data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this case the transmitter must leave the data line high to enable the master to generate the STOP condition.

Figure 11. Serial bus data transfer sequence

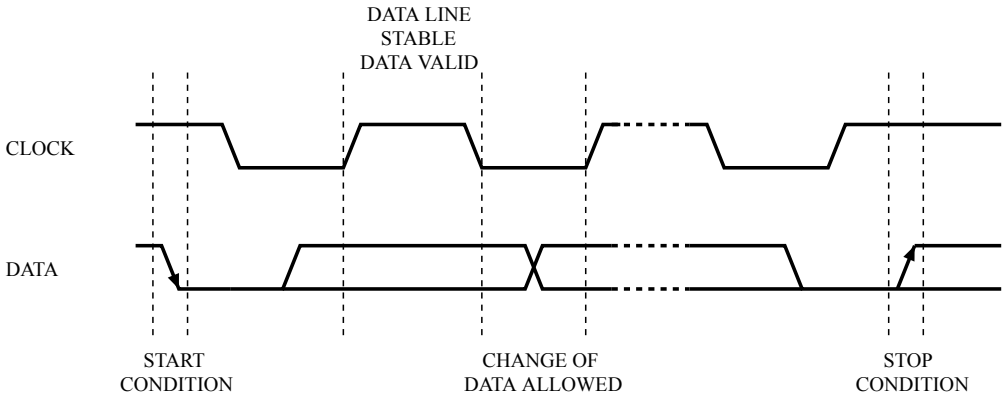
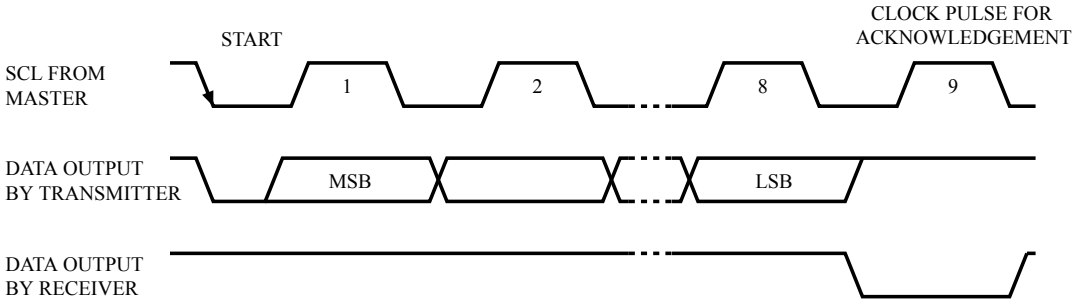


Figure 12. Acknowledgement sequence



2.2 READ mode

In this mode the master reads the M41T6x slave after setting the slave address (see Figure 14. READ mode sequence). Following the WRITE mode control bit (R/$\overline{W}$=0) and the acknowledge bit, the word address 'An' is written to the on-chip address pointer. Next the START condition and slave address are repeated followed by the READ mode control bit (R/$\overline{W}$=1). At this point the master transmitter becomes the master receiver. The data byte, which was addressed is transmitted and the master receiver sends an acknowledge bit to the slave transmitter. The address pointer is only incremented on reception of an acknowledge clock. The M41T6x slave transmitter now places the data byte at address An+1 on the bus, the master receiver reads and acknowledges the new byte and the address pointer is incremented to “An+2.”

This cycle of reading consecutive addresses continues until the master receiver sends a STOP condition to the slave transmitter.

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The system-to-user transfer of clock data will be halted whenever the address being read is a clock address (00h to 07h). The update will resume due to a stop condition or when the pointer increments to any non-clock address (08h-0Fh).

Note: This is true both in READ mode and WRITE mode.

An alternate READ mode may also be implemented whereby the master reads the M41T6x slave without first writing to the (volatile) address pointer. The first address that is read is the last one stored in the pointer (see Figure 15. Alternative READ mode sequence).

Figure 13. Slave address location

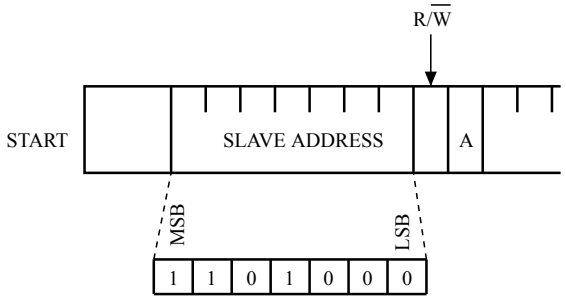


Figure 14. READ mode sequence

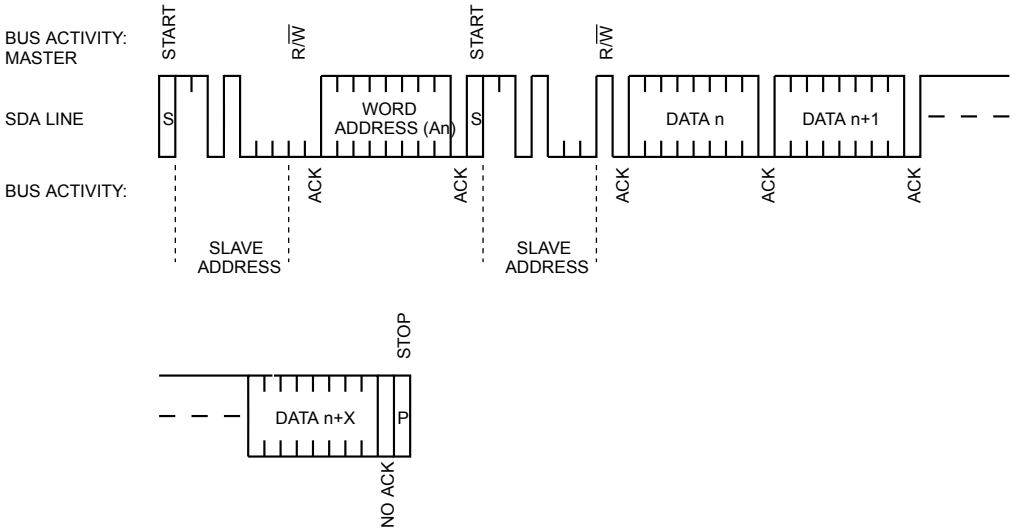
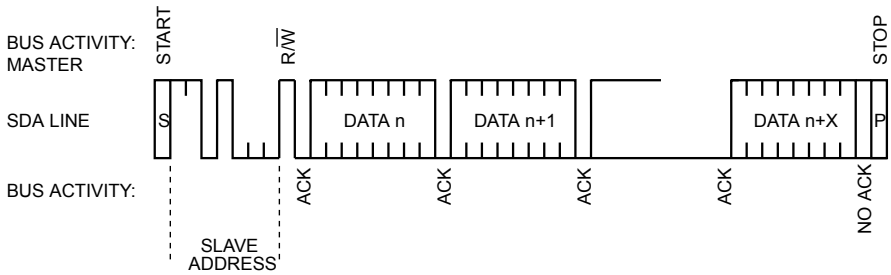


Figure 15. Alternative READ mode sequence

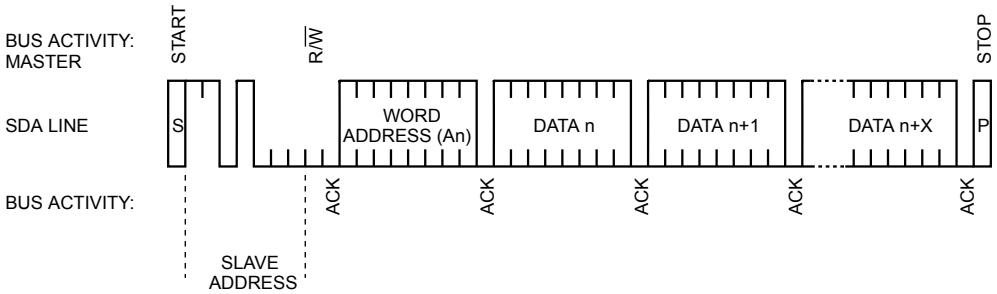


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2.3 WRITE mode

In this mode the master transmitter transmits to the M41T6x slave receiver. Bus protocol is shown in Figure 16. WRITE mode sequence. Following the START condition and slave address, a logic '0' (R/$\overline{W}$=0) is placed on the bus and indicates to the addressed device that word address “An” will follow and is to be written to the on-chip address pointer. The data word to be written to the memory is strobed in next and the internal address pointer is incremented to the next address location on the reception of an acknowledge clock. The M41T6x slave receiver will send an acknowledge clock to the master transmitter after it has received the slave address see Figure 13. Slave address location and again after it has received the word address and each data byte.

Figure 16. WRITE mode sequence



3 Clock operation

The M41T6x is driven by a quartz-controlled oscillator with a nominal frequency of 32.768 kHz. The accuracy of the real-time clock depends on the frequency of the quartz crystal that is used as the time-base for the RTC.

The eight byte clock register (see Table 3. M41T62 register map, Table 4. M41T64 register map, and Table 5. M41T65 register map) is used to both set the clock and to read the date and time from the clock, in a binary-coded decimal format. Tenths/hundredths of seconds, seconds, minutes, and hours are contained within the first four registers.

A WRITE to any clock register will result in the tenths/hundredths of seconds being reset to “00,” and tenths/hundredths of seconds cannot be written to any value other than “00.”

Bits D0 through D2 of register 04h contain the day (day of week). Registers 05h, 06h, and 07h contain the date (day of month), month, and years. The ninth clock register is the calibration register (this is described in the clock calibration section). Bit D7 of register 01h contains the STOP bit (ST). Setting this bit to a '1' will cause the oscillator to stop. When reset to a '0' the oscillator restarts within one second (typical).

Upon initial power-up, the user should set the ST bit to a '1,' then immediately reset the ST bit to '0.' This provides an additional “kick-start” to the oscillator circuit.

Bit D7 of register 02h (minute register) contains the oscillator fail interrupt enable bit (OFIE). When the user sets this bit to '1,' any condition which sets the oscillator fail bit (OF) (see Section 3.11 Oscillator stop detection) will also generate an interrupt output.

Bits D6 and D7 of clock register 06h (century/month register) contain the CENTURY bit 0 (CB0) and CENTURY bit 1 (CB1).

A WRITE to ANY location within the first eight bytes of the clock register (00h-07h), including the OFIE bit, RS0-RS3 bit, and CB0-CB1 bits will result in an update of the system clock and a reset of the divider chain. This could result in an inadvertent change of the current time. These non-clock related bits should be written prior to setting the clock, and remain unchanged until such time as a new clock time is also written.

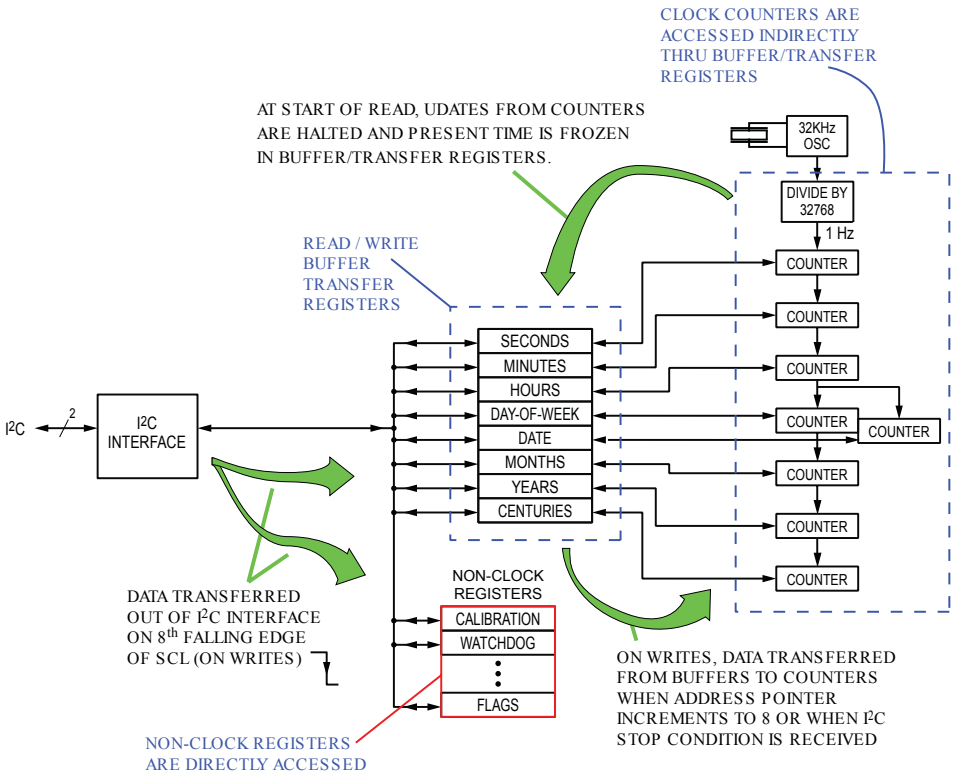
The eight clock registers may be read one byte at a time, or in a sequential block. Provision has been made to assure that a clock update does not occur while any of the eight clock addresses are being read. If a clock address is being read, an update of the clock registers will be halted. This will prevent a transition of data during the READ.

3.1 RTC registers

The M41T6x user interface is comprised of 16 memory mapped registers which include clock, calibration, alarm, watchdog, flags, and square wave control. The eight clock counters are accessed indirectly via a set of buffer/transfer registers while the other eight registers are directly accessed. Data in the clock and alarm registers is in BCD format.

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Figure 17. **Buffer/transfer registers**



Updates

During normal operation when the user is not accessing the device, the buffer/transfer registers are kept updated with a copy of the RTC counters. At the start of an I²C read or write cycle, the updating is halted and the present time is frozen in the buffer/transfer registers.

Reads of the clock registers

By halting the updates at the start of an I²C access, the user is ensured that all the data transferred out during a read sequence comes from the same instant in time.

Write timing

When writing to the device, the data is shifted into the M41T62's I²C interface on the rising edge of the SCL signal. As shown in Figure 17. Buffer/transfer registers, on the 8th clock cycle, the data is transferred from the I²C block into whichever register is being pointed to by the address pointer (not shown).

Writes to the clock registers (addresses 0-7)

Data written to the clock registers (addresses 0-7) is held in the buffer registers until the address pointer increments to 8, or an I²C stop condition occurs, at which time the data in the buffer/registers is simultaneously copied into the counters, and then the clock is re-started.

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Table 3. M41T62 register map

Addr	D7	D6	D5	D4	D3	D2	D1	D0	Function/range BCD format	
00h	0.1 seconds				0.01 seconds				10ths/100ths of seconds	00-99
01h	ST	10 seconds			Seconds				Seconds	00-59
02h	OFIE	10 minutes			Minutes				Minutes	00-59
03h	0	0	10 hours		Hours (24-hour format)				Hours	00-23
04h	RS3	RS2	RS1	RS0	0	Day of week			Day	01-7
05h	0	0	10 date		Date: day of month				Date	01-31
06h	CB1	CB0	0	10M	Month				Century/ month	0-3/01-12
07h	10 years				Year				Year	00-99
08h	OUT	0	S	Calibration					Calibration	
09h	RB2	BMB4	BMB3	BMB2	BMB1	BMB0	RB1	RB0	Watchdog	
0Ah	AFE	SQWE	0	AI 10M	Alarm month				AI month	01-12
0Bh	RPT4	RPT5	AI 10 date		Alarm date				AI date	01-31
0Ch	RPT3	0	AI 10 hour		Alarm hour				AI hour	00-23
0Dh	RPT2	Alarm 10 minutes			Alarm minutes				AI min	00-59
0Eh	RPT1	Alarm 10 seconds			Alarm seconds				AI sec	00-59
0Fh	WDF	AF	0	0	0	OF	0	0	Flags	

Keys:
0 = must be set to '0'
AF = alarm flag (read only)
AFE = alarm flag enable flag
BMB0 - BMB4 = watchdog multiplier bits
CB0-CB1 = century bits
OF = oscillator fail bit
OFIE = oscillator fail interrupt enable bit
OUT = output level
RB0 - RB2 = watchdog resolution bits
RPT1-RPT5 = alarm repeat mode bits
RS0-RS3 = SQW frequency bits
S = sign bit
SQWE = square wave enable bit
ST = stop bit
WDF = watchdog flag bit (read only)

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Table 4. M41T64 register map

Addr	D7	D6	D5	D4	D3	D2	D1	D0	Function/range BCD format	
00h	0.1 seconds				0.01 seconds				10ths/100ths of seconds	00-99
01h	ST	10 seconds			Seconds				Seconds	00-59
02h	0	10 minutes			Minutes				Minutes	00-59
03h	0	0	10 hours		Hours (24-hour format)				Hours	00-23
04h	RS3	RS2	RS1	RS0	0	Day of week			Day	01-7
05h	0	0	10 Date		Date: day of month				Date	01-31
06h	CB1	CB0	0	10M	Month				Century/ month	0-3/01-12
07h	10 years				Year				Year	00-99
08h	0	0	S	Calibration					Calibration	
09h	RB2	BMB4	BMB3	BMB2	BMB1	BMB0	RB1	RB0	Watchdog	
0Ah	0	SQWE	32KE	AI 10M	Alarm month				AI month	01-12
0Bh	RPT4	RPT5	AI 10 date		Alarm date				AI date	01-31
0Ch	RPT3	0	AI 10 hour		Alarm hour				AI hour	00-23
0Dh	RPT2	Alarm 10 minutes			Alarm minutes				AI min	00-59
0Eh	RPT1	Alarm 10 seconds			Alarm seconds				AI sec	00-59
0Fh	WDF	AF	0	0	0	OF	0	0	Flags	

Keys:
0 = must be set to '0'
32KE = 32 kHz enable bit
AF = alarm flag (read only)
BMB0 - BMB4 = watchdog multiplier bits
CB0-CB1 = century bits
OF = oscillator fail bit
RB0 - RB2 = watchdog resolution bits
RPT1-RPT5 = alarm repeat mode bits
RS0-RS3 = SQW frequency bits
S = sign bit
SQWE = square wave enable bit
ST = stop bit
WDF = watchdog flag bit (read only)

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Table 5. M41T65 register map

Addr	D7	D6	D5	D4	D3	D2	D1	D0	Function/range BCD format	
00h	0.1 seconds				0.01 seconds				10ths/100ths of seconds	00-99
01h	ST	10 seconds			Seconds				Seconds	00-59
02h	OFIE	10 minutes			Minutes				Minutes	00-59
03h	0	0	10 hours		Hours (24-hour format)				Hours	00-23
04h	0	0	0	0	0	Day of week			Day	01-7
05h	0	0	10 date		Date: day of month				Date	01-31
06h	CB1	CB0	0	10M	Month				Century/ month	0-3/01-12
07h	10 years				Year				Year	00-99
08h	OUT	FT	S	Calibration					Calibration	
09h	RB2	BMB4	BMB3	BMB2	BMB1	BMB0	RB1	RB0	Watchdog	
0Ah	AFE	0	0	AI 10M	Alarm month				AI month	01-12
0Bh	RPT4	RPT5	AI 10 date		Alarm date				AI date	01-31
0Ch	RPT3	0	AI 10 hour		Alarm hour				AI hour	00-23
0Dh	RPT2	Alarm 10 minutes			Alarm minutes				AI min	00-59
0Eh	RPT1	Alarm 10 seconds			Alarm seconds				AI sec	00-59
0Fh	WDF	AF	0	0	0	OF	0	0	Flags	

Keys:
0 = must be set to '0'
AF = alarm flag (read only)
AFE = alarm flag enable flag
BMB0 - BMB4 = watchdog multiplier bits
CB0-CB1 = century bits
FT = frequency test bit
OF = oscillator fail bit
OFIE = oscillator fail interrupt enable bit
OUT = output level
RB0 - RB2 = watchdog resolution bits
RPT1-RPT5 = alarm repeat mode bits
S = sign bit
ST = stop bit
WDF = watchdog flag bit (read only)

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3.2 Calibrating the clock

The M41T6x real-time clock is driven by a quartz controlled oscillator with a nominal frequency of 32.768 kHz. This provides the time-base for the RTC. The accuracy of the clock depends on the frequency accuracy of the crystal, and the match between the capacitive load of the oscillator circuit and the capacitive load for which the crystal was trimmed. The M41T6x oscillator is designed for use with a 6 - 7 pF crystal load capacitance. When the calibration circuit is properly employed, accuracy improves to better than ± 2 ppm at 25 °C.

The oscillation rate of crystals changes with temperature (see Figure 18. Crystal accuracy across temperature). Therefore, the M41T6x design employs periodic counter correction. The calibration circuit adds or subtracts counts from the oscillator divider circuit at the divide by 256 stage, as shown in Figure 19. Calibration waveform. The number of times pulses which are blanked (subtracted, negative calibration) or split (added, positive calibration) depends upon the value loaded into the five calibration bits found in the calibration register. Adding counts speeds the clock up, subtracting counts slows the clock down.

The calibration bits occupy the five lower order bits (D4-D0) in the calibration register (08h). These bits can be set to represent any value between 0 and 31 in binary form. Bit D5 is a sign bit; '1' indicates positive calibration, '0' indicates negative calibration. Calibration occurs within a 64 minute cycle. The first 62 minutes in the cycle may, once per minute, have one second either shortened by 128 or lengthened by 256 oscillator cycles. If a binary '1' is loaded into the register, only the first 2 minutes in the 64 minute cycle will be modified; if a binary 6 is loaded, the first 12 will be affected, and so on.

Therefore, each calibration step has the effect of adding 512 or subtracting 256 oscillator cycles for every 125,829,120 actual oscillator cycles, that is +4.068 or –2.034 ppm of adjustment per calibration step in the calibration register.

Assuming that the oscillator is running at exactly 32.768 kHz, each of the 31 increments in the calibration byte would represent +10.7 or –5.35 seconds per day which corresponds to a total range of +5.5 or –2.75 minutes per month (see Figure 19. Calibration waveform).

Two methods are available for ascertaining how much calibration a given M41T6x may require:

- The first involves setting the clock, letting it run for a month and comparing it to a known accurate reference and recording deviation over a fixed period of time. Calibration values, including the number of seconds lost or gained in a given period, can be found in application note AN934. This allows the designer to give the end user the ability to calibrate the clock as the environment requires, even if the final product is packaged in a non-user serviceable enclosure. The designer could provide a simple utility that accesses the calibration byte.
- The second approach is better suited to a manufacturing environment, and involves the use of either the SQW pin (M41T62/64) or the $\overline{\text{IRQ}}$/FT/OUT pin (M41T65). The SQW pin will toggle at 512 Hz when RS3 = '0,' RS2 = '1,' RS1 = '1,' RS0 = '0,' SQWE = '1,' and ST = '0.' Alternatively, for the M41T65, the $\overline{\text{IRQ}}$/FT/OUT pin will toggle at 512 Hz when FT and OUT bits = '1' and ST = '0.'

Any deviation from 512 Hz indicates the degree and direction of oscillator frequency shift at the test temperature. For example, a reading of 512.010124 Hz would indicate a +20 ppm oscillator frequency error, requiring a –10 (XX001010) to be loaded into the calibration byte for correction. Note that setting or changing the calibration byte does not affect the frequency test or square wave output frequency.

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Figure 18. **Crystal accuracy across temperature**

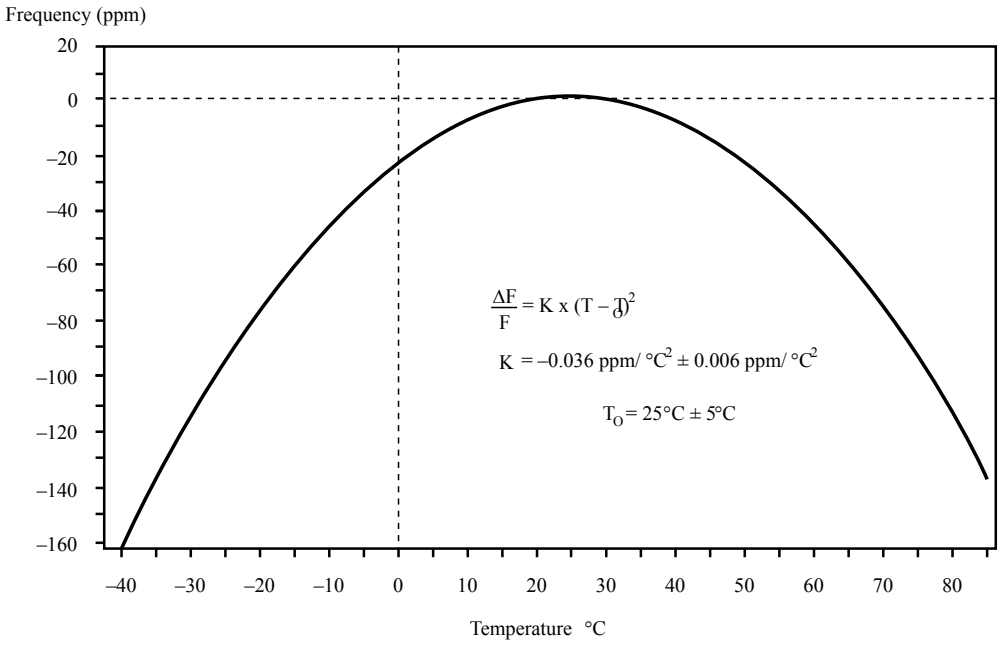
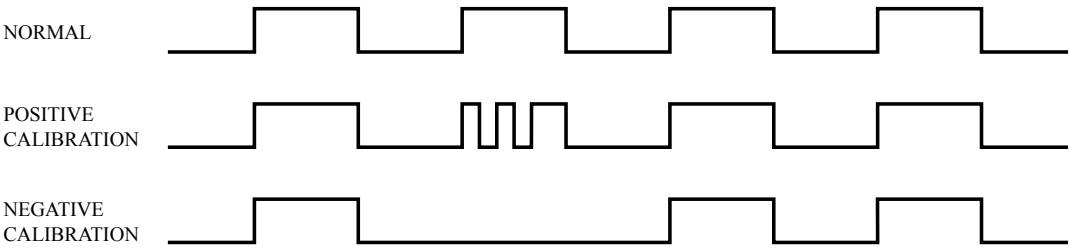


Figure 19. **Calibration waveform**



3.3 Setting alarm clock registers

Address locations 0Ah-0Eh contain the alarm settings. The alarm can be configured to go off at a prescribed time on a specific month, date, hour, minute, or second, or repeat every year, month, day, hour, minute, or second. Bits RPT5–RPT1 put the alarm in the repeat mode of operation. Table 6. Alarm repeat modes shows the possible configurations. Codes not listed in the table default to the once per second mode to quickly alert the user of an incorrect alarm setting.

When the clock information matches the alarm clock settings based on the match criteria defined by RPT5–RPT1, the AF (alarm flag) is set. If AFE (alarm flag enable) is also set (M41T62/65), the alarm condition activates the $\overline{\text{IRQ}}$ /OUT or $\overline{\text{IRQ}}$ /FT/OUT pin. To disable the alarm, write '0' to the alarm date register and to RPT5–RPT1.

Note: If the address pointer is allowed to increment to the flag register address, an alarm condition will not cause the interrupt/flag to occur until the address pointer is moved to a different address. It should also be noted that if the last address written is the "Alarm Seconds," the address pointer will increment to the flag address, causing this situation to occur.

The $\overline{\text{IRQ}}$ output is cleared by a READ to the flags register as shown in Figure 20. Alarm interrupt reset waveform. A subsequent READ of the flags register is necessary to see that the value of the alarm flag has been reset to '0.'

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Figure 20. **Alarm interrupt reset waveform**

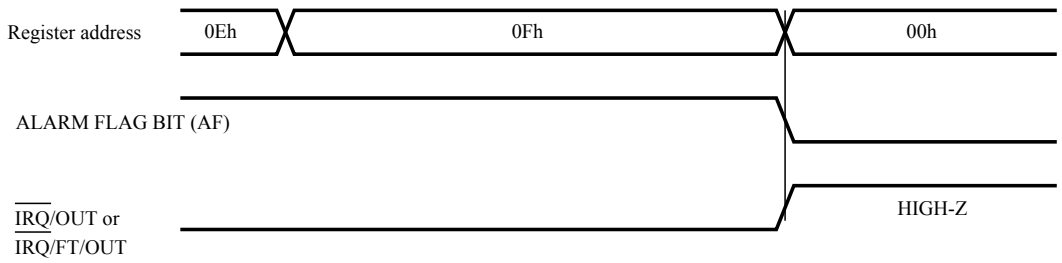


Table 6. **Alarm repeat modes**

RPT5	RPT4	RPT3	RPT2	RPT1	Alarm setting
1	1	1	1	1	Once per second
1	1	1	1	0	Once per minute
1	1	1	0	0	Once per hour
1	1	0	0	0	Once per day
1	0	0	0	0	Once per month
0	0	0	0	0	Once per year

3.4 Watchdog timer

The watchdog timer can be used to detect an out-of-control microprocessor. The user programs the watchdog timer by setting the desired amount of time-out into the watchdog register, address 09h.

Bits BMB4-BMB0 store a binary multiplier and the three bits RB2-RB0 select the resolution where:

000=1/16 second (16 Hz);

001=1/4 second (4 Hz);

010=1 second (1 Hz);

011=4 seconds (1/4 Hz); and

100 = 1 minute (1/60 Hz).

Note: Invalid combinations (101, 110, and 111) will NOT enable a watchdog time-out. Setting BMB4-BMB0 = 00000 with any combination of RB2-RB0, other than 000, will result in an immediate watchdog time-out.

The amount of time-out is then determined to be the multiplication of the five-bit multiplier value with the resolution. (For example: writing 00001110 in the watchdog register = 3*1 or 3 seconds). If the processor does not reset the timer within the specified period, the M41T6x sets the WDF (watchdog flag) and generates an interrupt on the $\overline{IRQ}$ pin (M41T62), or a watchdog output pulse (M41T65 only) on the $\overline{WDO}$ pin. The watchdog timer can only be reset by having the microprocessor perform a WRITE of the watchdog register. The time-out period then starts over.

Should the watchdog timer time out, any value may be written to the watchdog register in order to clear the $\overline{IRQ}$ pin. A value of 00h will disable the watchdog function until it is again programmed to a new value. A READ of the flags register will reset the watchdog flag (bit D7; register 0Fh). The watchdog function is automatically disabled upon power-up, and the watchdog register is cleared.

Note: A WRITE to any clock register will restart the watchdog timer.

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3.5 Watchdog output ($\overline{WDO}$ - M41T65 only)

If the processor does not reset the watchdog timer within the specified period, the watchdog output ($\overline{WDO}$) will pulse low for t_{rec} (see Table 7. Square wave output frequency). This output may be connected to the reset input of the processor in order to generate a processor reset. After a watchdog time-out occurs, the timer will remain disabled until such time as a new countdown value is written into the watchdog register.

Note: The crystal oscillator must be running for the $\overline{WDO}$ pulse to be available. The $\overline{WDO}$ output is an N-channel, open drain output driver (with I_{OL} as specified in Table 13. DC characteristics).

3.6 Square wave output (M41T62/64)

The M41T62/64 offers the user a programmable square wave function which is output on the SQW pin. RS3-RS0 bits located in 04h establish the square wave output frequency. These frequencies are listed in Table 7. Square wave output frequency. Once the selection of the SQW frequency has been completed, the SQW pin can be turned on and off under software control with the square wave enable bit (SQWE) located in register 0Ah.

The SQW output is an N-channel, open drain output driver for the M41T64, and a full CMOS output driver for the M41T62. The initial power-up default for the SQW output is 32 kHz (except for M41T64, which defaults disabled).

Table 7. Square wave output frequency

Square wave bits				Square wave	
RS3	RS2	RS1	RS0	Frequency	Units
0	0	0	0	None	–
0	0	0	1	32.768	kHz
0	0	1	0	8.192	kHz
0	0	1	1	4.096	kHz
0	1	0	0	2.048	kHz
0	1	0	1	1.024	kHz
0	1	1	0	512	Hz
0	1	1	1	256	Hz
1	0	0	0	128	Hz
1	0	0	1	64	Hz
1	0	1	0	32	Hz
1	0	1	1	16	Hz
1	1	0	0	8	Hz
1	1	0	1	4	Hz
1	1	1	0	2	Hz
1	1	1	1	1	Hz

3.7 Full-time 32 kHz square wave output (M41T64)

The M41T64 offers the user a special 32 kHz square wave function which is enabled on power-up to output on the F_{32K} pin as long as $V_{CC} \geq 1.3$ V, and the oscillator is running (ST bit = '0'). This function is available within one second (typ) of initial power-up and can only be disabled by setting the 32KE bit to '0' or the ST bit to '1.' If not used, the F_{32K} pin should be disconnected and allowed to float.

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3.8 Century bits

The two century bits, CB1 and CB0, are bits D7 and D6, respectively, in the century/month register at address 06h. Together, they comprise a 2-bit counter which increments at the turn of each century. CB1 is the most significant bit.

The user may arbitrarily assign the meaning of CB1:CB0 to represent any century value, but the simplest way of using these bits is to extend the year register (07h) by mapping them directly to bits 9 and 8. (The reader is reminded that the year register is in BCD format.) Higher order year bits can be maintained in the application software.

Figure 21. Century bits CB1 and CB0

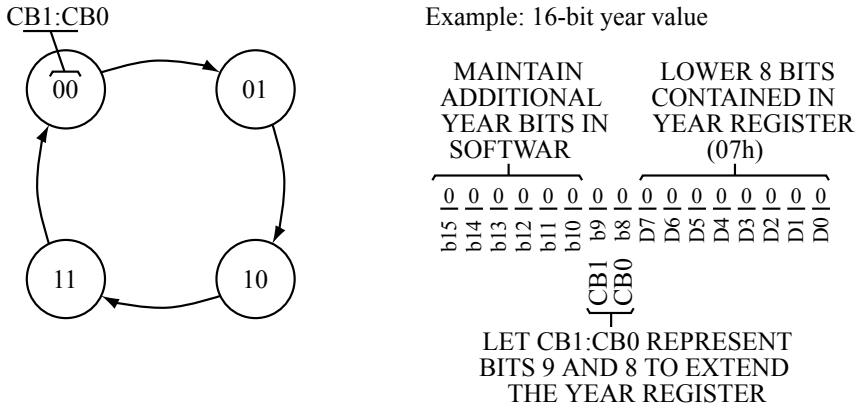


Table 8. Examples using century bits

CB1	CB0	CENTURY
0	0	2000
0	1	2100
1	0	2200
1	1	2300

3.9 Leap year

Leap year occurs every four years, in years which are multiples of 4. For example, 2012 was a leap year. An exception to that is any year which is a multiple of 100. For example, the year 2100 is not a leap year. A further exception is that years which are multiples of 400 are indeed leap years. Hence, while 2100 is not a leap year, 2400 is.

During any year which is a multiple of 4, the M41T6x RTC will automatically insert leap day, February 29. Therefore, the application software must correct for this during the exception years (2100, 2200, etc.) as noted above.

3.10 Output driver pin (M41T62/65)

When the OFIE bit, AFE bit, and watchdog register are not set to generate an interrupt, the $\overline{IRQ}$/OUT pin becomes an output driver that reflects the contents of D7 of the calibration register. In other words, when D7 (OUT bit) is a '0,' then the $\overline{IRQ}$/OUT pin will be driven low.

Note: The $\overline{IRQ}$/OUT pin is an open drain which requires an external pull-up resistor.

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3.11 Oscillator stop detection

If the oscillator fail (OF) bit is internally set to a '1,' this indicates that the oscillator has either stopped, or was stopped for some period of time and can be used to judge the validity of the clock and date data. This bit will be set to '1' any time the oscillator stops.

In the event the OF bit is found to be set to '1' at any time other than the initial power-up, the STOP bit (ST) should be written to a '1,' then immediately reset to '0.' This will restart the oscillator.

The following conditions can cause the OF bit to be set:

- The first time power is applied (defaults to a '1' on power-up).

Note: If the OF bit cannot be written to '0' four (4) seconds after the initial power-up, the STOP bit (ST) should be written to a '1,' then immediately reset to '0.'

- The voltage present on V_{CC} or battery is insufficient to support oscillation.
- The ST bit is set to '1.'
- External interference of the crystal

If the oscillator fail interrupt enable bit (OFIE) is set to a '1,' the $\overline{IRQ}$ pin will also be activated. The $\overline{IRQ}$ output is cleared by resetting the OFIE or OF bit to '0' (NOT by reading the flag register).

The OF bit will remain set to '1' until written to logic '0.' The oscillator must start and have run for at least 4 seconds before attempting to reset the OF bit to '0.' If the trigger event occurs during a power-down condition, this bit will be set correctly.

3.12 Initial power-on defaults

Upon application of power to the device, the register bits will initially power-on in the state indicated in Table 9. Initial power-up values.

Table 9. Initial power-up values

Condition	Device	ST	OF	OFIE	OUT	FT	AFE	SQWE	32KE	RS3-1	RS0	Watchdog
Initial power-up(1)	M41T62	0	1	0	1	N/A	0	1	N/A	0	1	0
	M41T64	0	1	N/A	N/A	N/A	N/A	0	1	0	1	0
	M41T65	0	1	0	1	0	0	N/A	N/A	N/A	N/A	0

1. *All other control bits power up in an undetermined state.*

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4 Maximum ratings

Stressing the device above the rating listed in the absolute maximum ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 10. Absolute maximum ratings

Sym	Parameter	Condition (1)	Value (2)	Unit
T_{STG}	Storage temperature (V_{CC} off, oscillator off)		–55 to 125	°C
V_{CC}	Supply voltage		–0.3 to 5.0	V
T_{SLD} (3)	Lead solder temperature for 10 seconds		260	°C
V_{IO}	Input or output voltages		–0.2 to Vcc+0.3	V
I_O	Output current		20	mA
P_D	Power dissipation		1	W
$V_{ESD(HBM)}$	Electro-static discharge voltage (human body model)	T_A = 25 °C	>1500	V
$V_{ESD(RCDM)}$	Electro-static discharge voltage (robotic charged device model)	T_A = 25 °C	>1000	V

1. *Test conforms to JEDEC standard.*
2. *Data based on characterization results, not tested in production.*
3. *Reflow at peak temperature of 260 °C. The time above 255 °C must not exceed 30 seconds.*

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5 DC and AC parameters

This section summarizes the operating and measurement conditions, as well as the DC and AC characteristics of the device. The parameters in the following DC and AC characteristic tables are derived from tests performed under the measurement conditions listed in the relevant tables. Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

Table 11. Operating and AC measurement conditions

Parameter	M41T6x
Supply voltage (V_{CC})	1.3 V to 4.4 V
Ambient operating temperature (T_A)	–40 to 85 °C
Load capacitance (C_L)	50 pF
Input rise and fall times	≤ 5 ns
Input pulse voltages	0.2 V_{CC} to 0.8 V_{CC}
Input and output timing ref. voltages	0.3 V_{CC} to 0.7 V_{CC}

Note: Output Hi-Z is defined as the point where data is no longer driven.

Figure 22. AC measurement I/O waveform

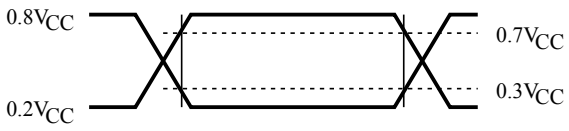
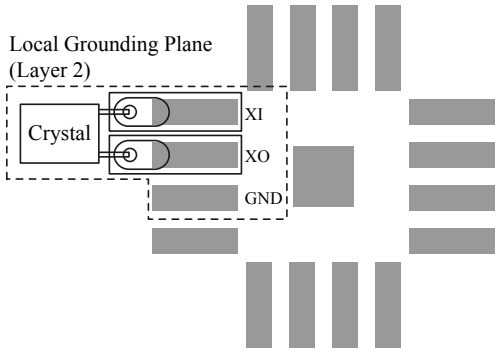


Figure 23. Crystal isolation example



Note: Substrate pad should be tied to V_{SS}.

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Table 12. Capacitance

Symbol	Parameter (1) (2)	Min.	Max.	Unit
C_{IN}	Input capacitance	-	7	pF
C_{OUT} (3)	Output capacitance	-	10	pF
t_{LP}	Low-pass filter input time constant (SDA and SCL)	-	50	ns

1. *At 25°C, f = 1 MHz.*
2. *Effective capacitance measured with power supply at 3.6 V; sampled only, not 100% tested.*
3. *Outputs deselected.*

Table 13. DC characteristics

Sym	Parameter	Test condition(1)			Min.	Typ.	Max.	Unit
V_{CC} (2)	Operating voltage	Clock			1.0		4.4	V
		I^2C bus (400 kHz)			1.3		4.4	V
I_{CC1}	Supply current	SCL = 400 kHz (no load)		4.4 V			100	µA
				3.6 V		50	70	µA
				3.0 V		35		µA
				2.5 V		30		µA
				2.0 V		20		µA
I_{CC2}	Supply current (standby)	SCL = 0 Hz all inputs ≥ V_{CC} – 0.2 V ≤ V_{SS} + 0.2 V	SQW off	4.4 V			950	nA
				3.6 V		375	700	nA
				3.0 V at 25 °C		350		nA
				2.0 V at 25 °C		310		nA
V_{IL}	Input low voltage				–0.2		0.3 V_{CC}	V
V_{IH}	Input high voltage				0.7 V_{CC}		V_{CC}+0.3	V
V_{OL}	Output low voltage	V_{CC} = 4.4 V, I_{OL} = 3.0 mA (SDA)					0.4	V
		V_{CC} = 4.4 V, I_{OL} = 1.0 mA (SQW, $\overline{WDO}$, $\overline{IRQ}$)					0.4	V
V_{OH}	Output high voltage	V_{CC} = 4.4 V, I_{OH} = –1.0 mA (CMOS)			2.4			V
	Open drain pull-up supply voltage	M41T62: $\overline{IRQ}$/OUT M41T64: SQW (3) M41T65: $\overline{WDO}$ and $\overline{IRQ}$/FT/OUT					4.4	V
I_{LI}	Input leakage current	0 V ≤ V_{IN} ≤ V_{CC}					±1	µA
I_{LO}	Output leakage current	0 V ≤ V_{OUT} ≤ V_{CC}					±1	µA

1. *Valid for ambient operating temperature: T_A = –40 to 85 °C; V_{CC} = 1.3 V to 4.4 V (except where noted).*
2. *Oscillator startup guaranteed at 1.5 V only.*
3. *While the M41T64's SQW output is open drain, the reader is reminded that the SQW output on the M41T62 is CMOS and hence is not included in this list.*

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Table 14. Crystal electrical characteristics

Sym	Parameter [1] [2]	Min.	Typ.	Max.	Units
f_O	Resonant frequency	-	32.768		kHz
R_S	Series resistance (T_A = –40 to 70 °C, oscillator startup at 2.0 V)	-		75 [3] [4]	kΩ
C_L	Load capacitance	-	6		pF

1. *Load capacitors are integrated within the M41T6x. Circuit board layout considerations for the 32.768 kHz crystal of minimum trace lengths and isolation from RF generating signals should be taken into account.*
2. *For the QFN16 package, user-supplied external crystals are required. The 6 and 7 pF crystals listed in Table 15. Crystals suitable for use with M41T6x series RTCs have been evaluated by ST and have been found to be satisfactory for use with the M41T6x series RTC.*
3. *$R_{S\ (max)}$ = 65 kΩ for T_A = –40 to 85 °C and oscillator startup at 1.5 V.*
4. *Guaranteed by design.*

Table 15. Crystals suitable for use with M41T6x series RTCs

Vendor	Order number	Package	Manufacturer's specifications			
			ESR max.	Temp. range (°C)	Rated tolerance at 25 °C	Rated load cap.
Citizen	CMJ206T-32.768KDZB-UB	8.3 x 2.5 mm leaded SMT	50 kΩ	–40/+85	±20 ppm	6 pF
Citizen	CM315-32.768KDZY-UB	3.2 x 1.5 x 0.9 mm SMT	70 kΩ	–40/+85	±20 ppm	7 pF
Ecliptek	E4WCDA06-32.768K [1]	2.0 x 6.0 mm thru-hole	50 kΩ	–10/+60	±20 ppm	6 pF
Ecliptek	E5WSDC 07 - 32.768K	7 x 1.5 x 1.4 mm SMT	65 kΩ	–40/+85	±20 ppm	7 pF
ECS	ECS-.327-6-17X-TR	3.8 x 8.5 x 2.5 mm SMT	50 kΩ	–40/+85	±20 ppm	6 pF
ECS	ECS-.327-7-34B-TR	3.2 x 1.5 x 0.9 mm SMT	70 kΩ	–40/+85	±20 ppm	7 pF
ECS	ECS-.327-7-38-TR	7 x 1.5 x 1.4 mm SMT	65 kΩ	–40/+85	±20 ppm	7 pF
Epson	MC-146 32.7680KA-AG: ROHS [2]	7 x 1.5 x 1.4 mm SMT	65 kΩ	–40/+85	±20 ppm	7 pF
Fox	298LF-0.032768-19	1.5 x 5.0 mm thru-hole	50 kΩ	–20/+60	±20 ppm	6 pF
Fox	299LF-0.032768-37	2.0 x 6.0 mm thru-hole	50 kΩ	–20/+60	±20 ppm	6 pF
Fox	414LF-0.032768-12	3.8 x 8.5 x 2.5 mm SMT	50 kΩ	–40/+85	±20 ppm	6 pF
Fox	501LF-0.032768-5	7 x 1.5 x 1.4 mm SMT	65 kΩ	–40/+85	±20 ppm	7 pF
Micro Crystal	MS3V-T1R 32.768KHZ 7PF 20PPM	6.7 x 1.4 mm leaded SMT	65 kΩ	–40/+85	±20 ppm	7 pF
Pletronics	SM20S - 32.768K - 6pF	3.8 x 8.5 x 2.5 mm SMT	50 kΩ	–40/+85	±20 ppm	6 pF
Seiko	SSPT7F-7PF20PPM	7 x 1.5 x 1.4 mm SMT	65 kΩ	–40/+85	±20 ppm	7 pF
Seiko	VT200F-6PF20PPM	2.0 x 6.0 mm thru-hole	50 kΩ	–10/+60	±20 ppm	6 pF

1. *ST has been informed that this crystal has been terminated by the vendor.*
2. *Epson MC-146 32.7680KA-E: ROHS is 6 pF version.*

Table 16. Oscillator characteristics

Sym	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{STA}	Oscillator start voltage	≤ 10 seconds	1.5			V
t_{STA}	Oscillator start time	V_{CC} = 3.0 V			1	s
C_g	XIN capacitance			12		pF

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Sym	Parameter	Conditions	Min.	Typ.	Max.	Unit
C_d	XOUT capacitance			12		pF
	IC-to-IC frequency variation (1) (2)		–10		+10	ppm

1. *Devices in LCC8 package ((M41T62LC6F) are tested not to exceed ±20 ppm oscillator frequency error at 25 °C, which equates to about 52 seconds per month.*
2. *Reference value. T_A = 25 °C, V_{CC} = 3.0 V, CMJ-145 (C_L = 6 pF, 32.768 Hz) manufactured by Citizen, $C_L = C_g \cdot C_d / (C_g + C_d)$.*

Figure 24. Bus timing requirements sequence

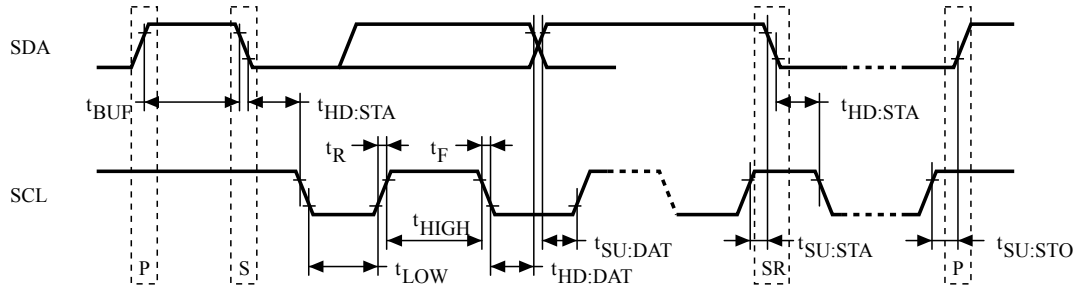


Table 17. AC characteristics

Sym	Parameter (1)	Min.	Max.	Units
f_{SCL}	SCL clock frequency	0	400	kHz
t_{LOW}	Clock low period	1.3		µs
t_{HIGH}	Clock high period	600		ns
t_R	SDA and SCL rise time		300	ns
t_F	SDA and SCL fall time		300	ns
$t_{HD:STA}$	START condition hold time (after this period the first clock pulse is generated)	600		ns
$t_{SU:STA}$	START condition setup time (only relevant for a repeated start condition)	600		ns
$t_{SU:DAT}$ (2)	Data set-up time	100		ns
$t_{HD:DAT}$	Data hold time	0		µs
$t_{SU:STO}$	STOP condition setup time	600		ns
t_{BUF}	Time the bus must be free before a new transmission can start	1.3		µs
t_{rec}	Watchdog output pulse width	96	98	ms

1. *Valid for ambient operating temperature: T_A = –40 to 85 °C; V_{CC} = 1.3 to 4.4 V (except where noted).*
2. *Transmitter must internally provide a hold time to bridge the undefined region (300 ns max.) of the falling edge of SCL.*

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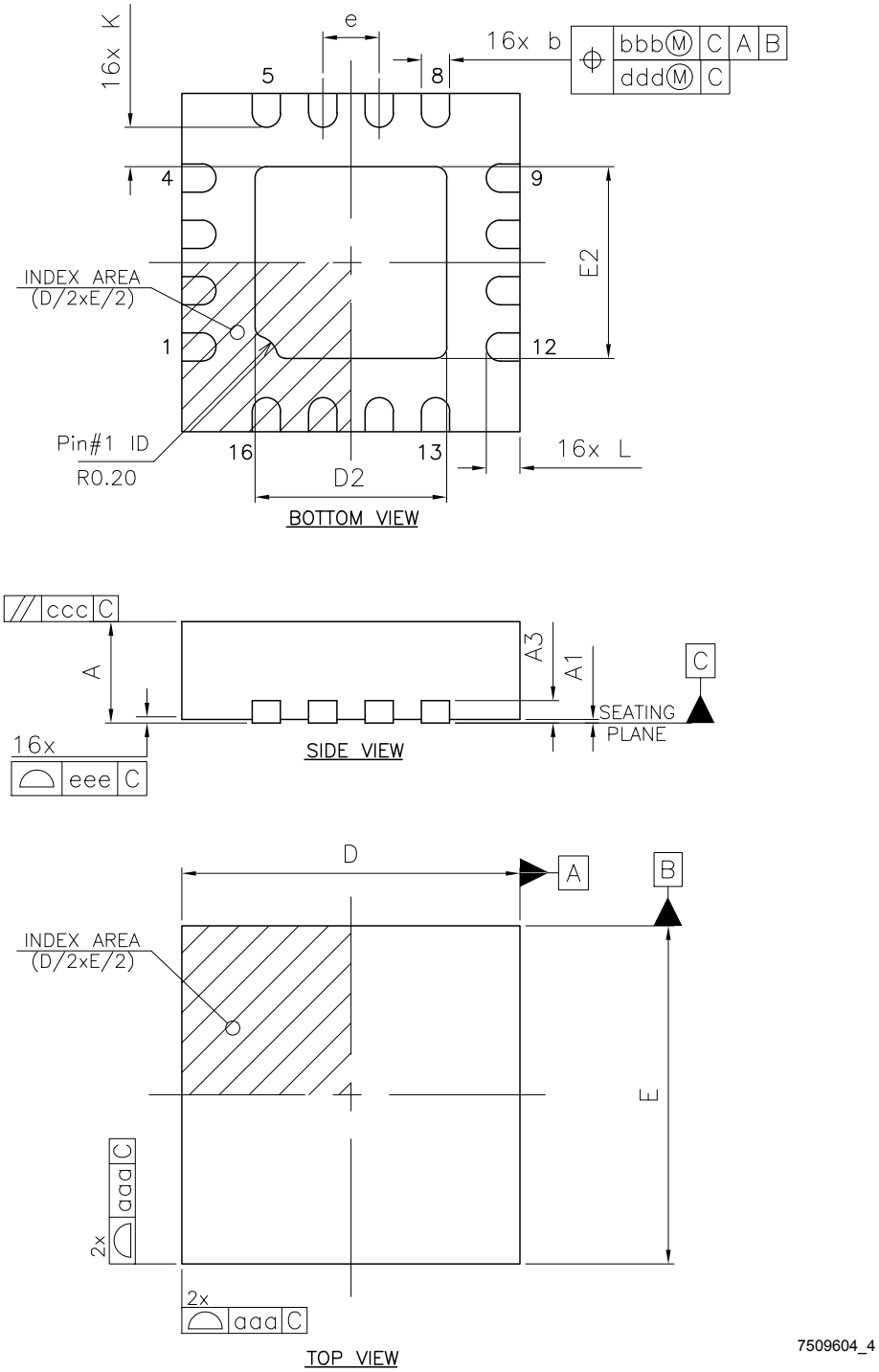
6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

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6.1 QFN16 package information

Figure 25. QFN16 — 16-pin, quad, flat package, no-lead, 3x3 mm, package outline



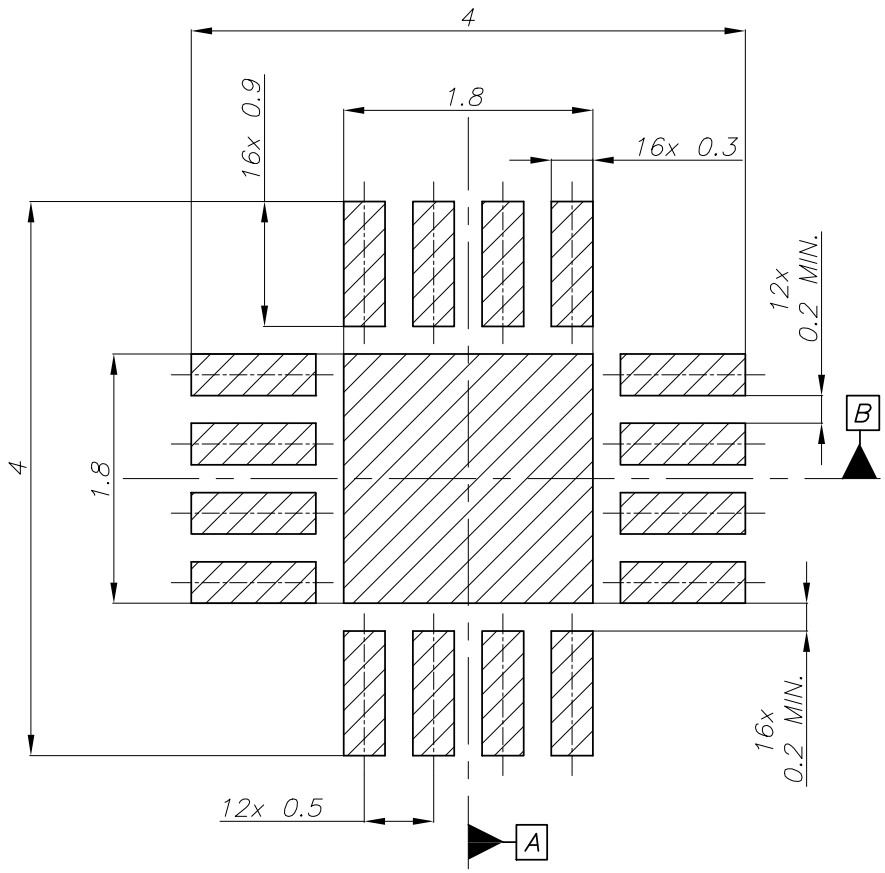
Note: Drawing is not to scale.

Table 18. **QFN16 — 16-pin, quad, flat package, no-lead, 3x3 mm, package mechanical data**

Symbol	mm			inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.80	0.90	1.00	0.032	0.035	0.039
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3		0.20			0.008	
b	0.18	0.25	0.30	0.007	0.010	0.012
D		3.00			0.118	
D2	1.55	1.70	1.80	0.061	0.067	0.071
E		3.00			0.118	
E2	1.55	1.70	1.80	0.061	0.067	0.071
e		0.50			0.020	
L	0.20	0.30	0.40	0.008	0.012	0.016
K		0.20			0.008	
aaa		0.50			0.020	
bbb		0.10			0.004	
ccc		0.10			0.004	
ddd		0.05			0.002	
eee		0.08			0.003	

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Figure 26. **QFN16 — 16-pin, quad, flat package, no-lead, 3 x 3 mm recommended footprint**



Note: Dimensions shown are in millimeters (mm).

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6.2 LCC8 package information

Figure 27. **LCC8 — 8-pin, 1.5 x 3.2 mm leadless chip carrier package outline**

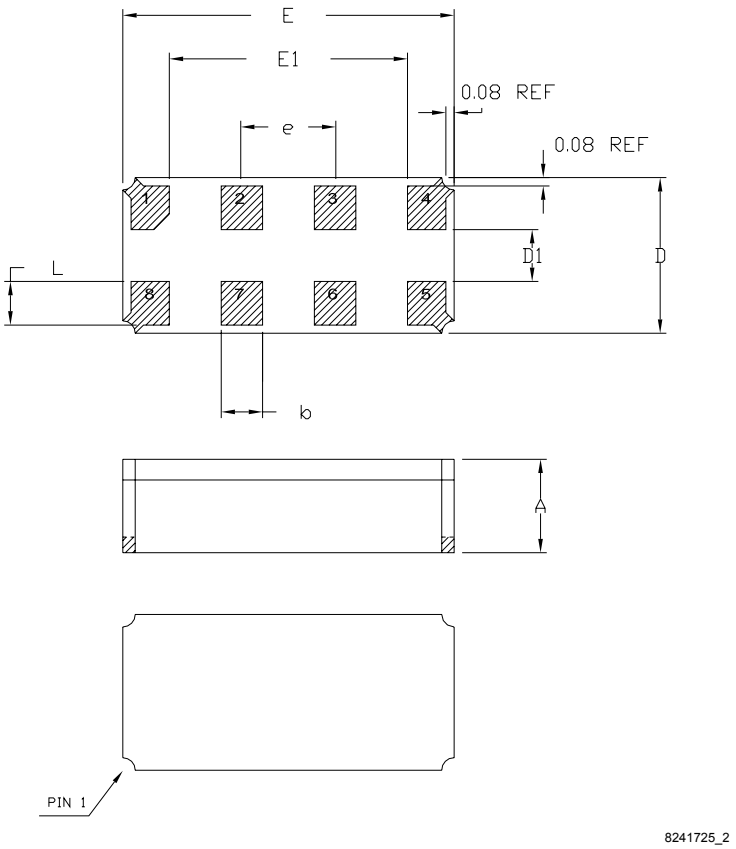
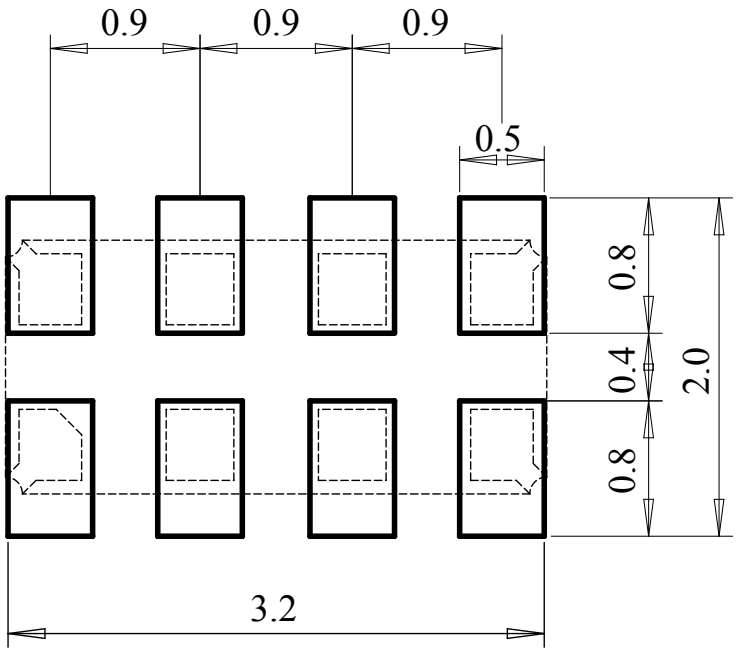


Table 19. **LCC8 — 8-pin, 1.5 x 3.2 mm leadless chip carrier package mechanical data**

Symbol	mm			inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			0.80			0.031
b	0.30	0.40	0.50	0.012	0.016	0.020
D	1.40	1.50	1.60	0.055	0.059	0.063
D1	0.40	0.50	0.60	0.016	0.020	0.024
E	3.10	3.20	3.30	0.122	0.126	0.130
E1	2.20	2.30	2.40	0.087	0.091	0.094
e	0.80	0.90	1.00	0.032	0.035	0.039
L	0.32	0.42	0.52	0.013	0.017	0.020
N	8			8		

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Figure 28. **LCC8 — 8-pin, 1.5 x 3.2 mm leadless chip carrier recommended footprint**



Note: Dimensions shown are typical values, in millimeters (mm).

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7 Packing information

7.1 QFN16 carrier tape

Figure 29. **Carrier tape for QFN16 3 x 3 mm package**

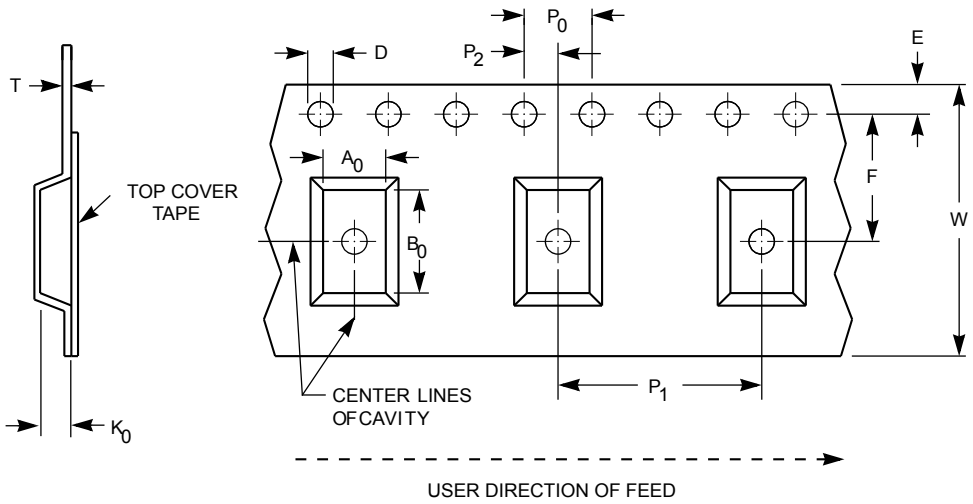


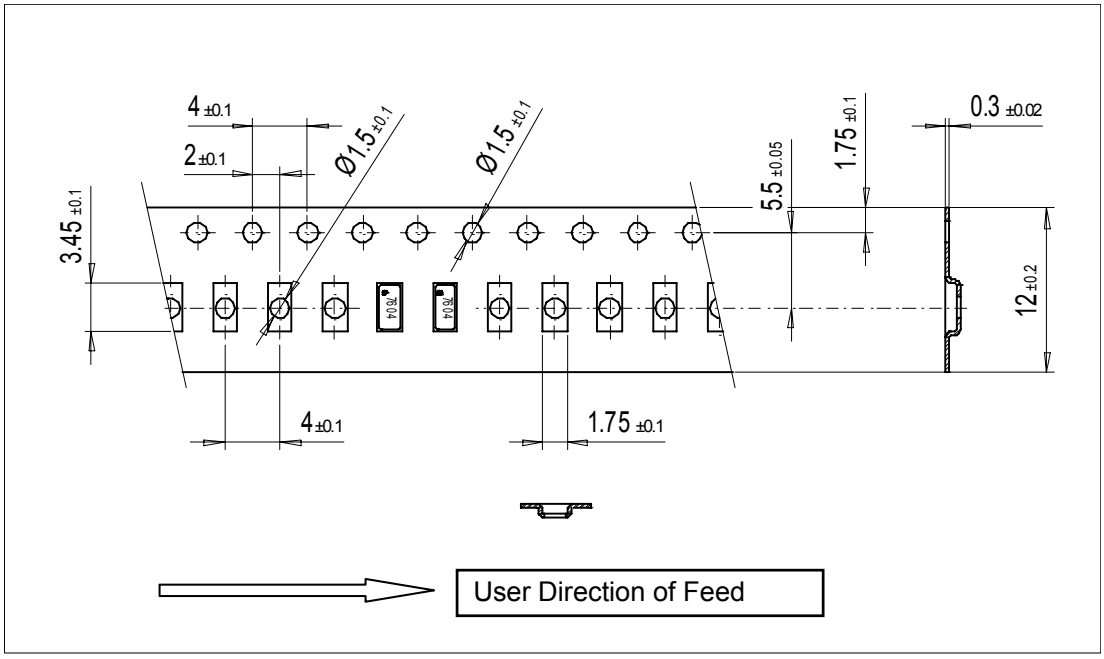
Table 20. **Carrier tape dimensions for QFN16 3 x 3 mm package**

Package	W	D	E	P_0	P_2	F	A_0	B_0	K_0	P_1	T	Unit	Bulk qty
QFN16	12.00 ±0.30	1.50 +0.10 /-0.00	1.75 ±0.10	4.00 ±0.10	2.00 ±0.10	5.50 ±0.05	3.30 ±0.10	3.30 ±0.10	1.10 ±0.10	8.00 ±0.10	0.30 ±0.05	mm	3000

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7.2 LCC8 carrier tape

Figure 30. **Carrier tape for LCC8 1.5 x 3.2 mm package**



Note: Dimensions shown are in millimeters (mm).

7.3 Reel information for QFN16 and LCC8

Figure 31. **Reel schematic**

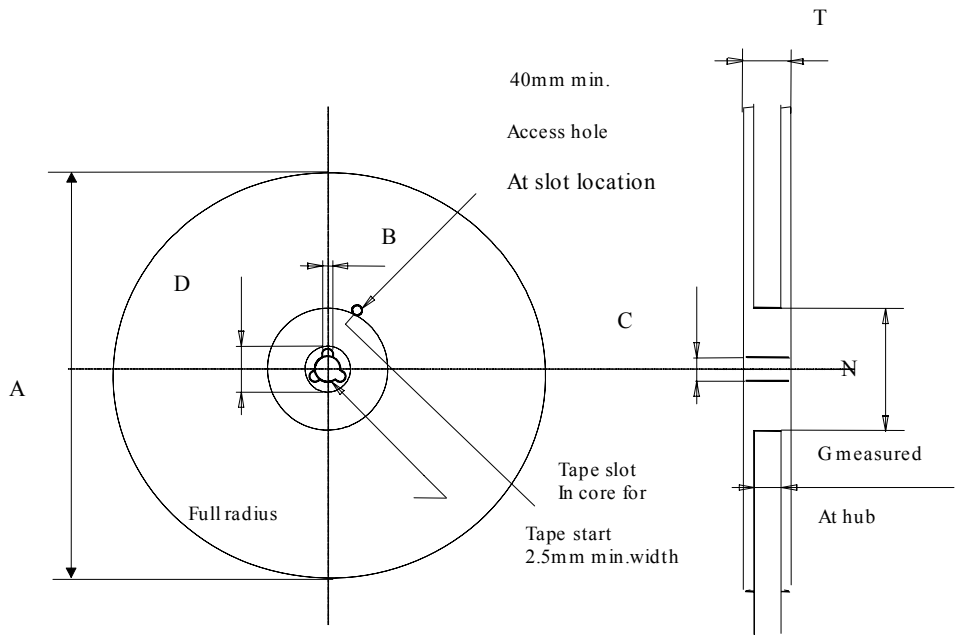


Table 21. Reel dimensions for 12 mm carrier tape - QFN16 and LCC8 packages

Package	A (max)	B (min)	C	D (min)	N (min)	G	T (max)
QFN16	330 mm (13-inch)	1.5 mm	13 mm ± 0.2 mm	20.2 mm	60 mm	12.4 mm + 2/–0 mm	18.4 mm
LCC8	180 mm (7-inch)	1.5 mm	13 mm ± 0.2 mm	20.2 mm	60 mm	12.4 mm + 2/–0 mm	18.4 mm

Note: The dimensions given in Table 21. Reel dimensions for 12 mm carrier tape - QFN16 and LCC8 packages incorporate tolerances that cover all variations on critical parameters.

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8 Part numbering

Table 22. Ordering information scheme

Example:	M41T	62	Q	6	F

Device family

M41T

Device type and supply voltage

62 = V_{CC} = 1.3 V to 4.4 V

64 = V_{CC} = 1.3 V to 4.4 V

65 = V_{CC} = 1.3 V to 4.4 V

Package

Q = QFN16 (3 x 3 mm)

LC = LCC8 (1.5 x 3.2 mm) (M41T62 only)

Temperature range

6 = –40 °C to 85 °C

Shipping method

F = ECOPACK® package, tape & reel

For other options, or for more information on any aspect of this device, please contact the ST sales office nearest you.

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Revision history

Table 23. **Document revision history**

Date	Revision	Changes
21-Feb-2013	20	Updated title of datasheet; updated Section 3.8: "Century bits"; added Figure 21: "Century bits CB1 and CB0; moved and modified Table 8: "Examples using century bits"; added Section 3.9: "Leap year"; added footnote 1 to Table 15: "Crystals suitable for use with M41T6x series RTCs.
21-Aug-2015	21	Removed M41T63 part number and all references to it from document. Moved Table 1: "Device summary" to Section 1: "Description" Replaced Figure 10: "Hardware hookup for SuperCap™ backup operation" Updated Section 6.1: "QFN16 package information" Updated dimension e in Table 19: "LCC8 – 8-pin, 1.5 x 3.2 mm leadless chip carrier package mechanical data"
01-Oct-2015	22	Clarified open drain pull-up supply voltage for devices in Table 13: "DC characteristics"
18-Jan-2019	23	Updated note on Figure 10. Hardware hookup for SuperCap™ backup operation
05-Sep-2019	24	Minor text changes

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