M24C16-W M24C16-R M24C16-F

Datasheet

16-Kbit serial I2C bus EEPROM



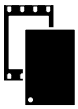
TSSOP8 (DW)

169 mil width



SO8 (MN)

150 mil width



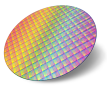
UFDFPN8 (MC)

DFN8 - 2x3 mm



UFDFPN5 (MH)

DFN5 - 1.7x1.4 mm



Unsawn wafer

Product status link
M24C16-W
M24C16-R
M24C16-F

Features

- Compatible with following I^2C bus modes:
  - 400 kHz
  - 100 kHz
- Memory array:
  - 16 Kbit (2 Kbyte) of EEPROM
  - Page size: 16 byte
- Single supply voltage:
  - M24C16-W: 2.5 V to 5.5 V
  - M24C16-R: 1.8 V to 5.5 V
  - M24C16-F: 1.7 V to 5.5 V (full temperature range) and 1.6 V to 1.7 V (limited temperature range)
- Write time:
  - Byte write within 5 ms
  - Page write within 5 ms
- Operating temperature range:
  - from -40 °C up to +85 °C
- Random and sequential read modes
- Write protect of the whole memory array
- Enhanced ESD/latch-up protection
- More than 4 million Write cycles
- More than 200-year data retention

Packages

- SO8 ECOPACK2
- TSSOP8 ECOPACK2
- UFDFPN8 ECOPACK2
- UFDFPN5 ECOPACK2
- Unsawn wafer (each die is tested)

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1 Description

The M24C16 is a 16-Kbit I²C-compatible EEPROM (electrically erasable programmable memory) organized as 2K x 8 bits.

The M24C16-W can be accessed (Read and Write) with a supply voltage from 2.5 V to 5.5 V, the M24C16-R can be accessed (Read and Write) with a supply voltage from 1.8 V to 5.5 V, and the M24C16-F can be accessed with a supply voltage from 1.7 V to 5.5 V (over the full temperature range) or with an extended supply voltage from 1.6 V to 1.7 V. The M24C16-F can also operate down to 1.6 V, under some restricting conditions.

All these devices operate with a clock frequency of 400 kHz (or lower).

Figure 1. Logic diagram

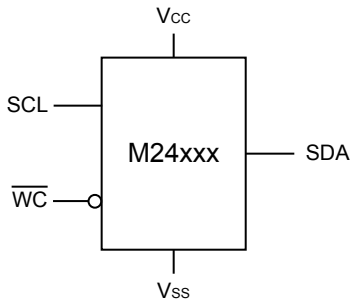
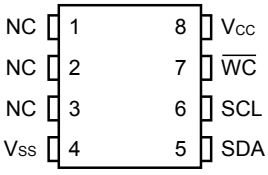


Table 1. Signal names

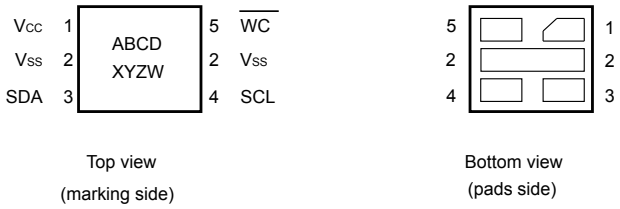
Signal name	Function	Direction
SDA	Serial data	I/O
SCL	Serial clock	Input
$\overline{WC}$	Write control	Input
V_{CC}	Supply voltage	-
V_{SS}	Ground	-

Figure 2. 8-pin package connections, top view



1. NC: Not Connected

Figure 3. UFDFPN5 (DFN5) package connections



1. See Section 9 Package information for package dimensions, and how to identify pin 1

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2 Signal description

2.1 Serial clock (SCL)

The signal applied on the SCL input is used to strobe the data available on SDA(in) and to output the data on SDA(out).

2.2 Serial data (SDA)

SDA is an input/output used to transfer data in or data out of the device. SDA(out) is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A pull-up resistor must be connected from serial data (SDA) to V_{CC} (Figure 11 indicates how to calculate the value of the pull-up resistor).

2.3 Write control ($\overline{WC}$)

This input signal is useful for protecting the entire contents of the memory from inadvertent write operations. Write operations are disabled to the entire memory array when write control ($\overline{WC}$) is driven high. Write operations are enabled when write control ($\overline{WC}$) is either driven low or left floating.

When write control ($\overline{WC}$) is driven high, device select and address bytes are acknowledged, Data bytes are not acknowledged.

2.4 V_{SS} (ground)

V_{SS} is the reference for the V_{CC} supply voltage.

2.5 Supply voltage (V_{CC})

2.5.1 Operating supply voltage (V_{CC})

Prior to selecting the memory and issuing instructions to it, a valid and stable V_{CC} voltage within the specified [V_{CC}(min), V_{CC}(max)] range must be applied (see Operating conditions in Section 8 DC and AC parameters). In order to secure a stable DC supply voltage, it is recommended to decouple the V_{CC} line with a suitable capacitor (usually of the order of 10 nF to 100 nF) close to the V_{CC}/V_{SS} package pins.

This voltage must remain stable and valid until the end of the transmission of the instruction and, for a write instruction, until the completion of the internal write cycle (t_W).

2.5.2 Power-up conditions

The V_{CC} voltage has to rise continuously from 0 V up to the minimum V_{CC} operating voltage (see Operating conditions in Section 8 DC and AC parameters).

2.5.3 Device reset

In order to prevent inadvertent write operations during power-up, a power-on-reset (POR) circuit is included.

At power-up, the device does not respond to any instruction until V_{CC} has reached the internal reset threshold voltage. This threshold is lower than the minimum V_{CC} operating voltage (see Operating conditions in Section 8 DC and AC parameters). When V_{CC} passes over the POR threshold, the device is reset and enters the Standby Power mode; the device must not be accessed until V_{CC} reaches a valid and stable DC voltage within the specified [V_{CC}(min), V_{CC}(max)] range (see Operating conditions in Section 8 DC and AC parameters).

In a similar way, during power-down (continuous decrease in V_{CC}), the device must not be accessed when V_{CC} drops below V_{CC}(min). When V_{CC} drops below the threshold voltage, the device stops responding to any instruction sent to it.

2.5.4 Power-down conditions

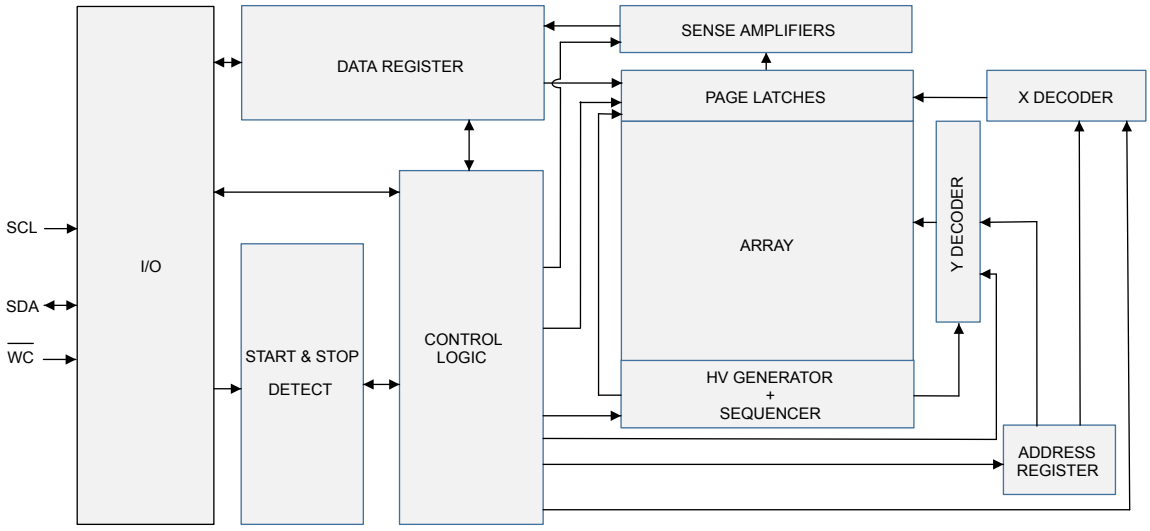
During power-down (continuous decrease in V_{CC}), the device must be in the standby power mode (mode reached after decoding a Stop condition, assuming that there is no internal write cycle in progress).

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3 Memory organization

The memory is organized as shown below.

Figure 4. Block diagram

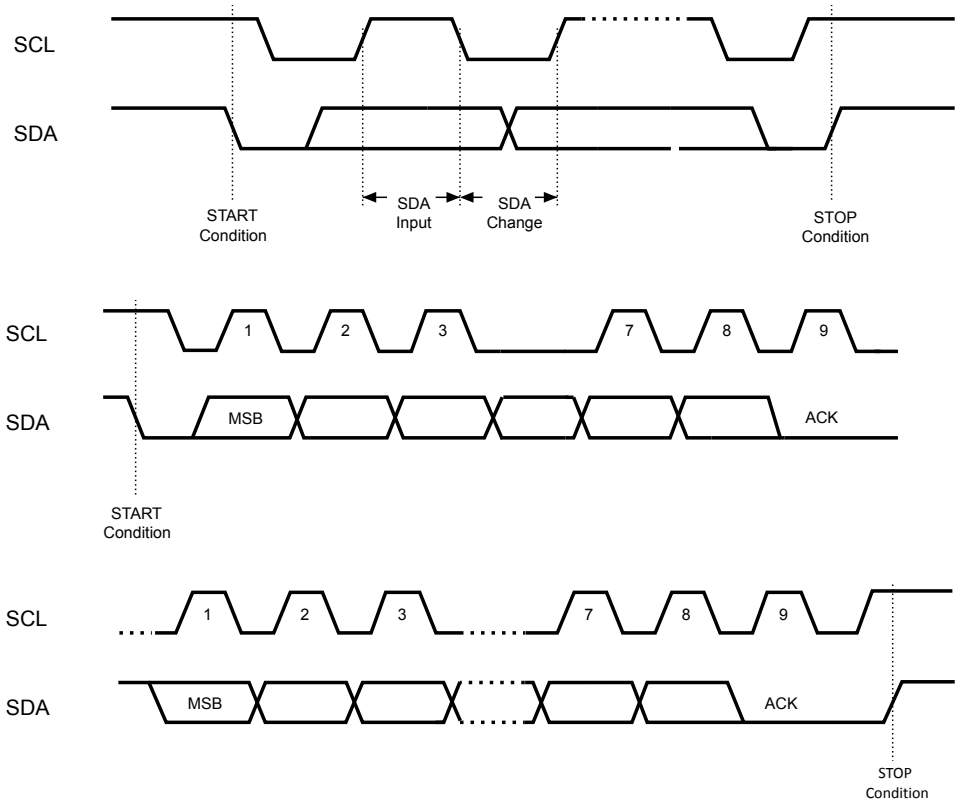


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4 Device operation

The device supports the I²C protocol (see Figure 5). Any device that sends data on to the bus is defined a transmitter, and any device that reads the data a receiver. The device that controls the data transfer is known as the bus master, and the other as the slave device. A data transfer can only be initiated by the bus master, which also provides the serial clock for synchronization. The device is always a slave in all communications.

Figure 5. I²C bus protocol



4.1 Start condition

Start is identified by a falling edge of serial data (SDA) while serial clock (SCL) is stable in the high state. A start condition must precede any data transfer instruction. The device continuously monitors (except during a write cycle) serial data (SDA) and serial clock (SCL) for a start condition.

4.2 Stop condition

Stop is identified by a rising edge of serial data (SDA) while serial clock (SCL) is stable and driven high. A stop condition terminates communication between the device and the bus master. A Read instruction that is followed by NoAck can be followed by a stop condition to force the device into the standby mode.

A stop condition at the end of a Write instruction triggers the internal write cycle.

4.3 Data input

During data input, the device samples serial data (SDA) on the rising edge of serial clock (SCL). For correct device operation, serial data (SDA) must be stable during the rising edge of serial clock (SCL), and the serial data (SDA) signal must change only when serial clock (SCL) is driven low.

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4.4 Acknowledge bit (ACK)

The acknowledge bit is used to indicate a successful byte transfer. The bus transmitter, whether it be bus master or slave device, releases serial data (SDA) after sending eight bits of data. During the ninth clock pulse period, the receiver pulls serial data (SDA) low to acknowledge the receipt of the eight data bits.

4.5 Device addressing

To start communication between the bus master and the slave device, the bus master must initiate a Start condition. Following this, the bus master sends the device select code, shown in not Table 2 (most significant bit first).

Table 2. Device select code

Device type identifier(1)				Chip enable address			RW̄
b7	b6	b5	b4	b3	b2	b1	b0
1	0	1	0	A10	A9	A8	RW̄

1. *The most significant bit, b7, is sent first.*

The eighth bit is the Read/Write bit (R/W̄), set to 1 / 0, respectively, for Read / Write operations.

If a match occurs on the device select code, the corresponding device gives an acknowledgement on serial data (SDA) during the ninth bit time. If the device does not match the device select code, it deselects itself from the bus, and goes into standby mode.

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5 Instructions

5.1 Write operations

Following a start condition the bus master sends a device select code with the R/$\overline{W}$ bit (R$\overline{W}$) reset to 0. The device acknowledges this, as shown in Figure 6, and waits for the address byte. The device responds to each address byte with an acknowledge bit, and then waits for the data byte.

Table 3. Address byte

A7	A6	A5	A4	A3	A2	A1	A0

When the bus master generates a stop condition immediately after a data byte Ack bit (in the "10th bit" time slot), either at the end of a byte write or a page write, the internal write cycle t_W is triggered. A stop condition at any other time slot does not trigger the internal write cycle.

After the stop condition and the successful completion of an internal write cycle (t_W), the device internal address counter is automatically incremented to point to the next byte after the last modified byte.

During the internal write cycle, serial data (SDA) is disabled internally, and the device does not respond to any requests.

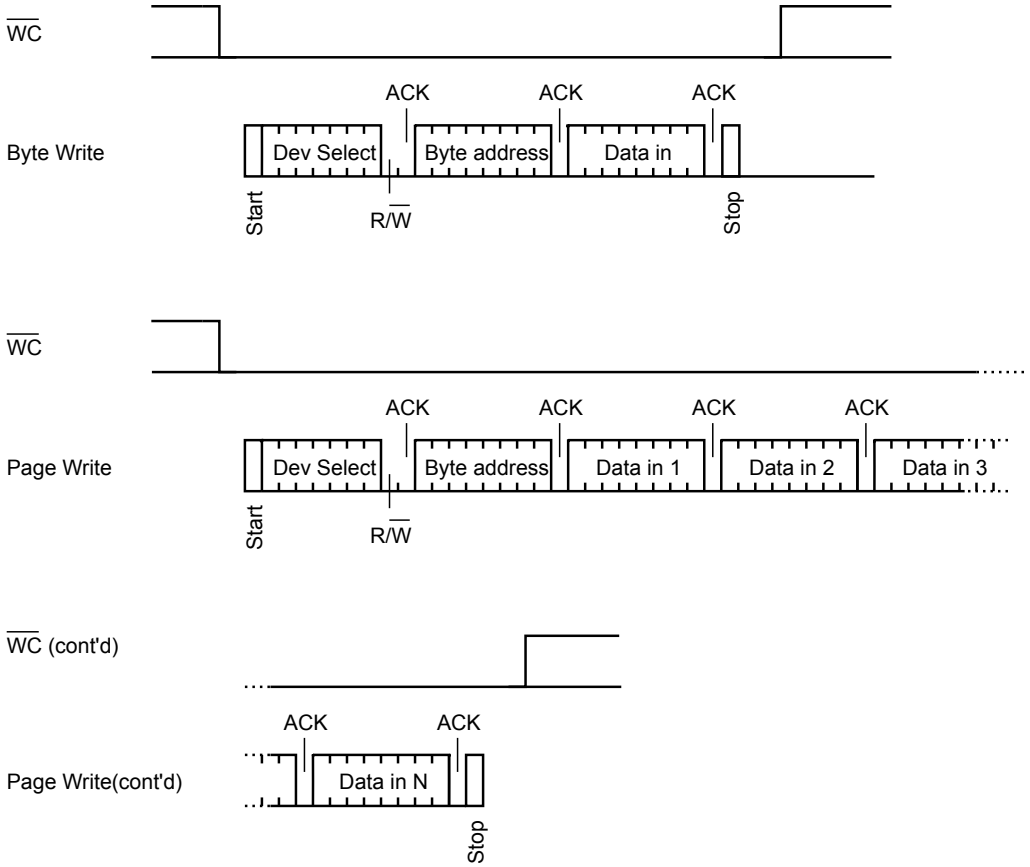
If the write control input ($\overline{WC}$) is driven high, the Write instruction is not executed and the accompanying data bytes are *not acknowledged* , as shown in Figure 7.

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5.1.1 Byte write

After the device select code and the address byte, the bus master sends one data byte. If the addressed location is write-protected, by write control ($\overline{WC}$) being driven high, the device replies with NoAck, and the location is not modified. If, instead, the addressed location is not write-protected, the device replies with Ack. The bus master terminates the transfer by generating a stop condition, as shown in Figure 6.

Figure 6. Write mode sequences with $\overline{WC}$ = 0 (data write enabled)



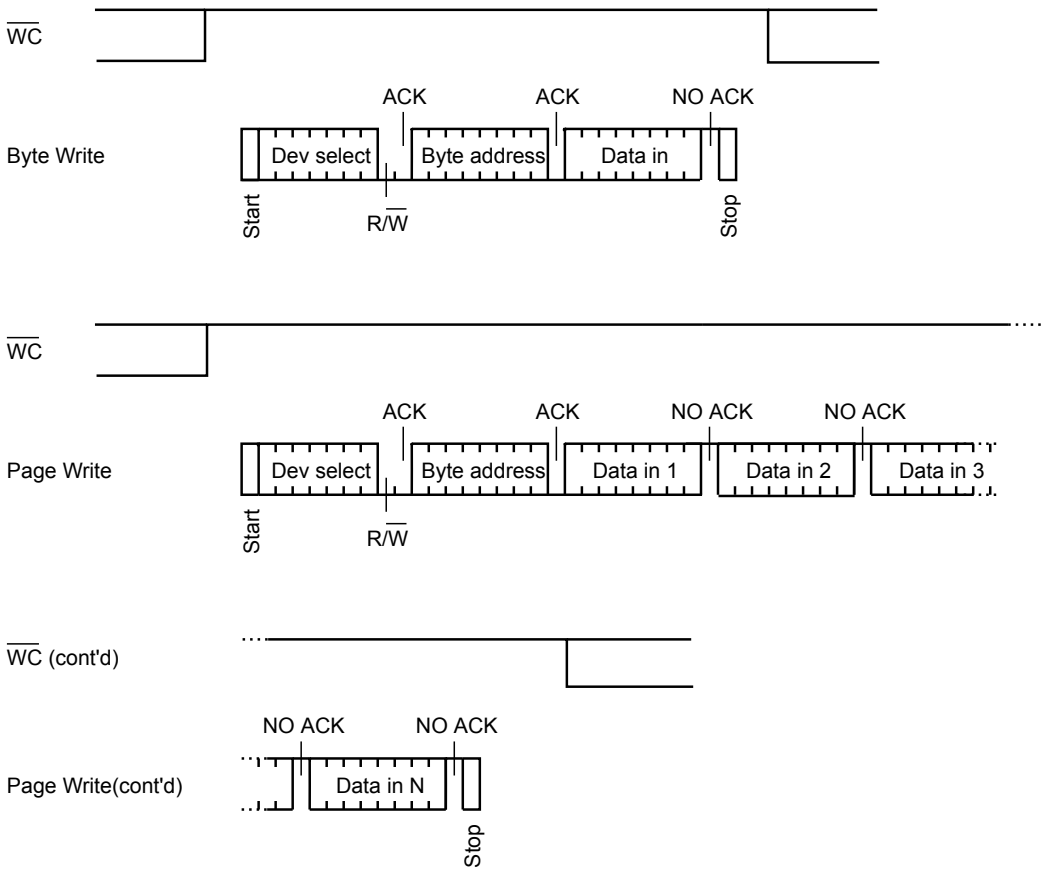
5.1.2 Page Write

The page write mode allows up to 16 byte to be written in a single write cycle, provided that they are all located in the same page in the memory: that is, the most significant memory address bits, A10/A4, are the same. If more bytes are sent than fit up to the end of the page, a "roll-over" occurs, i.e. the bytes exceeding the page end are written on the same page, from location 0.

The bus master sends from 1 to 16 byte of data, each of which is acknowledged by the device if write control ($\overline{WC}$) is low. If write control ($\overline{WC}$) is high, the contents of the addressed memory location are not modified, and each data byte is followed by a NoAck, as shown in Figure 7. After each transferred byte, the internal page address counter is incremented.

The transfer is terminated by the bus master generating a Stop condition.

Figure 7. Write mode sequences with $\overline{WC}$ = 1 (data write inhibited)



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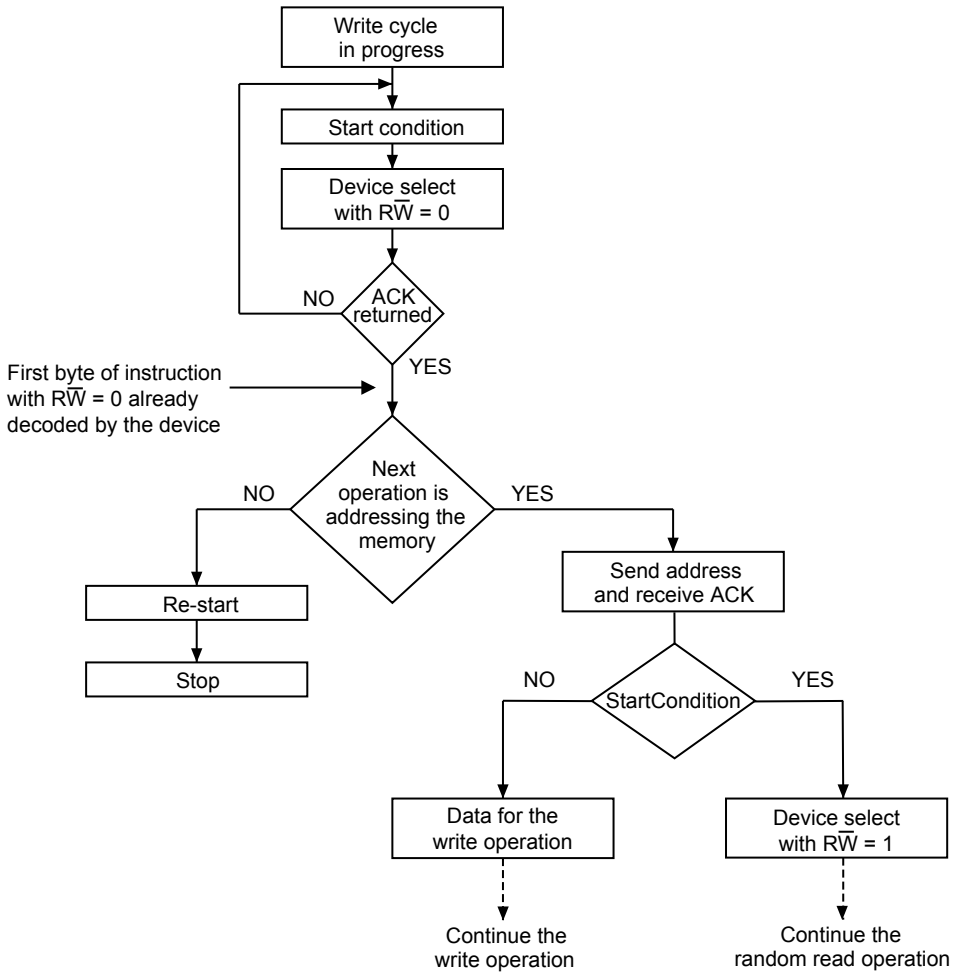
5.1.3 Minimizing write delays by polling on ACK

The maximum write time (t_w) is shown in AC characteristics tables in Section 8 DC and AC parameters, but the typical time is shorter. To make use of this, a polling sequence can be used by the bus master.

The sequence, as shown in Figure 8, is:

- Initial condition: a write cycle is in progress.
- Step 1: the bus master issues a Start condition followed by a device select code (the first byte of the new instruction).
- Step 2: if the device is busy with the internal write cycle, no ACK is returned and the bus master goes back to step 1. If the device has terminated the internal write cycle, it responds with an ACK, indicating that the device is ready to receive the second part of the instruction (the first byte of this instruction having been sent during Step 1).

Figure 8. Write cycle polling flowchart using ACK



Note: The seven most significant bits of the device select code of a random read (bottom right box in the figure)must be identical to the seven most significant bits of the device select code of the write (polling instruction in the figure).

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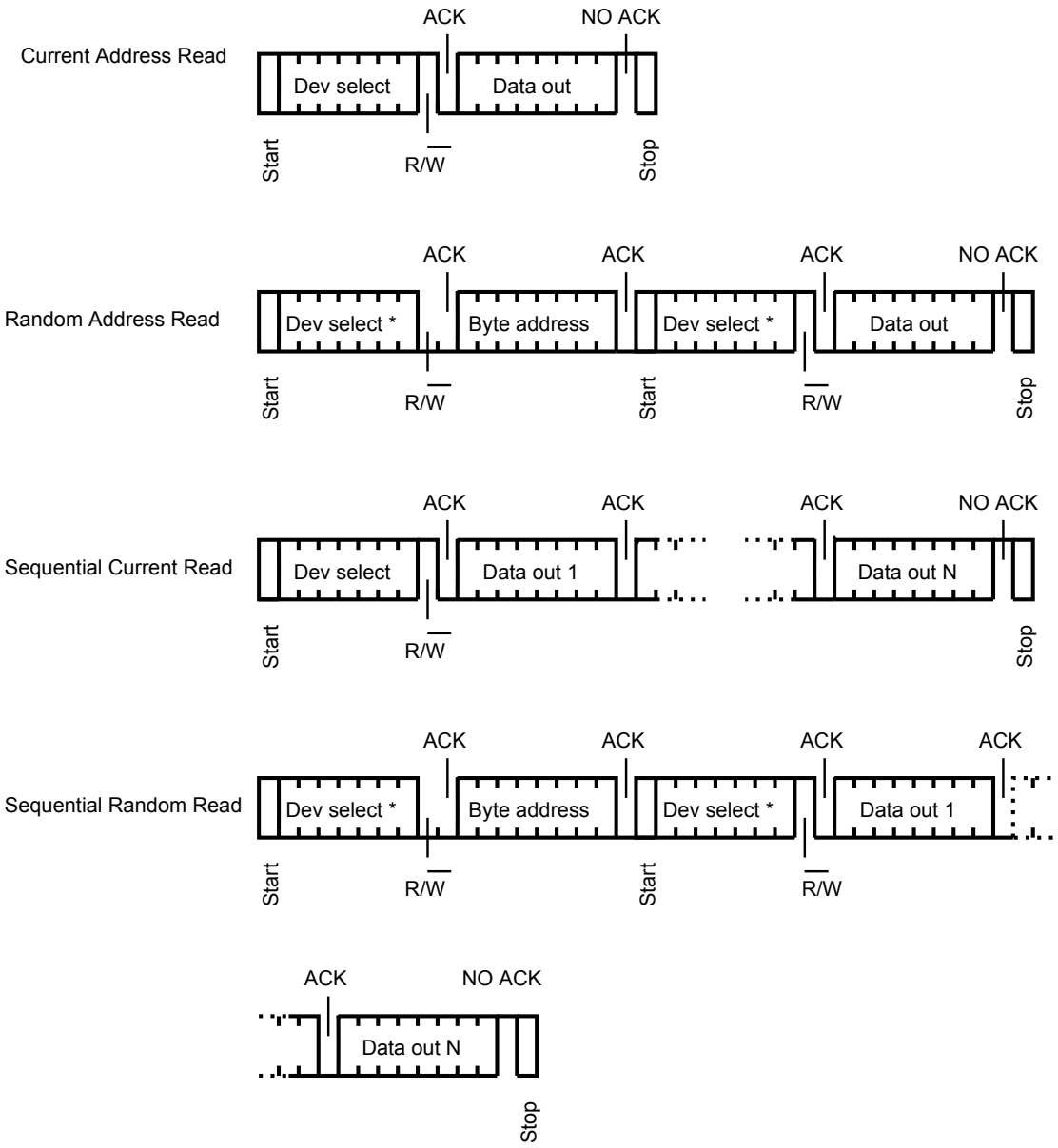
5.2 Read operations

Read operations are performed independently of the state of the write control ($\overline{WC}$) signal.

After the successful completion of a read operation, the device internal address counter is incremented by one, to point to the next byte address.

For the read instructions, after each byte read (data out), the device waits for an acknowledgement (data in) during the 9th bit time. If the bus master does not acknowledge during this 9th time, the device terminates the data transfer and switches to its standby mode.

Figure 9. Read mode sequences



5.2.1 Random address read

A dummy write is first performed to load the address into this address counter (as shown in Figure 9) but without sending a stop condition. Then, the bus master sends another start condition, and repeats the device select code, with the R/$\overline{W}$ bit set to 1. The device acknowledges this, and outputs the contents of the addressed byte. The bus master must not acknowledge the byte, and terminates the transfer with a stop condition.

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5.2.2 Current address read

For the current address read operation, following a start condition, the bus master only sends a device select code with the R/$\overline{W}$ bit set to 1. The device acknowledges this, and outputs the byte addressed by the internal address counter. The counter is then incremented. The bus master terminates the transfer with a stop condition, as shown in Figure 9, without acknowledging the byte.

5.2.3 Sequential read

This operation can be used after a current address read or a random address read. The bus master does acknowledge the data byte output, and sends additional clock pulses so that the device continues to output the next byte in sequence. To terminate the stream of bytes, the bus master must not acknowledge the last byte, and must generate a stop condition, as shown in Figure 9.

The output data comes from consecutive addresses, with the internal address counter automatically incremented after each byte output. After the last memory address, the address counter "rolls-over", and the device continues to output data from memory address 00h.

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6 Initial delivery state

The device is delivered with all the memory array bits set to 1 (each byte contains FFh).

When delivered in unsawn wafer, all memory bits are set to 1 (each memory byte contains FFh) except the last byte located at address FFFh which is written with the value 22h.

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7 Maximum ratings

Stressing the device outside the ratings listed in Table 4 may cause permanent damage to it. These are stress ratings only, and operation of the device at these, or any other conditions outside those indicated in the operating sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
T_A	Ambient operating temperature	-40	130	° C
T_{STG}	Storage temperature	–65	150	° C
T_{LEAD}	Lead temperature during soldering	see note (1)		° C
I_{OL}	DC output current (SDA = 0)	-	5	mA
V_{IO}	Input or output range	–0.50	6.5	V
V_{CC}	Supply voltage	–0.50	6.5	V
V_{ESD}	Electrostatic pulse (human body model)(2)	-	3000	V

1. *Compliant with JEDEC Std J-STD-020D (for small body, Sn-Pb or Pb-free assembly), the ST ECOPACK 7191395 specification, and the European directive on Restrictions of Hazardous Substances (RoHS directive 2011/65/EU of July 2011).*
2. *Positive and negative pulses applied on different combinations of pin connections, according to AEC-Q100-002 (compliant with ANSI/ESDA/JEDEC JS-001-2012 standard, C1=100 pF, R1=1500 Ω).*

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8 DC and AC parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device.

Table 5. Operating conditions (voltage range W)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	2.5	5.5	V
T_A	Ambient operating temperature	-40	85	° C
f_C	Operating clock frequency	-	400	kHz

Table 6. Operating conditions (voltage range R)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	1.8	5.5	V
T_A	Ambient operating temperature	-40	85	° C
f_C	Operating clock frequency	-	400	kHz

Table 7. Operating conditions (voltage range F)

Symbol	Parameter	Min.			Max.	Unit
V_{CC}	Supply voltage	1.60	1.65	1.70	5.5	V
T_A	Ambient operating temperature: READ	-40	-40	-40	85	° C
	Ambient operating temperature: WRITE	0	-20	-40	85	
f_C	Operating clock frequency	-	-	-	400	kHz

Table 8. AC measurement conditions

Symbol	Parameter	Min.	Max.	Unit
C_{bus}	Load capacitance	-	100	pF
-	SCL input rise/fall time, SDA input fall time	-	50	ns
-	Input levels	0.2 V_{CC} to 0.8 V_{CC}		V
-	Input and output timing reference levels	0.3 V_{CC} to 0.7 V_{CC}		

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Figure 10. AC measurement I/O waveform

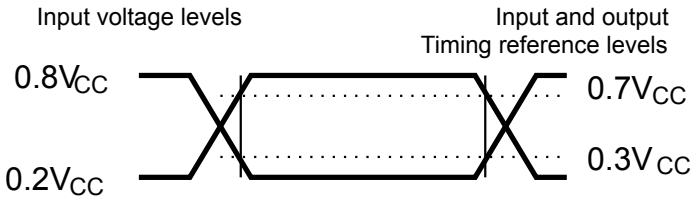


Table 9. Input parameters

Symbol	Parameter[1]	Test condition	Min.	Max.	Unit
C_{IN}	Input capacitance (SDA)	-	-	8	pF
C_{IN}	Input capacitance (other pins)	-	-	6	
Z_L	Input impedance ($\overline{WC}$)	$V_{IN} < 0.3\ V_{CC}$	30	-	kΩ
Z_H		$V_{IN} > 0.7\ V_{CC}$	500	-	

1. *Characterized only, not tested in production.*

Table 10. Cycling performance

Symbol	Parameter	Test condition	Max	Unit
Ncycle	Write cycle endurance [1]	$T_A \leq$ 25 °C, $V_{CC}(min) < V_{CC} < V_{CC}(max)$	4,000,000	Write cycle [2]
		$T_A =$ 85 °C, $V_{CC}(min) < V_{CC} < V_{CC}(max)$	1,200,000	

1. *The write cycle endurance is defined by characterization and qualification.*
2. *A write cycle is executed when either a page write or a byte write instruction is decoded.*

Table 11. Memory cell data retention

Parameter	Test condition	Min.	Unit
Data retention [1]	T_A = 55 °C	200	Year

1. *The data retention behaviour is checked in production, while the data retention limit defined in this table is extracted from characterization and qualification results.*

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Table 12. DC characteristics (M24C16-W, device grade 6)

Symbol	Parameter	Test conditions (in addition to those in Table 5 and Table 8)	Min.	Max.	Unit
I_{LI}	Input leakage current (SCL, SDA)	$V_{IN} = V_{SS}$ or V_{CC}, device in Standby mode	-	± 2	µA
I_{LO}	Output leakage current	SDA in Hi-Z, external voltage applied on SDA: V_{SS} or V_{CC}	-	± 2	
I_{CC}	Supply current (Read)	V_{CC} = 5.5 V, f_c = 400 kHz	-	1	mA
		V_{CC} = 2.5 V, f_c = 400 kHz	-	1	
I_{CC0}	Supply current (Write)	Value overaged over t_W, 2.5 V ≤ V_{CC} ≤ 5.5 V	-	1(1)	
I_{CC1}	Standby supply current	Device not selected(2), $V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 2.5 V	-	2	µA
		Device not selected(2), $V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5.5 V	-	3	
V_{IL}	Input low voltage (SCL, SDA, $\overline{WC}$)	-	–0.45	0.3 V_{CC}	V
V_{IH}	Input high voltage (SCL, SDA, $\overline{WC}$)	-	0.7 V_{CC}	V_{CC} +1	
V_{OL}	Output low voltage	I_{OL} = 2.1 mA, V_{CC} = 2.5 V or I_{OL} = 3 mA, V_{CC} = 5.5 V	-	0.4	

1. *Characterized only, not tested in production.*
2. *The device is not selected after power-up, after a Read instruction (after the stop condition), or after the completion of the internal write cycle t_W (t_W is triggered by the correct decoding of a Write instruction).*

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Table 13. DC characteristics (M24C16-R device grade 6)

Symbol	Parameter	Test conditions[1] (in addition to those in Table 6 and Table 8)	Min.	Max.	Unit
I_{LI}	Input leakage current (SCL, SDA)	V_{IN} = V_{SS} or V_{CC}, device in Standby mode	-	± 2	µA
I_{LO}	Output leakage current	SDA in Hi-Z, external voltage applied on SDA: V_{SS} or V_{CC}	-	± 2	
I_{CC}	Supply current (Read)	V_{CC} = 1.8 V, f_c= 400 kHz	-	0.8	mA
I_{CC0}	Supply current (Write)	Value overaged over t_W V_{CC} ≤ 2.5 V	-	1[2]	
I_{CC1}	Standby supply current	Device not selected[3], V_{IN} = V_{SS} or V_{CC}, V_{CC} = 1.8 V	-	1	µA
V_{IL}	Input low voltage (SCL, SDA, $\overline{WC}$)	2.5 V ≤ V_{CC}	–0.45	0.3 V_{CC}	V
		V_{CC} < 2.5 V	–0.45	0.25 V_{CC}	
V_{IH}	Input high voltage (SCL, SDA)	V_{CC} < 2.5 V	0.75 V_{CC}	6.5	
	Input high voltage ($\overline{WC}$)	V_{CC} < 2.5 V	0.75 V_{CC}	V_{CC}+ 0.6	
V_{OL}	Output low voltage	I_{OL} = 0.7 mA, V_{CC} = 1.8 V	-	0.2	

1. *If the application uses the voltage range R device with 2.5 V ≤ V_{cc} ≤ 5.5 V and -40 ° C < T_A < +85 ° C refer to Table 12 instead of this table.*
2. *Characterized value, not tested in production.*
3. *The device is not selected after power-up, after a Read instruction (after the Stop condition), or after the completion of the internal write cycle t_W (t_W is triggered by the correct decoding of a Write instruction).*

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Table 14. DC characteristics (M24C16-F device grade 6)

Symbol	Parameter	Test conditions[1] (in addition to those in Table 7 and Table 8)	Min.	Max.	Unit
I_{LI}	Input leakage current (SCL, SDA)	V_{IN} = V_{SS} or V_{CC}, device in standby mode	-	± 2	µA
I_{LO}	Output leakage current	SDA in Hi-Z, external voltage applied on SDA: V_{SS} or V_{CC}	-	± 2	
I_{CC}	Supply current (Read)	V_{CC} = 1.6 V or 1.7 V, f_c= 400 kHz	-	0.8	mA
I_{CC0}	Supply current (Write)	Value overaged over t_W, V_{CC} ≤ 2.5 V	-	1[2]	
I_{CC1}	Standby supply current	Device not selected[3], V_{IN} = V_{SS} or V_{CC}, V_{CC} ≤ 1.8 V	-	1	µA
V_{IL}	Input low voltage (SCL, SDA, $\overline{WC}$)	2.5 V ≤ V_{CC}	–0.45	0.3 V_{CC}	V
		V_{CC} < 2.5 V	–0.45	0.25 V_{CC}	
V_{IH}	Input high voltage (SCL, SDA)	V_{CC} < 2.5 V	0.75 V_{CC}	6.5	
	Input high voltage ($\overline{WC}$)	V_{CC} < 2.5 V	0.75 V_{CC}	V_{CC}+0.6	
V_{OL}	Output low voltage	I_{OL} = 0.7 mA, V_{CC} ≤ 1.8 V	-	0.2	

1. *If the application uses the voltage range F device with 1.8 V ≤ V_{cc} ≤ 5.5 V refer to Table 12 instead of this table.*
2. *Characterized only, not tested in production.*
3. *The device is not selected after power-up, after a Read instruction (after the Stop condition), or after the completion of the internal write cycle t_W (t_W is triggered by the correct decoding of a Write instruction).*

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Table 15. 400 kHz AC characteristics

Symbol	Alt.	Parameter	Min.	Max.	Unit
f_C	f_{SCL}	Clock frequency	-	400	kHz
t_{CHCL}	t_{HIGH}	Clock pulse width high	600	-	ns
t_{CLCH}	t_{LOW}	Clock pulse width low	1300	-	
t_{QL1QL2}(1)	t_F	SDA fall time	20(2)	300	
t_{XH1XH2}	t_R	Input signal rise time	(3)	(3)	
t_{XL1XL2}	t_F	Input signal fall time	(3)	(3)	
t_{DXCH}	$t_{SU:DAT}$	Data in setup time	100	-	
t_{CLDX}	$t_{HD:DAT}$	Data in hold time	0	-	
t_{CLQX}(4)	t_{DH}	Data out hold time	100	-	
t_{CLQV}(5)	t_{AA}	Clock low to next data valid (access time)	-	900	
t_{CHDL}	$t_{SU:STA}$	Start condition setup time	600	-	
t_{DLCL}	$t_{HD:STA}$	Start condition hold time	600	-	
t_{CHDH}	$t_{SU:STO}$	Stop condition setup time	600	-	
t_{DHDL}	t_{BUF}	Time between Stop condition and next Start condition	1300	-	
t_W	t_{WR}	Write time	-	5	ms
t_{NS}(1)	-	Pulse width ignored (input filter on SCL and SDA), single glitch	-	100	ns

1. *Characterized only, not tested in production.*
2. *With C_L = 10 pF.*
3. *There are no minimum or maximum values for the input signal rise and fall times. It is however recommended by the I²C specification that the input signal rise and fall times are between 20 and 300 ns when f_C < 400 kHz.*
4. *The minimum value for t_{CLQX} (Data out hold time) of the M24xxx devices offers a safe timing to bridge the undefined region of the falling edge SCL.*
5. *t_{CLQV} is the time (from the falling edge of SCL) required by the SDA bus line to reach either 0.3 V_{CC} or 0.7 V_{CC}, assuming that R_{bus} x C_{bus} time constant is within the values specified in Figure 12.*

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Table 16. 100 kHz AC characteristics (I^2C Standard mode)

Symbol	Alt.	Parameter	Min.	Max.	Unit
f_C	f_{SCL}	Clock frequency	-	100	kHz
t_{CHCL}	t_{HIGH}	Clock pulse width high	4	-	µs
t_{CLCH}	t_{LOW}	Clock pulse width low	4.7	-	
t_{XH1XH2}	t_R	Input signal rise time	-	1	
t_{XL1XL2}	t_F	Input signal fall time	-	300	ns
t_{QL1QL2}(1)	t_F	SDA fall time	-	300	
t_{DXCH}	$t_{SU:DAT}$	Data in setup time	250	-	
t_{CLDX}	$t_{HD:DAT}$	Data in hold time	0	-	
t_{CLQX}(2)	t_{DH}	Data out hold time	200	-	
t_{CLQV}(3)	t_{AA}	Clock low to next data valid (access time)	-	3450	
t_{CHDL}(4)	$t_{SU:STA}$	Start condition setup time	4.7	-	µs
t_{DLCL}	$t_{HD:STA}$	Start condition hold time	4	-	
t_{CHDH}	$t_{SU:STO}$	Stop condition setup time	4	-	
t_{DHDL}	t_{BUF}	Time between Stop condition and next Start condition	4.7	-	
t_W	t_{WR}	Write time	-	5	ms
t_{NS}(1)	-	Pulse width ignored (input filter on SCL and SDA), single glitch	-	100	ns

1. *Characterized only.*
2. *To avoid spurious Start and Stop conditions, a minimum delay is placed between SCL=1 and the falling or rising edge of SDA.*
3. *t_{CLQV} is the time (from the falling edge of SCL) required by the SDA bus line to reach either 0.3 V_{CC} or 0.7 V_{CC}, assuming that R_{bus} x C_{bus} time constant is within the values specified in Figure 12.*
4. *For a reStart condition, or following a Write cycle.*

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Figure 11. Maximum R_{bus} vs. bus parasitic capacitance (C_{bus}) for an I^2C bus at maximum frequency f_C = 400 kHz

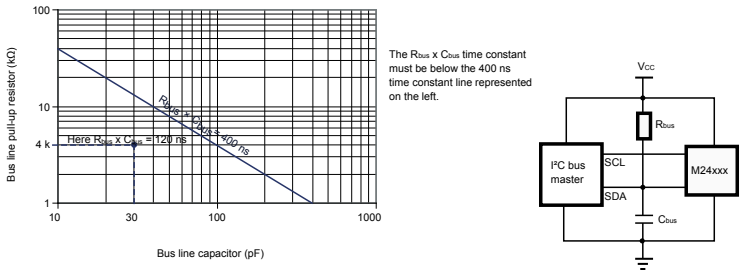
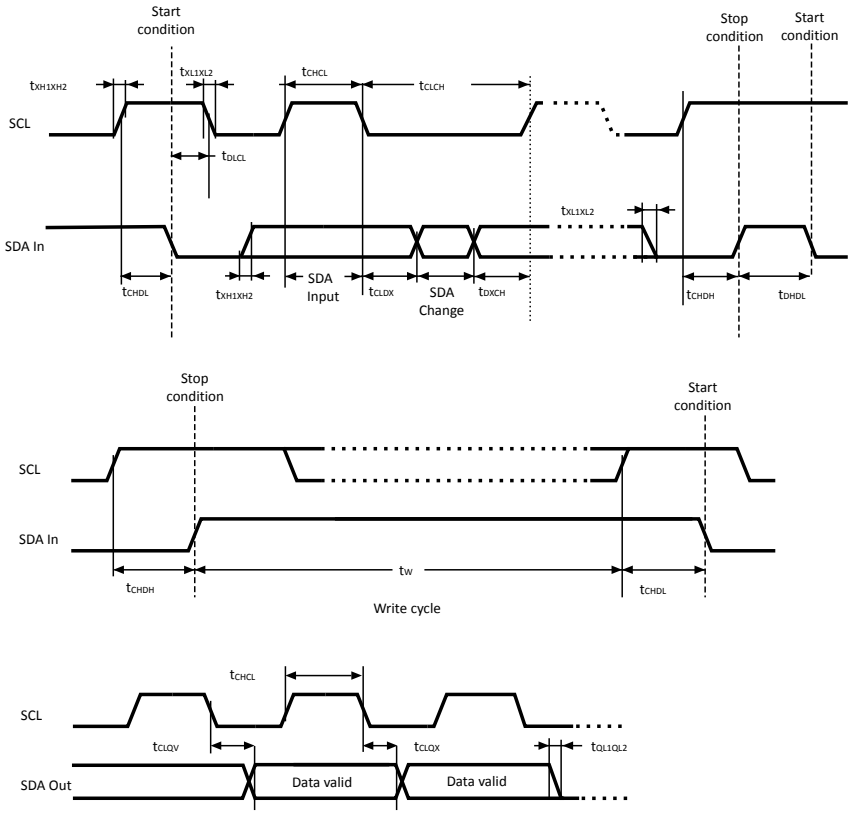


Figure 12. AC waveforms



9 Package information

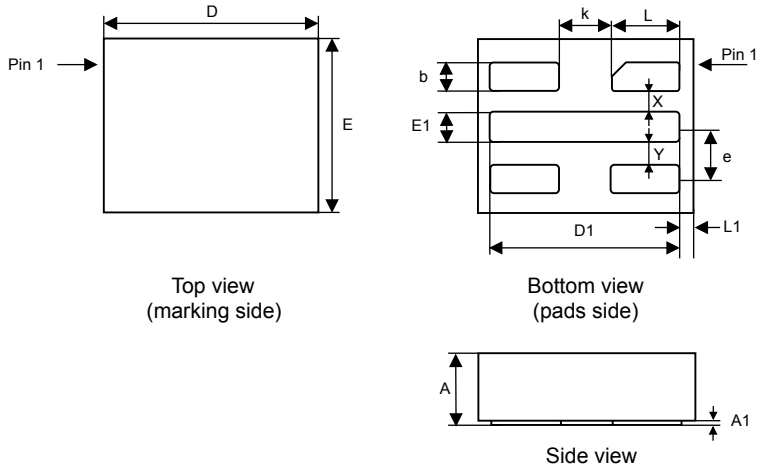
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at www.st.com. ECOPACK is an ST trademark.

For die information concerning the M24C16 delivered in unsawn wafer, please contact your nearest ST Sales Office.

9.1 UFDFPN5 (DFN5) package information

UFDFPN5 is a 5-lead, 1.7 × 1.4 mm, 0.55 mm thickness, ultra thin fine pitch dual flat package.

Figure 13. UFDFPN5 - Outline



1. Maximum package warpage is 0.05 mm.
2. Exposed copper is not systematic and can appear partially or totally according to the cross section.
3. Drawing is not to scale.
4. On the bottom side, pin 1 is identified by the specific pad shape and, on the top side, pin 1 is defined from the orientation of the marking. When reading the marking, pin 1 is below the upper left package corner.

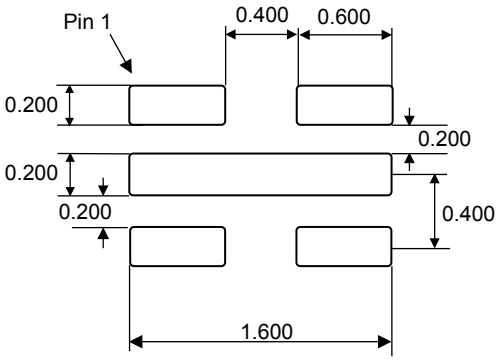
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Table 17. UFDFPN5 - Mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	-	0.050	0.0000	-	0.0020
b[2]	0.175	0.200	0.225	0.0069	0.0079	0.0089
D	1.600	1.700	1.800	0.0630	0.0669	0.0709
D1	1.400	1.500	1.600	0.0551	0.0591	0.0630
E	1.300	1.400	1.500	0.0512	0.0551	0.0591
E1	0.175	0.200	0.225	0.0069	0.0079	0.0089
X	-	0.200	-	-	0.0079	-
Y	-	0.200	-	-	0.0079	-
e	-	0.400	-	-	0.0157	-
L	0.500	0.550	0.600	0.0197	0.0217	0.0236
L1	-	0.100	-	-	0.0039	-
k	-	0.400	-	-	0.0157	-

1. *Values in inches are converted from mm and rounded to four decimal digits.*
2. *Dimension b applies to plated terminal and is measured between 0.15 and 0.30mm from the terminal tip.*

Figure 14. UFDFPN5 - Recommended footprint



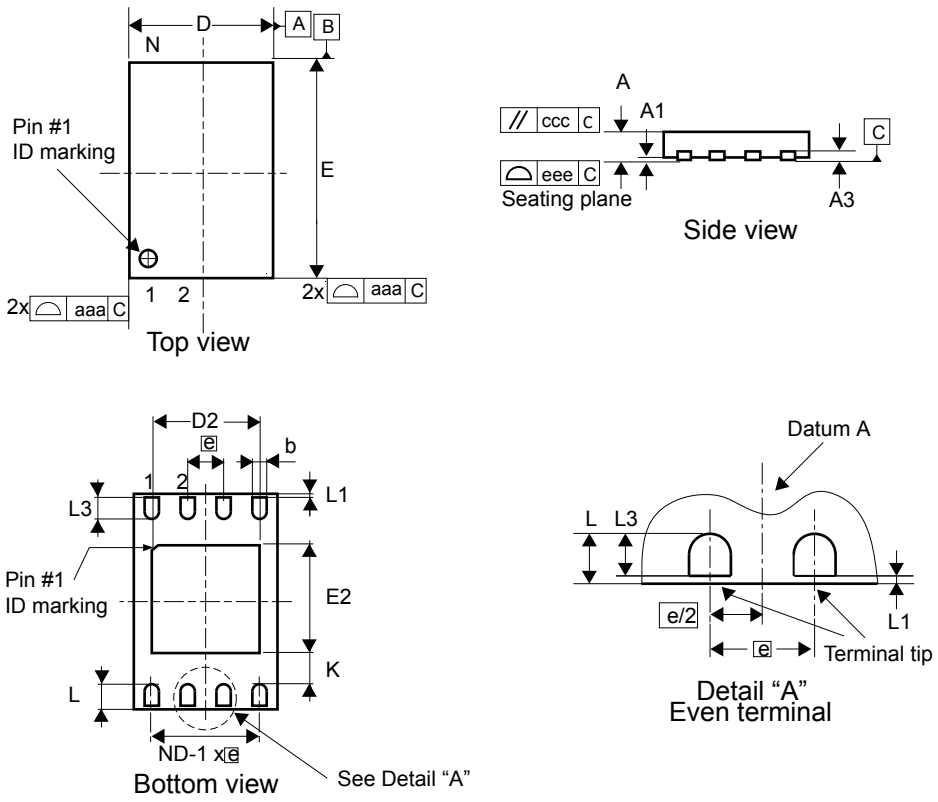
Note: Dimensions are expressed in millimeters.

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9.2 UFDFPN8 (DFN8) package information

UFDFPN8 is an 8-lead, 2 × 3 mm, 0.55 mm thickness ultra thin profile fine pitch dual flat package.

Figure 15. UFDFPN8 - Outline



1. Maximum package warpage is 0.05 mm.
2. Exposed copper is not systematic and can appear partially or totally according to the cross section.
3. Drawing is not to scale.
4. The central pad (the area E2 by D2 in the above illustration) must be either connected to V_{SS} or left floating (not connected) in the end application.

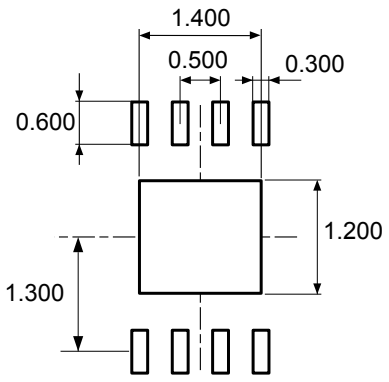
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Table 18. UFDFPN8 - Mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.450	0.550	0.600	0.0177	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
b[2]	0.200	0.250	0.300	0.0079	0.0098	0.0118
D	1.900	2.000	2.100	0.0748	0.0787	0.0827
D2	1.200	-	1.600	0.0472	-	0.0630
E	2.900	3.000	3.100	0.1142	0.1181	0.1220
E2	1.200	-	1.600	0.0472	-	0.0630
e	-	0.500	-	0.0197		
K	0.300	-	-	0.0118	-	-
L	0.300	-	0.500	0.0118	-	0.0197
L1	-	-	0.150	-	-	0.0059
L3	0.300	-	-	0.0118	-	-
aaa	-	-	0.150	-	-	0.0059
bbb	-	-	0.100	-	-	0.0039
ccc	-	-	0.100	-	-	0.0039
ddd	-	-	0.050	-	-	0.0020
eee[3]	-	-	0.080	-	-	0.0031

1. *Values in inches are converted from mm and rounded to four decimal digits.*
2. *Dimension b applies to plated terminal and is measured between 0.15 and 0.30 mm from the terminal tip.*
3. *Applied for exposed die paddle and terminals. Exclude embedding part of exposed die paddle from measuring.*

Figure 16. UFDFPN8 - Recommended footprint



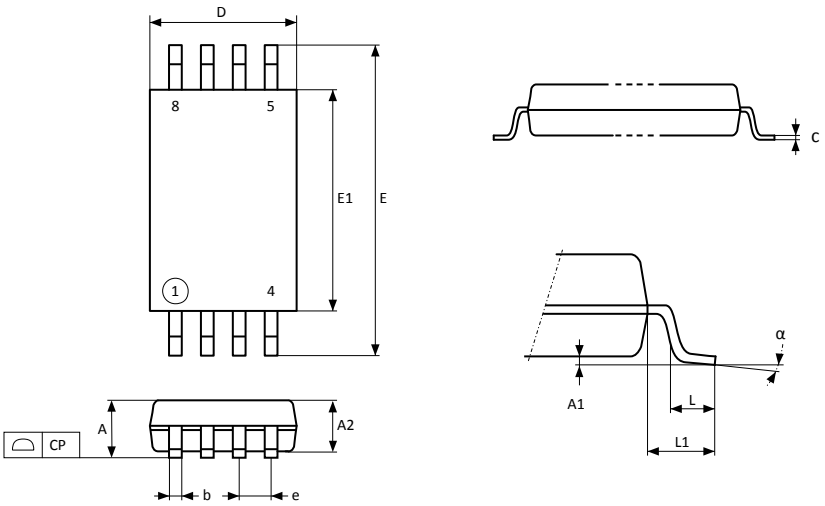
1. Dimensions are expressed in millimeters.

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9.3 TSSOP8 package information

TSSOP8 is an 8-lead thin shrink small outline, 3 x 6.4 mm, 0.65 mm pitch, package.

Figure 17. TSSOP8 – Outline



1. Drawing is not to scale.

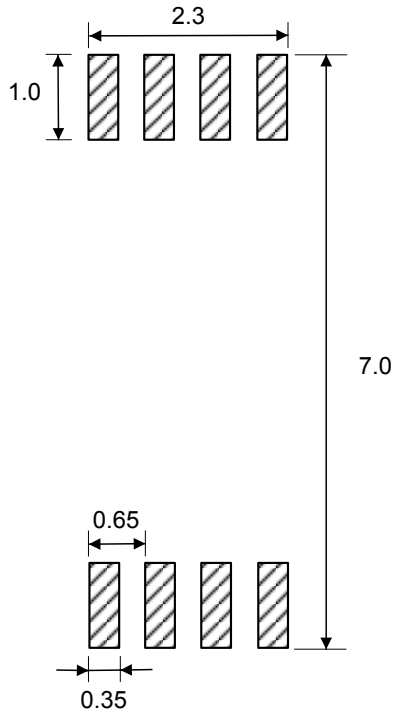
Table 19. TSSOP8 – Mechanical data

Symbol	millimeters			inches [1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.200	-	-	0.0472
A1	0.050	-	0.150	0.0020	-	0.0059
A2	0.800	1.000	1.050	0.0315	0.0394	0.0413
b	0.190	-	0.300	0.0075	-	0.0118
c	0.090	-	0.200	0.0035	-	0.0079
CP	-	-	0.100	-	-	0.0039
D	2.900	3.000	3.100	0.1142	0.1181	0.1220
e	-	0.650	-	-	0.0256	-
E	6.200	6.400	6.600	0.2441	0.2520	0.2598
E1	4.300	4.400	4.500	0.1693	0.1732	0.1772
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
α	0°	-	8°	0°	-	8°

1. *Values in inches are converted from mm and rounded to four decimal digits.*

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Figure 18. **TSSOP8 – Recommended footprint**



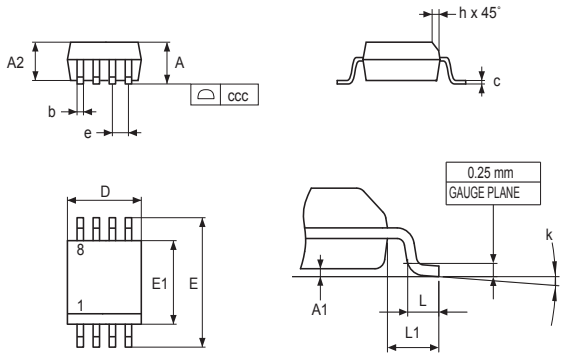
1. Dimensions are expressed in millimeters.

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9.4 SO8N package information

SO8N is an 8-lead, 4.9 x 6 mm, plastic small outline, 150 mils body width, package.

Figure 19. SO8N – Outline



1. Drawing is not to scale.

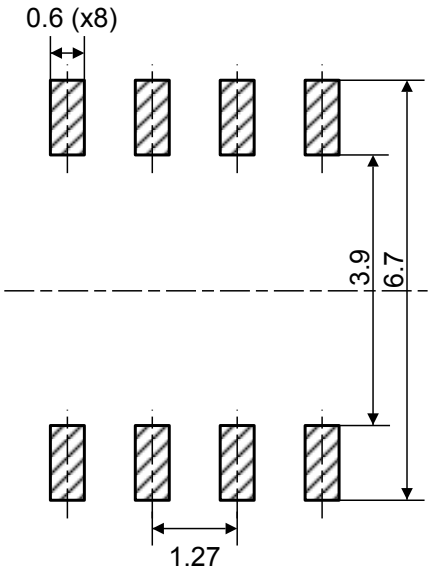
Table 20. SO8N – Mechanical data

Symbol	millimeters			inches [1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.750	-	-	0.0689
A1	0.100	-	0.250	0.0039	-	0.0098
A2	1.250	-	-	0.0492	-	-
b	0.280	-	0.480	0.0110	-	0.0189
c	0.170	-	0.230	0.0067	-	0.0091
D	4.800	4.900	5.000	0.1890	0.1929	0.1969
E	5.800	6.000	6.200	0.2283	0.2362	0.2441
E1	3.800	3.900	4.000	0.1496	0.1535	0.1575
e	-	1.270	-	-	0.0500	-
h	0.250	-	0.500	0.0098	-	0.0197
k	0°	-	8°	0°	-	8°
L	0.400	-	1.270	0.0157	-	0.0500
L1	-	1.040	-	-	0.0409	-
ccc	-	-	0.100	-	-	0.0039

1. *Values in inches are converted from mm and rounded to four decimal digits.*

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Figure 20. **SO8N - Recommended footprint**



1. Dimensions are expressed in millimeters.

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10 Ordering information

Table 21. Ordering information scheme

Example: M24 C16- W MC 6 T P /12

Device type

M24 = I^2C serial access EEPROM

Device function

C16- = 16 Kbit (2 K x 8 bit)

Operating voltage

W = V_{CC} = 2.5 V to 5.5 V

F = V_{CC} = 1.6 V or 1.7 V to 5.5 V

R = V_{CC} = 1.8 V to 5.5 V

Package (1)

MN = SO8 (150 mil width)

DW = TSSOP8 (169 mil width)

MC = UFDFPN8 (DFN8)

MH = UFDFPN5 (DFN5)

Device grade

5 = Consumer: device tested with standard test flow over –20 to 85 °C
6 = Industrial: device tested with standard test flow over -40 to 85 °C

Option

T = Tape and reel packing

blank = Tube packing

Planting technology

P or G = ECOPACK

Option

/12 = Packing 12 mm tape

1. *ECOPACK2 (RoHS compliant and free of brominated, chlorinated and antimony oxide flame retardants).*

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Table 22. Ordering information scheme (unsawn wafer)

Example:	M24	C16 -	F	T	W	20	I	/90
Device type[1]								
M24 = I^2C serial access EEPROM								
Device function								
C16 = 16 Kbit (2 K x 8 bit)								
Operating voltage								
F = V_{CC} = 1.7 V to 5.5 V								
Process								
T = F8H								
Delivery form								
W =Unsawn wafer								
Wafer thickness								
20 = Non-backlapped wafer								
22 = 180 µm backlapped wafer								
Wafer testing								
I = Inkless test								
Device grade								
90 = -40 °C to 85 °C								

1. *For all information concerning the M24C16 delivered in unsawn wafer contact your nearest ST Sales Office.*

Note: Parts marked as "ES" or "E" are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

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Revision history

Table 23. **Document revision history**

Date	Revision	Changes
05-Oct-2012	1	Initial release resulting from splitting datasheet M24C16 revision 17 as follows: • M24C16-125 datasheet for automotive products (range 3) • M24C16-W M24C16-R M24C16-F (this datasheet) for standard products range Updated in Section 8: DC and AC parameters: • ESD value in Table 15: Operating conditions (voltage range W) • Extended temperature range in Table 14: Operating conditions (voltage range F) • ICC Standby in Table 32: DC characteristics (M24128-BWvoltage range W, device grade 6) Added dimensions in Table 22: M24C16-FCS5TP/S WLCSP 5 bumps package data and Figure 18: M24C16-FCS5TP/S WLCSP 5 bumps package outline.
19-Mar-2013	2	Reformatted document. Added UFDFPN5 package. Rephrased text in Section 6: Initial delivery state. Renamed Figure 52 and Table 43. Modified note 1 under Table 24.
10-Jul-2013	3	Updated: • Features: cycling performance and data retention • Table 31: Memory cell data retention • Note (2) under Table 14: Absolute maximum ratings. Added Table 20: Cycling performance
09-Oct-2013	4	Replaced “WLCSP” by “M24C16-FCS5TP/S WLCSP” across the document. Added: Table 17: Operating conditions (voltage range F, for devices identified by process letter T) and Table 18: Operating conditions (voltage range F, for all other devices). Updated: • “Single supply voltage” in cover page. • Section 1: Description • Table 33: DC characteristics (voltage range M24128M24128-BR, M24128-DR device grade 6) and Table 35: DC characteristics (M24C32M24C02-F, device grade 6 and grade 5) • Figure 43: AC measurement I/O waveform (third waveform) • Table 70: Ordering information scheme: added note 1 for WLCSP package.
15-Sep-2014	5	Added reference to unsawn wafer availability on: • Cover page, Section 9 • Table 90 • note 2 on Table 31 • Updated Figure 4. Removed figure 5 and table 9 related to revision 4. Updated: • note 1 on Table 29 and Table 31 • I_{LI} parameter on Table 32, Table 33 and Table 35 • Table 24

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Date	Revision	Changes
18-Feb-2015	6	Removed: WLCSP package reference, tables and figures in all document Updated: Table 54 and Table 70
01-Jul-2015	7	Updated: Section 6, Table 70 Added note 1 on Table 70
18-Mar-2016	8	Updated Features, Figure 41: Read mode sequences, Figure 51: UFDFPN5 – 1.7x1.4 mm, 0.55 mm thickness, ultra thin fine pitch dual flat package, no lead - package outline and Table 53: UFDFPN5 - 1.7 × 1.4 mm, 0.55 mm thickness, ultra thin fine pitch dual flat package, no lead - package mechanical data
02-Oct-2017	9	Added reference to DFN8 and DFN5 in: • cover page figure, Figure 3: UFDFPN5 (DFN5) package connections • Section 9.1: UFDFPN5 (DFN5) package information, Section 9.2: UFDFPN8 (DFN8) package information. Updated Table 9: AC measurement conditions, Table 23: Ordering information scheme. Added Figure 14: UFDFPN5 - 5-lead, 1.7 × 1.4 mm, 0.55 mm thickness, ultra thin fine pitch dual flat package, no lead recommended footprint
04-Jun-2020	10	Updated: • Section Features • Figure 4. Block diagram • Table 4. Absolute maximum ratings, • title of Table 7. Operating conditions (voltage range F) • notes in: Table 10. Cycling performance, Table 11. Memory cell data retention, Table 12. DC characteristics (M24C16-W, device grade 6)Table 13. DC characteristics (M24C16-R device grade 6), Table 14. DC characteristics (M24C16-F device grade 6) Removed Package PDIP8 in whole document, Table 8. Operating conditions (voltage range F, for all other devices) Added specification in Wafer thickness feature of Table 22. Ordering information scheme (unsawn wafer)
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