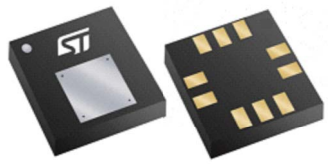
LPS25HB

MEMS pressure sensor: 260-1260 hPa absolute digital output barometer

Datasheet - production data



HLGA-10L
(2.5 x 2.5 x 0.76 mm typ.)

Features

- 260 to 1260 hPa absolute pressure range
- High-resolution mode: 0.01 hPa RMS
- Low power consumption
  - Low-resolution mode: 4 µA
  - Low current & noise mode with FIFO: 4.5 µA
- High overpressure capability: 20x full scale
- Embedded temperature compensation
- 24-bit pressure data output
- ODR from 1 Hz to 25 Hz
- SPI and I^2C interfaces
- Embedded FIFO
- Interrupt functions: Data Ready, FIFO flags, pressure thresholds
- Supply voltage: 1.7 to 3.6 V
- High shock survivability: 10,000 *g*
- ECOPACK® lead-free compliant

Applications

- Altimeter and barometer for portable devices
- Enhanced GPS applications
- Weather station equipment
- Wearable devices

Description

The LPS25HB is a piezoresistive absolute pressure sensor which functions as a digital output barometer. The device comprises a sensing element and an IC interface which communicates through I^2C or SPI from the sensing element to the application.

The sensing element, which detects absolute pressure, consists of a suspended membrane manufactured using a dedicated process developed by ST.

The LPS25HB is available in a full-mold, holed LGA package (HLGA). It is guaranteed to operate over a temperature range extending from -30 to +105 °C. The package is holed to allow external pressure to reach the sensing element.

Table 1. Device summary

Order code	Temperature range [°C]	Package	Packing
LPS25HBTR	-30 to +105 °C	HLGA-10L	Tape and reel

This is information on a product in full production. www.st.com

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1 Block diagram and pin description

Figure 1. Block diagram

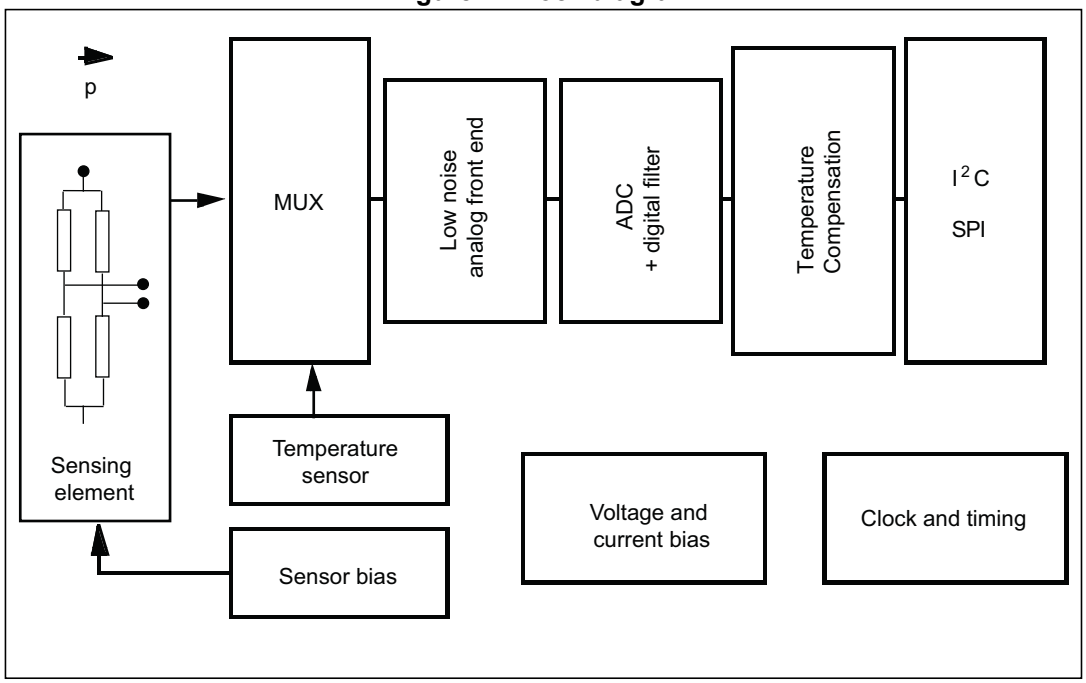
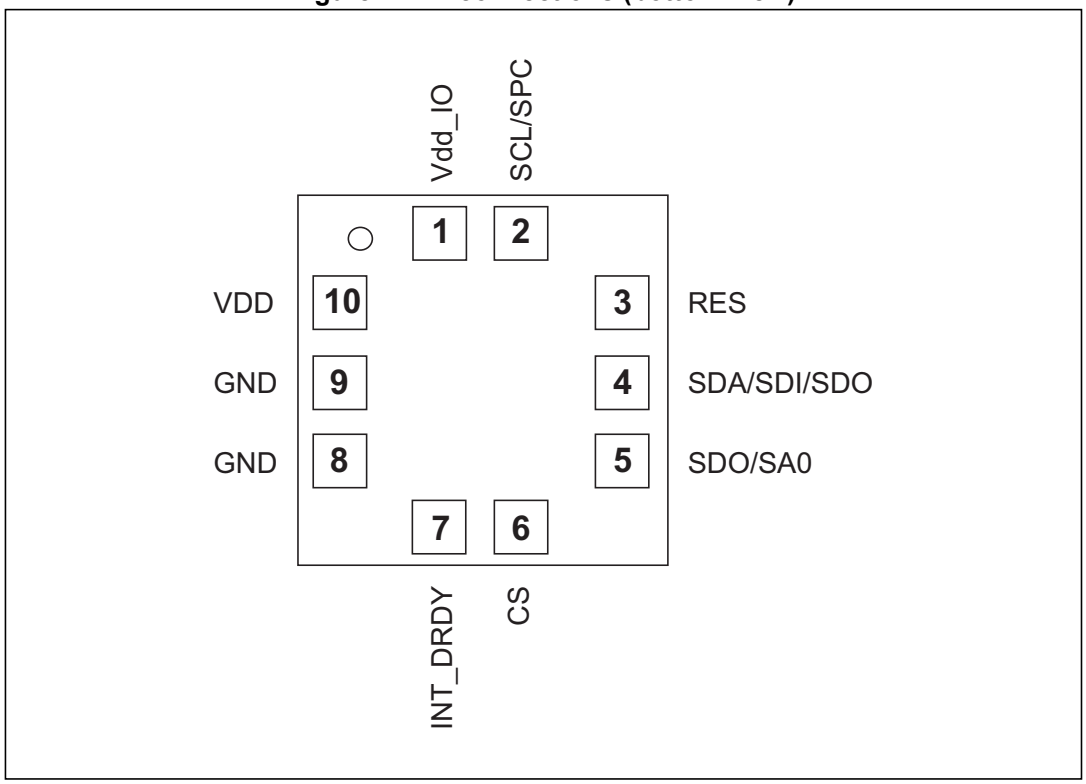


Figure 2. Pin connections (bottom view)



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Table 2. Pin description

Pin number	Name	Function
1	Vdd_IO	Power supply for I/O pins
2	SCL SPC	I²C serial clock (SCL) SPI serial port clock (SPC)
3	Reserved	Connect to GND
4	SDA SDI SDI/SDO	I²C serial data (SDA) 4-wire SPI serial data input (SDI) 3-wire serial data input /output (SDI/SDO)
5	SDO SA0	4-wire SPI serial data output (SDO) I²C less significant bit of the device address (SA0)
6	CS	SPI enable I²C/SPI mode selection (1: SPI idle mode / I^2C communication enabled; 0: SPI communication mode / I^2C disabled)
7	INT_DRDY	Interrupt or Data Ready
8	GND	0 V supply
9	GND	0 V supply
10	VDD	Power supply

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2 Mechanical and electrical specifications

2.1 Mechanical characteristics

VDD = 1.8 V, T = 25 °C, unless otherwise noted.

Table 3. Pressure and temperature sensor characteristics

Symbol	Parameter	Test condition	Min.	Typ.(1)	Max.	Unit
Pressure sensor characteristics						
PT_{op}	Operating temperature range		-30		+105	°C
PT_{full}	Full accuracy temperature range		0		+80	°C
P_{op}	Operating pressure range		260		1260	hPa
P_{bits}	Pressure output data			24		bits
P_{sens}	Pressure sensitivity			4096		LSB/ hPa
P_{accrel}	Relative accuracy over pressure(2)	P = 800 to 1100 hPa T = 25°C		± 0.1		hPa
P_{accT}	Absolute accuracy pressure over temperature(3)	P = 260 to 1260 hPa T = 20 ~ +60 °C after OPC(4)		± 0.2		hPa
		P = 260 to 1260 hPa T = 0 ~ +80 °C before OPC(4)		± 1		
P_{noise}	Pressure noise(5)	without embedded filtering		0.03		hPa RMS
		with embedded filtering		0.01		
ODR_{Pres}	Pressure output data rate			1 7 12.5 25		Hz
Temperature sensor characteristics						
T_{op}	Operating temperature range		-30		105	°C
T_{bits}	Temperature output data			16		bits
T_{sens}	Temperature sensitivity			480		LSB/°C
Tacc	Absolute accuracy temperature	T= 0 ~ +65 °C		± 2		°C
ORD_T	Temperature output data rate			1 7 12.5 25		Hz

1. Typical specifications are not guaranteed.

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2. Characterization data. Parameter not tested at final test.
3. Embedded quadratic compensation.
4. OPC: One Point Calibration in the application.
5. Pressure noise RMS evaluated in a controlled environment based on the average standard deviation of 32 measurements at highest ODR.

2.2 Electrical characteristics

VDD = 1.8 V, T = 25 °C, unless otherwise noted.

Table 4. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.(1)	Max.	Unit
VDD	Supply voltage		1.7		3.6	V
Vdd_IO	IO supply voltage		1.7		VDD + 0.1	V
Idd	Supply current	@ ODR 1 Hz, Low-resolution mode: RES_CONF (10h) = 04h		4		µA
		@ ODR 1 Hz, Low current & noise mode with FIFO: *RES_CONF (10h)* = 05h, *FIFO_CTRL (2Eh)* = DFh, *CTRL_REG2 (21h)* = 50h		4.5		µA
		@ ODR 1 Hz, High-resolution mode: RES_CONF (10h) = 0Fh		25		µA
IddPdn	Supply current in power-down mode			0.5		µA

1. Typical specifications are not guaranteed.

Table 5. DC characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
DC input characteristics						
Vil	Low-level input voltage (Schmitt buffer)				0.2 * Vdd_IO	V
Vih	High-level input voltage (Schmitt buffer)		0.8 * Vdd_IO			V
DC output characteristics						
Vol	Low-level output voltage		0.2			V
Voh	High-level output voltage				Vdd_IO - 0.2	V

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2.3 Communication interface characteristics

2.3.1 SPI - serial peripheral interface

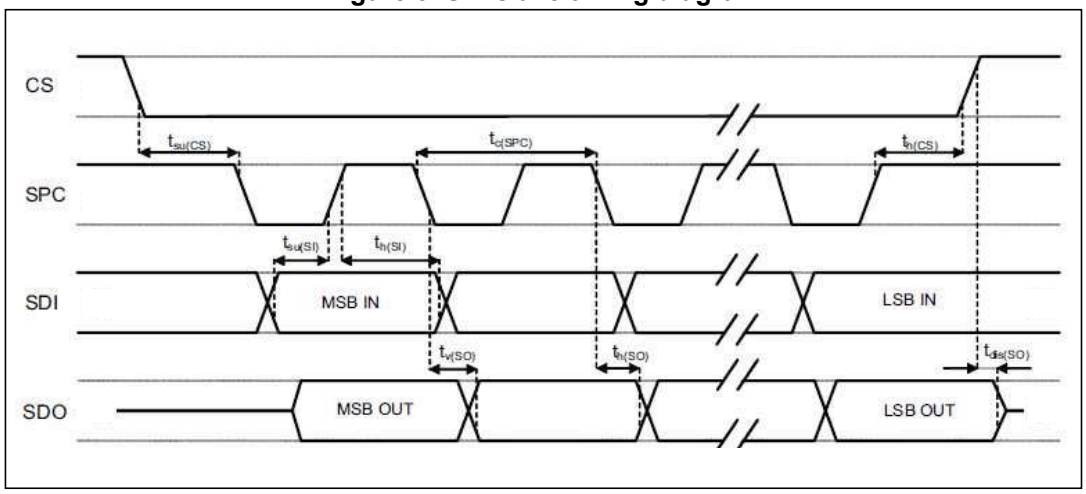
Subject to general operating conditions for Vdd and T_{OP}.

Table 6. SPI slave timing values

Symbol	Parameter	Value(1)		Unit
		Min	Max	
$t_{c(SPC)}$	SPI clock cycle	100		ns
$f_{c(SPC)}$	SPI clock frequency		10	MHz
$t_{su(CS)}$	CS setup time	6		ns
$t_{h(CS)}$	CS hold time	8		
$t_{su(SI)}$	SDI input setup time	5		
$t_{h(SI)}$	SDI input hold time	15		
$t_{v(SO)}$	SDO valid output time		50	
$t_{h(SO)}$	SDO output hold time	9		
$t_{dis(SO)}$	SDO output disable time		50	

1. Values are guaranteed at 10 MHz clock frequency for SPI with both 4 and 3 wires, based on characterization results, not tested in production.

Figure 3. SPI slave timing diagram



Note: Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both ports.

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2.3.2 I²C - inter-IC control interface

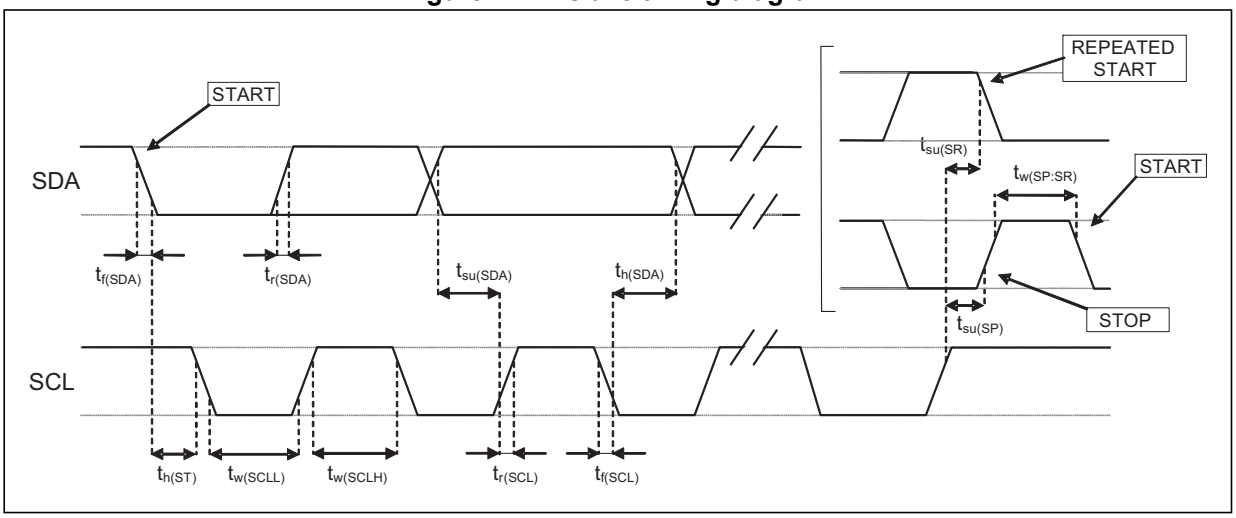
Subject to general operating conditions for Vdd and T_{OP}.

Table 7. I²C slave timing values

Symbol	Parameter (1)	I²C standard		I²C fast mode(1)		Unit
		Min	Max	Min	Max	
$f_{(SCL)}$	SCL clock frequency	0	100	0	400	kHz
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		µs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0.01	3.45	0	0.9	µs
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time		1000	20	300	ns
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time		300	20x(VDD/5.5)	300	
$t_{h(ST)}$	START condition hold time	4		0.6		µs
$t_{su(SR)}$	Repeated START condition setup time	4.7		0.6		
$t_{su(SP)}$	STOP condition setup time	4		0.6		
$t_{w(SP:SR)}$	Bus free time between STOP and START condition	4.7		1.3		

1. Data based on standard I²C protocol requirement, not tested in production.

Figure 4. I²C slave timing diagram



Note: Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both ports.

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2.4 Absolute maximum ratings

Stress above those listed as “Absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 8. Absolute maximum ratings

Symbol	Ratings	Maximum value	Unit
VDD	Supply voltage	-0.3 to 4.8	V
Vdd_IO	I/O pins supply voltage	-0.3 to 4.8	V
Vin	Input voltage on any control pin	-0.3 to Vdd_IO +0.3	V
P	Overpressure	2	MPa
T_{STG}	Storage temperature range	-40 to +125	°C
ESD	Electrostatic discharge protection	2 (HBM)	kV

Note: Supply voltage on any pin should never exceed 4.8 V.



This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part.



This device is sensitive to electrostatic discharge (ESD), improper handling can cause permanent damage to the part.

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3 Functionality

The LPS25HB is a high resolution, digital output pressure sensor packaged in an HLGA full-mold package. The complete device includes a sensing element based on a piezoresistive Wheatstone bridge approach, and an IC interface which communicates a digital signal from the sensing element to the application.

3.1 Sensing element

An ST proprietary process is used to obtain a silicon membrane for MEMS pressure sensors. When pressure is applied, the membrane deflection induces an imbalance in the Wheatstone bridge piezoresistances whose output signal is converted by the IC interface.

3.2 I^2C interface

The complete measurement chain is composed of a low-noise amplifier which converts the resistance unbalance of the MEMS sensors (pressure and temperature) into an analog voltage using an analog-to-digital converter.

The pressure and temperature data may be accessed through an I²C/SPI interface thus making the device particularly suitable for direct interfacing with a microcontroller.

The LPS25HB features a Data-Ready signal which indicates when a new set of measured pressure and temperature data are available, thus simplifying data synchronization in the digital system that uses the device.

3.3 Factory calibration

The IC interface is factory calibrated at three temperatures and two pressures for sensitivity and accuracy.

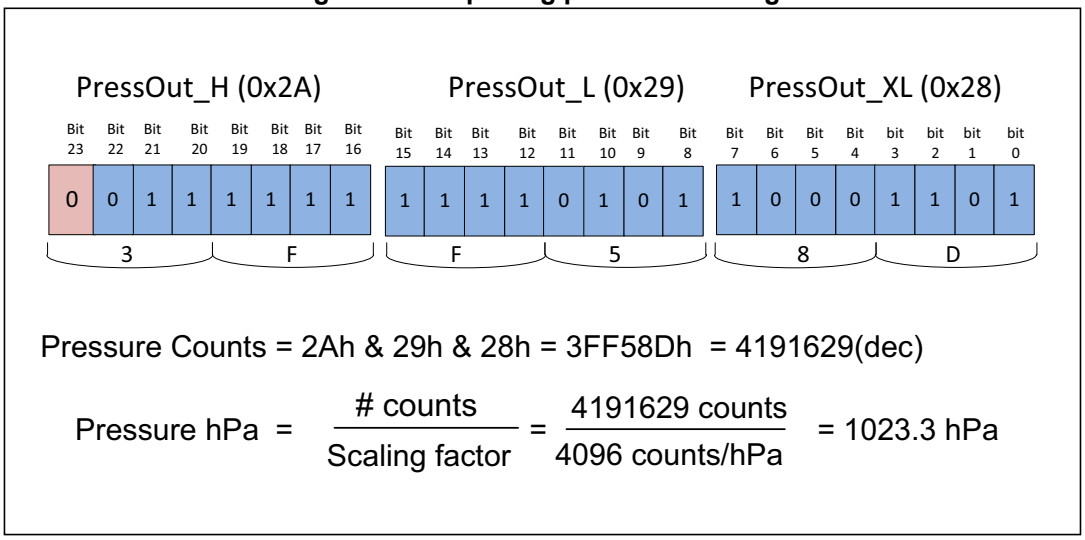
The trimming values are stored inside the device in a non-volatile structure. When the device is turned on, the trimming parameters are downloaded into the registers to be employed during normal operation which allows the device to be used without requiring any further calibration.

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3.4 How to interpret pressure readings

The pressure data are stored in 3 registers: *PRESS_OUT_H (2Ah)*, *PRESS_OUT_L (29h)* and *PRESS_OUT_XL (28h)*. The value is expressed as 2's complement. To obtain the pressure in hPa, take the two's complement of the complete word and then divide by 4096 hPa.

Figure 5. Interpreting pressure readings



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4 FIFO

The LPS25HB embeds 32-slot data FIFO to store the pressure output values. The FIFO allows consistent power saving for the system, since the host processor does not need to continuously poll data from the sensor, but it can wake up only when needed and burst the significant data out from the FIFO.

This buffer can work according to seven different modes: Bypass mode, FIFO mode, Stream mode, Stream-to-FIFO mode, Bypass-to-Stream mode, Bypass-to-FIFO mode and FIFO Mean mode.

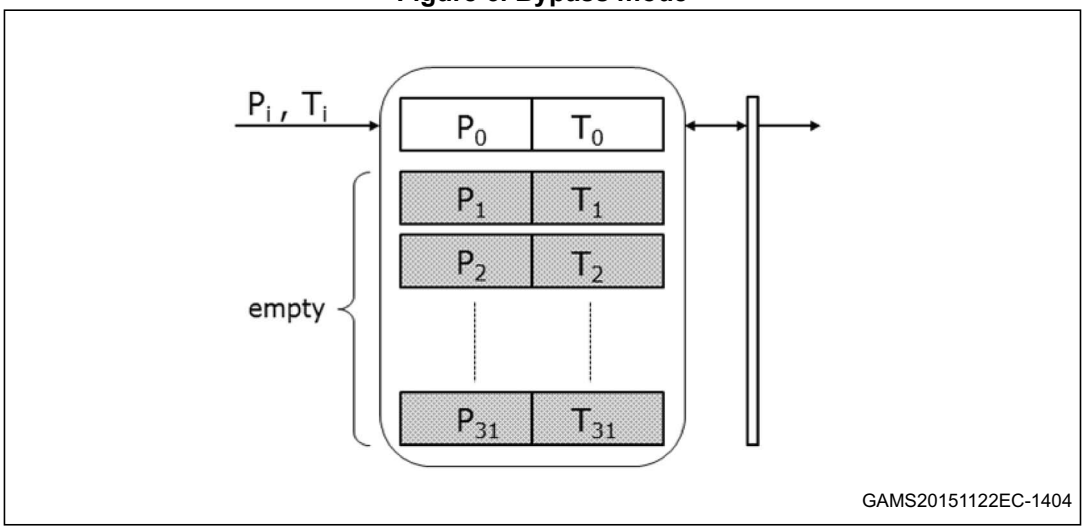
The FIFO buffer is enabled when the FIFO_EN bit in *CTRL_REG2 (21h)* is set to '1' and each mode is selected by the F_MODE[2:0] bits in *FIFO_CTRL (2Eh)*.

FIFO threshold status, FIFO overrun events and the number of unread samples stored are available in the *FIFO_STATUS (2Fh)* register and can be set to generate dedicated interrupts on the INT_DRDY pin in the *CTRL_REG4 (23h)* register.

4.1 Bypass mode

In Bypass mode (F_MODE[2:0] in *FIFO_CTRL (2Eh)* set to '000'), the FIFO is not operational and it remains empty.

Figure 6. Bypass mode



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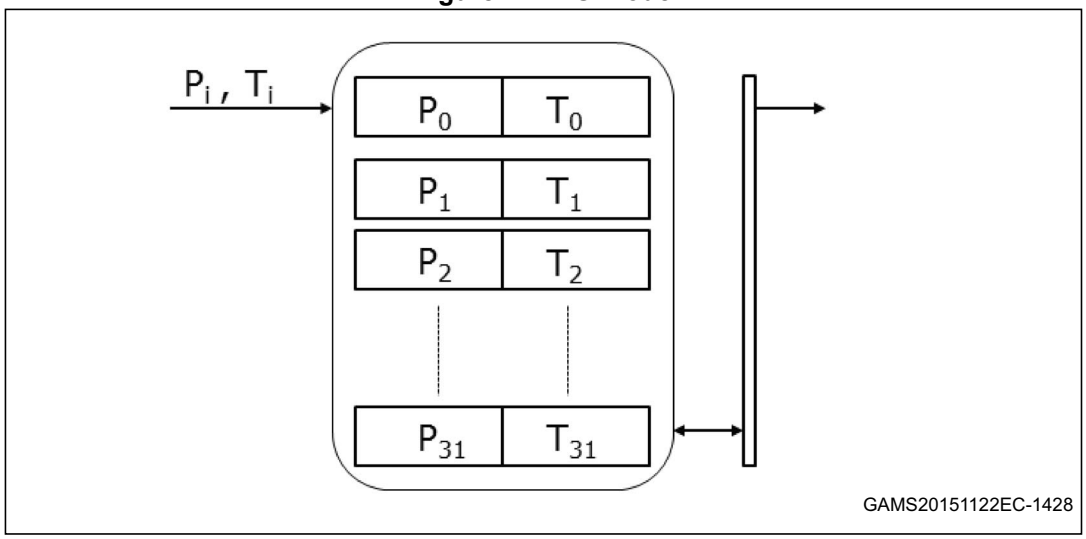
4.2 FIFO mode

In FIFO mode (F_MODE[2:0] in *FIFO_CTRL (2Eh)* set to '001'), the data from *PRESS_OUT_H (2Ah)*, *PRESS_OUT_L (29h)*, and *PRESS_OUT_XL (28h)* are stored in the FIFO.

A watermark interrupt can be enabled (STOP_ON_FTH bit set to '1' in *CTRL_REG2 (21h)*) in order to be raised when the FIFO is filled to the level specified by the WTM_POINT[4:0] bits of *FIFO_CTRL (2Eh)*. The FIFO continues filling until it is full (32 slots of data for pressure output). When full, the FIFO stops collecting data.

The FIFO buffer can store up to 32 levels of data. The FIFO depth can be limited by setting the STOP_ON_FTH bit 5 in *CTRL_REG2 (21h)* to ‘1’ and by selecting a watermark level with the WTM_POINT[4:0] bits in *FIFO_CTRL (2Eh)*.

Figure 7. FIFO mode

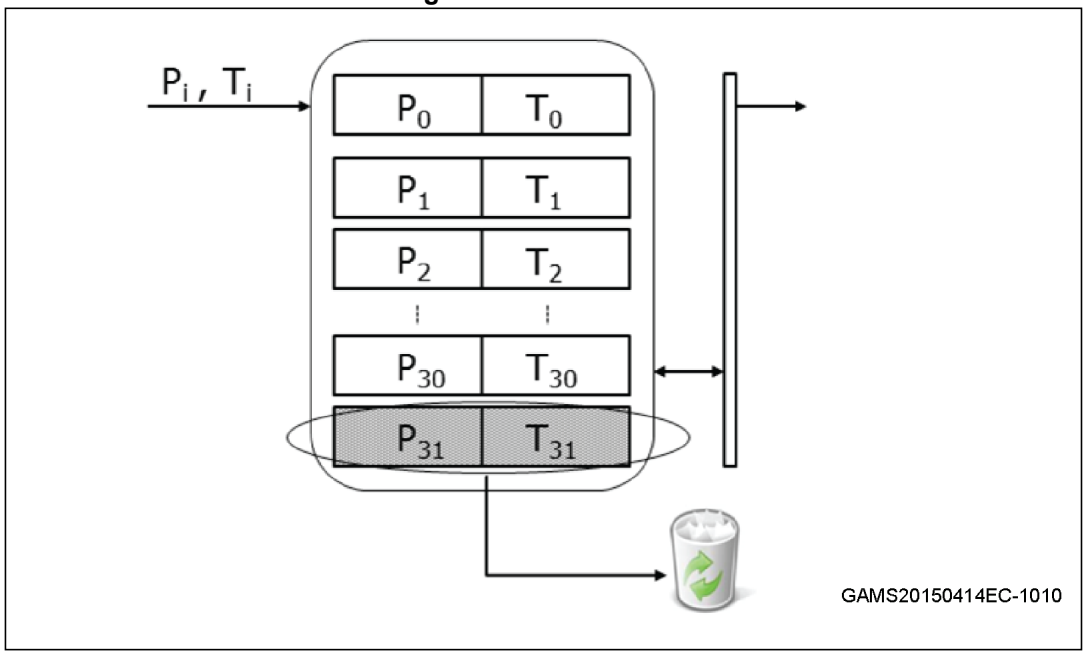


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4.3 Stream mode

In Stream mode (F_MODE[2:0] in *FIFO_CTRL (2Eh)* set to '010'), the data from *PRESS_OUT_H (2Ah)*, *PRESS_OUT_L (29h)*, and *PRESS_OUT_XL (28h)* are stored in the FIFO. The FIFO continues filling until it's full (32 slots of data for pressure output). When full, the FIFO discards the older data as the new arrive. An interrupt can be enabled and set as in FIFO mode.

Figure 8. Stream mode



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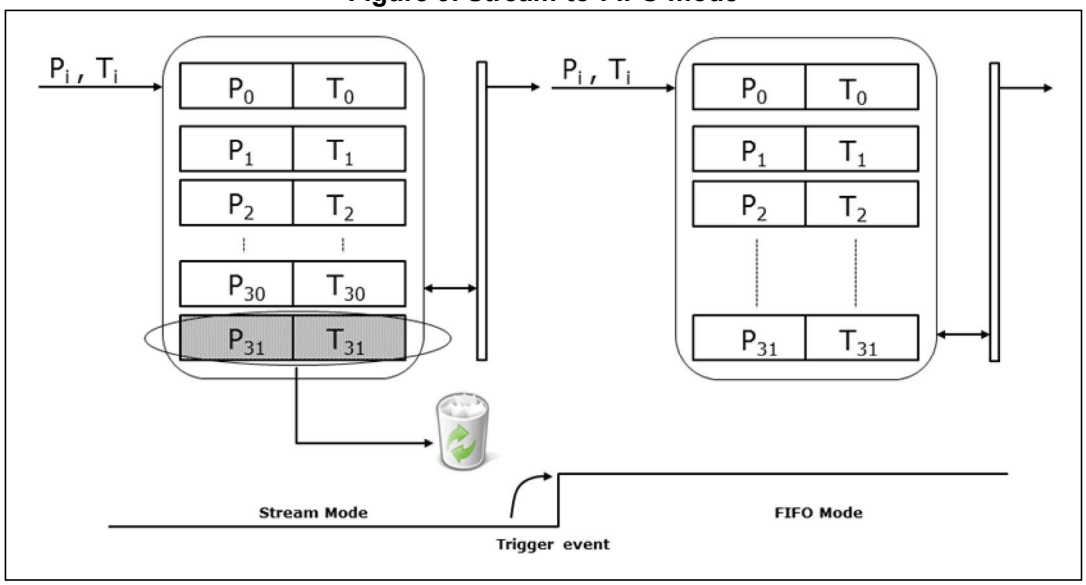
4.4 Stream-to-FIFO mode

In Stream-to-FIFO mode (F_MODE[2:0] in *FIFO_CTRL (2Eh)* set to '011'), the data from *PRESS_OUT_H (2Ah)*, *PRESS_OUT_L (29h)* PRESS_OUT_L (29h) and PRESS_OUT_XL (28h) are stored in the FIFO.

An interrupt can be enabled (STOP_ON_FTH bit set to '1' in *CTRL_REG2 (21h)*) in order to be raised when the FIFO is filled to the level specified by the WTM_POINT[4:0] bits of *FIFO_CTRL (2Eh)*.The FIFO continues filling until it's full (32 slots of data for pressure output). When full, the FIFO discards the older data as the new arrive. Once a trigger event occurs, the FIFO starts operating in FIFO mode. A trigger event can be configured in *INTERRUPT_CFG (24h)*.

The LIR bit in *INTERRUPT_CFG (24h)* should be set to '1' in order to have latched interrupt for triggering and reading the data in FIFO mode.

Figure 9. Stream-to-FIFO mode

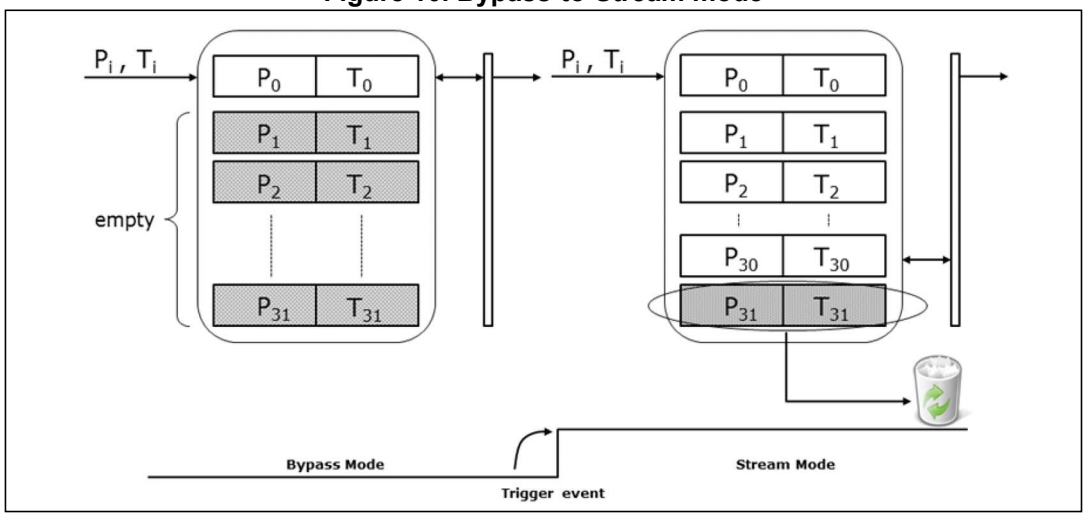


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4.5 Bypass-to-Stream mode

In Bypass-to-Stream mode (F_MODE[2:0] in *FIFO_CTRL (2Eh)* set to '100'), the FIFO is in Bypass mode until a trigger event occurs which is based on the IA bit in *INT_SOURCE (25h)* and the FIFO starts operating in Stream mode. A trigger event can be configured in *INTERRUPT_CFG (24h)*.

Figure 10. Bypass-to-Stream mode



4.6 FIFO Mean mode

In FIFO Mean mode (F_MODE[2:0] in *FIFO_CTRL (2Eh)* set to '110'), the pressure data are not directly sent to the output register but are first stored in the FIFO to calculate the average. In this mode the FIFO is used to implement a moving average of the pressure data with a 2, 4, 8, 16 or 32 sample set by changing the FIFO Mean mode sample size defined by the WTM_POINT[4:0] bits of *FIFO_CTRL (2Eh)* (refer to *Table 9*).

Table 9. Running average sample size

WTM_POINT[4:0]	FIFO Mean mode sample size
00001	2-sample moving average
00011	4-sample moving average
00111	8-sample moving average
01111	16-sample moving average
11111	32-sample moving average

There are two possible ways of providing the output pressure data averaged by FIFO:

1. If the FIFO_MEAN_DEC bit in *CTRL_REG2 (21h)* is set to '0', the output is at the same ODR of the data coming from the sensor;
2. If the FIFO_MEAN_DEC bit in *CTRL_REG2 (21h)* is set to '1', the output is decimated (@1 Hz when ODR = 4 or 2; @1.04 Hz when ODR=3).

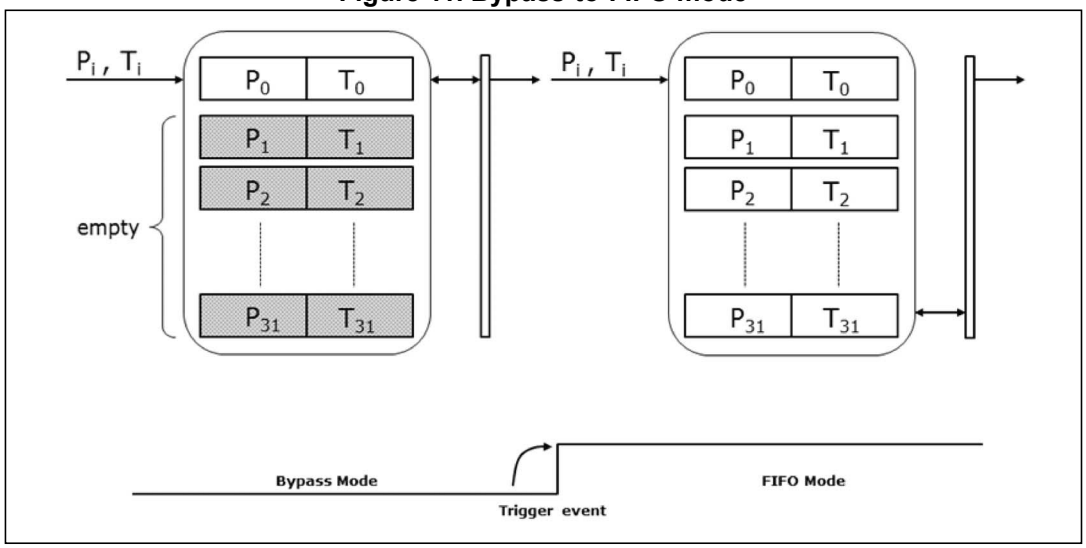
Please note that when using the FIFO Mean mode it is not possible to access the FIFO content.

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4.7 Bypass-to-FIFO mode

In Bypass-to-FIFO (F_MODE[2:0] in *FIFO_CTRL (2Eh)* set to '111'), the FIFO is in Bypass mode until a trigger event occurs and the FIFO starts operating in FIFO mode. A trigger event is based on the IA bit in *INT_SOURCE (25h)* and it is configured by *INTERRUPT_CFG (24h)*.

Figure 11. Bypass-to-FIFO mode



4.8 Retrieving data from FIFO

When the FIFO is enabled, FIFO data are read from *PRESS_OUT_H (2Ah)*, *PRESS_OUT_L (29h)*, and *PRESS_OUT_XL (28h)* registers.

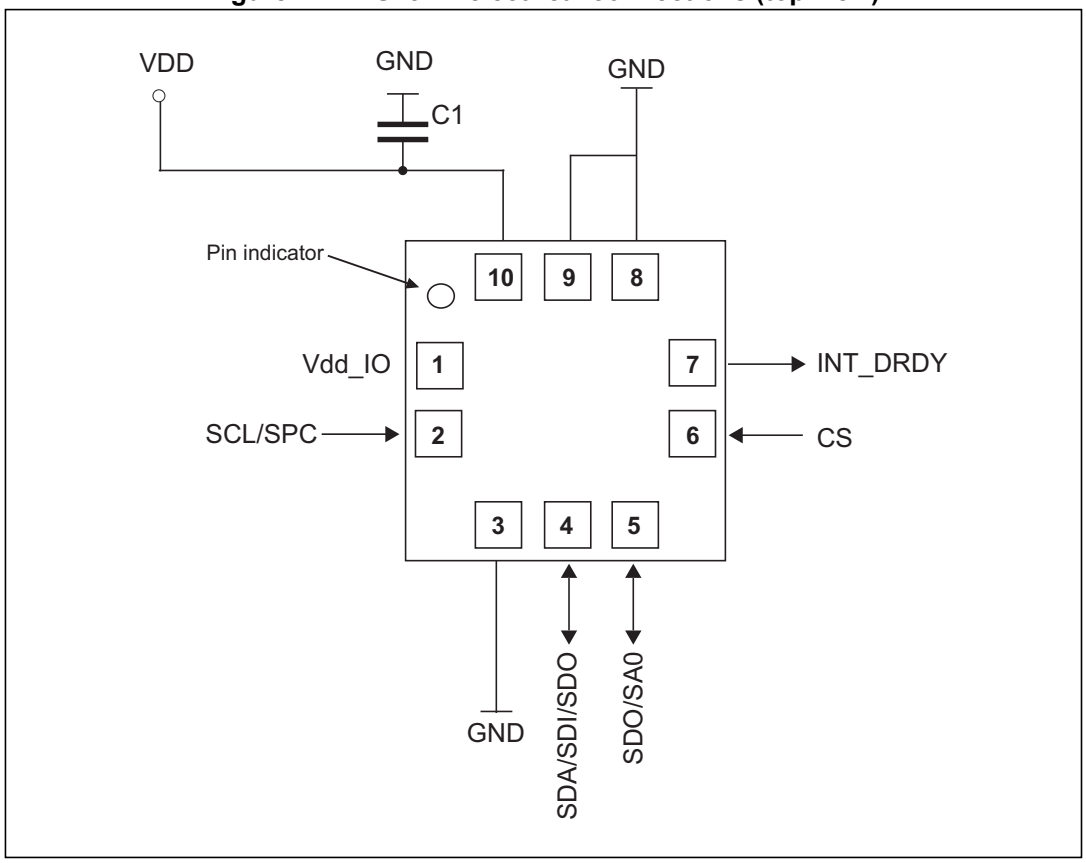
Each time data is read from the FIFO, the oldest data are placed in the *PRESS_OUT_H (2Ah)*, *PRESS_OUT_L (29h)* and *PRESS_OUT_XL (28h)* registers and both single-read and read-burst operations can be used.

The reading address is automatically updated by the device and it rolls back to 28h when register 2Ah is reached. In order to read all FIFO levels in a multiple byte reading, 96 bytes (3 output registers by 32 levels) must be read.

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5 Application hints

Figure 12. LPS25HB electrical connections (top view)



The device power supply must be provided through the VDD line; the power supply decoupling capacitor C1 (100 nF) must be placed as near as possible to the supply pads of the device. Depending on the application, an additional capacitor of 4.7 µF could be placed on VDD line.

The functionality of the device and the measured data outputs are selectable and accessible through the I²C/SPI interface. When using the I²C, CS must be tied to Vdd_IO.

All the voltage and ground supplies must be present at the same time to have proper behavior of the IC (refer to *Figure 12.*). It is possible to remove VDD while maintaining Vdd_IO without blocking the communication bus, in this condition the measurement chain is powered off.

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5.1 Soldering information

The HLGA package is compliant with the ECOPACK® standard and it is qualified for soldering heat resistance according to JEDEC J-STD-020.

The HLGA package is compliant with the ECOPACK®, RoHS and "Green" standard. It is qualified for soldering heat resistance according to JEDEC J-STD-020. Leave "Pin 1 Indicator" unconnected during soldering.

Please refer the technical note TN1198, “Surface mount guidelines for MEMS sensors in HLGA packages” available on *www.st.com* for any additional information

Land pattern and soldering recommendations are available at *www.st.com/mems*.

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6 Digital interfaces

6.1 I²C serial interface

The registers embedded in the LPS25HB may be accessed through both the I²C and SPI serial interfaces. The latter may be SW configured to operate either in 3-wire or 4-wire interface mode.

The serial interfaces are mapped onto the same pads. To select/exploit the I²C interface, the CS line must be tied high (i.e. connected to Vdd_IO); to select the SPI interface, the CS line must be tied low (i.e. connected to GND).

Table 10. Serial interface pin description

Pin name	Pin
CS	SPI enable I²C/SPI mode selection (1: I²C mode; 0: SPI enabled
SCL/SPC	I²C serial clock (SCL) SPI serial port clock (SPC)
SDA SDI SDI/SDO	I²C serial data (SDA) 4-wire SPI serial data input (SDI) 3-wire serial data input /output (SDI/SDO)
SDO SAO	SPI serial data output (SDO) I²C less significant bit of the device address (SA0)

6.2 I²C serial interface (CS = High)

The LPS25HB I²C is a bus slave. The I²C is employed to write data into registers whose content can also be read back.

The relevant I²C terminology is given in *Table 9*.

Table 11. I²C terminology

Term	Description
Transmitter	The device which sends data to the bus
Receiver	The device which receives data from the bus
Master	The device which initiates a transfer, generates clock signals and terminates a transfer
Slave	The device addressed by the master

There are two signals associated with the I²C bus: the serial clock line (SCL) and the serial data line (SDA). The latter is a bi-directional line used for sending and receiving the data to/from the interface. Both lines have to be connected to Vdd_IO through pull-up resistors.

The I²C interface is compliant with fast mode (400 kHz) I²C standards as well as with the normal mode.

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6.2.1 I²C operation

The transaction on the bus is started through a START (ST) signal. A start condition is defined as a HIGH-to-LOW transition on the data line while the SCL line is held HIGH. After this has been transmitted by the master, the bus is considered busy. The next data byte transmitted after the start condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the master.

The slave address (SAD) associated to the LPS25HB is 101110xb. The **SDO**/**SA0** pad can be used to modify the less significant bit of the device address. If the SA0 pad is connected to the voltage supply, LSb is ‘1’ (address 1011101b), otherwise if the SA0 pad is connected to ground, the LSb value is ‘0’ (address 1011100b). This solution permits to connect and address two different LPS25HB devices to the same I²C lines.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line LOW so that it remains stable low during the HIGH period of the acknowledge clock pulse. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data received.

The I²C embedded in the LPS25HB behaves like a slave device and the following protocol must be adhered to. After the start condition (ST) a slave address is sent, once a slave acknowledge (SAK) has been returned, an 8-bit sub-address (SUB) will be transmitted: the 7 LSB represents the actual register address while the MSB enables address auto increment. If the MSb of the SUB field is ‘1’, the SUB (register address) will be automatically increased to allow multiple data read/write.

The slave address is completed with a Read/Write bit. If the bit is ‘1’ (Read), a repeated START (SR) condition must be issued after the two sub-address bytes; if the bit is ‘0’ (Write) the master will transmit to the slave with direction unchanged. *Table 12* explains how the SAD+read/write bit pattern is composed, listing all the possible configurations.

Table 12. SAD+Read/Write patterns

Command	SAD[6:1]	SAD[0] = SA0	R/W	SAD+R/W
Read	101110	0	1	10111001 (B9h)
Write	101110	0	0	10111000 (B8h)
Read	101110	1	1	10111011 (BBh)
Write	101110	1	0	10111010 (BAh)

Table 13. Transfer when master is writing one byte to slave

Master	ST	SAD + W		SUB		DATA		SP
Slave			SAK		SAK		SAK	

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Table 14. Transfer when master is writing multiple bytes to slave

Master	ST	SAD + W		SUB		DATA		DATA		SP
Slave			SAK		SAK		SAK		SAK	

Table 15. Transfer when master is receiving (reading) one byte of data from slave

Master	ST	SAD + W		SUB		SR	SAD + R			NMAK	SP
Slave			SAK		SAK			SAK	DATA		

Table 16. Transfer when master is receiving (reading) multiple bytes of data from slave

Master	ST	SAD+W		SUB		SR	SAD+R			MAK		MAK		NMAK	SP
Slave			SAK		SAK			SAK	DATA		DATA		DATA		

Data are transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes transferred per transfer is unlimited. Data is transferred with the most significant bit (MSb) first. If a receiver can't receive another complete byte of data until it has performed some other functions, it can hold the clock line, SCL LOW to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases the data line. If a slave receiver does not acknowledge the slave address (i.e. it is not able to receive because it is performing some real-time function) the data line must be kept HIGH by the slave. The master can then abort the transfer. A LOW-to-HIGH transition on the SDA line while the SCL line is HIGH is defined as a STOP condition. Each data transfer must be terminated by the generation of a STOP (SP) condition.

In order to read multiple bytes incrementing the register address, it is necessary to assert the most significant bit of the sub-address field. In other words, SUB(7) must be equal to 1 while SUB(6-0) represents the address of the first register to be read.

In the presented communication format MAK is Master acknowledge and NMAK is no master acknowledge.

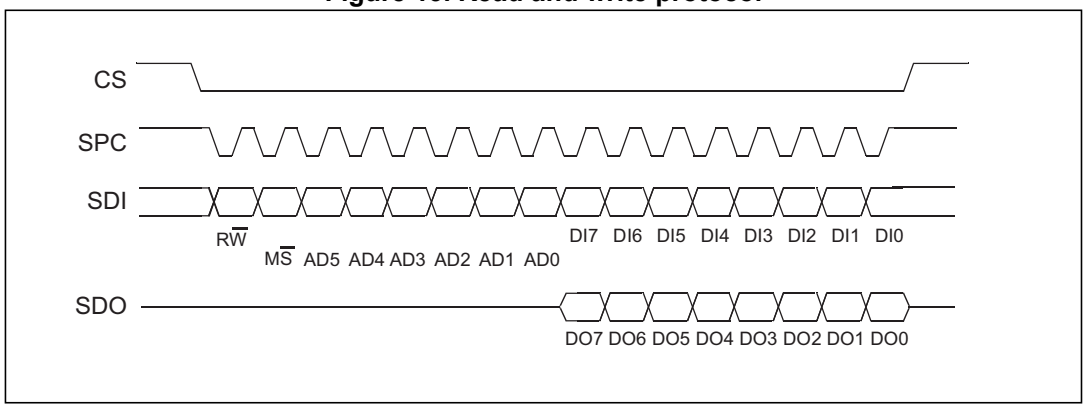
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6.3 SPI bus interface

The LPS25HB SPI is a bus slave. The SPI allows writing to and reading from the registers of the device.

The serial interface interacts with the outside world with 4 wires: **CS**, **SPC**, **SDI** and **SDO**.

Figure 13. Read and write protocol



CS is the serial port enable and it is controlled by the SPI master. It goes low at the start of the transmission and returns to high at the end. **SPC** is the serial port clock and it is controlled by the SPI master. It is stopped high when **CS** is high (no transmission). **SDI** and **SDO** are respectively the serial port data input and output. Those lines are driven at the falling edge of **SPC** and should be captured at the rising edge of **SPC**.

Both the read register and write register commands are completed in 16 clock pulses or in multiples of 8 in the case of multiple read/write bytes. Bit duration is the time between two falling edges of **SPC**. The first bit (bit 0) starts at the first falling edge of **SPC** after the falling edge of **CS** while the last bit (bit 15, bit 23,...) starts at the last falling edge of SPC just before the rising edge of **CS**.

bit 0: RW bit. When 0, the data DI(7:0) is written into the device. When 1, the data DO(7:0) from the device is read. In the latter case, the chip will drive **SDO** at the start of bit 8.

bit 1: MS bit. When 0, the address will remain unchanged in multiple read/write commands. When 1, the address will be auto incremented in multiple read/write commands.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

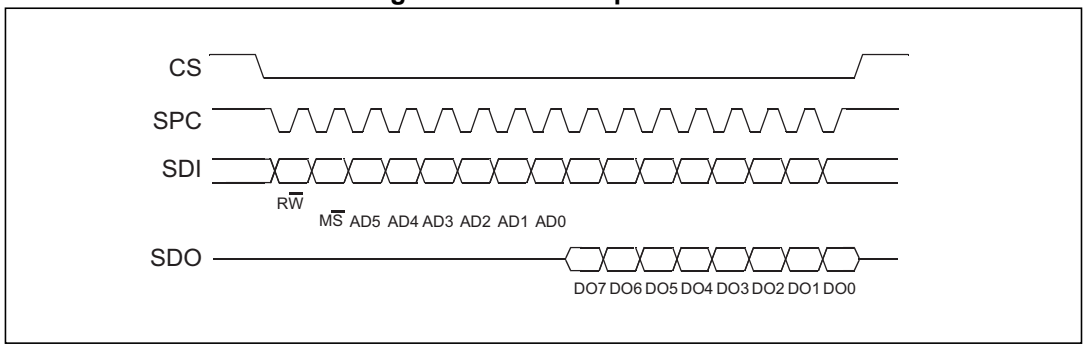
bit 8-15: data DI(7:0) (write mode). This is the data that is written into the device (MSb first).
bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).
In multiple read/write commands further blocks of 8 clock periods are added. When the MS bit is 0 the address used to read/write data remains the same for every block. When the MS bit is 1 the address used to read/write data is increased at every block.

The function and the behavior of **SDI** and **SDO** remain unchanged.

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6.3.1 SPI read

Figure 14. SPI read protocol



The SPI read command is performed with 16 clock pulses. The multiple byte read command is performed by adding blocks of 8 clock pulses to the previous one.

bit 0: READ bit. The value is 1.

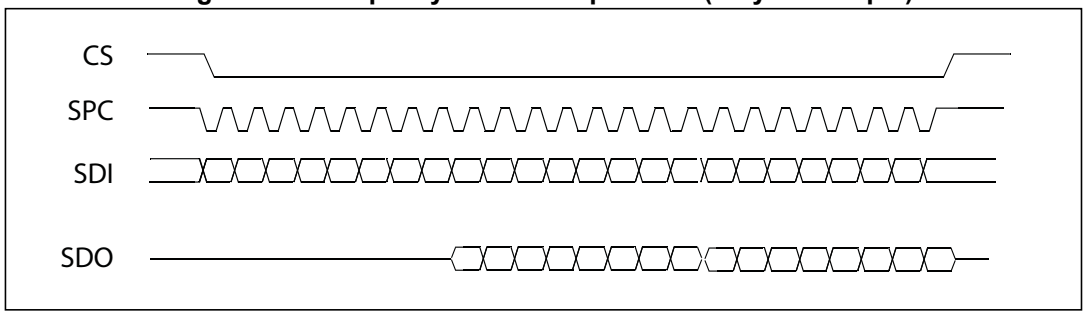
bit 1: MS bit. When 0, does not increment the address; when 1, increments the address in multiple reads.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

bit 16-...: data DO(...-8). Further data in multiple byte reads.

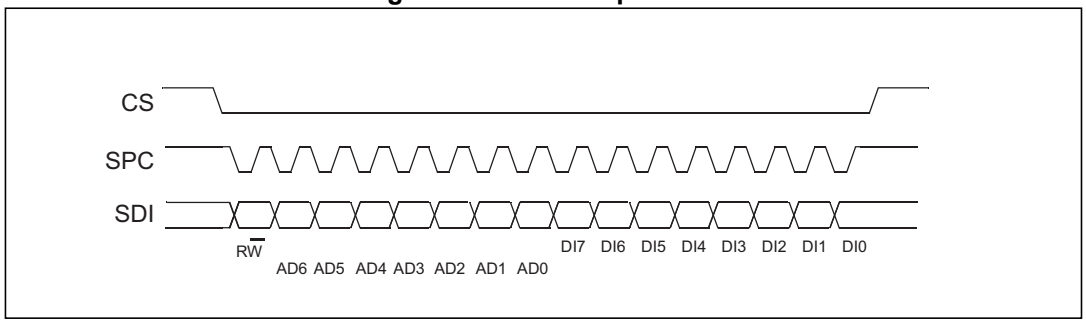
Figure 15. Multiple byte SPI read protocol (2-byte example)



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6.3.2 SPI write

Figure 16. SPI write protocol



The SPI write command is performed with 16 clock pulses. The multiple byte write command is performed by adding blocks of 8 clock pulses to the previous one.

bit 0: WRITE bit. The value is 0.

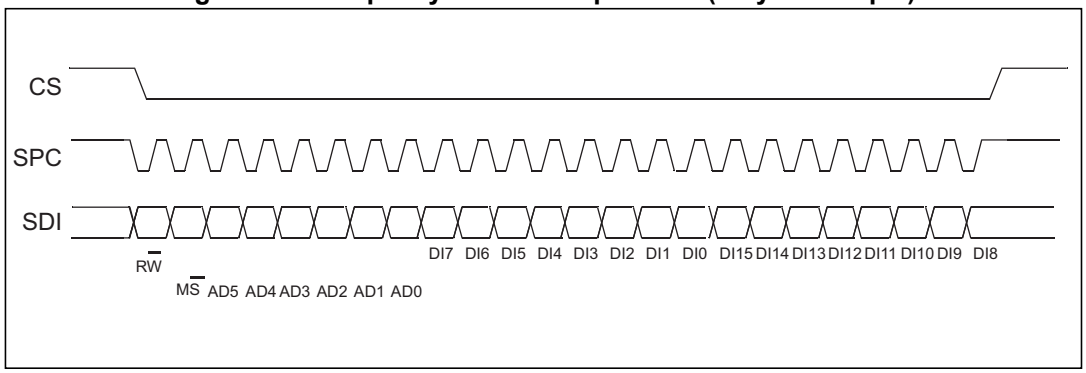
bit 1: MS bit. When 0, does not increment the address; when 1, increments the address in multiple writes.

bit 2 -7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that is written in the device (MSb first).

bit 16-...: data DI(...-8). Further data in multiple byte writes.

Figure 17. Multiple byte SPI write protocol (2-byte example)

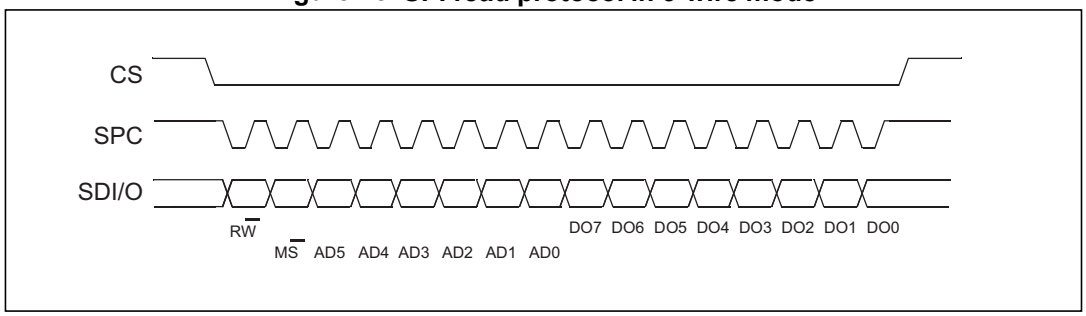


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6.3.3 SPI read in 3-wire mode

A 3-wire mode is entered by setting to '1' bit SIM (SPI serial interface mode selection) in CTRL_REG1.

Figure 18. SPI read protocol in 3-wire mode



The SPI read command is performed with 16 clock pulses:

bit 0: READ bit. The value is 1.

bit 1: MS bit. When 0, does not increment the address; when 1, increments the address in multiple reads.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first). A multiple read command is also available in 3-wire mode.

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7 Register mapping

Table 17 provides a quick overview of the 8-bit registers embedded in the device.

Table 17. Registers address map

Name	Type	Register Address	Default	Function and comment
		Hex	Binary	
Reserved		00-07 0D - 0E	-	Reserved
REF_P_XL	R/W	08	00000000	Reference pressure registers
REF_P_L	R/W	09	00000000	
REF_P_H	R/W	0A	00000000	
WHO_AM_I	R	0F	10111101	Who am I register
RES_CONF	R/W	10	00001111	Resolution register
Reserved		11-1F	-	Reserved
CTRL_REG1	R/W	20	00000000	Control registers
CTRL_REG2	R/W	21	00000000	
CTRL_REG3	R/W	22	00000000	
CTRL_REG4	R/W	23	00000000	
INTERRUPT_CFG	R/W	24	00000000	Interrupt registers
INT_SOURCE	R	25	00000000, output	
Reserved		26	-	Reserved
STATUS_REG	R	27	00000000, output	Status register
PRESS_OUT_XL	R	28	output	Pressure output registers
PRESS_OUT_L	R	29	output	
PRESS_OUT_H	R	2A	output	
TEMP_OUT_L	R	2B	output	Temperature output registers
TEMP_OUT_H	R	2C	output	
Reserved		2D	-	Reserved
FIFO_CTRL	R/W	2E	00000000	FIFO configure registers
FIFO_STATUS	R	2F	00100000, output	
THS_P_L	R/W	30	00000000	Pressure threshold registers
THS_P_H	R/W	31	00000000	
Reserved		32-38	-	Reserved
RPDS_L	R/W	39	00000000	Pressure offset registers
RPDS_H	R/W	3A	00000000	

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Registers marked as Reserved must not be changed. Writing to those registers may cause permanent damage to the device.

To guarantee the proper behavior of the device, all register addresses not listed in the previous table must not be accessed and the content stored in those registers must not be changed.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.

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8 Register description

The device contains a set of registers which are used to control its behavior and to retrieve pressure and temperature data. The register address, made up of 7 bits, is used to identify them and to read/write the data through the serial interface.

8.1 REF_P_XL (08h)

Reference pressure (LSB data)

7	6	5	4	3	2	1	0
REFL7	REFL6	REFL5	REFL4	REFL3	REFL2	REFL1	REFL0

REFL[7:0]	This register contains the low part of the reference pressure value.

The Reference pressure value is a 24-bit data subtracted from the sensor output measurement and it is composed of *REF_P_H (0Ah)*, *REF_P_L (09h)* and *REF_P_XL (08h)*. The value is expressed as 2's complement.

The reference pressure value is subtracted from the sensor output measurement, to detect a measured pressure beyond programmed limits (refer to *INTERRUPT_CFG (24h)* register), and is used for the Autozero function.

8.2 REF_P_L (09h)

Reference pressure (middle part)

15	14	13	12	11	10	9	8
REFL15	REFL14	REFL13	REFL12	REFL11	REFL10	REFL9	REFL8

REFL[15:8]	This register contains the mid part of the reference pressure value. Refer to *REF_P_XL (08h)*.

8.3 REF_P_H (0Ah)

Reference pressure (MSB data)

23	22	21	20	19	18	17	16
REFL23	REFL22	REFL21	REFL20	REFL19	REFL18	REFL17	REFL16

REFL[23:16]	This register contains the high part of the reference pressure value. Refer to *REF_P_XL (08h)*.

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8.4 WHO_AM_I (0Fh)

Device who am I

7	6	5	4	3	2	1	0
1	0	1	1	1	1	0	1

8.5 RES_CONF (10h)

Pressure and temperature resolution

7	6	5	4	3	2	1	0
Reserved				AVGT1	AVGT0	AVGP1	AVGP0

AVGT[1:0]	Temperature internal average configuration. Default: 11 Refer to *Table 18* for all the configurations
AVGP[1:0]	Pressure internal average configuration. Default: 11 Refer to *Table 19* for all the configurations

Table 18. Temperature resolution configuration

AVGT1	AVGT0	Nr. internal average
0	0	8
0	1	16
1	0	32
1	1	64

Table 19. Pressure resolution configuration

AVGP1	AVGP0	Nr. internal average
0	0	8
0	1	32
1	0	128
1	1	512

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8.6 CTRL_REG1 (20h)

Control register 1

7	6	5	4	3	2	1	0
PD	ODR2	ODR1	ODR0	DIFF_EN	BDU	RESET_AZ	SIM

PD	Power-down control. Default value: 0 (0: power-down mode; 1: active mode)
ODR [2:0]	Output data rate selection. Default value: 000 Refer to *Table 20*.
DIFF_EN	Interrupt generation enable. Default value: 0 (0: interrupt generation disabled; 1: interrupt generation enabled)
BDU	Block data update. Default value: 0 (0: continuous update; 1: output registers not updated until MSB and LSB have been read)
RESET_AZ	Reset Autozero function. Default value: 0 (0: normal mode; 1: reset Autozero function)
SIM	SPI Serial Interface Mode selection.Default value: 0 (0: 4-wire interface; 1: 3-wire interface)

The **PD** bit allows the turn on of the device. The device is in power-down mode when PD is set to ‘0’ (default value after boot). The device is active when PD is set to ‘1’.

The **ODR[2,0]** bits can be configured as described in *Table 20*. When ODR[2,0] are set to ‘000’ the device enables one-shot mode. When ‘ONESHOT’ bit in *CTRL_REG2 (21h)* is set to ‘1’, a new set of data for pressure and temperature is acquired.

Table 20. Output data rate bit configurations

ODR2	ODR1	ODR0	Pressure (Hz)	Temperature (Hz)
0	0	0	One-shot mode enabled	
0	0	1	1 Hz	1 Hz
0	1	0	7 Hz	7 Hz
0	1	1	12.5 Hz	12.5 Hz
1	0	0	25 Hz	25 Hz
1	0	1	Reserved	

The **DIFF_EN** bit is used to enable the computing of differential pressure output. It is recommended to enable DIFF_EN after the configuration of *REF_P_H (0Ah)*, *REF_P_L (09h)*, *REF_P_XL (08h)*, *THS_P_H (31h)* and *THS_P_L (30h)*.

The **BDU** bit is used to inhibit the update of the output registers between the reading of the upper and lower register parts. In default mode (BDU = ‘0’), the lower and upper register parts are updated continuously. When the BDU is activated (BDU = ‘1’), the content of the

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output registers is not updated until both MSB and LSB are read, avoiding the reading of values related to different samples.

The **RESET_AZ** bit is used to reset the AutoZero function. Resetting *REF_P_H (0Ah)*, *REF_P_L (09h)* and *REF_P_XL (08h)* sets the pressure reference registers *RPDS_H (3Ah)* and *RPDS_L (39h)* to the default value. RESET_AZ is self-cleared. For the AutoZero function please refer to *CTRL_REG2 (21h)*.

The **SIM** bit selects the SPI serial interface mode:

- 0: (default value) 4-wire SPI interface mode selected;
- 1: 3-wire SPI interface mode selected.

8.7 CTRL_REG2 (21h)

Control register 2

7	6	5	4	3	2	1	0
BOOT	FIFO_EN	STOP_ON_FTH	FIFO_MEAN_DEC	I2C_DIS	SWRESET	AUTO_ZERO	ONE_SHOT

BOOT	Reboot memory content. Default value: 0. (0: normal mode; 1: reboot memory content). The bit is self-cleared when the BOOT is completed.
FIFO_EN	FIFO enable. Default value: 0. (0: disable; 1: enable)
STOP_ON_FTH	Enable the FTH_FIFO bit in *FIFO_STATUS (2Fh)* for monitoring of FIFO level. Default value: 0 (0: disable; 1: enable).
FIFO_MEAN_DEC	Enable to decimate the output pressure to 1Hz with FIFO Mean mode. Default value: 0 (0: disable / 1: enable)
I2C_DIS	I^2C interface enabled. Default value 0. (0: I^2C enabled;1: I^2C disabled)
SWRESET	Software reset. Default value: 0. (0: normal mode; 1: software reset). The bit is self-cleared when the reset is completed.
AUTOZERO	Autozero enable. Default value: 0. (0: normal mode; 1: Autozero enabled)
ONE_SHOT	One shot mode enable. Default value: 0. (0: idle mode; 1: a new dataset is acquired)

The **BOOT** bit is used to refresh the content of the internal registers stored in the Flash memory block. At device power-up the content of the Flash memory block is transferred to the internal registers related to the trimming functions to allow correct behavior of the device itself. If for any reason the content of the trimming registers is modified, it is sufficient to use this bit to restore the correct values. When the BOOT bit is set to '1', the content of the internal Flash is copied inside the corresponding internal registers and is used to calibrate

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the device. These values are factory trimmed and they are different for every device. They allow correct behavior of the device and normally they should not be changed. The boot process takes 2.2 msec. At the end of the boot process, the BOOT bit is set to ‘0’ automatically.

FIFO_MEAN_DEC bit is to decimate the output pressure to 1Hz with FIFO Mean mode. When this bit is ‘1’, the output is decimated to 1 Hz as the moving average is being taken at the rate of the ODR. Otherwise, averaged pressure data will be updated according to the ODR defined.

SWRESET is the software reset bit. The device is reset to the power-on configuration after SWRESET bit is set to '1'. The software reset process takes 4 µsec. When BOOT follows, the recommended sequence is SWRESET first and then BOOT.

AUTOZERO, when set to ‘1’, the actual pressure output value is copied in *REF_P_H (0Ah)*, *REF_P_L (09h)* and *REF_P_XL (08h)*. When this bit is enabled, the register content of REF_P is subtracted from the pressure output value.

The **ONE_SHOT** bit is used to start a new conversion when the ODR[2,0] bits in *CTRL_REG1 (20h)* are set to ‘000’. Writing a ‘1’ in ONE_SHOT triggers a single measurement of pressure and temperature. Once the measurement is done, the ONE_SHOT bit will self-clear, the new data are available in the output registers, and the STATUS_REG bits are updated.

8.8 CTRL_REG3 (22h)

Interrupt control

7	6	5	4	3	2	1	0
INT_H_L	PP_OD	Reserved				INT_S2	INT_S1

INT_H_L	Interrupt active high, low. Default value: 0. (0: active high; 1: active low)
PP_OD	Push-pull/open drain selection on interrupt pads. Default value: 0. (0: push-pull; 1: open drain)
INT_S[2:1]	Data signal on INT_DRDY pin control bits. Default value: 00. Refer to *Table 21*.

Table 21. Interrupt configurations

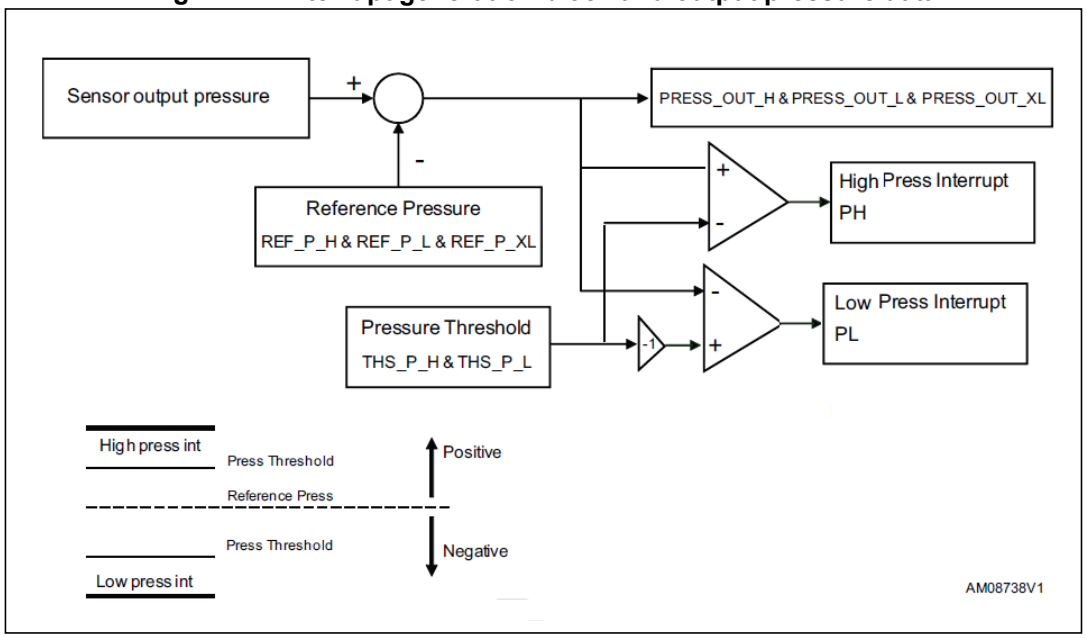
INT_S2	INT_S1	INT_DRDY pin configuration
0	0	Data signal (see *CTRL_REG4 (23h)*)
0	1	Pressure high (P_high)
1	0	Pressure low (P_low)
1	1	Pressure low OR high

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The device features one set of programmable interrupt sources (*INT*) that can be configured to trigger different pressure events. *Figure 19* shows the block diagram of the interrupt generation block and output pressure data.

The device may also be configured to generate, through the INT_DRDY pin, a Data Ready signal (DRDY) which indicates when a new measured pressure data is available, thus simplifying data synchronization in digital systems or optimizing system power consumption.

Figure 19. Interrupt generation block and output pressure data



8.9 CTRL_REG4 (23h)

Interrupt configuration

7	6	5	4	3	2	1	0
0	0	0	0	F_EMPTY	F_FTH	F_OVR	DRDY

F_EMPTY	FIFO empty flag on INT_DRDY pin. Default value: 0. (0: disable; 1: enable)
F_FTH	FIFO threshold (watermark) status on INT_DRDY pin to indicate that FIFO is filled up to the threshold level. Default value: 0. (0: disable; 1: enable)
F_OVR	FIFO overrun interrupt on INT_DRDY pin to indicate that FIFO is full in FIFO mode or that an overrun occurred in Stream mode. Default value: 0. (0: disable; 1: enable)
DRDY	Data-ready signal on INT_DRDY pin. Default value: 0. (0: disable; 1: enable)

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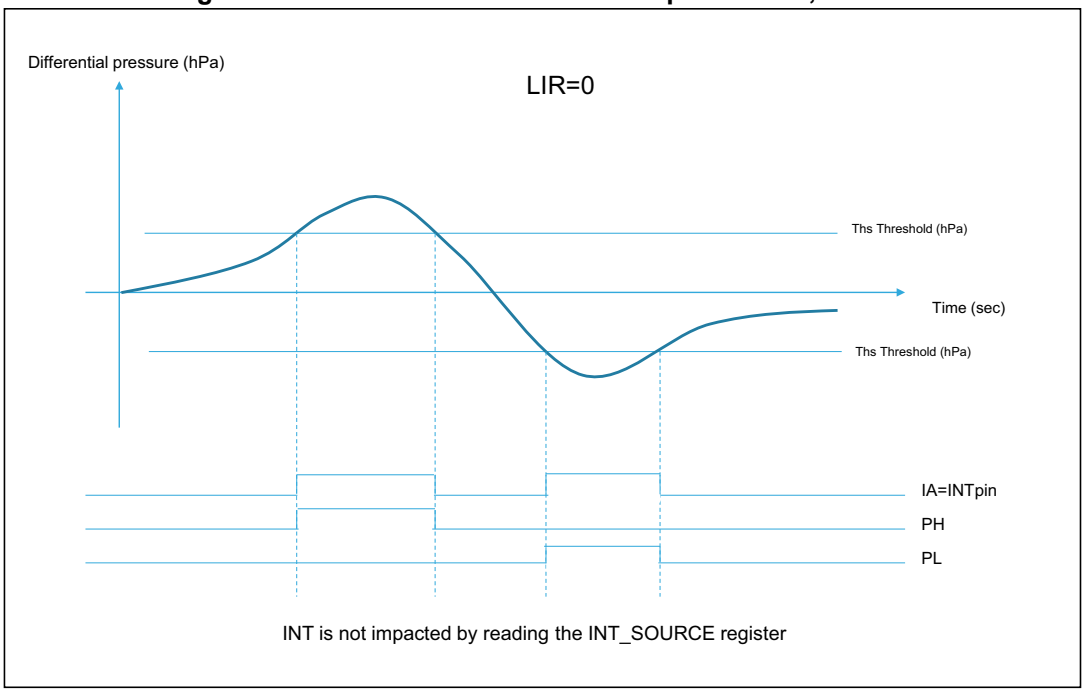
8.10 INTERRUPT_CFG (24h)

Interrupt configuration

7	6	5	4	3	2	1	0
Reserved					LIR	PL_E	PH_E

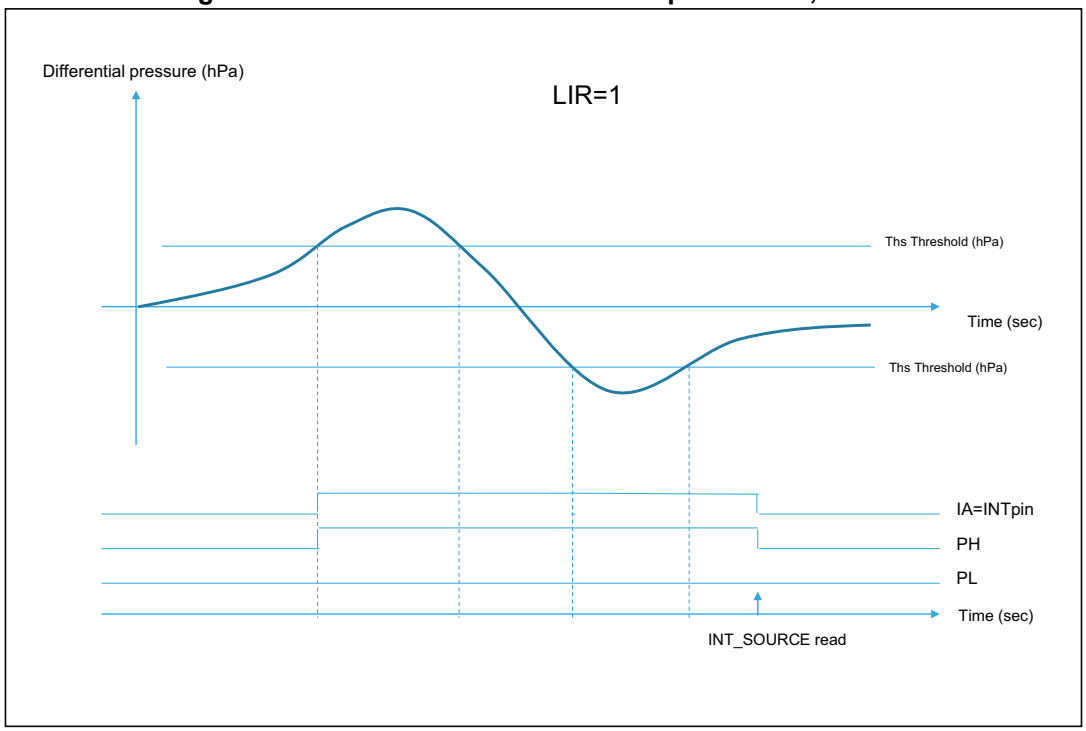
LIR	Latch interrupt request to the *INT_SOURCE (25h)* register. Default value: 0. (0: interrupt request not latched; 1: interrupt request latched)
PL_E	Enable interrupt generation on differential pressure low event. Default value: 0. (0: disable interrupt request; 1: enable interrupt request on measured differential pressure value lower than preset threshold)
PH_E	Enable interrupt generation on differential pressure high event. Default value: 0. (0: disable interrupt request; 1: enable interrupt request on measured differential pressure value higher than preset threshold)

Figure 20. Differential threshold interrupt behavior, LIR = 0



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Figure 21. Differential threshold interrupt behavior, LIR = 1



8.11 INT_SOURCE (25h)

Interrupt source

7	6	5	4	3	2	1	0
0	0	0	0	0	IA	PL	PH

IA	Interrupt active. (0: no interrupt has been generated; 1: one or more interrupt events have been generated).
PL	Differential pressure Low. (0: no interrupt has been generated; 1: Low differential pressure event has occurred).
PH	Differential pressure High. (0: no interrupt has been generated; 1: High differential pressure event has occurred).

INT_SOURCE register is cleared by reading it.

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8.12 STATUS_REG (27h)

Status register

7	6	5	4	3	2	1	0
RES		P_OR	T_OR	RES		P_DA	T_DA

P_OR	Pressure data overrun. (0: no overrun has occurred; 1: new data for pressure has overwritten the previous one)
T_OR	Temperature data overrun. (0: no overrun has occurred; 1: a new data for temperature has overwritten the previous one)
P_DA	Pressure data available. (0: new data for pressure is not yet available; 1: new data for pressure is available)
T_DA	Temperature data available. (0: new data for temperature is not yet available; 1: new data for temperature is available)

This register is updated every ODR cycle, regardless of the BDU value in *CTRL_REG1 (20h)*.

P_OR bit is set to '1' whenever new pressure data is available and P_DA was set in the previous ODR cycle and not cleared. P_OR is cleared when the *PRESS_OUT_H (2Ah)* register is read.

T_OR is set to ‘1’ whenever new temperature data is available and T_DA was set in the previous ODR cycle and not cleared. T_OR is cleared when the *TEMP_OUT_H (2Ch)* register is read.

P_DA is set to 1 whenever a new pressure sample is available. P_DA is cleared when the *PRESS_OUT_H (2Ah)* register is read.

T_DA is set to 1 whenever a new temperature sample is available. T_DA is cleared when the *TEMP_OUT_H (2Ch)* register is read.

8.13 PRESS_OUT_XL (28h)

Pressure output value (LSB)

7	6	5	4	3	2	1	0
POUT7	POUT6	POUT5	POUT4	POUT3	POUT2	POUT1	POUT0

POUT[7:0]	This register contains the low part of the pressure output value.

The pressure output value is a 24-bit data that contains the measured pressure. It is composed of *PRESS_OUT_H (2Ah)*, *PRESS_OUT_L (29h)* and *PRESS_OUT_XL (28h)*. The value is expressed as 2’s complement.

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8.14 PRESS_OUT_L (29h)

Pressure output value (mid part)

15	14	13	12	11	10	9	8
POUT15	POUT14	POUT13	POUT12	POUT11	POUT10	POUT9	POUT8

POUT[15:8]	This register contains the mid part of the pressure output value. Refer to *PRESS_OUT_XL (28h)*.

8.15 PRESS_OUT_H (2Ah)

Pressure output value (MSB)

23	22	21	20	19	18	17	16
POUT23	POUT22	POUT21	POUT20	POUT19	POUT18	POUT17	POUT16

POUT[23:16]	This register contains the high part of the pressure output value. Refer to *PRESS_OUT_XL (28h)*.

8.16 TEMP_OUT_L (2Bh)

Temperature output value (LSB)

7	6	5	4	3	2	1	0
TOUT7	TOUT6	TOUT5	TOUT4	TOUT3	TOUT2	TOUT1	TOUT0

TOUT[7:0]	This register contains the low part of the temperature output value.

The temperature output value is a 16-bit data that contains the measured temperature. It is composed of *TEMP_OUT_H (2Ch)* and *TEMP_OUT_L (2Bh)*. The value is expressed as 2's complement.

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8.17 TEMP_OUT_H (2Ch)

Temperature output value (MSB)

15	14	13	12	11	10	9	8
TOUT15	TOUT14	TOUT13	TOUT12	TOUT11	TOUT10	TOUT9	TOUT8

TOUT[15:8]	This register contains the high part of the temperature output value.

The temperature output value is a 16-bit data that contains the measured temperature. It is composed by *TEMP_OUT_H (2Ch)* and *TEMP_OUT_L (2Bh)*. The value is expressed as 2's complement.

8.18 FIFO_CTRL (2Eh)

FIFO control

7	6	5	4	3	2	1	0
F_MODE2	F_MODE1	F_MODE0	WTM_POINT4	WTM_POINT3	WTM_POINT2	WTM_POINT1	WTM_POINT0

F_MODE[2:0]	FIFO mode selection. Default value: 000. Refer to *Table 22* and *Section 4* for additional details.
WTM_POINT[4:0]	FIFO threshold (watermark) level selection. Refer to *Table 23* for additional details.

Table 22. FIFO mode selection

F_MODE	F_MODE	F_MODE	FIFO mode
0	0	0	Bypass mode
0	0	1	FIFO mode
0	1	0	Stream mode
0	1	1	Stream-to-FIFO mode
1	0	0	Bypass-to-Stream mode
1	0	1	Not available
1	1	0	FIFO Mean mode
1	1	1	Bypass-to-FIFO mode

FIFO Mean mode: The FIFO can be used for implementing a HW moving average on the pressure measurements. The number of samples of the moving average can be 2, 4, 8, 16 or 32 samples by selecting the FIFO Mean mode sample size as per *Table 23*. Different configurations are not allowed.

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Table 23. Running average sample size

WTM_POINT[4:0]	FIFO Mean mode sample size
00001	2-sample moving average
00011	4-sample moving average
00111	8-sample moving average
01111	16-sample moving average
11111	32-sample moving average

Please note that when using the FIFO Mean mode it is not possible to access the FIFO content.

8.19 FIFO_STATUS (2Fh)

FIFO status

7	6	5	4	3	2	1	0
FTH_FIFO	OVR	EMPTY_FIFO	FSS4	FSS3	FSS2	FSS1	FSS0

FTH_FIFO	FIFO threshold status. (0: FIFO filling is lower than FTH level; 1: FIFO filling is equal or higher than FTH level).
OVR	Overrun bit status. (0: FIFO not full; 1: FIFO is full and at least one sample in the FIFO has been overwritten).
EMPTY_FIFO	Empty FIFO bit status. (0: FIFO not empty; 1: FIFO is empty).
FSS[4:0]	FIFO stored data level. (00000: FIFO empty @ EMPTY_FIFO "1" or 1st sample stored in FIFO@EMPTY_FIFO "0"; 11111: FIFO is full and has 32 unread samples).

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8.20 THS_P_L (30h)

Least significant bits of the threshold value for pressure interrupt generation.

7	6	5	4	3	2	1	0
THS7	THS6	THS5	THS4	THS3	THS2	THS1	THS0

THS[7:0]	This register contains the low part of threshold value for pressure interrupt generation.

The threshold value for pressure interrupt generation is a 16-bit register composed of *THS_P_H (31h)* and *THS_P_L (30h)*. The value is expressed as unsigned number: Interrupt threshold(hPA) = (THS_P)/16.

8.21 THS_P_H (31h)

Most significant bits of the threshold value for pressure interrupt generation.

15	14	13	12	11	10	9	8
THS15	THS14	THS13	THS12	THS11	THS10	THS9	THS8

THS[15:8]	This register contains the high part of threshold value for pressure interrupt generation. Refer to *THS_P_L (30h)*.

8.22 RPDS_L (39h)

Pressure offset (LSB data)

7	6	5	4	3	2	1	0
RPDS7	RPDS6	RSPDS5	RPDS4	RPDS3	RPDS2	RPDS1	RPDS0

RPDS[7:0]	This register contains the low part of the pressure offset value.

The pressure offset value is a 16-bit data that can be used to implement One-Point Calibration (OPC) after soldering, This value is composed of *RPDS_H (3Ah)* and *RPDS_L (39h)*. The value is expressed as 2's complement.

8.23 RPDS_H (3Ah)

Pressure offset (MSB data)

7	6	5	4	3	2	1	0
RPDS15	RPDS14	RSPDS13	RPDS12	RPDS11	RPDS2	RPDS9	RPDS8

RPDS[15:8]	This register contains the high part of the pressure offset value. Refer to *RPDS_L (39h)*.

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9 Package mechanical data

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Figure 22. HLGA-10L (2.5 x 2.5 x 0.76 mm typ.) outline and mechanical data

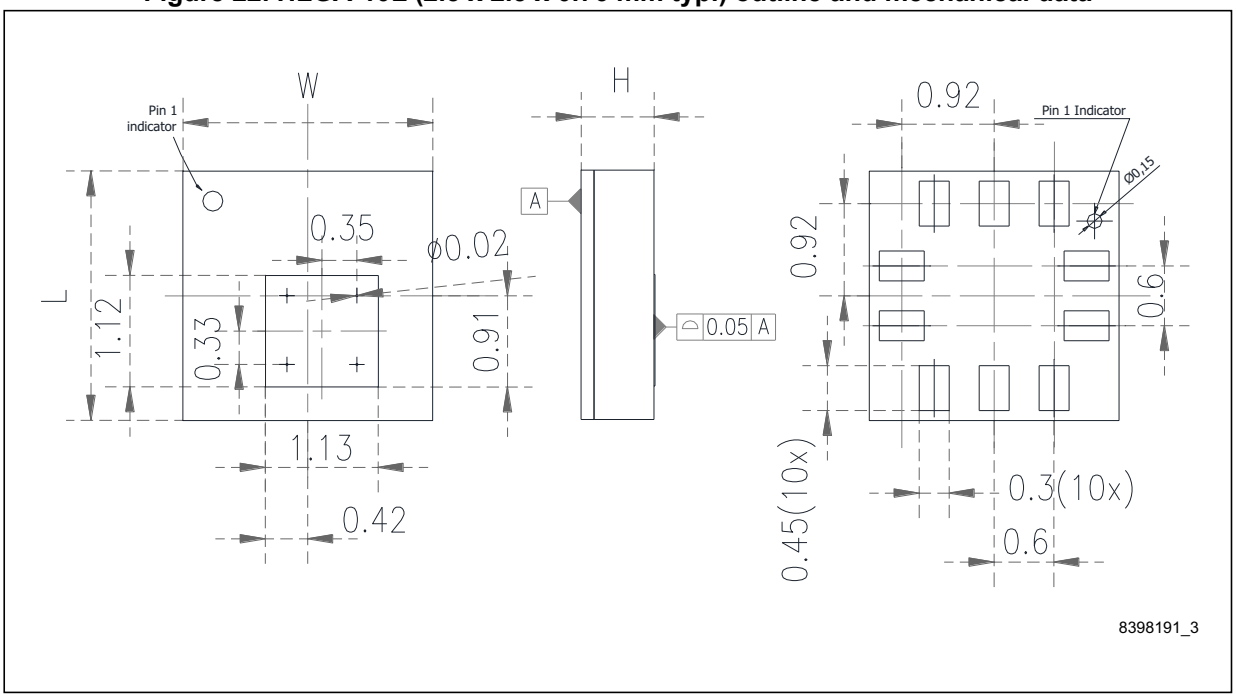


Table 24. HLGA-10L (2.5 x 2.5 x 0.76 mm typ.) outer dimensions

Item	Dimension	Tolerance (mm)
Length (L)	2.5	±0.1
Width (W)	2.5	±0.1
Height (H)	0.8 MAX	/
Pad size	0.3 x 0.45	±0.05

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9.1 HLGA-10 packing information

Figure 23. Carrier tape information for HLGA-10L

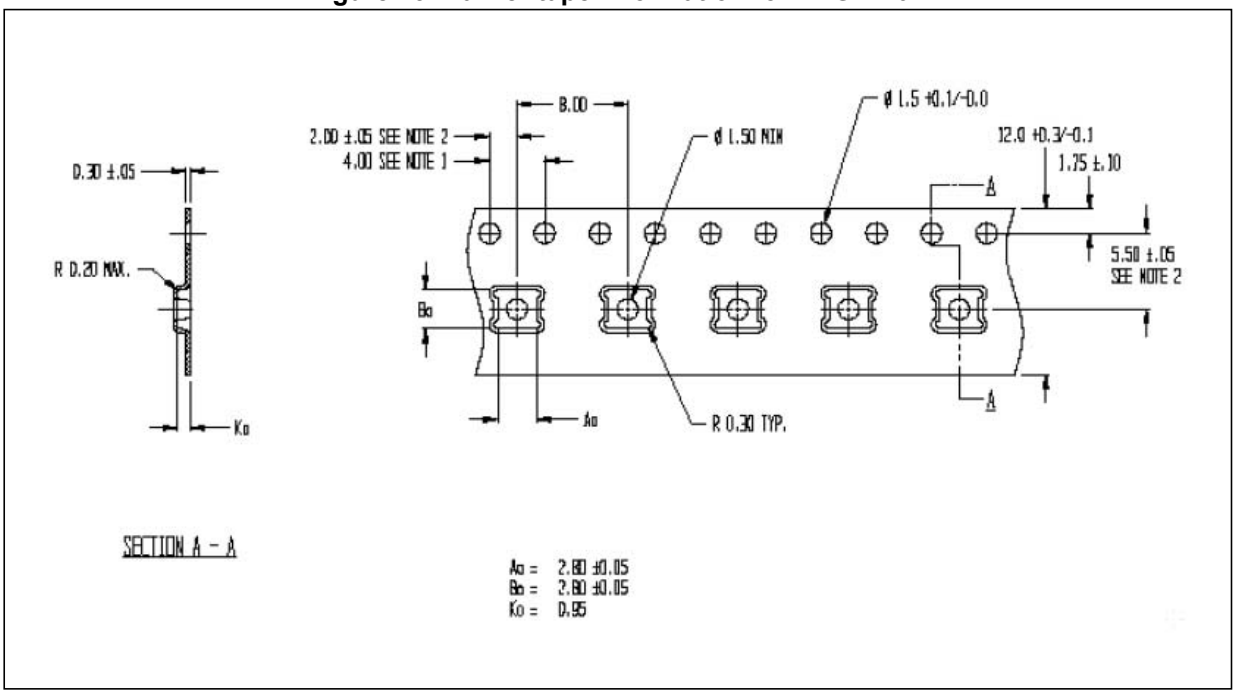
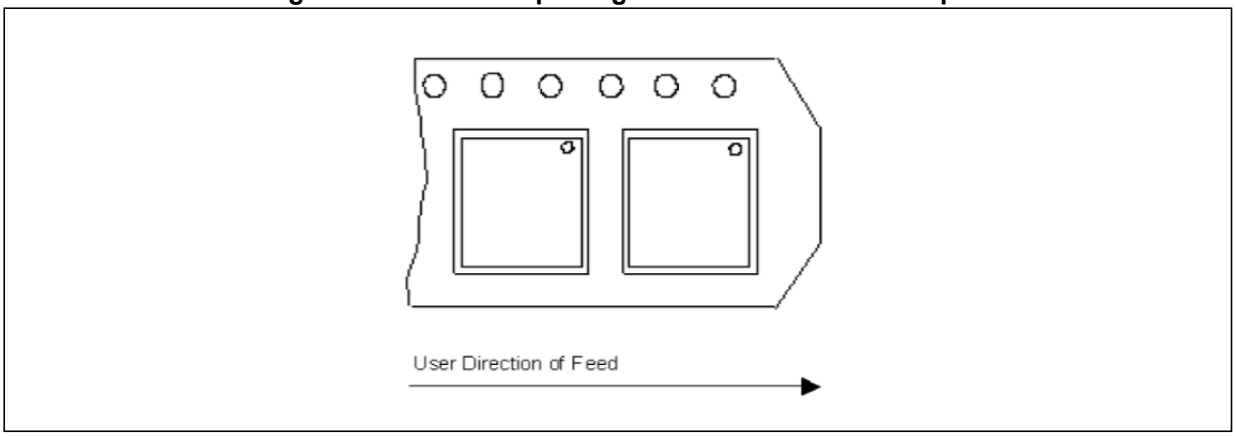


Figure 24. HLGA-10L package orientation in carrier tape



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Figure 25. Reel information for carrier tape of HLGA-10L

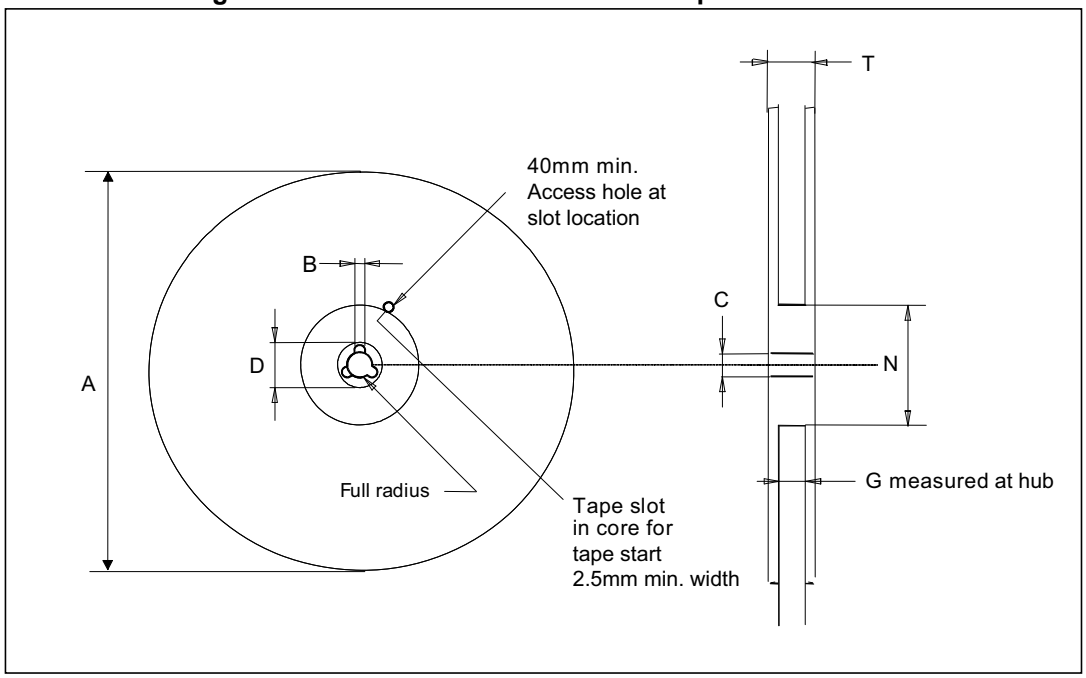


Table 25. Reel dimensions for carrier tape of HLGA-10L

Reel dimensions (mm)	
A (max)	330
B (min)	1.5
C	13 ±0.25
D (min)	20.2
N (min)	60
G	12.4 +2/-0
T (max)	18.4

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10 Revision history

Table 26. Document revision history

Date	Revision	Changes
30-Oct-2014	1	Initial release
21-May-2015	2	Updated Table 1: Device summary. Minor update in Figure 2: Pin connections (bottom view), Figure 5: LPS25HB electrical connections (top view), Section 4: FIFO, Section 8.1: REF_P_XL (08h), Section 8.15: PRESS_OUT_H (2Ah) and Figure 12: Interrupt generation block and output pressure data.
14-Jun-2016	3	Updated: - Features - Table 4: Electrical characteristics; - Table 6: I2C slave timing values; - Table 4: Electrical characteristics, - Table 16: Registers address map - Section 9: Package mechanical data Updated register information: - 8.7: CTRL_REG2 (21h); - 8.8: CTRL_REG3 (22h) - 8.12: STATUS_REG (27h), - 8.18: FIFO_CTRL (2Eh), - 8.19: FIFO_STATUS (2Fh).
16-Aug-2016	4	Updated *Table 3: Pressure and temperature sensor characteristics* Added *Table 5: DC characteristics* Added *Section 3.4: How to interpret pressure readings* Updated *Section 4: FIFO* Updated *Section 5.1: Soldering information* Updated *Table 17: Registers address map* Updated *CTRL_REG2 (21h)* Added *Figure 20* and *Figure 21* Added *Section 9.1: HLGA-10 packing information*

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