L99DZ100G, L99DZ100GP

Automotive door module with LIN and HS-CAN (L99DZ100G) or HS-CAN supporting selective wake up (L99DZ100GP)

Datasheet - production data



LQFP-64

GAPG2907151543CFT

Features

- AEC Q100 compliant qualified
- 1 half bridge for 7.5 A load (R_{ON} = 100 mΩ)
- 1 half bridge for 7.5 A load (R_{ON} = 150 mΩ)
- 2 half bridges for 0.5 A load (R_{ON} = 2000 mΩ)
- 2 half bridges for 3 A load (R_{ON} = 300 mΩ)
- 1 configurable high-side driver for up to 1.5 A (R_{ON} = 500 mΩ) or 0.35 A (R_{ON} = 1600 mΩ) load
- 1 configurable high-side driver for 0.8 A (R_{ON} = 800 mΩ) or 0.35 A (R_{ON} = 1600 mΩ) load
- 3 configurable high-side drivers for 0.15 A/0.35 A (R_{ON} =2 Ω)
- 1 configurable high-side driver for 0.25 A/0.5 A (R_{ON} = 2 Ω) to supply EC Glass MOSFET
- 4 configurable high-side drivers for 0.15 A/0.25 A (R_{ON} = 5 Ω)
- Internal 10bit PWM timer for each stand-alone high-side driver
- Buffered supply for voltage regulators and 2 high-side drivers (OUT15 & OUT_HS / both P-channel) to supply e.g. external contacts
- Programmable soft-start function to drive loads with higher inrush currents as current limitation value (for OUT1-6, OUT7, OUT8 and OUT_HS) with thermal expiration feature
- All the embedded outputs come with protection and supervision features:
  - Current Monitor (high-side only)
  - Open-load
  - Overcurrent
  - Thermal warning
  - Thermal shutdown
- Fully protected driver for external MOSFETs in H-bridge configuration or dual Half bridge configuration
- Fully protected driver for external high-side MOSFET
- Control block for electro-chromic element
- Two 5 V voltage regulators for microcontroller and peripheral supply
- Programmable reset generator for power-on and undervoltage
- Configurable window watchdog
- LIN 2.2a compliant (SAEJ2602 compatible) transceiver
- Advanced high speed CAN transceiver (ISO 11898-2:2003 /-5:2007 and SAE J2284 compliant) with local failure and bus failure diagnosis and selective wake-up functionality according to ISO 11898-6:2013
- Separated (Isolated) fail-safe block with 2 LS (R_{ON} = 1 Ω) to pull down the gates of the external HS MOSFETs
- Thermal clusters
- A/D conversion of supply voltages and internal temperature sensors
- Embedded and programmable VS duty cycle adjustment for LED driver outputs

Applications

Door zone applications.

This is information on a product in full production.

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Table 1. Device summary

Package	Variant	Order codes	
		Tray	Tape and reel
LQFP-64 epad	High Speed CAN Transceiver with partial networking (ISO 11898-6:2013)	L99DZ100GP	L99DZ100GPTR
LQFP-64 epad	High Speed CAN Transceiver (ISO 11898-2:2003 and 11898-5:2007)	L99DZ100G	L99DZ100GTR

Product label


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Contents

1 Description 14

2 Block diagram and pin descriptions 15

3 Electrical specifications 20

3.1 Absolute maximum ratings 20

3.2 ESD protection 22

3.3 Thermal data 23

3.3.1 LQFP64 thermal data 23

3.4 Electrical characteristics 27

3.4.1 Supply and supply monitoring 27

3.4.2 Oscillator 29

3.4.3 Power-on reset (VSREG) 29

3.4.4 Voltage regulator V1 30

3.4.5 Voltage regulator V2 31

3.4.6 Reset output 32

3.4.7 Watchdog timing 34

3.4.8 Current monitor output (CM) 36

3.4.9 Charge pump 37

3.4.10 Outputs OUT1 - OUT15, OUT_HS, ECV, ECDR 38

3.4.11 Power outputs switching times 40

3.4.12 Current monitoring 41

3.4.13 Heater 43

3.4.14 H-bridge driver 44

3.4.15 Gate drivers for the external Power-MOS switching times 45

3.4.16 Drain source monitoring external H-bridge 48

3.4.17 Drain source monitoring external heater MOSFET 49

3.4.18 Open-load monitoring external H-bridge 49

3.4.19 Open-load monitoring external heater MOSFET 50

3.4.20 Electro-chrome mirror driver 50

3.4.21 Fail safe low-side switch 51

3.4.22 Wake up input WU 52

3.4.23 High speed CAN transceiver 52

3.4.24 LIN transceiver 58

深圳市满度科技有限公司
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Tel:150-1290-5940
Email:sales@manduic.com

3.4.25 SPI . . . 61
3.4.26 Inputs TxD_C and TxD_L for Flash mode . . . 63
3.4.27 Inputs DIRH, PWMH . . . 64
3.4.28 Debug input . . . 64
3.4.29 ADC characteristics . . . 64
3.4.30 Temperature diode characteristics . . . 65
3.4.31 Interrupt outputs . . . 65
3.4.32 Timer1 and Timer2 . . . 66
3.4.33 SGND loss comparator . . . 69

4 Application information . . . 70

4.1 Supply V_S, V_{SREG} . . . 70
4.2 Voltage regulators . . . 70
4.2.1 Voltage regulator: V1 . . . 70
4.2.2 Voltage regulator: V2 . . . 71
4.2.3 Voltage regulator failure . . . 71
4.2.4 Short to ground detection . . . 71
4.2.5 Voltage regulator behavior . . . 72
4.3 Operating modes . . . 72
4.3.1 Active mode . . . 72
4.3.2 Flash modes . . . 73
4.3.3 SW-debug mode . . . 73
4.3.4 V1_standby mode . . . 74
4.3.5 Interrupt . . . 74
4.3.6 CAN wake-up signalization . . . 75
4.3.7 VBAT_standby mode . . . 76
4.4 Wake-up from Standby modes . . . 76
4.4.1 Wake up input . . . 77
4.5 Functional overview (truth table) . . . 77
4.6 Configurable window watchdog . . . 79
4.6.1 Change watchdog timing . . . 82
4.7 Fail-safe mode . . . 82
4.7.1 Temporary failures . . . 82
4.7.2 Non-recoverable failures – forced Vbat_standby mode . . . 83
4.8 Reset output (NReset) . . . 84
4.9 LIN Bus Interface . . . 85

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Tel:150-1290-5940
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4.9.1 Features . . . 85
4.9.2 Error handling . . . 86
4.9.3 Wake up from Standby modes . . . 86
4.9.4 Receive-only mode . . . 87
4.10 High-speed CAN bus transceiver . . . 87
4.10.1 Features: . . . 88
4.10.2 CAN transceiver operating modes . . . 89
4.10.3 Automatic voltage biasing . . . 90
4.10.4 Wake-up by CAN . . . 90
4.10.5 CAN looping . . . 92
4.10.6 Pretended networking . . . 92
4.10.7 CAN error handling . . . 92
4.11 Serial Peripheral Interface (ST SPI Standard) . . . 93
4.12 Power supply failure . . . 94
4.12.1 V_S supply failure . . . 94
4.12.2 V_{SREG} supply failure . . . 95
4.13 Temperature warning and thermal shutdown . . . 97
4.14 Power outputs OUT1..15 and OUT_HS . . . 98
4.15 Auto-recovery alert and thermal expiration . . . 99
4.16 Charge pump . . . 101
4.17 Inductive loads . . . 102
4.18 Open-load detection . . . 102
4.19 Overcurrent detection . . . 102
4.20 Current monitor . . . 102
4.21 PWM mode of the power outputs . . . 102
4.22 Cross-current protection . . . 102
4.23 Programmable soft-start function to drive loads with higher inrush current . . . 103
4.24 H-bridge control . . . 105
4.25 H-bridge driver slew-rate control . . . 107
4.26 Resistive low . . . 107
4.27 Short circuit detection / drain source monitoring . . . 108
4.28 H-bridge monitoring in off-mode . . . 108
4.29 Programmable cross current protection . . . 111

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4.30 Power window H-bridge safety switch off block 111
4.31 Heater MOSFET Driver 113
4.32 Controller of electro-chromic glass 114
4.33 Temperature warning and shutdown 115
4.34 Thermal clusters 116
4.35 V_S compensation (duty cycle adjustment) module 117
4.36 Analog digital converter 118

5 Serial Peripheral Interface (SPI) 120
5.1 ST SPI 4.0 120
5.1.1 Physical layer 121
5.2 Signal description 121
5.2.1 Clock and Data Characteristics 122
5.2.2 Communication protocol 123
5.2.3 Address definition 126
5.2.4 Protocol failure detection 132

6 Application 134

7 SPI Registers 135
7.1 Global Status Byte GSB 135
7.2 Control register overview 139
7.3 Status register overview 144
7.4 Control registers 146
7.4.1 Control Register CR1 (0x01) 146
7.4.2 Control Register CR2 (0x02) 149
7.4.3 Control Register CR3 (0x03) 152
7.4.4 Control Register CR4 (0x04) 154
7.4.5 Control Register CR5 (0x05) 156
7.4.6 Control Register CR6 (0x06) 158
7.4.7 Control Register CR7 (0x07) 159
7.4.8 Control Register CR8 (0x08) 161
7.4.9 Control Register CR9 (0x09) 162
7.4.10 Control Register CR10 (0x0A) 163
7.4.11 Control Register CR11 (0x0B) 165
7.4.12 Control Register CR12 (0x0C) 166

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7.4.13 Control Register CR13 (0x0D) to CR17 (0x11) 167
7.4.14 Control Register CR18 (0x12) to CR22 (0x16) 168
7.4.15 Control Register CR23 (0x17) 170
7.4.16 Control Register CR24 (0x18) 170
7.4.17 Control Register CR25 (0x19) 172
7.4.18 Control Register CR26 (0x1A) 172
7.4.19 Control Register CR27 (0x1B) 173
7.4.20 Control Register CR28 (0x1C) 173
7.4.21 Control Register CR29 (0x1D) 174
7.4.22 Control Register CR34 (0x22) 174
7.4.23 Configuration Register (0x3F) 175
7.5 Status Registers 178
7.5.1 Status Register SR1 (0x31) 178
7.5.2 Status Register SR2 (0x32) 180
7.5.3 Status Register SR3 (0x33) 182
7.5.4 Status Register SR4 (0x34) 184
7.5.5 Status Register SR5 (0x35) 185
7.5.6 Status Register SR6 (0x36) 187
7.5.7 Status Register SR7 (0x37) to SR9 (0x39) 188
7.5.8 Status Register SR10 (0x3A) 189
7.5.9 Status Register SR11 (0x3B) 190
7.5.10 Status Register SR12 (0x3C) 191

8 Package information 193
8.1 LQFP-64 package information 193
8.2 LQFP-64 marking information 195

9 Revision history 196

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List of tables

Table 1. Device summary . . . 2
Table 2. Pin definitions and functions . . . 15
Table 3. Absolute maximum ratings . . . 20
Table 4. ESD protection . . . 22
Table 5. Operating junction temperature . . . 23
Table 6. Temperature warning and thermal shutdown . . . 23
Table 7. Supply and supply monitoring . . . 28
Table 8. Oscillator . . . 29
Table 9. Power-on reset (V_{SREG}) . . . 29
Table 10. Voltage regulator V1 . . . 30
Table 11. Voltage regulator V2 . . . 31
Table 12. Reset output . . . 32
Table 13. Watchdog timing . . . 34
Table 14. Current monitor output (CM) . . . 36
Table 15. Charge pump electrical characteristics . . . 37
Table 16. Outputs OUT1 - OUT15, OUT_HS, ECV, ECDR . . . 38
Table 17. Power outputs switching times . . . 40
Table 18. Current monitoring . . . 41
Table 19. Heater . . . 43
Table 20. H-bridge driver . . . 44
Table 21. Gate drivers for the external Power-MOS switching times . . . 45
Table 22. Drain source monitoring external H-bridge . . . 48
Table 23. Drain source monitoring external heater MOSFET . . . 49
Table 24. Open-load monitoring external H-bridge . . . 49
Table 25. Open-load monitoring external heater MOSFET . . . 50
Table 26. Electro-chrome mirror driver . . . 50
Table 27. Fail safe low-side switch . . . 51
Table 28. Wake-up inputs . . . 52
Table 29. CAN communication operating range . . . 52
Table 30. CAN transmit data input: pin TxDC . . . 53
Table 31. CAN receive data output: Pin RxDC . . . 53
Table 32. CAN transmitter dominant output characteristics . . . 53
Table 33. CAN transmitter recessive output characteristics, CAN normal mode . . . 54
Table 34. CAN transmitter recessive output characteristics, CAN low-power mode, biasing active . 54
Table 35. CAN transmitter recessive output characteristics, CAN low-power mode, biasing inactive 55
Table 36. CAN receiver input characteristics during CAN normal mode . . . 55
Table 37. CAN receiver input characteristics during CAN low power mode, biasing active . . . 55
Table 38. CAN Receiver input characteristics during CAN Low power mode, biasing inactive . . . 56
Table 39. CAN receiver input resistance biasing active . . . 56
Table 40. CAN transceiver delay . . . 56
Table 41. Maximum leakage currents on CAN_H and CAN_L, unpowered . . . 57
Table 42. Biasing control timings . . . 57
Table 43. LIN transmit data input: pin TxD . . . 58
Table 44. LIN receive data output: pin RxD . . . 58
Table 45. LIN transmitter and receiver: pin LIN . . . 58
Table 46. LIN transceiver timing . . . 60
Table 47. Input: CSN . . . 61
Table 48. Inputs: CLK, DI . . . 61

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Table 49. DI, CLK and CSN timing . . . 62
Table 50. Output: DO . . . 62
Table 51. DO timing . . . 62
Table 52. CSN timing . . . 63
Table 53. Inputs: TxD_C and TxD_L for Flash mode . . . 63
Table 54. Inputs DIRH, PWMH . . . 64
Table 55. Debug input . . . 64
Table 56. ADC characteristics . . . 64
Table 57. Temperature diode characteristics . . . 65
Table 58. Interrupt outputs . . . 65
Table 59. Timer1 and Timer2 . . . 66
Table 60. SGND loss comparator . . . 69
Table 61. CAN wake-up signalization . . . 75
Table 62. Wake-up events description . . . 76
Table 63. Status of different functions/features vs operating modes . . . 77
Table 64. Temporary failures description . . . 83
Table 65. Non-recoverable failure . . . 84
Table 66. Power output settings . . . 99
Table 67. H-bridge control truth table . . . 106
Table 68. H-bridge monitoring in off-mode . . . 110
Table 69. Heater MOSFET control truth table . . . 114
Table 70. Thermal cluster definition . . . 117
Table 71. Operation codes . . . 123
Table 72. Global Status Byte . . . 125
Table 73. Device application access . . . 126
Table 74. Device information read access . . . 126
Table 75. RAM address range . . . 126
Table 76. ROM address range . . . 127
Table 77. Information Registers Map . . . 128
Table 78. SPI Mode Register . . . 129
Table 79. Burst Read Bit . . . 129
Table 80. SPI Data Length . . . 130
Table 81. Data Consistency Check . . . 130
Table 82. WD Type/Timing . . . 130
Table 83. WD bit position . . . 131
Table 84. Global Status Byte (GSB) . . . 135
Table 85. GSB signals description . . . 135
Table 86. Control register overview . . . 139
Table 87. Status register overview . . . 144
Table 88. Control Register CR1 . . . 146
Table 89. CR1 signals description . . . 146
Table 90. Wake-up input1 filter configuration . . . 148
Table 91. CAN transceiver mode . . . 148
Table 92. Voltage regulator V2 configuration . . . 149
Table 93. Standby transition configuration . . . 149
Table 94. Control Register CR2 . . . 149
Table 95. CR2 signals description . . . 149
Table 96. Configuration of Timer x on-time . . . 151
Table 97. Control Register CR3 . . . 152
Table 98. CR3 signals description . . . 153
Table 99. Control Register CR4 . . . 154
Table 100. CR4 signals description . . . 154

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Table 101. Control Register CR5 . . . 156
Table 102. CR5 signals description . . . 156
Table 103. OUTx Configuration bits . . . 157
Table 104. Control Register CR6 . . . 158
Table 105. CR6 signals description . . . 158
Table 106. Control Register CR7 . . . 159
Table 107. CR7 signals description . . . 159
Table 108. Half-bridge minimum ON time and related overcurrent recovery frequency . . . 160
Table 109. High-side minimum ON time and related overcurrent recovery frequency . . . 160
Table 110. Control Register CR8 . . . 161
Table 111. CR8 signals description . . . 161
Table 112. Control Register CR9 . . . 162
Table 113. CR9 signals description . . . 162
Table 114. Control Register CR10 . . . 163
Table 115. CR10 signals description . . . 163
Table 116. Control Register CR11 . . . 165
Table 117. CR11 signals description . . . 165
Table 118. Control Register CR12 . . . 166
Table 119. CR12 signals description . . . 166
Table 120. Control Register CR13 to CR17 . . . 167
Table 121. CR13 to CR17 signals description . . . 168
Table 122. Control Register CR18 . . . 168
Table 123. CR18 to CR22 signals description . . . 169
Table 124. Control Register CR23 . . . 170
Table 125. CR23 signals description . . . 170
Table 126. Control Register CR24 . . . 170
Table 127. CR24 signals description . . . 170
Table 128. Control Register CR25 . . . 172
Table 129. CR25 signals description . . . 172
Table 130. Control Register CR26 . . . 172
Table 131. CR26 signals description . . . 172
Table 132. Control Register CR27 . . . 173
Table 133. CR27 signals description . . . 173
Table 134. Control Register CR28 . . . 173
Table 135. CR28 signals description . . . 174
Table 136. Control Register CR29 . . . 174
Table 137. CR29 signals description . . . 174
Table 138. Control Register CR34 . . . 174
Table 139. CR34 signals description . . . 175
Table 140. Configuration Register . . . 175
Table 141. CR signals description . . . 175
Table 142. Status Register SR1 (0x31) . . . 178
Table 143. SR1 signals description . . . 178
Table 144. Status Register SR2 (0x32) . . . 180
Table 145. SR2 signals description . . . 180
Table 146. Status Register SR3 (0x33) . . . 182
Table 147. SR3 signals description . . . 183
Table 148. Status Register SR4 (0x34) . . . 184
Table 149. SR4 signals description . . . 184
Table 150. Status Register SR5 (0x35) . . . 185
Table 151. SR5 signals description . . . 186
Table 152. Status Register SR6 (0x36) . . . 187

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Table 153. SR6 signals description . . . 187
Table 154. Status Register SR7 (0x37) to SR9 (0x39) . . . 188
Table 155. SR7 to SR9 signals description . . . 188
Table 156. Status Register SR10 (0x3A) . . . 189
Table 157. SR10 signals description . . . 189
Table 158. Status Register SR11 (0x3B) . . . 190
Table 159. SR11 signals description . . . 190
Table 160. Status Register SR12 (0x3B) . . . 191
Table 161. SR12 signals description . . . 191
Table 162. LQFP-64 mechanical data . . . 193
Table 163. Document revision history . . . 196

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List of figures

Figure 1. Block diagram . . . 15
Figure 2. Pin connection (top view) . . . 19
Figure 3. Activation profile 1 . . . 24
Figure 4. Activation profile 1 (first cycle) . . . 25
Figure 5. Activation profile 2 . . . 26
Figure 6. Activation profile 2 (first cycle) . . . 26
Figure 7. LQFP64 package and PCB thermal configuration . . . 27
Figure 8. Voltage regulator V1 characteristics (quiescent current and accuracy) . . . 31
Figure 9. Watchdog timing . . . 35
Figure 10. Watchdog early, late and safe windows . . . 36
Figure 11. H-driver delay times . . . 47
Figure 12. IGHxr ranges . . . 47
Figure 13. IGHxf ranges . . . 48
Figure 14. LIN transmit, receive timing . . . 61
Figure 15. SPI – transfer timing diagram . . . 66
Figure 16. SPI input timing . . . 67
Figure 17. SPI output timing . . . 68
Figure 18. SPI CSN - output timing . . . 69
Figure 19. SPI – CSN high to low transition and global status bit access . . . 69
Figure 20. Voltage regulator behaviour and diagnosis during supply voltage . . . 72
Figure 21. Sequence to disable/enable the watchdog in CAN Flash mode . . . 73
Figure 22. NINT pins . . . 74
Figure 23. Main operating modes . . . 79
Figure 24. Watchdog in normal operating mode (no errors) . . . 80
Figure 25. Watchdog with error conditions . . . 81
Figure 26. Watchdog in Flash mode . . . 81
Figure 27. NReset pin . . . 84
Figure 28. RxDL pin . . . 85
Figure 29. Wake-up behavior according to LIN 2.2a . . . 86
Figure 30. RxDC pin . . . 87
Figure 31. CAN transceiver state diagram . . . 89
Figure 32. CAN wake up capabilities . . . 91
Figure 33. Thermal shutdown protection and diagnosis . . . 97
Figure 34. Example of long auto-recovery on OUT7. Temperature acquisition starts after t_{AR}, thermal expiration occurs after a $\Delta T = 30°$ . . . 100
Figure 35. Block diagram of physical realization of AR alert and thermal expiration . . . 101
Figure 36. Charge pump low filtering and start up implementation . . . 101
Figure 37. Software strategy for half bridges before applying auto-recovery mode . . . 104
Figure 38. Overcurrent recovery mode . . . 105
Figure 39. H-bridge GSHx slope . . . 107
Figure 40. H-bridge diagnosis . . . 108
Figure 41. H-bridge open-load-detection (no open-load detected) . . . 109
Figure 42. H-bridge open-load-detection (open-load detected) . . . 109
Figure 43. H-bridge open-load-detection (short to ground detected) . . . 110
Figure 44. H-bridge open-load detection (short to V_S detected) . . . 110
Figure 45. PWMH cross current protection time implementation . . . 111
Figure 46. LSx_FSO: low-side driver “passively” turned on, taking supply from output pin (if main supply fails), can guarantee $V_{LSx_FSO} < V_{OUT_max}$ . . . 112

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Figure 47. Safety concept . . . 112
Figure 48. Heater MOSFET open-load and short-circuit to GND detection . . . 113
Figure 49. Electro-chrome control block . . . 115
Figure 50. Thermal clusters identification . . . 117
Figure 51. Block diagram V_S compensation (duty cycle adjustment) module . . . 118
Figure 52. Sequential ADC Read Out for V_{SREG}, V_S, WU and THCL1 ..THCL6 . . . 119
Figure 53. SPI pin description . . . 121
Figure 54. SDO pin . . . 122
Figure 55. SPI signal description . . . 122
Figure 56. SDI Frame . . . 123
Figure 57. SDO frame . . . 125
Figure 58. Window watchdog operation . . . 131
Figure 59. Typical application diagram . . . 134
Figure 60. Timer_x controlled by DIR1 . . . 152
Figure 61. Extended ID and extended ID mask . . . 173
Figure 62. LQFP-64 package dimension . . . 193
Figure 63. LQFP-64 footprint . . . 195
Figure 64. LQFP-64 marking information . . . 195

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1 Description

The L99DZ100G and L99DZ100GP are door zone systems IC providing electronic control modules with enhanced power management power supply functionality, including various standby modes, as well as LIN and HS CAN physical communication layers.

The two low-drop voltage regulators of the devices supply the system microcontroller and external peripheral loads such as sensors and provide enhanced system standby functionality with programmable local and remote wake-up capability. In addition 8 high-side drivers to supply LEDs, 2 high-side drivers to supply bulbs increase the system integration level.

Up to 5 DC motors and 4 external MOS transistors in H-bridge configuration can be driven. An additional gate drive can control an external MOSFET in high-side configuration to supply a resistive load connected to GND (e.g. mirror heater). An electro-chromic mirror glass can be controlled using the integrated SPI-driven module in conjunction with an external MOS transistor. All outputs are SC protected and implement an open-load diagnosis.

The ST standard SPI interface (4.0) allows control and diagnosis of the device and enables generic software development.

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2 Block diagram and pin descriptions

Figure 1. Block diagram

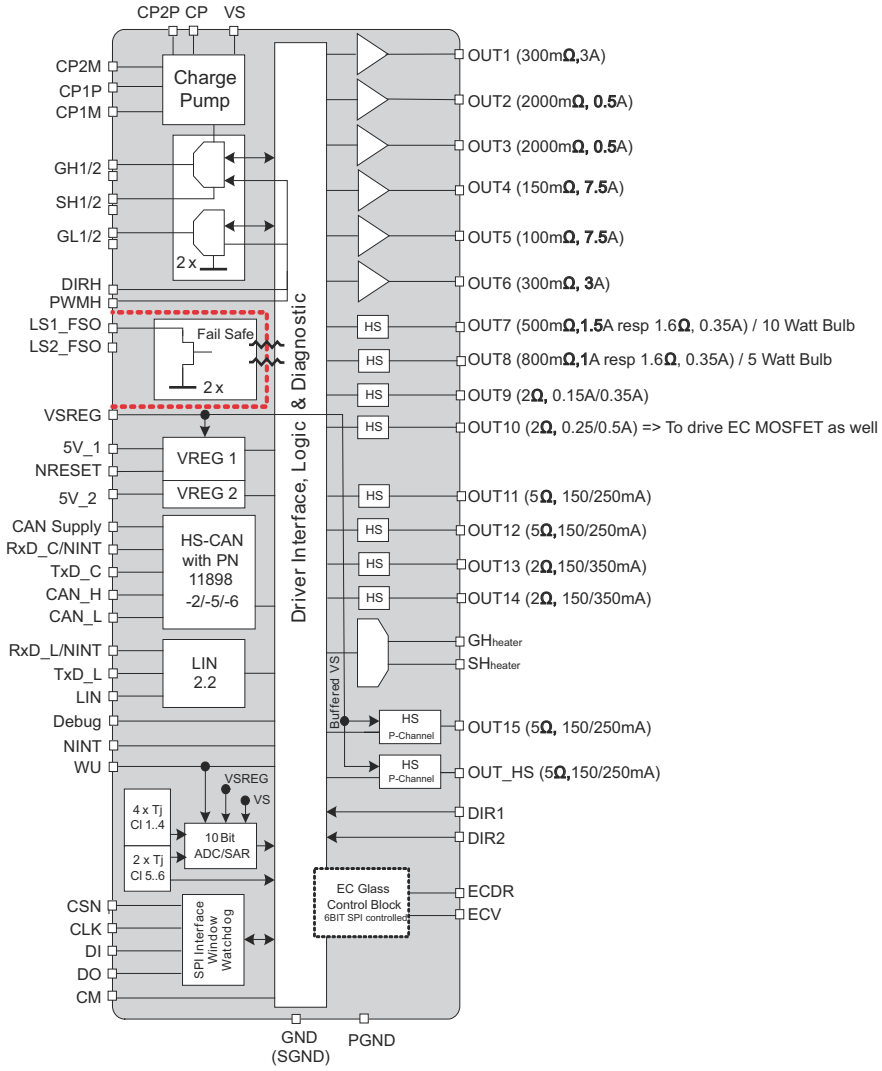


Table 2. Pin definitions and functions

Pin	Symbol	Function
1	WU	Wake-up Input: Input pin for static or cyclic monitoring of external contacts
2	CP2M	Charge pump pin for capacitor 2, negative side
3	CP2P	Charge pump pin for capacitor 2, positive side
4	CP	Charge pump output
5	CP1P	Charge pump pin for capacitor 1, positive side
6	CP1M	Charge pump pin for capacitor 1, negative side

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Table 2. Pin definitions and functions (continued)

Pin	Symbol	Function
7	GHheater	Gate driver for external power N-Channel MOSFET in high-side configuration to control the heater
8	SHheater	Source of high-side MOSFET to control the heater
9	OUT14	High-side-driver output to drive LEDs
10	OUT13	High-side-driver output to drive LEDs
11	OUT12	High-side-driver output to drive LEDs
12	OUT9	High-side-driver output to drive LEDs
13	OUT10	High-side-driver-output; Important: Beside the bits *OUT10_x* (*CR 5*) this output can be switched on setting the *ECON* bit for electro-chrome control mode with higher priority.
14	OUT11	High-side-driver output to drive LEDs
15	LS1_FSO	Fail Safe low-side switch (Active low)
16	LS2_FSO	Fail Safe low-side switch (Active low)
17	VS	Power supply voltage for power stage outputs (external reverse battery protection required), for this input a ceramic capacitor as close as possible to GND is recommended. Important: For the capability of driving, the full current at the outputs all pins of VS must be connected externally!
18	VS; 2nd pin	Current capability (pin description see above)
19	OUT7	High-side-driver output to drive LEDs or a 10 Watt bulb (programmable R_{dson})
20	OUT6	Half-bridge outputs: the output is built by a high-side and a low-side switch which are internally connected. The output stage of both switches is a power DMOS transistor. Each driver has an internal parasitic reverse diode (bulk-drain-diode: high-side driver from output to VS, low-side driver from GND to output)
21	OUT1	Half-bridge outputs: the output is built by a high-side and a low-side switch which are internally connected. The output stage of both switches is a power DMOS transistor. Each driver has an internal parasitic reverse diode (bulk-drain-diode: high-side driver from output to VS, low-side driver from GND to output)
22	OUT2	Half-bridge outputs: the output is built by a high-side and a low-side switch which are internally connected. The output stage of both switches is a power DMOS transistor. Each driver has an internal parasitic reverse diode (bulk-drain-diode: high-side driver from output to VS, low-side driver from GND to output)
23	OUT5	Half-bridge outputs: the output is built by a high-side and a low-side switch which are internally connected. The output stage of both switches is a power DMOS transistor. Each driver has an internal parasitic reverse diode (bulk-drain-diode: high-side driver from output to V_S, low-side driver from GND to output)
24	OUT5; 2nd pin	Current capability (pin description see above)

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Table 2. Pin definitions and functions (continued)

Pin	Symbol	Function
25	V_{SREG}	Power supply voltage to supply the internal voltage regulators, OUT15 and the OUT_HS (external reverse battery protection required / Diode) for this input a ceramic capacitor as close as possible to GND and an electrolytic back up capacitor is recommended.
26	OUT_HS	High-side-driver output to drive LEDs or to supply contacts
27	OUT4	Half-bridge outputs: the output is built by a high-side and a low-side switch which are internally connected. The output stage of both switches is a power DMOS transistor. Each driver has an internal parasitic reverse diode (bulk-drain-diode: high-side driver from output to V_S, low-side driver from GND to output)
28	OUT4; 2nd pin	Current capability (pin description see above)
29	OUT3	Half-bridge outputs: the output is built by a high-side and a low-side switch which are internally connected. The output stage of both switches is a power DMOS transistor. Each driver has an internal parasitic reverse diode (bulk-drain-diode: high-side driver from output to V_S, low-side driver from GND to output)
30	VS; 3rd pin	Current capability (for the pin description see above)
31	OUT15	High-side-driver output to drive LEDs
32	PGND	Power GND
33	OUT8	High-side-driver output to drive LEDs or a 5 Watt bulb (programmable R_{dson})
34	ECDR	ECDR: using the device in EC control mode this pin is used to control the gate of an external N-Channel MOSFET
35	SGND	Signal Ground
36	CM	Current monitor output: depending on the selected multiplexer bits *CM_SEL_x* (*CR 7*) of the; Control Register this output sources an image of the instant current; through the corresponding high-side driver with a fixed ratio
37	ECV	ECV: using the device in EC control mode this pin is used as voltage monitor input. For fast discharge an additional low-side-switch is implemented
38	CLK	SPI: serial clock input
39	DO	SPI: serial data output (push pull output stage)
40	DI	SPI: serial data input
41	CSN	SPI: chip select not input
42	TxD_L	LIN Transmit data input
43	RxD_L/NINT	RxDL -> LIN receive data output; NINT -> indicates local/remote wake-up events (push pull output stage)
44	TxD_C	CAN transmit data input
45	RxD_C/NINT	CAN receive data output NINT -> indicates local/remote wake-up events (push pull output stage)
46	DIR1	Direct Drive Input 1

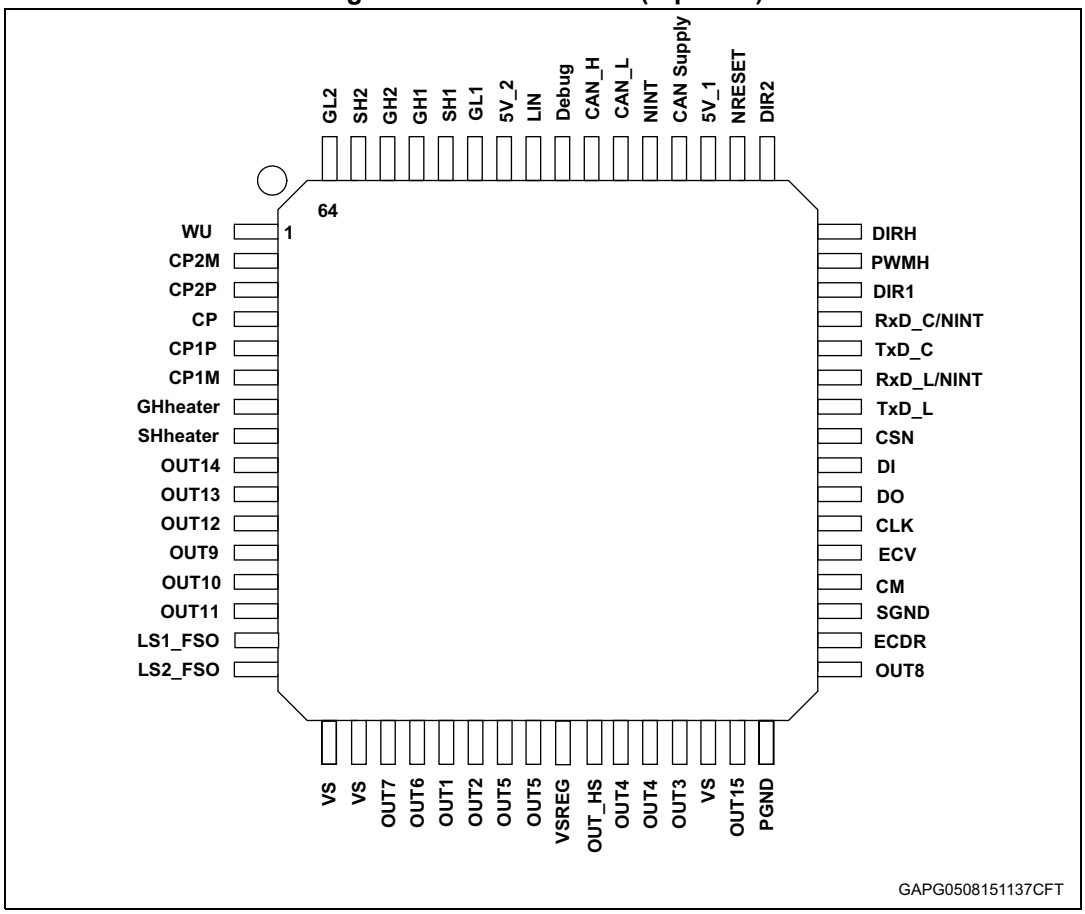
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Table 2. Pin definitions and functions (continued)

Pin	Symbol	Function
47	PWMH	PWMH input: this input signal can be used to control the H-bridge Gate Drivers.
48	DIRH	Direction Input: this input controls the H-bridge Drivers for the external MOSFETs
49	DIR2	Direct Drive Input 2
50	NRESET	NReset output to micro controller; (reset state = LOW) (Low-side switch with drain connected to the output pin and internal pull up resistance to 5V_1)
51	5V_1	Voltage regulator 1 output: 5 V supply e.g. micro controller, CAN transceiver
52	CAN Supply	CAN supply input; to allow external CAN supply from V_1 or V_2 regulator
53	NINT	Interrupt output (low active; push-pull output stage) to indicate V_{SREG} early warning (Active mode); indicates wake-up events from V1_standby mode
54	CAN_L	CAN low level voltage I/O
55	CAN_H	CAN high level voltage I/O
56	Debug	Debug input to deactivate the window watchdog (high active)
57	LIN	LIN bus line
58	5V_2	Voltage regulator 2 output: 5 V supply for external loads (potentiometer, sensors) or CAN Transceiver. V_2 is protected against reverse supply
59	GL1	Gate driver for PowerMOS low-side switch in half-bridge 1
60	SH1	Source of high-side switch in half-bridge 1
61	GH1	Gate driver for PowerMOS high-side switch in half-bridge 1
62	GH2	Gate driver for PowerMOS high-side switch in half-bridge 2
63	SH2	Source of high-side switch in half-bridge 2
64	GL2	Gate driver for PowerMOS low-side switch in half-bridge 2

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Figure 2. Pin connection (top view)



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3 Electrical specifications

3.1 Absolute maximum ratings

Stressing the device above the rating listed in *Table 3* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability

Table 3. Absolute maximum ratings

Symbol	Parameter / test condition	Value [DC voltage]	Unit
V_S, V_{SREG}	DC supply voltage / “jump start”	-0.3 to +28	V
	Load dump	-0.3 to +40	V
5V_1	Stabilized supply voltage, logic supply	-0.3 to 6.5 V1 < V_{SREG}	V
5V_2(1)	Stabilized supply voltage	-0.3 to +28(2)	V
V_{DI}, V_{CLK} V_{CSN} V_{DO}, $V_{RXDL/NINT}$, V_{RXDC}, V_{NRESET}, V_{CM}, V_{DIR}, V_{DIR2}, V_{PWMH}, V_{DIRH}, V_{INT}	Logic input / output voltage range	-0.3 to V1+0.3	V
V_{TXDC}, V_{TXDL}	Multi Level Inputs	-0.3 to 40	V
V_{Debug}	Debug input pin voltage range	-0.3 to 40	V
V_{LS1_FSO}, V_{LS2_FSO}	Output voltage range of Fail-Safe Low-side Switches	-0.3 to 35	V
V_{WU}	DC Wake up input voltage / “jump start”	-0.3 to +28	V
	Load dump	-0.3 to +40	V
V_{LIN}	LIN bus I/O voltage range	-20 to +40	V
I_{Input}(3)	Current injection into V_S related input pins	20	mA
I_{OUT_INJ}(3)	Current injection into V_S related outputs	20	mA
V_{CANSUP}	CAN supply	-0.3 to +5.25	V
V_{CANH}, V_{CANL}	CAN bus I/O voltage range	-27 to +40	V
V_{CANH} - V_{CANL}	Differential CAN-Bus Voltage	-5 to +10	V
V_{OUTn}, V_{ECDR}, V_{ECV}, V_{out_HS}	Output voltage (n = 1 to 15)	-0.3 to V_S+0.3	V
V_{GH1}, V_{GH2} (V_{Gxy})	High Voltage Signal Pins	V_{Sxy}-0.3 to V_{Sxy}+13; V_{CP}+0.3	V
V_{GL1}, V_{GL2}, (V_{Gxy})	High Voltage Signal Pins	V_{Sxy}-0.3 to V_{Sxy}+13; V_{CP}-0.3V to +12V; Vcp+0.3V	V

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Table 3. Absolute maximum ratings (continued)

Symbol	Parameter / test condition	Value [DC voltage]	Unit
V_{SH1}, V_{SH2} (V_{Sxy})	High Voltage Signal Pins	-1 to 40	V
	High Voltage Signal Pins; single pulse with t_{max} = 200ns	-5 to 40	V
V_{CP1P}	High Voltage Signal Pins	V_S-0.3 to V_S+14	V
V_{CP2P}	High Voltage Signal Pins	V_S-0.6 to V_S+14	V
V_{CP1M}, V_{CP2M}	High Voltage Signal Pins	-0.3 to V_S+0.3	V
V_{CP}	High Voltage Signal Pin $V_S \leq 26$ V	V_S-0.3 to V_S+14	V
	High Voltage Signal Pin $V_S > 26$ V	V_S-0.3 to +40	V
V_{GH_heater}		$V_{Sheater}$ -0.3 to $V_{Sheater}$+13; V_{CP}+0.3	V
V_{SH_heater}		-0.3 to 40V Or -0.3 to Vs+0.3	V
ISH_Heater		+/-10	mA
I_{ECV}, I_{OUT2}, I_{OUT3}, I_{OUT9}, I_{OUT10}, I_{OUT11}, I_{OUT12}, I_{OUT13}, I_{OUT14}, I_{OUT15}, I_{OUT_HS}	Output current(2)	±1.25	A
I_{OUT8}		±2.5	A
I_{OUT7}		±5	A
$I_{OUT1,6}$		±5	A
$I_{OUT4,5}$		±10	A
I_{VScum}	Maximum cumulated current at V_S drawn by OUT1 & OUT2(2)	±7.5	A
I_{VScum}	Maximum cumulated current at V_S drawn by OUT3, OUT8 & OUT10(2)	±2.5	A
I_{VScum}	Maximum cumulated current at V_S drawn by OUT4(2)	±10	A
I_{VScum}	Maximum cumulated current at V_S drawn by OUT5(2)	±10	A
I_{VScum}	Maximum cumulated current at V_S drawn by OUT6 & OUT7(2)	±7.5	A
I_{VScum}	Maximum cumulated current at V_S drawn by OUT9, OUT11, OUT12, OUT13, OUT14, OUT15 and CP	±2.5	A
I_{VSREG}	Maximum current at V_{SREG} pin (2) (5V_1. 5V_2 and OUT_HS)	±2.5	A
$I_{PGNDcum}$	Maximum cumulated current at PGND drawn by OUT1 & OUT6(2)	±7.5	A

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Table 3. Absolute maximum ratings (continued)

Symbol	Parameter / test condition	Value [DC voltage]	Unit
$I_{PGNDcum}$	Maximum cumulated current at PGND drawn by OUT2 & OUT5(2)	±12.5	A
$I_{PGNDcum}$	Maximum cumulated current at PGND drawn by OUT3, OUT4 & ECV(2)	±12.5	A
I_{SGND}	Maximum current at SGND(2)	±1.25	A
GND pins	PGND versus SGND	-0.3 to 0.3	V

1. 5V_2 is robust against SC to 28 V only in case V_{SREG} is supplied.
2. Values for the absolute maximum DC current through the bond wires. This value does not consider maximum power dissipation or other limits.
3. Guaranteed by design.

Note: All maximum ratings are absolute ratings. Leaving the limitation of any of these values may cause an irreversible damage of the integrated circuit!

Note: Loss of ground or ground shift with externally grounded loads: ESD structures are configured for nominal currents only. If external loads are connected to different grounds, the current load must be limited to this nominal current.

3.2 ESD protection

Table 4. ESD protection

Parameter	Value	Unit
All pins(1)	+/-2	kV
All power output pins (2): OUT1 – OUT15, OUT_HS, ECV	+/-4	kV
LIN	+/-8(2) +/-9(3) (4) +/-6(5)	kV
CAN_H, CAN_L	+/-8(2) +/-6(5) (4)	kV
All pins(6)	+/-500	V
Corner pins(6)	+/-750	V
All pins(7)	+/- 200	V

1. HBM (human body model, 100 pF, 1.5 kΩ) according to MIL 883C, Method 3015.7 or EIA/JESD22A114-A.
2. HBM with all none zapped pins grounded.
3. Indirect ESD Test according to IEC 61000-4-2 (150 pF, 330 Ω) and ‘Hardware Requirements for LIN, CAN and Flexray Interfaces in Automotive Applications’ (version 1.3, 2012-05-04).
4. Value has been verified by an external test house; the result was equal or better than minimum requirement.
5. Direct ESD Test according to IEC 61000-4-2 (150 pF, 330 Ω) and ‘Hardware Requirements for LIN, CAN and Flexray Interfaces in Automotive Applications’ (version 1.3, 2012-05-04).
6. Charged device model.
7. Machine model; C = 220 pF, R = 0 Ω.

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3.3 Thermal data

Table 5. Operating junction temperature

Symbol	Parameter	Value	Unit
T_j	Operating junction temperature	-40 to 175	°C

All parameters are guaranteed in the junction temperature range -40 to 150°C (unless otherwise specified); the device is still operative and functional at higher temperatures (up to 175°C).

Note: Parameters limits at higher junction temperatures than 150°C may change respect to what is specified as per the standard temperature range.

Note: Device functionality at high junction temperature is guaranteed by characterization.

Table 6. Temperature warning and thermal shutdown

Symbol	Parameter		Min.	Typ.	Max.	Unit
T_W	Thermal overtemperature warning threshold	T_j(1)	140	150	160	°C
T_{SD1}	Thermal shutdown junction temperature 1	T_j(1) Cluster 1-4 Cluster 5-6	 165 165	 175 175	 185 190	°C
T_{SD2}	Thermal shutdown junction temperature 2	T_j(1)	175	185	195	°C
$T_{SD12hys}$		Hysteresis		5		°C
T_{jtft}	Thermal warning / shutdown filter time			32		µs

1. Non-overlapping.

3.3.1 LQFP64 thermal data

Devices belonging to L99DZxxx family embed a multitude of junctions (i.e. Outputs based on a PowerMOSFET stage) housed in a relatively small piece of silicon. The devices contain, among all the described features, 6 Half-bridges (12 N-Channel PowerMOS), 10 high-sides and two voltage regulators; all the other derivatives, even if smaller than the family super set device, still contain a significant number of junctions.

For this reason, using the Thermal Impedance of a single junction (i.e. voltage regulator or major power dissipation contributor) does not allow to predict thermal behavior of the whole device and therefore it is not possible to assess if a device is thermally suitable for a given activation profile and loads characteristics.

Thermal information is provided as temperature reading by different clusters placed close to the most dissipative junctions.

Some representative and realistic worst-case thermal profiles are described in the below paragraph.

Following measurement methods can be easily implemented, by final user, for a specific activation profile.

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L99DZ100G and L99DZ100GP thermal profiles

Profile 1

Battery Voltage: 16V, Ambient temperature start: 85°C

DC activation

- V1 charged with 70 mA (DC activation)
- V2 charged with 30 mA (DC activation)
- OUT7: 1 x10W bulb (DC activation)
- OUT8: 1 x 5W bulb (DC activation)
- OUT11: 300 Ω resistor (DC activation)
- OUT12: 300 Ω resistor (DC activation)
- OUT13: 300 Ω resistor (DC activation)
- OUT14: 300 Ω resistor (DC activation)

Cyclic activation

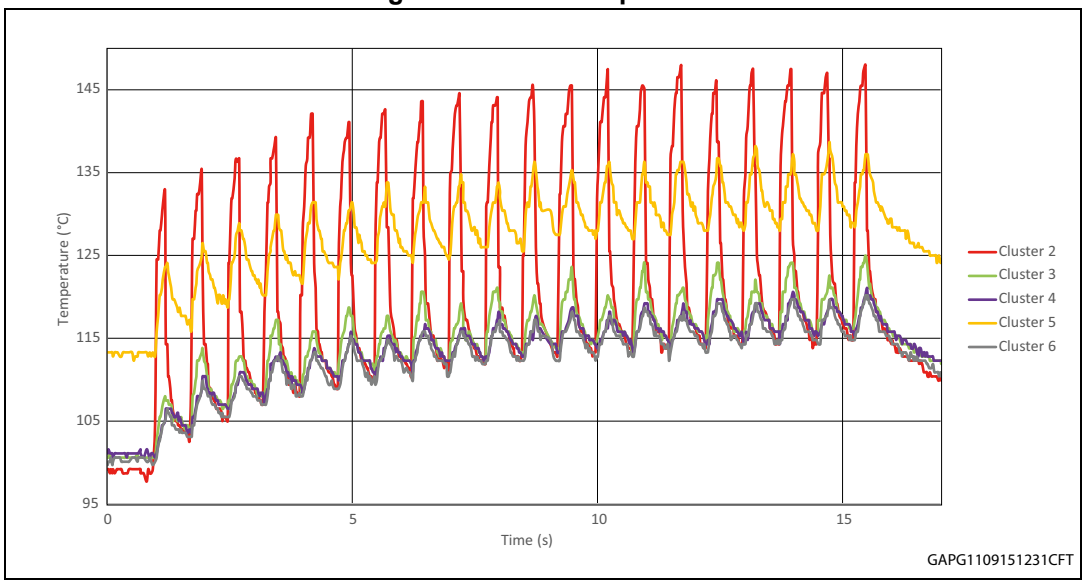
- OUT4 – OUT5: 3,3 Ω resistor placed across those outputs
  - 10 activations of Lock/Un-lock (250 ms ON Lock; 500 ms wait; 250 ms ON Un-lock unlock; 500 ms wait)
- OUT5 – OUT6: 10 Ω resistor placed across those outputs
  - (250 ms ON Safe Lock; 500 ms wait; 250 ms ON Safe unlock; 500 ms wait)

Test execution:

Once thermal equilibrium is reached with all DC load active, the “Cyclic Activation” sequence is applied.

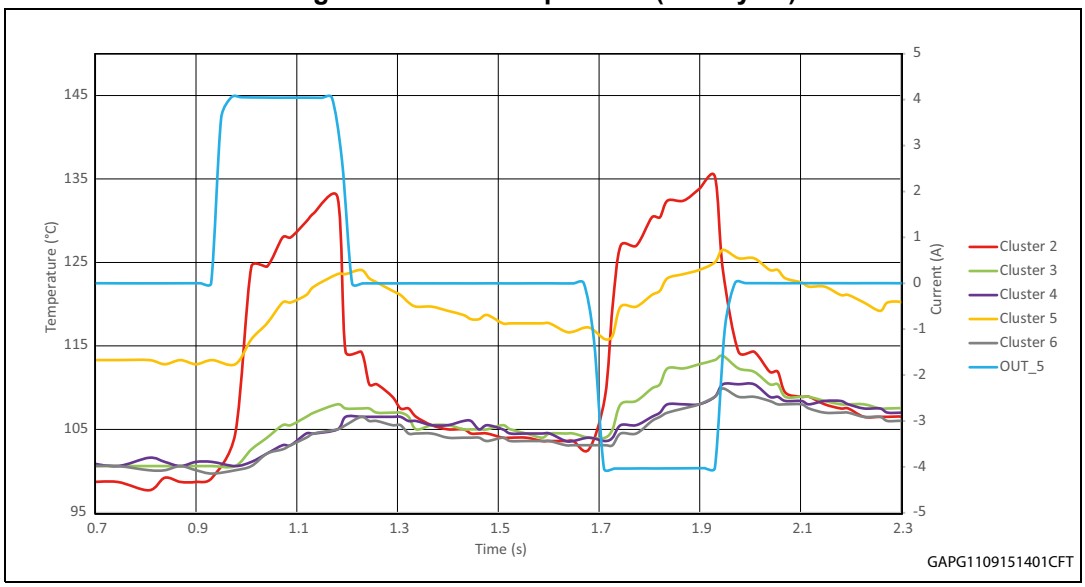
Temperature reading is logged just at the end of the whole sequence.

Figure 3. Activation profile 1



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Figure 4. Activation profile 1 (first cycle)



Note: All curves are plotted interpolating measured samples with 15 ms of period.

Profile 2

Battery Voltage: 16V, Ambient temperature start: 85°C

DC activation

- V1 charged with 70 mA (DC activation)
- V2 charged with 30 mA (DC activation)
- OUT7: 1 x10W bulb (DC activation)
- OUT8: 1 x 5W bulb (DC activation)
- OUT11: 300 Ω resistor (DC activation)
- OUT12: 300 Ω resistor (DC activation)
- OUT13: 300 Ω resistor (DC activation
- OUT14: 300 Ω resistor (DC activation)

Cyclic activation

- OUT1 – OUT6: 6,8 Ω resistor placed across those outputs
  - 2 activations of Fold/Unfold. (3s ON; 1s OFF; 2x)

Test execution:

Once thermal equilibrium is reached with all DC load active, the “Cyclic Activation” sequence is applied.

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Figure 5. Activation profile 2

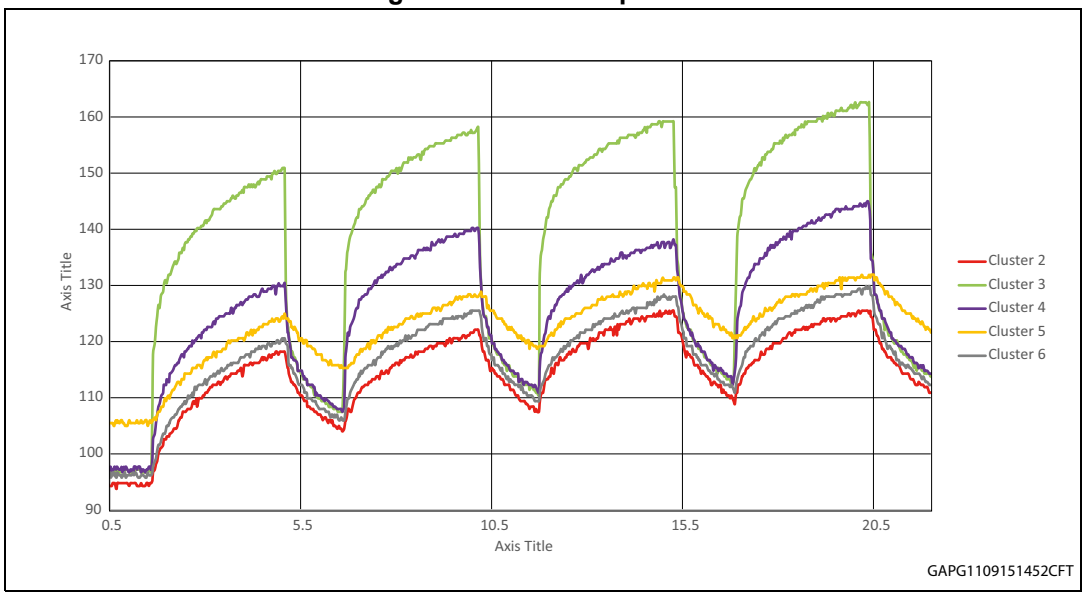
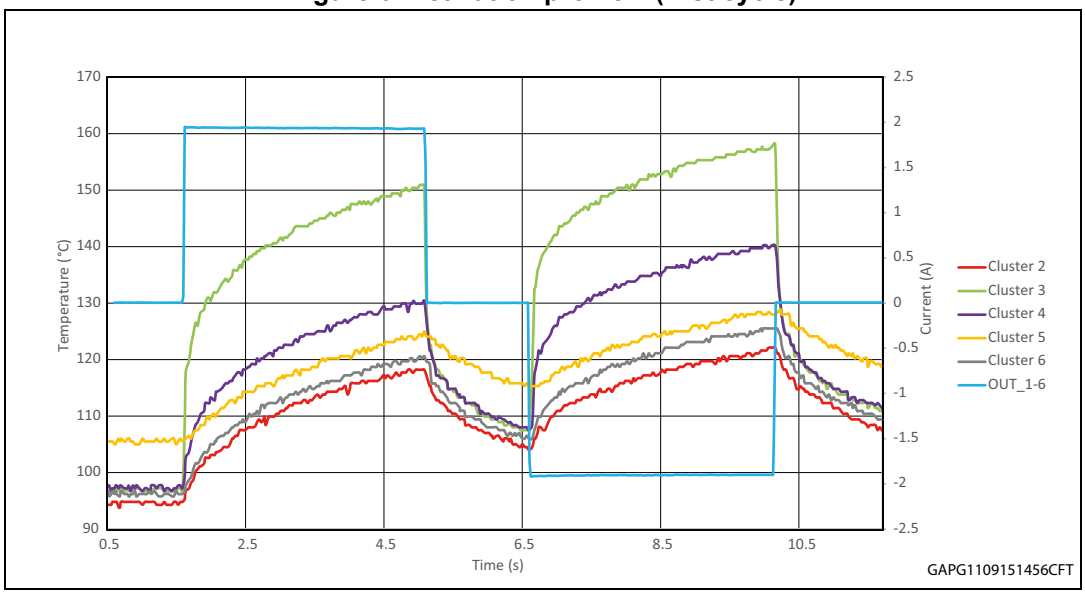


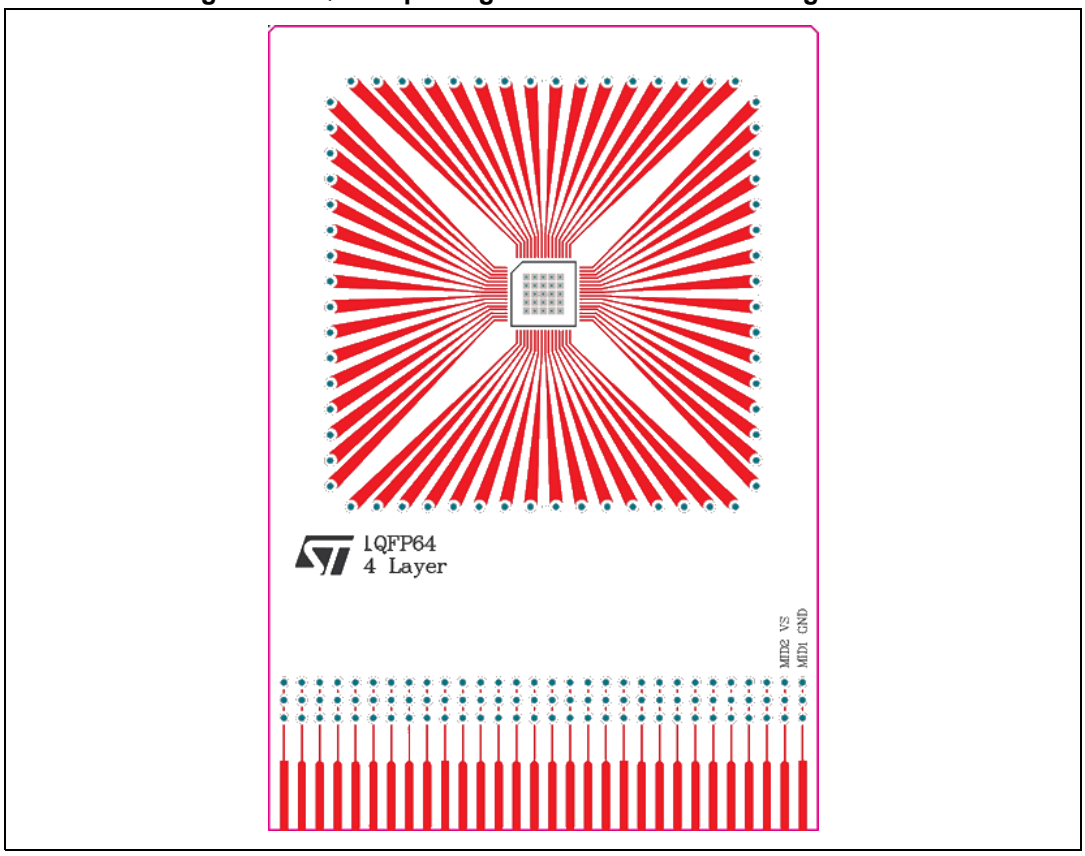
Figure 6. Activation profile 2 (first cycle)



Note: All curves are plotted interpolating measured samples with 15 ms of period.

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Figure 7. LQFP64 package and PCB thermal configuration



Note: Layout condition for Thermal Characterization (board finishing thickness 1.5 mm +/- 10%, board four layers, board dimension 77 mm x 114 mm, board material FR4, Cu thickness 0,070 mm for outer layers, 0.0035 mm for inner layers, thermal vias separation 1.2 mm.

3.4 Electrical characteristics

3.4.1 Supply and supply monitoring

All SPI communication, logic and oscillator parameter are working down to V_{SREG} = 3.5 V and parameter are as specified in the according chapters (guaranteed by design).

- SPI thresholds
- Oscillator frequency (delay times correctly elapsed)
- Internal register status correctly kept (reset at default values for $V_{SREG} < V_{POR}$)
- Reset threshold correctly detected

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 6 V ≤ V_S ≤ 28 V; 6 V ≤ V_{SREG} ≤ 28 V; T_j = -40 °C to 150 °C, unless otherwise specified.

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Table 7. Supply and supply monitoring

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{SUV}	V_S undervoltage threshold	V_S increasing / decreasing	4.7		5.4	V
V_{hyst_UV}	V_S undervoltage hysteresis		0.04	0.1	0.2	V
V_{SOV}	V_S overvoltage threshold	V_S increasing	20		22.5	V
		V_S decreasing	18.5		22.5	
V_{hyst_OV}	V_S overvoltage hysteresis		0.5	1	1.5	V
V_{SREG_UV}	V_{SREG} undervoltage threshold	V_{SREG} increasing / decreasing	4.2		4.9	V
V_{hyst_UV}	V_{SREG} undervoltage hysteresis		0.04	0.1	0.2	V
V_{SREG_OV}	V_{SREG} overvoltage threshold	V_{SREG} increasing	20		22.5	V
		V_{SREG} decreasing	18.5		22.5	
V_{hyst_OV}	V_{SREG} overvoltage hysteresis		0.5	1	1.5	V
t_{ovuv_filt}	V_S/V_{SREG} over/undervoltage filter time			64		µs
$I_{V(act)}$	Current consumption in Active mode	V_S = V_{SREG} = 12 V; TxD CAN = high; TxD LIN = high; V1 = ON; V2 = ON; HS/LS Driver OFF; CP = ON		11	15	mA
$I_{V(BAT)}$	Current consumption in V_{bat}_standby mode (1)	V_S = 12 V; Both voltage regulators deactivated; HS/LS Driver OFF; No CAN communication; CAN automatic voltage biasing enabled	8	21	35	µA
$I_{V(BAT)CS}$	Current consumption in V_{bat}_standby mode with cyclic sense enabled (1)	V_S = 12 V; Both voltage regulators deactivated; T = 50 ms, t_{ON} = 100 µs	40	100	143	µA
$I_{V(BAT)CW}$	Current consumption in V_{bat}_standby mode with cyclic wake enabled (1)	V_S = 12 V; Both voltage regulators deactivated during standby phase	40	100	143	µA
$I_{V(V1stby)}$	Current consumption in V_1_standby mode (1)	V_S = 12 V; Voltage regulator V1 active; (I_{V1} = 0); HS/LS Driver OFF	16	56	76	µA
	Current consumption in V_1_standby mode (1) (2)	V_S = 12 V; Voltage regulator V1 active; (I_{V1} = I_{CMP}); HS/LS Driver OFF			196	µA
	Current consumption in V_1_standby mode (1)	V_S = 12V; Voltage regulator V1 active; (I_{V1} = I_{PEAK}); HS/LS Driver OFF			436	µA
$I_{V(SW)}$	Current consumption adder in standby mode if Selective Wakeup enabled and CAN communication on the bus TRX_BIAS mode (1)	V_S = 12 V		1570	2000	µA

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Table 7. Supply and supply monitoring (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{qCAN}	Quiescent current adder for CAN wake up activated	Guaranteed by design		0		µA
I_{qLIN}	Quiescent current adder for LIN wake up activated	Guaranteed by design		0		µA
I_{OUT_HS}	Additional bias quiescent current for switched on OUT_HS or OUT15 by DIR or Timer; value for 1 output	Guaranteed by design		620	1100	µA
I_{OUTHS_DIR}	Quiescent current adder if OUT_HS and/or OUT15 are configured for Direct Drive; value during output off	Guaranteed by design		0	5	µA
I_{timer}	Quiescent current adder if timer1 and/or timer 2 are active to provide interrupt on NINT upon timer expiration	Guaranteed by design		65	110	µA

1. Conditions for specified current consumption:
   — $V_{LIN} > (V_S\text{-}1.5\ V)$
   — $(V_{CAN_H} - V_{CAN_L}) < 0.4\ V$ or $(V_{CAN_H} - V_{CAN_L}) > 1.2\ V$
   — $V_{WU} < 1\ V$ or $V_{WU} > (V_S - 1.5\ V)$
2. $I_q = I_{q0} + 2\% * I_{LOAD}$ (see also *Figure 8: Voltage regulator V1 characteristics (quiescent current and accuracy)*

3.4.2 Oscillator

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 6 V ≤ V_S ≤ 28 V; 6 V ≤ V_{SREG} ≤ 28 V; T_j = -40 °C to 150 °C, unless otherwise specified.

Table 8. Oscillator

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
f_{CLK1}(1)	Oscillation frequency OSC1		1.66	2.0	2.34	MHz
f_{CLK2}(1)	Oscillation frequency OSC2		30.4	32.0	33.6	MHz

1. OSC1: charge pump, SPI, output drivers, watchdog
   OSC2: ADC, CAN-PN

3.4.3 Power-on reset (V_{SREG})

All outputs open; T_j = -40 °C to 150 °C, unless otherwise specified.

Table 9. Power-on reset (V_{SREG})

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{POR_R}	V_{POR} threshold	V_{SREG} rising		3.45	4.5	V
V_{POR_F}	V_{POR} threshold	V_{SREG} falling(1)	2.45		3.5	V

1. This threshold is valid if V_{SREG} had already reached $V_{POR_R(max)}$ previously.

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3.4.4 Voltage regulator V1

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 4.5 V ≤ V_S ≤ 28 V; 4.5 V ≤ V_{SREG} ≤ 28 V; T_j = -40 °C to 150 °C, unless otherwise specified.

Table 10. Voltage regulator V1

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V1	Output voltage	V_{SREG} = 13.5V		5.0		V
V_{SREG_absmin}	V_{SREG} absolute minimum value for controlling NRESET output	V_{SREG} rising/falling			2	V
$V1_{_low_acc}$	Output voltage tolerance Low accuracy mode	I_{LOAD} = 0 mA to I_{CMP}; (Active mode) or I_{LOAD} = 0 mA to I_{PEAK} (V1stdby); V_{SREG} = 13.5 V	-3		3	%
$V1_{_hi_acc}$	Output voltage tolerance High accuracy mode	I_{LOAD} = I_{CMP} to 100 mA; (Active mode) or I_{LOAD} = I_{PEAK} to 100 mA (V1stdby); V_{SREG} = 13.5 V	-2		2	%
$V1_{_250mA}$	Output voltage tolerance (100 to 250mA)	I_{LOAD} = 250 mA; V_{SREG} = 13.5 V	-3		3	%
V_{DP1}	Drop-out Voltage	I_{LOAD} = 50 mA; V_{SREG} = 5 V		0.2	0.4	V
		I_{LOAD} = 100 mA; V_{SREG} = 5 V		0.3	0.5	V
		I_{LOAD} = 150 mA; V_{SREG} = 5 V		0.45	0.6	V
I_{CC1}	Output current in Active mode	Max. continuous load current			250	mA
I_{CCmax1}	Short circuit output current	Current limitation	340	600	900	mA
C_{load1}	Load capacitor1	Ceramic (+/- 20%)	0.22(1)			µF
t_{TSD}	V1 deactivation time after thermal shut-down			1		sec
I_{CMP_ris}	Current comp. rising thresh	Rising current	2	4	6	mA
I_{CMP_fal}	Current comp. falling threshold	Falling current	1.4	2.8	4.2	mA
I_{CMP_hys}	Current comp. Hysteresis			1.2		mA
I_{Peak_ris}(2)	Current comp. rising thresh.	Rising current	6	12	18	mA
I_{Peak_fal}(2)	Current comp. falling threshold	Falling current	5	10	15	mA
I_{Peak_hys}(2)	Current comp. Hysteresis			2		mA

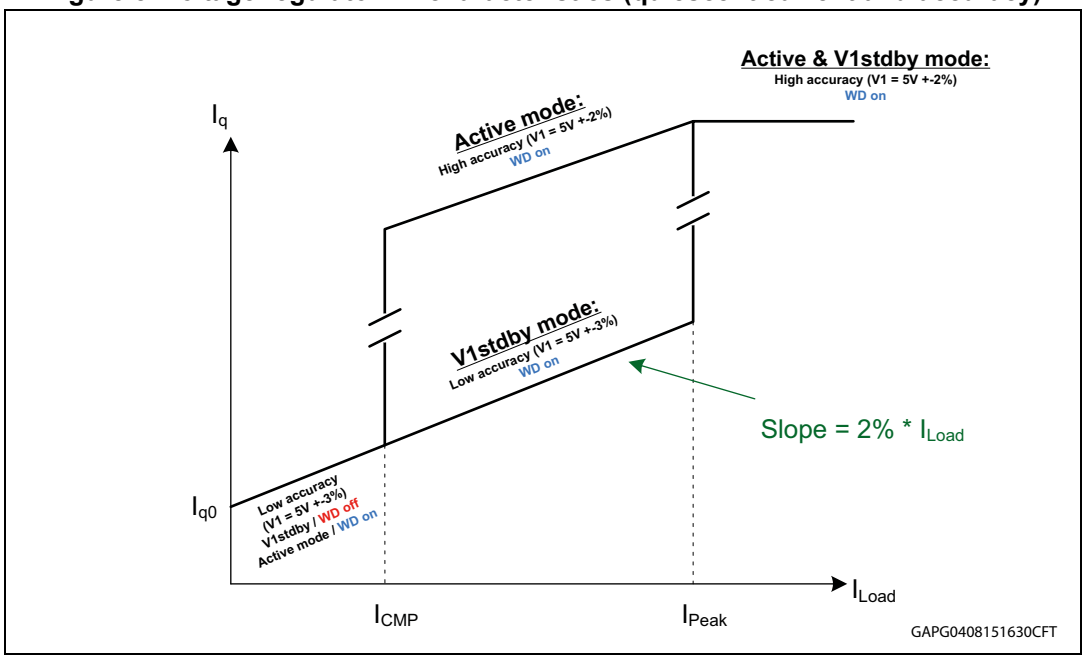
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Table 10. Voltage regulator V1 (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V1_{fail}$	V1 fail threshold	V1 forced		2		V
t_{V1fail}	V1 fail filter time			2		µs
$t_{V1short}$	V1 short filter time			4		ms
t_{V1FS}	V1 Fail-Safe Filter Time			2		ms
t_{V1off}	V1 deactivation time after 8 consecutive WD failures	Tested by scan	150	200	250	ms

1. Nominal capacitor value required for stability of the regulator. Tested with 220 nF ceramic (+/- 20%). Capacitor must be located close to the regulator output pin. A 2.2 µF capacitor is recommended to minimize the DPI stress in the application.
2. In Active mode, V1 regulator is switched to high accuracy mode, dropping below the I_{CMP} threshold regulator switches to low accuracy mode.

Figure 8. Voltage regulator V1 characteristics (quiescent current and accuracy)



3.4.5 Voltage regulator V2

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 4.5 V ≤ V_S ≤ 28 V; 4.5 V ≤ V_{SREG} ≤ 28 V; T_j = -40 °C to 150 °C, unless otherwise specified.

Table 11. Voltage regulator V2

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V2	Output voltage	V_{SREG} = 13.5 V		5.0		V
$V2_{_1mA}$	Output voltage tolerance (0 to 1 mA)	I_{LOAD} = 1 mA; V_{SREG} = 13.5 V	-6.5		6.5	%

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Table 11. Voltage regulator V2 (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V2_{_25mA}$	Output voltage tolerance (1 to 25 mA)	I_{LOAD} = 25 mA; V_{SREG} = 13.5 V	-3		3	%
$V2_{_50mA}$	Output voltage tolerance (25 to 50 mA)	I_{LOAD} = 50 mA; V_{SREG} = 13.5 V	-4		4	%
$V2_{_100mA}$	Output voltage tolerance (50 to 100 mA)	I_{LOAD} = 100 mA; V_{SREG} = 13.5 V	-4		4	%
V_{DP2}	Drop-out voltage	I_{LOAD} = 25 mA; V_{SREG} = 5.25 V		0.3	0.4	V
		I_{LOAD} = 50 mA; V_{SREG} = 5.25 V		0.4	0.8	V
		I_{LOAD} = 100 mA; V_{SREG} = 13.5 V		1	1.6	V
I_{CC2}	Output current in Active mode	Max. continuous load current			50	mA
I_{CCmax2}	Short circuit output current	Current limitation	100	150	250	mA
C_{load}	Load capacitor	Ceramic (+/- 20%)	0.22 (1)			µF
$V2_{fail}$	V2 fail threshold	V2 forced		2		V
t_{V2fail}	V2 fail filter time			2		µs
$t_{V2short}$	V2 short filter time			4		ms

1. Nominal capacitor value required for stability of the regulator. Tested with 220 nF ceramic (+/- 20%). Capacitor must be located close to the regulator output pin. A 2.2 µF capacitor is recommended to minimize the DPI stress in the application.

3.4.6 Reset output

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 4V ≤ V_{SREG} ≤ 28V; T_j = -40 °C to 150 °C, unless otherwise specified.

Table 12. Reset output

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{RT1falling}$	Reset threshold voltage1	V_{V1} decreasing	3.25	3.5	3.7	V
$V_{RT2falling}$	Reset threshold voltage2	V_{V1} decreasing	3.55	3.8	4	V
$V_{RT3falling}$	Reset threshold voltage3	V_{V1} decreasing	3.75	4.0	4.2	V
$V_{RT4falling}$	Reset threshold voltage4	V_{V1} decreasing	4.1	4.3	4.5	V
$V_{RTrising}$	Reset threshold voltage4	V_{V1} increasing	4.67	4.8	4.87	V
V_{RESET}	Reset Pin low output voltage	V1 > 1 V; I_{RESET} = 5 mA		0.2	0.4	V
R_{RESET}	Reset pull up int. resistor		10	20	30	kΩ

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Table 12. Reset output (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
t_{RR}	Reset reaction time	I_{LOAD} = 1 mA	6		40	µs
t_{UV1}	V1 undervoltage filter time			16		µs
t_{V1R}	Reset pulse duration (V1 undervoltage and V1 power on reset)		1.5	2.0	2.5	ms
t_{WDR}	Reset pulse duration (watchdog failure)		3	4	5	ms

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3.4.7 Watchdog timing

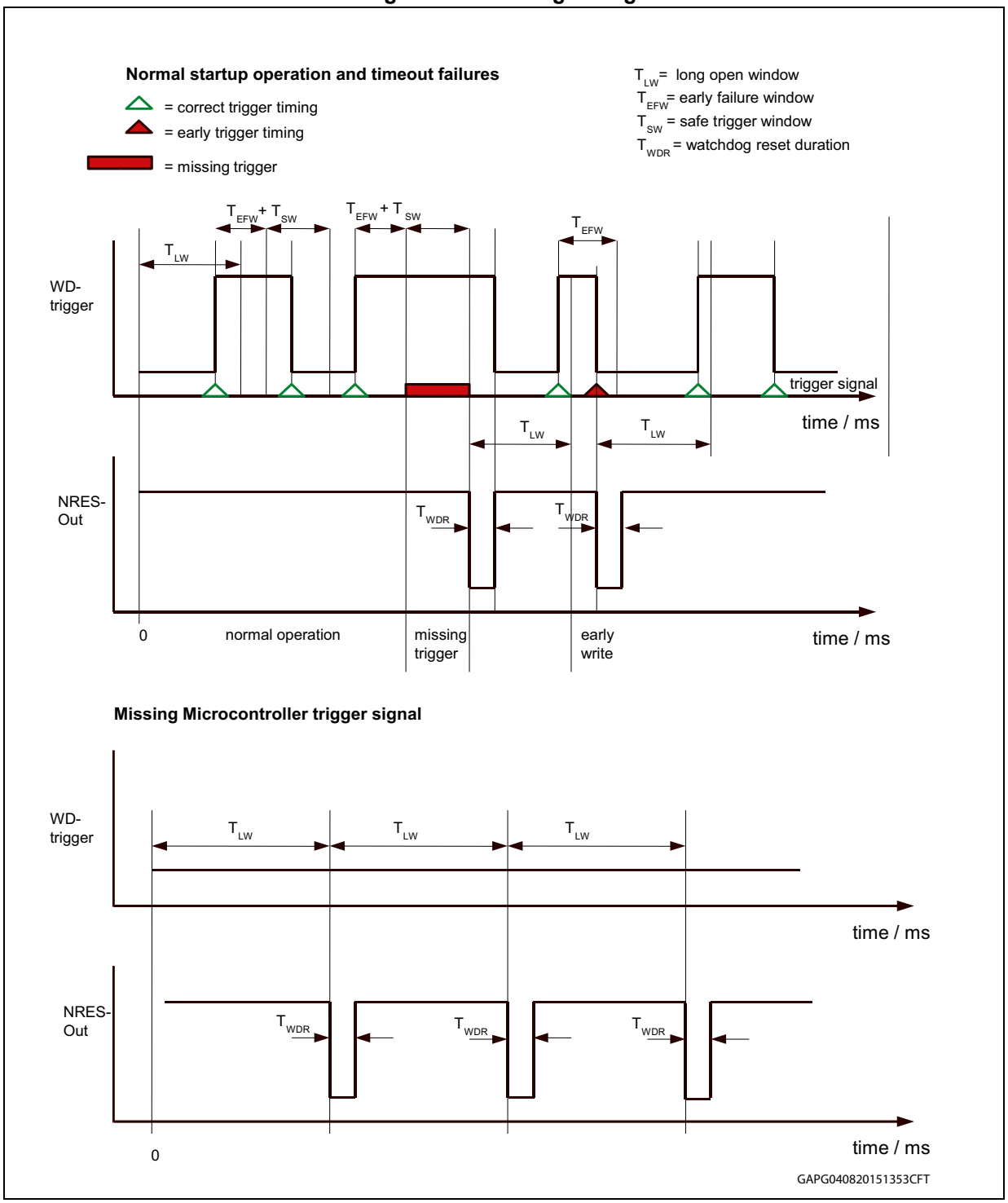
4.5 V ≤ V_{SREG} ≤ 28 V; T_j = -40 °C to 150 °C, unless otherwise specified.

Table 13. Watchdog timing

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
t_{LW}	Long open window		160	200	240	ms
T_{EFW1}	Early Failure Window 1				4.5	ms
T_{LFW1}	Late Failure Window 1		20			ms
T_{SW1}	Safe Window 1		7.5		12	ms
T_{EFW2}	Early Failure Window 2				22.3	ms
T_{LFW2}	Late Failure Window 2		100			ms
T_{SW2}	Safe Window 2		37.5		60	ms
T_{EFW3}	Early Failure Window 3				45	ms
T_{LFW3}	Late Failure Window 3		200			ms
T_{SW3}	Safe Window 3		75		120	ms
T_{EFW4}	Early Failure Window 4				90	ms
T_{LFW4}	Late Failure Window 4		400			ms
T_{SW4}	Safe Window 4		150		240	ms

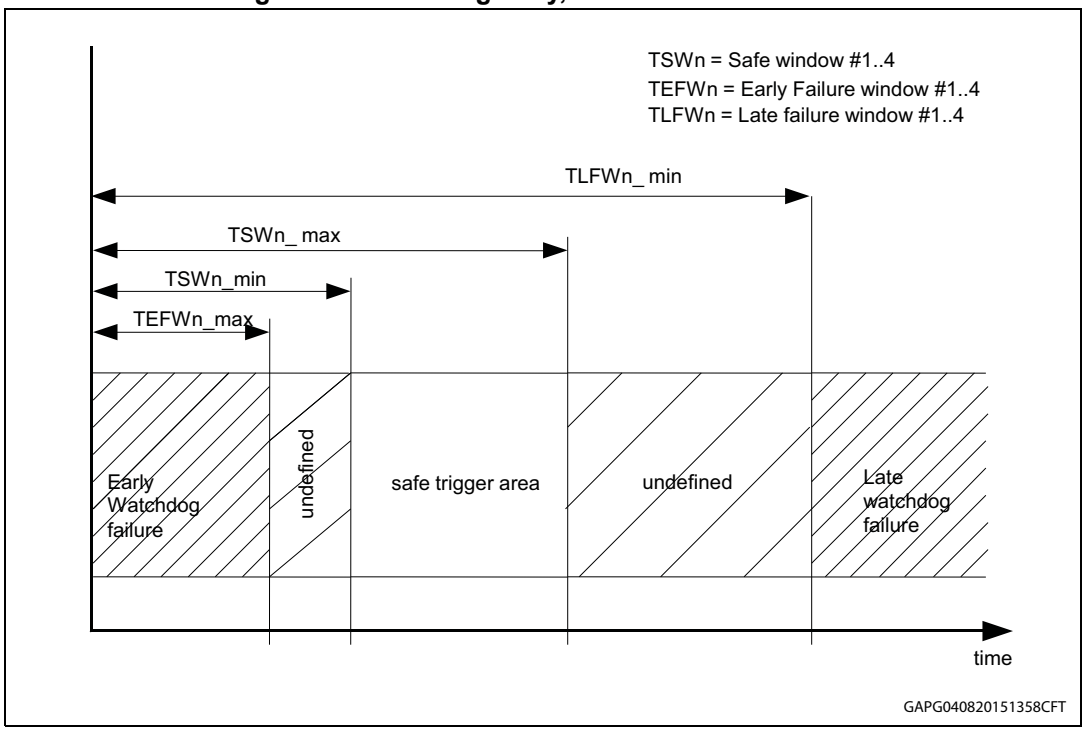
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Figure 9. Watchdog timing



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Figure 10. Watchdog early, late and safe windows



3.4.8 Current monitor output (CM)

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 6 V ≤ V_S ≤ 28V; 6 V ≤ V_{SREG} ≤ 28 V; T_j = -40 °C to 150 °C, unless otherwise specified

Table 14. Current monitor output (CM)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{CM}	Functional voltage range		0		V_1-1V	V
I_{CMr}	Current monitor output ratio: $I_{CM}/I_{OUT1,4,5,6 \text{ and } 7}$ (low on-resistance)	0 V ≤ V_{CM} ≤ (V_1 - 1 V)		1/10000		
	I_{CM}/I_{OUT8} (low on-resistance)			1/6500		
	$I_{CM}/I_{OUT\ 2,3,\ 7,8}$ (high on-resistance)			1/2000		
	$I_{CM}/I_{OUT9,10,11,12,13,14,15 \text{ and HS}}$			1/1000		

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Table 14. Current monitor output (CM) (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$I_{CM\ acc}$	Current monitor accuracy $accI_{CMOUT1,4,5,6\ and\ 7}$(low on-resistance)	0 V ≤ V_{CM} ≤ (V_1 - 1 V); I_{OUTmin} = 500 mA; $I_{OUT4,5max}$=7.4 A; $I_{OUT1,6max}$ = 2.9 A; $I_{OUT7max}$ = 1.4 A		4% + 1% FS(1)	8% + 2% FS(1)	
	Current monitor accuracy $accI_{CMOUT\ 8}$ (low on-resistance)	0 V ≤ V_{CM} ≤ (V_1 - 1 V); I_{OUTmin} = 100 mA; $I_{OUT8max}$=0.9 A				
	Current monitor accuracy $accI_{CMOUT2,3,\ 9,10,11,12,13,14,15\ ,HS\ and\ OUT7,8}$ (high on-resistance)	0 V ≤ V_{CM} ≤ (V_1 - 1 V); $I_{OUT.min}$ = 100 mA; $I_{OUT11,12,\ 15\ HS}$ = 0.2 A; $I_{OUT7,8\ max}$ = 0.3 A				
$I_{CM\ acc_2ol}$	Current monitor accuracy $accI_{CMOUT1,4,5,6\ and\ 7}$ (low on-resistance)	0 V ≤ V_{CM} ≤ (V_1 - 1 V); I_{OUTmin} = 2 * I_{OLD}; $I_{OUT4,5max}$ = 7.4 A; $I_{OUT1,6max}$ = 2.9 A; $I_{OUT7max}$ = 1.4 A		4% + 1% FS(1)	8% + 2% FS(1)	
	Current monitor accuracy $accI_{CMOUT\ 8}$(low on-resistance)	0 V ≤ V_{CM} ≤ (V_1 - 1 V); I_{OUTmin} = 2 * I_{OLD}; $I_{OUT8max}$ = 0.9 A				
	Current monitor accuracy $accI_{CMOUT2,\ 3,\ 9,11,12,13,14,15,\ HS\ and\ OUT7,8}$ (high on-resistance)	0 V ≤ V_{CM} ≤ (V_1 - 1 V); $I_{OUT.min}$ = 2 * I_{OLD}; $I_{OUT2,3max}$ = 0.4 A; $I_{OUT9,13,14max}$ = 0.3 A; $I_{OUT11,12,15\ HS}$ = 0.2 A; $I_{OUT7,8\ max}$ = 0.3 A				
	Current monitor accuracy $accI_{CMOUT10}$	0 V ≤ V_{CM} ≤ (V_1 - 1 V); $I_{OUT.min}$ = 2 * I_{OLD}; $I_{OUT10max}$ = 0.4 A		4% + 1% FS(1)	8% + 4% FS(1)	
t_{cmb}	Current monitor blanking time			32		µs

1. FS (full scale) = I_{OUTmax} * I_{CMr}

3.4.9 Charge pump

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 6 V ≤ V_S ≤ 28V; T_j = -40 °C to 150 °C, unless otherwise specified.

Table 15. Charge pump electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{CP}	Charge pump output voltage	V_S = 6 V, I_{CP} = -15 mA	V_S+6	V_S+7		V
		V_S ≥ 10 V, I_{CP} = -15 mA	V_S+11	V_S+12	V_S+13.5	V
I_{CP}	Charge pump output current(1)	V_{CP} = V_S + 10 V; V_S = 13.5 V; C_1 = C_2 = C_{CP} = 100 nF	22.5			mA

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Table 15. Charge pump electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{CPlim}	Charge pump output current limitation(2)	$V_{CP} = V_S$; V_S = 13.5 V; $C_1 = C_2 = C_{CP}$ = 100 nF			70	mA
V_{CP_low}	Charge pump low threshold voltage		V_S+4.5	V_S+5	V_S+5.5	V
T_{CP}	Charge pump low filter time			64		µs
f_{CP}	Charge Pump frequency			400		kHz

1. I_{CP} is the minimum current the device can provide to an external circuit without V_{CP} going below V_S + 10 V.
2. I_{CPlim} is the maximum current, which flows out of the device in case of a short to V_S.

3.4.10 Outputs OUT1 - OUT15, OUT_HS, ECV, ECDR

The voltages are referred to power ground and currents are assumed positive, when the current flows into the pin. 6 V ≤ V_S ≤ 28 V; 6 V ≤ V_{SREG} ≤ 28 V, all outputs open; T_j = -40 °C to 150 °C, unless otherwise specified.

Table 16. Outputs OUT1 - OUT15, OUT_HS, ECV, ECDR

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$r_{ON\ OUT1,6}$	On-resistance to supply or GND	V_S = 13.5 V; T_j = 25 °C; $I_{OUT1,6}$ = ±1.5A		300		mΩ
		V_S = 13.5V; T_j = 130°C $I_{OUT1,6}$ = ±1.5 A			600	mΩ
$r_{ON\ OUT2,3}$	On-resistance to supply or GND	V_S = 13.5 V; T_j = 25 °C; $I_{OUT2,3}$ = ±0.25 A		2000		mΩ
		V_S = 13.5 V; T_j = 130 °C; $I_{OUT2,3}$ = ±0.25 A			4000	mΩ
$r_{ON\ OUT4}$	On-resistance to supply or GND	V_S = 13.5V; T_j = 25 °C; I_{OUT4} = ±3 A		150		mΩ
		V_S = 13.5 V; T_j = 130 °C; I_{OUT4} = ±3 A			300	mΩ
$r_{ON\ OUT5}$	On-resistance to supply or GND	V_S = 13.5 V; T_j = 25°C; I_{OUT5} = ±3 A		100		mΩ
		V_S = 13.5 V; T_j = 130 °C; I_{OUT5} = 3 A			200	mΩ
$r_{ON\ OUT7}$	On-resistance to supply in low resistance mode	V_S = 13.5 V; T_j = 25 °C; I_{OUT7} = -0.8 A		500		mΩ
		V_S = 13.5 V; T_j = 130 °C; I_{OUT7} = -0.8 A			1000	mΩ
	On-resistance to supply in high resistance mode	V_S = 13.5 V; T_j = 25°C; I_{OUT7} = -0.2 A		1600		mΩ
		V_S = 13.5 V; T_j = 130 °C; I_{OUT7} = -0.2 A			3200	mΩ

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Table 16. Outputs OUT1 - OUT15, OUT_HS, ECV, ECDR (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$r_{ON\ OUT8}$	On-resistance to supply in low resistance mode	V_S = 13.5 V; T_j = 25 °C; I_{OUT8} = -0.4 A		800		mΩ
		V_S = 13.5 V; T_j = 130 °C; I_{OUT8} = -0.4 A			1600	mΩ
	On-resistance to supply in high resistance mode	V_S = 13.5 V; T_j = 25 °C; I_{OUT8} = -0.2 A		1600		mΩ
		V_S = 13.5 V; T_j = 130 °C; I_{OUT8} = -0.2 A			3200	mΩ
$r_{ON\ OUT9,10,13,14}$	On-resistance to supply	V_S = 13.5 V; T_j = 25 °C; $I_{OUT9,10,13,14}$ = -75 mA		2000		mΩ
		V_S = 13.5 V; T_j = 130 °C; $I_{OUT9,10,13,14}$ = -75 mA			4000	mΩ
$r_{ON\ OUT11,12,15,\ HS}$	On-resistance to supply	V_S = 13.5 V; T_j = 25 °C; $I_{OUT11,12,15,\ HS}$ = -75 mA		5		Ω
		V_S = 13.5 V; T_j = 130 °C; $I_{OUT11,12,15,\ HS}$ = -75 mA			10	Ω
$r_{ON\ ECV}$	On-resistance to GND	V_S = 13.5 V; T_j = 25 °C; $I_{OUTECV,ECFD}$ = +0.4 A		1600	2200	mΩ
		V_S = 13.5 V; T_j = 130 °C; $I_{OUTECV,ECFD}$ = +0.4 A		2500	3400	mΩ
I_{QLH}	Switched-off output current high-side drivers of OUT7-15, OUT_HS	V_{OUT} = 0 V; standby mode	-5			µA
		V_{OUT} = 0 V; active mode	-10			µA
I_{QLH}	Switched-off output current high-side drivers of OUT1-6	V_{OUT} = 0 V; standby mode	-5			µA
		V_{OUT} = 0 V; Active mode	-100			µA
I_{QLL}	Switched-off output current low-side drivers of OUT1-6	V_{OUT} = V_S; standby mode			165	µA
		V_{OUT} = V_S - 0.5 V; active mode	-100			µA
	Switched-off output current low-side driver of ECV	V_{OUT} = V_S - 2.5 V with ECDR = V_S; standby mode	-15		15	µA
		V_{OUT} = V_S - 2.5 V with ECDR = V_S; active mode	-10			µA

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3.4.11 Power outputs switching times

The voltages are referred to power ground and currents are assumed positive, when the current flows into the pin. 6 V ≤ V_S ≤ 28 V; 6 V ≤ V_{SREG} ≤ 28 V; T_j = -40 °C to 150 °C, unless otherwise specified.

Table 17. Power outputs switching times

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{d\ ON\ H}$	Output delay time high-side driver on ($OUT_{1,2,3,4,5,6}$)	V_S = 13.5 V; V_1 = 5 V; corresponding low-side driver is not active (1)(2)(3) (from CSN 50% to OUT 50%) see *Figure 18*	15	40	80	µs
	Output delay time high-side driver on ($OUT_{7,8}$)		20	40	90	µs
$t_{d\ OFF\ H}$	Output delay time high-side driver off ($OUT_{1,4,5,6}$)	V_S = 13.5 V; V_1 = 5 V (1)(2)(3) (from CSN 50% to OUT 50%) see *Figure 18*	50	150	300	µs
	Output delay time high-side driver off ($OUT_{2,3,7,8}$)		20	70	130	µs
$t_{d\ ON\ H}$	Output delay time high-side driver on (OUT9 …OUT15, OUT_HS)	V_S/V_{SREG} = 13.5 V; V_1 = 5 V; (from CSN 80% to OUT 80%)			30	µs
$t_{d\ OFF\ H}$	Output switch off delay time high-side driver on (OUT9 …OUT15, OUT_HS)	V_S/V_{SREG} = 13.5 V; V_1 = 5 V; (from CSN 80% to OUT 20%)			35	µs
$t_{d\ ON\ L}$	Output delay time low-side driver (OUT_{1-6}, ECV) on	V_S = 13.5 V; V_1 = 5 V; corresponding high-side driver is not active (1)(2)(3) (from CSN 50% to OUT 50%) see *Figure 18*	15	30	70	µs
$t_{d\ OFF\ L}$	Output delay time low-side driver (OUT_{1-6}) off	V_S = 13.5 V; V_1 = 5 V (1)(2)(3) (from CSN 50% to OUT 50%) see *Figure 18*	40	150	300	µs
	Output delay time low-side driver (ECV) off	V_S = 13.5 V; V_1 = 5 V (1)(2)(3) (from CSN 50% to OUT 50%) see *Figure 18*	15	45	110	µs
$t_{d\ HL}$	Cross current protection time (OUT_{1-6})	$t_{cc\ ONLS_OFFHS} - t_{d\ OFF\ H}$ (4)	50	200	400	µs
$t_{d\ LH}$		$t_{cc\ ONHS_OFFLS} - t_{d\ OFF\ L}$ (4)				
dV_{OUT}/dt	Slew rate of OUT_1-OUT_8, ECV	V_S = 13.5 V; V_1 = 5 V (1)(2)(3)	0.1	0.2	0.6	V/µs
dVmax/dt	Maximum external applied slew rate on OUT1-OUT6 without switching on the LS and HS (only in Active mode)	Guaranteed by design	20			V/µs
dV_{OUT}/dt	Slew rate of OUT9-OUT15, OUT_HS	V_S/V_{SREG} = 13.5 V; V_1 = 5 V (1)(2)(3)		2		V/µs
$f_{PWMx}(00)$	PWM switching frequency	V_S/V_{SREG} = 13.5 V; V_1 = 5 V		100		Hz

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Table 17. Power outputs switching times (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$f_{PWMx}(01)$	PWM switching frequency	V_S/V_{SREG} = 13.5 V; V_1 = 5 V		200		Hz
$f_{PWMx}(10)$	PWM switching frequency	V_S/V_{SREG} = 13.5 V; V_1 = 5 V		330		Hz
$f_{PWMx}(11)$	PWM switching frequency	V_S/V_{SREG} = 13.5 V; V_1 = 5 V		500		Hz

1. R_{LOAD} = 16 Ω at $OUT_{1,6}$ and $OUT_{7,8}$ in low on-resistance mode
2. R_{LOAD} = 4 Ω at $OUT_{4,5}$
3. R_{LOAD} = 128 Ω at $OUT_{2,3,4,9,10,11,12,13,15,15,HS}$, ECV and $OUT_{7,8}$ in high on-resistance mode
4. t_{CC} is the switch-on delay time if complement in half bridge has to switch off

3.4.12 Current monitoring

The voltages are referred to power ground and currents are assumed positive, when the current flows into the pin. 6 V ≤ V_S ≤ 28 V; 6 V ≤ V_{SREG} ≤ 28 V; T_j = -40 °C to 150 °C, unless otherwise specified.

Table 18. Current monitoring

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$\|I_{OC1}\|$, $\|I_{OC6}\|$	Overcurrent threshold HS & LS	V_S = 13.5 V; V1 = 5 V; sink and source	3		5	A
$\|I_{OC2}\|$, $\|I_{OC3}\|$			0.5		1.0	A
$\|I_{OC4}\|$		V_S = 13.5 V; V1 = 5 V; sink and source; T_j = -40 °C to 70 °C	7.5		10	A
		V_S = 13.5 V; V1 = 5 V; sink and source; T_j = 130 °C	6		10	A
$\|I_{OC5_1}\|$		V_S = 13.5 V; V1 = 5 V; sink and source	3	4	5	A
$\|I_{OC5_2}\|$			4.5	6	7.5	A
$\|I_{OC5_3}\|$			7.5		10	A

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Table 18. Current monitoring (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$\|I_{OC7}\|$	Overcurrent threshold HS in low on-resistance mode	V_S/V_{SREG} = 13.5 V; V_1 = 5 V; source	1.5		2.5	A
	Overcurrent threshold HS in high on-resistance mode		0.35		0.65	A
$\|I_{OC8}\|$	Overcurrent threshold HS in low on-resistance mode		0.7		1.3	A
	Overcurrent threshold HS in high on-resistance mode		0.35		0.65	A
$\|I_{OC9}\|$, $\|I_{OC13}\|$, $\|I_{OC14}\|$	Overcurrent threshold HS in high current mode		0.35		0.7	A
	Overcurrent threshold to HS in low current mode		0.15		0.3	A
$\|I_{OC10}\|$	Overcurrent threshold HS in high current mode		0.5		1	A
	Overcurrent threshold HS in low current mode		0.25		0.5	A
$\|I_{OC11}\|$, $\|I_{OC12}\|$, $\|I_{OC15}\|$, $\|I_{OC_HS}\|$	Overcurrent threshold HS in high current mode		0.25		0.5	A
	Overcurrent threshold HS in low current mode		0.15		0.3	A
$\|I_{OCECV}\|$	output current threshold LS	V_S = 13.5 V; V_1= 5 V; sink	0.5		1.0	A
t_{FOC}	Filter time of overcurrent signal	Duration of overcurrent condition to set the status bit	10	55	100	µs
f_{rec0}	Recovery frequency for OC; OCR_FREQ (CR 7) = 0		1		4	kHz
f_{rec1}	Recovery frequency for OC; OCR_FREQ (CR 7) = 1		2		6	kHz
t_{AR}	Auto recovery time limit	OUT1 to OUT6		100		ms
		OUT7, OUT8, OUT_HS		120		ms
$\|I_{OLD1}\|$, $\|I_{OLD6}\|$	Under-current threshold HS & LS	V_S = 13.5 V; V_1 = 5 V; sink and source	6	30	80	mA
$\|I_{OLD2}\|$, $\|I_{OLD3}\|$			6	20	30	mA
$\|I_{OLD4}\|$, $\|I_{OLD5}\|$			40	150	300	mA

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Table 18. Current monitoring (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$\|I_{OLD7}\|$	Under-current threshold HS in low on-resistance mode	V_S/V_{SREG} = 13.5 V; V_1 = 5 V; source	15	40	60	mA
	Under-current threshold HS in high on-resistance mode		5	10	15	mA
$\|I_{OLD8}\|$	Under-current threshold HS in low on-resistance mode		10	30	45	mA
	Under-current threshold HS in high on-resistance mode		5	10	15	mA
I_{OLD9}, $\|I_{OLD13}\|$, $\|I_{OLD14}\|$	Under-current threshold HS in high current mode		6		12	mA
	Under-current threshold HS in low current mode		0.5		4	mA
$\|I_{OLD10}\|$	Under -current threshold HS in high current mode		10		30	mA
	Under -current threshold HS in low current mode		0.3		4	mA
$\|I_{OLD11}\|$, $\|I_{OLD12}\|$, $\|I_{OLD15}\|$, $\|I_{OLD_HS}\|$	Under -current threshold HS in high current mode		6		12	mA
	Under -current threshold HS in low current mode		0.85		4	mA
$\|I_{OLDECV}\|$	Under-current threshold LS	V_S = 13.5 V; V_1 = 5 V; sink	6	20	30	mA
t_{OL_out}	Filter time of open-load signal	Duration of open-load condition to set the status bit	150	200	250	µs

3.4.13 Heater

The voltages are referred to power ground and currents are assumed positive, when the current flows into the pin. 6 V ≤ V_S ≤ 28 V; T_j = -40 °C to 150 °C, unless otherwise specified.

Table 19. Heater

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$I_{GHheater}$	Average charge-current (charge stage)	T_j = 25 °C		0.3		A
$R_{GLheater}$	On-resistance (discharge-stage)	V_{SLx} = 0 V; I_{GHx} = 50 mA; T_j = 25 °C	4	8	10	Ω
		V_{SLx} = 0 V; I_{GHx} = 50 mA; T_j = 130 °C		11	14	Ω
$V_{GHheater}$	Gate-on voltage	V_S = SH= 6 V; I_{CP} = 15 mA	$V_{SHheater}$ + 6			V
		V_S = SH = 12 V; I_{CP} = 15 mA	$V_{SHeahter}$ + 8	$V_{SHeater}$ + 10	$V_{SHeater}$ + 11.5	V

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Table 19. Heater (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$R_{GSHeater}$	Passive gate-clamp resistance			15		kΩ
$T_{G(HL)xHL}$	Propagation delay time high to low (switch mode)	V_S = 13.5 V; V_{SHx} = 0; R_G = 0 Ω; C_G = 2.7 nF		1.5		µs
$T_{G(HL)xLH}$	Propagation delay time low to high (switch mode)	V_S = 13.5 V; V_{SLx} = 0; R_G = 0 Ω; C_G = 2.7 nF		1.5		µs
$t0_{GHheaterr}$	Rise time (switch mode)	V_S = 13.5 V; $V_{Sheater}$ = 0; R_G = 0 Ω; C_G = 2.7 nF		45		ns
$t0_{GHheaterf}$	Fall time (switch mode)	V_S = 13.5 V; $V_{Sheater}$ = 0; R_G = 0 Ω; C_G = 2.7 nF		85		ns

3.4.14 H-bridge driver

The voltages are referred to power ground and currents are assumed positive, when the current flows into the pin. 6 V ≤ V_S ≤ 28 V; 6 V ≤ V_{SREG} ≤ 28 V; T_j = -40°C to 150 °C, unless otherwise specified.

Table 20. H-bridge driver

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Drivers for external high-side PowerMOS						
$I_{GHx(Ch)}$	Average charge current (charge stage)	T_j = 25 °C		0.3		A
R_{GHx}	On-resistance (discharge-stage)	V_{SHx} = 0 V; I_{GHx} = 50 mA; T_j = 25 °C	6	10	14	Ω
		V_{SHx} = 0 V; I_{GHx} = 50 mA; T_j = 130 °C		14	20	Ω
V_{GHHx}	Gate-on voltage	V_S = SH = 6 V; I_{CP} = 15 mA	V_{SHx} + 6			V
		V_S = SH = 12 V; I_{CP} = 15 mA	V_{SHx} + 8	V_{SHx} + 10	V_{SHx} + 11.5	V
R_{GSHx}	Passive gate-clamp resistance	V_{GHx} = 0.5 V		15		kΩ
Drivers for external low-side Power-MOS						
$I_{GLx(Ch)}$	Average charge-current (charge stage)	T_j = 25 °C		0.3		A
R_{GLx}	On-resistance (discharge-stage)	V_{SLx} = 0 V; I_{GHx} = 50 mA; T_j = 25 °C	6	10	14	Ω
		V_{SLx} = 0 V; I_{GHx} = 50 mA; T_j = 130 °C		14	20	Ω
V_{GHLx}	Gate-on voltage	V_S = 6 V; I_{CP} = 15 mA	V_{SLx} + 6			V
		V_S = 12 V; I_{CP} = 15 mA	V_{SLx} + 8	V_{SLx} + 10	V_{SLx} + 11.5	V
R_{GSLx}	Passive gate-clamp resistance			15		kΩ

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3.4.15 Gate drivers for the external Power-MOS switching times

The voltages are referred to power ground and currents are assumed positive, when the current flows into the pin. 6 V ≤ V_S ≤ 28 V; 6 V ≤ V_{SREG} ≤ 28 V; T_j = -40 °C to 150 °C, unless otherwise specified.

Table 21. Gate drivers for the external Power-MOS switching times

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$T_{G(HL)xHL}$	Propagation delay time high to low (switch mode(1)	V_S = 13.5 V; V_{SHx} = 0; R_G = 0 Ω; C_G = 2.7 nF		1.5		µs
$T_{G(HL)xLH}$	Propagation delay time low to high (switch mode)(1)	V_S = 13.5 V; V_{SLx} = 0; R_G = 0 Ω; C_G = 2.7 nF		1.5		µs
$I_{GHxrmax}$	Maximum source current (current mode)	V_S = 13.5 V; V_{SHx} = 0; V_{GHx} = 1 V; SLEW<4:0> = 1 F_H		32		mA
$I_{GHxfmax}$	Maximum sink current (current mode)	V_S = 13.5 V, V_{SHx} = 0; V_{GHx} = 2 V; SLEW<4:0> = 1 F_H		32		mA
dI_{IGHxr}	Source current accuracy	V_S = 13.5 V; V_{SHx} = 0; V_{GHx} = 1 V	See *Figure 12: IGHxr ranges*			
dI_{IGHxf}	Sink current accuracy	V_S = 13.5 V; V_{SHx} = 0; V_{GHx} = 2 V	See *Figure 13: IGHxf ranges*			
$V_{DSHxrSW}$	Switching voltage (V_S-V_{SH}) between current mode and switch mode (rising)	V_S = 13.5 V		2.8		V
$V_{DSHxfSW}$	Switching voltage (V_S-V_{SH}) between switch mode and current mode (falling)	V_S = 13.5 V		2.8		V
$t0_{GHxr}$	Rise time (switch mode)	V_S = 13.5 V; V_{SHx} = 0; R_G = 0 Ω; C_G = 2.7 nF		45		ns
$t0_{GHxf}$	Fall time (switch mode)	V_S = 13.5 V; V_{SHx} = 0; R_G = 0 Ω; C_G = 2.7 nF		85		ns
$t0_{GLxr}$	Rise time	V_S = 13.5 V; V_{SLx} = 0; R_G = 0 Ω; C_G = 2.7 nF		45		ns
$t0_{GLxf}$	Fall time	V_S = 13.5 V; V_{SLx} = 0; R_G = 0 Ω; C_G = 2.7 nF		85		ns
$tccp_{0001}$	Programmable cross-current protection time			500		ns
$tccp_{0010}$	Programmable cross-current protection time			750		ns
$tccp_{0011}$	Programmable cross-current protection time			1000		ns
$tccp_{0100}$	Programmable cross-current protection time			1250		ns
$tccp_{0101}$	Programmable cross-current protection time			1500		ns

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Table 21. Gate drivers for the external Power-MOS switching times (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$tccp_{0110}$	Programmable cross-current protection time			1750		ns
$tccp_{0111}$	Programmable cross-current protection time			2000		ns
$tccp_{1000}$	Programmable cross-current protection time			2250		ns
$tccp_{1001}$	Programmable cross-current protection time			2500		ns
$tccp_{1010}$	Programmable cross-current protection time			2750		ns
$tccp_{1011}$	Programmable cross-current protection time			3000		ns
$tccp_{1100}$	Programmable cross-current protection time			3250		ns
$tccp_{1101}$	Programmable cross-current protection time			3500		ns
$tccp_{1110}$	Programmable cross-current protection time			3750		ns
$tccp_{1111}$	Programmable cross-current protection time			4000		ns
f_{PWMH}	PWMH switching frequency(1)	V_S = 13.5 V; V_{SLx} = 0; R_G = 0 Ω; C_G = 2.7 nF; PWMH-Duty-Cycle = 50%			50	kHz

1. Without cross-current protection time t_{CCP}.

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Figure 11. H-driver delay times

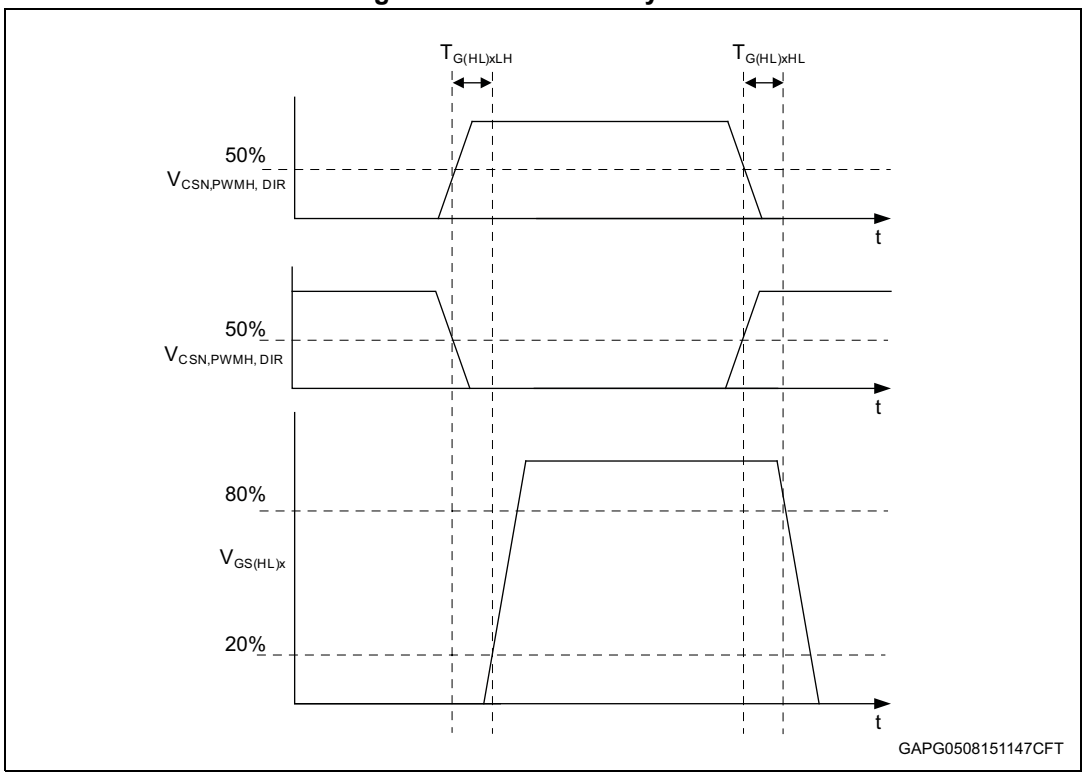
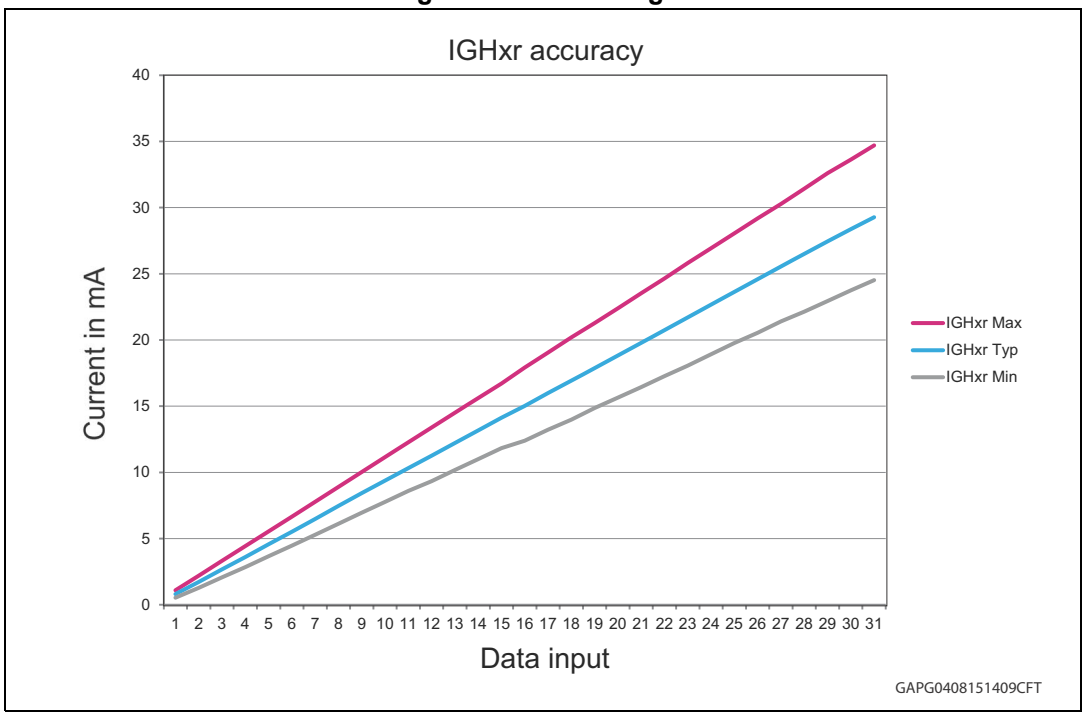
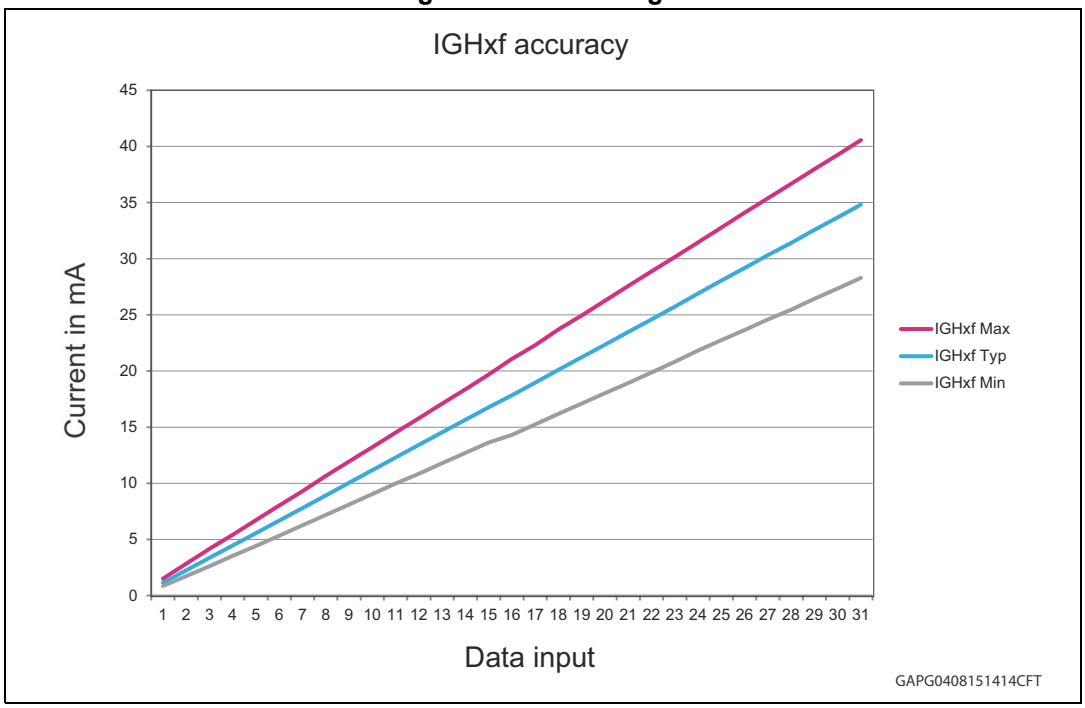


Figure 12. IGHxr ranges



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Figure 13. IGHxf ranges



3.4.16 Drain source monitoring external H-bridge

The voltages are referred to power ground and currents are assumed positive, when the current flows into the pin. 6 V ≤ V_S ≤ 28 V; 6 V ≤ V_{SREG} ≤ 28 V; T_j = -40°C to 150 °C, unless otherwise specified.

Table 22. Drain source monitoring external H-bridge

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{SCd1_HB}	Drain-source threshold voltage		0.375	0,5	0.625	V
V_{SCd2_HB}	Drain-source threshold voltage		0.6	0,75	0.9	V
V_{SCd3_HB}	Drain-source threshold voltage		0,85	1	1,15	V
V_{SCd4_HB}	Drain-source threshold voltage		1,06	1,25	1,43	V
V_{SCd5_HB}	Drain-source threshold voltage		1,27	1,5	1,73	V
V_{SCd6_HB}	Drain-source threshold voltage		1,49	1,75	2,01	V
V_{SCd7_HB}	Drain-source threshold voltage		1,7	2	2,3	V
t_{SCd_HB}	Drain-source monitor filter time			6		µs
t_{scs_HB}	Drain-source comparator settling time	V_S = 13.5 V; V_{SH} = jump from GND to V_S			5	µs

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3.4.17 Drain source monitoring external heater MOSFET

The voltages are referred to power ground and currents are assumed positive, when the current flows into the pin. 6 V ≤ V_S ≤ 28 V; 6 V ≤ V_{SREG} ≤ 28 V; T_j = -40 °C to 150 °C, unless otherwise specified.

Table 23. Drain source monitoring external heater MOSFET

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{SCd1_HE}	Drain-source threshold voltage		160	200	250	mV
V_{SCd2_HE}	Drain-source threshold voltage		200	250	305	mV
V_{SCd3_HE}	Drain-source threshold voltage		240	300	360	mV
V_{SCd4_HE}	Drain-source threshold voltage		280	350	420	mV
V_{SCd5_HE}	Drain-source threshold voltage		320	400	480	mV
V_{SCd6_HE}	Drain-source threshold voltage		360	450	540	mV
V_{SCd7_HE}	Drain-source threshold voltage		400	500	600	mV
V_{SCd8_HE}	Drain-source threshold voltage		440	550	660	mV
t_{SCd_HE}	Drain-source monitor filter time			6		µs
t_{scs_HE}	Drain-source comparator settling time	V_S = 13.5 V; V_{SH} = jump from GND to V_S			5	µs
t_{scbl_HE}	Drain-source monitoring blanking time			8		µs

3.4.18 Open-load monitoring external H-bridge

The voltages are referred to power ground and currents are assumed positive, when the current flows into the pin. 6 V ≤ V_S ≤ 28 V; 6 V ≤ V_{SREG} ≤ 28 V; T_j = -40 °C to 150 °C, unless otherwise specified.

Table 24. Open-load monitoring external H-bridge

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{ODSL}	Low-side drain-source monitor low off-threshold voltage	V_{SLx} = 0 V; V_S = 13.5 V		0.15 V_S		V
V_{ODSH}	Low-side drain-source monitor high off-threshold voltage	V_{SLx} = 0 V; V_S = 13.5 V		0.85 V_S		V
V_{OLSHx}	Output voltage of selected SHx in open-load test mode	V_{SLx} = 0 V; V_S = 13.5 V		0.5 V_S		V
R_{pdOL}	Pull-down resistance of the non-selected *SHx* pin in open-load mode	V_{SLx} = 0 V; V_S = 13.5 V; V_{SHX} = 4.5 V		20		kΩ
t_{OL_HB}	Open-load filter time			2		ms

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3.4.19 Open-load monitoring external heater MOSFET

The voltages are referred to power ground and currents are assumed positive, when the current flows into the pin. 6 V ≤ V_S ≤ 28 V; 6 V ≤ V_{SREG} ≤ 28 V; T_j = -40 °C to 150 °C, unless otherwise specified.

Table 25. Open-load monitoring external heater MOSFET

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{OLheater}$	Open-load -threshold voltage	V_{SLx} = 0 V; V_S = 13.5 V		2		V
$I_{OLheater}$	Pull-up current source open-load diagnosis activated	V_{SLx} = 0 V; V_S = 13.5 V; $V_{SHheater}$ = 4.5 V		1		mA
t_{OL_HE}	Open-load filter time			2		ms

3.4.20 Electro-chrome mirror driver

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 6V ≤ V_S ≤ 28V; 6V ≤ V_{SREG} ≤ 28V; T_j = -40 °C to 150 °C, unless otherwise specified.

Table 26. Electro-chrome mirror driver

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{CTRLmax}$	Maximum EC-control voltage	ECV_HV (Config Reg) = 1 (1)	1.4		1.6	V
		ECV_HV (Config Reg) = 0 (1)	1.12		1.28	V
DNL_{ECV}	Differential Non Linearity		-2		2	LSB (2)
$\|dV_{ECV}\|$	Voltage deviation between target and ECV	dV_{ECV} = V_{target}(3) - V_{ECV}; $\|I_{ECDR}\|$ < 1 µA	-5% - 1LSB(2)		+5% + 1LSB(2)	mV
dV_{ECVnr}	Difference voltage between target and ECV sets flag if V_{ECV} is below it	dV_{ECV} = V_{target}(3) - V_{ECV}; toggle bitx = 1; status reg. x		120		mV
dV_{ECVhi}	Difference voltage between target and ECV sets flag if V_{ECV} is above it	dV_{ECV} = V_{target}(3) - V_{ECV}; toggle bitx = 1; status reg. x		-180		mV
t_{FECVNR}	ECV_{NR} filter time			32		µs
t_{FECVHI}	ECV_{HI} filter time			32		µs
$V_{ECDRminHIGH}$	Output voltage range	I_{ECDR} = -10 µA	V1 - 0.3 V		V1	V
$V_{ECDRmaxLOW}$		I_{ECDR} = 10 µA	0		0.7	V

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Table 26. Electro-chrome mirror driver (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{ECDR}	Current into ECDR	V_{target}(3) > V_{ECV} + 500 mV; V_{ECDR} = 3.5 V	-100		-10	µA
		V_{target}(3) < V_{ECV} - 500 mV; V_{ECDR} = 1.0 V; V_{target} = 0 V; V_{ECV} = 0.5 V	10		100	µA
$R_{ecdrdis}$	Pull-down resistance at ECDR in fast discharge mode and while EC-mode is off	V_{ECDR} = 0.7 V; ECON = ‘1’, EC<5:0> = 0 or ECON = ‘0’			10	kΩ

1. Bit ECV_HV (Config Reg) ='1' or ‘0’: ECV voltage, where I_{ECDR} can change sign.
2. 1 LSB (Least Significant Bit) = 23.8 mV typ
3. V_{target} is set by bits EC<5:0> (CR 11) and bit ECV_HV (Config Reg); tested for each individual bit.

3.4.21 Fail safe low-side switch

The voltages are referred to power ground and currents are assumed positive, when the current flows into the pin. 6 V ≤ V_S ≤ 18 V; T_j = 40 °C to 150 °C, unless otherwise specified.

Table 27. Fail safe low-side switch

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{OUT_max}	Max output voltage in case of missing supply	I_{OUT} = 1 mA; V_S = V_{SREG} = 0 V		2	2.5	V
R_{DSON}	DC output resistance	I_{LOAD} = 250 mA; T_j = 25 °C		1.4		Ω
		I_{LOAD} = 250 mA; T_j = 130 °C			2.2	Ω
I_{OLimit}	Overcurrent limitation	8 V < V_S < 16 V	500		1500	mA
t_{ONHL}	Turn on delay time to 10% V_{OUT}				100	µs
t_{OFFLH}	Turn off delay time to 90% V_{OUT}				100	µs
t_{SCF}	Short circuit filter time			64		µs
dV_{max}/dt	Maximum external applied slew rate on LS1_FSO and LS2_FSO without switching on LS	Guaranteed by design	60			V/µs

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3.4.22 Wake up input WU

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 6 V ≤ V_{SREG} ≤ 28 V; T_j = 40 °C to 150 °C, unless otherwise specified.

Table 28. Wake-up inputs

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{WUthn}	Wake-up negative edge threshold voltage		0.4 V_{SREG}	0.45 V_{SREG}	0.5 V_{SREG}	V
V_{WUthp}	Wake-up positive edge threshold voltage		0.5 V_{SREG}	0.55 V_{SREG}	0.6 V_{SREG}	V
V_{HYST}	Hysteresis		0.05 V_{SREG}	0.1 V_{SREG}	0.15 V_{SREG}	V
t_{WU_stat}	Static wake filter time			64		µs
I_{WU_stdby}	Input current in standby mode	V_{WU} < 1 V or V_{WU} > (V_{SREG} – 1.5 V)	5	30	60	µA
R_{WU_act}	Input resistor to GND in Active mode and in Standby mode during Wake-up input sensing		80	160	300	kΩ
t_{WU_cyc}	Cyclic wake filter time			16		µs

3.4.23 High speed CAN transceiver

ISO 11898-2:2003 and ISO 11898-5:2007 compliant.

SAE J2284 compliant.

Selective wake functionality according to ISO 11898-6:2013.

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin.

5.5 V ≤ V_{SREG} ≤ 18 V; V_{CANSUP} = V1; $T_{junction}$ = -40 °C to 150 °C, unless otherwise specified. -12 V ≤ (V_{CANH} + V_{CANL}) / 2 ≤ 12 V

Table 29. CAN communication operating range

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{SREG_COM}	Supply voltage operating range for CAN communication	V_{V1} = V_{CANSUP}	5.5		18	V
$V_{CANSUPlow}$	CAN supply low voltage flag	V_{V1} = V_{CANSUP} decreasing	4.5	4.65	4.8	V
$V_{CANHL,CM}$	Common mode Bus voltage	Measured with respect to the ground of each CAN node	-12		12	V

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Table 30. CAN transmit data input: pin TxDC

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{TXDCLOW}$	Input voltage dominant level		1.0	1.45	2.0	V
$V_{TXDCHIGH}$	Input voltage recessive level		1.2	1.85	2.3	V
$V_{TXDCHYS}$	$V_{TXDCHIGH}$-$V_{TXDCLOW}$		0.2	0.4	0.7	V
R_{TXDCPU}	TXDC pull up resistor		16	35	60	kΩ
$t_{d,TXDC(dom-rec)}$	TXDC - $CAN_{H,L}$ delay time dominant - recessive	R_L = 60 Ω; C_L = 100 pF; 70 % V_{RXD} – 30% V_{DIFF}; TXDC rise time = 10 ns (10% - 90%)(1)	0		120	ns
$t_{d,TXDC(rec-diff)}$	TXDC - $CAN_{H,L}$ delay time recessive - dominant	R_L = 60 Ω; C_L = 100 pF; 30 % V_{RXD} – 70% V_{DIFF}; TXDC fall time = 10 ns (90% - 10%)(1)	0		120	ns
$t_{dom(TXDC)}$	TXDC dominant time-out		0.8	2	5	ms

1. Guaranteed by design.

Table 31. CAN receive data output: Pin RxDC

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{RXDCLOW}$	Output voltage dominant level	I_{RXDC} = 2 mA	0	0.2	0.5	V
$V_{RXDCHIGH}$	Output voltage recessive level	I_{RXDC} = -2 mA	V1 - 0.5	V1 - 0.2	V1	V
$t_{r,RXDC}$	RXDC rise time	C_L = 15 pF; 30% - 70% V_{RXDC}(1)	0		25	ns
$t_{f,RXDC}$	RXDC fall time	C_L = 15 pF; 70% - 30% V_{RXDC}(1)	0		25	ns
$t_{d,RXDC(dom-rec)}$	$CAN_{H,L}$ – RXDC delay time dominant - recessive	C_L = 15 pF; 30% V_{DIFF} – 70% V_{RXDC}(1)	0		120	ns
$t_{d,RXDC(rec - dom)}$	$CAN_{H,L}$ – RXDC delay time recessive - dominant	C_L = 15 pF; 70% V_{DIFF} – 30% V_{RXDC}(1)	0		120	ns

1. Guaranteed by design.

Table 32. CAN transmitter dominant output characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{CANHdom}$	Single ended CANH voltage level in dominant state	V_{TXDC} = $V_{TXDCLOW}$; R_L = 50 Ω; 65 Ω	2.75	3.5	4.5	V
$V_{CANLdom}$	Single ended CANL voltage level in dominant state	V_{TXDC} = $V_{TXDCLOW}$; R_L = 50 Ω; 65 Ω	0.5	1.5	2.25	V
$V_{DIFF,dom}$	Differential output voltage in dominant state: $V_{CANHdom}$-$V_{CANLdom}$	V_{TXDC} = $V_{TXDCLOW}$; R_L = 50 Ω; 65 Ω	1.5	2.0	3	V

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Table 32. CAN transmitter dominant output characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{SYM}	Driver symmetry $V_{SYM} = V_{CANHdom} + V_{CANLdom}$	Measured over one 250 kHz period (4 µs) R_L = 50 Ω; 65 Ω; f_{TXDC} = 250 kHz (square wave, 50% duty cycle); (1) C_{SPLIT} = 4.7 nF (+-5%)	4.5	5	5.5	V
$I_{OCANH,dom\ (0V)}$	CANH output current in dominant state	$V_{TXDC} = V_{TXDCLOW}$; V_{CANH} = 0 V	-100	-75	-45	mA
$I_{OCANL,dom\ (5V)}$	CANL output current in dominant state	$V_{TXDC} = V_{TXDCLOW}$; V_{CANL} = 5 V	45	75	100	mA
$I_{OCANH,dom\ (40V)}$	CANH output current in dominant state	$V_{TXDC} = V_{TXDCLOW}$; V_{CANH} = 40 V; R_L = 65 Ω; V_S = 40 V	0		5	mA
$I_{OCANL,dom\ (40V)}$	CANL output current in dominant state	$V_{TXDC} = V_{TXDCLOW}$; V_{CANL} = 40 V; R_L = 65 Ω; V_S = 40 V	0		100	mA

1. Measurement equipment input load <20 pF, >1 MΩ.

Table 33. CAN transmitter recessive output characteristics, CAN normal mode

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{CANHrec}$	CANH voltage level in recessive state	TRX ready state; $V_{TXDC} = V_{TXDCHIGH}$; No load	2	2.5	3	V
$V_{CANLrec}$	CANL voltage level in recessive state	TRX Ready state; $V_{TXDC} = V_{TXDCHiGH}$; No load	2	2.5	3	V
$V_{DIFF,recOUT}$	Differential output voltage in recessive state $V_{CANHrec}$-$V_{CANLrec}$	TRX Ready state; $V_{TXDC} = V_{TXDCHIGH}$; No load	-50		50	mV

Note: CAN normal mode: tested in TRX ready state while the device is in active mode.

Table 34. CAN transmitter recessive output characteristics, CAN low-power mode, biasing active

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{CANHrecLPbias}$	CANH voltage level in recessive state	TRX BIAS state; $V_{TXDC} = V_{TXDCHIGH}$; No load	2	2.5	3	V
$V_{CANLrecLPbias}$	CANL voltage level in recessive state	TRX BIAS state; $V_{TXDC} = V_{TXDCHiGH}$; No load	2	2.5	3	V
$V_{DIFF,recOUTLPbias}$	Differential output voltage in recessive state $V_{CANHrec}$-$V_{CANLrec}$	TRX BIAS state; $V_{TXDC} = V_{TXDCHIGH}$; No load	-50		50	mV

Note: CAN low power mode, biasing active: tested in TRX BIAS state while the device is in active mode, V1 Standby mode and Vbat_standby mode

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Table 35. CAN transmitter recessive output characteristics, CAN low-power mode, biasing inactive

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{CANHrecLP}$	CANH voltage level in recessive state	TRX Sleep state; $V_{TXDC} = V_{TXDCHIGH}$; No load	-0.1	0	0.1	V
$V_{CANLrecLP}$	CANL voltage level in recessive state	TRX Sleep state; $V_{TXDC} = V_{TXDCHIGH}$; No load	-0.1	0	0.1	V
$V_{DIFF,recOUTLP}$	Differential output voltage in recessive state $V_{CANHrec} - V_{CANLrec}$	TRX Sleep state; $V_{TXDC} = V_{TXDCHIGH}$; No load	-50		50	mV

Note: CAN Low Power mode, biasing inactive: tested in TRX sleep state while the device is in active mode, V1 Standby mode and Vbat_standby mode.

Table 36. CAN receiver input characteristics during CAN normal mode

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{THdom}	Differential receiver threshold voltage recessive to dominant state	TRX ready state; $(V_{CANH} + V_{CANL}) / 2$ = -12 V, 2.5 V, 12 V (1)	0.5	—	0.9	V
V_{THrec}	Differential receiver threshold voltage dominant to recessive state	TRX Ready state; $(V_{CANH} + V_{CANL}) / 2$ = -12 V, 2.5 V, 12 V (1)	0.5	—	0.9	V

1. Parameter evaluated with specific R_L = 60 Ω; guaranteed by characterization.

Note: CAN normal mode: tested in TRX ready state while the device is in active mode.

Table 37. CAN receiver input characteristics during CAN low power mode, biasing active

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{THdomLPbias}$	Differential receiver threshold voltage recessive to dominant state	TRX BIAS state; $(V_{CANH} + V_{CANL}) / 2$ = -12 V, 2.5 V, 12 V(1)	0.5	—	0.9	V
$V_{THrecLPbias}$	Differential receiver threshold voltage dominant to recessive state	TRX BIAS state; $(V_{CANH} + V_{CANL}) / 2$ = -12 V, 2.5 V, 12 V(1)	0.5	—	0.9	V

1. Parameter evaluated with specific R_L = 60 Ω; guaranteed by characterization.

Note: CAN low power mode, biasing active: tested in TRX BIAS state while the device is in active mode, V1 Standby mode and Vbat_standby mode.

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Table 38. CAN Receiver input characteristics during CAN Low power mode, biasing inactive

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{THdomLP}$	Differential receiver threshold voltage recessive to dominant state	TRX sleep state; (V_{CANH} + V_{CANL}) / 2 = -12 V; 0 V; 12 V(1)	0.5	—	0.9	V
$V_{THrecLP}$	Differential receiver threshold voltage dominant to recessive state	TRX Sleep state; (V_{CANH} + V_{CANL}) / 2 = -12 V; 0 V; 12 V(1)	0.5	—	0.9	V

1. Parameter evaluated with specific R_L = 60 Ω; guaranteed by characterization.

Note: CAN Low Power mode, biasing inactive: Tested in TRX Sleep state while the device is in active mode, V1 Standby mode and Vbat_standby mode.

Table 39. CAN receiver input resistance biasing active

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
R_{diff}	Differential internal resistance	TRX Ready & TRX BIAS states; V_{TXDC} = $V_{TXDCHIGH}$; no load	40	60	100	kΩ
$R_{CANH, CANL}$	Single ended Internal resistance	TRX Ready & TRX BIAS states; V_{TXDC} = $V_{TXDCHIGH}$; no load	20	30	50	kΩ
m_R	Internal Resistance matching $R_{CANH,CANL}$	TRX Ready & TRX BIAS states; V_{TXDC} = $V_{TXDCHIGH}$; no load; m_R = 2 x (R_{CAN_H} - R_{CAN_L}) / (R_{CAN_H} + R_{CAN_L})	-0.03		0.03	
C_{in}	Internal capacitance	Guaranteed by design		20	35	pF
$C_{in,diff}$	Differential internal capacitance	Guaranteed by design		10	20	pF

Note: CAN Normal and Low Power mode, biasing active: Tested in TRX Ready and TRX BIAS state while the device is in active and V1 Standby mode.

Table 40. CAN transceiver delay

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{TXpd,hl}$	Loop delay TXDC to RXDC (High to Low)	R_L = 60 Ω; C_L = 100 pF; 30% V_{TXDC} – 30% V_{RXDC}; TXDC fall time = 10 ns (90% - 10%); C_{RXDC} = 15 pF; f_{TXDC} = 250 kHz			255	ns
$t_{TXpd,lh}$	Loop delay TXDC to RXDC (Low to High)	R_L = 60Ω; C_L = 100pF; 70% V_{TXD} – 70% V_{RXD}; TXDC rise time = 10 ns (10% - 90%); C_{RXDC} = 15 pF; f_{TXDC} = 250 kHz			255	ns

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Table 40. CAN transceiver delay (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
T_{Bitrec}	Recessive Bit symmetry	R_L = 60 Ω; C_L = 100 pF; 70% V_{TXDC} (rising) - 30% V_{RXDC} (falling); C_{RXD} = 15 pF; 10 ns (10% - 90%, 90% - 10%); Rectangular pulse signal T_{TXDC} = 6000 ns, high pulse 1000 ns, low pulse 5000 ns	765	1000	1255	ns
t_{CAN}	CAN permanent dominant time-out		500	700	1000	µs
t_{WUP-V1}(1)	Time between WUP(2) on the CAN bus until V1 goes active	Wake-Up according to ISO11898-5:2007 (Bit SWEN = 0); 70% V_{DIFF} – 90% V1(min)	0		200	µs
t_{WUF-V1}(1)	Time between WUF(3) on the CAN bus until V1 goes active	Wake-Up according to ISO11898-6:2013 (Bit SWEN = 1); 30% V_{DIFF} – 90% V1(min)	0		200	µs

1. Guaranteed by characterization.
2. Time starts with the end of last dominant phase of the WUP.
3. Time starts with the end of CRC delimiter of the WUF.

Table 41. Maximum leakage currents on CAN_H and CAN_L, unpowered

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$I_{Leakage, CANH}$	Input leakage current CANH	Unpowered device; V_{CANH} = 5 V; V_{CANL} = 5 V; V_{SREG}, V_{CANSUP} connected via 0 Ω to GND; V_{SREG}, V_{CANSUP} connected via 47 kΩ to GND(1) T_j = -40 °C to 105 °C(2) T_j = 130 °C(3)	 -10 -12		 10 12	µA
$I_{Leakage, CANL}$	Input leakage current CANL	Unpowered device; V_{CANH} = 5 V; V_{CANL} = 5 V; V_{SREG}, V_{CANSUP} connected via 0 Ω to GND; V_{SREG}, V_{CANSUP} connected via 47 kΩ to GND(1) T_j = -40 °C to 105 °C(2) T_j = 130 °C(3)	 -10 -12		 10 12	µA

1. Guaranteed by design.
2. 105°C is the maximum junction temperature of an unpowered device according to this test condition within the specified ambient temperature range
3. Used for device test only.

Table 42. Biasing control timings

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
t_{filter}	CAN activity filter time		0.5		5	µs
t_{wake}	Wake-up time out		0.5	1	5	ms

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Table 42. Biasing control timings (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{Silence}$	CAN timeout		600	700	1200	ms
t_{BIAS}	Bias reaction time	R_L = 50 Ω, 65 Ω; C_L = 100 pF; C_{GND} (= C_{SPLIT}) = 100 pF; V_{TXDC} = $V_{TXDCLOW}$; 50% V_{DIFF} - V_{CANH} = V_{CANL} = $V_{CAN(H,L)rec(min)}$ (1); Transition TRX Sleep to TRX BIAS in Active, V1-Standby and Vbat_standby modes	0		200	µs

1. A wake-up-pattern is sent with a bit length of t_{filter}. T_{BIAS} is measured from the rising edge after having released the bus at the end of the 2nd dominant bit until CANH and CANL reach the minimum recessive output voltage ($V_{CANHrec}$, $V_{CANHrec}$).

3.4.24 LIN transceiver

LIN 2.2 compliant for bit-rates up to 20 kBit/s SAE J2602 compatible.

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 6 V ≤ V_{SREG} ≤ 18 V; $T_{junction}$ = -40 °C to 150°C unless otherwise specified.

Table 43. LIN transmit data input: pin TxD

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{TXDLOW}	Input voltage dominant level	Active mode	1.0			V
$V_{TXDHIGH}$	Input voltage recessive level	Active mode			2.3	V
V_{TXDHYS}	$V_{TXDHIGH}$-V_{TXDLOW}	Active mode	0.2			V
R_{TXDPU}	TXD pull up resistor	Active mode	13	29	46	kΩ

Table 44. LIN receive data output: pin RxD

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{RXDLOW}	Output voltage dominant level	Active mode		0.2	0.5	V
$V_{RXDHIGH}$	Output voltage recessive level	Active mode	V1-0.5	V1-0.2		V

Table 45. LIN transmitter and receiver: pin LIN

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{THdom}	Receiver threshold voltage recessive to dominant state		0.4 V_{SREG}	0.45 V_{SREG}	0.5 V_{SREG}	V
V_{Busdom}	Receiver dominant state				0.4V_{SREG}	V
V_{THrec}	Receiver threshold voltage dominant to recessive state		0.5 V_{SREG}	0.55 V_{SREG}	0.6 V_{SREG}	V
V_{Busrec}	Receiver recessive state		0.6 V_{SREG}			V

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Table 45. LIN transmitter and receiver: pin LIN (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{THhys}	Receiver threshold hysteresis: V_{THrec} -V_{THdom}		0.07 V_{SREG}	0.1 V_{SREG}	0.175 V_{SREG}	V
V_{THcnt}	Receiver tolerance center value: (V_{THrec} +V_{THdom})/2		0.475 V_{SREG}	0.5 V_{SREG}	0.525 V_{SREG}	V
V_{THwkup}	Activation threshold for wake-up comparator		1.0	1.5	2	V
$V_{THwkdwn}$	Activation threshold for wake-up comparator		V_{SREG} - 3.5	V_{SREG} - 2.5	V_{SREG}- 1.5	V
t_{LINBUS}	LIN Bus Wake-up Dominant Filter time	Sleep mode; edge: rec-dom		64		µs
t_{dom_LIN}	LIN Bus Wake-up Dominant Filter time	Sleep mode; edge: rec-dom-rec	28			µs
$I_{LINDomSC}$	Transmitter input current limit in dominant state	V_{TXD} = V_{TXDLOW}; V_{LIN} = V_{BATMAX} = 18 V	40	100	180	mA
$I_{bus_PAS_dom}$	Input leakage current at the receiver incl. pull-up resistor	V_{TXD} = $V_{TXDHIGH}$; V_{LIN} = 0 V; V_{BAT} = 12 V; Slave mode	-1			mA
$I_{bus_PAS_rec}$	Transmitter input current in recessive state	In standby modes; V_{TXD} = $V_{TXDHIGH}$; V_{LIN} > 8 V; V_{BAT} < 18 V; V_{LIN} ≥ V_{BAT}			20	µA
$I_{bus_NO_GND}$	Input current if loss of GND at device	GND = V_{SREG}; 0 V < V_{LIN} < 18 V; V_{BAT} = 12 V	-1		1	mA
I_{bus}	Input current if loss of V_{BAT} at device	GND = V_S; 0 V < V_{LIN} < 18 V Tj=-40 °C ....105 °C(1)			30	µA
		GND = V_S; 0 V < V_{LIN} < 18 V Tj = 130°C(2)			35	µA
V_{LINdom}	LIN voltage level in dominant state	Active mode; V_{TXD} = V_{TXDLOW} RBus=500 Ohm			1.2	V
V_{LINrec}	LIN voltage level in recessive state	Active mode; V_{TXD} = $V_{TXDHIGH}$; I_{LIN} = 10 µA	0.8*V_S			V
R_{LINup}	LIN output pull up resistor	V_{LIN} = 0 V	20	40	60	kΩ
C_{LIN}	LIN input capacitance				30	pF

1. 105°C is the maximum junction temperature of an unpowered device according to this test condition within the specified ambient temperature range.
2. Used for device test only.

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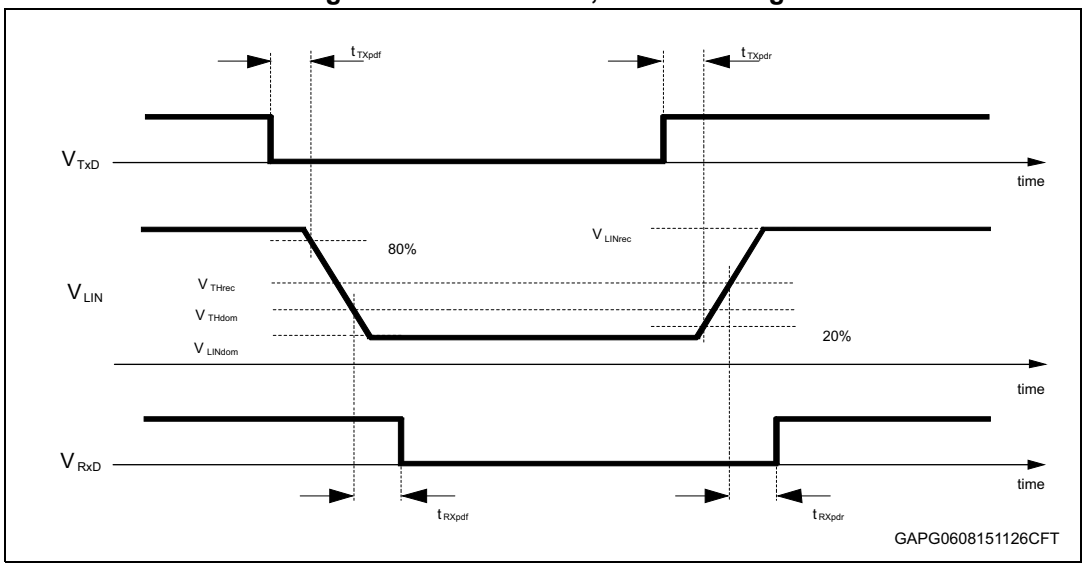
The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. $6V \leq V_S \leq 28V$; T_j = -40 °C to 150 °C, unless otherwise specified.

Table 46. LIN transceiver timing

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
t_{RXpd}	Receiver propagation delay time	$t_{RXpd} = max(t_{RXpdr}, t_{RXpdf})$; $t_{RXpdf} = t(0.5\ V_{RXD})-t(0.45\ V_{LIN})$; $t_{RXpdr} = t(0.5\ V_{RXD})-t(0.55\ V_{LIN})$; V_{SREG} = 12 V; C_{RXD}=20 pF; R_{bus} = 1 kΩ, C_{bus} = 1 nF; R_{bus} = 660 Ω, C_{bus} = 6.8 nF; R_{bus} = 500 Ω, C_{bus} = 10 nF			6	µs
t_{RXpd_sym}	Symmetry of receiver propagation delay time (rising vs. falling edge)	$t_{RXpd_sym} = t_{RXpdr} - t_{RXpdf}$; V_{SRE} = 12 V; R_{bus} = 1 kΩ; C_{bus} = 1 nF; C_{RXD} = 20 pF	-2		2	µs
D1	Duty Cycle 1	$TH_{Rec}(max) = 0.744 * V_{SREG}$; $TH_{Dom}(max) = 0.581 * V_{SREG}$; V_{SREG} = 7 to 18 V, t_{bit} = 50 µs; D1 = $t_{bus_rec}(min) / (2 \times t_{bit})$; R_{bus} = 1 kΩ, C_{bus} = 1 nF; R_{bus} = 660 Ω, C_{bus} = 6.8 nF; R_{bus} = 500 Ω, C_{bus} = 10 nF	0.396			
D2	Duty Cycle 2	$TH_{Rec}(min) = 0.422* V_{SREG}$; $TH_{Dom}(min) = 0.284* V_{SREG}$; V_{SREG} = 7.6 to 18 V, t_{bit} = 50 µs; D2 = $t_{bus_rec}(max) / (2 \times t_{bit})$; R_{bus} = 1 kΩ, C_{bus} = 1 nF; R_{bus} = 660 Ω, C_{bus} = 6.8 nF; R_{bus} = 500 Ω, C_{bus} = 10 nF			0.581	
D3	Duty Cycle 3	$TH_{Rec}(max) = 0.778* V_{SREG}$; $TH_{Dom}(max) = 0.616* V_{SREG}$; V_{SREG} = 7 to 18 V, t_{bit} = 96 µs; D3 = $t_{bus_rec}(min) / (2 \times t_{bit})$; R_{bus} = 1 kΩ, C_{bus} = 1 nF; R_{bus} = 660 Ω, C_{bus} = 6.8 nF; R_{bus} = 500 Ω, C_{bus} = 10 nF	0.417			
D4	Duty Cycle 4	$TH_{Rec}(min) = 0.389* V_{SREG}$; $TH_{Dom}(min) = 0.251* V_{SREG}$; V_{SREG} = 7.6 to 18 V, t_{bit} = 96 µs; D4 = $t_{bus_rec}(max) / (2 \times t_{bit})$; R_{bus} = 1 kΩ, C_{bus} = 1 nF; R_{bus} = 660 Ω, C_{bus} = 6.8 nF; R_{bus} = 500 Ω, C_{bus} = 10 nF			0.590	
$t_{dom(TXDL)}$	TXDL dominant time-out			12		ms
t_{LIN}	LIN permanent recessive time-out			40		µs
$t_{dom(bus)}$	LIN Bus permanent dominant time-out			12		ms

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Figure 14. LIN transmit, receive timing



3.4.25 SPI

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 6 V < V_{SREG} < 18 V; V1 = 5 V; all outputs open; T_j = -40 °C to 150 °C, unless otherwise specified.

Table 47. Input: CSN

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{CSNLOW}	Input voltage low level	Normal mode	1.0			V
$V_{CSNHIGH}$	Input voltage high level	Normal mode			2.3	V
V_{CSNHYS}	$V_{CSNHIGH}$ - V_{CSNLOW}	Normal mode	0.2			V
I_{CSNPU}	CSN Pull up resistor	Normal mode	13	29	46	kΩ

Table 48. Inputs: CLK, DI

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
t_{set}	Delay time from standby to Active mode	Time until SPI, ADC and OUT15/OUT_HS are operative		10		µs
t_{set_CP}	Delay time from standby to Active mode	Time until power stages that are supplied by the CP are operative	560	750	960	µs
V_{in_L}	Input low level		1.0			V
V_{in_H}	Input high level				2.3	V
V_{in_Hyst}	Input hysteresis		0.2			V
I_{pdin}	Pull down current at input	V_{in} = 1.5 V	5	30	60	µA

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Table 48. Inputs: CLK, DI (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
C_{in} (1)	Input capacitance at input CSN, CLK, DI and $PWM_{1,2}$	Guaranteed by design			15	pF
f_{CLK}	SPI input frequency at CLK				4	MHz

1. Value of input capacity is not measured in production test. Parameter guaranteed by design.

Table 49. DI, CLK and CSN timing

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
t_{CLK}	Clock period		250			ns
t_{CLKH}	Clock high time		100			ns
t_{CLKL}	Clock low time		100			ns
t_{set_CSN}	CSN setup time, CSN low before rising edge of CLK		150			ns
t_{set_CLK}	CLK setup time, CLK high before rising edge of CSN		150			ns
t_{set_DI}	DI setup time		25			ns
t_{hold_DI}	DI hold time		25			ns
t_{r_in}	Rise time of input signal DI, CLK, CSN				25	ns
t_{f_in}	Fall time of input signal DI, CLK, CSN				25	ns

Note: See Figure 16: SPI input timing.

Table 50. Output: DO

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{DOL}	Output low level	I_{DO} = -4 mA			0.5	V
V_{DOH}	Output high level	I_{DO} = 4 mA	V1 - 0.5			V
I_{DOLK}	3-state leakage current	V_{CSN} = V1, 0 V < V_{DO} < V1	-10		10	µA
C_{DO}	3-state input capacitance	Guaranteed by design		10	15	pF

Table 51. DO timing

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{r\ DO}$	DO rise time	C_L = 50 pF; I_{LOAD} = -1 mA			25	ns
$t_{f\ DO}$	DO fall time	C_L = 50 pF; I_{LOAD} = -1 mA			25	ns

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Table 51. DO timing (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{en\ DO\ tri\ L}$	DO enable time from 3-state to low level	C_L = 50 pF; I_{LOAD} = -1 mA; pull-up load to V1		50	100	ns
$t_{dis\ DO\ L\ tri}$	DO disable time from low level to 3-state	C_L = 50 pF; I_{LOAD} = -1 mA; pull-up load to V1		50	100	ns
$t_{en\ DO\ tri\ H}$	DO enable time from 3-state to high level	C_L = 50 pF; I_{LOAD} = -1 mA; pull-down load to GND		50	100	ns
$t_{dis\ DO\ H\ tri}$	DO disable time from high level to 3-state	C_L = 50 pF; I_{LOAD} = -1 mA; pull-down load to GND		50	100	ns
$t_{d\ DO}$	DO delay time	V_{DO} < 0.3 V1; V_{DO} > 0.7 V1; C_L = 50 pF		30	60	ns

Note: See Figure 17: SPI output timing.

Table 52. CSN timing

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{CSN_HI,min}$	Minimum CSN High time, active mode	Transfer of SPI-command to Input Register	6			µs
$t_{CSNfail}$	CSN low timeout		20	35	50	ms

Note: See Figure 18: SPI CSN - output timing.

3.4.26 Inputs TxD_C and TxD_L for Flash mode

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 6V ≤ V_{SREG} ≤ 18; V1 = 5 V; T_j = -40 °C to 150 °C.

Table 53. Inputs: TxD_C and TxD_L for Flash mode

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{flashL}	Input low level ($V_{TXDC/L}$ for exit from Flash mode)		6.1	7.25	8.4	V
V_{flashH}	Input high level ($V_{TXDC/L}$ for transition into Flash mode)		7.4	8.4	9.4	V
$V_{flashHYS}$	Input voltage hysteresis		0.6	0.8	1.0	V

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3.4.27 Inputs DIRH, PWMH

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 6 V ≤ V_{SREG} ≤ 18 V; T_j = -40 °C to 150 °C.

Table 54. Inputs DIRH, PWMH

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{IL}	Input voltage low level	V_{SREG} = 13.5 V	1			V
V_{IH}	Input voltage high level	V_{SREG} = 13.5 V			2.3	V
V_{IHYS}	Input hysteresis	V_{SREG} = 13.5 V	0.2			V
I_{in}	Input pull-down current	V_{SREG} = 13.5 V	5	30	60	µA

3.4.28 Debug input

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 6 V ≤ V_{SREG} ≤ 18 V; T_j = -40 °C to 150 °C.

Table 55. Debug input

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{dIL}	Input voltage low level	V_{SREG} = 13.5 V	1			V
V_{dIH}	Input voltage high level	V_{SREG} = 13.5 V			2.3	V
V_{dIHYS}	Input hysteresis	V_{SREG} = 13.5 V	0.2			V
R_{din}	Pull-down resistor	V_{DEBUG} = 6 to 18 V	2.5	5	7.5	kΩ

3.4.29 ADC characteristics

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 6 V ≤ V_{SREG} ≤ 18 V, T_j = -40 °C to 150 °C.

Table 56. ADC characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
t_{con}	Conversion time			2.5		µs
f_{ADC}	Clock frequency (see $f_{clk}2$)			8		MHz
Acc	Accuracy	Voltage divider + reference(1)	-2		2	%
		Overall accuracy for WU input: V_S = 22 V	-3		3	
		Overall accuracy for WU input: V_S = 18 V	-3.5		3.5	
		Overall accuracy for WU input: V_S = 6 V	-4		4	
		Overall accuracy for WU input: V_S = 4.5 V	-4.6		4.6	

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Table 56. ADC characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$IE_I I$	Integral linearity error				4	LSB
$IE_D I$	Differential linearity error				2	LSB
V_{AINVS}	Conversion voltage range (V_S, V_{SREG} & WU)		1		22	V
$V_{AINTemp}$	Conversion voltage range ($T_{CL}1$ …$T_{CL}6$)		0		2	V

1. Guaranteed by design.

3.4.30 Temperature diode characteristics

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 6 V ≤ V_{SREG} ≤ 18 V, T_j = -40 °C to 150 °C

Table 57. Temperature diode characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{TROOM\ 1\text{-}6}$	T_{SENSE} output voltage at 25 °C	V_S = 12 V; T = 25 °C	—	1.4		V
$V_{TSENSE1\text{-}6}$	T_{SENSE} output voltage 1 - 8	T = 25 °C; T = 130 °C; T = -40 °C	—	-4		mV/K

3.4.31 Interrupt outputs

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 6 V ≤ V_{SREG} ≤ 18 V, T_j = -40 °C to 150°C

Table 58. Interrupt outputs

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{INTL}	Output low level	I_{INT} = -4 mA			0.5	V
V_{INTH}	Output high level	I_{INT} = 4 mA	V1 - 0.5			V
I_{INTLK}	3-state leakage current	0 V < V_{INT} < V1	-10		10	µA
$t_{Interrupt}$	Interrupt pulse duration (NINT, RxD_L/NINT, RxD_C/NINT			56		µs
t_{Int_react}	Interrupt reaction time	Tested by scan chain	6		40	µs

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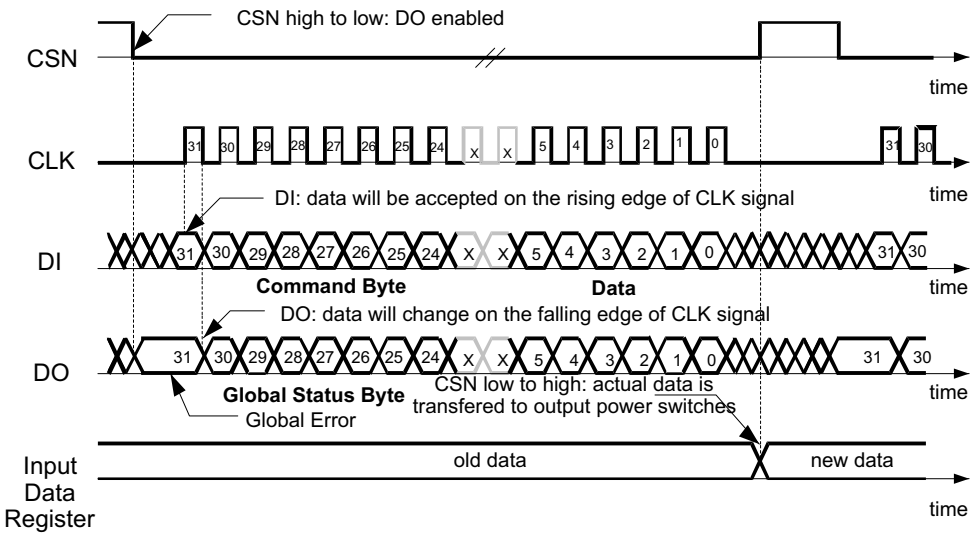
3.4.32 Timer1 and Timer2

6 V ≤ V_{SREG} ≤ 18 V; T_j = -40 °C to 150 °C

Table 59. Timer1 and Timer2

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
ton 1	Timer on time			0.1		ms
ton 2	Timer on time			0.3		ms
ton 3	Timer on time			1		ms
ton 4	Timer on time			10		ms
ton 5	Timer on time			20		ms
T1	Timer period			10		ms
T2	Timer period			20		ms
T3	Timer period			50		ms
T4	Timer period			100		ms
T5	Timer period			200		ms
T6	Timer period			500		ms
T7	Timer period			1000		ms
T8	Timer period			2000		ms

Figure 15. SPI – transfer timing diagram



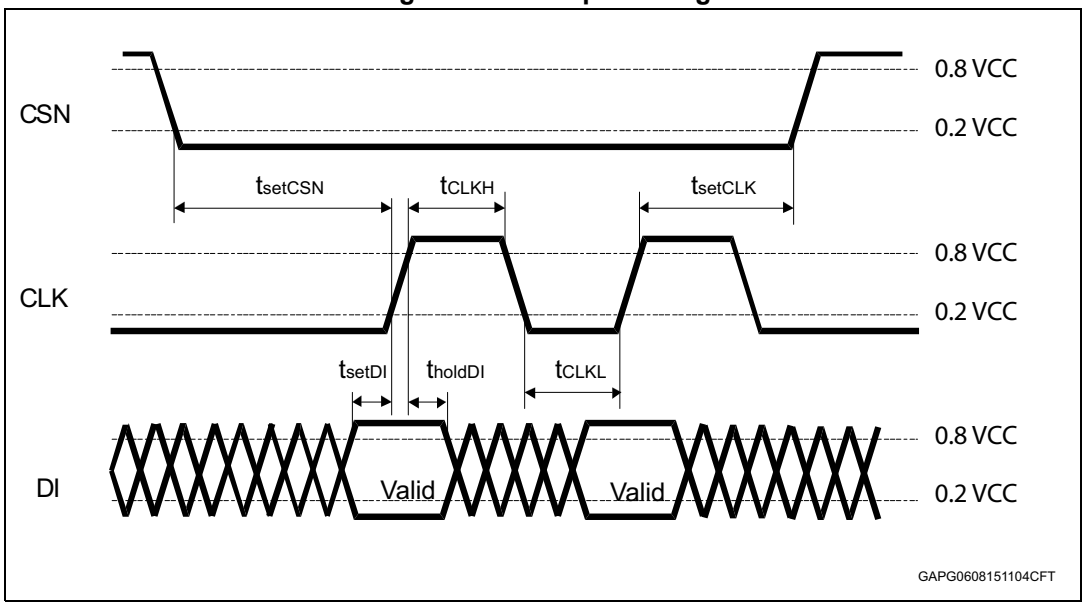
The SPI can be driven by a micro controller with its SPI peripheral running in following mode:

CPOL = 0 and CPHA = 0.

For this mode input data is sampled by the low to high transition of the clock CLK, and output data is changed from the high to low transition of CLK.

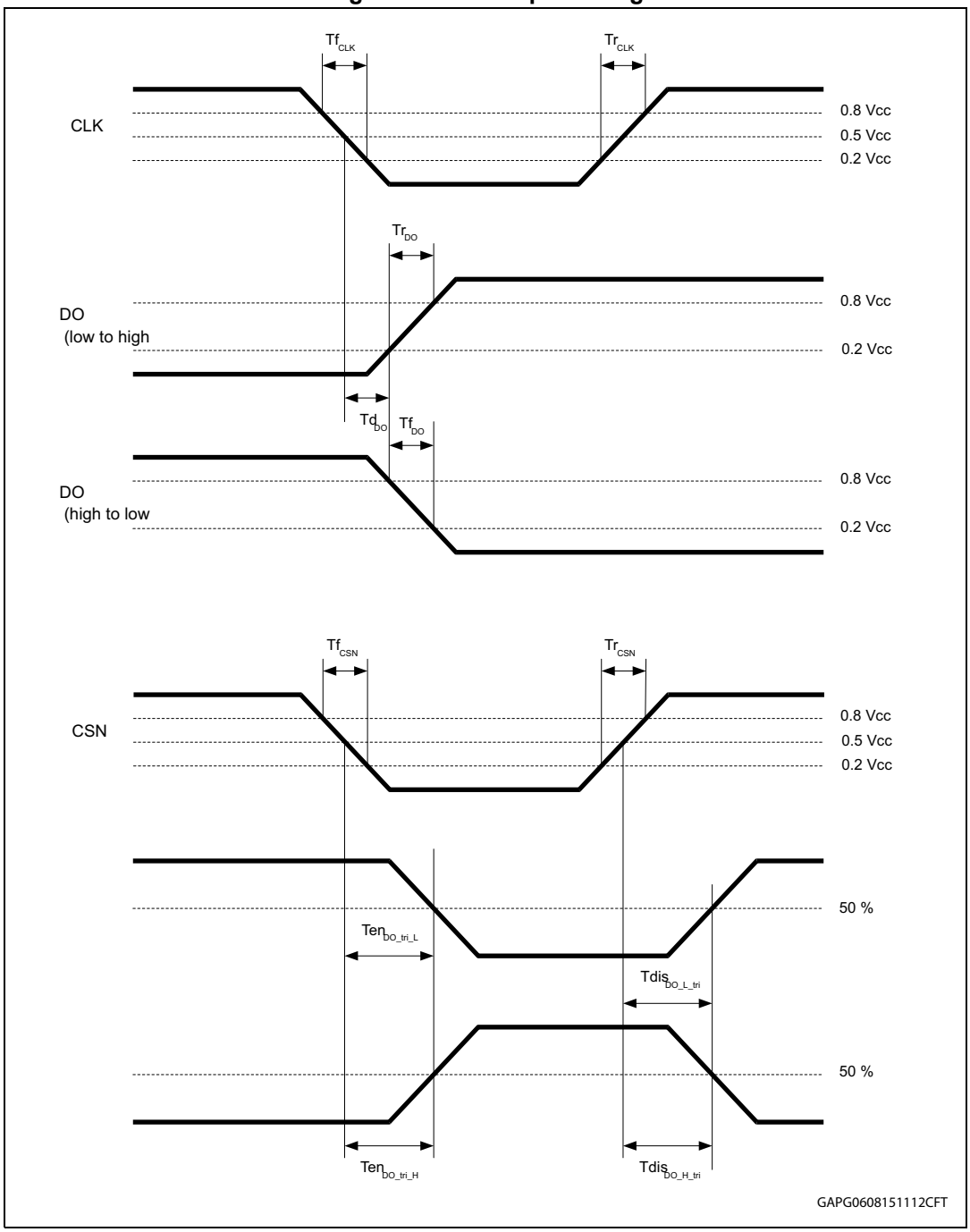
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Figure 16. SPI input timing



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Figure 17. SPI output timing



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Figure 18. SPI CSN - output timing

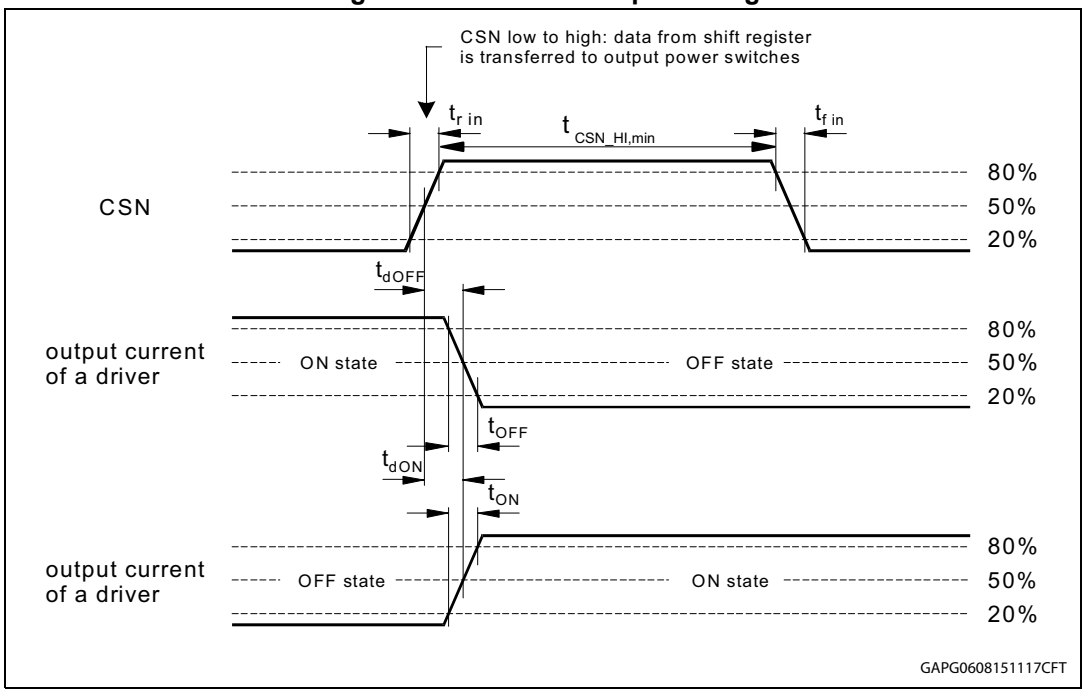
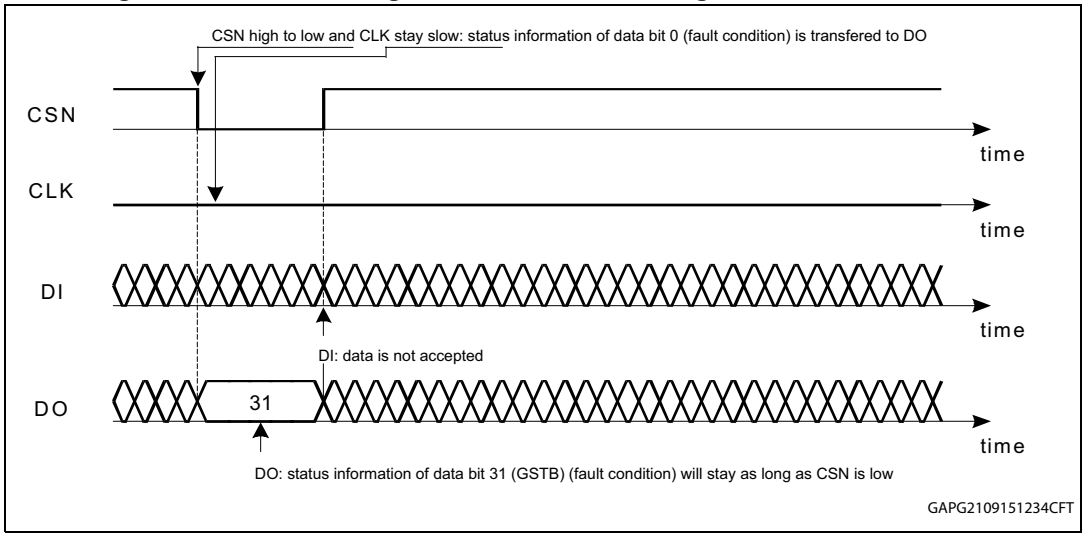


Figure 19. SPI – CSN high to low transition and global status bit access



3.4.33 SGND loss comparator

T_j = -40 °C to 150 °C, unless otherwise specified.

Table 60. SGND loss comparator

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{SGNDloss}$	V_{SGND} loss threshold	(V_{SGND} – V_{PGND})	100	270	500	mV
$t_{SGNDloss}$	V_{SGND} loss filter time		5	7	9	µs

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4 Application information

4.1 Supply V_S, V_{SREG}

V_{SREG} supplies voltage regulators V1 and V2, all internal regulated voltages for analog and digital functionality, LIN, CAN, the EC control block and both P-channel high-side switches OUT15 and OUT_HS.

All other high-sides, Fail Safe block and the charge pump are supplied by V_S.

In case the V_{SREG} pin is disconnected, all power outputs connected to V_S are automatically switched off.

4.2 Voltage regulators

The device contains two independent and fully protected low drop voltage regulators designed for very fast transient response and do not require electrolytic output capacitors for stability.

The output voltage is stable with ceramic load capacitors >220 nF.

4.2.1 Voltage regulator: V1

The V1 voltage regulator provides 5 V supply voltage and up to 250 mA continuous load current to supply the system microcontroller and the integrated CAN transceiver. The V1 regulator is embedded in the power management and fail-safe functionality of the device and operates according to the selected operating mode. The V1 voltage regulator is supplied by pin V_{SREG}.

In addition, the V1 regulator supplies the devices internal loads. The voltage regulator is protected against overload and overtemperature. An external reverse current protection has to be provided by the application circuitry to prevent the input capacitor from being discharged by negative transients or low input voltage. Current limitation of the regulator ensures fast charge of external bypass capacitors. The output voltage is stable for ceramic load capacitors >220 nF.

In case the device temperature exceeds the TSD1 threshold (either cluster or grouped mode) the V1 regulator remains on. The micro controller has the possibility for interaction or error logging. If the chip temperature exceeds the TSD2 threshold (TSD2 > TSD1), V1 will be deactivated and all wakeup sources (CAN, LIN, WU and Timer) are disabled. After t_{TSD}, the voltage regulator will restart automatically. If the restart fails 7 times within one minute the devices enter the Forced Vbat_standby mode. The status bit FORCED_SLEEP_TSD2/V1SC (SR1) is set.

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4.2.2 Voltage regulator: V2

The voltage regulator V2 is supplied by pin V_{SREG} and can supply additional 5 V loads such as sensors or potentiometers. The maximum continuous load current is 50 mA. The regulator is protected against:

- Overload
- Overtemperature
- Short-circuit (short to ground and battery supply voltage)
- Reverse biasing

4.2.3 Voltage regulator failure

The V1, and V2 regulator output voltages are monitored.

In case of a drop below the failure thresholds ($V1 < V1_{fail}$ for $t > t_{V1fail}$, $V2 < V2_{fail}$ for $t > t_{V2fail}$), the failure bits V1FAIL, V2FAIL (SR 2) are latched.

4.2.4 Short to ground detection

At turn-on of the V1 and V2 regulators, a short-to-GND condition is detected by monitoring the regulator output voltage.

If V1 or V2 is below the $V1_{fail}$ (or $V2_{fail}$) threshold for $t > t_{V1short}$ ($t > t_{V2short}$) after turn-on, the devices will identify a short circuit condition at the related regulator will be switched off.

In case of V1 short-to-GND the device enters Forced Vbat_standby mode automatically. Bits FORCED_SLEEP_TSD2/V1SC and (SR 1) V1FAIL (SR 2) are set.

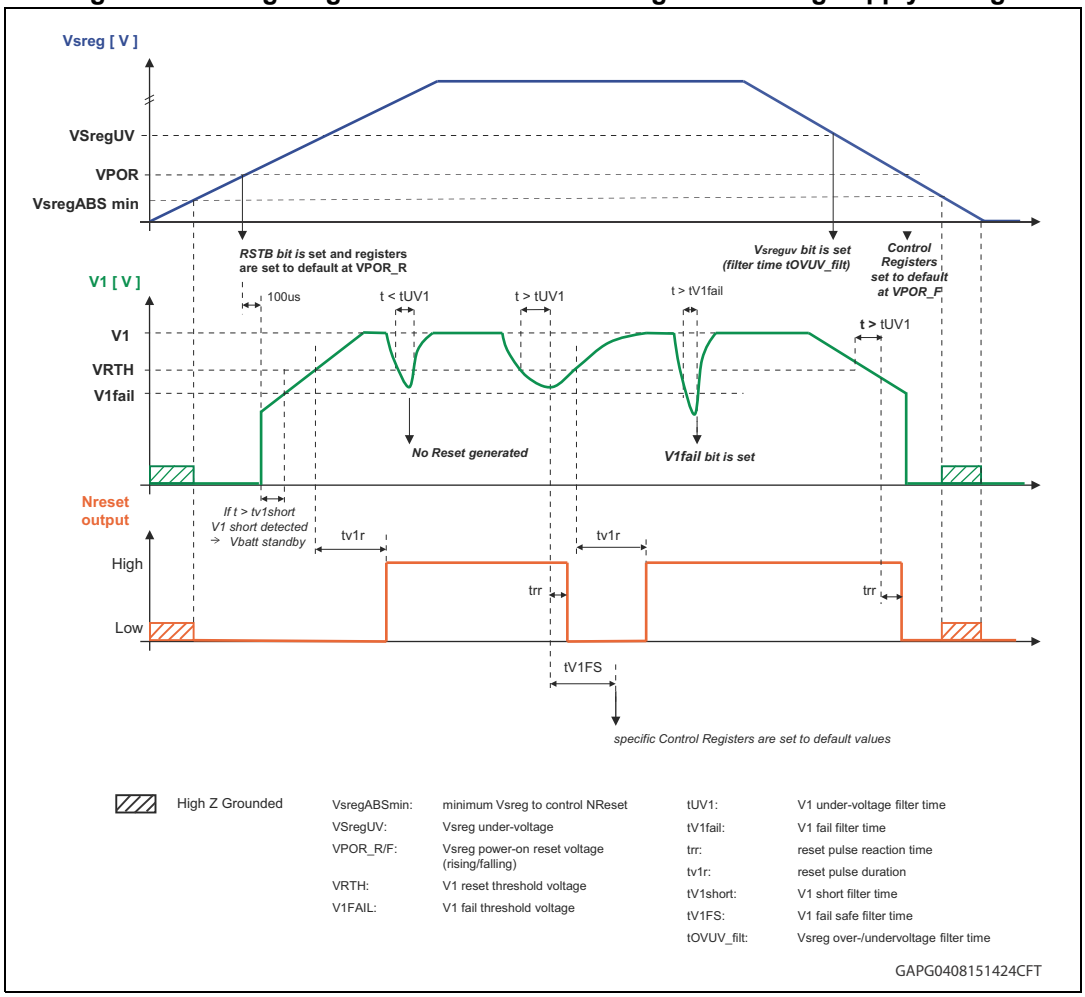
In case of a V2 short-to-GND failure the V2SC (SR 2) and V2FAIL (SR 2) bits are set.

Once the output voltage of the corresponding regulator exceeded the $V1_{fail}$ ($V2_{fail}$) threshold the short-to-ground detection is disabled. In case of a short-to-ground condition, the regulator is switched off due to thermal shutdown. V1 is switched off at TSD2, V2 is switched off at TSD1.

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4.2.5 Voltage regulator behavior

Figure 20. Voltage regulator behaviour and diagnosis during supply voltage



4.3 Operating modes

The devices can be operated in the following operating modes:

- Active
- LIN Flash
- CAN Flash
- V1_standby
- VBAT_standby
- Debug

4.3.1 Active mode

All functions are available and the device is controlled by SPI.

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4.3.2 Flash modes

To program the system microcontroller via LIN or HS CAN bus signals, the devices can be operated in LIN Flash mode or CAN Flash mode. The watchdog is disabled in these modes.

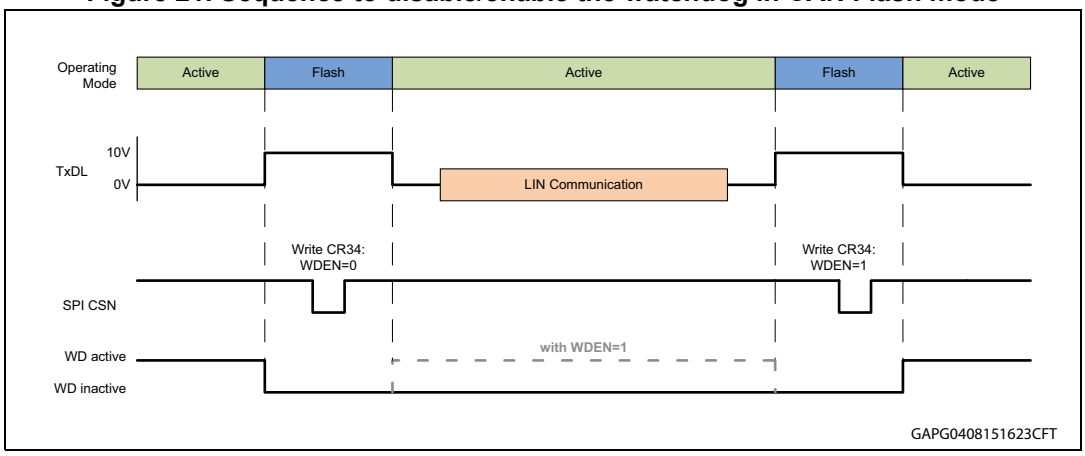
The Flash modes are entered by applying an external voltage at the respective pin:

- $V_{TxDL} \geq V_{FlashH}$ (CAN Flash mode)
- $V_{TxDC} \geq V_{FlashH}$ (LIN Flash mode)

In CAN Flash mode the CAN transceiver is set in TRX bias mode (CAN_GO_TO_TRX_RDY = 1) and TRX Normal mode automatically

During CAN Flash mode, the watchdog can be deactivated by setting CR34: WDEN = 0. Write access to this bit is only possible during CAN Flash mode in order to prevent accidental deactivation of the watchdog. After setting WDEN (CR 34) the CAN Flash mode can be left ($V_{TxDL} < V_{FlashL}$) and the Watchdog will remain deactivated (see *Figure 21*)

Figure 21. Sequence to disable/enable the watchdog in CAN Flash mode



In LIN Flash mode the maximum bitrate is increased to 100 kbit/s automatically (LIN_HS_EN = 1).

A transition from Flash modes to V1_standby or Vbat_standby mode is not possible.

At exit from Flash modes ($V_{TxDL} < V_{FlashL}$, $V_{TxDC} < V_{FlashL}$) no NReset pulse is generated. The watchdog starts with a Long Open Window (t_{LW}).

Note: Setting both TxDL and TxDC to high voltage levels (> V_{FlashH}) is not allowed. Communication at the respective TxD pin is not possible.

4.3.3 SW-debug mode

To allow software debugging, the watchdog can be deactivated by applying an external voltage to the DEBUG input pin ($V_{debug} > V_{diH}$).

In Debug mode, all device functionality and Operating modes are available. The watchdog is deactivated. At Exit from Debug mode ($V_{debug} < V_{diL}$) the watchdog starts with a Long Open Window.

Note: The device includes a test mode. This mode is activated by a dedicated sequence which includes a high voltage at the Debug Pin. The Debug Pin must be kept at nominal voltage levels in order to avoid accidental activation of the test mode.

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4.3.4 V1_standby mode

The transition from Active mode to V1_standby mode is controlled by SPI.

To supply the micro controller in a low power mode, the V1 voltage regulator remains active.

After the V1_standby command (CSN low to high transition), the device enters V1_standby mode immediately and the watchdog starts a Long Open Window (t_{LW}). The watchdog is deactivated as soon as the V1 load current drops below the I_{CMP} threshold ($I_{V1} < I_{cmp_fal}$).

The V1 load current monitoring can be deactivated by setting ICMP = 1. In this configuration the watchdog will be deactivated upon transition into V1_standby mode without monitoring the V1 load current.

Writing ICMP (CR 34) = 1 is only possible with the first SPI command after setting ICMP_CONFIG_EN (Config Reg) = 1.

The ICMP_CONFIG_EN bit is reset to 0 automatically with the next SPI command.

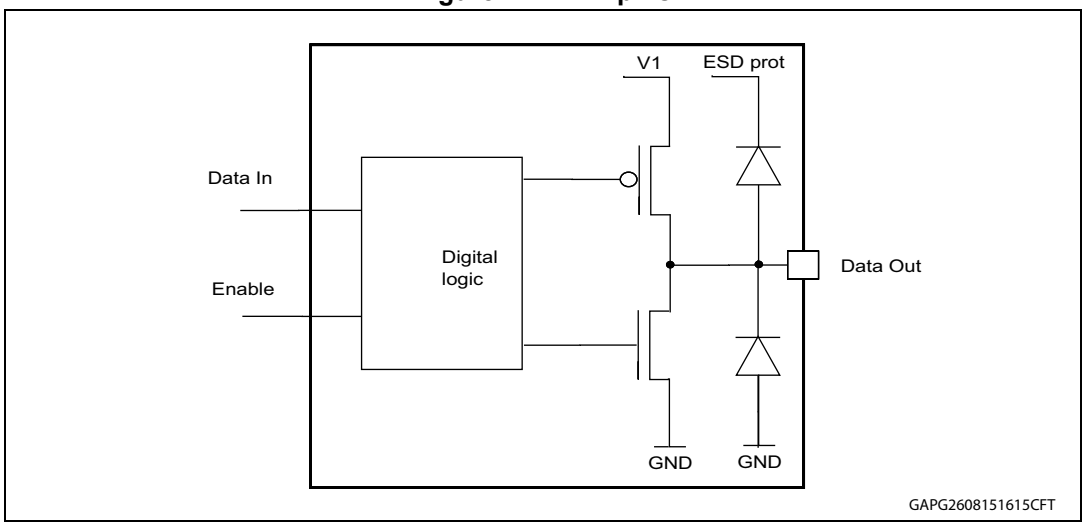
Power outputs (except OUT_HS & OUT15) are switched off in V1_standby mode. OUT_HS & OUT15 remain in the configuration programmed prior to the standby command in order to enable (cyclic) supply of external contacts. The timer signal (Timer1 or Timer2) can be mirrored to the NINT output pin during V1_standby mode.

CAN and LIN transmitters (TxDL, TxDC) are off.

Wake-up capability by CAN and LIN can be disabled by SPI. The CAN transceiver can be configured in Listen mode (TxDC disabled, RxDC enabled) in order to support pretended networking concepts (for details see *Section 4.10.6: Pretended networking*)

4.3.5 Interrupt

Figure 22. NINT pins



RxDL/NINT indicates:

- a wake-up event from V1_standby mode (except wake-up by CAN) and the programmable timer interrupt

  RxDL/NINT pin is pulled low for t = $t_{interrupt}$.

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RxDC/NINT indicates:

- Mode transitions of the CAN transceiver according to *Figure 31: CAN transceiver state diagram*
- CAN communication timeout (no CAN communication for t > $t_{Silence}$). The CANTO flag is set. This interrupt can be masked by SPI (CR2: CANTO_IRQ_EN).

  RxDC/NINT pin is pulled low for t = $t_{interrupt}$.

  See also *Section 4.3.6: CAN wake-up signalization*

NINT indicates:

- In Active mode:

  V_{SREG} dropped below the programmed early warning threshold in Control Register 3 (V_{SREG} < VSREG_EW_TH); feature is deactivated if VSREG_EW_TH is set to 0 V.

  In V1_standby mode
  - Programmable timer interrupt; An NINT pulse is generated at the beginning of the timer on-time (Timer 1 or Timer2)
  - CAN communication timeout (no CAN communication for t > $t_{Silence}$). The CANTO flag is set. This interrupt can be masked by SPI (CR2: CANTO_IRQ_EN).
  - Wake-up from V1_standby mode by any wake-up source

  NINT is pulled low for t = $t_{interrupt}$

In case of increasing V1 load current during V1_standby mode (I_{V1} > I_{cmp_ris}), the device remains in standby mode and the watchdog starts with a Long Open Window. No Interrupt signal is generated.

4.3.6 CAN wake-up signalization

Table 61. CAN wake-up signalization

Operating mode	Event	Mode transition	Status flag	Interrupt pin
Active	WUP or WUP/WUF(1)	Transition to TRX_Ready	WAKE_CAN WUP/WUF(1)	RxDC
	CAN Timeout	Transition to TRX_Sleep	CANTO	*RxDC* (2)
	WUP(3)	Transition into TRX_Bias	WUP	*RxDC* and *NINT*
V1_standby	WUP or WUP/WUF(1)	Transition into Active mode; TRX_Ready	WAKE_CAN WUP/WUF(1)	*RxDC* and *NINT*
	CAN Timeout	Transition to TRX_Sleep	CANTO	*RxDC* and *NINT* (2)
	WUP(3)	Transition into TRX_Bias	WUP	*RXDC* and *NINT*
V_{bat}_standby	WUP or WUP/WUF(1)	Transition into Active mode; TRX_Ready	WAKE_CAN WUP/WUF(1)	none
	CAN Timeout	Transition to TRX_Sleep	CANTO	

1. SW_EN = 0, PNW_EN = 0:
   — wake-up according ISO 11898-5:2007 (on WUP)
   — Flags: Wake_CAN, WUP
   SW_EN = 1:
   — wake-up according ISO 11898-6:2013 (on WUP/WUF combination)
   — After the reception of a wake-up pattern (WUP) the CAN Enhanced Voltage Biasing is turned on until a CAN timeout is detected
   — Flags: Wake_CAN, WUP, WUF

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2. Interrupt can be disabled by SPI (CANTO_IRQ_EN).
3. SW_EN = 0, PWN_EN = 1 (Pretended Networking mode)
   — no wake-up
   — after reception of a wake-up patter (WUP) the transceiver enters TRX Bias mode
   — Flags: WUP

Note: See also Figure 31: CAN transceiver state diagram.

4.3.7 VBAT_standby mode

The transition from Active mode to Vbat_standby mode is initiated by an SPI command. In Vbat_standby mode, the voltage regulators V1 and V2 (depending on configuration in CR 1), the power outputs (except OUT15 and OUT_HS) as well as LIN and CAN transmitters are switched off.

An NReset pulse is generated upon wake-up from Vbat_standby mode. At transition into Vbat_standby mode with selective wake-up enabled (SWEN = 1), the CAN transceiver is automatically set to TRX_standby configuration (RXEN = 0).

4.4 Wake-up from Standby modes

A wake-up from standby mode will switch the device to Active mode. This can be initiated by one or more of the following events:

Table 62. Wake-up events description

Wake up source	Description
LIN bus activity	Can be disabled by SPI
CAN bus activity	Can be disabled by SPI Selective Wake-up can be enabled and configured by SPI
Level change of WU	Can be configured or disabled by SPI
$I_{V1} > I_{cmp_ris}$	Device remains in *V1_standby mode* but watchdog is enabled (If I_{CMP} = 0). No interrupt is generated.
Timer Interrupt / Wake up of µC by TIMER	Programmable by SPI: – *V_1_standby mode*: configurable timer interrupt. NINT and RxDL/NINT interrupt signals are generated – *V_{bat}_standby mode*: device wakes up after programmable timer expiration, V1 regulator is turned on and NReset signal is generated
SPI Access	Always active (except in $V_{BAT_STANDBY}$ *mode*) Wake up event: CSN is low and first rising edge on CLK

To prevent the system from a deadlock condition (no wake up from standby possible) a configuration where the wake up by LIN and HS CAN are both disabled is not allowed. All wake-up sources are configured to default values in case of such invalid setting. The SPI Error Bit *SPIE (Global Status Byte)* is set.

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4.4.1 Wake up input

The WU input can be configured as wake-up source. The wake-up input is sensitive to any level transition (positive and negative edge) and can be configured for static or cyclic monitoring of the input voltage level.

For static contact monitoring, a filter time of t_{WU_STAT} is implemented. The filter is started when the input voltage passes the specified threshold V_{WU_THP} or V_{WU_THN}.

Cyclic contact monitoring allows periodical activation of the wake-up input to read the status of the external contact. The periodical activation can be configured to Timer 1 or Timer 2. The input signal is filtered with a filter time of t_{WU_CYC} after a delay (80% of the configured Timer on-time. A Wake-up will be processed if the status has changed versus the previous cycle. The buffered output OUT_HS can be used to supply the external contacts with the timer setting according to the cyclic monitoring of the wake-up input.

In standby modes, the input WU is configurable with an internal pull-up or pull-down current source according to the setup of the external contact. In Active mode the inputs have an internal pull down resistor (R_{WU_act}) and the input status can be read by SPI. Static sense should be configured before the read operation is started in order to reflect the actual input level.

4.5 Functional overview (truth table)

Table 63. Status of different functions/features vs operating modes

Function	Comments	Operating modes		
		Active mode	V_1-standby static mode (cyclic sense)	V_{bat}-standby static mode (cyclic sense)
Voltage regulator V1	V_{OUT} = 5 V	On	On(1)	Off
Voltage regulator V2	V_{OUT} = 5 V	On/ Off(2)	On(2) / Off	On(2) / Off
Reset generator		On	On	Off
Window watchdog	V_1 monitor	On	Off (on if $I_{V1} > I_{CMP}$ and I_{CMP} = 0)	Off
Wake up		Off	Active(3)	Active(3)
HS-cyclic supply	Oscillator time base	On / Off	On(2) / Off	On(2) / Off
LIN	LIN 2.2a	On	Off(4)	Off(4)
HS_CAN		On / Off(5)	Off(4)	Off(4)
Oscillator OSC1	2 MHz	On	On/Off(6)	On/Off(6)
Oscillator OSC2	32 MHz	ON	ON/Off(7)	ON/Off(7)
$V_{SREG-Monitor}$		On	(8)	(8)
$V_{S-Monitor}$		On	Off	Off

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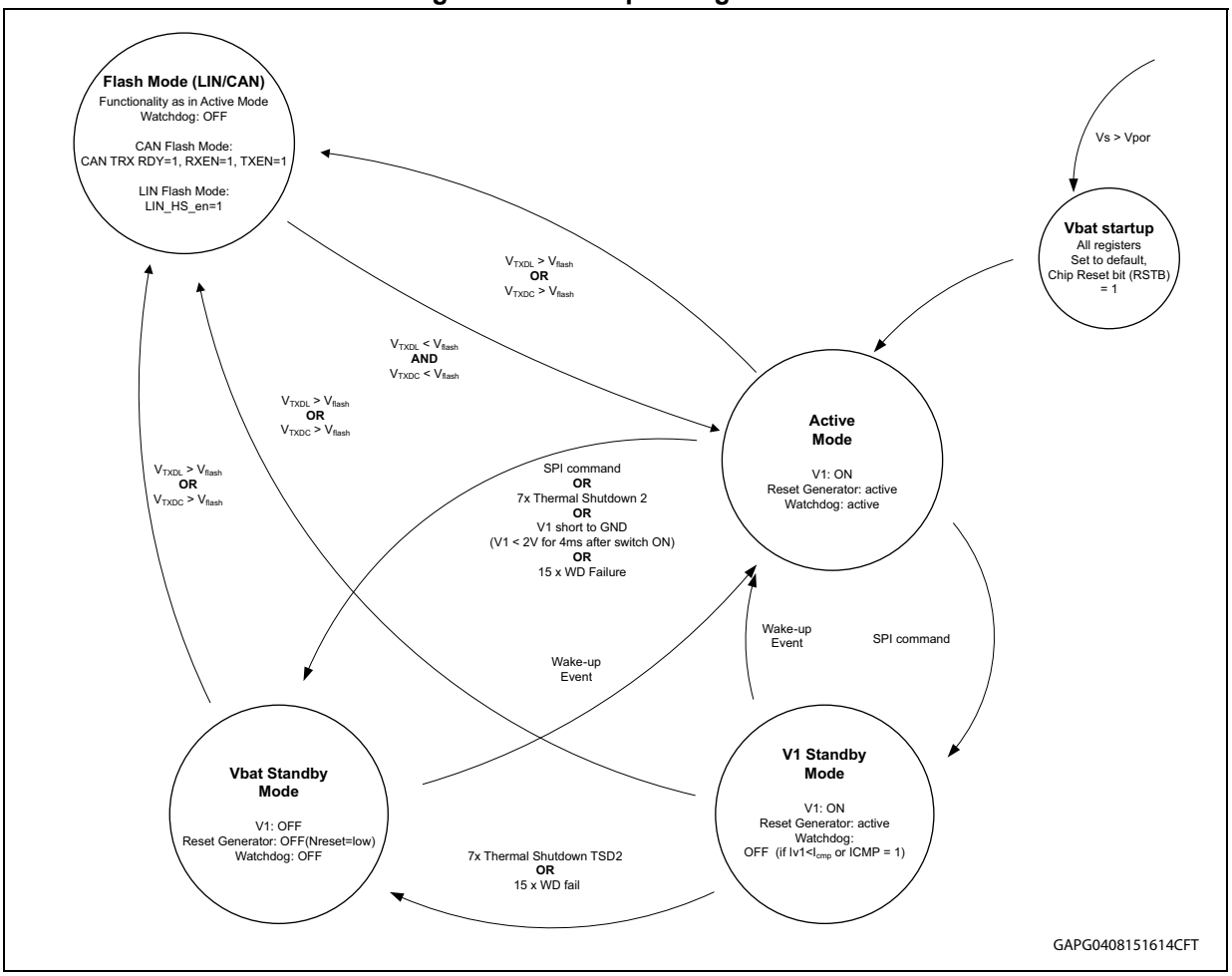
Table 63. Status of different functions/features vs operating modes (continued)

Function	Comments	Operating modes		
		Active mode	V_1-standby static mode (cyclic sense)	V_{bat}-standby static mode (cyclic sense)
H Bridge Gate Driver, EC control, bridge drivers, heater driver, all high-side drivers (except OUT_HS & OUT15) supplied by V_S		On/ Off(2)	Off	Off
Fail-safe low-side switches		On/ Off(9)	On	On
Short circuit protection for fail-safe low-side switches (in case LS is switched on)		On	On	On
OUT_HS & OUT15 (P-channel HS) supplied by V_{SREG}		On/ Off(2)	On/ Off (2)	On/ Off(2)
Charge pump		On	Off	Off
ADC (SPI read out and V_{SREG} early warning interrupt)		On	Off	Off
Thermal shutdown TSD2		On	On	Off
Thermal shutdown TSD1x for OUT_HS and OUT15 (P-channel HS)		On	On/ Off(2)	On/ Off(2)

1. Supply the processor in low current mode.
2. According to SPI setting and DIR.
3. Unless disabled by SPI.
4. The bus state is internally stored when going to standby mode. A change of bus state will lead to a wake-up after exceeding of internal filter time (if wake-up by LIN or CAN is not disabled by SPI). Selective Wake functionality if enabled by SPI
5. After power-on, the HS CAN transceiver is in CAN_TRX_SLEEP mode. It is activated by SPI command (CAN_GO_TRX_RDY= 1)
6. ON, if cyclic sense is enabled or during wake-up request.
7. ON if SWEN=1 (CAN partial networking enabled) and ongoing CAN communication on the bus.
8. Cyclic activation = pulsed ON during cyclic sense.
9. ON in Fail-Safe mode; if standby mode is entered with active Fail-safe mode the output remains ON in standby mode.

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Figure 23. Main operating modes



4.6 Configurable window watchdog

During normal operation, the watchdog monitors the micro controller within a programmable trigger cycle.

After power-on or standby mode, the watchdog is started with a timeout (Long Open Window t_{LW}). The timeout allows the micro controller to run its own setup and then to start the window watchdog by setting TRIG (CR1,ConfigReg) =1

Subsequently, the micro controller has to serve the watchdog by alternating the watchdog trigger bit TRIG (CR1,Config Reg) within the safe trigger area T_{SWX}.

The trigger time is configurable by SPI. A correct watchdog trigger signal will immediately start the next cycle. After 8 watchdog failures in sequence, the V1 regulator is switched off for t_{V1OFF}. After 7 additional watchdog failures the V1 regulator is turned off permanently and the device goes into Forced Vbat_standby mode. The status bit FORCED_SLEEP_WD (SR 1) is set. A wake-up is possible by any activated wake-up source.

After wake-up from Forced Vbat_standby mode and the watchdog trigger still fails, the device enters Forced Vbat_standby mode again after one Long Open Window.

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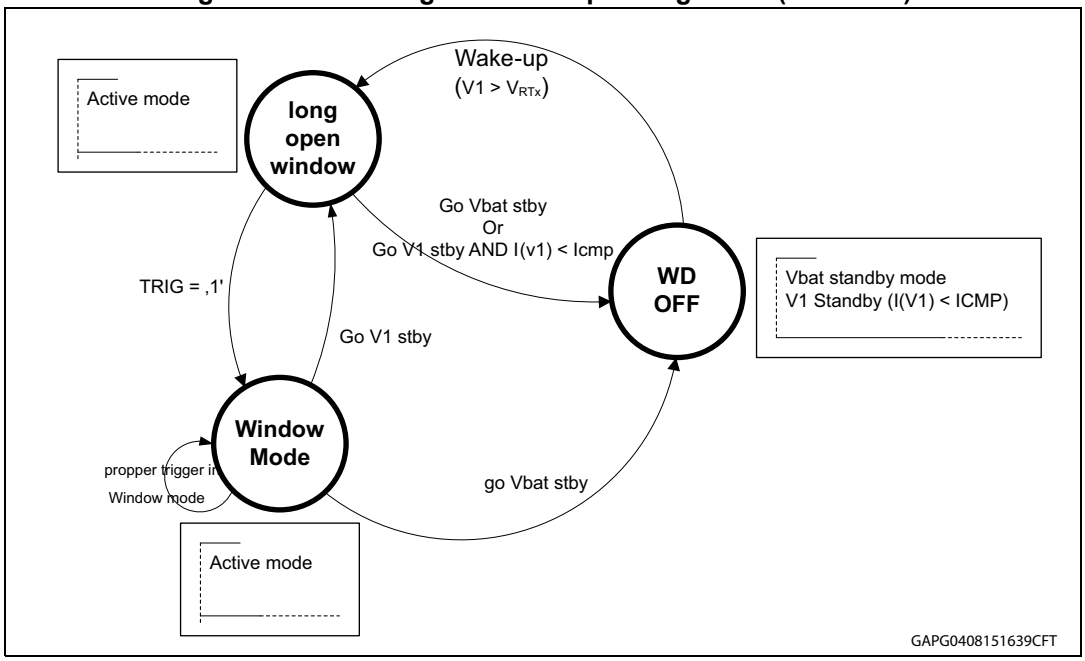
This actually produces an additional watchdog failure but the watchdog fail counter will remain at maximum value of 15 failures.

This sequence is repeated until a valid watchdog trigger event is performed by writing TRIG = 1.

In case of a Watchdog failure, the power outputs and V2 are switched off and the status bit WDFAIL (SR 1) is set to 1. A reset pulse is generated at NReset output and the device enters Fail-safe mode. Control registers are set to their Fail Safe values and the Fail-safe low-side switches are turned on. Please refer to chapter *Section 4.7: Fail-safe mode* for more details.

The following diagrams illustrate the Watchdog behavior of the devices. The diagrams are split into 3 parts. First diagram shows the functional behavior of the watchdog without any error. The second diagram covers the behavior covering all the error conditions, which can affect the watchdog behavior. *Figure 26: Watchdog in Flash mode* shows the transition in and out of Flash modes. *Figure 24*, *Figure 25* and *Figure 26* can be overlapped to get all the possible state transitions under all circumstances. For a better readability, they were split in normal operating, operating with errors and Flash mode.

Figure 24. Watchdog in normal operating mode (no errors)



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Figure 25. Watchdog with error conditions

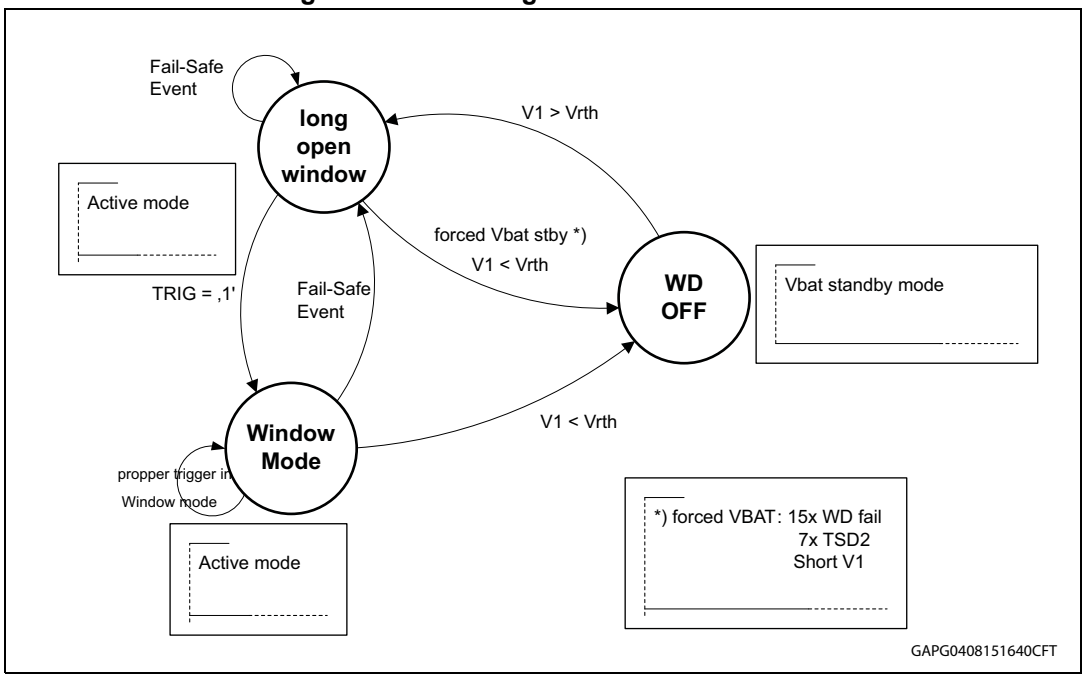
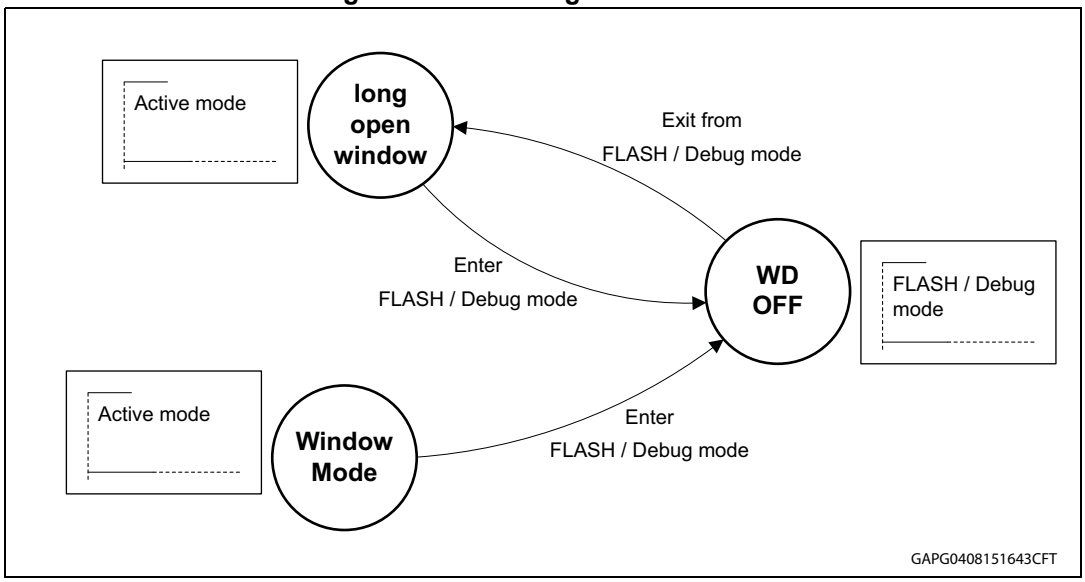


Figure 26. Watchdog in Flash mode



Note: Whenever the device is operated without servicing the mandatory watchdog trigger events, a sequence of 15 consecutive reset events is performed and the device enters the Forced_Vbat_Stby mode with bit FORCED_SLEEP_WD in SR1 set.

If the device is woken up after such a forced VBAT_Standby condition and the watchdog is still not serviced, the device, after one long open watchdog window will re-enter the same Forced_Vbat_Stby mode until the next wake up event. In this case, an additional watchdog failure is generated, but the fail counter is not cleared, keeping the maximum number of 15 failures. This sequence is repeated until a valid watchdog trigger event is performed by writing TRIG = 1.

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4.6.1 Change watchdog timing

The watchdog trigger time is configured by setting WD_TIME_x (CR 2). Writing to these bits is possible only using the first SPI command after setting WD_CONFIG_EN = 1 (Config Reg). The WD_CONFIG_EN bit is reset to 0 automatically with the next SPI command.

4.7 Fail-safe mode

4.7.1 Temporary failures

The devices enter Fail-safe mode in case of:

- Watchdog failure
- V1 turn on failure
  - V1 short ($V1 < V1_{fail}$ for $t > t_{V1short}$)
- V1 failure ($V1 < V_{RTxfalling}$ for $t > t_{V1FS}$)
- Thermal Shutdown TSD2

The Fail Safe functionality is also available in V1_Standby mode. During V1_Standby mode the Fail Safe mode is entered in the following cases:

- V1 failure ($V1 < V_{RTxfalling}$ for $t > t_{V1FS}$)
- Watchdog failure (if watchdog still running due to $I_{V1} > I_{cmp_fal}$)
- Thermal Shutdown TSD2

In Fail Safe mode the devices return to a fail safe state. The Fail Safe condition is indicated to the system in the Global Status Byte. The conditions during Fail Safe mode are:

- All outputs beside LS1_FSO and LS2_FSO are turned off
- All Control Registers are set to fail safe default values except:
  - SWEN (CR1<bit 7>): selective Wake-up enable
  - Partial Networking Configuration: CR23-CR29
- Write operations to Control Registers are blocked until the Fail Safe condition is cleared. The following bits are not WRITE protected:
  - TRIG (CR1<bit 0>, Config Register <bit 0>): watchdog trigger bit
  - V2_x (CR1<bit 4:5>): Voltage Regulator V2 control
  - CAN_GO_TRX_RDY (CR1<bit 8>): activation of CAN transceiver
  - CR2 (bit <8:23>): Timer1 and Timer2 settings
  - OUT_HS_x (CR5 <bit 0:3>): OUT_HS configuration
  - OUT15_x (CR6<bit 0:3>): OUT15 configuration
  - PWMx_freq_y (CR12): PWM frequency configuration
  - PWMx_DC_y (CR13 – CR17): PWM duty cycle configuration
- LIN and HS CAN transmitter and SPI remain on (transmitters are deactivated in case of thermal shutdown TSD1 (TSD1 cluster 5 or 6 in cluster mode)
- Corresponding Failure Bits in Status Registers are set
- FS Bit (Global Status Byte) is set
- LS1_FSO and LS2_FSO will be turned on
- Charge pump is switched off

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If the Fail Safe mode was entered it keeps active until the Fail safe condition is removed and the Fail Safe was read by SPI. Depending on the root cause of the Fail Safe operation, the actions to exit Fail safe mode are as shown in the following table.

Table 64. Temporary failures description

Failure source	Failure condition	Diagnosis	Exit from Fail-safe mode
Microcontroller (oscillator)	Watchdog early write failure or expired window	FS (Global Status Byte) =1; WDFAIL (SR 1) =1; WDFAIL_CNT_x (SR 1) = n+1	TRIG (CR 1) = 1 during long open window Read&Clear SR1
V1	Short at turn-on	FS (Global Status Byte) =1; FORCED_SLEEP_TSD2/V1SC (SR 1) =1	Wake-up; Read&Clear *SR1*
	Undervoltage	FS (Global Status Byte) = 1; V1UV (SR 1) = 1; V1fail (SR 2) = 1(1)	V1 >$V_{RTrising}$; Read&Clear *SR1*
Temperature	$T_j > T_{SD2}$	FS (Global Status Byte) = 1; TW (SR 2) = 1; TSD1 (SR 1) =1; TSD2 (SR 1) =1	$T_j < T_{SD2}$; Read&Clear *SR1*

1. If V1 < $V1_{fail}$ (for t > t_{V1fail}). The Fail-safe Bit is located in the Global Status Register.

4.7.2 Non-recoverable failures – forced Vbat_standby mode

If the Fail-safe condition persists and all attempts to return to normal system operation fail, the devices enter the *Forced* Vbat_standby mode in order to prevent damage to the system. The Forced Vbat_standby mode can be terminated by any wake-up source. The root cause of the Forced Vbat_standby mode is indicated in the SPI Status Registers. In forced Vbatstby mode and with Fail Safe conditions still present at wake-up, the Fails safe low side outputs LSx_FSO are switched OFF for 25us after the wake up event.

In Forced Vbat_standby mode, all Control Registers are set to power-on default values except:

- SWEN (CR1<bit 7>)
- All bits from CR23 to CR29
- CP_DITH_DIS (Config. Reg <bit 5>)

The Forced Vbat_standby mode is entered in case of:

- Multiple watchdog failures: FORCED_SLEEP_WD (SR 1) = 1 (15 x watchdog failure)
- Multiple thermal shutdown 2: FORCED_SLEEP_TSD2/V1SC (SR 1) = 1 (7 x TSD2)
- V1 short at turn-on (V1 < $V1_{fail}$ for t > $t_{V1short}$): FORCED_SLEEP_TSD2/V1SC (SR 1) = 1

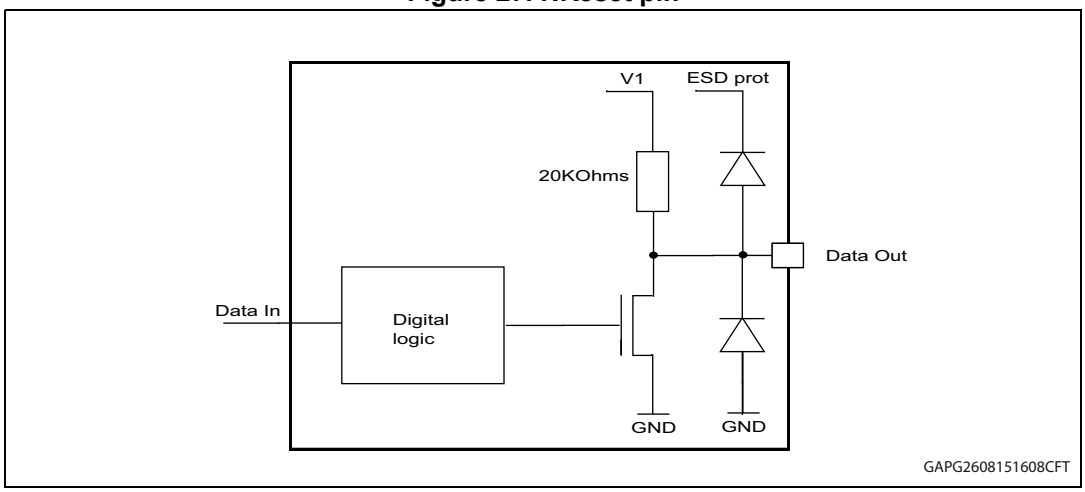
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Table 65. Non-recoverable failure

Failure source	Failure condition	Diagnosis	Exit from Fail-safe mode
Microcontroller (Oscillator)	15 consecutive Watchdog Failures	FS (Global Status Byte) = 1; WDFAIL (SR 1) = 1; FORCED_SLEEP_WD (SR 1) = 1	Wake-up; TRIG (CR 1) = 1 during long open window; Read&Clear SR1
V1	Short at turn-on	FS (Global Status Byte) = 1; FORCED_SLEEP_TSD2/V1SC (SR 1) = 1	Wake-up; Read&Clear SR1
Temperature	7 times TSD2	FS (Global Status Byte) =1; TW (SR 2) = 1; TSD1 (SR 1) = 1; TSD2 (SR 1) = 1; FORCED_SLEEP_TSD2/V1SC (SR 1) = 1	Wake-up; Read&Clear SR1

4.8 Reset output (NReset)

Figure 27. NReset pin



If V1 is turned on and the voltage exceeds the V1 reset threshold, the reset output *NReset* is pulled up to V1 by an internal pull-up resistor after a reset delay time (t_{V1R}). This is necessary for a defined start of the micro controller when the application is switched on. Since the *NReset* output is realized as an open drain output it is also possible to connect an external *NReset* open drain *NReset* source to the output. As soon as the NReset is released by the devices the watchdog starts with a long open window.

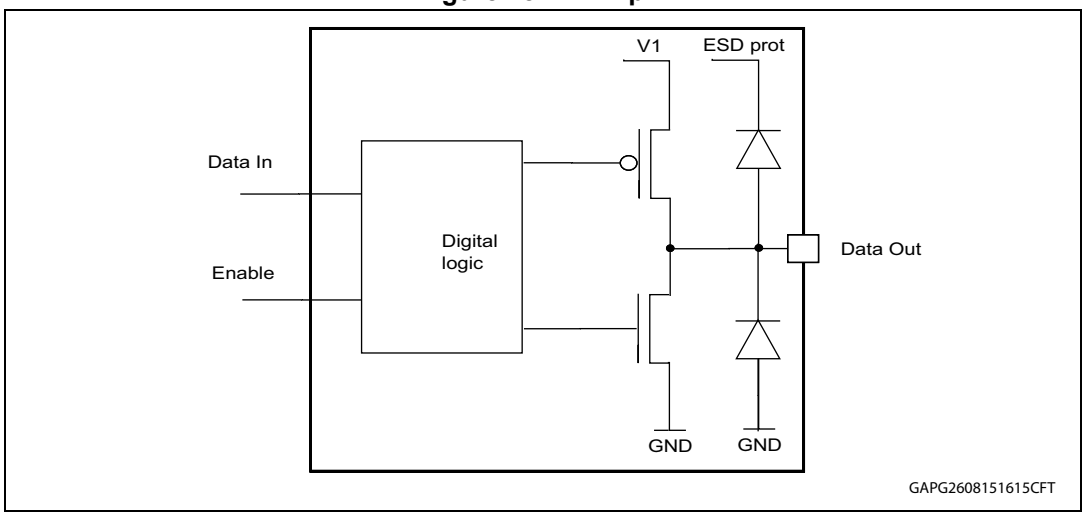
A reset pulse is generated in case of:

- V1 drops below $V_{RTxfalling}$ (configurable by SPI) for t > t_{UV1}
- Watchdog failure
- Turn-on of the V1 regulator (V_{SREG} Power-on or wake-up from Vbat_standby mode)

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4.9 LIN Bus Interface

Figure 28. RxDL pin



4.9.1 Features

- LIN 2.2a compliant (SAEJ2602 compatible) transceiver
- LIN Cell has been designed according to “Hardware requirements for transceivers (version 1.3)”
- Bitrate up to 20 kbit/s
- Dedicated LIN Flash mode with bitrate up to 100 kbit/s
- GND disconnection fail safe at module level
- Off mode: does not disturb network
- GND shift operation at system level
- Micro controller Interface with CMOS-compatible I/O pins
- Internal pull-up resistor
- Receive-only mode
- ESD and transient immunity according to ISO7637 and EN / IEC61000-4-2
- Matched output slopes and propagation delay
- Wake-up behaviour according to LIN2.2a and Hardware Requirements for LIN, CAN and Flexray Interfaces (version 1.3)

At $V_{SREG} > V_{POR}$ (i.e. V_{SREG} power-on reset threshold), the LIN transceiver is enabled. The LIN transmitter is disabled in case of the following errors:

- Dominant TxDL time out
- LIN permanent recessive
- Thermal shutdown 1
- V_{SREG} overvoltage/ undervoltage

The LIN receiver is not disabled in case of any failure condition.

The default bitrate of the transceiver allows communication up to 20 kbit/s. To enable fast flashing via the LIN bus, the transceiver can be operated in high speed mode by setting bit LIN_HS_EN (Config Reg) = 1. This feature is enabled automatically in LIN Flash mode.

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4.9.2 Error handling

The devices LIN transceiver provides the following 3 error handling features.

Dominant TxDL time out

If TXD_L is in dominant state (low) for t > $t_{dom(TXDL)}$ the transmitter will be disabled, the status bit LIN_TXD_DOM (SR 2) will be set.

The transmitter remains disabled until the status bit is cleared.

The TxD dominant timeout detection can be disabled via SPI (LIN_TXD_TOUT_EN = 0).

Permanent recessive

If TXD_L changes to dominant (low) state but RXD_L signal does not follow within t < t_{LIN} the transmitter will be disabled, the status bit LIN_PERM_REC (SR 2) will be set.

The transmitter remains disabled until the status bit is cleared.

Permanent dominant

If the bus state is dominant (low) for t > tdom(bus) a bus permanent dominant failure will be detected. The status bit LIN_PERM_DOM (SR 2) will be set.

The transmitter will not be disabled.

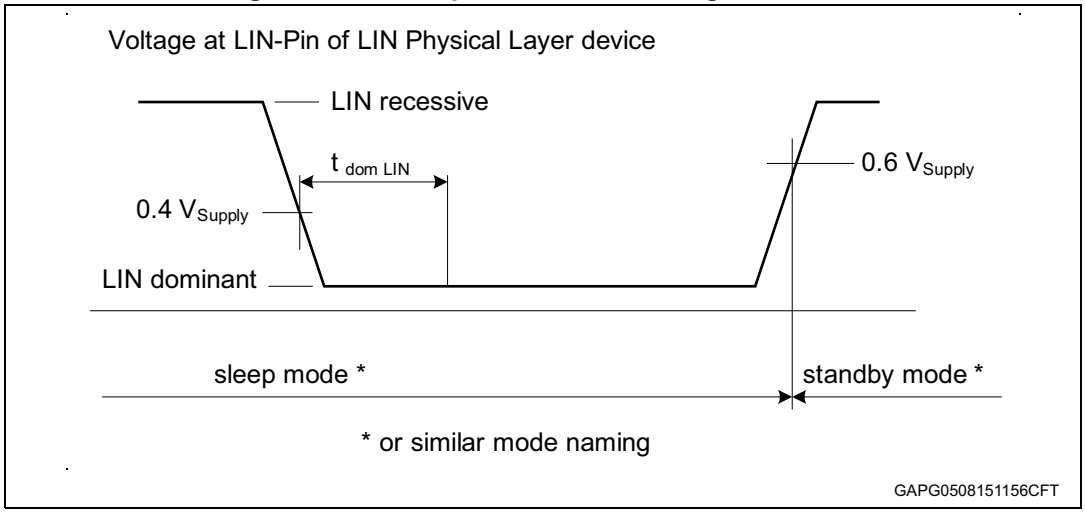
4.9.3 Wake up from Standby modes

In low power modes (V1_standby mode and Vbat_standby mode) the devices can receive two types of wake up signals from the LIN bus (configurable by SPI bit LIN_WU_CONFIG (Config Reg)):

- Recessive-Dominant-recessive pattern with t > t_{dom_LIN} (default, according LIN 2.2a)
- State Change recessive-to-dominant or dominant-to-recessive (according LIN 2.1)

Pattern Wake-up (default)

Figure 29. Wake-up behavior according to LIN 2.2a



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Status change wake-up - Recessive-to-dominant

Normal wake-up can occur when the LIN transceiver was set in standby mode while LIN was in recessive (high) state. A dominant level at LIN for t > t_{LINBUS}, will switch the devices to Active mode.

Status change wake-up - Dominant-to-recessive

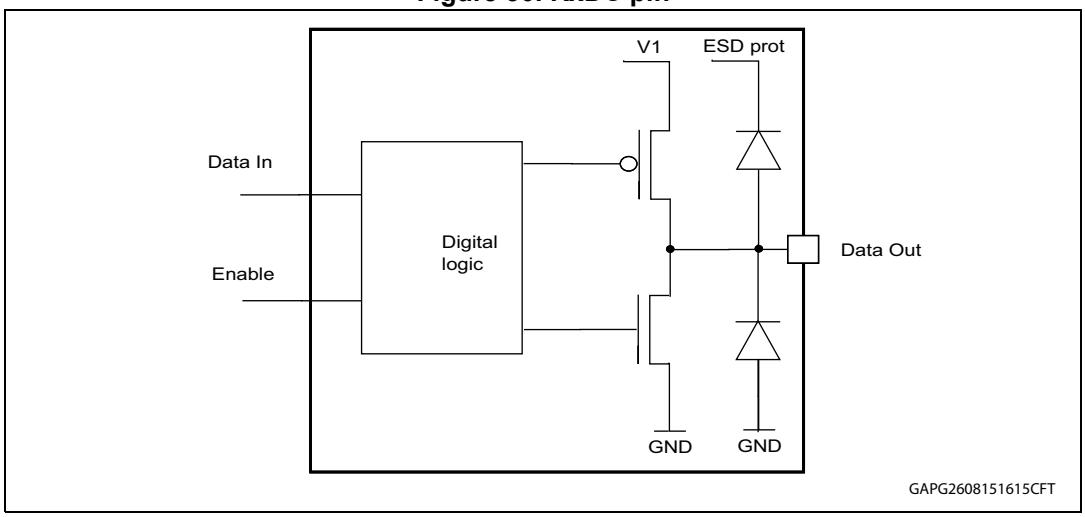
If the LIN transceiver was set in standby mode while LIN was in dominant (low) state, recessive level at LIN for t > t_{LINBUS}, will switch the devices to Active mode.

4.9.4 Receive-only mode

The LIN transmitter can be disabled in Active mode by setting the bit LIN_REC_ONLY (CR2). In this mode it is possible to listen to the bus but not sending to it.

4.10 High-speed CAN bus transceiver

Figure 30. RxDC pin



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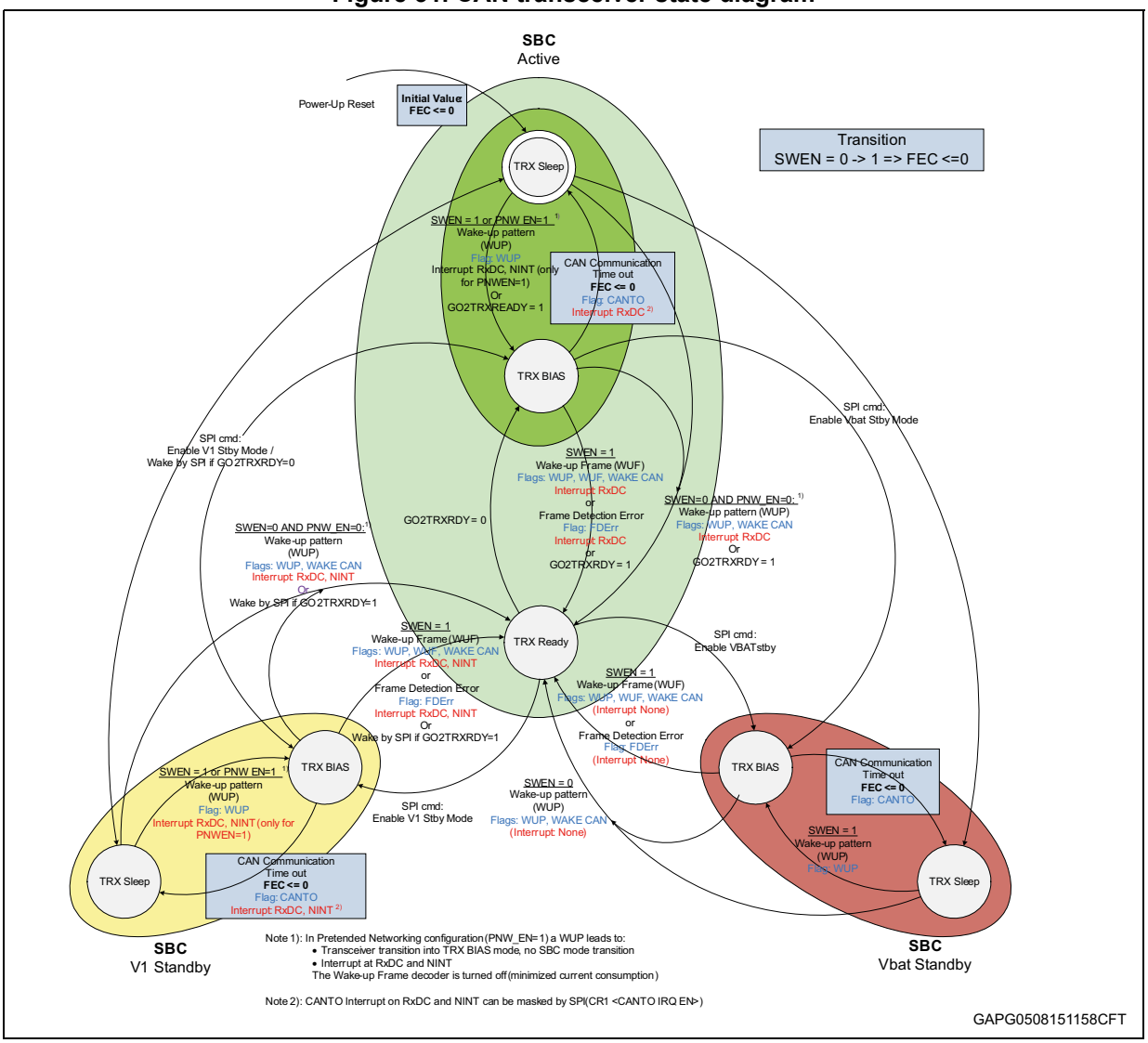
4.10.1 Features:

- ISO 11898-2:2003 and ISO 11898-5:2007 compliant
- ISO 11898-6: 2013 compliant (Selective wake-up functionality up to 500kbps); only L99DZ100GP
- HS-CAN cell has been designed according to “Requirements for partial networking (version 2.2)” and “Hardware requirements for transceivers (version 1.3)”
- Supports pretended networking
- Listen mode (transmitter disabled)
- Enhanced Voltage Biasing according to ISO 11898-6:2013
- SAE J2284 compliant
- Bitrate up to 1Mbit/s.
- Function range from -27V to +40V DC at CAN pins.
- GND disconnection fail safe at module level.
- GND shift operation at system level.
- Micro controller Interface with CMOS compatible I/O pins.
- ESD and transient immunity according to ISO7637 and EN / IEC61000-4-2
- Matched output slopes and propagation delay

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4.10.2 CAN transceiver operating modes

Figure 31. CAN transceiver state diagram



TRX Ready State

In this state the bus-biasing is on. The Frame Decoder is enabled, if selective wake-up is activated (SWEN=1).

The transmitter and receiver can be configured by SPI (RXEN, TXEN) as follows:

- TRX Standby (default): transmitter and receiver disabled
- TRX Listen: transmitter disabled, receiver enabled
- TRX Normal: transmitter enabled, receiver enabled

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TRX BIAS State

In this transceiver state the bus biasing is on and the Automatic Voltage Biasing is active (i.e. transceiver enters TRX_Sleep at t > $t_{Silence}$ and turns off the biasing). The Frame Decoder is enabled if selective wake-up is configured (SWEN = 1).

The CAN transmitter is disabled. The receiver can be configured by SPI (RXEN) as follows:

- TRX Standby(default): receiver disabled
- TRX Listen: receiver enabled

The CAN receiver is capable to detect a wake-up pattern (WUP) or a wake-up frame (WUF; if selective wake-up is enabled by SWEN = 1). In V1_standby mode and Active mode, a wake-up is indicated to the micro-controller by an interrupt signal and the transceiver enters TRX_Ready State (receiver and transmitter according to setting of TXEN and RXEN). After serving the interrupt, the micro controller can enable the receiver and transmitter by setting TXEN = 1 and RXEN = 1.

In case of a Frame-Detect-Error (FDERR = 1), an automatic wake up is performed and the selective wakeup feature is disabled (SWEN = 0).

TRX SLEEP State

After Power-on the CAN transceiver enters TRX_Sleep state. In this state, the CAN transceiver is disabled and the biasing is turned off. Transmitter and receiver are disabled (TRX_Standby state). The CAN selective wakeup reference oscillator and the Frame Decoder are off. After the detection of CAN communication (WUP), an interrupt signal is generated and the transceiver enters TRX_Ready state (if SWEN = 0) or TRX_BIAS state (if SWEN = 1). Receiver and transmitter are configured according to setting of TXEN and RXEN.

TRX_Sleep state is entered automatically after a CAN communication timeout (see *Section 4.10.3: Automatic voltage biasing*)

4.10.3 Automatic voltage biasing

The Automatic Voltage Biasing is described in ISO 11898-6:2013. This feature is active in all transceiver low-power modes independent of the SBC operating modes and independent if selective wake-up is enabled or not (SWEN (CR 1) = 0 or SWEN = 1).

If there has been no activity on the bus for longer than $t_{Silence}$, the bus lines are biased towards 0V via the receiver input resistors R_{in}. If wake-up activity on the bus lines is detected (Wake-up pattern, WUP), the bus lines are biased to $V_{CANHrec}$ respectively $V_{CANLrec}$ via the internal receiver input resistors R_{in}. The biasing is activated not later than t_{Bias}.

4.10.4 Wake-up by CAN

The devices support 2 wake-up modes. The selective wake-up according to ISO 11898-6:2013 or the wake-up by any bus activity according to ISO 11898-2:2003/-5:2007 (default configuration). The wake-up behavior can be configured by SPI.

Wake-up by CAN pattern (WUP)

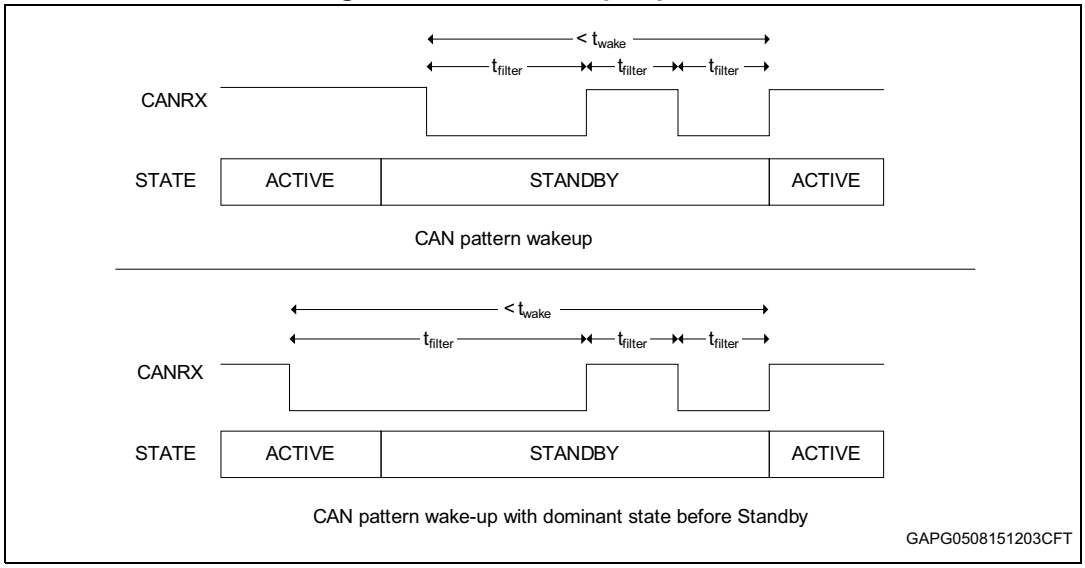
The default setting for the wake up behavior after Power-on reset is the wake-up by regular communication on the CAN bus according to ISO 11898-5:2007 (SWEN=0). When the CAN

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transceiver is in a low power mode (TRX_BIAS or TRX_Sleep) the device can be woken up by sending 2 consecutive dominant bits separated by a recessive bit.

A wake-up can be detected if the CAN transceiver was set in standby mode while the CAN bus was in recessive (high) state or dominant (low) state (see *Figure 32: CAN wake up capabilities*).

Figure 32. CAN wake up capabilities



For details, see *Figure 31: CAN transceiver state diagram*

Wakeup by Wake-up Frame (WUF)

In this configuration, the wake-up behavior is according to ISO 11898-6:2013. This option is activated by setting SWEN = 1. Upon reception of a valid wake up frame, an interrupt will be generated, the WUF flag will be set and the device enters Active mode.

The included frame-error-counter according ISO 11898-6:2013 is reset whenever selective wake-up is set to enable and whenever $t_{Silence}$ has expired in TRX BIAS state (i.e. either on a transition SWEN = 0 -> 1 or on a transition TRX BIAS -> TRX Sleep).

To detect a failure of the internal 32 MHz oscillator, the following mechanism is implemented. While selective wake-up is enabled a timer is started with each recessive to dominant edge. After 64 µs and with periodic 64 µs timer, a check is performed on CAN PN oscillator activity, and if an oscillator fail is detected, the osc_mon bit is set to ‘1’. Subsequently the device enters wake-up mode according to ISO11898-5 (wake-up pattern wake-up).

For details, see *Figure 31: CAN transceiver state diagram*.

Sequence for enabling selective wakeup

After Power-On-Reset, the selective wakeup feature is disabled. The PN Configuration Registers have to be read and verified by the microcontroller in order to ensure a valid configuration. A read operation to Registers CR23 to CR29 is required to allow enabling the selective wake-up feature (set SWEN=1). SWRD_CRxx (SR 12) bits will indicate a valid read operation. The SWRD_CRxx bits are reset to 0 with every WRITE operation.

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When all SWRD_CRxx bits are set, SWEN can be set to enable the Selective Wakeup function. In case SYSERR (SR 12) is set while Selective Wakeup is enabled, the Selective Wakeup will be disabled automatically. In case SYSERR is set, enabling the Selective Wakeup function is blocked. While selective wake-up is enabled (SWEN = 1), writing to CR23 – CR29 is blocked but SWEN is reset to ‘0’. To re-configure the selective wakeup feature, it is recommended to set SWEN = 0 before writing to CR23 - CR29.

Wake up from TRX SLEEP

If the CAN Transceiver is in TRX_Sleep state the CAN frame detection logic is disabled. The wake up can be done in two steps. To enable the CAN frame detection logic a wake up pattern must be sent on the bus. With the detection of the wake up pattern an automatic state transition to TRX_BIAS State is done. WUP flag is set. In TRX_BIAS State the CAN frame detection logic is enabled. If there is no bus communication for longer than $t_{Silence}$ an automatic state transition to TRX_Sleep state will be done and the CAN frame detection logic will be disabled. At frame error counter (FECNT_x) overflow, a wake up will be performed and the selective wakeup feature will be disabled. For details, see *Figure 31: CAN transceiver state diagram*.

4.10.5 CAN looping

If CAN_LOOP_EN (CR 2) is set the TxD_C input is mapped directly to the RxD_C pin. This mode can be used in combination with the CAN Receive-only mode, to run diagnosis for the CAN protocol handler of the micro controller.

4.10.6 Pretended networking

To support pretended networking concepts, the devices can be configured as follows:

- V1_standby mode or Active mode (if watchdog is required)
- Pretended Networking enabled (PNW_EN (CR 2) = 1)

In this configuration, the microcontroller is supplied by V1 in low current mode. The CAN Automatic Voltage Biasing is active. Upon incoming CAN messages, the biasing is turned on (TRX_BIAS State) and an interrupt is generated. If the device is in V1_standby mode it remains in this mode.

The incoming CAN frames are passed to the microcontroller via the RxD_C signal line for decoding.

4.10.7 CAN error handling

The devices provide the following four error handling features. After Power-on Reset (V_S > V_{POR}) the CAN transceiver is disabled. The transceiver is enabled by setting CAN_GO_TRX_RDY(CR 1) = 1. The CAN transmitter will be disabled automatically in case of the following errors:

- Dominant TxD_C time out
- CAN permanent recessive
- RxD_C permanent recessive
- Thermal Shutdown 1

The CAN receiver is not disabled in case of any failure condition.

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Dominant TxDC time out

If TXD_C is in dominant state (low) for t > $t_{dom(TxDC)}$ the transmitter will be disabled, CAN_TXD_DOM (SR 2) will be latched and can be read and optionally cleared by SPI. The transmitter remains disabled until the status register is cleared.

CAN Permanent Recessive

If TXD_C changes to dominant (low) state but CAN bus does not follow for 4 times, the transmitter will be disabled, CAN_PERM_REC (SR 2) will be latched and can be read and optionally cleared by SPI. The transmitter remains disabled until the status register is cleared.

CAN Permanent Dominant

If the bus state is dominant (low) for t > t_{CAN} a permanent dominant status will be detected. CAN_PERM_DOM (SR 2) will be latched and can be read and optionally cleared by SPI. The transmitter will not be disabled.

RXDC Permanent Recessive

If RXD_C pin is clamped to recessive (high) state, the controller is not able to recognize a bus dominant state and could start messages at any time, which results in disturbing the overall bus communication. Therefore, if RXD_C does not follow TXD_C for 4 times the transmitter will be disabled. CAN_RXD_REC (SR 2) will be latched and can be read and optionally cleared by SPI. The transmitter remains disabled until the status register is cleared.

4.11 Serial Peripheral Interface (ST SPI Standard)

A 32-bit SPI is used for bi-directional communication with the microcontroller.

The SPI is driven by a microcontroller with its SPI peripheral running in following mode: CPOL = 0 and CPHA = 0. For this mode input data is sampled by the low to high transition of the clock CLK, and output data is changed from the high to low transition of CLK.

This device is not limited to microcontroller with a built-in SPI. Only three CMOS-compatible output pins and one input pin is needed to communicate with the device. A fault condition can be detected by setting CSN to low. If CSN = 0, the DO-Pin reflects the global error flag (fault condition) of the device.

- Chip Select Not (CSN)

  The input Pin is used to select the serial interface of this device. When CSN is high, the output Pin (DO) is in high impedance state. A low signal activates the output driver and a serial communication can be started.

  The state during CSN = 0 is called a communication frame.

  If CSN = low for t > $t_{CSNfail}$ the DO output is switched to high impedance in order to not block the signal line for other SPI nodes.

- Serial Data In (DI)

  The input Pin is used to transfer data serial into the device. The data applied to the DI is sampled at the rising edge of the CLK signal and shifted into an internal 32-bit shift register. At the rising edge of the CSN signal the content of the shift register is transferred to Data Input Register. The writing to the selected Data Input Register is only enabled if exactly 32-bit are transmitted within one communication frame (i.e. CSN

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low). If more or less clock pulses are counted within one frame the complete frame is ignored. This safety function is implemented to avoid an activation of the output stages by a wrong communication frame.

Note: Due to this safety functionality a daisy chaining of SPI is not possible. Instead, a parallel operation of the SPI bus by controlling the CSN signal of the connected IC's is recommended.

- Serial Data Out (DO)

  The data output driver is activated by a logical low level at the CSN input and will go from high impedance to a low or high level depending on the global error flag (fault condition). The first rising edge of the CLK input after a high to low transition of the CSN Pin will transfer the content of the selected status register into the data out shift register. Each subsequent falling edge of the CLK will shift the next bit out.
- Serial Clock (CLK)

  The CLK input is used to synchronize the input and output serial bit streams. The data input (DI) is sampled at the rising edge of the CLK and the data output (DO) will change with the falling edge of the CLK signal. The SPI can be driven with a CLK Frequency up to 4 MHz.

4.12 Power supply failure

4.12.1 V_S supply failure

V_S overvoltage

If the supply voltages V_S reaches the overvoltage threshold V_{SOV}:

- LIN remains enabled
- CAN remains enabled
- OUT1 to OUT_14 are turned off (default).

  The shutdown of outputs may be disabled by SPI (VS_OV_SD_EN (CR 3) = 0)
- Charge pump is disabled (and is switched on automatically in case the supply voltage recovers to normal operating voltage)
- H-bridge gate driver and heater MOSFET gate driver are switched into sink condition
- ECV is switched in high impedance state and ECDR is discharged by $R_{ECDRDIS}$ (to ensure the gate of the external MOSFET is discharged => EC mode considered as off)
- Recovery of outputs after overvoltage condition is configurable by SPI:
  - VS_LOCK_EN (CR 3) = 1: outputs are off until Read&Clear VS_OV (SR 2).
  - VS_LOCK_EN (CR 3) = 0: outputs turned on automatically after V_S overvoltage condition has recovered.
- The overvoltage bit VS_OV (SR 2) is set and can be cleared with a ‘Read&Clear’ command. The overvoltage bit is reset automatically if VS_LOCK_EN (CR 3) = 0 and the overvoltage condition has recovered.

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V_S undervoltage

If the supply voltage V_S drops below the under voltage threshold voltage (V_{SUV}):

- LIN remains enabled
- CAN remains enabled
- OUT1 to OUT14 are turned off (default).
- The shutdown of outputs may be disabled by SPI (VS_UV_SD_EN (CR 3) = 0)
- Heater MOSFET gate driver switched into sink condition
- ECV is switched in high impedance state and ECDR is discharged by $R_{ECDRDIS}$ (to ensure the gate of the external MOSFET is discharged => EC mode considered as off)
- Recovery of outputs after undervoltage condition is configurable by SPI:
  - VS_LOCK_EN (CR 3) = 1: outputs are off until Read&Clear VS_UV (SR 2).
  - VS_LOCK_EN (CR 3) = 0: outputs turned on automatically after V_S undervoltage condition has recovered.
- The undervoltage bit VS_UV (SR 2) is set and can be cleared with a ‘Read&Clear’ command. The undervoltage bit is removed automatically if VS_LOCK_EN (CR 3) = 0 and the undervoltage condition has recovered.

4.12.2 V_{SREG} supply failure

V_{SREG} overvoltage

If the supply voltages V_{SREG} reaches the overvoltage threshold V_{SREG_OV}:

- LIN is switched to high impedance
- CAN remains enabled
- OUT15 and OUT_HS are turned off (default).

  The shutdown of outputs may be disabled by SPI ($V_{SREG_OV_SD_EN}$ (CR 3) = 0)
- Recovery of outputs after overvoltage condition is configurable by SPI:
  - VSREG_LOCK_EN (CR 3) = 1: outputs are off until Read&Clear VSREG_OV (SR 2).
  - VSREG_LOCK_EN (CR 3) = 0: outputs turned on automatically after V_{SREG} overvoltage condition has recovered.
- The overvoltage bit VSREG_OV (SR 2) is set and can be cleared with a ‘Read&Clear’ command. The overvoltage bit is reset automatically if VSREG_LOCK_EN (CR 3) = 0 and the overvoltage condition has recovered.

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V_{SREG} undervoltage

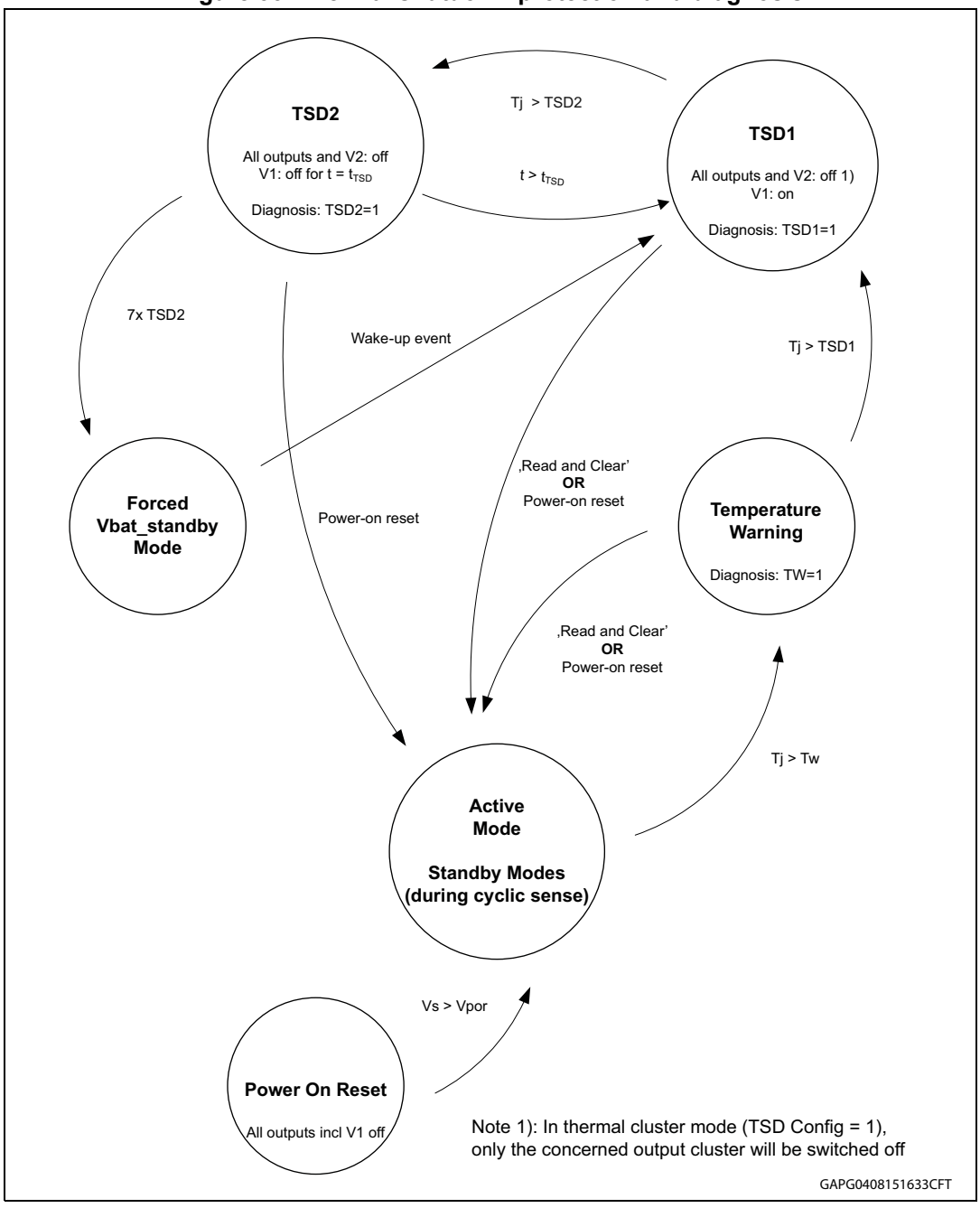
If the supply voltage V_{SREG} drops below the under voltage threshold voltage (V_{SREG_UV}):

- LIN is switched to high impedance
- CAN remains enabled
- OUT15 and OUT_HS are turned off (default).
- The shutdown of outputs may be disabled by SPI (VSREG_UV_SD_EN (CR 3) = 0)
- Recovery of outputs after undervoltage condition is configurable by SPI:
  - VSREG_LOCK_EN (CR 3) = 1: outputs are off until Read&Clear VSREG_UV (SR 2).
  - VSREG_LOCK_EN (CR 3) = 0: Outputs turned on automatically after V_{SREG} undervoltage condition has recovered.
- The undervoltage bit VSREG_UV (SR 2) is set and can be cleared with a ‘Read&Clear’ command. The undervoltage bit is removed automatically if VSREG_LOCK_EN (CR 3) = 0 and the undervoltage condition has recovered.

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4.13 Temperature warning and thermal shutdown

Figure 33. Thermal shutdown protection and diagnosis



Note: The Thermal State machine will recover the same state were it was before entering Standby mode. In case of a TSD2 it will enter TSD1 state.

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4.14 Power outputs OUT1..15 and OUT_HS

The component provides a total of 6 half bridges outputs OUT1..6 to drive motors and 10 stand alone high-side outputs OUT7..15 and OUT_HS to drive e.g. LED's, bulbs or to supply contacts. All high-side outputs beside OUT_HS and OUT15 are supplied by the pin VS and OUT_HS and OUT15 are supplied by the buffered supply V_{SREG}. OUT_HS is intended to be used as contact supply. Beside OUT15 and OUT_HS the high-side switches can be activated only in case of running charge pump. OUT15 and OUT_HS can be activated also in standby modes.

All high-side and low-side outputs switch off in case of:

- V_S (V_{SREG}) overvoltage and undervoltage (depending on configuration, see *Section 4.12.2: VSREG supply failure*)
- Overcurrent (depending on configuration, auto recovery mode (see below)
- Overtemperature (TSD1x/ cluster or single mode)
- Fail safe event
- Loss of GND at SGND pin

In case of overcurrent or overtemperature (TSD1_CLx (SR 6)) condition, the drivers will switch off. The according status bit will be latched and can be read and optionally cleared by SPI. The drivers remain off until the status is cleared. In case overvoltage/ undervoltage condition, the drivers will be switched off. The according status bit will be latched and can be read and optionally cleared by SPI. If VSREG_LOCK_EN (CR 3) respectively VS_LOCK_EN (CR 3) are set, the drivers remain off until the status is cleared. If the VS_LOCK_EN or VSREG_LOCK_EN) bit is set to 0, the drivers will switch on automatically if the error condition disappears. Undervoltage and overvoltage shutdown can be disabled by SPI. In case of open-load condition, the according status register will be latched. The status can be read and optionally cleared by SPI. The high and low-side outputs are not switched off in case of open-load condition.

For OUT1..OUT8 and OUT_HS the auto recovery feature (OUTx_OCR (CR 7)) can be enabled. If these bits are set to 1 the driver will automatically restart from an overload condition. This overload recovery feature is intended for loads which have an initial current higher than the overcurrent limit of the output (e.g. Inrush current of cold light bulbs). The SPI bits OUTx_OCR_ALERT (SR4) indicate that the output reached auto-recovery condition.

Note: The maximum voltage and current applied to the High-side Outputs is specified in the 'Absolute Maximum Ratings'. Appropriate external protection may be required in order to respect these limits under application conditions. In case of outputs switch off due to loss of ground at SGND pin, the device has to be re-started through a power off on both V_S and V_{SREG}.

Each of the stand alone high-side driver outputs OUT7 … OUT15 and OUT_HS can be driven with an internally generated PWM signal, an internal Timer or with DIR1 respectively DIR2. See table below.

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Table 66. Power output settings

OUTx_3	OUTx_2	OUTx_1	OUTx_0	Description
0	0	0	0	OFF
0	0	0	1	ON
0	0	1	0	Timer1 output is controlled by timer1; starting with ON phase after timer restart
0	0	1	1	Timer2 output is controlled by timer2; starting with ON phase after timer restart
0	1	0	0	PWM1
0	1	0	1	PWM2
0	1	1	0	PWM3
0	1	1	1	PWM4
1	0	0	0	PWM5
1	0	0	1	PWM6
1	0	1	0	PWM7
1	0	1	1	PWM8
1	1	0	0	PWM9
1	1	0	1	PWM10
1	1	1	0	DIR1
1	1	1	1	DIR2

4.15 Auto-recovery alert and thermal expiration

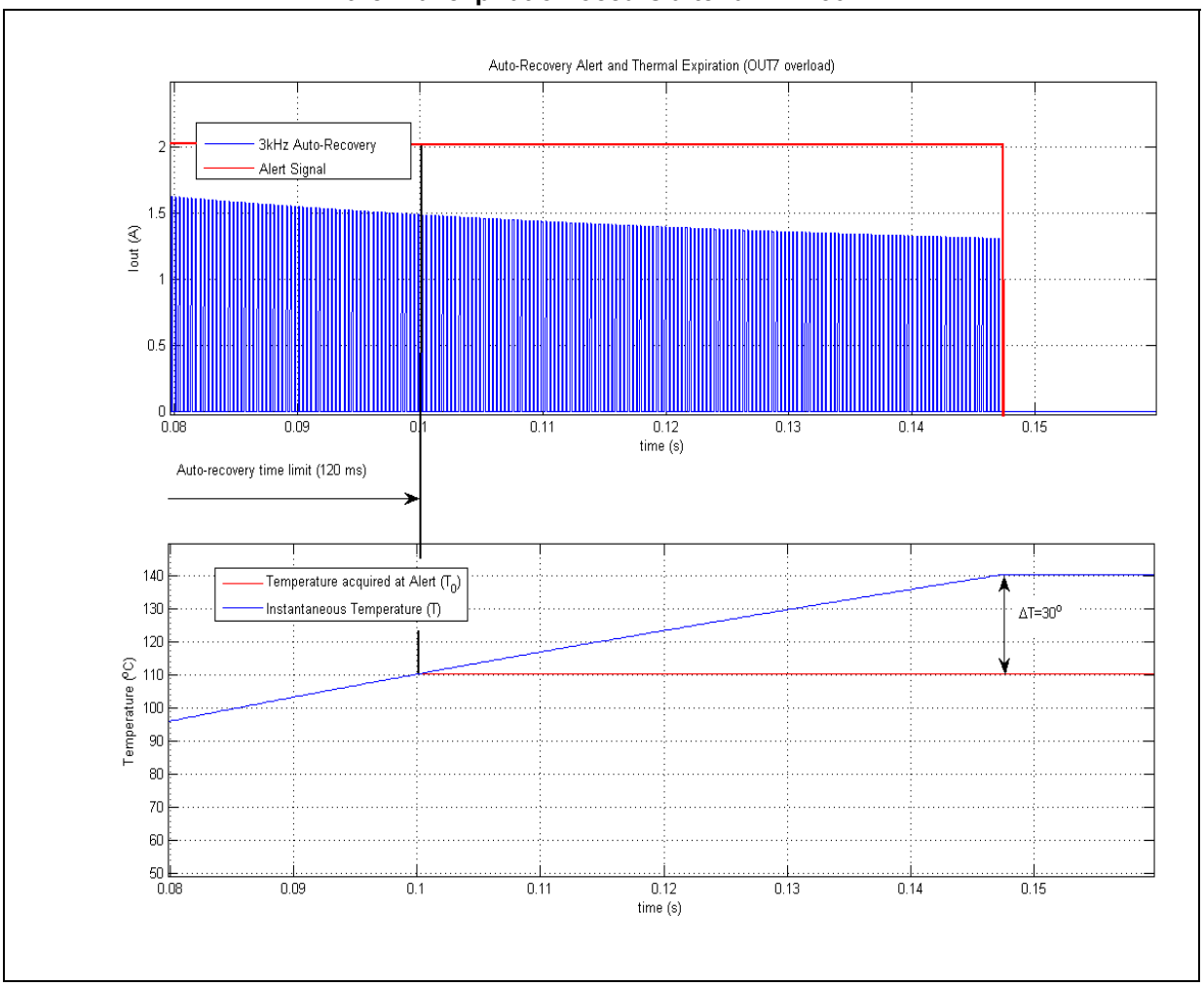
The thermal expiration feature provides a robust protection against possible microcontroller malfunction, switching off a given channel if continuously driven in auto-recovery. If the temperature of the related cluster increases by more than 30 °C after reaching the auto-recovery time t_{AR}, the channel is switched off. The thermal expiration status bit OUTx_TH_EX (SR 3) is set.

During auto-recovery condition, OUTx_OCR_ALERT (SR 4) is set. The Alert bit indicates that an overload condition (load in-rush, short-circuit, etc) is present.

The thermal expiration feature is controlled by SPI (OUTx_OCR_THX_EN (CR 8).

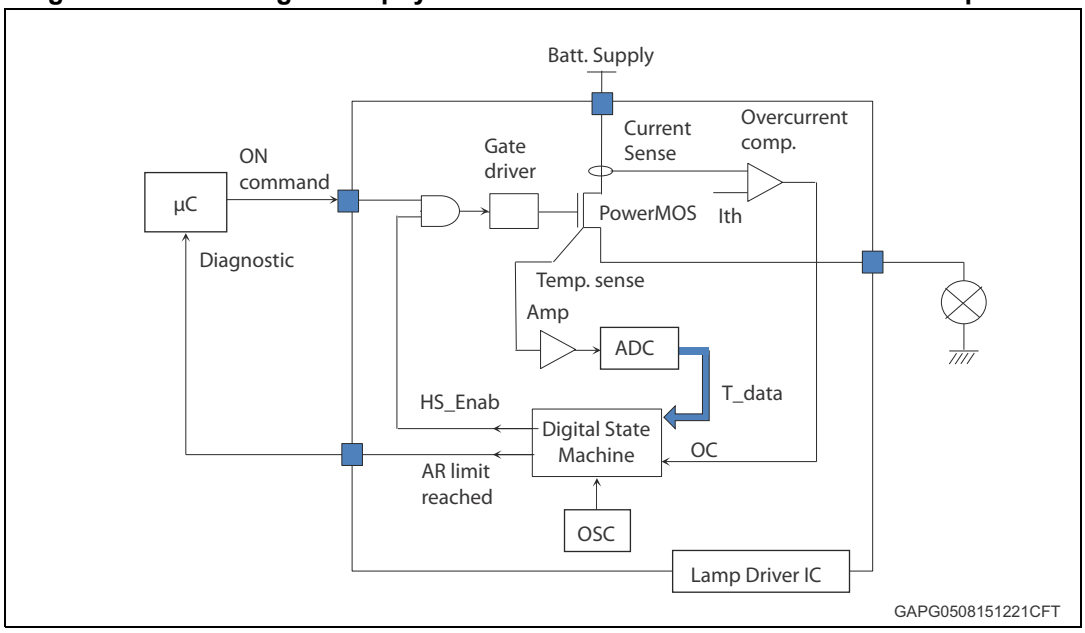
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Figure 34. Example of long auto-recovery on OUT7. Temperature acquisition starts after t_{AR}, thermal expiration occurs after a ΔT = 30°



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Figure 35. Block diagram of physical realization of AR alert and thermal expiration

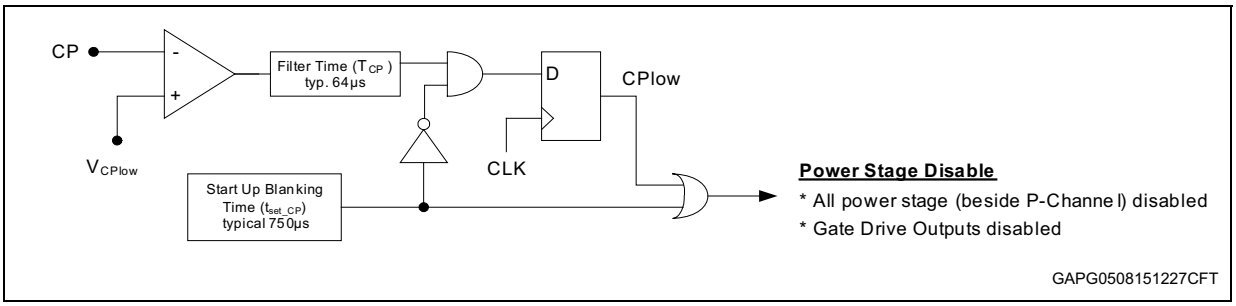


4.16 Charge pump

The charge pump uses two external capacitors, which are switched with f_{CP}. The output of the charge pump has a current limitation. In standby mode and after a thermal shutdown has been triggered the charge pump is disabled. If the charge pump output voltage remains too low for longer than T_{CP}, the power-MOS outputs and the EC-control are switched off. The H-bridge MOSFET gate drivers and the Heater MOSFET gate driver are switched to resistive low and CP_LOW (SR 2) is set. This bit has to be cleared to reactivate the drivers. If the bit CP_LOW_CONFIG (Configuration Register 0x3F) is set to '1', CP_LOW (SR2) behaves as a 'live' bit and the outputs are re-activated automatically upon recovery of the charge pump output voltage.

In case of reaching the overvoltage shutdown threshold V_{SOV} the charge pump is disabled and automatically restarted after V_S recovered to normal operating voltage.

Figure 36. Charge pump low filtering and start up implementation



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4.17 Inductive loads

Each of the half bridges is built by internally connected high-side and low-side power DMOS transistors. Due to the built-in reverse diodes of the output transistors, inductive loads can be driven at the outputs OUT1 to OUT6 without external freewheeling diodes. The high-side drivers OUT7 to OUT15 and OUT_HS are intended to drive resistive loads only. Therefore only a limited energy (E < 1 mJ) can be dissipated by the internal ESD-diodes in freewheeling condition. For inductive loads (L > 100 µH) an external freewheeling diode connected between GND and the corresponding output is required. The low-side driver at ECV does not have a freewheel diode built into the device.

4.18 Open-load detection

The open-load detection monitors the load current in each activated output stage. If the load current is below the open-load detection threshold for t > t_{OL_OUT} the corresponding open-load bit OUTx_OL (SR 5) is set in the status register.

4.19 Overcurrent detection

An overcurrent condition is detected after a filter time of t_{FOC} and is indicated by the status bit OUTx_OC (SR 3). In case of overcurrent, the corresponding driver switches off to reduce the power dissipation and to protect the integrated circuit. If the outputs are not configured in recovery mode, the microcontroller has to clear the according status bits to reactivate the corresponding drivers.

4.20 Current monitor

The current monitor sources a current image of the power stage output current at the current monitor pin CM, which has a fixed ratio (I_{CMr}) of the instantaneous current of the selected high-side driver. The signal at output CM is blanked for t_{cmb} after switching on the driver until correct settlement of the circuitry. The bits CM_SELx (CR 7) define which of the outputs is multiplexed to the current monitor output CM. The current monitor output allows a more precise analysis of the actual state of the load rather than the detection of an open-load or overload condition. For example, it can be used to detect the motor state (starting, free running, stalled). The current monitor output is enabled after the current-monitor blanking time, when the selected output is switched on. If this output is off, the current monitor output is in high impedance mode. The current monitor can be deactivated by CM_EN (CR 7).

4.21 PWM mode of the power outputs

Description see *Section 7.3: Status register overview*.

4.22 Cross-current protection

The six half-brides of the device are cross-current protected by an internal delay time. If one driver (LS or HS) is turned off, the activation of the other driver of the same half bridge will be automatically delayed by the crosscurrent protection time. After the crosscurrent

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protection time is expired the slew-rate limited switch-off phase of the driver is changed to a fast turn-off phase and the opposite driver is turned-on with slew-rate limitation. Due to this behavior, it is always guaranteed that the previously activated driver is completely turned off before the opposite driver starts to conduct.

4.23 Programmable soft-start function to drive loads with higher inrush current

Loads with start-up currents higher than the overcurrent limits (e.g. inrush current of lamps, start current of motors) can be driven by using the programmable soft-start function (i.e. overcurrent recovery mode). Each driver has a corresponding overcurrent recovery bit OUTx_OCR (CR 7). If this bit is set, the device automatically switches the outputs on again after a programmable recovery time. The PWM modulated current will provide sufficient average current to power up the load (e.g. heat up the bulb) until the load reaches operating condition. The PWM frequency is defined by CR7<8:12> setting.

The device itself cannot distinguish between a real overload (e.g. short-circuit condition) and a load characterized by operation currents exceeding the short-circuit threshold.

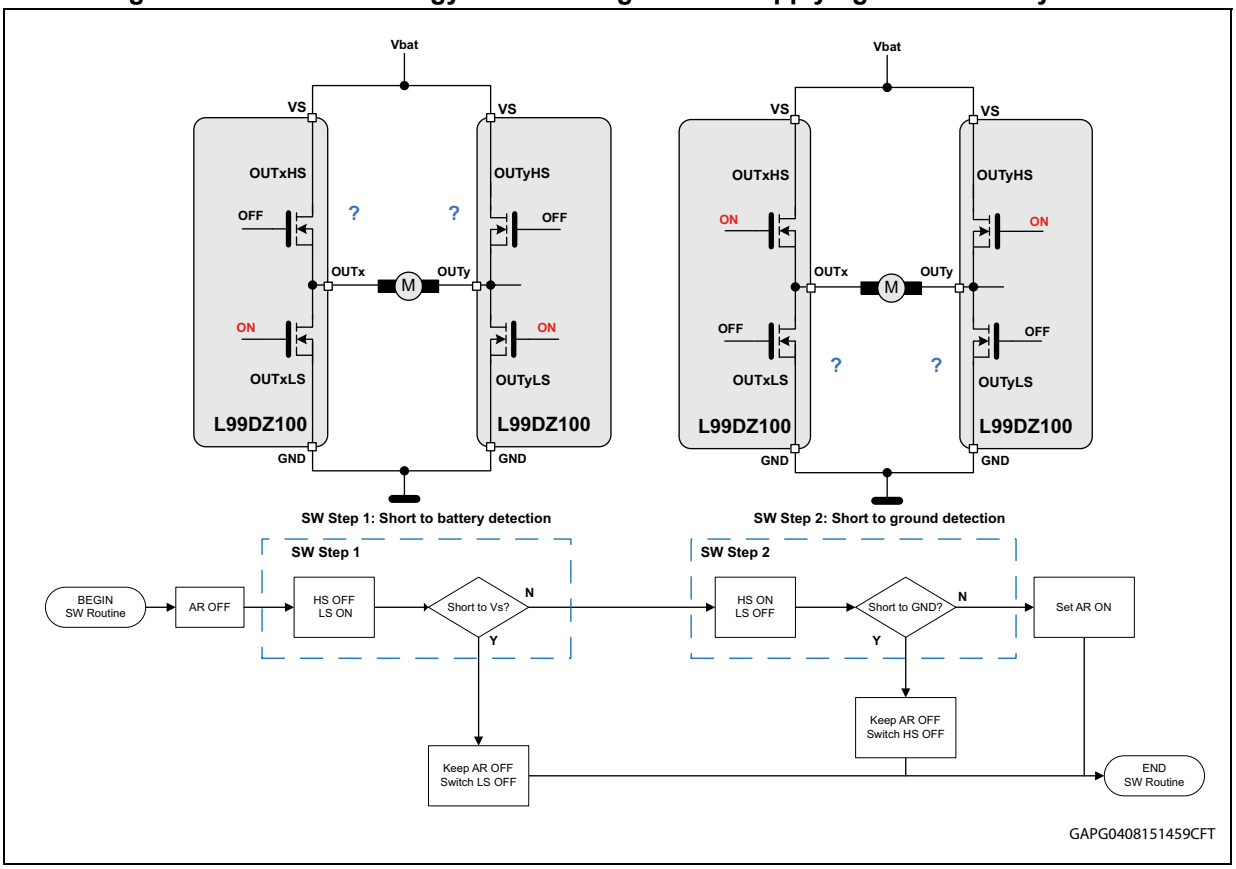
Examples are non-linear loads like a light bulb used on the HS outputs or a motor used on the half bridge output with inrush and stall currents that shall be limited by the auto recovery feature.

For the bulb, a real overload condition can only be qualified by time. For overload detection the microcontroller can switch on the light bulbs by setting the overcurrent recovery bit for the first e.g. 50 ms. After clearing the recovery bit, the output will be switched off automatically if the overload condition remains.

For the half bridges the high current can be present during all motor activation and another SW strategy must be applied to identify a SC to GND or Supply. Before running the motor e.g. with a first SPI command all bridge LS are switched on (without auto recovery functionality / cleared overcurrent recovery bit), all HS are switched off and a SC to Battery can be diagnosed. With a next SPI command, all HS are switched on (without auto recovery functionality/ cleared overcurrent recovery bit) and all LS are switched off. In this sequence, a short to GND can be diagnosed. If in both sequences no overload condition is identified, the motor can be run by switching on the according HS and LS each configured in auto recovery mode (see *Figure 37: Software strategy for half bridges before applying auto-recovery mode*). Such sequence can be applied before any motor activation to identify SC just before operating the motor (in case the delay due to the 2 additional SPI commands is not limiting the application) or in case of power up of the system resp. applied on a certain time base.

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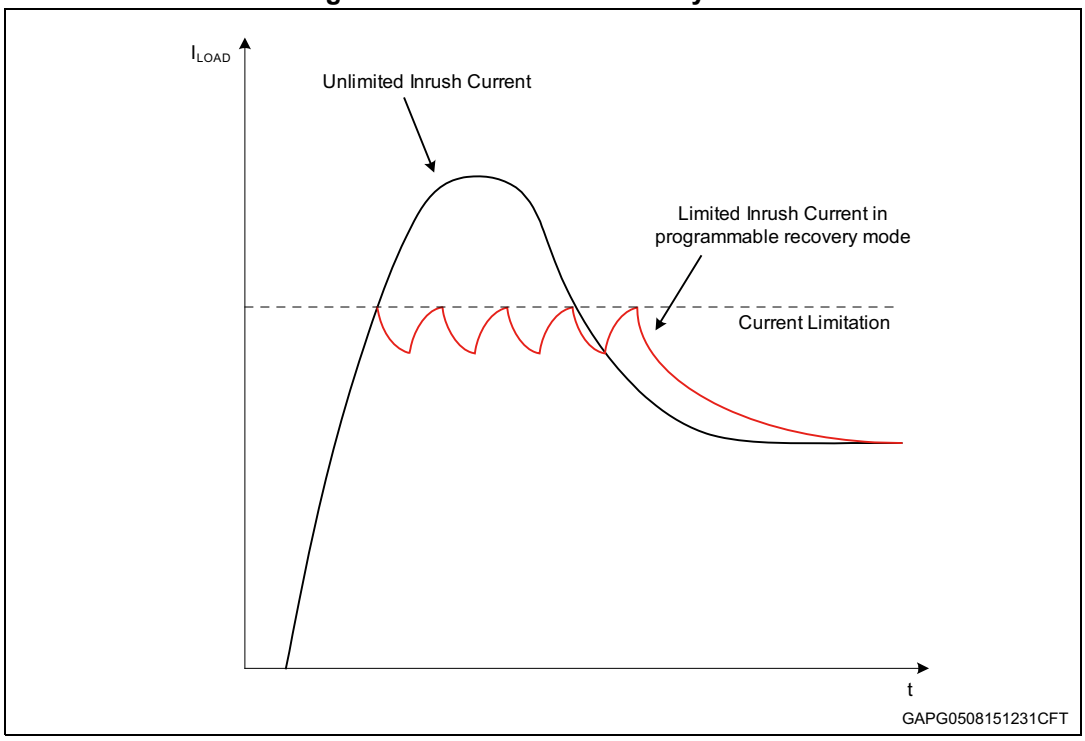
Figure 37. Software strategy for half bridges before applying auto-recovery mode



As soon as an output reaches auto-recovery condition, OUTx_OCR_ALERT (SR 4)) is set. The Alert bit indicates that an overload condition (load in-rush, short-circuit, etc) is present.

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Figure 38. Overcurrent recovery mode



4.24 H-bridge control

The PWMH and DIRH inputs control the drivers of the external H-bridge transistors. In single Motor mode the motor direction can be chosen with the direction input (DIRH), the duty cycle and frequency with the PWMH input (single mode). With the SPI bits SD (CR 10) and SDS (CR 10) four different slow-decay modes (via drivers and via diode) can be selected using the high-side or the low-side transistors. Unconnected inputs are defined by internal pull-down current.

Alternatively, the bridge can be driven in half bridge mode (dual mode). By setting the dual mode bit DM (Config Reg) = 1, both half-bridges can be controlled independently.

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Table 67. H-bridge control truth table

	Control pins		Control bits				Failure bits					Output pins				Motor config	Comment
Nb	DIRH	PWMH	HEN	SD	SDS	DM	CP_LOW	VS_OV	VS_UV	DS	TSD1	GH1	GL1	GH2	GL2		
1	x	x	0	x	x	x	x	x	x	x	x	RL	RL	RL	RL		H-bridge disabled
2	x	x	1	x	x	0	1	0	0	0	0	RL	RL	RL	RL	Single	Charge pump voltage too low
3	x	x	1	x	x	0	0	x	x	x	1	RL	RL	RL	RL		Thermal shutdown
4	x	x	1	x	x	0	0	1	0	0	0	L	L	L	L		Overvoltage
5	x	x	1	x	x	0	0	0	0	1	0	L(1)	L(1)	L(1)	L(1)		Short-circuit(1)
6	0	1	1	x	x	0	0	0	0	0	0	L	H	H	L		Bridge H2/L1 on
7	x	0	1	0	0	0	0	0	0	0	0	L	H	L	H		Slow-decay mode LS1 and LS2 on
8	0	0	1	0	1	0	0	0	0	0	0	L	H	L	L		Slow-decay mode LS1 on
9	1	0	1	0	1	0	0	0	0	0	0	L	L	L	H		Slow-decay mode LS2 on
10	1	1	1	x	x	0	0	0	0	0	0	H	L	L	H		Bridge H1/L2 on
11	x	0	1	1	0	0	0	0	0	0	0	H	L	H	L		Slow-decay mode HS1 and HS2 on
12	0	0	1	1	1	0	0	0	0	0	0	L	L	H	L		Slow-decay mode HS1 on
13	1	0	1	1	1	0	0	0	0	0	0	H	L	L	L		Slow-decay mode HS2 on
14	0	0	1	1	0	1	0	0	0	0	0	L	L	L	L	Dual	Half bridge mode
15	0	1	1	1	0	1	0	0	0	0	0	L	L	L	H		
16	1	0	1	1	0	1	0	0	0	0	0	L	H	L	L		
17	1	1	1	1	0	1	0	0	0	0	0	L	H	L	H		
18	0	0	1	0	1	1	0	0	0	0	0	L	L	L	L		
19	0	1	1	0	1	1	0	0	0	0	0	L	L	H	L		
20	1	0	1	0	1	1	0	0	0	0	0	H	L	L	L		
21	1	1	1	0	1	1	0	0	0	0	0	H	L	H	L		
22	0	0	1	1	1	1	0	0	0	0	0	H	L	H	L		
23	0	1	1	1	1	1	0	0	0	0	0	H	L	L	H		
24	1	0	1	1	1	1	0	0	0	0	0	L	H	H	L		
25	1	1	1	1	1	1	0	0	0	0	0	L	H	L	H		

1. Only the H-bridge (low-side and high-side), in which one MOSFET is in short-circuit condition is switched off. Both MOSFETs of the other H-bridge remain active and driven by DIRH and PWMH.

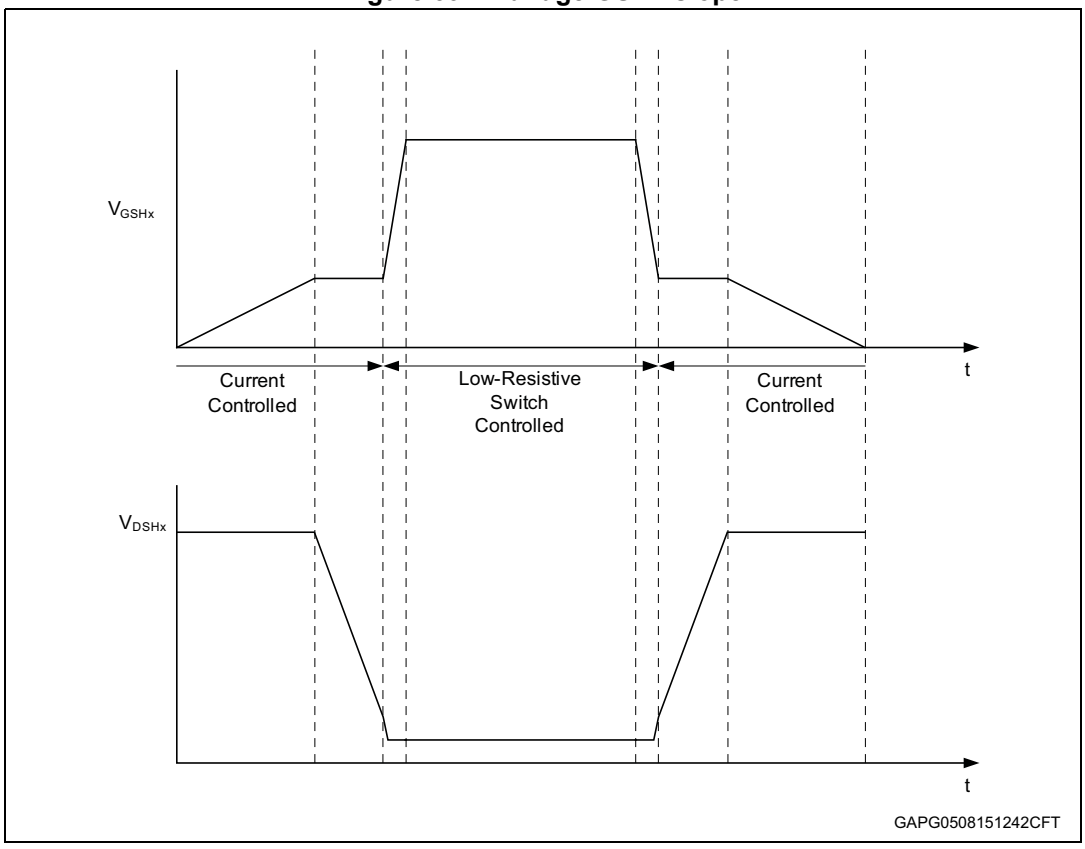
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During watchdog long-open window, the H-bridge drivers are forced off until the first valid watchdog trigger in window mode (setting TRIG = 0 during safe window). The Control Registers remain accessible during long open window.

4.25 H-bridge driver slew-rate control

The rising and falling slope of the drivers for the external high-side Power-MOS can be slew rate controlled. If this mode is enabled the gate of the external high-side Power-MOS is driven by a current source instead of a low-impedance output driver switch as long as the drain-source voltage over this Power-MOS is below the switch threshold. The current is programmed using the bits SLEW_x<4:0> (CR 10), which represent a binary number. This number is multiplied by the minimum current step. This minimum current step is the maximum source-/sink-current ($I_{GHxrmax}$ / $I_{GHxfmax}$) divided by 31. Programming SLEW_x <4:0> to 0 disables the slew rate control and the output is driven by the low-impedance output driver switch.

Figure 39. H-bridge GSHx slope



4.26 Resistive low

The resistive output mode protects the devices and the H-bridge in the standby mode and in some failure modes (thermal shutdown TSD1 (SR 1), charge pump low CP_LOW (SR 2) and DI pin stuck at ‘1’ SPI_INV_CMD (SR 2)). When a gate driver changes into the resistive output mode due to a failure a sequence is started. In this sequence the concerning driver is

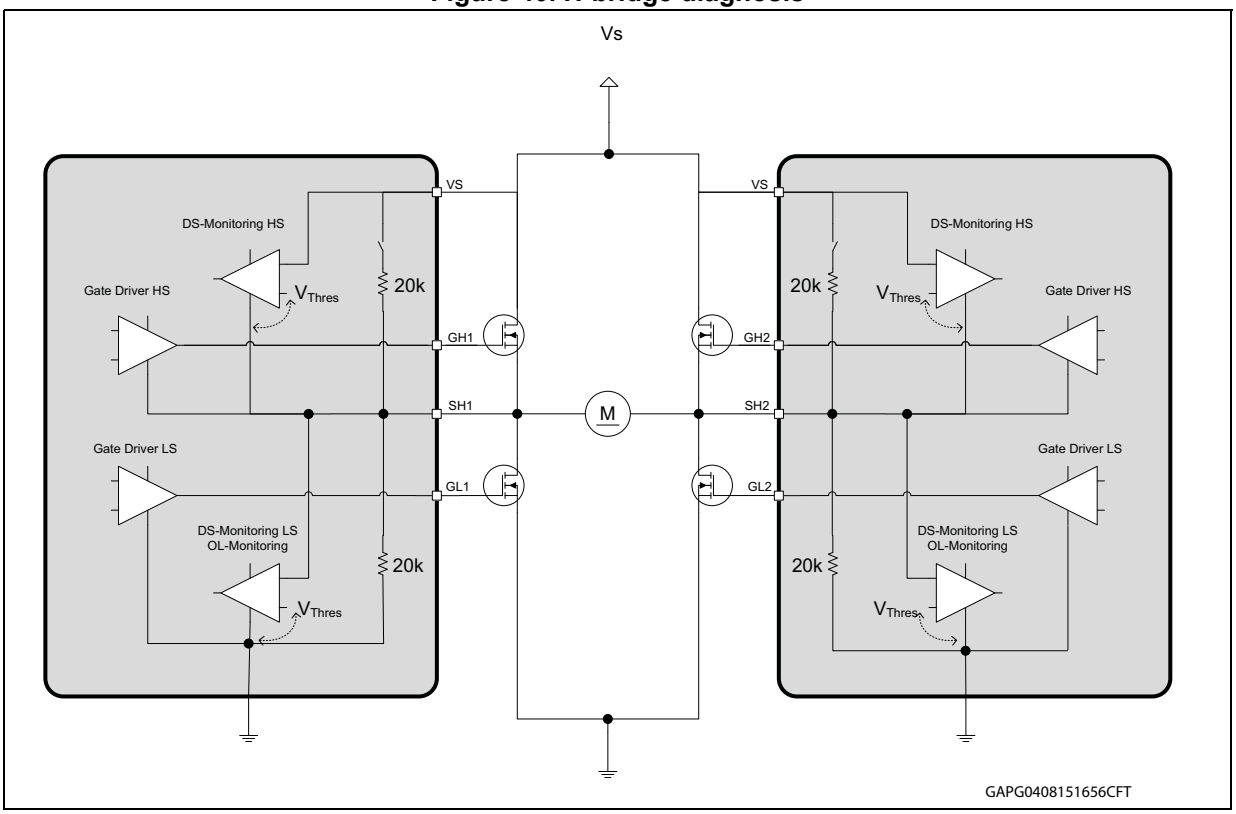
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switched into sink condition for 32 µs to 64 µs to ensure a fast switch-off of the H-bridge transistor. If slew rate control is enabled, the sink condition is slew-rate controlled. Afterwards the driver is switched into the resistive output mode (resistive path to source).

4.27 Short circuit detection / drain source monitoring

The Drain - Source voltage of each activated external MOSFET of the H-bridge is monitored by comparators to detect shorts to ground or battery. If the voltage-drop over the external MOSFET exceeds the configurable threshold voltage V_{SCd_HB} (DIAG_x (CR 10) for longer $t > t_{SCd_HB}$ the corresponding gate driver switches off the external MOSFET and the corresponding drain source monitoring flag DS_MON_x (SR 2) is set. The DSMON_x bits have to be cleared through the SPI to reactivate the gate drivers. This monitoring is only active while the corresponding gate driver is activated. If a drain-source monitor event is detected, the corresponding gate-driver remains activated for at maximum the filter time. When the gate driver switches on, the drain-source comparator requires the specified settling time until the drain-source monitoring is valid. During this time, this drain-source monitor event may start the filter time. The threshold voltage V_{SCd_HB} can be programmed using the SPI bits DIAG_x (CR 10).

Figure 40. H-bridge diagnosis



4.28 H-bridge monitoring in off-mode

The drain source voltages of the H-bridge driver external transistors can be monitored, while the transistors are switched off. If either bit OL_H1L2 (CR 10) or OL_H2L1 (CR 10) is set to

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1, while bit HEN (CR 1) = 1, the H-drivers enter resistive low mode and the drain-source voltages can be monitored. Since the pull-up resistance is equal to the pull-down resistance on both sides of the bridge a voltage of 2/3 V_S on the pull-up highside and 1/3 V_S on the low-side is expected, if they drive a low-resistive inductive load (e.g. motor). If the drain source voltage on each of these Power-MOS is less than 1/6 V_S, the drain-source monitor bit of the associated driver is set.

The open-load filter time is t_{OL_HB}.

Figure 41. H-bridge open-load-detection (no open-load detected)

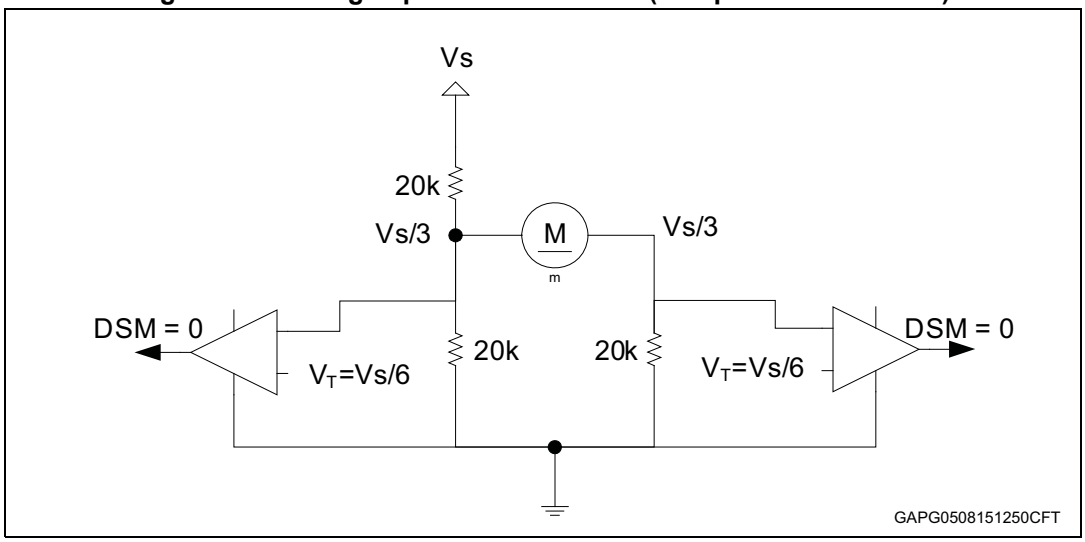
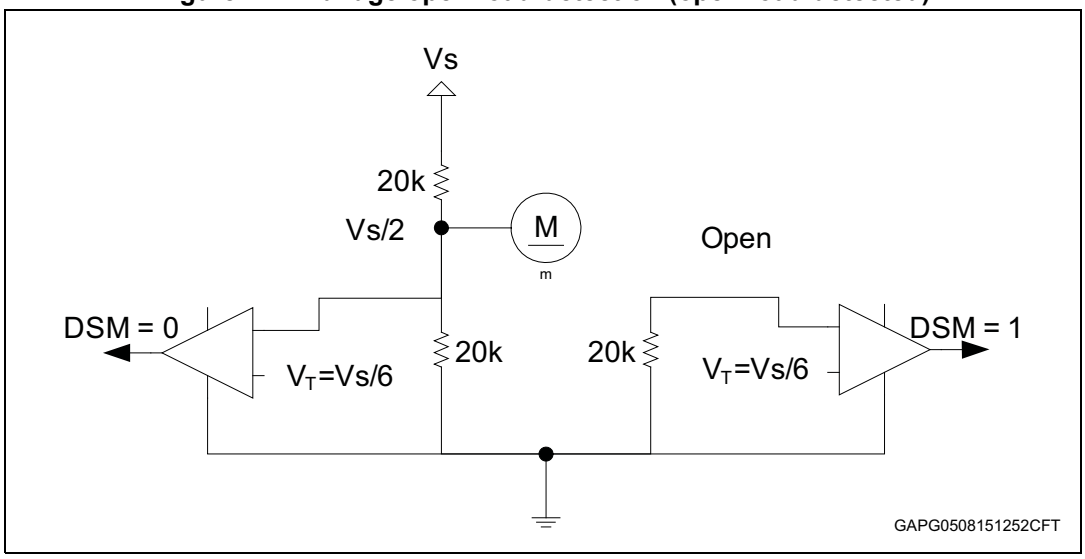


Figure 42. H-bridge open-load-detection (open-load detected)



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Figure 43. H-bridge open-load-detection (short to ground detected)

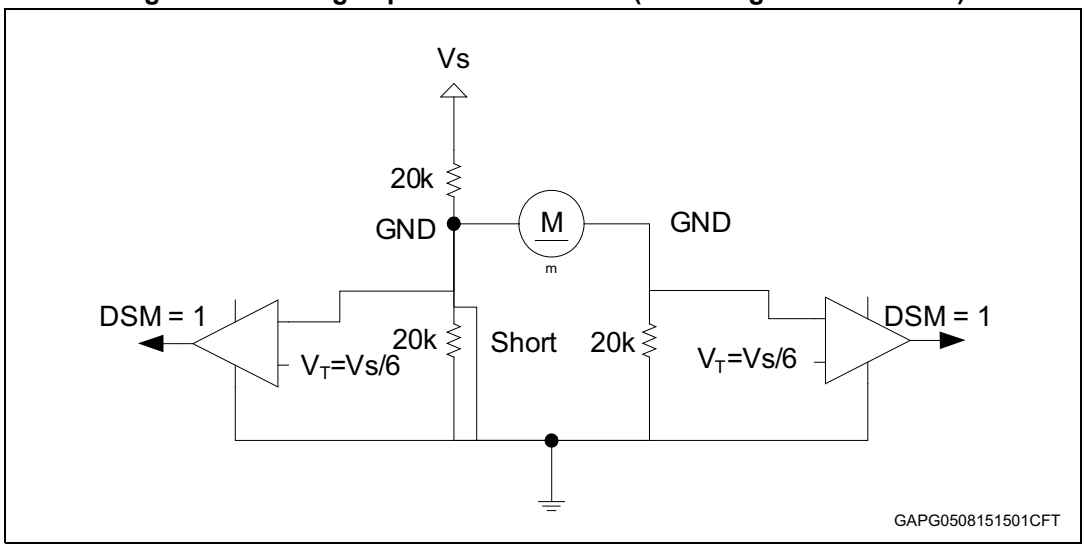


Figure 44. H-bridge open-load detection (short to V_S detected)

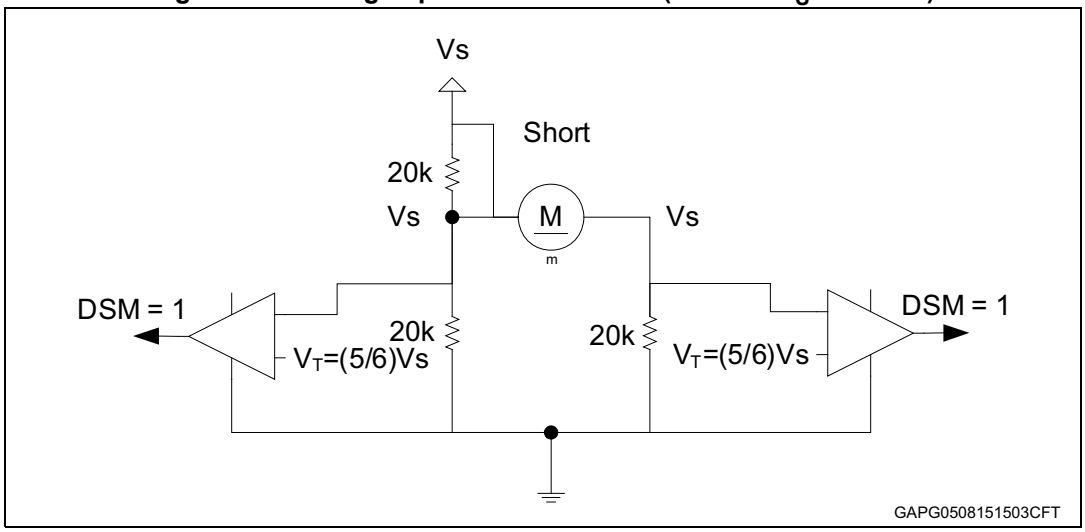


Table 68. H-bridge monitoring in off-mode

	Control bits			Failure bits		Comments
Nb	OL H1L2	OL H2L1	H OLTH High	DSMON LS1	DSMON LS2	
1	0	0	0	0	0	Drain-Source monitor disabled
2	1	0	x	0	0	No open-load detected
3	1	0	0	0	1	Open-load SH2
4	1	0	0	1	1	Short to GND
5	1	0	1	1	1	Short to VS
6	0	1	x	0	0	No open-load detected
7	0	1	0	1	0	Open-load SH1

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Table 68. H-bridge monitoring in off-mode (continued)

	Control bits			Failure bits		Comments
Nb	OL H1L2	OL H2L1	H OLTH High	DSMON LS1	DSMON LS2	
8	0	1	0	1	1	Short to GND
9	0	1	1	1	1	Short to VS

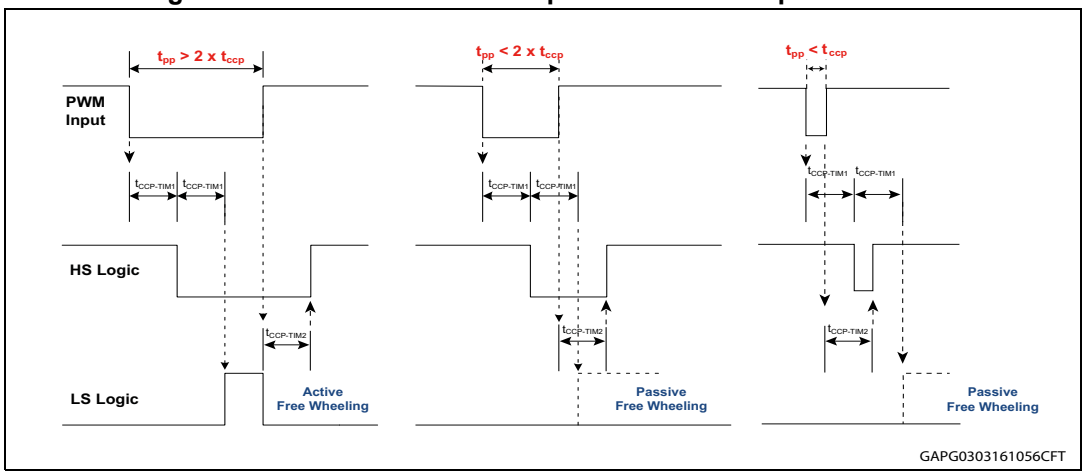
4.29 Programmable cross current protection

The external PowerMOSFETs transistors in H-bridge (two half-bridges) configuration are switched on with an additional delay time t_{CCP} to prevent cross current in the halfbridge. The cross current protection time t_{CCP} can be programmed with the SPI bits COPT_x<3:0> (CR 10). The timer is started when the gate driver is switched on in the device.

The PWMH module has 2 timers to configure locking time for high-side and freewheeling low-side. The programmable time $t_{CCP-TIM1}$ / $t_{CCP-TIM2}$ is the same. Sequence for switching in PWM mode is the following:

- HS switch off after locking $t_{CCP-TIM1}$
- LS switch on after 2nd locking $t_{CCP-TIM1}$
- HS switch on after locking $t_{CCP-TIM2}$ which starts with rising edge on PWM input

Figure 45. PWMH cross current protection time implementation



4.30 Power window H-bridge safety switch off block

The two LS Switches LS1_FSO and LS2_FSO are intended to be used to switch off the gates of the external high-side MOSFETs in the power window h-bridge if a fatal error happens. This block must work also in case the MOSFET driver and the according control blocks on the chip are destroyed. Therefore it is necessary to have a complete separated safety block on the device, which has it's own supply and GND connection, separated from the other supplies and GNDs. In the block is implemented an own voltage regulator and oscillator.

The safety block is surrounded by a GND isolation ring realized by deep trench isolation. The LS driver must work down to a lower voltage than the other circuits. The block has its

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own internal supply and an own oscillator for monitoring the failure signals (WWD, V1 fail, SPI fail & Tj) which are Manchester encoded and decoupled by high ohmic resistances. In case of fail-safe event, both LS switches LS1_FSO and LS2_FSO are switched on.

In case of entering V1_standby mode or Vbat_standby mode both fail safe low-side switches are switched on to minimize the current drawn by the fail safe block (e.g. oscillator is switched off and Manchester Encoding is deactivated). Short circuit protection to V_S is active in both standby modes limiting the current to I_{OLimit} for a filter of t_{SCF}.

After this filter time the fail-safe switches are switched off and LSxFSO_OC (SR 3) is set. To reactivate the low-side functionality this bit has to be set back by a read and clear command. In case of V_S loss the fail safe switches are biased by their own output voltage to turn on the low-side switches down to VOUT_max.

To allow verification of the Fail-Safe path, the low-side switches LS1_FSO and LS2_FSO can be turned on by SPI (Configuration Register 0x3F bit 4: FS_FORCED)

Figure 46. LSx_FSO: low-side driver "passively" turned on, taking supply from output pin (if main supply fails), can guarantee $V_{LSx_FSO} < V_{OUT_max}$

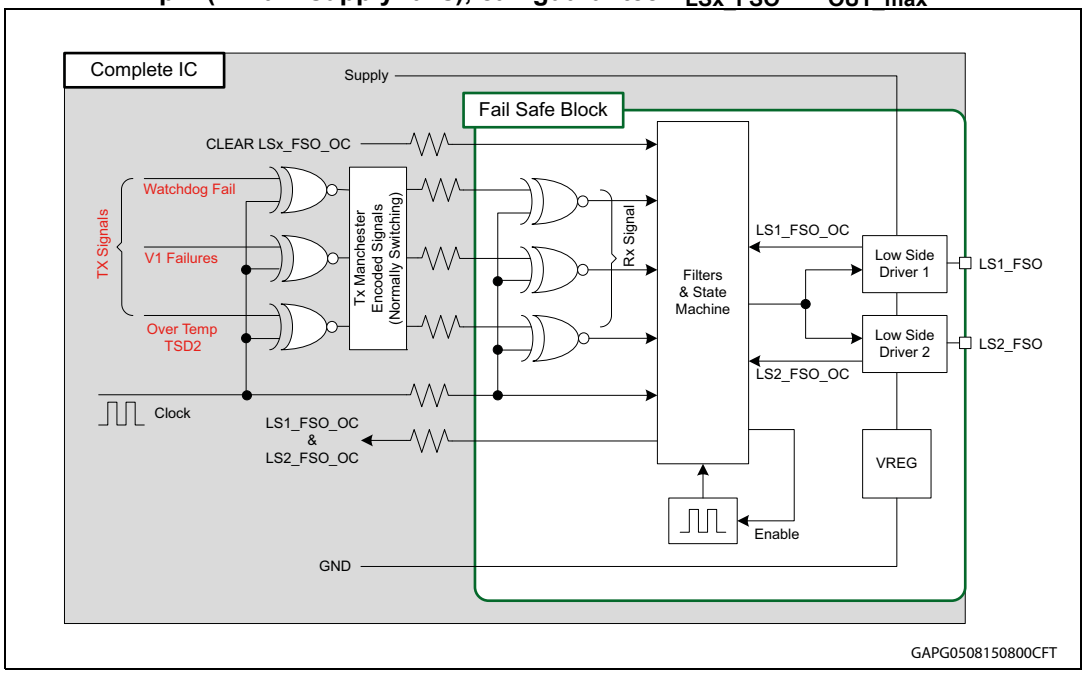
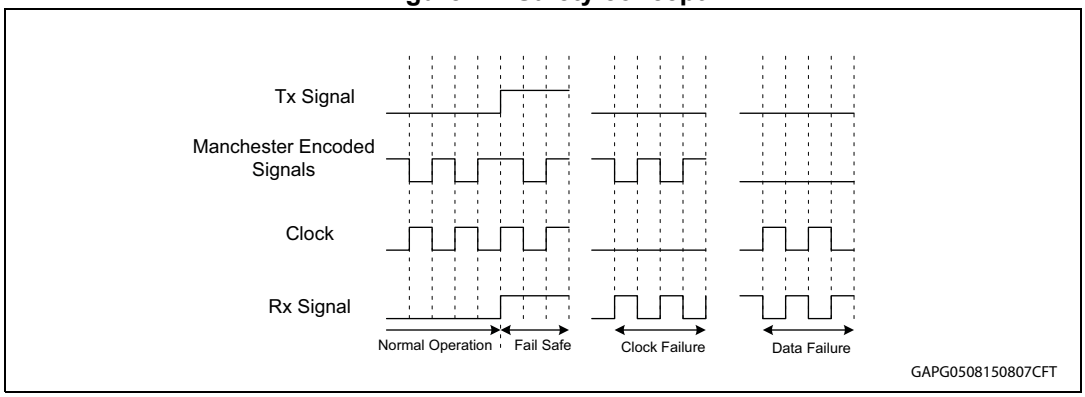


Figure 47. Safety concept



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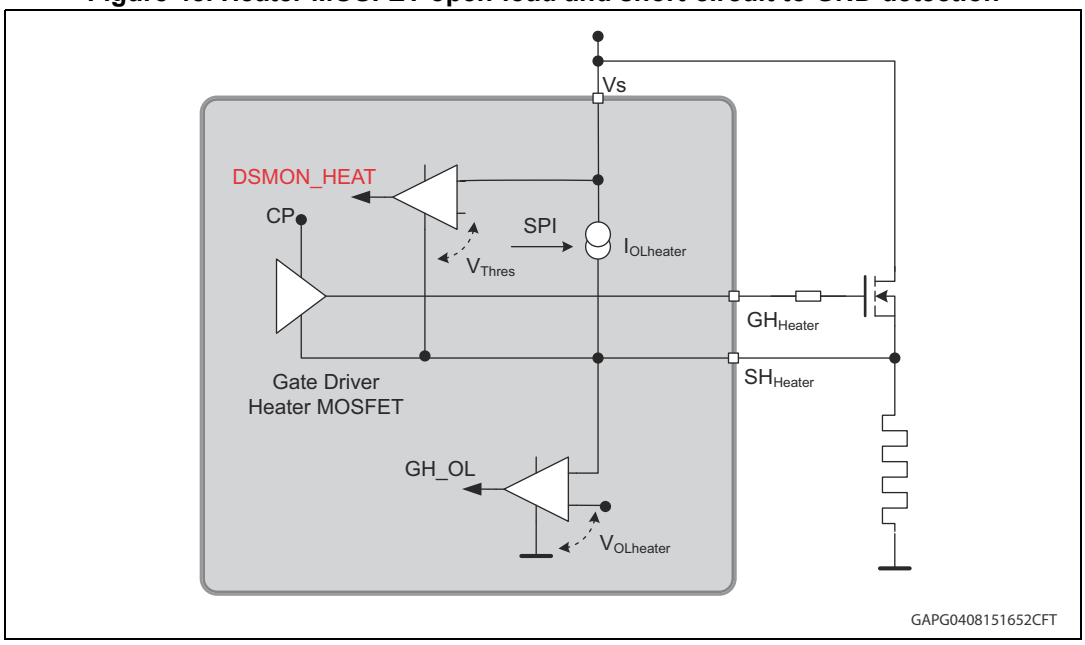
4.31 Heater MOSFET Driver

The Heater MOSFET Driver stage is controlled by control bit GH (CR 5). The driver contains two diagnosis features to indicate short-circuit in active mode (external MOSFET switched on) and open-load in off state (External MOSFET switched off).

Short circuit detection in on state is realized by monitoring the drain source voltage of the activated external MOSFET by a comparator to detect a short-circuit of SH_{heater} to ground. If the voltage-drop over the external MOSFET exceeds the programmed threshold voltage V_{SCd_HE} for longer than the drain-source monitor filter time t_{SCd_HE} the gate driver switches off the external MOSFET and the corresponding drain source monitoring flag DSMON_HEAT (SR 4) is set. The drain source-monitoring bit has to be cleared by SPI to reactivate the gate driver. The drain source monitoring is only active while the gate driver is activated. If a drain source monitoring event is detected, the gate-driver remains activated for the maximum filter time. The threshold voltage can be programmed by SPI bits GH_THx (CR 10).

Open-load detection in off state is realized by monitoring the voltage difference between SH_{heater} and GND and supplying SH_{heater} by a pull up current source that can be controlled by SPI bit GH_OL_EN (CR 10). When no load is connected to the external MOSFET source, the voltage will be pulled to V_S and in case of exceeding the threshold $V_{OLheater}$ for a time longer than the open-load filter time t_{OL_He} the open-load bit GH_OL (SR 5) will be set.

Figure 48. Heater MOSFET open-load and short-circuit to GND detection



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Table 69. Heater MOSFET control truth table

	Control bit	Failure bits					Output pin	Comment
Nb	GH ON/OFF	CP_LOW	VS_OV	VS_UV	DS	TSD1	GH_{heater}	
1	x	1	x	x	x	x	RL	Charge puump voltage too low
2	x	0	x	x	x	1	RL	Thermal shutdown
3	x	0	1	x	x	0	L	Overload
4	1	0	0	x	1	0	L	Short-circuit condition
5	x	0	0	1	0	0	L	Undervoltage
6	1	0	0	0	0	0	H	Heater MOFET driver enabled
7	0	0	0	0	0	0	L	Heater MOFET driver enabled

Note: RL = resistive low, L = active low, H = active high.

4.32 Controller of electro-chromic glass

The voltage of an electro-chromic element connected at pin ECV can be controlled to a target value, which is set by the bits EC_x <5:0> (CR 11). Setting bit ECON (CR 11) enables this function. An on-chip differential amplifier and an external MOS source follower, with its gate connected to pin ECDR, and which drives the electro-chrome mirror voltage at pin ECV, form the control loop. The drain of the external MOS transistor is supplied by OUT10. A diode from pin ECV (anode) to pin ECDR (cathode) has been placed on the chip to protect the external MOS source follower. A capacitor of at least 5 nF has to be added to pin ECDR for loop-stability.

The target voltage is binary coded with a full-scale range of 1.5 V. If bit ECV_HV (Config Reg) is set to 0, the maximum controller output voltage is clamped to 1.2 V without changing the resolution of bits EC_x<5:0> (CR 11). When programming the ECV low-side driver ECV_LS (CR 11) to on-state, the voltage at pin ECV is pulled to ground by a 1.6 Ω low-side switch until the voltage at pin ECV is less than d_{VECVhi} higher than the target voltage (fast discharge). The status of the voltage control loop is reported via SPI. Bit ECV_VHI (SR 6) is set, if the voltage at pin ECV is higher, whereas Bit ECV_VNR (SR 6) is set, if the voltage at pin ECV is lower than the target value. Both status bits are valid, if they are stable for at least the filter time t_{FEC_VNR} and t_{FEC_VHI}. Since OUT10 is the output of a high-side driver, it contains the same diagnose functions as the other high-side drivers (e.g. during an overcurrent detection, the control loop is switched off). In electro-chrome mode, OUT10 cannot be controlled by PWM mode. For EMS reasons, the loop capacitor at pin ECDR as well as the capacitor between ECV and GND has to be placed to the respective pins as close as possible (see*Figure 49: Electro-chrome control block* for details).

Pin ECDR is pulled resistively ($R_{ECDRDIS}$) to ground while not in electro-chrome mode.

EC glass control behavior in case of failure on OUT10:

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ECON (CR11) = 1 (EC glass control enabled)

- OUT10 is turned ON
- OUT10 settings in CR5 are ignored (PWM, DIRx, TIMERx)
- OUT10 settings in CR5 are recovered when ECON is set to 0.

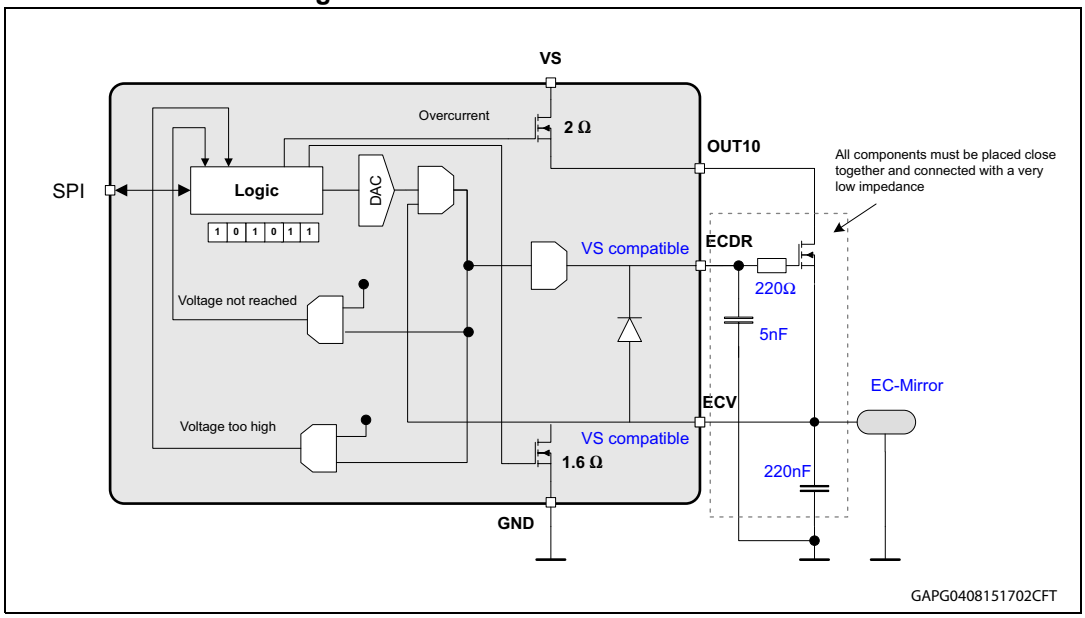
In case of a failure on OUT10 while ECON = 1 (overcurrent, V_S overvoltage /undervoltage, TSD1)

- OUT10 is turned OFF (regardless of VS_OV_SD_EN and VS_UV_SD_EN in CR3)
- DAC is reset: EC_x (CR11) set to '000000'
- ECDR pin is pulled to GND
- ECON (CR11) remains '1'
- ECV_LS (CR11) remains as programmed

Re-start of EC control after OUT10 failure

- Read&Clear or automatic restart (if CR3 Vs_LOCK_EN = 0)
- Write EC_x (CR11)

Figure 49. Electro-chrome control block



4.33 Temperature warning and shutdown

If any of the cluster (see *Section 4.34: Thermal clusters*) junction temperatures rises above the temperature warning threshold TW, the temperature warning flag TW (SR 2) is set after the temperature warning filter time t_{jtft} and can be read via SPI. If the junction temperature increases above the temperature shutdown threshold (TSD1), the thermal shutdown bit TSD1 (SR 1) is set and the power transistors of all output stages are switched off to protect the device after the thermal shutdown filter time. The gates of the H-bridge and the heater MOSFET are discharged by the 'Resistive Low' mode. After these bits have been cleared, the output stages are reactivated. If the temperature is still above the thermal warning threshold, the thermal warning bit is set after t_{jtft}. Once this bit is set and the temperature is above the temperature shutdown threshold, temperature shutdown is detected after t_{jtft} and

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the outputs are switched off. Therefore the minimum time after which the outputs are switched off after the bits have been cleared in case the temperature is still above the thermal shutdown threshold is twice the thermal warning/ thermal shutdown filter time t_{jtft}.

4.34 Thermal clusters

In order to provide an advanced on-chip temperature control, the power outputs are grouped in six clusters with dedicated thermal sensors. The sensors are suitably located on the device (see *Figure 50: Thermal clusters identification*). In case the temperature of an output cluster reaches the thermal shutdown threshold, the outputs assigned to this cluster are shut down (all other outputs remain active). Each output cluster has a dedicated temperature warning and shutdown flag (SR 6) and the cluster temperature can be read out by SPI.

Hence, the thermal cluster concept allows to identify a group of outputs in which one or more channels are in overload condition.

If thermal shutdown has occurred within an output cluster, or if temperature is rising within a cluster, it may be desired to identify which of the output (s) is (are) determining the temperature increase. An additional evaluation, based on current monitoring and cluster temperature read-out, supports identification of the outputs mainly contributing to the temperature increase. The cluster temperatures are available in SR 7, SR 8 and SR 9 and can be calculated from the binary coded register value using the following formula:

Decimal code = (350 – Temp) / 0.488

Example:

T = -40 °C => decimal code is 799 (0x31F)

T = 25 °C => decimal code is 666 (0x29A)

Thermal clusters can be configured using bit TSD_CONFIG (Config Reg):

- Standard mode (default): as soon as any cluster reaches thermal threshold the device is switched off. V1 regulator remains on and is switched off reaching TSD2.
- Cluster mode: only the cluster which reached shutdown temperature is switched off.

If Cluster Th_CL6 (global) or Cluster Th_CL5 (Voltage Regulators) reachTSD1, the whole device is OFF (beside V1).

Note: Clusters related to power outputs (clusters 1 to 4, see Figure 50: Thermal clusters identification) will be managed digitally only, by mean of the ADC conversion of related thermal sensors, while clusters 5 and 6 will be managed in an analog way (comparators) since ADC can be off, e.g. in V1_standby mode. Temperature reading provided by ADC may differ from real junction temperature of a specific output due to spatial placement of thermal sensor. Such an effect is more visible during fast thermal increases of junction temperature. For some of the Power outputs, located between two different sensors, it may happen that temperature raising also affects the adjacent Cluster.

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Figure 50. Thermal clusters identification

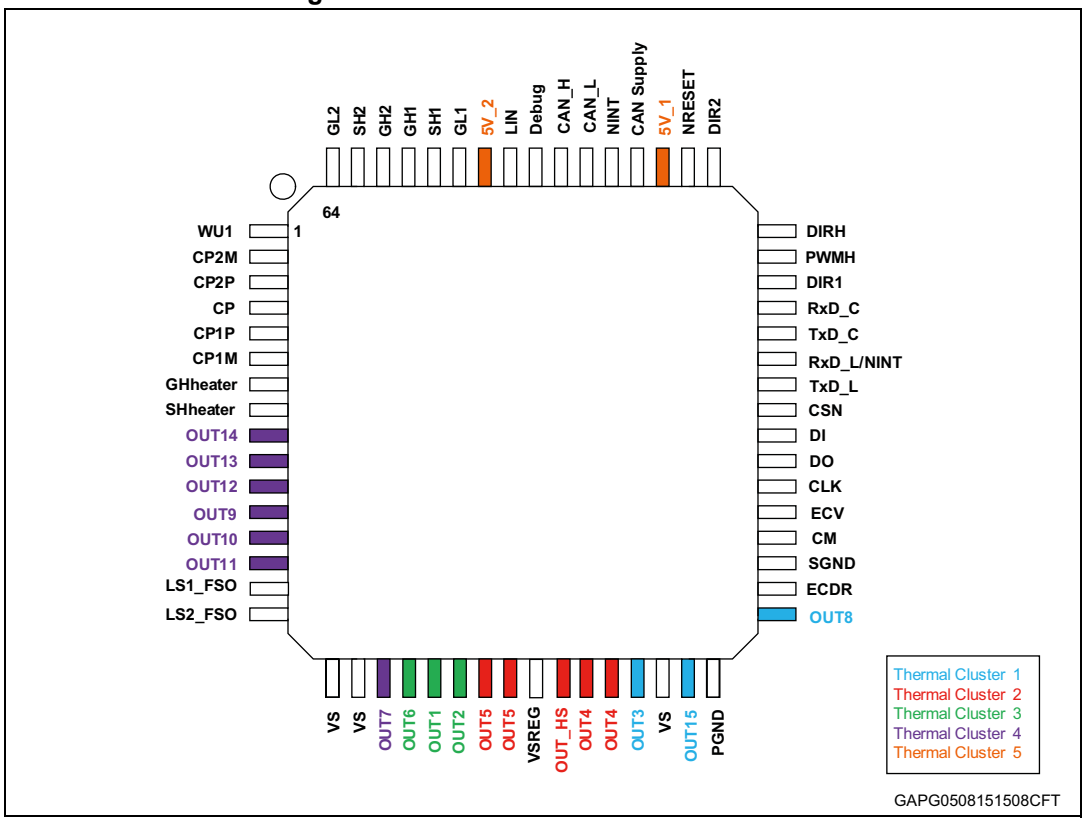


Table 70. Thermal cluster definition

Th_CL1	Th_CL2	Th_CL3	Th_CL4	Th_CL5	Th_CL6
5 W Driver + Mirror-y+OUT15	Door lock+OUT_HS	Folder+Mirror-x	10W driver high ohmic channels	VREG 1 VREG 2	Global
TW & TSD1 Both digitally managed	TW & TSD1 Both digitally managed	TW & TSD1 Both digitally managed	TW & TSD1 Both digitally managed	TW digitally managed TSD1 & TSD2 Both analog managed	TW digitally managed TSD1 Analog managed

4.35 V_S compensation (duty cycle adjustment) module

All stand-alone HS outputs can be programmed to calculate some internal duty cycle adjustment to adapt the duty cycle to a changing supply voltage at V_S. This feature is aimed to avoid LED brightness flickering in case of alternating supply voltage. The correction of the duty cycle is based on the following formula:

Equation 1: Duty cycle correction

$$DutyCycle = \frac{V_{th} - V_{LED}}{V_{Bat} - V_{LED}} \times DC_{nom}$$

V_{th} = Duty cycle reference voltage: defined as 10 V

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V_{Bat} = Reference voltage: defined as voltage at pin VS

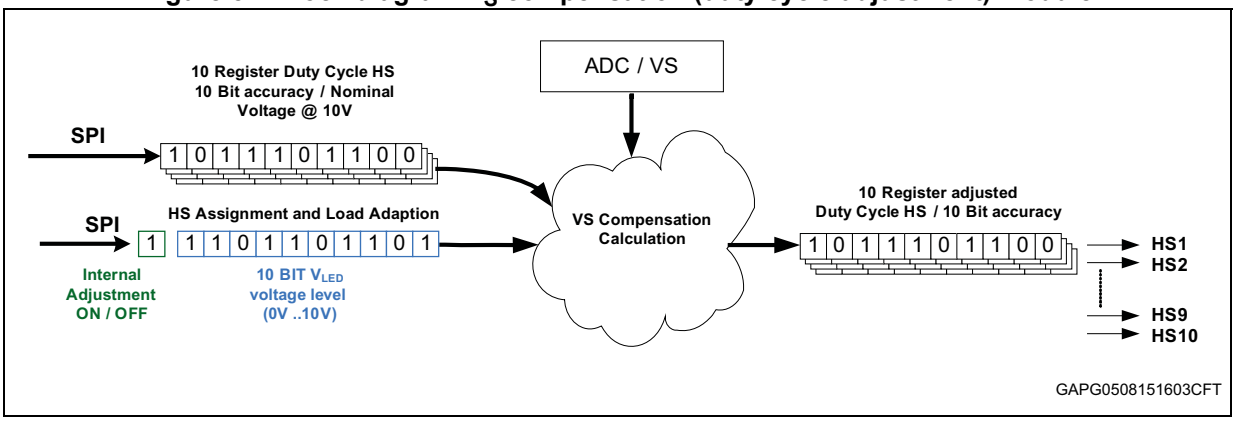
V_{LED} = Voltage drop on the external LED

DC_{nom} = Nominal Duty Cycle programmed by SPI< PWMx DCx>

To be compatible to different LED load characteristics the value for V_{LED} can be programmed for each output by a dedicated control register OUT7_VLED … OUT_HS_VLED (CR 18 to CR 22). Auto compensation features can be activated for all HS outputs each by setting OUTx_AUTOCOMP_EN (CR 18 to CR 22).

The programmed LED voltage (OUTx_V_LED (CR18 to CR22)) must be lower than V_{th} (10 V).

Figure 51. Block diagram V_S compensation (duty cycle adjustment) module



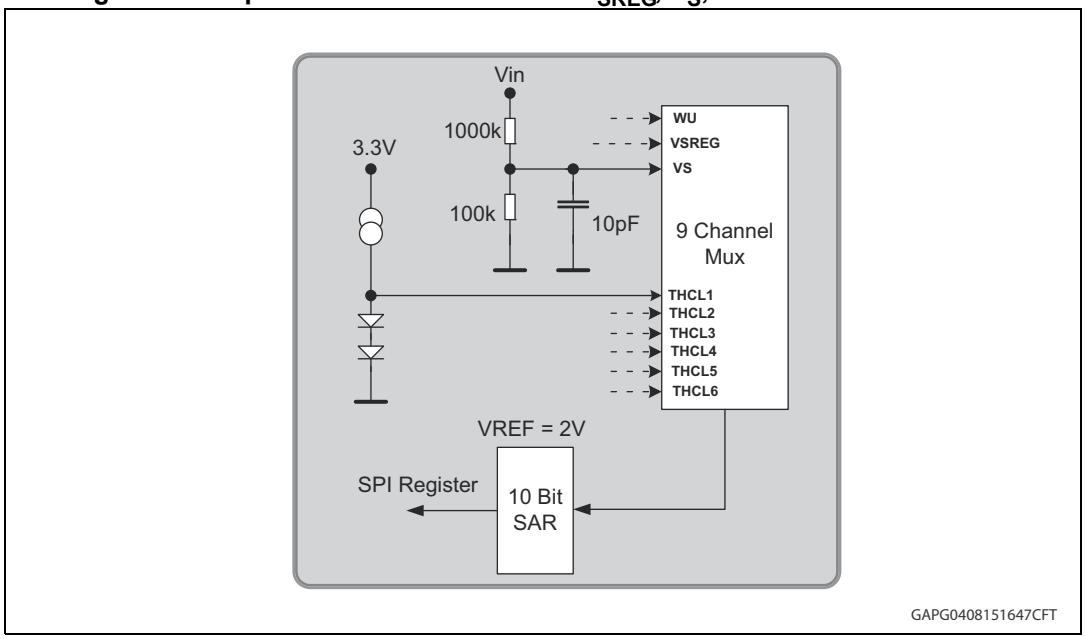
4.36 Analog digital converter

Voltage signals V_S, V_{SREG}, V_{WU} and TH_CL1..6 are read out sequentially. The voltage signals are multiplexed to an ADC. The ADC is realized as a 10 Bit SAR, that is sampled with the main clock f_{clk2} / f_{ADC}.

Each channel will be converted with a conversion time tcon, therefore an update of the ADC value is available every t_{con} * 9. In case of WU is directly connected to Clamp 30, the input must be protected by a series resistance of typical 1kΩ to sustain reverse battery condition.

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Figure 52. Sequential ADC Read Out for V_{SREG}, V_S, WU and THCL1 ..THCL6



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5 Serial Peripheral Interface (SPI)

A 32-bit SPI is used for bi-directional communication with the microcontroller.

The SPI is driven by a microcontroller with its SPI peripheral running in the following mode: CPOL = 0 and CPHA = 0.

For this mode input data is sampled by the low to high transition of the clock CLK, and output data is changed from the high to low transition of CLK. This device is not limited to microcontroller with a built-in SPI. Only three CMOS-compatible output Pins and one input Pin will be needed to communicate with the device. A fault condition can be detected by setting CSN to low. If CSN = 0, the DO-Pin will reflect the global error flag (fault condition) of the device.

- Chip Select Not (CSN)

  The input Pin is used to select the serial interface of this device. When CSN is high, the output Pin (DO) is in high impedance state. A low signal activates the output driver and a serial communication can be started. The state during CSN = 0 is called a communication frame. If CSN = low for t > $t_{CSNfail}$ the DO output will be switched to high impedance in order to not block the signal line for other SPI nodes.

- Serial Data In (DI)

  The input Pin is used to transfer data serial into the device. The data applied to the DI will be sampled at the rising edge of the CLK signal and shifted into an internal 32-bit shift register. At the rising edge of the CSN signal the content of the shift register will be transferred to Data Input Register. The writing to the selected Data Input Register is only enabled if exactly 32-bit are transmitted within one communication frame (i.e. CSN low). If more or less clock pulses are counted within one frame the complete frame will be ignored. This safety function is implemented to avoid an activation of the output stages by a wrong communication frame.

Note: Due to this safety functionality a daisy chaining of SPI is not possible. Instead, a parallel operation of the SPI bus by controlling the CSN signal of the connected IC's is recommended.

- Serial Data Out (DO)

  The data output driver is activated by a logical low level at the CSN input and will go from high impedance to a low or high level depending on the global error flag (fault condition). The first rising edge of the CLK input after a high to low transition of the CSN Pin will transfer the content of the selected status register into the data out shift register. Each subsequent falling edge of the CLK will shift the next bit out.

- Serial Clock (CLK)

  The CLK input is used to synchronize the input and output serial bit streams. The data input (DI) is sampled at the rising edge of the CLK and the data output (DO) will change with the falling edge of the CLK signal. The SPI can be driven with a CLK Frequency up to 4 MHz.

5.1 ST SPI 4.0

The ST-SPI is a standard used in ST Automotive ASSP devices.

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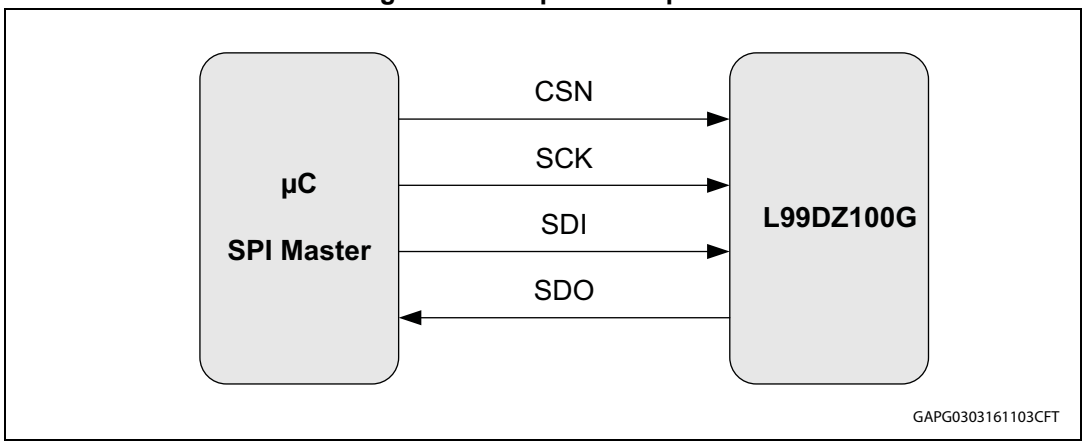
This chapter describes the SPI protocol standardization. It defines a common structure of the communication frames and defines specific addresses for product and status information.

The ST-SPI allows usage of generic software to operate the devices while maintaining the required flexibility to adapt it to the individual functionality of a particular product. In addition, failsafe mechanisms are implemented to protect the communication from external influences and wrong or unwanted usage.

The devices Serial Peripheral Interface are compliant to the ST SPI Standard Rev. 4.0.

5.1.1 Physical layer

Figure 53. SPI pin description



5.2 Signal description

- Chip Select Not (CSN)

  The communication interface is de-selected, when this input signal is logically high. A falling edge on CSN enables and starts the communication while a rising edge finishes the communication and the sent command is executed when a valid frame was sent. During communication start and stop the Serial Clock (SCK) has to be logically low. The Serial Data Out (SDO) is in high impedance when CSN is high or a communication timeout was detected.
- Serial Clock (SCK)

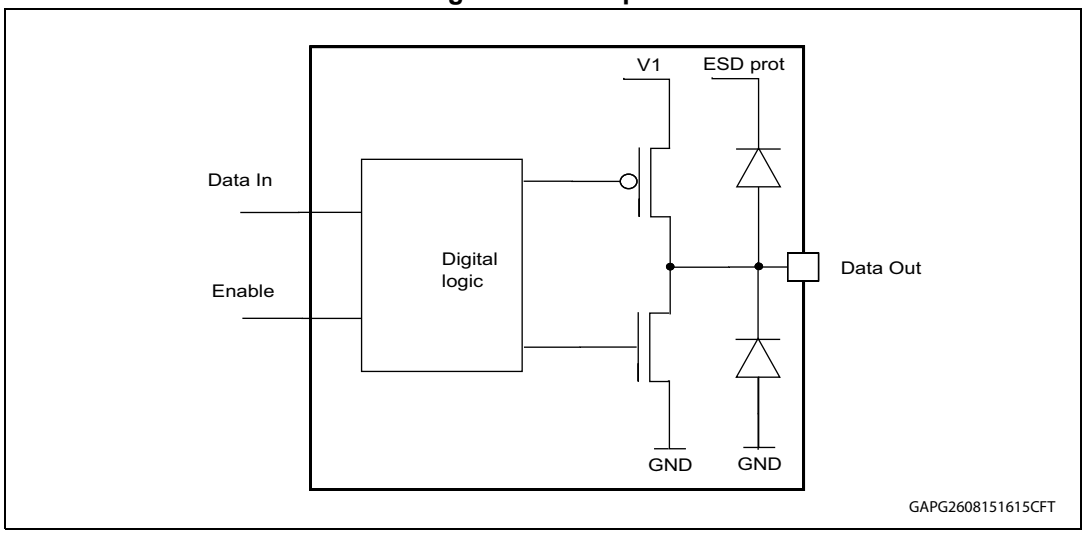
  This SCK provides the clock of the SPI. Data present at Serial Data Input (SDI) is latched on the rising edge of Serial Clock (SCK) into the internal shift registers while on the falling edge data from the internal shift registers are shifted out to Serial Data Out (SDO).
- Serial Data Input (SDI)

  This input is used to transfer data serially into the device. Data is latched on the rising edge of Serial Clock (SCK).
- Serial Data Output (SDO)

  This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of Serial Clock (SCK).

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Figure 54. SDO pin



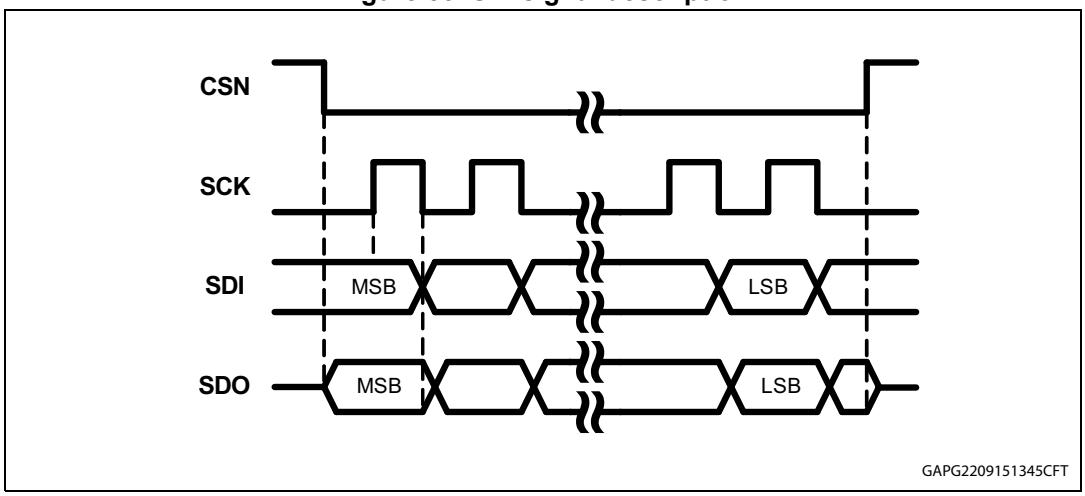
5.2.1 Clock and Data Characteristics

The ST-SPI can be driven by a microcontroller with its SPI peripheral running in following mode:

CPOL = 0

CPHA = 0

Figure 55. SPI signal description



The communication frame starts with the falling edge of the CSN (Communication Start). SCK has to be low.

The SDI data is then latched at all following rising SCK edges into the internal shift registers. After Communication Start the SDO will leave 3-state mode and present the MSB of the data shifted out to SDO. At all following falling SCK edges data is shifted out through the internal shift registers to SDO.

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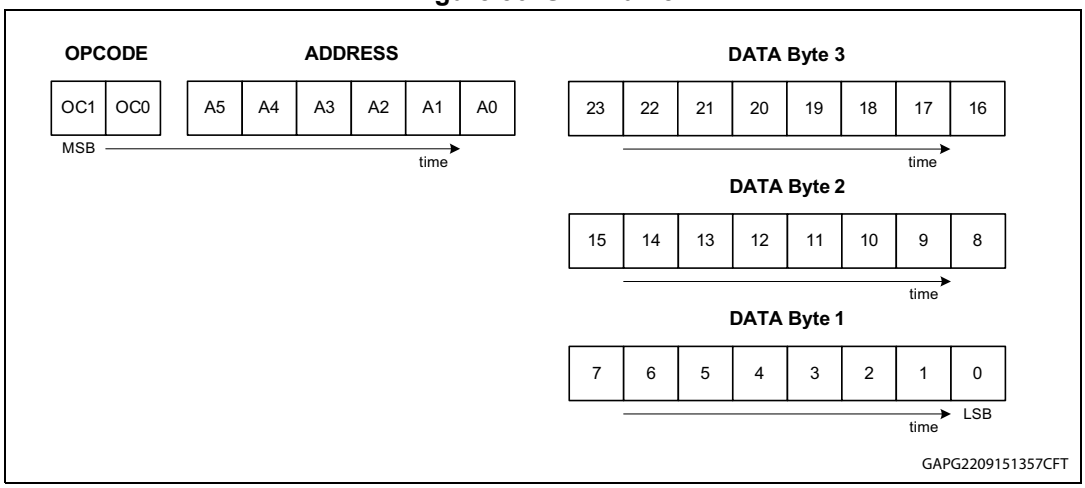
The communication frame is finished with the rising edge of CSN. If a valid communication took place (e.g. correct number of SCK cycles, access to a valid address), the requested operation according to the Operating Code will be performed (Write or Clear operation).

5.2.2 Communication protocol

SDI Frame

The devices Data-In Frame consist of 32-bit (OpCode (2 bits) + Address (6 bits) + Data Byte 3 + Data Byte 2 + Data Byte 1). The first two transmitted bits (MSB, MSB-1) contain the Operation Code which represents the instruction which will be performed. The following 6 bits (MSB-2 to MSB-7) represent the address on which the operation will be performed. The subsequent bytes contain the payload.

Figure 56. SDI Frame



Operating code

The operating code is used to distinguish between different access modes to the registers of the slave device.

Table 71. Operation codes

OC1	OC0	Description
0	0	Write Operation
0	1	Read Operation
1	0	Read & Clear Operation
1	1	Read Device Information

A Write Operation will lead to a modification of the addressed data by the payload if a write access is allowed (e.g. Control Register, valid data). Beside this a shift out of the content (data present at Communication Start) of the registers is performed.

A Read Operation shifts out the data present in the addressed register at Communication Start. The payload data will be ignored and internal data will not be modified. In addition a Burst Read can be performed.

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A Read & Clear Operation will lead to a clear of addressed status bits. The bits to be cleared are defined first by address, second by payload bits set to ‘1’. Beside this a shift out of the content (data present at Communication Start) of the registers is performed.

Note: Status registers which change status during communication could be cleared by the actual Read & Clear Operation and are neither reported in actual communication nor in the following communications. To avoid a loss of any reported status it is recommended just clear status registers which are already reported in the previous communication (Selective Bitwise Clear).

Advanced operation codes

To provide beside the separate write of all control registers and the bitwise clear of all status registers, two Advanced Operation Codes can be used to set all control registers to the default value and to clear all status registers. A ‘set all control registers to default’ command is performed when an OpCode ‘11’ at address b’111111 is performed.

Note: Please consider that potential device specific write protected registers cannot be cleared with this command as therefore a device Power-on-Reset is needed.

A ‘clear all status registers’ command is performed when an OpCode ‘10’ at address b’111111 is performed.

Data-in payload

The Payload (Data Byte 1 to Data Byte 3) is the data transferred to the devices with every SPI communication. The Payload always follows the OpCode and the Address bits. For Write access the Payload represents the new data written to the addressed register. For Read & Clear operations the Payload defines which bits of the adressed Status Register will be cleared. In case of a ‘1’ at the corresponding bit position the bit will be cleared.

For a Read Operation the Payload is not used. For functional safety reasons it is recommended to set unused Payload to ‘0’.

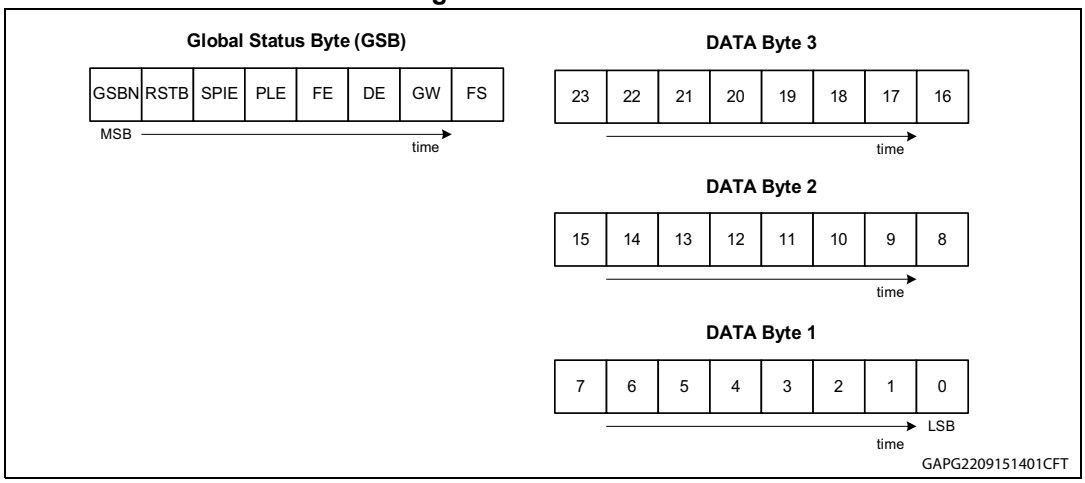
SDO frame

The data-out frame consists of 32-bit (GSB + Data Byte 1 to 3).

The first eight transmitted bits contain device related status information and are latched into the shift register at the time of the Communication Start. These 8-bit are transmitted at every SPI transaction. The subsequent bytes contain the payload data and are latched into the shift register with the eighth positive SCK edge. This could lead to an inconsistency of data between the GSB and Payload due to different shift register load times. Anyhow, no unwanted Status Register clear should appear, as status information should just be cleared with a dedicated bit clear after.

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Figure 57. SDO frame



Global Status Byte (GSB)

The bits (Bit0 to Bit4) represent a logical OR combination of bits located in the Status Registers. Therefore no direct Read & Clear can be performed on these bits inside the GSB.

Table 72. Global Status Byte

Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
GSBN	RSTB	SPIE	PLE	FE	DE	GW	FS

Global Status Bit Not (GSBN)

The GSBN is a logically NOR combination of Bit 24 to Bit 30. This bit can also be used as Global Status Flag without starting a complete communication frame as it is present directly after pulling CSN low.

Reset Bit (RSTB)

The RSTB indicates a device reset. In case this bit is set, specific internal Control Registers are set to default and kept in that state until the bit is cleared. The RSTB bit is cleared after a Read & Clear of all the specific bits in the Status Registers which caused the reset event.

SPI Error (SPIE)

The SPIE is a logical OR combination of errors related to a wrong SPI communication.

Physical Layer Error (PLE)

The PLE is a logical OR combination of errors related to the LIN and HS CAN transceivers.

Functional Error (FE)

The FE is a logical OR combination of errors coming from functional blocks (e.g. High-side overcurrent).

Device Error (DE)

The DE is a logical OR combination of errors related to device specific blocks (e.g. VS overvoltage, overtemperature

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Global Warning (GW)

The GW is a logical OR combination of warning flags (e.g. thermal warning).

Fail Safe (FS)

The FS bit indicates that the device was forced into a safe state due to mistreatment or fundamental internal errors (e.g. Watchdog failure, Voltage regulator failure).

Data-Out Payload

The Payload (Data Bytes 1 to 3) is the data transferred from the slave device with every SPI communication to the master device. The Payload always follows the OpCode and the address bits of the actual shifted in data (In-frame-Response).

5.2.3 Address definition

Table 73. Device application access

Operating Code	
OC1	**OC0**
0	0
0	1
1	0

Table 74. Device information read access

Operating Code	
OC1	**OC0**
1	1

Table 75. RAM address range

RAM Address	Description	Access
3FH	Configuration Register	R/W
3CH	Status Register 12	R/C
…	…	
32H	Status Register 2	R/C
31H	Status Register 1	R/C
…	…	
22H	Control Register 34	R/W
1DH	Control Register 29	R/W
…	…	
02H	Control Register 2	R/W

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Table 75. RAM address range (continued)

RAM Address	Description	Access
01H	Control Register 1	R/W
00H	reserved	

Table 76. ROM address range

ROM Address	Description	Access
3FH	<Advanced Op.>	W
3EH	<GSB Options>	R
…		
20H	<SPI CPHA test>	R
16H	<WD bit pos. 4>	R
15H	<WD bit pos. 3>	R
14H	<WD bit pos. 2>	R
13H	<WD bit pos. 1>	R
12H	<WD Type 2>	R
11H	<WD Type 1>	R
10H	<SPI mode>	R
…		
0AH	<Silicon Ver.>	R
…		
06H	<Device No.5>	R
05H	<Device No.4>	R
04H	<Device No.3>	R
03H	<Device No.2>	R
02H	<Device No.1>	R
01H	<Device Family>	R
00H	<Company Code>	R

Information registers

The *Device Information Registers* can be read by using OpCode ‘11’. After shifting out the GSB the 8-bit wide payload will be transmitted. By reading *Device Information Registers* a communication width which is minimum 16-bit plus a multiple by 8 can be used. After shifting out the GSB followed by the 8-bit wide payload a series of ‘0’ is shifted out at the SDO.

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Table 77. Information Registers Map

ROM Adress	Description	Access		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
3FH	<Advanced Op.>										
3EH	<GSB Options>	R	→	0	0	0	0	0	0	0	0
…											
20H	<SPI CPHA test>	R	→	0	1	0	1	0	1	0	1
16H	<WD bit pos. 4>	R	→	C0H							
15H	<WD bit pos. 3>	R	→	7FH							
14H	<WD bit pos. 2>	R	→	C0H							
13H	<WD bit pos. 1>	R	→	41H							
12H	<WD Type 2>	R	→	91H							
11H	<WD Type 1>	R	→	28H							
10H	<SPI mode>	R	→	B0H							
…			→								
0AH	<Silicon Ver.>	R	→	major revision				minor revision			
…			→								
06H	<Device No.5>	R		L99DZ100G: 01H L99DZ100GP: 00H							
05H	<Device No.4>	R	→	09H							
04H	<Device No.3>	R	→	46H							
03H	<Device No.2>	R	→	42H							
02H	<Device No.1>	R	→	55H							
01H	<Device Family>	R	→	01H							
00H	<Company Code>	R	→	00H							

Device Identification Registers

These registers represent a unique signature to identify the device and silicon version.

<Company Code>: 00H (STMicroelectronics)

<Device Family>: 01H (BCD Power Management)

<Device No. 1>: 55H

<Device No. 2>: 42H

<Device No. 3>: 46H

<Device No. 4>: 09H

<Device No. 5>: for L99DZ100G: 01H for L99DZ100GP: 00H

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SPI modes

By reading out the <SPI mode> register general information of SPI usage of the *Device Application Registers* can be read.

Table 78. SPI Mode Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BR	DL2	DL1	DL0	0	0	S1	S0
1	0	1	1	0	0	0	0

<SPI mode>: B0H (Burst mode read available, 32-bit, no data consistency check)

SPI Burst Read

Table 79. Burst Read Bit

Bit 7	Description
0	BR not available
1	BR available

The SPI Burst Read bit indicates if a burst read operation is implemented. The intention of a Burst Read is e.g. used to perform a device internal memory dump to the SPI Master.

The start of the Burst Read is like a normal Read Operation. The difference is, that after the SPI Data Length the CSN is not pulled high and the SCK will be continuously clocked. When the normal SCK max count is reached (SPI Data Length) the consecutive addressed data will be latched into the shift register. This procedure is performed every time when the SCK payload length is reached.

In case the automatic incremented address is not used by the device, undefined data is shifted out. An automatic address overflow is implemented when address 3FH is reached. The SPI Burst Read is limited by the CSN low timeout.

SPI Data Length

The SPI Data Length value indicates the length of the SCK count monitor which is running for all accesses to the Device Application Registers. In case a communication frame with an SCK count not equal to the reported one will lead to a SPI Error and the data will be rejected.

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Table 80. SPI Data Length

Bit 6	Bit 5	Bit 4	Description
DL2	DL1	DL0	
0	0	0	invalid
0	0	1	16-bit SPI
0	1	0	24-bit SPI
0	1	1	32-bit SPI
			…
1	1	1	64-bit SPI

Data Consistency Check (Parity/CRC)

N/A

Table 81. Data Consistency Check

Bit 1	Bit 0	Description
S1	S0	
0	0	not used
0	1	Parity used
1	0	CRC used
1	1	Invalid

Watchdog Definition

In case a watchdog is implemented the default settings can be read out via the *Device Information Registers*.

Table 82. WD Type/Timing

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	WD1	WD0						
<WD Type 1/2>	0	0	Register is not used					
<WD Type 1>	0	1	WT5	WT4	WT3	WT2	WT1	WT0
		1	1	0	1	0	0	0
			Watchdog Timeout / Long Open Window WT[5:0] * 5ms					
<WD Type 2>	1	0	OW2	OW1	OW0	CW2	CW1	CW0
	1	0	0	1	0	0	0	1
			Open Window OW[2:0] * 5ms			Closed Window CW[2:0] * 5ms		

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Table 82. WD Type/Timing (continued)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
<WD Type 1/2>	1	1	Invalid					

<*WD Type 1*>: 28H (Long Open Window: 200ms)

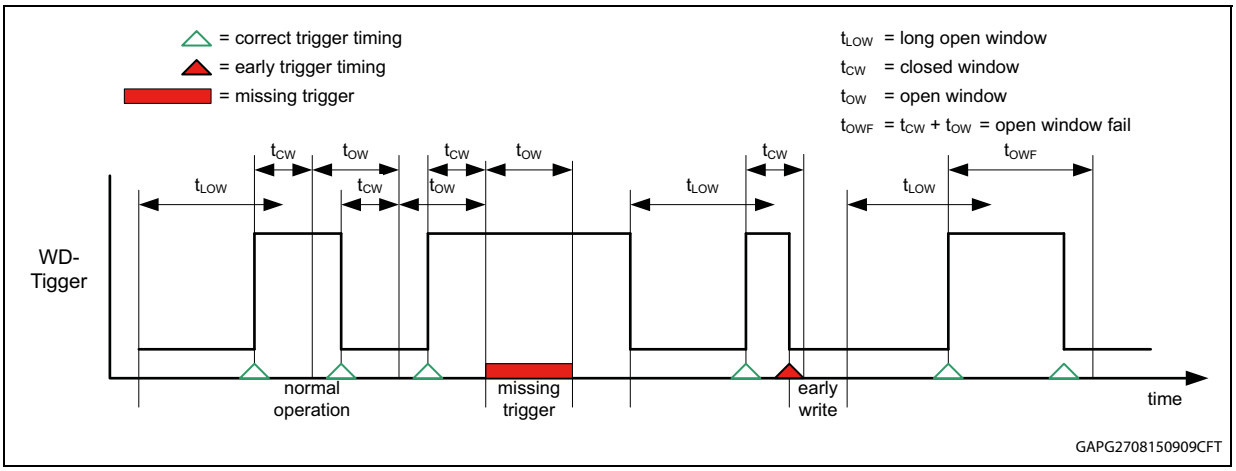
<*WD Type 2*>: 91H (Open Window. 10ms, Closed Window: 5ms)

<WD Type 1> indicates the Long Open Window (timeout) which is opened at the start of the watchdog. The binary value of WT[5:0] times 5ms indicates the typical value of the Timeout Time.

<WD Type 2> describes the default timing of the window watchdog.

The binary value of CW[2:0] times 5ms defines the typical Closed Window time and OW[2:0] times 5ms defines the typical Open Window time.

Figure 58. Window watchdog operation



The watchdog trigger bit location is defined by the <WD bit pos. X> registers.

Table 83. WD bit position

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	WB1	WB0						
<WD bit pos. X>	0	0	Register is not used					
<WD bit pos. X>	0	1	WBA5	WBA4	WBA3	WBA2	WBA1	WBA0
<WD bit pos. 1>	0	1	0	0	0	0	0	1
<WD bit pos. 3>	0	1	1	1	1	1	1	1
			Defines the register addresses of the WD trigger bits					
<WD bit pos. X>	1	0	WBA5	WBA4	WBA3	WBA2	WBA1	WBA0

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Table 83. WD bit position (continued)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
			Defines the stop address of the address range (previous <WD bit pos. X> is a WB = ‘01’). The consecutive <WD bit pos. X> has to be a WB = ‘11’					
<WD bit pos. X>	1	1	0	WBP 4	WBP3	WBP2	WBP1	WBP0
<WD bit pos. 2>	1	1	0	0	0	0	0	0
<WD bit pos. 4>	1	1	0	0	0	0	0	0
				Defines the binary bit position of the WD trigger bit within the register				

<*WD bit pos 1*>*:* 41H;watchdog trigger bit located at address 01H (*CR1*)

<*WD bit pos 2*>*:* C0H; watchdog trigger bit location is bit0

<*WD bit pos 3*>*:* 7FH;watchdog trigger bit located at address 3FH (Config Register)

<*WD bit pos 4*>*:* C0H; watchdog trigger bit location is bit0

Device Application Registers (RAM)

The *Device Application Registers* are all registers accessible using OpCode ‘00’, ‘01’ and ‘10’. The functions of these registers are defined in the device specification.

5.2.4 Protocol failure detection

To realize a protocol which covers certain failsafe requirements a basic set of failure detection mechanisms are implemented.

Clock monitor

During communication (CSN low to high phase) a clock monitor counts the valid SCK clock edges. If the SCK edges do not correlate with the SPI Data Length an SPIE is reported with the next command and the actual communication is rejected.

By accessing the Device Information Registers (OpCode = ‘11’) the Clock Monitor is set to a minimum of 16 SCK edges plus a multiple by 8 (e.g. 16, 25, 32, …). Providing no SCK edge during a CSN low to high phase is not recognized as an SPIE. For a SPI Burst Read also the SPI Data Length plus multiple numbers of Payloads SCK edges are assumed as a valid communication.

SCK Polarity (CPOL) check

To detect the wrong polarity access via SCK the internal Clock monitor is used. Providing first a negative edge on SCK during communication (CSN low to high phase) or a positive edge at last will lead to an SPI Error reported in the next communication and the actual data is rejected.

SCK Phase (CPHA) check

To verify, that the SCK Phase of the SPI master is set correctly a special Device Information Register is implemented. By reading this register the data must be 55H. In case AAH is read

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the CPHA setting of the SPI master is wrong and a proper communication cannot be guaranteed.

CSN timeout

By pulling CSN low the SDO is set active and leaves its 3-state condition. To ensure communication between other SPI devices within the same bus even in case of CSN stuck at low a CSN timeout is implemented. By pulling CSN low an internal timer is started. After timer end is reached the actual communication is rejected and the SDO is set to 3-state condition.

SDI stuck at GND

As a communication with data all-‘0’ and OpCode ‘00’ on address b’000000 cannot be distinguished between a valid command and a SDI stuck at GND this communication is not allowed. Nevertheless, in case a stuck at GND is detected the communication will be rejected and the SPIE will be set with the next communication.

SDI stuck at HIGH

As a communication with data all-‘1’ and OpCode ‘11’ on address b’111111 cannot be distinguished between a valid command and a SDI stuck at HIGH this communication is not allowed. In case a stuck at HIGH is detected the communication will be rejected and the SPIE will be set with the next communication.

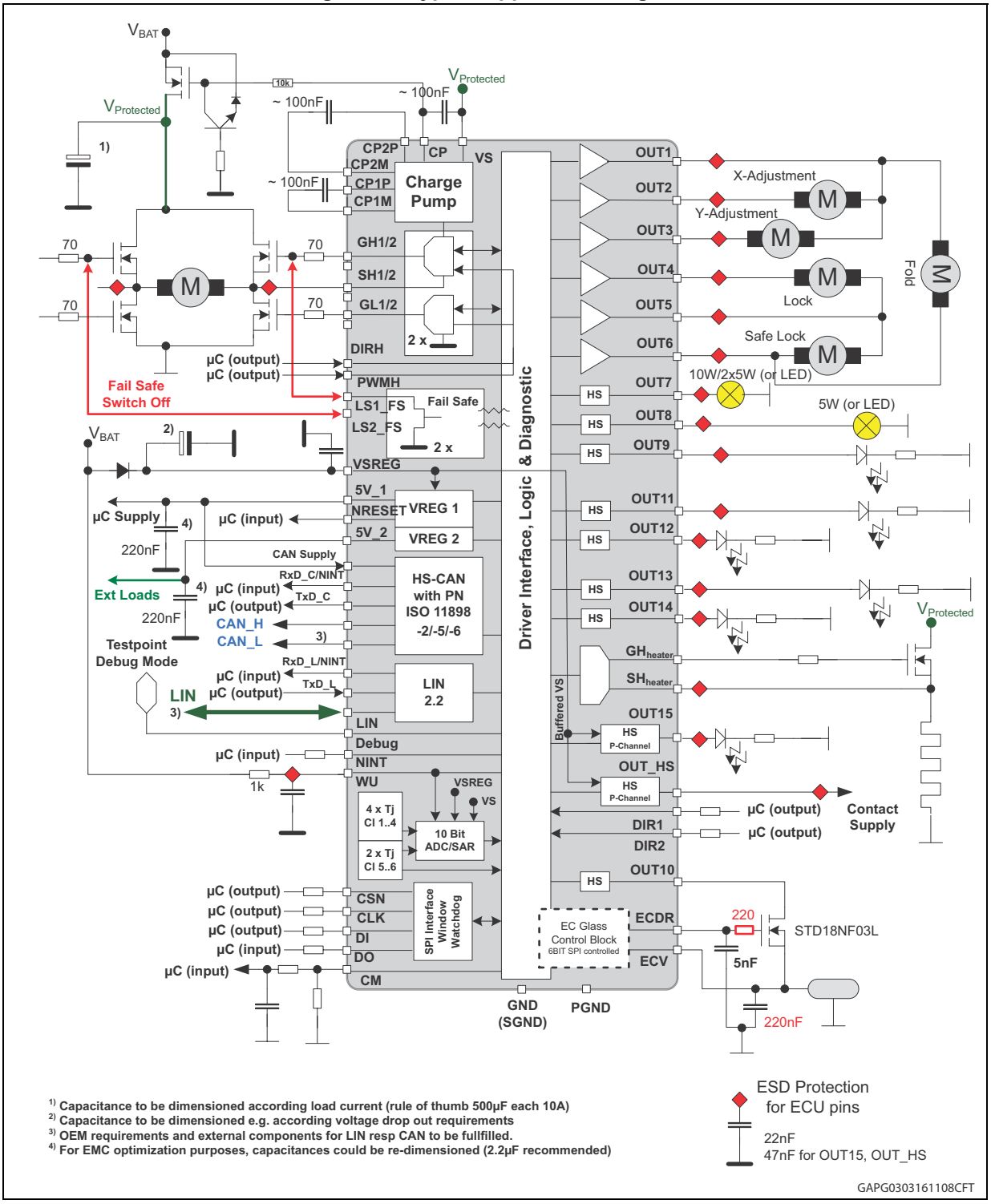
SDO stuck @

The SDO stuck at GND and stuck at HIGH has to be detected by the SPI master. As the definition of the GSB guarantees at least one toggle, a GSB with all-‘0’ or all –‘1’ reports a stuck at error.

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6 Application

Figure 59. Typical application diagram



1) Capacitance to be dimensioned according load current (rule of thumb 500µF each 10A)
2) Capacitance to be dimensioned e.g. according voltage drop out requirements
3) OEM requirements and external components for LIN resp CAN to be fullfilled.
4) For EMC optimization purposes, capacitances could be re-dimensioned (2.2µF recommended)

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7 SPI Registers

7.1 Global Status Byte GSB

Table 84. Global Status Byte (GSB)

	31	30	29	28	27	26	25	24
Bit name	GSBN	RSTB	SPIE	PLE	FE	DE	GW	FS
Reset	1	0	0	0	0	0	0	0
Access	R							

Table 85. GSB signals description

Bit	Name	Description
31	GSBN	Global Status Bit Inverted The GSBN is a logically NOR combination of GSB Bits 24 to Bit 30(1). This bit can also be used as Global Status Flag without starting a complete communication frame as it is present at SDO directly after pulling CSN low. 0: error detected (1 or several GSB bits from 24 to 30 are set) 1: no error detected (default after Power-on) Specific failures may be masked in the Configuration Register 0x3F. A masked failure will still be reported in the GSB by the related failure flag, however it is not reflected in the GSBN (bit 31).
30	RSTB	Reset The RSTB indicates a device reset and it is set in case of the following events: – VPOR (SR1 - 0x31) – WDFAIL (SR1 - 0x31) – V1UV (SR1 - 0x31) – FORCED_SLEEP_TSD2/V1SC (SR1 - 0x31) 0: no reset signal has been generated (default) 1: Reset signal has been generated RSTB is cleared by a *Read & Clear* command to all bits in *Status Register 1* causing the Reset event.
29	SPIE(2)	SPI Error Bit The SPIE indicates errors related to a wrong SPI communication. – SPI_INV_CMD (SR2 - 0x32) – SPI_SCK_CNT (SR2 - 0x32) The bit is also set in case of an SPI CSN Time-out detection 0: no error (default) 1: error detected SPIE is cleared by a valid SPI command.

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Table 85. GSB signals description (continued)

Bit	Name	Description
28	PLE(2)	Physical Layer Error The PLE is a logical OR combination of errors related to the LIN and CAN transceivers. – LIN_PERM_DOM (SR2 - 0x32) – LIN_TXD_DOM (SR2 - 0x32) – LIN_PERM_REC (SR2 - 0x32) – CAN_RXD_REC (SR2 - 0x32) – CAN_PERM_REC (SR2 - 0x32) – CAN_PERM_DOM (SR2 - 0x32) – CAN_TXD_DOM (SR2 - 0x32) – SYSERR (SR12 - 0x3C) – OSC_FAIL (SR12 - 0x3C) – FDERR (SR12 - 0x3C) 0: no error (default) 1: error detected PLE is cleared by a *Read & Clear* command to all related bits in *Status Registers 2 and 12*.
27	FE	Functional Error Bit The FE is a logical OR combination of errors coming from functional blocks. – V2SC (SR2 - 0x32) – DSMON_HSx (SR2 - 0x32) – DSMON_LSx (SR2 - 0x32) – OUTxHS_OC TH EX (SR3 - 0x33) – OUTxLS_OC TH EX (SR3 - 0x33) – OUTHS_OC TH EX (SR3 - 0x33) – OUTx_OC (SR3 - 0x33) – LSxFS_OC (SR3 - 0x33) – ECV_OC (SR4 - 0x34) – DSMON_HEAT (SR4 - 0x34) – OUTxHS_OL (SR5 - 0x35)(3) – OUTxLS_OL (SR5 - 0x35) – OUTx_OL (SR5 - 0x35) – OUTHS_OL (SR5 - 0x35) – GH_OL (SR5 - 0x35) – ECV_OL (SR5 - 0x35) 0: no error (default) 1: error detected FE is cleared by a *Read & Clear* command to all related bits in *Status Registers 2, 3, 4, 5*

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Table 85. GSB signals description (continued)

Bit	Name	Description
26	DE	Device Error Bit DE is a logical OR combination of global errors related to the device. – VS_OV (SR2 - 0x32) – VS_UV (SR2 - 0x32) – VSREG_OV (SR2 - 0x32) – VSREG_UV (SR2 - 0x32) – CP_LOW (SR2 - 0x32) – TSD1_CLx (SR6 - 0x36) 0: no error (default) 1: error detected DE is cleared by a *Read & Clear* command to all related bits in *Status Registers 2 and 6*
25	GW (2)	Global Warning Bit GW is a logical OR combination of warning flags. Warning bits do not lead to any device state change or switch off of functions. – VSREG_EW (SR2 - 0x32) – V1_FAIL (SR2 - 0x32) – V2_FAIL (SR2 - 0x32) – CAN_SUP_LOW (SR2 - 0x32) – TW (3) (SR2 - 0x32) – SPI_INV_CMD (SR2 - 0x32) – SPI_SCK_CNT (SR2 - 0x32) 0: no error (default) 1: error detected GW is cleared by a *Read & Clear* command to all related bits in *Status Register 2.*

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Table 85. GSB signals description (continued)

Bit	Name	Description
24	FS	Fail Safe The FS bit indicates the device was forced into a safe state due to the following failure conditions: – WDFAIL (SR1 - 0x31) – V1UV (SR1 - 0x31) – TSD2 (SR1 - 0x31) – FORCED_SLEEP_TSD/V1SC (SR1 - 0x31) All Control Registers are set to default except the following bits: – SWEN (CR1 - 0x01) – CR23 (0x17) to CR29 (0x1D); Configuration of CAN Selective Wake-up functionality Control Registers are blocked for WRITE access except the following bits: – TRIG (CR1 - 0x01) – V2_0 (CR1 - 0x01) – V2_1 (CR1 - 0x01) – GoTRXRDY (CR1 - 0x01) – Timer settings (bits 8…23) (CR2 - 0x02) – OUTHS_x (bits 0…3) (CR5 - 0x05) – OUT15_x (bits 0…3) (CR6 - 0x06) – CR12 (0x0C) to CR17 (0x11); PWM frequency and duty cycles 0: Fail Safe inactive (default) 1: Fail Safe active FS is cleared upon exit from Fail-Safe mode (refer to chapter ‘Fail-Safe mode’)

1. Individual failure flags may be masked in the Configuration Register (0x3F).
2. Bit may be masked in the Configuration Register (0x3F), i.e. the bit will not be included in the Global Status Bit (GSBN).
3. Open-load status flags may be masked in the Configuration register (0x3F), i.e. the open-load flag will be included in the FE flag, but will not set the GSBN. TW failure status flags may be masked in the Configuration register (0x3F), i.e. the TW flag will be included in the GW flag, but will not set the GSBN.

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7.2 Control register overview

Table 86. Control register overview

Addr.	Reg.	Bit 23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Access
0x00		reserved																								
0x01	CR1	Reserved	WU_EN	Reserved	WU_PU	Reserved		WU_FILT_1	WU_FILT_0	TIMER_NINT_WAKE_SEL	TIMER_NINT_EN	LIN_WU_EN	CAN_WU_EN	CANTO_IRQ_EN	CAN_RXEN	CAN_TXEN	CAN_Go_TRX_RDY	SWEN	HEN	V2_1	V2_0	PARITY	STBY_SEL	GO_STBY	TRIG	R/W
0x02	CR2	T1_RESTART	T1_DIR	T1_ON_2	T1_ON_1	T1_ON_0	T1_PER_2	T1_PER_1	T1_PER_0	T2_RESTART	T2_DIR	T2_ON_2	T2_ON_1	T2_ON_0	T2_PER_2	T2_PER_1	T2_PER_0	LIN_REC_ONLY	LIN_TXD_TOUT_EN	CAN_LOOP_EN	PNW_EN	V1_RESET_1	V1_RESET_0	WD_TIME_1	WD_TIME_0	R/W
0x03	CR3	VSREG_LOCK_EN	VS_LOCK_EN	VSREG_OV_SD_EN	VSREG_UV_SD_EN	VS_OV_SD_EN	VS_UV_SD_EN	Reserved								VSREG_EWTH_9	VSREG_EWTH_8	VSREG_EWTH_7	VSREG_EWTH_6	VSREG_EWTH_5	VSREG_EWTH_4	VSREG_EWTH_3	VSREG_EWTH_2	VSREG_EWTH_1	VSREG_EWTH_0	R/W
0x04	CR4	Reserved		OUT1_HS	OUT1_LS	Reserved		OUT2_HS	OUT2_LS	Reserved		OUT3_HS	OUT3_LS	Reserved		OUT4_HS	OUT4_LS	Reserved		OUT5_HS	OUT5_LS	Reserved		GH		R/W
0x05	CR5	OUT7_3	OUT7_2	OUT7_1	OUT7_0	OUT8_3	OUT8_2	OUT8_1	OUT8_0	Reserved				OUT10_3	OUT10_2	OUT10_1	OUT10_0	Reserved				OUTHS_3	OUTHS_2	OUTHS_1	OUTHS_0	R/W
0x06	CR6	OUT9_3	OUT9_2	OUT9_1	OUT9_0	OUT11_3	OUT11_2	OUT11_1	OUT11_0	OUT12_3	OUT12_2	OUT12_1	OUT12_0	OUT13_3	OUT13_2	OUT13_1	OUT13_0	OUT14_3	OUT14_2	OUT14_1	OUT14_0	OUT15_3	OUT15_2	OUT15_1	OUT15_0	R/W
0x07	CR7	OUT1_OCR	OUT2_OCR	OUT3_OCR	OUT4_OCR	OUT5_OCR	OUT6_OCR	OUT7_OCR	OUT8_OCR	OUTHS_OCR	Reserved		HB_TON_1	HB_TON_0	HS_TON_1	HS_TON_0	OCR_FREQ	OUT5_OC1	OUT5_OC0	CM_EN	Reserved	CM_SEL_3	CM_SEL_2	CM_SEL_1	CM_SEL_0	R/W

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Table 86. Control register overview (continued)

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0x08	CR8	OUT1_OCR_THX_EN	OUT2_OCR_THX_EN	OUT3_OCR_THX_EN	OUT4_OCR_THX_EN	OUT5_OCR_THX_EN	OUT6_OCR_THX_EN	OUT7_OCR_THX_EN	OUT8_OCR_THX_EN	OUTHS_OCR_THX_EN	Reserved															R/W
0x09	CR9	OUT7_RDSON	OUT8_RDSON	Reserved						OUTHS_OL	OUT15_OL	OUT14_OL	OUT13_OL	OUT12_OL	OUT11_OL	OUT10_OL	OUT9_OL	OUTHS_OC	OUT15_OC	OUT14_OC	OUT13_OC	OUT12_OC	OUT11_OC	OUT10_OC	OUT9_OC	R/W
0x0A	CR10	DIAG_2	DIAG_1	DIAG_0	GH_OL_EN	Reserved	GH_TH_2	GH_TH_1	GH_TH_0	Reserved		SD	SDS	COPT_3	COPT_2	COPT_1	COPT_0	H_OLTH_HIGH	OL_H1L2	OL_H2L1	SLEW_4	SLEW_3	SLEW_2	SLEW_1	SLEW_0	R/W
0x0B	CR11	Reserved										ECV_LS	ECV_OCR	Reserved			ECON	Reserved		EC_5	EC_4	EC_3	EC_2	EC_1	EC_0	R/W
0x0C	CR12	PMW1_FREQ_1	PMW1_FREQ_0	PMW2_FREQ_1	PMW2_FREQ_0	PMW3_FREQ_1	PMW3_FREQ_0	PMW4_FREQ_1	PMW4_FREQ_0	PMW5_FREQ_1	PMW5_FREQ_0	PMW6_FREQ_1	PMW6_FREQ_0	PMW7_FREQ_1	PMW7_FREQ_0	PMW8_FREQ_1	PMW8_FREQ_0	PMW9_FREQ_1	PMW9_FREQ_0	PMW10_FREQ_1	PMW10_FREQ_0	Reserved				R/W
0x0D	CR13	Reserved		PWM1_DC_9	PWM1_DC_8	PWM1_DC_7	PWM1_DC_6	PWM1_DC_5	PWM1_DC_4	PWM1_DC_3	PWM1_DC_2	PWM1_DC_1	PWM1_DC_0	Reserved		PWM2_DC_9	PWM2_DC_8	PWM2_DC_7	PWM2_DC_6	PWM2_DC_5	PWM2_DC_4	PWM2_DC_3	PWM2_DC_2	PWM2_DC_1	PWM2_DC_0	R/W
0x0E	CR14	Reserved		PWM3_DC_9	PWM3_DC_8	PWM3_DC_7	PWM3_DC_6	PWM3_DC_5	PWM3_DC_4	PWM3_DC_3	PWM3_DC_2	PWM3_DC_1	PWM3_DC_0	Reserved		PWM4_DC_9	PWM4_DC_8	PWM4_DC_7	PWM4_DC_6	PWM4_DC_5	PWM4_DC_4	PWM4_DC_3	PWM4_DC_2	PWM4_DC_1	PWM4_DC_0	R/W
0x0F	CR15	Reserved		PWM5_DC_9	PWM5_DC_8	PWM5_DC_7	PWM5_DC_6	PWM5_DC_5	PWM5_DC_4	PWM5_DC_3	PWM5_DC_2	PWM5_DC_1	PWM5_DC_0	Reserved		PWM6_DC_9	PWM6_DC_8	PWM6_DC_7	PWM6_DC_6	PWM6_DC_5	PWM6_DC_4	PWM6_DC_3	PWM6_DC_2	PWM6_DC_1	PWM6_DC_0	R/W

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Table 86. Control register overview (continued)

Addr.	Reg.	Bit																						Access
		23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x10	CR16	Reserved		PWM7_DC_9	PWM7_DC_8	PWM7_DC_7	PWM7_DC_6	PWM7_DC_5	PWM7_DC_4	PWM7_DC_3	PWM7_DC_2	PWM7_DC_1	PWM7_DC_0	Reserved		PWM8_DC_9	PWM8_DC_8	PWM8_DC_7	PWM8_DC_6	PWM8_DC_5	PWM8_DC_4	PWM8_DC_3	PWM8_DC_2	PWM8_DC_1	PWM8_DC_0	R/W
0x11	CR17	Reserved		PWM9_DC_9	PWM9_DC_8	PWM9_DC_7	PWM9_DC_6	PWM9_DC_5	PWM9_DC_4	PWM9_DC_3	PWM9_DC_2	PWM9_DC_1	PWM9_DC_0	Reserved		PWM10_DC_9	PWM10_DC_8	PWM10_DC_7	PWM10_DC_6	PWM10_DC_5	PWM10_DC_4	PWM10_DC_3	PWM10_DC_2	PWM10_DC_1	PWM10_DC_0	R/W
0x12	CR18	Reserved	OUT7_AUTOCOMP_EN	OUT7_VLED_9	OUT7_VLED_8	OUT7_VLED_7	OUT7_VLED_6	OUT7_VLED_5	OUT7_VLED_4	OUT7_VLED_3	OUT7_VLED_2	OUT7_VLED_1	OUT7_VLED_0	Reserved	OUT8_AUTOCOMP_EN	OUT8_VLED_9	OUT8_VLED_8	OUT8_VLED_7	OUT8_VLED_6	OUT8_VLED_5	OUT8_VLED_4	OUT8_VLED_3	OUT8_VLED_2	OUT8_VLED_1	OUT8_VLED_0	R/W
0x13	CR19	Reserved	OUT9_AUTOCOMP_EN	OUT9_VLED_9	OUT9_VLED_8	OUT9_VLED_7	OUT9_VLED_6	OUT9_VLED_5	OUT9_VLED_4	OUT9_VLED_3	OUT9_VLED_2	OUT9_VLED_1	OUT9_VLED_0	Reserved	OUT10_AUTOCOMP_EN	OUT10_VLED_9	OUT10_VLED_8	OUT10_VLED_7	OUT10_VLED_6	OUT10_VLED_5	OUT10_VLED_4	OUT10_VLED_3	OUT10_VLED_2	OUT10_VLED_1	OUT10_VLED_0	R/W
0x14	CR20	Reserved	OUT11_AUTOCOMP_EN	OUT11_VLED_9	OUT11_VLED_8	OUT11_VLED_7	OUT11_VLED_6	OUT11_VLED_5	OUT11_VLED_4	OUT11_VLED_3	OUT11_VLED_2	OUT11_VLED_1	OUT11_VLED_0	Reserved	OUT12_AUTOCOMP_EN	OUT12_VLED_9	OUT12_VLED_8	OUT12_VLED_7	OUT12_VLED_6	OUT12_VLED_5	OUT12_VLED_4	OUT12_VLED_3	OUT12_VLED_2	OUT12_VLED_1	OUT12_VLED_0	R/W

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Table 86. Control register overview (continued)

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0x15	CR21	Reserved	OUT13_AUTOCOMP_EN	OUT13_VLED_9	OUT13_VLED_8	OUT13_VLED_7	OUT13_VLED_6	OUT13_VLED_5	OUT13_VLED_4	OUT13_VLED_3	OUT13_VLED_2	OUT13_VLED_1	OUT13_VLED_0	Reserved	OUT14_AUTOCOMP_EN	OUT14_VLED_9	OUT14_VLED_8	OUT14_VLED_7	OUT14_VLED_6	OUT14_VLED_5	OUT14_VLED_4	OUT14_VLED_3	OUT14_VLED_2	OUT14_VLED_1	OUT14_VLED_0	R/W
0x16	CR22	Reserved	OUT15_AUTOCOMP_EN	OUT15_VLED_9	OUT15_VLED_8	OUT15_VLED_7	OUT15_VLED_6	OUT15_VLED_5	OUT15_VLED_4	OUT15_VLED_3	OUT15_VLED_2	OUT15_VLED_1	OUT15_VLED_0	Reserved	OUTHS_AUTOCOMP_EN	OUTHS_VLED_9	OUTHS_VLED_8	OUTHS_VLED_7	OUTHS_VLED_6	OUTHS_VLED_5	OUTHS_VLED_4	OUTHS_VLED_3	OUTHS_VLED_2	OUTHS_VLED_1	OUTHS_VLED_0	R/W
0x17	CR23	Reserved						EXT_ID_17	EXT_ID_16	EXT_ID_15	EXT_ID_14	EXT_ID_13	EXT_ID_12	EXT_ID_11	EXT_ID_10	EXT_ID_9	EXT_ID_8	EXT_ID_7	EXT_ID_6	EXT_ID_5	EXT_ID_4	EXT_ID_3	EXT_ID_2	EXT_ID_1	EXT_ID_0	R/W
0x18	CR24	Reserved	CAN_IDE	BR_1	BR_0	SAMPLE_3	SAMPLE_2	SAMPLE_1	SAMPLE_0	DLC_3	DLC_2	DLC_1	DLC_0	Reserved	ID_10	ID_9	ID_8	ID_7	ID_6	ID_5	ID_4	ID_3	ID_2	ID_1	ID_0	R/W
0x19	CR25	Reserved						EXT_ID_MASK_17	EXT_ID_MASK_16	EXT_ID_MASK_15	EXT_ID_MASK_14	EXT_ID_MASK_13	EXT_ID_MASK_12	EXT_ID_MASK_11	EXT_ID_MASK_10	EXT_ID_MASK_9	EXT_ID_MASK_8	EXT_ID_MASK_7	EXT_ID_MASK_6	EXT_ID_MASK_5	EXT_ID_MASK_4	EXT_ID_MASK_3	EXT_ID_MASK_2	EXT_ID_MASK_1	EXT_ID_MASK_0	R/W
0x1A	CR26	Reserved													ID_MASK_10	ID_MASK_9	ID_MASK_8	ID_MASK_7	ID_MASK_6	ID_MASK_5	ID_MASK_4	ID_MASK_3	ID_MASK_2	ID_MASK_1	ID_MASK_0	R/W
0x1B	CR27	DATA_BYTE3_7	DATA_BYTE3_6	DATA_BYTE3_5	DATA_BYTE3_4	DATA_BYTE3_3	DATA_BYTE3_2	DATA_BYTE3_1	DATA_BYTE3_0	DATA_BYTE2_7	DATA_BYTE2_6	DATA_BYTE2_5	DATA_BYTE2_4	DATA_BYTE2_3	DATA_BYTE2_2	DATA_BYTE2_1	DATA_BYTE2_0	DATA_BYTE1_7	DATA_BYTE1_6	DATA_BYTE1_5	DATA_BYTE1_4	DATA_BYTE1_3	DATA_BYTE1_2	DATA_BYTE1_1	DATA_BYTE1_0	R/W

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Table 86. Control register overview (continued)

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0x1C	CR28	DATA_BYTE6_7	DATA_BYTE6_6	DATA_BYTE6_5	DATA_BYTE6_4	DATA_BYTE6_3	DATA_BYTE6_2	DATA_BYTE6_1	DATA_BYTE6_0	DATA_BYTE5_7	DATA_BYTE5_6	DATA_BYTE5_5	DATA_BYTE5_4	DATA_BYTE5_3	DATA_BYTE5_2	DATA_BYTE5_1	DATA_BYTE5_0	DATA_BYTE4_7	DATA_BYTE4_6	DATA_BYTE4_5	DATA_BYTE4_4	DATA_BYTE4_3	DATA_BYTE4_2	DATA_BYTE4_1	DATA_BYTE4_0	R/W
0x1D	CR29	Reserved								DATA_BYTE8_7	DATA_BYTE8_6	DATA_BYTE8_5	DATA_BYTE8_4	DATA_BYTE8_3	DATA_BYTE8_2	DATA_BYTE8_1	DATA_BYTE8_0	DATA_BYTE7_7	DATA_BYTE7_6	DATA_BYTE7_5	DATA_BYTE7_4	DATA_BYTE7_3	DATA_BYTE7_2	DATA_BYTE7_1	DATA_BYTE7_0	R/W
0x22	CR34	Reserved																					CP_OFF	ICMP	WD_EN	R/W
0x3F	Conf Reg	WU_CONFIG	LIN_WU_CONFIG	LIN_HS_EN	TSD_CONFIG	ECV_HV	DM	ICMP_CONFIG_EN	WD_CONFIG_EN	MASK_OL_HS1	MASK_OL_LS1	MASK_TW	MASK_EC_OL	MASK_OL	MASK_SPIE	MASK_PLE	MASK_GW	CP_OFF_EN	CP_LOW_CONFIG	CP_DITH_DIS	FS_FORCED	CAN_SUP_5V2_EN	Reserved		TRIG	R/W

Note: All reserved bits (RES) are read-only (R) and will be read as '0'. Writing '1' to a reserved bit is ignored and does not cause an SPI error.

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7.3 Status register overview

Table 87. Status register overview

		Bit																						Access
Addr.	Reg.	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x31	SR1	Reserved	WU_STATE	Reserved	WU_WAKE	WAKE_CAN	WAKE_LIN	WAKE_TIMER	DEBUG_ACTIVE	V1UV	V1_RESTART_2	V1_RESTART_1	V1_RESTART_0	WDFAIL_CNT_3	WDFAIL_CNT_2	WDFAIL_CNT_1	WDFAIL_CNT_0	DEVICE_STATE_1	DEVICE_STATE_0	TSD2	TSD1	FORCED_SLEEP_TSD2/V1SC	FORCED_SLEEP_WD	WDFAIL	VPOR	R
0x32	SR2	LIN_PERM_DOM	LIN_TXD_DOM	LIN_PERM_REC	CAN_RXD_REC	CAN_PERM_REC	CAN_PERM_DOM	CAN_TXD_DOM	CAN_SUP_LOW	DSMON_HS2	DSMON_HS1	DSMON_LS2	DSMON_LS1	SPI_INV_CMD	SPI_SCK_CNT	CP_LOW	TW	V2SC	V2FAIL	V1FAIL	VSREG_EW	VSREG_OV	VSREG_UV	VS_OV	VS_UV	R
0x33	SR3	OUT1_HS_OC_TH_EX	OUT1_LS_OC_TH_EX	OUT2_HS_OC_TH_EX	OUT2_LS_OC_TH_EX	OUT3_HS_OC_TH_EX	OUT3_LS_OC_TH_EX	OUT4_HS_OC_TH_EX	OUT4_LS_OC_TH_EX	OUT5_HS_OC_TH_EX	OUT5_LS_OC_TH_EX	OUT6_HS_OC_TH_EX	OUT6_LS_OC_TH_EX	OUT7_OC_TH_EX	OUT8_OC_TH_EX	OUT9_OC	OUT10_OC	OUT11_OC	OUT12_OC	OUT13_OC	OUT14_OC	OUT15_OC	OUTHS_OC_TH_EX	LS2FSO_OC	LS1FSO_OC	R
0x34	SR4	OUT1_HS_OCR_ALERT	OUT1_LS_OCR_ALERT	OUT2_HS_OCR_ALERT	OUT2_LS_OCR_ALERT	OUT3_HS_OCR_ALERT	OUT3_LS_OCR_ALERT	OUT4_HS_OCR_ALERT	OUT4_LS_OCR_ALERT	OUT5_HS_OCR_ALERT	OUT5_LS_OCR_ALERT	OUT6_HS_OCR_ALERT	OUT6_LS_OCR_ALERT	OUT7_OCR_ALERT	OUT8_OCR_ALERT	Reserved							OUTHS_OCR_ALERT	DSMON_HEAT	ECV_OC	R
0x35	SR5	OUT1_HS_OL	OUT1_LS_OL	OUT2_HS_OL	OUT2_LS_OL	OUT3_HS_OL	OUT3_LS_OL	OUT4_HS_OL	OUT4_LS_OL	OUT5_HS_OL	OUT5_LS_OL	OUT6_HS_OL	OUT6_LS_OL	OUT7_OL	OUT8_OL	OUT9_OL	OUT10_OL	OUT11_OL	OUT12_OL	OUT13_OL	OUT14_OL	OUT15_OL	OUTHS_OL	GH_OL	ECV_OL	R

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Table 87. Status register overview

Addr.	Reg.	Bit 23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Access
0x36	SR6	WD_TIMER_STATE_1	WD_TIMER_STATE_0	Reserved				ECV_VNR	ECV_VHI	Reserved		TW_CL6	TW_CL5	TW_CL4	TW_CL3	TW_CL2	TW_CL1	Reserved		TSD1_CL6	TSD1_CL5	TSD1_CL4	TSD1_CL3	TSD1_CL2	TSD1_CL1	R
0x37	SR7	Reserved		TEMP_CL2_9	TEMP_CL2_8	TEMP_CL2_7	TEMP_CL2_6	TEMP_CL2_5	TEMP_CL2_4	TEMP_CL2_3	TEMP_CL2_2	TEMP_CL2_1	TEMP_CL2_0	Reserved		TEMP_CL1_9	TEMP_CL1_8	TEMP_CL1_7	TEMP_CL1_6	TEMP_CL1_5	TEMP_CL1_4	TEMP_CL1_3	TEMP_CL1_2	TEMP_CL1_1	TEMP_CL1_0	R
0x38	SR8	Reserved		TEMP_CL4_9	TEMP_CL4_8	TEMP_CL4_7	TEMP_CL4_6	TEMP_CL4_5	TEMP_CL4_4	TEMP_CL4_3	TEMP_CL4_2	TEMP_CL4_1	TEMP_CL4_0	Reserved		TEMP_CL3_9	TEMP_CL3_8	TEMP_CL3_7	TEMP_CL3_6	TEMP_CL3_5	TEMP_CL3_4	TEMP_CL3_3	TEMP_CL3_2	TEMP_CL3_1	TEMP_CL3_0	R
0x39	SR9	Reserved		TEMP_CL6_9	TEMP_CL6_8	TEMP_CL6_7	TEMP_CL6_6	TEMP_CL6_5	TEMP_CL6_4	TEMP_CL6_3	TEMP_CL6_2	TEMP_CL6_1	TEMP_CL6_0	Reserved		TEMP_CL5_9	TEMP_CL5_8	TEMP_CL5_7	TEMP_CL5_6	TEMP_CL5_5	TEMP_CL5_4	TEMP_CL5_3	TEMP_CL5_2	TEMP_CL5_1	TEMP_CL5_0	R
0x3A	SR10	Reserved		VSREG_9	VSREG_8	VSREG_7	VSREG_6	VSREG_5	VSREG_4	VSREG_3	VSREG_2	VSREG_1	VSREG_0	Reserved												R
0x3B	SR11	Reserved		VS_9	VS_8	VS_7	VS_6	VS_5	VS_4	VS_3	VS_2	VS_1	VS_0	Reserved		VWU_9	VWU_8	VWU_7	VWU_6	VWU_5	VWU_4	VWU_3	VWU_2	VWU_1	VWU_0	R
0x3C	SR12	Reserved			FECNT_4	FECNT_3	FECNT_2	FECNT_1	FECNT_0	Reserved	SWRD_CR29	SWRD_CR28	SWRD_CR27	SWRD_CR26	SWRD_CR25	SWRD_CR24	SWRD_CR23	SYSERR	OSC_FAIL	CAN_SILENT	TX_SYNC	CANTO	WUP	WUF	FDERR	R

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7.4 Control registers

7.4.1 Control Register CR1 (0x01)

Table 88. Control Register CR1

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	Reserved	WU_EN	Reserved	WU_PU	Reserved		WU_FILT_1	WU_FILT_0	TIMER_NIONT_WAKE_SEL	TIMER_NINT_EN	LIN_WU_EN(1)	CAN_WU_EN(1)	CANTO_IRQ_EN	CAN_RXEN	CAN_TXEN	CAN_ Go_TRX_RDY	SWEN	HEN	V2_1	V2_0	PARITY	STBY_SEL	GO_STBY	TRIG
Reset	0	1	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0
Access	R	R/W	R	R/W	R		R/W																	

1. Either LIN or CAN must be enabled as wake-up source. Setting both bits 12 and 13 to '0' is an invalid setting. In this case, both bits will be set to '1' (wake-up enabled; default) and the SPI Error Bit (SPIE) in the Global Status Byte will be set.

Table 89. CR1 signals description

Bit	Name	Description
23	Reserved	—
22	WU_EN	Wake-up Input 1 (WU) enable(1) 0: WU disabled 1: WU enabled (default)
21	Reserved	—
20	WU_PU	Wake-up Input1 Pull-up/down configuration: configuration of internal current source(1) 0: pull-down (default) 1: pull-up
19	Reserved	—
18		
17	WU_FILT_1	Wake-up Input1 Filter configuration Bits: configuration of input filter(1) See *Table 90: Wake-up input1 filter configuration*
16	WU_FILT_0	
15	TIMER_NINT_WAKE_SEL	Select Timer for NINT / Wake: select timer for periodic interrupt in standby modes 0: Timer 2 (default) 1: Timer 1

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Table 89. CR1 signals description (continued)

Bit	Name	Description
14	TIMER_NINT_EN	Timer NINT enable: enable timer interrupt in standby modes 0: timer interrupt disabled (default) 1: timer interrupt enabled V1_standby mode: periodic NINT pulse generated by timer (NINT pulse at start of timer on-phase) Vbat_standby mode: device wakes up after timer expiration and generates NReset
13	LIN_WU_EN (2)	LIN Wake-up enable: enable wake-up by LIN(3) 0: disabled 1: enabled (default)
12	CAN_WU_EN (2)	CAN Wake-up enable: enable wake-up by CAN(4) 0: disabled 1: enabled (default)
11	CANTO_ IRQ_EN	CANTO Interrupt enable: enables interrupt signal in case of CAN timeout 0: CAN TO interrupt disabled 1: CAN TO interrupt enabled (default)
10	CAN_ RXEN	CAN transceiver configuration See *Table 91: CAN transceiver mode*
9	CAN_TXEN	
8	CAN_Go_TRX_RDY	CAN Transceiver transition into TRX READY mode. 0: CAN transceiver in TRX BIAS mode (default) 1: CAN transceiver is sent into TRX READY mode At Exit from TRX READY mode, this bit is set to '0' automatically. CAN Flash mode: CAN Go TRX RDY is set to '1' automatically After power-on, this bit should be set to ’0’ and a clear command should be sent to status registers.
7	SWEN	CAN Selective Wake-up enable: enable selective wake-up for CAN(5) 0: No Selective Wakeup (default) 1: Selective Wakeup enabled
6	HEN	Enable H-bridge 0: H-bridge disabled (default) 1: H-bridge enabled Refer to chapter *H-bridge Control* for details
5	V2_1	Voltage Regulator V2 Configuration See *Table 92: Voltage regulator V2 configuration*
4	V2_0	

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Table 89. CR1 signals description (continued)

Bit	Name	Description
3	PARITY	PARITY: Standby Command Parity Bit STBY SEL: Select Standby mode GO_STBY: Execute transition into Standby mode The STBY_SEL and GO_STBY bits are protected by a parity check. The bits STBY_SEL, GO_STBY and PARITY must represent an even number of '1', otherwise the command is ignored and the SPI_INV_CMD bit is set. *Table 93: Standby transition configuration* shows the valid settings. All other settings are invalid; command will be ignored and SPI_INV_CMD will be set. The GO_STBY bit is not cleared automatically after wake-up.
2	STBY_SEL	
1	GO_STBY	
0	TRIG	Watchdog Trigger Bit

1. Setting is only valid if input is configured as wake-up input in Configuration Register (0x3F).
2. Either LIN or CAN must be enabled as wake-up source. Setting both bits 12 and 13 to '0' is an invalid setting. All wake-up sources will be configured according to default setting; SPI Error Bit (SPIE) in Global Status Byte will be set.
3. The wake-up behavior is configurable in the Configuration Register (0x3F).
4. Wake-up occurs at a wake –up event according to ISO 11898-5:2007 (default) Wake-up according ISO 11898-6:2013 (selective wake-up) is configurable (refer to chapter High Speed CAN Bus Transceiver).
5. A dedicated procedure must be followed to set SWEN (CR 1) = 1 (refer to chapter High Speed CAN Bus Transceiver).

Table 90. Wake-up input1 filter configuration

WU_FILT_1	WU_FILT_0	
0	0	Wake-up inputs monitored in static mode (filter time twu_stat) (default)
0	1	Wake- up inputs monitored in cyclic mode with Timer2 (filter time: t_{WU_cyc}; blanking time 80% of timer ON time)
1	0	Wake- up inputs monitored in cyclic mode with Timer1 (filter time: t_{WU_cyc}; blanking time 80% of timer ON time)
1	1	Invalid setting; command will be ignored and SPI INV CMD will be set

Table 91. CAN transceiver mode

CAN_RXEN	CAN_TXEN	
0	x	TRX Standby: Receiver disabled, Transmitter disabled
0	x	
1	0	TRX Listen: Receiver enabled, Transmitter disabled
1	1	TRX Normal(1): Receiver enabled, Transmitter enabled

1. CAN Flash mode: TRX Normal Mode functionality is configured automatically but SPI registers are not updated.

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Table 92. Voltage regulator V2 configuration

V2_1	V2_0	
0	0	V2 OFF in all modes (default)
0	1	V2 ON in Active mode; OFF in Standby modes
1	0	V2 ON in Active and V1_standby mode; OFF in Vbat_standby mode
1	1	V2 ON in all modes(1)

1. This configuration will not be taken into account if CAN_SUP_5V2_EN = 1.

Table 93. Standby transition configuration

PARITY	STBY_SEL	GO_STBY	
0	1	1	Go to V1 standby
1	0	1	Go to Vbat_standby
0	0	0	No transition to standby
1	1	0	

7.4.2 Control Register CR2 (0x02)

Table 94. Control Register CR2

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	T1_RESTART	T1_DIR	T1_ON_2	T1_ON_1	T1_ON_0	T1_PER_2	T1_PER_1	T1_PER_0	T2_RESTART	T2_DIR	T2_ON_2	T2_ON_1	T2_ON_0	T2_PER_2	T2_PER_1	T2_PER_0	LIN_REC_ONLY	LIN_TXD_TOUT_EN	CAN_LOOP_EN	PNW_EN	V1_RESET_1	V1_RESET_0	WD_TIME_1	WD_TIME_0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
Access	R/W																							

Table 95. CR2 signals description

Bit	Name	Description
23	T1_RESTART	Timer 1 Restart: Restart of Timer 1 0: timer is running with period and on-time according to configuration (default) 1: restart of timer at CSN low to high transition; starting with ON phase(1) Bit is automatically reset with next SPI frame.
22	T1_DIR1	T1_DIR1: Timer 1 Direct Drive by DIR1 T1_ON_x: Timer 1 On-Time Bits Configuration of Timer 1 on-time, for details see *Table 96* and *Figure 60*
21	T1_ON_2	
20	T1_ON_1	
19	T1_ON_0	

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Table 95. CR2 signals description (continued)

Bit	Name	Description
18	T1_PER_2	Configuration of Timer 1 Period 000: T1 (default) 001: T2 010: T3 011: T4 100: T5 101: T6 110: T7 111: T8
17	T1_PER_1	
16	T1_PER_0	
15	T2_RESTART	Timer 2 Restart: restart of timer 2 0: timer is running with period and on-time according to configuration (default) 1: restart of timer at CSN low to high transition; starting with ON phase(1) Bit is automatically reset with next SPI frame.
14	T2_DIR1	T2_DIR1: Timer 2 Direct Drive by DIR1 T2_ON_x: Timer 2 On-Time Bits Configuration of Timer 2 on-time, for details see *Table 96* and *Figure 60*
13	T2_ON_2	
12	T2_ON_1	
11	T2_ON_0	
10	T2_PER_2	Configuration of Timer 2 Period 000: T1 (default) 001: T2 010: T3 011: T4 100: T5 101: T6 110: T7 111: T8
9	T2_PER_1	
8	T2_PER_0	
7	LIN_REC_ONLY	LIN Transceiver Receive Only mode 0: LIN receive only mode disabled (default) 1: LIN receive only mode enabled
6	LIN_TXD_TOUT_EN	LIN TxD Timeout Enable 0: LIN TxD timeout detection disabled 1: LIN TxD timeout detection enabled (default)
5	CAN_LOOP_EN	CAN Loop Enable: CAN Looping of TxDC to RxDC 0: CAN looping disabled (default) 1: CAN looping enabled

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Table 95. CR2 signals description (continued)

Bit	Name	Description
4	PNW_EN	CAN Pretented Networking mode A WUP leads to transition into TRX Bias mode and an interrupt is generated. 0: pretended networking disabled (default) 1: pretended networking enabled This bit can only be set to '1' if: SWEN = 0 (selective wake-up disabled) CAN RXEN = 1 The bit is automatically reset to '0' if selective wake-up is enabled (SWEN = 1) device enters Vbat_standby mode
3	V1_RESET_1	Voltage Regulator V1 Reset Threshold 00: Vrt4 (default) 01: Vrt3 10: Vrt2 11: Vrt1 thresholds are monitored in Active mode and V1_standby mode
2	V1_RESET_0	
1	WD_TIME_1	Watchdog Trigger Time 00: TSW1 (default) 01: TSW2 10: TSW3 11: TSW4 Writing to WD_TIME_x is blocked unless WD CONFIG EN = 1. The modified WD Trigger Time is valid immediately after the Write command (CSN transition low-high). The watchdog timer is reset when the trigger time is modified (restart at CSN transition low-high).
0	WD_TIME_0	

1. Timer restart behavior:
Write to CR2 when Tx_ON_x and Tx_PERx remain unchanged:
Tx_RESTART = 1: timers restart at end of SPI frame, starting with ON time
Tx_RESTART = 0: write operation to CR2 has no effect on timers
Write to CR2 when Tx_ON_x and Tx_PERx are modified
Tx_RESTART = 1: timers restart at end of SPI frame, starting with ON time and according to new setting (ON time and period)
Tx_RESTART = 0: behavior is not defined; if a predictable behavior is needed, it is recommended to set Tx_RESTART = 1

Table 96. Configuration of Timer x on-time

Tx_DIR1	Tx_ON_2	Tx_ON_1	Tx_ON_0	
0	0	0	0	ton1 (default)
0	0	0	1	ton2
0	0	1	0	ton3
0	0	1	1	ton4
0	1	0	0	ton5
0	1	0	1	Invalid setting; command will be ignored and *SPI INV CMD* will be set
0	1	1	0	
0	1	1	1	

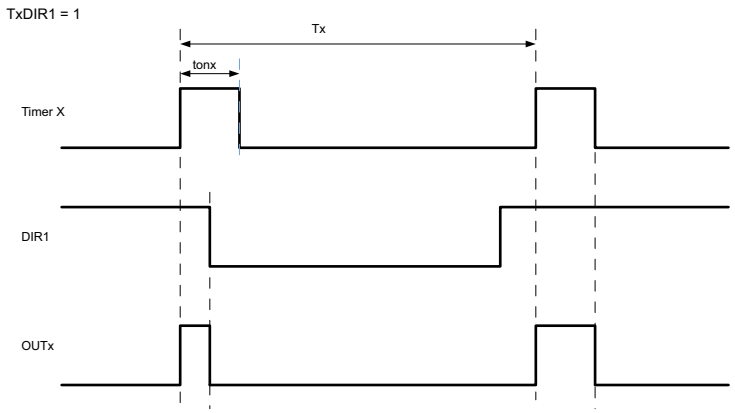
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Table 96. Configuration of Timer x on-time (continued)

Tx_DIR1	Tx_ON_2	Tx_ON_1	Tx_ON_0	
1(1)	0	0	0	ton1 controlled by DIR1 input signal (logical AND)
1(1)	0	0	1	ton2 controlled by DIR1 input signal (logical AND)
1(1)	0	1	0	ton3 controlled by DIR1 input signal (logical AND)
1(1)	0	1	1	ton4 controlled by DIR1 input signal (logical AND)
1(1)	1	0	0	ton5 controlled by DIR1 input signal (logical AND)
1(1)	1	0	1	Invalid setting; command will be ignored and *SPI INV CMD* will be set
1(1)	1	1	0	
1(1)	1	1	1	

1. Tx_DIR1 = 1 is only valid for OUT7-OUT15 and OUT_HS control; the DIR1 signal has no influence for WU monitoring if WU is monitored by timer.

Figure 60. Timer_x controlled by DIR1



7.4.3 Control Register CR3 (0x03)

Table 97. Control Register CR3

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	VSREG_LOCK_EN	VS_LOCK_EN	VSREG_OV_SD_EN	VSREG_UV_SD_EN	VS_OV_SD_EN	VS_UV_SD_EN	Reserved								VSREG_EWTH_9	VSREG_EWTH_8	VSREG_EWTH_7	VSREG_EWTH_6	VSREG_EWTH_5	VSREG_EWTH_4	VSREG_EWTH_3	VSREG_EWTH_2	VSREG_EWTH_1	VSREG_EWTH_0
Reset	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W																							

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Table 98. CR3 signals description

Bit	Name	Description
23	VSREG_LOCK_EN	V_{SREG} lockout enable: Lockout of V_{SREG} related outputs after V_{SREG} overvoltage/ undervoltage shutdown 0: V_{SREG} related Outputs are turned on automatically and status bits (VSREG_UV, VSREG_OV) are cleared 1: V_{SREG} related Outputs remain turned off until status bits (VSREG_UV, VSREG_OV) are cleared (default) Lockout is always disabled in standby modes in order to ensure supply of external contacts and detect wake-up conditions
22	VS_LOCK_EN	V_S lockout enable: Lockout of V_S related outputs after V_S over/undervoltage shutdown 0: V_S related Outputs are turned on automatically and status bits (VS_UV, VS_OV) are cleared 1: V_S related Outputs remain turned off until status bits (VS_UV, VS_OV) are cleared (default) Lockout is always disabled in standby modes in order to ensure supply of external contacts and detect wake-up conditions
21	VSREG_OV_SD_EN	V_{SREG} overvoltage shutdown enable: shutdown of V_{SREG} related outputs in case of V_{SREG} overvoltage 0: no shutdown of V_{SREG} related outputs in case of V_{SREG} overvoltage 1: shutdown of V_{SREG} related outputs in case of V_{SREG} overvoltage (default)
20	VSREG_UV_SD_EN	V_{SREG} undervoltage shutdown enable: shutdown of V_{SREG} related outputs in case of V_{SREG} undervoltage 0: no shutdown of V_{SREG} related outputs in case of V_{SREG} undervoltage 1: shutdown of V_{SREG} related outputs in case of V_{SREG} undervoltage (default) In case of V1 undervoltage due to VSREG_UV, the device enters Fail-Safe mode and the outputs are turned off
19	VS_OV_SD_EN	V_S overvoltage shutdown enable: shutdown of V_S related outputs in case of V_S overvoltage 0: no shutdown of V_S related outputs in case of V_S overvoltage if charge pump output voltage is still sufficient (until CPLOW threshold is reached) 1: shutdown of V_S related outputs in case of V_S overvoltage (default)
18	VS_UV_SD_EN	V_S undervoltage shutdown enable: shutdown of V_S related outputs in case of V_S undervoltage 0: no shutdown V_S related of outputs in case of V_S undervoltage 1: shutdown of V_S related outputs in case of V_S undervoltage (default) In case of V1 undervoltage due to VS_UV, the device enters Fail-Safe mode and the outputs are turned off
17:10	Reserved	Reserved

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Table 98. CR3 signals description (continued)

Bit	Name	Description
9	VSREG_EW_TH_9	V_{SREG} early warning threshold. At V_{SREG} < VSREG_EW_TH, an interrupt is generated at NINT and status bit VSREG_EW in SR2 is set (in Active mode) 0000000000: 0 V (default) feature deactivated ... 1111111111: V_{AINVS}
8	VSREG_EW_TH_8	
7	VSREG_EW_TH_7	
6	VSREG_EW_TH_6	
5	VSREG_EW_TH_5	
4	VSREG_EW_TH_4	
3	VSREG_EW_TH_3	
2	VSREG_EW_TH_2	
1	VSREG_EW_TH_1	
0	VSREG_EW_TH_0	

7.4.4 Control Register CR4 (0x04)

Table 99. Control Register CR4

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	Reserved		OUT1_HS	OUT1_LS	Reserved		OUT2_HS	OUT2_LS	Reserved		OUT3_HS	OUT3_LS	Reserved		OUT4_HS	OUT4_LS	Reserved		OUT5_HS	OUT5_LS	Reserved		OUT6_HS	OUT6_LS
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W																							

Table 100. CR4 signals description

Bit	Name	Description
23:22	Reserved	Reserved
21	OUT1_HS	OUT1 High-Side Driver control 0: OUT1_HS is turned off (default) 1: OUT1_HS is turned on An internal cross-current protection prevents, that both the low- and high-side drivers of the half-bridge OUT1 are switched on simultaneously.
20	OUT1_LS	OUT1 Low-Side Driver control 0: OUT1_LS is turned off (default) 1: OUT1_LS is turned on An internal cross-current protection prevents, that both the low- and high-side drivers of the half-bridge OUT1 are switched on simultaneously.
19:18	Reserved	Reserved

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Table 100. CR4 signals description (continued)

Bit	Name	Description
17	OUT2_HS	OUT2 High-Side Driver control 0: OUT2_HS is turned off (default) 1: OUT2_HS is turned on An internal cross-current protection prevents, that both the low- and high-side drivers of the half-bridge OUT2 are switched on simultaneously.
16	OUT2_LS	OUT2 Low-Side Driver control 0: OUT2_LS is turned off (default) 1: OUT2_LS is turned on An internal cross-current protection prevents, that both the low- and high-side drivers of the half-bridge OUT2 are switched on simultaneously.
15:14	Reserved	Reserved
13	OUT3_HS	OUT3 High-Side Driver control 0: OUT3_HS is turned off (default) 1: OUT3_HS is turned on An internal cross-current protection prevents, that both the low- and high-side drivers of the half-bridge OUT3 are switched on simultaneously.
12	OUT3_LS	OUT3 Low-Side Driver control 0: OUT3_LS is turned off (default) 1: OUT3_LS is turned on An internal cross-current protection prevents, that both the low- and high-side drivers of the half-bridge OUT3 are switched on simultaneously.
11:10	Resrved	Reserved
9	OUT4_HS	OUT4 High-Side Driver control 0: OUT4_HS is turned off (default) 1: OUT4_HS is turned on An internal cross-current protection prevents, that both the low- and high-side drivers of the half-bridge OUT4 are switched on simultaneously.
8	OUT4_LS	OUT4 Low-Side Driver control 0: OUT4_LS is turned off (default) 1: OUT4_LS is turned on An internal cross-current protection prevents, that both the low- and high-side drivers of the half-bridge OUT4 are switched on simultaneously.
7:6	Reserved	Reserved
5	OUT5_HS	OUT5 High-Side Driver control 0: OUT5_HS is turned off (default) 1: OUT5_HS is turned on An internal cross-current protection prevents, that both the low- and high-side drivers of the half-bridge OUT5 are switched on simultaneously.
4	OUT5_LS	OUT5 Low-side Driver control 0: OUT5_LS is turned off (default) 1: OUT5_LS is turned on An internal cross-current protection prevents, that both the low- and high-side drivers of the half-bridge OUT5 are switched on simultaneously.

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Table 100. CR4 signals description (continued)

Bit	Name	Description
3:2	Reserved	Reserved
1	OUT6_HS	OUT6 High-side Driver control 0: OUT6_HS is turned off (default) 1: OUT6_HS is turned on An internal cross-current protection prevents, that both the low-side and high-side drivers of the half-bridge OUT6 are switched on simultaneously.
0	OUT6_LS	OUT6 Low-side Driver control 0: OUT6_LS is turned off (default) 1: OUT6_LS is turned on An internal cross-current protection prevents, that both the low-side and high-side drivers of the half-bridge OUT6 are switched on simultaneously.

7.4.5 Control Register CR5 (0x05)

Table 101. Control Register CR5

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	OUT7_3	OUT7_2	OUT7_1	OUT7_0	OUT8_3	OUT8_2	OUT8_1	OUT8_0	Reserved				OUT10_3	OUT10_2	OUT10_1	OUT10_0	Reserved			GH	OUTHS_3	OUTHS_2	OUTHS_1	OUTHS_0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W																							

Table 102. CR5 signals description

Bit	Name	Description
23	OUT7_3	OUT7 Configuration Bits: High-Side Driver OUT7 Configuration For OUT7 bits configuration see *Table 103: OUTx Configuration bits*
22	OUT7_2	
21	OUT7_1	
20	OUT7_0	
19	OUT8_3	OUT8 Configuration Bits: High-Side Driver OUT8 Configuration For OUT8 bits configuration see *Table 103: OUTx Configuration bits*
18	OUT8_2	
17	OUT8_1	
16	OUT8_0	
15:12	Reserved	—
11	OUT10_3	OUT10 Configuration Bits: High-Side Driver OUT10 Configuration For OUT10 bits configuration see *Table 103: OUTx Configuration bits*
10	OUT10_2	
9	OUT10_1	
8	OUT10_0	

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Table 102. CR5 signals description (continued)

Bit	Name	Description
7:5	Reserved	—
4	GH	Gate Heater Control: Control of gate driver for external heater MOSFET 0: GH_heater is turned off (default) 1: GH_heater is turned on
3	OUTHS_3	OUTHS Configuration Bits: High-side Driver OUTHS Configuration For OUTHS bits configuration see *Table 103: OUTx Configuration bits*
2	OUTHS_2	
1	OUTHS_1	
0	OUTHS_0	

Table 103. OUTx Configuration bits

OUTx_3	OUTx_2	OUTx_1	OUTx_0	Description
0	0	0	0	Off (default)
0	0	0	1	On
0	0	1	0	Timer1
0	0	1	1	Timer2
0	1	0	0	PWM1
0	1	0	1	PWM2
0	1	1	0	PWM3
0	1	1	1	PWM4
1	0	0	0	PWM5
1	0	0	1	PWM6
1	0	1	0	PWM7
1	0	1	1	PWM8
1	1	0	0	PWM9
1	1	0	1	PWM10
1	1	1	0	DIR1
1	1	1	1	DIR2

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7.4.6 Control Register CR6 (0x06)

Table 104. Control Register CR6

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	OUT9_3	OUT9_2	OUT9_1	OUT9_0	OUT11_3	OUT11_2	OUT11_1	OUT11_0	OUT12_3	OUT12_2	OUT12_1	OUT12_0	OUT13_3	OUT13_2	OUT13_1	OUT13_0	OUT14_3	OUT14_2	OUT14_1	OUT14_0	OUT15_3	OUT15_2	OUT15_1	OUT15_0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W																							

Table 105. CR6 signals description

Bit	Name	Description
23	OUT9_3	OUT9 Configuration Bits: High-Side Driver OUT9 Configuration For OUT9 bits configuration see *Table 103: OUTx Configuration bits*
22	OUT9_2	
21	OUT9_1	
20	OUT9_0	
19	OUT11_3	OUT11 Configuration Bits: High-Side Driver OUT11 Configuration For OUT11 bits configuration see *Table 103: OUTx Configuration bits*
18	OUT11_2	
17	OUT11_1	
16	OUT11_0	
15	OUT12_3	OUT12 Configuration Bits: High-Side Driver OUT12 Configuration For OUT12 bits configuration see *Table 103: OUTx Configuration bits*
14	OUT12_2	
13	OUT12_1	
12	OUT12_0	
11	OUT13_3	OUT13 Configuration Bits: High-Side Driver OUT13 Configuration For OUT13 bits configuration see *Table 103: OUTx Configuration bits*
10	OUT13_2	
9	OUT13_1	
8	OUT13_0	
7	OUT14_3	OUT14 Configuration Bits: High-Side Driver OUT14 Configuration For OUT14 bits configuration see *Table 103: OUTx Configuration bits*
6	OUT14_2	
5	OUT14_1	
4	OUT14_0	
3	OUT15_3	OUT15 Configuration Bits: High-side Driver OUT15 Configuration For OUT15 bits configuration see *Table 103: OUTx Configuration bits*
2	OUT15_2	
1	OUT15_1	
0	OUT15_0	

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7.4.7 Control Register CR7 (0x07)

Table 106. Control Register CR7

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	OUT1_OCR	OUT2_OCR	OUT3_OCR	OUT4_OCR	OUT5_OCR	OUT6_OCR	OUT7_OCR	OUT8_OCR	OUTHS_OCR	Reserved		HB_TON_1	HB_TON_0	HS_TON_1	HS_TON_0	OCR_FREQ	OUT5_OC1	OUT5_OC0	CM_EN	Reserved	CM_SEL_3	CM_SEL_2	CM_SEL_1	CM_SEL_0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
Access	R/W																							

Table 107. CR7 signals description

Bit	Name	Description
23	OUT1_OCR	Overcurrent recovery for OUTx 0: overcurrent recovery is turned off (default) 1: overcurrent recovery is turned on
22	OUT2_OCR	
21	OUT3_OCR	
20	OUT4_OCR	
19	OUT5_OCR	
18	OUT6_OCR	
17	OUT7_OCR	
16	OUT8_OCR	
15	OUTHS_OCR	Overcurrent recovery for OUTHS 0: overcurrent recovery is turned off (default) 1: overcurrent recovery is turned on
14:13	Reserved	—
12	HB_TON_1	Half-bridge minimum ON time and related overcurrent recovery frequency For details see *Table 108: Half-bridge minimum ON time and related overcurrent recovery frequency*
11	HB_TON_0	
10	HS_TON_1	High-side minimum ON time and related overcurrent recovery frequency For details see *Table 109: High-side minimum ON time and related overcurrent recovery frequency*
9	HS_TON_0	
8	OCR_FREQ	Overcurrent recovery frequency See *Table 108: Half-bridge minimum ON time and related overcurrent recovery frequency* and *Table 109: High-side minimum ON time and related overcurrent recovery frequency*
7	OUT5_OC1	Overcurrent Threshold for OUT5 00: IOC5_3 overcurrent threshold 3 (default) 01: IOC5_1 overcurrent threshold 1 10: IOC5_2 overcurrent threshold 2 11: IOC5_3 overcurrent threshold 3
6	OUT5_OC0	

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Table 107. CR7 signals description (continued)

Bit	Name	Description
5	CM_EN	Current monitor: 0: off (3-state) 1: on (default)
4	Reserved	—
3	CM_SEL_3	Current Monitor Select Bits. A current image of the selected binary coded output is multiplexed to the CM output. If a corresponding output does not exist, the current monitor is deactivated. 0000: OUT1 0001: OUT2 0010: OUT3 0011: OUT4 0100: OUT5 0101: OUT6 0110: OUT7 0111: OUT8 1000: OUT9 1001: OUT10 1010: OUT11 1011: OUT12 1100: OUT13 1101: OUT14 1110: OUT15 1111: OUT_HS
2	CM_SEL_2	
1	CM_SEL_1	
0	CM_SEL_0	

Table 108. Half-bridge minimum ON time and related overcurrent recovery frequency

HB_TON_1	HB_TON_	OCR_FREQ	T_{ON_min} (recovery frequency)
0	0	0	104 µs (1.7 kHz)
0	0	1	104 µs (3 kHz)
0	1	0	88 µs (2.2 kHz)
0	1	1	88 µs (3.8 kHz)
1	0	0	80 µs (2.6 kHz)
1	0	1	80 µs (4.4 kHz)
1	1	0	72 µs (3 kHz)
1	1	1	72 µs (5 kHz)

Table 109. High-side minimum ON time and related overcurrent recovery frequency

HS_TON_1	HS_TON_	OCR_FREQ	T_{ON_min} (recovery frequency)
0	0	0	104 µs (1.7 kHz)
0	0	1	104 µs (3 kHz)

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Table 109. High-side minimum ON time and related overcurrent recovery frequency

HS_TON_1	HS_TON_	OCR_FREQ	T_{ON_min} (recovery frequency)
0	1	0	88 µs (2.2 kHz)
0	1	1	88 µs (3.8 kHz)
1	0	0	80 µs (2.6 kHz)
1	0	1	80 µs (4.4 kHz)
1	1	0	72 µs (3 kHz)
1	1	1	72 µs (5 kHz)

7.4.8 Control Register CR8 (0x08)

Table 110. Control Register CR8

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	OUT1_OCR_THX_EN	OUT2_OCR_THX_EN	OUT3_OCR_THX_EN	OUT4_OCR_THX_EN	OUT5_OCR_THX_EN	OUT6_OCR_THX_EN	OUT7_OCR_THX_EN	OUT8_OCR_THX_EN	OUTHS_OCR_THX_EN	Resrved														
Reset	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W																							

Table 111. CR8 signals description

Bit	Name	Description
23	OUT1_OCR_THX_EN	Enable Overcurrent Recovery with Thermal Expiration for OUTx. 0: Overcurrent Recovery with Thermal Expiration is off 1: Overcurrent Recovery with Thermal Expiration is on (default) The output is turned off after Thermal Expiration.
22	OUT2_OCR_THX_EN	
21	OUT3_OCR_THX_EN	
20	OUT4_OCR_THX_EN	
19	OUT5_OCR_THX_EN	
18	OUT6_OCR_THX_EN	
17	OUT7_OCR_THX_EN	
16	OUT8_OCR_THX_EN	

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Table 111. CR8 signals description (continued)

Bit	Name	Description
15	OUTHS_OCR_THX_EN	Enable Overcurrent Recovery with Thermal Expiration for OUTHS. 0: Overcurrent Recovery with Thermal Expiration is off 1: Overcurrent Recovery with Thermal Expiration is on (default) The output is turned off after Thermal Expiration.
14:0	Reserved	—

7.4.9 Control Register CR9 (0x09)

Table 112. Control Register CR9

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	OUT7_RDSON	OUT8_RDSON	Reserved						OUTHS_OL	OUT15_OL	OUT14_OL	OUT13_OL	OUT12_OL	OUT11_OL	OUT10_OL	OUT9_OL	OUTHS_OC	OUT15_OC	OUT14_OC	OUT13_OC	OUT12_OC	OUT11_OC	OUT10_OC	OUT9_OC
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W																							

Table 113. CR9 signals description

Bit	Name	Description
23	OUT7_RDSON	Select Rdson for OUT7 0: r_{on_low} (default) 1: r_{on_high}
22	OUT8_RDSON	Select Rdson for OUT8 0: r_{on_low} (default) 1: r_{on_high}
21:16	Reserved	—
15	OUTHS_OL	Open-load Threshold for OUTx 0: I_{OLD1} ; high-current mode (default) 1: I_{OLD1}; low-current mode
14	OUT15_OL	
13	OUT14_OL	
12	OUT13_OL	
11	OUT12_OL	
10	OUT11_OL	
9	OUT10_OL	
8	OUT9_OL	

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Table 113. CR9 signals description (continued)

Bit	Name	Description
7	OUTHS_OC	Overcurrent Threshold for OUTx 0: I_{OC}; high-current mode (default) 1: I_{OC}; low-current mode
6	OUT15_OC	
5	OUT14_OC	
4	OUT13_OC	
3	OUT12_OC	
2	OUT11_OC	
1	OUT10_OC	
0	OUT9_OC	

7.4.10 Control Register CR10 (0x0A)

Table 114. Control Register CR10

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	DIAG_2	DIAG_1	DIAG_0	GH_OL_EN	Reserved	GH_TH_2	GH_TH_1	GH_TH_0	Reserved		SD	SDS	COPT_3	COPT_2	COPT_1	COPT_0	H_OLTH_HIGH	OL_H1L2	OL_H2L1	SLEW_4	SLEW_3	SLEW_2	SLEW_1	SLEW_0
Reset	1	1	1	0	0	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0
Access	R/W																							

Table 115. CR10 signals description

Bit	Name	Description
23	DIAG_2	Drain-source monitoring threshold for external H-bridge 000: V_{SCd1_HB} 001: V_{SCd2_HB} 010: V_{SCd3_HB} 011: V_{SCd4_HB} 100: V_{SCd5_HB} 101: V_{SCd6_HB} 110: V_{SCd7_HB} 111: V_{SCd7_HB} (default)
22	DIAG_1	
21	DIAG_0	
20	GH_OL_EN	Control open-load diagnosis for Gate Heater output 0: open-load diagnosis off (default) 1: open-load diagnosis on
19	Reserved	—

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Table 115. CR10 signals description (continued)

Bit	Name	Description
18	GH_TH_2	Drain source monitoring threshold voltage for external heater MOSFET 000: V_{SCd1_HE} 001: V_{SCd2_HE} 010: V_{SCd3_HE} 011: V_{SCd4_HE} 100: V_{SCd5_HE} 101: V_{SCd6_HE} 110: V_{SCd7_HE} 111: V_{SCd8_HE} (default)
17	GH_TH_1	
16	GH_TH_0	
15:14	Reserved	—
13	SD	Slow decay
12	SDS	Slow decay single
11	COPT_3	Cross current protection time 0000: not allowed 0001: $tccp_{0001}$ 0010: $tccp_{0010}$ 0011: $tccp_{0011}$ 0100: $tccp_{0100}$ 0101: $tccp_{0101}$ 0110: $tccp_{0110}$ 0111: $tccp_{0111}$ 1000: $tccp_{1000}$ 1001: $tccp_{1001}$ 1010: $tccp_{1010}$ 1011: $tccp_{1011}$ 1100: $tccp_{1100}$ 1101: $tccp_{1101}$ 1110: $tccp_{1110}$ 1111: $tccp_{1111}$ (default)
10	COPT_2	
9	COPT_1	
8	COPT_0	
7	H_OLTH_HIGH	H-bridge OL high threshold (5/6 * V_S) select
6	OL_H1L2	Test open-load condition between H1 and L2
5	OL_H2L1	Test open-load condition between H2 and L1
4	SLEW_4	Binary coded slew rate of H-bridge (bit0 = LSB; bit4 = MSB) 00000: Control disabled (default) 11111: I_{GHxmax}
3	SLEW_3	
2	SLEW_2	
1	SLEW_1	
0	SLEW_0	

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7.4.11 Control Register CR11 (0x0B)

Table 116. Control Register CR11

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	Reserved										ECV_LS	ECV_OCR	Reserved			ECON	Reserved		EC_5	EC_4	EC_3	EC_2	EC_1	EC_0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
Access	R/W																							

Table 117. CR11 signals description

Bit	Name	Description
23:14	Reserved	—
13	ECV_LS	Control of ECV low-side switch 0: ECV low-side switch off (default) 1: ECV low-side switch on
12	ECV_OCR	Overcurrent recovery for output ECV 0: overcurrent recovery is turned off (default) 1: overcurrent recovery is turned on
11:9	Reserved	—
8	ECON	Electro-chrome Control The electro-chrome control enables the driver at pin ECDR and switches OUT10 directly on ignoring the control bits OUT10_x in CR5 0: Electro-chrome control off (default) 1: Electro-chrome control on
7:6	Reserved	—
5	EC_5	EC Reference Voltage Bits The reference voltage for the electro-chrome voltage controller at pin ECV is binary coded. (bit0 = LSB; bit5 = MSB) 00 0000: V_{ECV} = 0 V xx xxxx: V_{ECV} = V_{CTRLma}x/63 x register value 11 1111: V_{ECV} = $V_{CTRLmax}$ For ECV_HV (Configuration Register) = 0, the maximum EC control voltage is clamped at lower value (see *Section 3.4.20: Electro-chrome mirror driver*)
4	EC_4	
3	EC_3	
2	EC_2	
1	EC_1	
0	EC_0	

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7.4.12 Control Register CR12 (0x0C)

Table 118. Control Register CR12

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	PMW1_FREQ_1	PMW1_FREQ_0	PMW2_FREQ_1	PMW2_FREQ_0	PMW3_FREQ_1	PMW3_FREQ_0	PMW4_FREQ_1	PMW4_FREQ_0	PMW5_FREQ_1	PMW5_FREQ_0	PMW6_FREQ_1	PMW6_FREQ_0	PMW7_FREQ_1	PMW7_FREQ_0	PMW8_FREQ_1	PMW8_FREQ_0	PMW9_FREQ_1	PMW9_FREQ_0	PMW10_FREQ_1	PMW10_FREQ_0	Reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W																							

Table 119. CR12 signals description

Bit	Name	Description
23	PMW1_FREQ_1	Frequency of PWM channel PWM1 00: f_{PWMx}(00) (default) 01: f_{PWMx}(01) 10: f_{PWMx}(10) 11: f_{PWMx}(11)
22	PMW1_FREQ_0	
21	PMW2_FREQ_1	Frequency of PWM channel PWM2 00: f_{PWMx}(00) (default) 01: f_{PWMx}(01) 10: f_{PWMx}(10) 11: f_{PWMx}(11)
20	PMW2_FREQ_0	
19	PMW3_FREQ_1	Frequency of PWM channel PWM3 00: f_{PWMx}(00) (default) 01: f_{PWMx}(01) 10: f_{PWMx}(10) 11: f_{PWMx}(11)
18	PMW3_FREQ_0	
17	PMW4_FREQ_1	Frequency of PWM channel PWM4 00: f_{PWMx}(00) (default) 01: f_{PWMx}(01) 10: f_{PWMx}(10) 11: f_{PWMx}(11)
16	PMW4_FREQ_0	
15	PMW5_FREQ_1	Frequency of PWM channel PWM5 00: f_{PWMx}(00) (default) 01: f_{PWMx}(01) 10: f_{PWMx}(10) 11: f_{PWMx}(11)
14	PMW5_FREQ_0	

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Table 119. CR12 signals description (continued)

Bit	Name	Description
13	PMW6_FREQ_1	Frequency of PWM channel PWM6 00: f_{PWMx}(00) (default) 01: f_{PWMx}(01) 10: f_{PWMx}(10) 11: f_{PWMx}(11)
12	PMW6_FREQ_0	
11	PMW7_FREQ_1	Frequency of PWM channel PWM7 00: f_{PWMx}(00) (default) 01: f_{PWMx}(01) 10: f_{PWMx}(10) 11: f_{PWMx}(11)
10	PMW7_FREQ_0	
9	PMW8_FREQ_1	Frequency of PWM channel PWM8 00: f_{PWMx}(00) (default) 01: f_{PWMx}(01) 10: f_{PWMx}(10) 11: f_{PWMx}(11)
8	PMW8_FREQ_0	
7	PMW9_FREQ_1	Frequency of PWM channel PWM9 00: f_{PWMx}(00) (default) 01: f_{PWMx}(01) 10: f_{PWMx}(10) 11: f_{PWMx}(11)
6	PMW9_FREQ_0	
5	PMW10_FREQ_1	Frequency of PWM channel PWM10 00: f_{PWMx}(00) (default) 01: f_{PWMx}(01) 10: f_{PWMx}(10) 11: f_{PWMx}(11)
4	PMW10_FREQ_0	
3:0	Reserved	—

7.4.13 Control Register CR13 (0x0D) to CR17 (0x11)

Table 120. Control Register CR13 to CR17

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	Reserved		PWMx_DC_9	PWMx_DC_8	PWMx_DC_7	PWMx_DC_6	PWMx_DC_5	PWMx_DC_4	PWMx_DC_3	PWMx_DC_2	PWMx_DC_1	PWMx_DC_0	Reserved		PWMy_DC_9	PWMy_DC_8	PWMy_DC_7	PWMy_DC_6	PWMy_DC_5	PWMy_DC_4	PWMy_DC_3	PWMy_DC_2	PWMy_DC_1	PWMy_DC_0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W																							

Where:

x = 1 + (z * 2), z = 0 to 4

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y = 2 + (z * 2), z = 0 to 4

Table 121. CR13 to CR17 signals description

Bit	Name	Description
23:22	Reserved	—
21	PWMx_DC_9	Binary coded on-dutycycle of PWM channel PWMx (bit12 = LSB; bit21 = MSB) 00 0000 0000: duty cycle 0% (default) xx xxxx xxxx: duty cycle 100%/1023 x register value 11 1111 1111. duty cycle 100%
20	PWMx_DC_8	
19	PWMx_DC_7	
18	PWMx_DC_6	
17	PWMx_DC_5	
16	PWMx_DC_4	
15	PWMx_DC_3	
14	PWMx_DC_2	
13	PWMx_DC_1	
12	PWMx_DC_0	
11:10	Reserved	—
9	PWMy_DC_9	Binary coded on-dutycycle of PWM channel PWMy (bit0 = LSB; bit9 = MSB) 00 0000 0000: duty cycle 0% (default) xx xxxx xxxx: duty cycle 100%/1023 x register value 11 1111 1111. Duty cycle 100% Binary coded on-dutycycle of PWM channel PWMy
8	PWMy_DC_8	
7	PWMy_DC_7	
6	PWMy_DC_6	
5	PWMy_DC_5	
4	PWMy_DC_4	
3	PWMy_DC_3	
2	PWMy_DC_2	
1	PWMy_DC_1	
0	PWMy_DC_0	

7.4.14 Control Register CR18 (0x12) to CR22 (0x16)

Table 122. Control Register CR18

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	Reserved	OUTx_AUTOCOMP_EN	OUTx_VLED_9	OUTx_VLED_8	OUTx_VLED_7	OUTx_VLED_6	OUTx_VLED_5	OUTx_VLED_4	OUTx_VLED_3	OUTx_VLED_2	OUTx_VLED_1	OUTx_VLED_0	Reserved	OUTy_AUTOCOMP_EN	OUTy_VLED_9	OUTy_VLED_8	OUTy_VLED_7	OUTy_VLED_6	OUTy_VLED_5	OUTy_VLED_4	OUTy_VLED_3	OUTy_VLED_2	OUTy_VLED_1	OUTy_VLED_0

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Table 122. Control Register CR18 (continued)

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W																							

Where:

x = 7 + (z * 2), z = 0 to 4

y = 8 + (z * 2), z = 0 to 4

Table 123. CR18 to CR22 signals description

Bit	Name	Description
23	Reserved	—
22	OUTx_AUTOCOMP_EN	Setting this bit to ‘1’ enables the automatic V_S compensation for OUTx
21	OUTx_VLED_9	Binary coded nominal LED voltage of OUTx (bit12 = LSB; bit21 = MSB) 00 0000 0000: V_{LED} = 0 V (default) xx xxxx xxxx: V_{LED} = V_{AINVS} /1023 x register value 01 1101 0000: V_{LED} = V_{AINVS} V_{LED} is clamped at 10 V (0x1D0h)
20	OUTx_VLED_8	
19	OUTx_VLED_7	
18	OUTx_VLED_6	
17	OUTx_VLED_5	
16	OUTx_VLED_4	
15	OUTx_VLED_3	
14	OUTx_VLED_2	
13	OUTx_VLED_1	
12	OUTx_VLED_0	
11	Reserved	—
10	OUTy_AUTOCOMP_EN	Setting this bit to ‘1’ enables the automatic V_S compensation for OUTy
9	OUTy_VLED_9	Binary coded nominal LED voltage of OUTy (bit0 = LSB; bit9 = MSB) 00 0000 0000: V_{LED} = 0 V (default) xx xxxx xxxx: V_{LED} = V_{AINVS} /1023 x register value 01 1101 0000: V_{LED} = V_{AINVS} V_{LED} is clamped at 10 V (0x1D0h)
8	OUTy_VLED_8	
7	OUTy_VLED_7	
6	OUTy_VLED_6	
5	OUTy_VLED_5	
4	OUTy_VLED_4	
3	OUTy_VLED_3	
2	OUTy_VLED_2	
1	OUTy_VLED_1	
0	OUTy_VLED_0	

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7.4.15 Control Register CR23 (0x17)

Table 124. Control Register CR23

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	Reserved						EXT_ID_17	EXT_ID_16	EXT_ID_15	EXT_ID_14	EXT_ID_13	EXT_ID_12	EXT_ID_11	EXT_ID_10	EXT_ID_9	EXT_ID_8	EXT_ID_7	EXT_ID_6	EXT_ID_5	EXT_ID_4	EXT_ID_3	EXT_ID_2	EXT_ID_1	EXT_ID_0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W																							

Table 125. CR23 signals description

Bit	Name	Description
23:18	Reserved	—
17:0	EXT_ID_x	Extended CAN Identifier Definition of Extended CAN Identifier which will cause a wake-up (WUF) To enable wake-up frame detection on Extended CAN Identifier also CAN_IDE (Control Register 24, bit 22) must be set ID Bits are maskable in CR25

7.4.16 Control Register CR24 (0x18)

Table 126. Control Register CR24

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	Reserved	CAN_IDE	BR_1	BR_0	SAMPLE_3	SAMPLE_2	SAMPLE_1	SAMPLE_0	DLC_3	DLC_2	DLC_1	DLC_0	Reserved	ID_10	ID_9	ID_8	ID_7	ID_6	ID_5	ID_4	ID_3	ID_2	ID_1	ID_0
Reset	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W																							

Table 127. CR24 signals description

Bit	Name	Description
23	Reserved	—
22	CAN_IDE	Enable CAN wake-up frame detection on Extended Identifier 0: CAN Identifier matching based on CAN Standard Message Format (default) 1: CAN Identifier Matching based on CAN Extended Message Format

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Table 127. CR24 signals description (continued)

Bit	Name	Description
21	BR_1	Bit Rate for CAN wake-up frame detection 00: 500 kbit/s (default) 01: 250 kbit/s 10: 500 kbit/s 11: 125 kbit/s
20	BR_0	
19	SAMPLE_3	Sample Point for CAN wake-up frame detection 0000: 65.625 % 0001: 67.1875 % 0010: 67.75 % ... 1010: 81.25 % (default) ... 1110: 87.5 % 1111: 89.065 %
18	SAMPLE_2	
17	SAMPLE_1	
16	SAMPLE_0	
15	DLC_3	CAN Data Length Code Defines the amount of Data Bytes used for the CAN wake-up frame detection. Possible values up to 8 Byte according to CAN message format
14	DLC_2	
13	DLC_1	
12	DLC_0	
11	Reserved	—
10	ID_10	CAN Identifier Definition of CAN Identifier which will cause a wake-up (WUF) ID Bits are maskable in CR26
9	ID_9	
8	ID_8	
7	ID_7	
6	ID_6	
5	ID_5	
4	ID_4	
3	ID_3	
2	ID_2	
1	ID_1	
0	ID_0	

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7.4.17 Control Register CR25 (0x19)

Table 128. Control Register CR25

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	Reserved						EXT_ID_MASK_17	EXT_ID_MASK_16	EXT_ID_MASK_15	EXT_ID_MASK_14	EXT_ID_MASK_13	EXT_ID_MASK_12	EXT_ID_MASK_11	EXT_ID_MASK_10	EXT_ID_MASK_9	EXT_ID_MASK_8	EXT_ID_MASK_7	EXT_ID_MASK_6	EXT_ID_MASK_5	EXT_ID_MASK_4	EXT_ID_MASK_3	EXT_ID_MASK_2	EXT_ID_MASK_1	EXT_ID_MASK_0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W																							

Table 129. CR25 signals description

Bit	Name	Description
23:18	Reserved	—
17:0	EXT_ID_MASK_x	Masking Bits for Extended CAN Identifier 0: Extended CAN Identifier Bit will be matched (default) 1: Extended CAN Identifier Bit will be ignored for matching

7.4.18 Control Register CR26 (0x1A)

Table 130. Control Register CR26

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	Reserved													ID_MASK_10	ID_MASK_9	ID_MASK_8	ID_MASK_7	ID_MASK_6	ID_MASK_5	ID_MASK_4	ID_MASK_3	ID_MASK_2	ID_MASK_1	ID_MASK_0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W																							

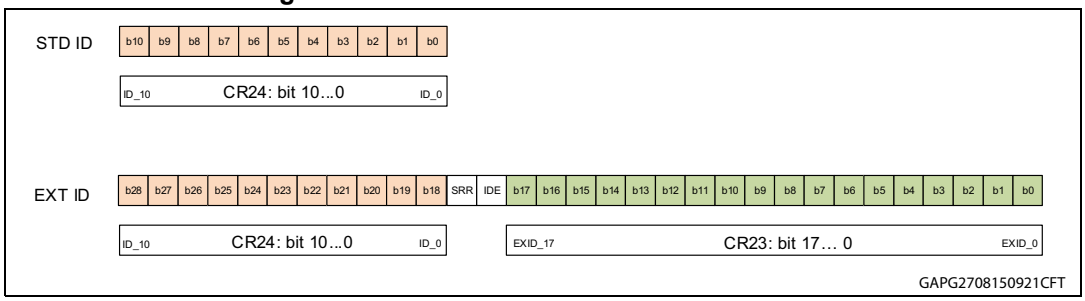
Table 131. CR26 signals description

Bit	Name	Description
23:11	Reserved	—
10:0	ID_MASK_x	Masking Bits Standard CAN Identifier 0: CAN Identifier Bit will be matched (default) 1: CAN Identifier Bit will be ignored for matching

The extended ID and extended ID mask are composed as follows (mask is composed by equivalent bits in CR25 and CR26:

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Figure 61. Extended ID and extended ID mask



7.4.19 Control Register CR27 (0x1B)

Table 132. Control Register CR27

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	DATA_BYTE3_7	DATA_BYTE3_6	DATA_BYTE3_5	DATA_BYTE3_4	DATA_BYTE3_3	DATA_BYTE3_2	DATA_BYTE3_1	DATA_BYTE3_0	DATA_BYTE2_7	DATA_BYTE2_6	DATA_BYTE2_5	DATA_BYTE2_4	DATA_BYTE2_3	DATA_BYTE2_2	DATA_BYTE2_1	DATA_BYTE2_0	DATA_BYTE1_7	DATA_BYTE1_6	DATA_BYTE1_5	DATA_BYTE1_4	DATA_BYTE1_3	DATA_BYTE1_2	DATA_BYTE1_1	DATA_BYTE1_0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W																							

Table 133. CR27 signals description

Bit	Name	Description
23:16	DATA_BYTE3	Data field for data matching
15:8	DATA_BYTE2	
7:0	DATA_BYTE1	

7.4.20 Control Register CR28 (0x1C)

Table 134. Control Register CR28

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	DATA_BYTE6_7	DATA_BYTE6_6	DATA_BYTE6_5	DATA_BYTE6_4	DATA_BYTE6_3	DATA_BYTE6_2	DATA_BYTE6_1	DATA_BYTE6_0	DATA_BYTE5_7	DATA_BYTE5_6	DATA_BYTE5_5	DATA_BYTE5_4	DATA_BYTE5_3	DATA_BYTE5_2	DATA_BYTE5_1	DATA_BYTE5_0	DATA_BYTE4_7	DATA_BYTE4_6	DATA_BYTE4_5	DATA_BYTE4_4	DATA_BYTE4_3	DATA_BYTE4_2	DATA_BYTE4_1	DATA_BYTE4_0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W																							

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Table 135. CR28 signals description

Bit	Name	Description
23:16	DATA_BYTE6	Data field for data matching
15:8	DATA_BYTE5	
7:0	DATA_BYTE4	

7.4.21 Control Register CR29 (0x1D)

Table 136. Control Register CR29

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	Reserved								DATA_BYTE8_7	DATA_BYTE8_6	DATA_BYTE8_5	DATA_BYTE8_4	DATA_BYTE8_3	DATA_BYTE8_2	DATA_BYTE8_1	DATA_BYTE8_0	DATA_BYTE7_7	DATA_BYTE7_6	DATA_BYTE7_5	DATA_BYTE7_4	DATA_BYTE7_3	DATA_BYTE7_2	DATA_BYTE7_1	DATA_BYTE7_0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W																							

Table 137. CR29 signals description

Bit	Name	Description
23:16	Reserved	—
15:8	DATA_BYTE8	Data field for data matching
7:0	DATA_BYTE7	

7.4.22 Control Register CR34 (0x22)

Table 138. Control Register CR34

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	Reserved																					CP_OFF	ICMP	WD_EN
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Access	R/W																							

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Table 139. CR34 signals description

Bit	Name	Description
23:3	Reserved	—
2	CP_OFF	Charge pump control 0: Enabled; charge pump on in active mode (default) 1: Disabled; charge pump off in active mode setting CP_OFF = 1 is only possible when CP_OFF_EN = 1
1	ICMP	V1 load current supervision 0: Enabled; Watchdog is disabled in V1 Standby when $I_{V1} < I_{CMP}$ (default) 1: Disabled; watchdog is disabled upon transition into V1_standby mode setting ICMP = 1 is only possible when ICMP_config_en = 1
0	WD_EN	Watchdog Enable 0: Watchdog disabled 1: Watchdog enabled (default) Writing to this bit is only possible during CAN Flash mode ($V_{TxDL} > V_{flash}$)

7.4.23 Configuration Register (0x3F)

Table 140. Configuration Register

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	WU_CONFIG	LIN_WU_CONFIG	LIN_HS_EN	TSD_CONFIG	ECV_HV	DM	ICMP_CONFIG_EN	WD_CONFIG_EN	MASK_OL_HS1	MASK_OL_LS1	MASK_TW	MASK_EC_OL	MASK_OL	MASK_SPIE	MASK_PLE	MASK_GW	CP_OFF_EN	CP_LOW_CONFIG	CP_DITH_DIS	FS_FORCED	CAN_SUP_5V2_EN	Reserved		TRIG
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Access	R/W																							

Table 141. CR signals description

Bit	Name	Description
23	WU_CONFIG	Configuration of input pin WU Input configured as wake-up input 0: WU configured as wake-up input 1: WU configured for input voltage measurement (default)
22	LIN_WU_CONFIG	Configuration of LIN wake-up behaviour 0: wake up at recessive - dominant - recessive with $t_{dom} > t_{dom_LIN}$ (default) (according to LIN 2.2a and Hardware Requirements for Transceivers version 1.3) 1: wake up at recessive - dominant transition

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Table 141. CR signals description (continued)

Bit	Name	Description
21	LIN_HS_EN	Configuration of LIN transceiver bit rate 0: LIN transceiver in normal communication mode (20kbit/s) (default) 1: LIN transceiver in high speed mode for fast Flashing (115kbit/s)
20	TSD_CONFIG	Configuration of thermal shutdown behaviour 0: in case of TSD1 all power stages are switched off (default) 1: selective shut down of power stage cluster
19	ECV_HV	Configuration of maximum voltage of electrochrome controller (see electrical parameter $V_{CTRLmax}$) 0: maximum electrochrome controller voltage clamped to 1.2V (typ); (default) 1: maximum electrochrome controller voltage set to 1.5V (typ)
18	DM	H-bridge configuration 0: single motor mode (default) 1: dual motor mode
17	ICMP_CONFIG_EN	ICMP configuration Enable 0: writing ICMP = 1 is blocked (writing ICMP=0 is possible); (default) 1: writing ICMP = 1 is possible with next SPI command bit is automatically reset to 0 after next SPI command
16	WD_CONFIG_EN	Watchdog configuration Enable 0: writing to WD Configuration (CR2 [0:1] is blocked (default) 1: writing to WD Configuration Bits is possible with next SPI command bit is automatically reset to 0 after next SPI command
15	MASK_OL_HS1	Mask Open-load HS1 0: Open-load condition at HS1 is not masked (default) 1: Open-load condition at HS1 is masked i.e. it is reported as a Functional Error (GSB bit 3) but not as a Global Error (GSB bit 7)
14	MASK_OL_LS1	Mask Open-load LS1 0: Open-load condition at LS1 is not masked (default) 1: Open-load condition at LS1 is masked i.e. it is reported as a Functional Error (GSB bit 3) but not as a Global Error (GSB bit 7)
13	MASK_TW	Mask Thermal Warning 0: Thermal warning is not masked (default) 1: Thermal warning is masked i.e. it is reported as a Global Warning (GSB bit 1) but not as a Global Error (GSB bit 7)
12	MASK_EC_OL	Mask Electro-chrome Open-load 0: Open-load condition at ECV and OUT10 is not masked (default) 1: Open-load condition at ECV and OUT10 is masked i.e. it is reported as a Functional Error (GSB bit 3) but not as a Global Error (GSB bit 7)

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Table 141. CR signals description (continued)

Bit	Name	Description
11	MASK_OL	Mask open-load 0: Open-load condition at all outputs are not masked (default) 1: Open-load condition at all outputs are masked i.e. it is reported as a Functional Error (GSB bit 3) but not as a Global Error (GSB bit 7)
10	MASK_SPIE	Mask SPI error 0: SPI errors are not masked (default) 1: SPI errors are masked i.e. reported as am SPI Error (GSB bit 5) but not as a Global Error (GSB bit 7)
9	MASK_PLE	Mask physical layer error 0: Physical Layer Errors are not masked (default) 1: Physical Layer Errors are masked i.e. reported as a Physical Layer Error (GSB bit 4) but not as a Global Error (GSB bit 7)
8	MASK_GW	Mask global warning 0: Global Warning conditions are not masked (default) 1: Global Warning conditions are masked i.e. reported as a Global Warning (GSB bit 1) but not as a Global Error (GSB bit 7)
7	CP_OFF_EN	Charge pump control enable 0: writing CP_OFF = 1 is blocked (writing CP OFF = 0 is possible); (default) 1: writing CP_OFF = 1 is possible with next SPI command Bit is automatically reset to 0 after next SPI command
6	CP_LOW_CONFIG	Charge pump low configuration 0: CP_low (SR 2, bit 9) is latched and outputs are off until R&C; (default) 1: CP_low (SR 2, bit 9) is a ‘live’ bit; outputs are re-activated automatically upon recovery of the charge pump output voltage
5	CP_DITH_DIS	Charge pump clock dithering 0: CP clock dithering is enabled; (default) 1: CP clock dithering is disabled
4	FS_FORCED	Force LSx_FSO ON LSx_FSO low-side outputs are forced ON (to allow diagnosis of the fail-safe path) 0: LSx_FSO outputs are controlled by the Fail-safe logic (default) 1: LSx_FSO outputs are forced ON and the device enters Fail-Safe mode; no NReset is generated
3	CAN_SUP_5V2_EN	CAN supplied by V2 enable (to allow CAN Partial Networking in V1stdby) 0: CAN supplied by V1; (default) 1: CAN supplied by V2; in this case the configuration CR1<5:4> = 11 is ignored
2:1	Reserved	—
0	TRIG	Watchdog Trigger bit

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7.5 Status Registers

7.5.1 Status Register SR1 (0x31)

Table 142. Status Register SR1 (0x31)

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	Reserved	WU_STATE	Reserved	WU_WAKE	WAKE_CAN	WAKE_LIN	WAKE_TIMER	DEBUG_ACTIVE	V1UV	V1_RESTART_2	V1_RESTART_1	V1_RESTART_0	WDFAIL_CNT_3	WDFAIL_CNT_2	WDFAIL_CNT_1	WDFAIL_CNT_0	DEVICE_STATE_1	DEVICE_STATE_0	TSD2	TSD1	FORCED_SLEEP_TSD2/V1SC	FORCED_SLEEP_WD	WDFAIL	VPOR
Access	R/C	R	R/C							R							R/C							

Table 143. SR1 signals description

Bit	Name	Description
23	Reserved	—
22	WU_STATE	State of WU input 0: input level is low 1: input level is high The bit shows the momentary status of WU and cannot be cleared (“Live bit”) Note: The status is only valid if WU is configured as wake-up input in Configuration Register (0x3F). Otherwise this bit is read at its previous logic state
21	Reserved	—
20	WU_WAKE	Wake-up by WU: shows wake up source 1: wake-up Bits are latched until a “Read and clear” command
19	WAKE_CAN	Wake-up by CAN: shows wake up source 1: wake-up Bits are latched until a “Read and clear” command
18	WAKE_LIN	Wake-up by LIN: shows wake up source 1: wake-up Bits are latched until a “Read and clear” command
17	WAKE_TIMER	Wake-up by Timer: shows wake up source 1: wake-up Bits are latched until a “Read and clear” command

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Table 143. SR1 signals description (continued)

Bit	Name	Description
16	DEBUG_ACTIVE	Debug Mode Active: indicates Device is in Debug mode 1: Debug mode The bit shows the momentary status and cannot be cleared (“Live bit”)
15	V1UV	Indicates undervoltage condition at voltage regulator V1 (V1 < V_{RTx}) 1: undervoltage Bit is latched until a “Read and clear” command
14	V1_RESTART_2	Indicates the number of TSD2 events which caused a restart of voltage regulator V1 Bits cannot be cleared; counter will be cleared automatically if no additional TSD2 event occurs within 1 minute.
13	V1_RESTART_1	
12	V1_RESTART_0	
11	WDFAIL_CNT_3	Indicates number of subsequent watchdog failures. Bits cannot be cleared; will be cleared with a valid watchdog trigger
10	WDFAIL_CNT_2	
9	WDFAIL_CNT_1	
8	WDFAIL CNT_0	
7	DEVICE_STATE_1	State from which the device woke up 00: Active mode, after Read&Clear command or after Flash mode state 01: Active mode after wake-up from V1_standby mode (before Read&Clear command) 10: in Active mode after Power-on or after wake-up from Vbat_standby mode (before Read&Clear command) 11: Flash mode (LIN Flash or CAN Flash mode) Bit is latched until a “Read and clear” command After a “read and clear access”, the device state will be updated
6	DEVICE_STATE_0	
5	TSD2	Thermal Shutdown 2 was reached Bit is latched until a "Read and clear" command
4	TSD1	Thermal Shutdown 1 was reached (Logical Or combination of all TSD1_CLx; see status register SR6). This bit cannot be cleared directly. It is reset if the corresponding TSD1_CLx bits in SR6 are cleared.
3	FORCED_SLEEP_ TSD2/V1SC	Device entered Forced Vbat_standby mode due to: – Thermal shutdown or – Short circuit on V1 during startup Bit is latched until a "Read and clear" command
2	FORCED_SLEEP_WD	Device entered Forced Vbat_standby mode due to multiple watchdog failures Bit is latched until a "Read and clear" command
1	WDFAIL	Watchdog failure Bit is latched until a "Read and clear" command
0	VPOR	V_S Power-on Reset threshold (VPOR) reached Bit is latched until a "Read and clear" command

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7.5.2 Status Register SR2 (0x32)

Table 144. Status Register SR2 (0x32)

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	LIN_PERM_DOM	LIN_TXD_DOM	LIN_PERM_REC	CAN_RXD_REC	CAN_PERM_REC	CAN_PERM_DOM	CAN_TXD_DOM	CAN_SUP_LOW	DSMON_HS2	DSMON_HS1	DSMON_LS2	DSMON_LS1	SPI_INV_CMD	SPI_SCK_CNT	CP_LOW	TW	V2SC	V2FAIL	V1FAIL	VSREG_EW	VSREG_OV	VSREG_UV	VS_OV	VS_UV
Access	R/C													R	R/C									

Table 145. SR2 signals description

Bit	Name	Description
23	LIN_PERM_DOM	LIN bus signal is dominant for t > $t_{dom(bus)}$ Bit is latched until a “Read and clear” command
22	LIN_TXD_DOM	TxDL pin is dominant for t > $t_{dom(TXDL)}$ The LIN transmitter is disabled until the bit is cleared Bit is latched until a “Read and clear” command
21	LIN_PERM_REC	LIN bus signal does not follow TxDL within t_{LIN} The LIN transmitter is disabled until the bit is cleared Bit is latched until a “Read and clear” command
20	CAN_RXD_REC	RxDC has not followed TxDC for 4 times The CAN transmitter is disabled until the bit is cleared Bit is latched until a “Read and clear” command
19	CAN_PERM_REC	CAN bus signal did not follow TxDC for 4 times The CAN transmitter is disabled until the bit is cleared Bit is latched until a “Read and clear” command
18	CAN_PERM_DOM	CAN bus signal is dominant for t > t_{CAN} Bit is latched until a “Read and clear” command
17	CAN_TXD_DOM	TxDC pin is dominant for t > $t_{dom(TXDC)}$ The CAN transmitter is disabled until the bit is cleared Bit is latched until a “Read and clear” command
16	CAN_SUP_LOW	Voltage at CAN supply pin reached the CAN supply low warning threshold V_{CANSUP} < $V_{CANSUPlow}$ Bit is latched until a “Read and clear” command
15	DSMON_HS2	Drain-Source Monitoring ‘1’ indicates a short-circuit or open-load condition was detected Bit is latched until a “Read and clear” command
14	DSMON_HS1	
13	DSMON_LS2	
12	DSMON_LS1	

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Table 145. SR2 signals description (continued)

Bit	Name	Description
11	SPI_INV_CMD	Invalid SPI command ‘1’ indicates one of the following conditions was detected: – access to undefined address – Write operation to Status Register – DI stuck at '0' or '1' – CSN timeout – Parity failure – invalid or undefined setting The SPI frame is ignored Bit is latched until a “Read and clear” command
10	SPI_SCK_CNT	SPI clock counter ‘1’ indicates an SPI frame with wrong number of CLK cycles was detected Bit is latched until a valid SPI frame
9	CP_LOW	Charge pump voltage low ‘1’ indicates that the charge pump voltage is too low Bit is latched until a “Read and clear” command
8	TW	Thermal warning ‘1’ indicates the temperature has reached the thermal warning threshold (logical OR combination of bits TW_CLx in SR6) Bit is latched until a “Read and clear” command
7	V2SC	V2 short circuit detection ‘1’ indicates a short circuit to GND condition of V2 at turn-on of the regulator (V2 < V2_fail for t > t_{v2_short}) Bit is latched until a “Read and clear” command
6	V2FAIL	V2 failure detection ‘1’ indicates a V2 fail event occurred since last readout (V2 < V2_fail for t > t_{v2_fail}) Bit is latched until a “Read and clear” command
5	V1FAIL	V1 failure detection ‘1’ indicates a V1 fail event occurred since last readout (V1 < V1_fail for t > t_{v1_fail}) Bit is latched until a “Read and clear” command
4	VSREG_EW	V_{SREG} early warning ‘1’ indicates the voltage at V_{SREG} has reached the early warning threshold (configured in CR3) In Active mode, an interrupt pulse is generated at NINT Bit is latched until a “Read and clear” command. Bit needs a "Read and clear" command after wake-up from standby modes
3	VSREG_OV	V_{SREG} overvoltage ‘1’ indicates the voltage at V_{SREG} has reached the overvoltage threshold Bit is latched until a “Read and clear” command

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Table 145. SR2 signals description (continued)

Bit	Name	Description
2	VSREG_UV	V_{SREG} undervoltage '1' indicates the voltage at V_{SREG} has reached the undervoltage threshold Bit is latched until a "Read and clear" command
1	VS_OV	V_S overvoltage '1' indicates the voltage at V_S has reached the overvoltage threshold Bit is latched until a "Read and clear" command
0	VS_UV	V_S undervoltage '1' indicates the voltage at V_S has reached the undervoltage threshold Bit is latched until a "Read and clear" command

7.5.3 Status Register SR3 (0x33)

Table 146. Status Register SR3 (0x33)

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	OUT1_HS_OC_TH_EX	OUT1_LS_OC_TH_EX	OUT2_HS_OC_TH_EX	OUT2_LS_OC_TH_EX	OUT3_HS_OC_TH_EX	OUT3_LS_OC_TH_EX	OUT4_HS_OC_TH_EX	OUT4_LS_OC_TH_EX	OUT5_HS_OC_TH_EX	OUT5_LS_OC_TH_EX	OUT6_HS_OC_TH_EX	OUT6_LS_OC_TH_EX	OUT7_OC_TH_EX	OUT8_OC_TH_EX	OUT9_OC	OUT10_OC	OUT11_OC	OUT12_OC	OUT13_OC	OUT14_OC	OUT15_OC	OUTHS_OC_TH_EX	LS2FSO_OC	LS1FSO_OC
Access	R/C																							

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Table 147. SR3 signals description

Bit	Name	Description
23	OUT1_HS_OC_TH_EX	Overcurrent shutdown '1' indicates the output was shut down due to overcurrent condition. If Overcurrent Recovery is disabled (CR7: OUTx_OCR = 0): Bit is set upon overcurrent condition and output is turned off. If Overcurrent Recovery is enabled (CR7: OUTx_OCR = 1): In case of overcurrent condition this bit is not set. The output goes into Overcurrent Recovery mode and OUTx_OCR_alert in SR4 is set to '1' In case of Thermal Expiration enabled (CR8: OUTx_OCR_THx_en = 1): Bit is set after thermal expiration and output is turned off Bit is latched until a "Read and clear" command
22	OUT1_LS_OC_TH_EX	
21	OUT2_HS_OC_TH_EX	
20	OUT2_LS_OC_TH_EX	
19	OUT3_HS_OC_TH_EX	
18	OUT3_LS_OC_TH_EX	
17	OUT4_HS_OC_TH_EX	
16	OUT4_LS_OC_TH_EX	
15	OUT5_HS_OC_TH_EX	
14	OUT5_LS_OC_TH_EX	
13	OUT6_HS_OC_TH_EX	
12	OUT6_LS_OC_TH_EX	
11	OUT7_OC_TH_EX	
10	OUT8_OC_TH_EX	
9	OUT9_OC	Overcurrent shutdown '1' indicates the output was shut down due to overcurrent condition. Bit is latched until a "Read and clear" command
8	OUT10_OC	
7	OUT11_OC	
6	OUT12_OC	
5	OUT13_OC	
4	OUT14_OC	
3	OUT15_OC	
2	OUTHS_OC_TH_EX	Overcurrent shutdown '1' indicates the output was shut down due to overcurrent condition. If Overcurrent Recovery is disabled (CR7: OUTx_OCR = 0): Bit is set upon overcurrent condition and output is turned off. If Overcurrent Recovery is enabled (CR7: OUTx_OCR = 1): In case of overcurrent condition this bit is not set. The output goes into Overcurrent Recovery mode and OUTx_OCR_alert in SR4 is set to '1' In case of Thermal Expiration enabled (CR8: OUTx_OCR_THx_en = 1): Bit is set after thermal expiration and output is turned off Bit is latched until a "Read and clear" command
1	LS2FSO_OC	Overcurrent shutdown '1' indicates the output was shut down due to overcurrent condition. Bit is latched until a "Read and clear" command
0	LS1FSO_OC	

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7.5.4 Status Register SR4 (0x34)

Table 148. Status Register SR4 (0x34)

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	OUT1_HS_OCR_ALERT	OUT1_LS_OCR_ALERT	OUT2_HS_OCR_ALERT	OUT2_LS_OCR_ALERT	OUT3_HS_OCR_ALERT	OUT3_LS_OCR_ALERT	OUT4_HS_OCR_ALERT	OUT4_LS_OCR_ALERT	OUT5_HS_OCR_ALERT	OUT5_LS_OCR_ALERT	OUT6_HS_OCR_ALERT	OUT6_LS_OCR_ALERT	OUT7_OCR_ALERT	OUT8_OCR_ALERT	Reserved							OUTHS_OCR_ALERT	DSMON_HEAT	ECV_OC
Access	R														R/C							R	R/C	

Table 149. SR4 signals description

Bit	Name	Description
23	OUT1_HS_OCR_ALERT	Autorecovery Alert '1' indicates that the output reached the overcurrent threshold and is in autorecovery mode Bit is not latched and cannot be cleared.
22	OUT1_LS_OCR_ALERT	
21	OUT2_HS_OCR_ALERT	
20	OUT2_LS_OCR_ALERT	
19	OUT3_HS_OCR_ALERT	
18	OUT3_LS_OCR_ALERT	
17	OUT4_HS_OCR_ALERT	
16	OUT4_LS_OCR_ALERT	
15	OUT5_HS_OCR_ALERT	
14	OUT5_LS_OCR_ALERT	
13	OUT6_HS_OCR_ALERT	
12	OUT6_LS_OCR_ALERT	
11	OUT7_OCR_ALERT	
10	OUT8_OCR_ALERT	
9:3	Reserved	—
2	OUTHS_OCR_ALERT	Autorecovery Alert '1' indicates that the output reached the overcurrent threshold and is in autorecovery mode Bit is not latched and cannot be cleared.

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Table 149. SR4 signals description (continued)

Bit	Name	Description
1	DSMON_HEAT	Drain-Source Monitoring Heater output '1' indicates a short-circuit condition was detected Bit is latched until a "Read and clear" command
0	ECV_OC	Overcurrent shutdown '1' indicates the output was shut down due to overcurrent condition. Bit is latched until a "Read and clear" command

7.5.5 Status Register SR5 (0x35)

Table 150. Status Register SR5 (0x35)

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	OUT1_HS_OL	OUT1_LS_OL	OUT2_HS_OL	OUT2_LS_OL	OUT3_HS_OL	OUT3_LS_OL	OUT4_HS_OL	OUT4_LS_OL	OUT5_HS_OL	OUT5_LS_OL	OUT6_HS_OL	OUT6_LS_OL	OUT7_OL	OUT8_OL	OUT9_OL	OUT10_OL	OUT11_OL	OUT12_OL	OUT13_OL	OUT14_OL	OUT15_OL	OUTHS_OL	GH_OL	ECV_OL
Access	R/C																							

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Table 151. SR5 signals description

Bit	Name	Description
23	OUT1_HS_OL	Open-load '1' indicates an open-load condition was detected at the output Bit is latched until a "Read and clear" command
22	OUT1_LS_OL	
21	OUT2_HS_OL	
20	OUT2_LS_OL	
19	OUT3_HS_OL	
18	OUT3_LS_OL	
17	OUT4_HS_OL	
16	OUT4_LS_OL	
15	OUT5_HS_OL	
14	OUT5_LS_OL	
13	OUT6_HS_OL	
12	OUT6_LS_OL	
11	OUT7_OL	
10	OUT8_OL	
9	OUT9_OL	
8	OUT10_OL	
7	OUT11_OL	
6	OUT12_OL	
5	OUT13_OL	
4	OUT14_OL	
3	OUT15_OL	
2	OUTHS_OL	
1	GH_OL	
0	ECV_OL	

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7.5.6 Status Register SR6 (0x36)

Table 152. Status Register SR6 (0x36)

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	WD_TIMER_STATE_1	WD_TIMER_STATE_0	Reserved				ECV_VNR	ECV_VHI	Reserved		TW_CL6	TW_CL5	TW_CL4	TW_CL3	TW_CL2	TW_CL1	Reserved		TSD1_CL6	TSD1_CL5	TSD1_CL4	TSD1_CL3	TSD1_CL2	TSD1_CL1
Access	R		R/C				R		R/C															

Table 153. SR6 signals description

Bit	Name	Description
23	WD_TIMER_STATE_1	Watchdog timer status 00: 0 - 33% 01: 33 - 66% 11: 66 - 100%
22	WD_TIMER_STATE_0	
21:18	Reserved	—
17	ECV_VNR	Electrochrome voltage not reached: electrochrome voltage status '1' indicates the electrochrome voltage is not reached Bit is not latched
16	ECV_VHI	Electrochrome voltage high: electrochrome voltage status '1' indicates the electrochrome voltage is not reached Bit is not latched
15:14	Resrved	—
13	TW_CL6	Thermal warning for Cluster x ‘1’ indicates Cluster x has reached the thermal warning threshold Bit is latched until a “Read and clear” command
12	TW_CL5	
11	TW_CL4	
10	TW_CL3	
9	TW_CL2	
8	TW_CL1	
7:6	Reserved	—

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Table 153. SR6 signals description (continued)

Bit	Name	Description
5	TSD1_CL6	Thermal shutdown of Cluster x '1' indicates Cluster x has reached the thermal shutdown threshold (TSD1) and the output cluster was shut down Bit is latched until a "Read and clear" command
4	TSD1_CL5	
3	TSD1_CL4	
2	TSD1_CL3	
1	TSD1_CL2	
0	TSD1_CL1	

7.5.7 Status Register SR7 (0x37) to SR9 (0x39)

Table 154. Status Register SR7 (0x37) to SR9 (0x39)

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	Reserved		TEMP_CLx_9	TEMP_CLx_8	TEMP_CLx_7	TEMP_CLx_6	TEMP_CLx_5	TEMP_CLx_4	TEMP_CLx_3	TEMP_CLx_2	TEMP_CLx_1	TEMP_CLx_0	Reserved		TEMP_CLy_9	TEMP_CLy_8	TEMP_CLy_7	TEMP_CLy_6	TEMP_CLy_5	TEMP_CLy_4	TEMP_CLy_3	TEMP_CLy_2	TEMP_CLy_1	TEMP_CLy_0
Access	R/C		R										R/C		R									

Where:

x = 2 + (z * 2), z = 0 to 2

y = 1 + (z * 2), z = 0 to 2

Table 155. SR7 to SR9 signals description

Bit	Name	Description
23:22	Reserved	—
21	TEMP_CLx_9	Temperature Cluster x: Binary coded voltage of temperature diode for cluster x (bit12 = LSB; bit21 = MSB) (see *Section 4.34: Thermal clusters*) Bits cannot be cleared.
20	TEMP_CLx_8	
19	TEMP_CLx_7	
18	TEMP_CLx_6	
17	TEMP_CLx_5	
16	TEMP_CLx_4	
15	TEMP_CLx_3	
14	TEMP_CLx_2	
13	TEMP_CLx_1	
12	TEMP_CLx_0	
11:10	Reserved	—

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Table 155. SR7 to SR9 signals description (continued)

Bit	Name	Description
9	TEMP_CLy_9	Temperature Cluster y: binary coded voltage of temperature diode for cluster y (bit0 = LSB; bit9 = MSB) (see *Section 4.34: Thermal clusters*) Bits cannot be cleared.
8	TEMP_CLy_8	
7	TEMP_CLy_7	
6	TEMP_CLy_6	
5	TEMP_CLy_5	
4	TEMP_CLy_4	
3	TEMP_CLy_3	
2	TEMP_CLy_2	
1	TEMP_CLy_1	
0	TEMP_CLy_0	

7.5.8 Status Register SR10 (0x3A)

Table 156. Status Register SR10 (0x3A)

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	Reserved		VSREG_9	VSREG_8	VSREG_7	VSREG_6	VSREG_5	VSREG_4	VSREG_3	VSREG_2	VSREG_1	VSREG_0	Reserved											
Access	R/C		R										R/C											

Table 157. SR10 signals description

Bit	Name	Description
23:22	Reserved	—
21	VSREG_9	Binary coded voltage at V_{SREG} pin (bit12 = LSB; bit21 = MSB) 00 0000 0000: 0V xx xxxx xxxx: V_{AINVS}/1023 x register value 11 1111 1111: V_{AINVS} Bits cannot be cleared.
20	VSREG_8	
19	VSREG_7	
18	VSREG_6	
17	VSREG_5	
16	VSREG_4	
15	VSREG_3	
14	VSREG_2	
13	VSREG_1	
12	VSREG_0	
11:0	Reserved	—

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7.5.9 Status Register SR11 (0x3B)

Table 158. Status Register SR11 (0x3B)

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	Reserved		VS_9	VS_8	VS_7	VS_6	VS_5	VS_4	VS_3	VS_2	VS_1	VS_0	Reserved		VWU_9	VWU_8	VWU_7	VWU_6	VWU_5	VWU_4	VWU_3	VWU_2	VWU_1	VWU_0
Access	R/C		R										R/C		R									

Table 159. SR11 signals description

Bit	Name	Description
23	Reserved	—
21	VS_9	Binary coded voltage at V_S pin (bit12 = LSB; bit21 = MSB) 00 0000 0000: 0V xx xxxx xxxx: V_{AINVS}/1023 x register value 11 1111 1111: V_{AINVS} Bits cannot be cleared.
20	VS_8	
19	VS_7	
18	VS_6	
17	VS_5	
16	VS_4	
15	VS_3	
14	VS_2	
13	VS_1	
12	VS_0	
11:10	Reserved	—
9	VWU_9	Binary coded voltage at WU pin (bit0 = LSB; bit9 = MSB) 00 0000 0000: 0V xx xxxx xxxx: V_{AINVS}/1023 x register value 11 1111 1111: V_{AINVS} Bits cannot be cleared.
8	VWU_8	
7	VWU_7	
6	VWU_6	
5	VWU_5	
4	VWU_4	
3	VWU_3	
2	VWU_2	
1	VWU_1	
0	VWU_0	

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7.5.10 Status Register SR12 (0x3C)

Table 160. Status Register SR12 (0x3B)

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	Reserved			FECNT_4	FECNT_3	FECNT_2	FECNT_1	FECNT_0	Reserved	SWRD_CR29	SWRD_CR28	SWRD_CR27	SWRD_CR26	SWRD_CR25	SWRD_CR24	SWRD_CR23	SYSERR	OSC_FAIL	CAN_SILENT	TX_SYNC	CANTO	WUP	WUF	FDERR
Access	R/C		R										R/C		R									

Table 161. SR12 signals description

Bit	Name	Description
23:21	Reserved	—
20	FECNT_4	CAN Frame Detect Error Counter This counter is increased by 1 in case a frame was not received/decoded correctly (CRC error, stuff-bit error, form error). The counter is decreased by 1 with every frame which is decoded correctly If FECNT = 31, the next erroneous frame will wake-up the device, set FDERR = 1 and reset FECNTx = 0 'Live' Bit Updated after each sent CAN Frame
19	FECNT_3	
18	FECNT_2	
17	FECNT_1	
16	FECNT_0	
15	Reserved	—
14	SWRD_CR29	Status flag for Read operation to Selective Wakeup relevant Registers 0: Read not done 1: Read done All bits must be '1' in order to allow activation of selective wake-up (set SWEN = 1) Bits are automatically cleared if the configuration of the respective Control Register is modified
13	SWRD_CR28	
12	SWRD_CR27	
11	SWRD_CR26	
10	SWRD_CR25	
9	SWRD_CR24	
8	SWRD_CR23	
7	SYSERR	CAN System Error Bit is a logical OR combination of: NOT(SWRD_x) OR OSC_Fail OR FD_ERR If SWRD_x are all 1, OSC_Fail is 0 and FD_ERR is 0, this bit is 0, otherwise this bit is 1. The selective wake feature cannot be enabled (SW_EN = 1) if SYS_ERR = 1 In case of a SYS_ERR the selective wake-up feature is disabled (SW_EN = 0) Live bit; will be updated upon change of SWRD_x, OSC_Fail and FD_ERR
6	OSC_FAIL	CAN selective wake oscillator failure OSC Failure Flag (used device internally) Bit is latched until a read and clear access

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Table 161. SR12 signals description (continued)

Bit	Name	Description
5	CAN_SILENT	Online monitoring bit to see if there is silence on the bus for longer than $t_{Silence}$ This flag shows the actual status of the CAN bus (activity/silence). A microcontroller in Stop mode may check this flag priodically
4	TX_SYNC	Status flag for synchronous reference oscillator of the CAN transceiver. Indicates that the last received frame was decoded correctly 0: Not synchronous 1: Synchronous 'Live' Bit Updated after each sent CAN Frame
3	CANTO	CAN communication timeout Bit is set if there is no communication on the bus for t > $t_{Silence}$ CANTO indicates that there was a transition from TRX BIAS to TRX Sleep Bit is latched until a read and clear access
2	WUP	Wake up flag for Wake up Pattern Bit is latched until a read and clear access
1	WUF	Wake up flag for Wake up Frame Bit is latched until a read and clear access
0	FDERR	Frame Detect Error This bit is set at overflow of the Frame Error Counter (FECNT) in SR12 In case of a Frame Detect Error, the device will wake up from TRX BIAS mode Bit is latched until a read and clear access

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8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

8.1 LQFP-64 package information

Figure 62. LQFP-64 package dimension

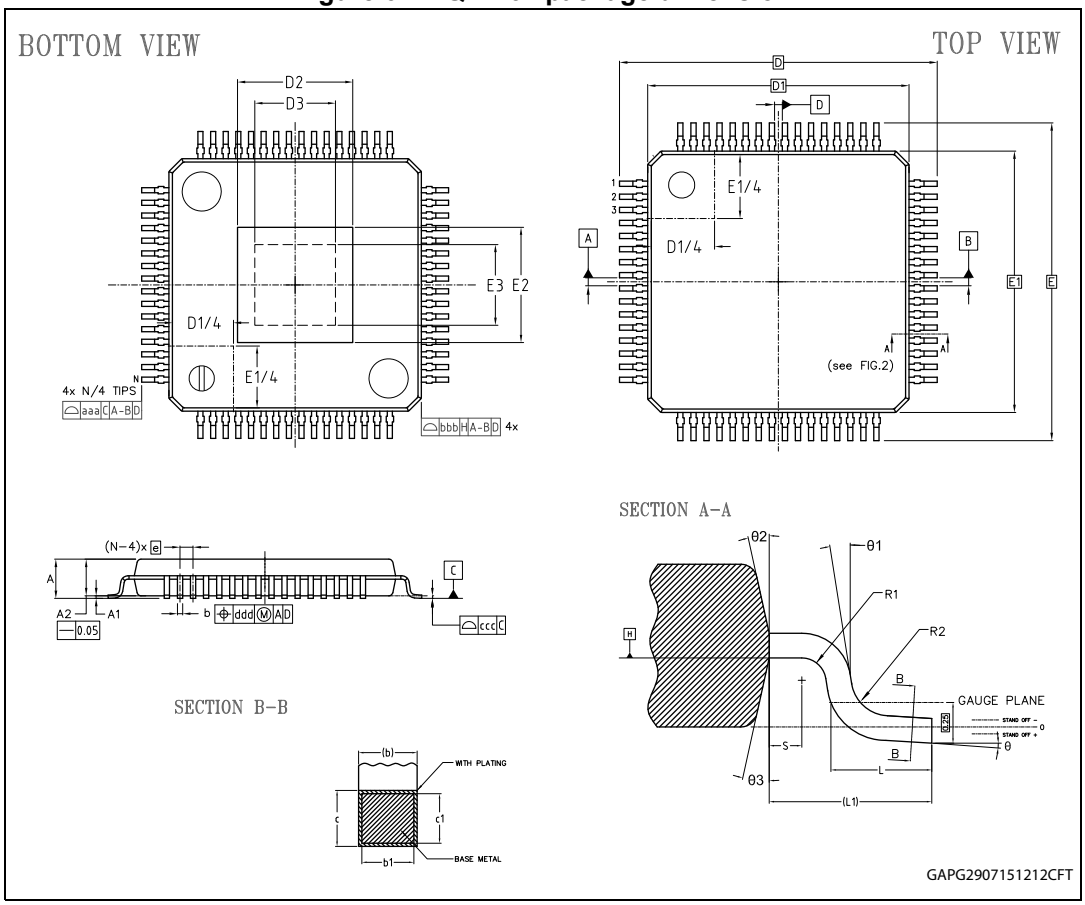


Table 162. LQFP-64 mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
Θ	0°	3.5°	6°
Θ1	0°	9°	12°
Θ2	11°	12°	13°
Θ3	11°	12°	13°

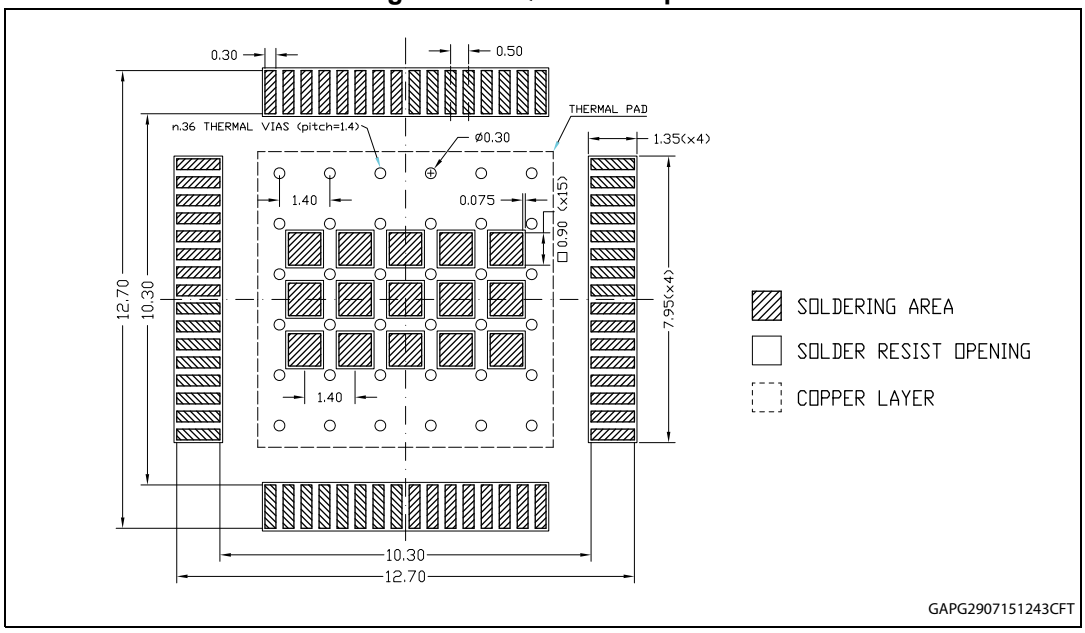
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Table 162. LQFP-64 mechanical data (continued)

Symbol	Millimeters		
	Min.	Typ.	Max.
A			1.60
A1	0.05		0.15
A2	1.35	1.40	1.45
b			0.27
b1	0.17	0.20	0.23
c	0.09		0.20
c1	0.09	0.127	0.16
D	12.00 BSC		
D1	10.00 BSC		
D2			6.85
D3	5.7		
e	0.50 BSC		
E	12.00 BSC		
E1	10.00 BSC		
E2			4.79
E3	3.3		
L	0.45	0.60	0.75
L1	1.00		
N	64		
R1	0.08		
R2	0.08		0.20
S	0.20		
Tolerance of form and position			
aaa	0.20		
bbb	0.20		
ccc	0.08		
ddd	0.08		

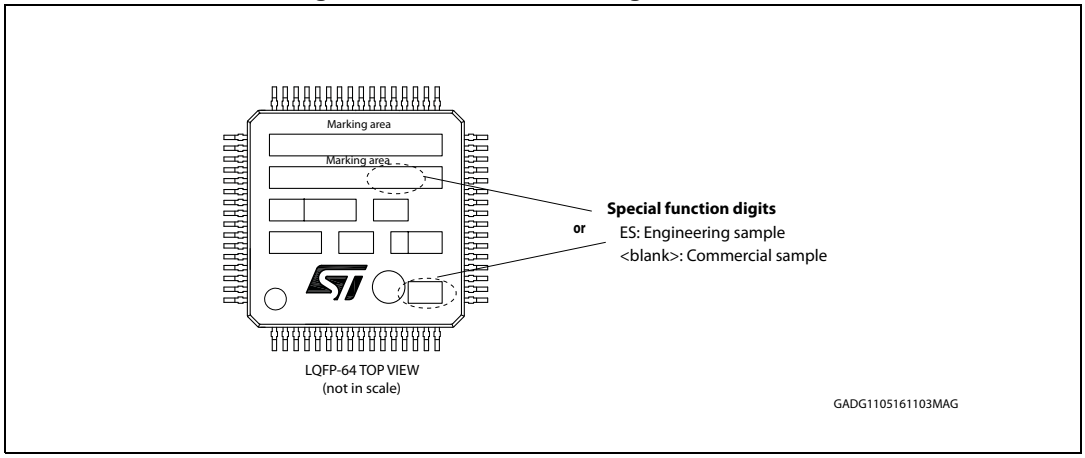
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Figure 63. LQFP-64 footprint



8.2 LQFP-64 marking information

Figure 64. LQFP-64 marking information



Parts marked as ES are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted to run a qualification activity prior to any decision to use these engineering samples.

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9 Revision history

Table 163. Document revision history

Date	Revision	Changes
16-Mar-2016	1	Initial release.
01-Sep-2016	2	Updated *Table 3: Absolute maximum ratings*; Updated *Table 12: Reset output*; Updated *Table 15: Charge pump electrical characteristics*; Updated *Table 17: Power outputs switching times*; Updated *Table 18: Current monitoring*; Updated *Table 20: H-bridge driver*; Updated *Section 4.7.2: Non-recoverable failures – forced Vbat_standby mode*; Updated *Table 115: CR10 signals description*; Updated *Table 143: SR1 signals description*; Added *Section 8.2: LQFP-64 marking information*
12-Sep-2016	3	Updated *Table 4: ESD protection*.
29-Sep-2016	4	Added AEC Q100 compliant qualified Updated *Section 8.2: LQFP-64 marking information*
11-Mar-2019	5	Moved “Device summary” table in cover page. Added the "Sustainable Technology" logo to the datasheet in cover page.

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