Rev. 1.2.1, Nov. 2019

KLMDG4UCTB-B041

Samsung eMMC Product Family

eMMC 5.1 Specification Compatibility

datasheet

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Revision History

Revision No.	History	Draft Date	Remark	Editor
1.0	1. Customer Sample	Oct. 10th, 2018	Final	TE.Kim
1.0.1	1. Package Dimension modification	Oct. 18th, 2018	Final	TE.Kim
1.1	1. Added PKG Ball map 2. Revised some typos	Oct. 24th, 2018	Final	TE.Kim
1.2	1. CSD register value modification 2. Revised some typos	Aug. 26th,2019	Final	TE.Kim
1.2.1	1. Revised some typos	Nov. 22th,2019	Final	TE.Kim

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1.0 PRODUCT LIST

1.1 General Description

SAMSUNG eMMC is an embedded MMC solution designed in a BGA package form. eMMC operation is identical to a MMC device and therefore is a simple read and write to memory using MMC protocol v5.1 which is a industry standard.

eMMC consists of NAND flash and a MMC controller. 3V supply voltage is required for the NAND area (V_{CC}) whereas 1.8V or 3V dual supply voltage (V_{CCQ}) is supported for the MMC controller. SAMSUNG eMMC supports HS400 in order to improve sequential bandwidth, especially sequential read performance.

There are several advantages of using eMMC. It is easy to use as the MMC interface allows easy integration with any microprocessor with MMC host. Any revision or amendment of NAND is invisible to the host as the embedded MMC controller insulates NAND technology from the host. This leads to faster product development as well as faster times to market.

The embedded flash management software or FTL(Flash Transition Layer) of eMMC manages Wear Leveling, Bad Block Management and ECC. The FTL supports all features of the Samsung NAND flash and achieves optimal performance.

1.2 Product Line-Up

[Table 1] Product Line-Up

Product	Part ID	User Density (%)	Package Size	Ball Configuration
128 GB	KLMDG4UCTB-B041	91.0	11.5mmx13mmx1.0mm	153FBGA

1.3 General Features

- embedded MultiMediaCard Ver. 5.1 compatible.
- SAMSUNG eMMC supports features of eMMC5.1 which are defined in JEDEC Standard.
  - Major Supported Features : HS400, Field Firmware Update, Cache, Command Queuing, Enhanced Strobe Mode, Secure Write Protection, Partition types.
  - Non-supported Features : Large Sector Size (4KB).
- Backward compatibility with previous MultiMediaCard system specification (1bit data bus, multi-eMMC systems).
- Data bus width : 1bit (Default), 4bit and 8bit.
- MMC I/F Clock Frequency : 0 ~ 200MHz
  MMC I/F Boot Frequency : 0 ~ 52MHz
- Temperature : Operation (-25°C ~ 85°C), Storage without operation (-40°C ~ 85°C)
- Power : Interface power → V_{CCQ} (1.70V ~ 1.95V), Memory power → V_{CC} (2.7V ~ 3.6V)

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2.0 PRODUCT SPECIFICATION

2.1 Mechanical Specification

2.1.1 Ball Assignment

[Table 2] 153 Ball Information

Pin NO	Name
A3	DAT0
A4	DAT1
A5	DAT2
B2	DAT3
B3	DAT4
B4	DAT5
B5	DAT6
B6	DAT7
K5	RSTN
C6	V_{CCQ}
M4	V_{CCQ}
N4	V_{CCQ}
P3	V_{CCQ}
P5	V_{CCQ}
E6	V_{CC}
F5	V_{CC}
J10	V_{CC}
K9	V_{CC}
C2	VDDi
M5	CMD
H5	Data Strobe
M6	CLK
J5	V_{SS}
A6	V_{SS}
C4	V_{SS}
E7	V_{SS}
G5	V_{SS}
H10	V_{SS}
K8	V_{SS}
N2	V_{SS}
N5	V_{SS}
P4	V_{SS}
P6	V_{SS}

Ball-side down view

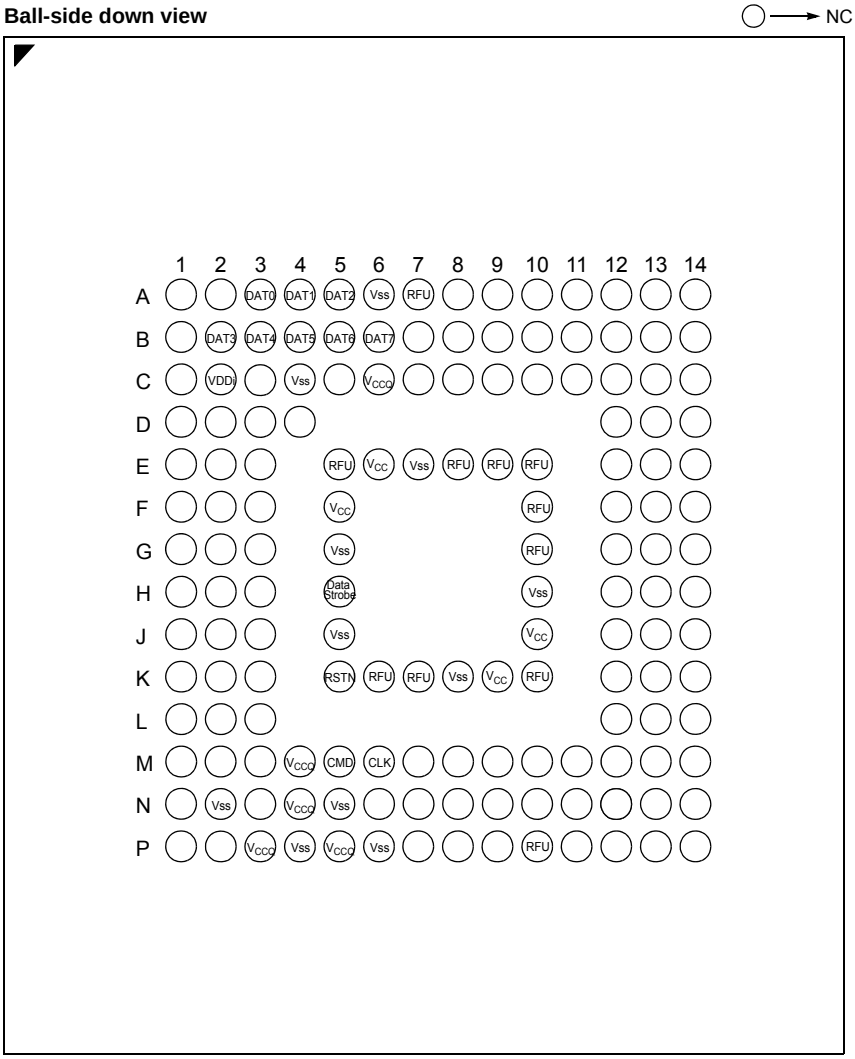


Figure 1. 153-FBGA

- CLK : Clock input.
- Data Strobe : Data Strobe is generated from eMMC to host.
  In HS400 mode, read data and CRC response are synchronized with Data Strobe.
- CMD : A bidirectional signal used for device initialization and command transfers.
  Command operates in two modes, open-drain for initialization and push-pull for fast command transfer.
- DAT0-7 : Bidirectional data channels. It operates in push-pull mode.
- RST_n : H/W reset signal pin.
- V_{CC} : Supply voltage for flash memory.
- V_{CCQ} : Supply voltage for memory controller.
- VDDi : Internal power node to stabilize regulator output to controller core logics.
- V_{SS} : Ground connections.
- RFU : Reserved for future use, do not use for any usage.

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2.1.2 11.5mm x 13mm x 1.0mm Package Dimension

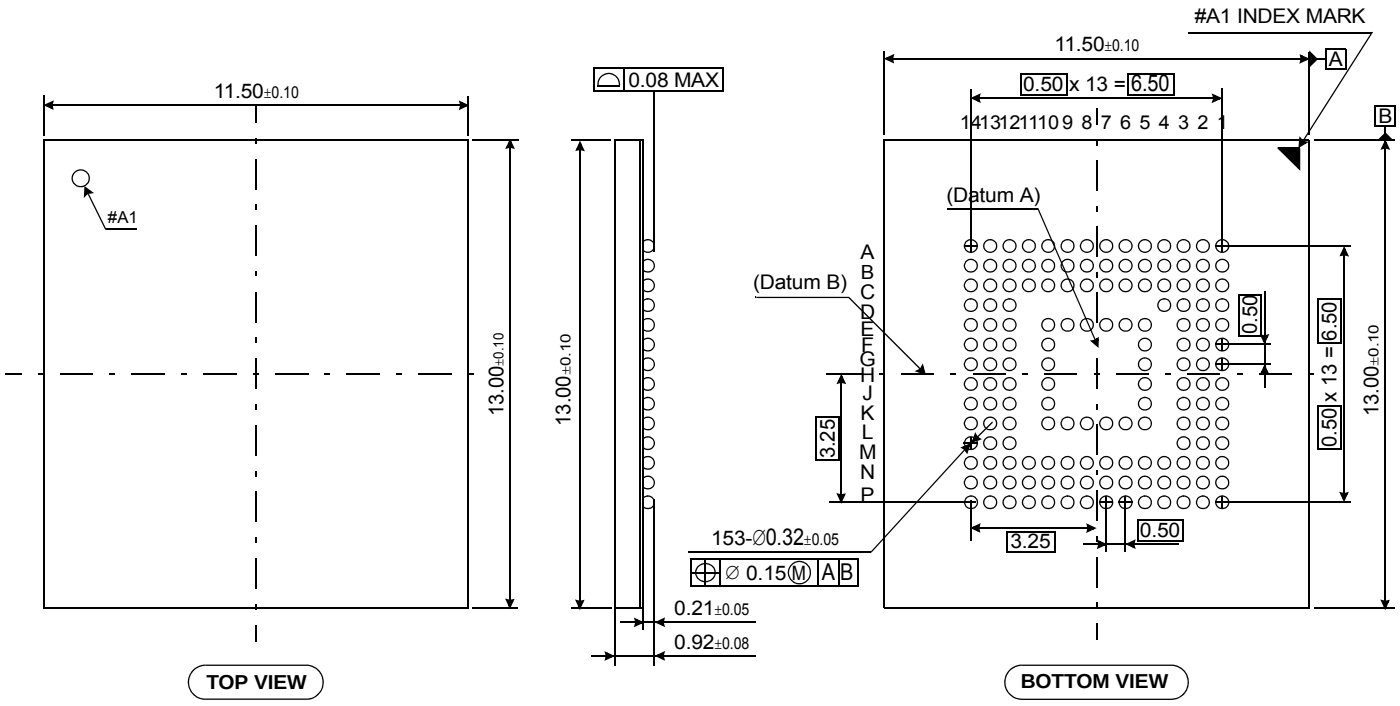


Figure 2. 11.5mm x 13mm x 1.0mm Package Dimension

2.2 Product Architecture

- eMMC consists of NAND Flash and Controller. V_{CCQ} is for Controller power and V_{CC} is for flash power.

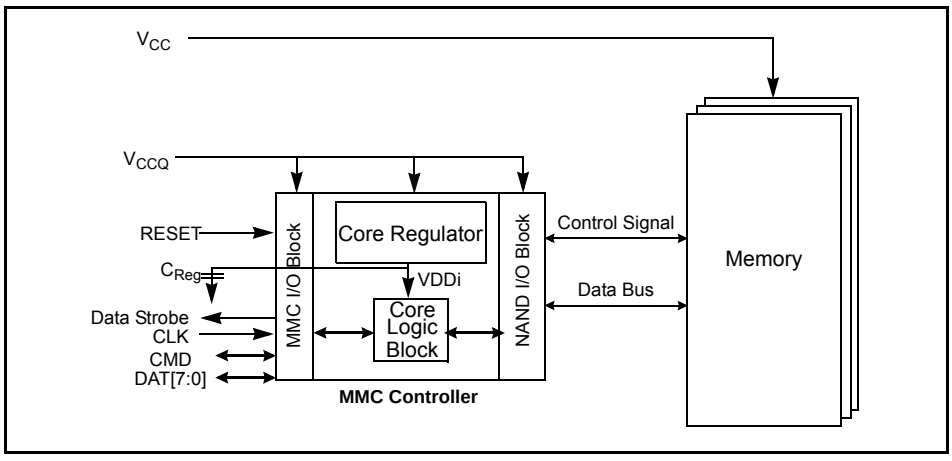


Figure 3. eMMC Block Diagram

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2.3 Supply Voltage

[Table 3] Supply Voltage

Item	Min	Max	Unit
V_{CCQ}	1.70	1.95	V
V_{CC}	2.7	3.6	
V_{SS}	-0.5	0.5	

2.4 Power Mode

2.4.1 Auto Power Saving Mode

If host does not issue any command during a certain duration (1ms), after previously issued command is completed, the device enters "Power Saving mode" to reduce power consumption.

At this time, commands arriving at the device while it is in power saving mode will be serviced in normal fashion.

[Table 4] Auto Power Saving Mode and Exit

Mode	Enter Condition	Escape Condition
Auto Power Saving Mode	When previous operation which came from Host is completed and no command is issued during a certain time.	If Host issues any command

[Table 5] Auto Power Saving Mode and Sleep Mode

	Auto Power Saving Mode	Sleep Mode
VCC Power	ON	OFF
Time to Sleep	< 1ms	< 1ms

2.5 Performance

[Table 6] Performance

Product	Seq.Read	Seq.Write	Unit
128 GB	320	200	MB/s

NOTE :
Test Condition : Bus width x8, HS400, 512KB data transfer, w/o file system overhead, measured on Samsung's internal board.

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3.0 HS400 MODE

eMMC 5.1 product supports high speed DDR interface timing mode up to 400MB/s at 200MHz with 1.8V I/O supply.
HS400 mode supports the following features:

- DDR Data sampling method
- CLK frequency up to 200MHz DDR (up to 400Mbps)
- Only 8-bits bus width available
- Signaling levels of 1.8V
- Six selectable Drive Strength (refer to the table below)

[Table 7] I/O Driver Strength Types

Driver Type	HS200 & HS400 Support	Nominal Impedance	Approximated Driving Capability Compared to Type-0	Remark
0	Default	50Ω	x1	Default Driver Type. Supports up to 200MHz operation.
1	Optional	33Ω	x1.5	Supports up to 200MHz Operation.
2	Optional	66Ω	x0.75	The weakest driver that supports up to 200MHz operation.
3	Optional	100Ω	x0.5	For low noise and low EMI systems. Maximal operating frequency is decided by Host design.
4	Optional	40Ω	x1.2	Supports up to 200MHz DDR operation

NOTE :
1) Support of Driver Type-0 is default for HS200 & HS400 Device, while supporting Driver types 1~ 4 are optional for HS200 & HS400 Device.

[Table 8] Device Type Values (EXT_CSD Register : DEVICE_TYPE [196])

Bit	Device Type	Supportability
7	HS400 Dual Data Rate eMMC @ 200 MHz - 1.2V I/O	Not support
6	HS400 Dual Data Rate eMMC @ 200 MHz - 1.8V I/O	Support
5	HS200 Single Data Rate eMMC @ 200 MHz - 1.2V I/O	Not support
4	HS200 Single Data Rate eMMC @ 200 MHz - 1.8V I/O	Support
3	High-Speed Dual Data Rate eMMC @ 52MHz - 1.2V I/O	Not support
2	High-Speed Dual Data Rate eMMC @ 52MHz - 1.8V or 3V I/O	Support[1)]
1	High-Speed eMMC @ 52MHz - at rated device voltage(s)	Support
0	High-Speed eMMC @ 26MHz - at rated device voltage(s)	Support

NOTE :
1) Only 1.8V Supported.

[Table 9] Extended CSD Revisions (EXT_CSD Register : EXT_CSD_REV [192])

Value	Timing Interface	EXT_CSD Register Value
255-8	Reserved	-
8	Revision 1.8 (for MMC V5.1)	0x08
7	Revision 1.7 (for MMC V5.0)	-
6	Revision 1.6 (for MMC V4.5, V4.51)	-
5	Revision 1.5 (for MMC V4.41)	-
4	Revision 1.4 (Obsolete)	-
3	Revision 1.3 (for MMC V4.3)	-
2	Revision 1.2 (for MMC V4.2)	-
1	Revision 1.1 (for MMC V4.1)	-
0	Revision 1.0 (for MMC V4.0)	-

[Table 10] High Speed Timing Values (EXT_CSD Register : HS_TIMING [185])

Value	Timing Interface	Supportability
0x0	Selecting backwards compatibility interface timing	Support
0x1	High Speed	Support
0x2	HS200	Support
0x3	HS400	Support

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4.0 NEW eMMC 5.1 FEATURES

4.1 Overview

[Table 11] Overview

New Feature	JEDEC	Support
Cache Flushing Report	Mandatory	Yes
Background operation control	Mandatory	Yes
Command Queuing	Optional	Yes
Enhanced Strobe	Optional	Yes
RPMB Throughput improve	Optional	Yes
Secure Write Protection	Optional	Yes

4.2 Command Queuing

To facilitate command queuing in eMMC, the device manages an internal task queue that the host can queue during data transfer tasks.

Every task is issued by the host and initially queued as pending. The device works to prepare pending tasks for execution. When a task is ready for execution, its state changes to “ready for execution”.

The host tracks the state of all queued tasks and may order the execution of any task, marked as “ready for execution”, by sending a command indicating its task ID. The device executes the data transfer transaction after receiving the execute command (CMD46/CMD47).

4.2.1 CMD Set Description

[Table 12] CMD Set Description and Details

CMD	Type	Argument	Abbreviation	Purpose
CMD44	ac/R1	[31] Reliable Write Request [30] DAT_DIR - "0" write / "1" read [29] tag request [28:25] context ID [24] forced programming [23] Priority: “0” simple / “1” high [20:16] TASK ID [15:0] number of blocks	QUEUED_TASK _PARAMS	Define direction of operation (Read or Write) and Set high priority CMD Queue with task ID
CMD45	ac/R1	[31:0] Start block address	QUEUED_TASK_ADDRESS	Indicate data address for Queued CMD
CMD46	adtc/R1	[20:16] TASK ID	EXECUTE_READ_TASK	(Read) Transmit the requested number of data blocks
CMD47	adtc/R1	[20:16] TASK ID	EXECUTE_WRITE_TASK	(Write) Transmit the requested number of data blocks
CMD48	ac/R1b	[20:16] Task ID [3:0] TM op-code	CMDQ_TASK _MGMT	Reset a specific task or entire queue. [20:16] when TM op-code = 2h these bits represent TaskID. When TM op-code = 1h these bits are reserved."

4.2.2 New Response : QSR (Queue Status Register)

The 32-bit Queue Status Register (QSR) carries the state of tasks in the queue at a specific point in time. The host has read access to this register through device response to SEND_STATUS command (CMD13 with bit[15]=”1”), R1’s argument will be the 32- bit Queue Status Register (QSR). Every bit in the QSR represents the task who’s ID corresponds to the bit index. If bit QSR[i] = “0”, then the queued task with a Task ID i is not ready for execution. The task may be queued and pending, or the Task ID is unused. If bit QSR[i] = “1”, then the queued task with Task ID i is ready for execution.

4.2.3 Send Status : CMD13

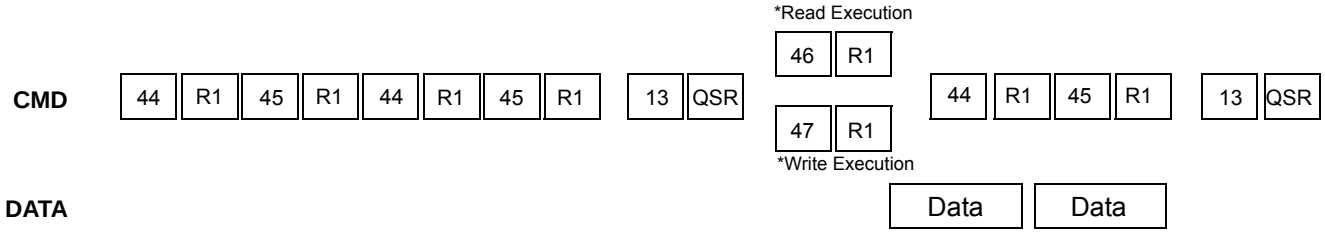
CMD13 for reading the Queue Status Register (QSR) by the host. If bit[15] in CMD13’s argument is set to 1, then the device shall send an R1 Response with the QSR instead of the Device Status. * There is still legacy CMD13 with R` response.

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4.2.4 Mechanism of CMD Queue Operation

Host issues CMD44 with Task ID number, Sector, Count, Direction, Priority to the device followed by CMD45 and host checks the Queue Status check with CMD13 [15]bits to 1. After that host issues CMD46 for Read or CMD47 for write During CMD queue operation, CMD44/CMD45 is able to be issued at anytime when the CMD line is not in use.



4.2.5 CMD Queue Register Description

Configuration and capability structures shall be added to the EXT_CSD register, as described below.

[Table 13] CMD Queuing Support (EXT_CSD Register : CMDQ_SUPPORT [308])

Bit7	Bit6	Bit5	Bit4	Bit 3	Bit2	Bit1	Bit0
Reserved							CMD Queue supportability

This field indicates whether the device supports command queuing or not.

0x0: CMD Queue function is not supported.
0x1: CMD Queue function is supported.

[Table 14] Command Queue Mode Enable (EXT_CSD Register : CMDQ_MODE_EN [15])

Bit7	Bit6	Bit5	Bit4	Bit 3	Bit2	Bit1	Bit0
Reserved							0x00

This field is used by the host enable command queuing.

0x0: Queue function is not enabled.
0x1: Queue function is enabled.

[Table 15] CMD Queuing Depth (EXT_CSD Register : CMDQ_DEPTH [307])

Bit7	Bit6	Bit5	Bit4	Bit 3	Bit2	Bit1	Bit0
Reserved			0x0F				

This field is used to calculate the depth of the queue supported by the device.

Bit encoding:
[7:5]: Reserved.
[4:0]: N,a parameter used to calculate the Queue Depth of task queue in the device.
Queue Depth = N+1.

4.3 Enhanced Strobe Mode

This product supports Enhanced Strobe in HS400 mode and refer to the details as described in eMMC5.1 JEDEC standard.

4.4 RPMB Throughput Improve

[Table 16] Related Parameter Register in EXT_CSD : WR_REL_PARAM [166]

Name	Field	Bit	Type
Enhanced RPMB Reliable Write	EN_RPMB_REL_WR	4	R

Bit[4]: EN_RPMB_REL_WR(R)
0x0: RPMB transfer size is either 256B (single 512B frame) or 512B (Two 512B frame).
0 x1: RPMB transfer size is either 256B (single 512B frame), 512B (Two 512B frame) or 8KB (Thirthy two 512B frames).

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4.5 Secure Write Protection

Configuration and capability structures shall be added to the EXT_CSD register and Authenticated Device Configuration Area as described below.

[Table 17] Parameter Register in EXT_CSD : SECURE_WP_INFO [211]

Bit7	Bit6	Bit5	Bit4	Bit	Bit2	Bit1	Bit0
Reserved						SECURE_WP_EN_STATUS	SECURE_WP_SUPPORT

Bit[7:2]: Reserved.
Bit[1]: SECURE_WP_EN_STATUS(R)
0x0: Legacy Write Protection mode.
0x1: Secure Write Protection mode.
Bit[0]: SECURE_WP_SUPPORT(R)
0x0: Secure Write Protection is NOT supported by this device.
0x1: Secure Write Protection is supported by this device.

[Table 18] Authenticated Device Configuration Area[1] : SECURE_WP_MODE_ENABLE

Bit7	Bit6	Bit5	Bit4	Bit	Bit2	Bit1	Bit0
Reserved							0x00

Bit[7:1] : Reserved.
Bit[0] : SECURE_WP_EN (R/W/E)
The default value of this field is 0x0.

- 0x0 : Legacy Write Protection mode, i.e., TMP_WRITE_PROTECT[12], PERM_WRITE_PROTECT[13] is updated by CMD27. USER_WP[171], BOOT_WP[173] and BOOT_WP_STATUS[174] are updated by CMD6.

- 0x1 : Secure Write Protection mode. The access to the write protection related EXT_CSD and CSD fields depends on the value of SECURE_WP_MASK bit in SECURE_WP_MODE_CONFIG field.

[Table 19] Authenticated Device Configuration Area[2] : SECURE_WP_MODE_CONFIG

Bit7	Bit6	Bit5	Bit4	Bit	Bit2	Bit1	Bit0
Reserved							0x00

Bit[7:1] : Reserved.
Bit[0] : SECURE_WP_MASK (R/W/E_P)
The default value of this field is 0x0.

- 0x0: Disabling updating WP related EXT_CSD and CSD fields. CMD27 (Program CSD) will generate generic error for setting TMP_WRITE_PROTECT[12] , PERM_WRITE_PROTECT[13]. CMD6 for updating USER_WP[171], BOOT_WP[173] and BOOT_WP_STATUS[174] generates SWITCH_ERROR. If a force erase command is issued, the command will fail (Device stays locked) and the LOCK_UNLOCK_FAILED error bit will be set in the status register. If CMD28 or CMD29 is issued, then generic error will be occurred. Power-on Write Protected boot partitions will keep protected mode after power failure, H/W reset assertion and any CMD0 reset. The device keeps the current value of BOOT_WP_STATUS in the EXT_CSD register to be same after power cycle, H/W reset assertion, and any CMD0 reset.

- 0x1: Enabling updating WP related EXT_CSD and CSD fields. I.e TMP_WRITE_PROTECT[12] , PERM_WRITE_PROTECT[13] , USER_WP[171], BOOT_WP[173] and BOOT_WP_STATUS[174] are accessed using CMD6, CMD8 and CMD27. If a force erase command is issued and accepted, then ALL THE DEVICE CONTENT WILL BE ERASED including the PWD and PWD_LEN register content and the locked Device will get unlocked. If a force erase command is issued and power-on protected or a permanently-write-protected write protect groups exist on the device, the command will fail (Device stays locked) and the LOCK_UNLOCK_FAILED error bit will be set in the status register. An attempt to force erase on an unlocked Device will fail and LOCK_UNLOCK_FAILED error bit will be set in the status register. Write Protection is applied to the WPG indicated by CMD28 with the WP type indicated by the bit[2] and bit[0] of USER_WP[171]. All temporary WP Groups and power-on Write Protected boot partitions become writable/erasable temporarily which means write protect type is not changed. All power-on and permanent WP Groups in user area will not become writable/erasable temporarily. Those temporarily writable/erasable area will become write protected when this bit is cleared to 0x0 by the host or when there is power failure, H/W reset assertion and any CMD0 reset. The device keeps the current value of BOOT_WP_STATUS in the EXT_CSD register to be same after power cycle, H/W reset assertion, and any CMD0 reset.

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5.0 TECHNICAL NOTES

5.1 S/W Algorithm

5.1.1 Partition Management

The device initially consists of two Boot Partitions and RPMB Partition and User Data Area.

The User Data Area can be divided into four General Purpose Area Partitions and User Data Area partition. Each of the General Purpose Area partitions and a section of User Data Area partition can be configured as enhanced partition.

5.1.1.1 Enhanced Partition (Area)

SAMSUNG eMMC adopts Enhanced User Data Area as SLC Mode. Therefore when master adopts some portion as enhanced user data area in User Data Area, that area occupies double size of original set up size. (ex> if master set 1MB for enhanced mode, total 3MB user data area is needed to generate 1MB enhanced area).

Max Enhanced User Data Area size is defined as (MAX_ENH_SIZE_MULT x HC_WP_GRP_SIZE x HC_ERASE_GRP_SIZE x 512K Bytes).

5.1.2 Boot Operation

Device supports not only boot mode but also alternative boot mode. Device supports high speed timing and dual data rate during boot.

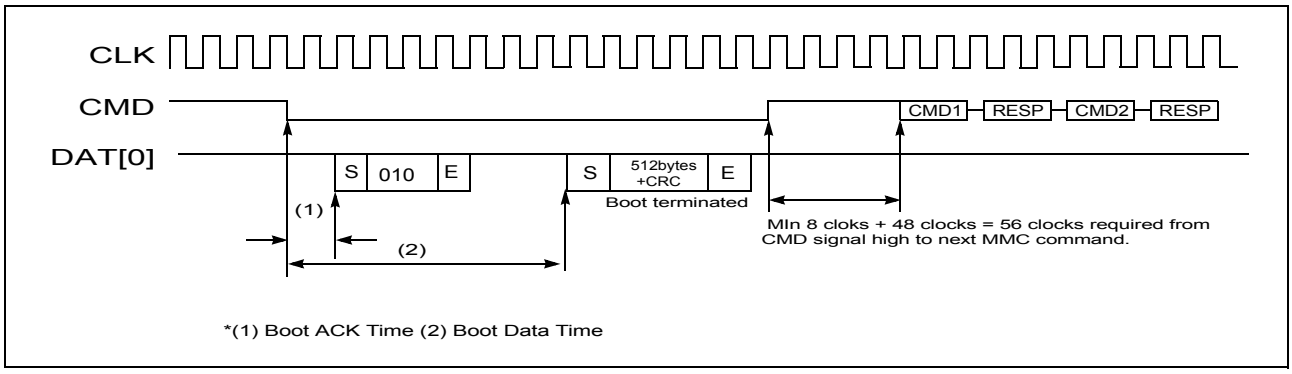


Figure 4. embedded MultiMediaCard State Diagram (Boot Mode)

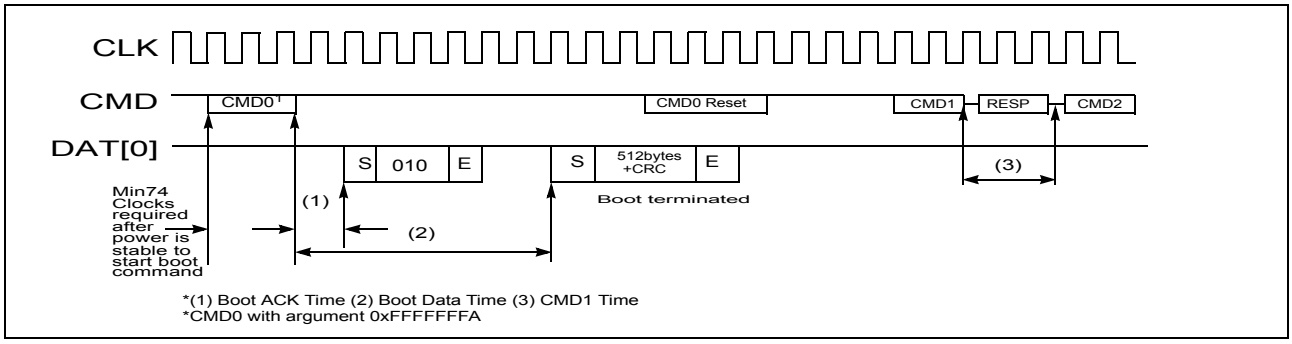


Figure 5. embedded MultiMediaCard State Diagram (Alternative Boot Mode)

[Table 20] Boot ACK, Boot Data and Initialization Time

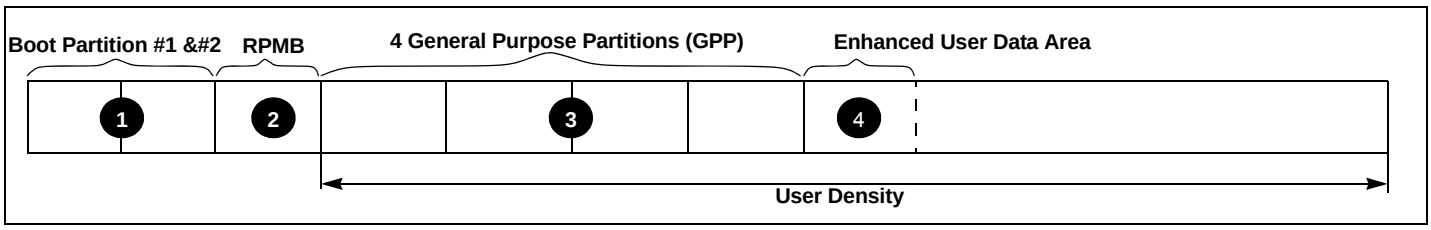
Timing Factor	Value
(1) Boot ACK Time	< 50 ms
(2) Boot Data Time	< 100 ms
(3) Initialization Time[1)]	< 3 secs

NOTE :
1) This initialization time includes partition setting, Please refer to INI_TIMEOUT_AP in 6.4 Extended CSD Register.
Normal initialization time (without partition setting) is completed within 1sec.

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5.1.3 User Density

Total User Density depends on device type.
For example, 32MB in the SLC Mode requires 64MB in TLC.
This results in decreasing of user density.



[Table 21] Capacity According to Partition

	Boot Partition 1	Boot Partition 2	RPMB
Default	4,096KB	4,096KB	16,384KB
Max	4,096KB	4,096KB	16,384KB

[Table 22] Maximum Enhanced Partition Size

Device	Max Enhanced Partition Size
128 GB	41,682,993,152 Byte

[Table 23] User Density Size

Device	User Density Size
128 GB	125,069,950,976 Byte

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6.0 REGISTER VALUE

6.1 OCR Register

The 32-bit operation conditions register stores the V_{CCQ} voltage profile of the eMMC. In addition, this register includes a status information bit. This status bit is set if the eMMC power up procedure has been finished. The OCR register shall be implemented by all eMMCs.

[Table 24] OCR Register

OCR bit	VCCQ Voltage Window[2)]	Register Value
[6:0]	Reserved	00 00000b
[7]	1.70 - 1.95	1b
[14:8]	2.0-2.6	000 0000b
[23:15]	2.7-3.6	1 1111 1111b
[28:24]	Reserved	0 0000b
[30:29]	Access Mode	00b (byte mode) 10b (sector mode) -[*Higher than 2GB only]
[31]	eMMC power up status bit (busy)[1)]	

NOTE :
1) This bit is set to LOW if the eMMC has not finished the power up routine.
2) The voltage for internal flash memory(V_{CC}) should be 2.7-3.6v regardless of OCR Register value.

6.2 CID Register

[Table 25] CID Register

Name	Field	Width	CID Slice	CID Value
Manufacturer ID	MID	8	[127:120]	0x15
Reserved		6	[119:114]	---
Card/BGA	CBX	2	[113:112]	0x01
OEM/Application ID	OID	8	[111:104]	___[1)]
Product name	PNM	48	[103:56]	See Product name table
Product revision	PRV	8	[55:48]	___[2)]
Product serial number	PSN	32	[47:16]	___[3)]
Manufacturing date	MDT	8	[15:8]	___[4)]
CRC7 checksum	CRC	7	[7:1]	___[5)]
not used, always '1'	-	1	[0:0]	---

NOTE :
1),4),5) description are same as eMMC JEDEC standard.
2) PRV is composed of the revision count of controller and the revision count of F/W patch.
3) A 32 bits unsigned binary integer. (Random Number).

6.2.1 Product Name Table (In CID Register)

[Table 26] Product Name Table

Part ID	Density	Product Name in CID Register (PNM)
KLMDG4UCTB-B041	128 GB	0 x 445554423432

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6.3 CSD Register

The Card-Specific Data register provides information on how to access the eMMC contents. The CSD defines the data format, error correction type, maximum data access time, data transfer speed, whether the DSR register can be used etc. The programmable part of the register (entries marked by W or E, see below) can be changed by CMD27. The type of the entries in the table below is coded as follows:
R: Read only.
W: One time programmable and not readable.
R/W: One time programmable and readable.
W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and not readable.
R/W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and readable.
R/W/C_P: Writable after value cleared by power failure and HW/ rest assertion (the value not cleared by CMD0 reset) and readable.
R/W/E_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and readable.
W/E/_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and not readable.

[Table 27] CSD Register

Name	Field	Width	Cell Type	CSD Slice	CSD Value
					128 GB
CSD structure	CSD_STRUCTURE	2	R	[127:126]	0x3
System specification version	SPEC_VERS	4	R	[125:122]	0x4
Reserved	-	2	R	[121:120]	-
Data read access-time 1	TAAC	8	R	[119:112]	0x27
Data read access-time 2 in CLK cycles (NSAC*100)	NSAC	8	R	[111:104]	0x1
Max. bus clock frequency	TRAN_SPEED	8	R	[103:96]	0x32
Device command classes	CCC	12	R	[95:84]	0xF5
Max. read data block length	READ_BL_LEN	4	R	[83:80]	0x9
Partial blocks for read allowed	READ_BL_PARTIAL	1	R	[79:79]	0x0
Write block misalignment	WRITE_BLK_MISALIGN	1	R	[78:78]	0x0
Read block misalignment	READ_BLK_MISALIGN	1	R	[77:77]	0x0
DSR implemented	DSR_IMP	1	R	[76:76]	0x0
Reserved	-	2	R	[75:74]	-
Device size	C_SIZE	12	R	[73:62]	0xFFF
Max. read current @ VDD min	VDD_R_CURR_MIN	3	R	[61:59]	0x6
Max. read current @ VDD max	VDD_R_CURR_MAX	3	R	[58:56]	0x6
Max. write current @ VDD min	VDD_W_CURR_MIN	3	R	[55:53]	0x6
Max. write current @ VDD max	VDD_W_CURR_MAX	3	R	[52:50]	0x6
Device size multiplier	C_SIZE_MULT	3	R	[49:47]	0x7
Erase group size	ERASE_GRP_SIZE	5	R	[46:42]	0x1F
Erase group size multiplier	ERASE_GRP_MULT	5	R	[41:37]	0x1F
Write protect group size	WP_GRP_SIZE	5	R	[36:32]	0xF
Write protect group enable	WP_GRP_ENABLE	1	R	[31:31]	0x1
Manufacturer default ECC	DEFAULT_ECC	2	R	[30:29]	0x0
Write speed factor	R2W_FACTOR	3	R	[28:26]	0x3
Max. write data block length	WRITE_BL_LEN	4	R	[25:22]	0x9
Partial blocks for write allowed	WRITE_BL_PARTIAL	1	R	[21:21]	0x0
Reserved	-	4	R	[20:17]	-
Content protection application	CONTENT_PROT_APP	1	R	[16:16]	0x0
File format group	FILE_FORMAT_GRP	1	R/W	[15:15]	0x0
Copy flag (OTP)	COPY	1	R/W	[14:14]	0x1
Permanent write protection	PERM_WRITE_PROTECT	1	R/W	[13:13]	0x0
Temporary write protection	TMP_WRITE_PROTECT	1	R/W/E	[12:12]	0x0
File format	FILE_FORMAT	2	R/W	[11:10]	0x0
ECC code	ECC	2	R/W/E	[9:8]	0x0
CRC	CRC	7	R/W/E	[7:1]	0x6
Not used, always'1'	-	1	—	[0:0]	1

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6.4 Extended CSD Register

The Extended CSD register defines the eMMC properties and selected modes. It is 512 bytes long.
The most significant 320 bytes are the Properties segment, which defines the eMMC capabilities and cannot be modified by the host. The lower 192 bytes are the Modes segment, which defines the configuration the eMMC is working in. These modes can be changed by the host by means of the SWITCH command.
R: Read only.
W: One time programmable and not readable.
R/W: One time programmable and readable.
W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and not readable.
R/W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and readable.
R/W/C_P: Writable after value cleared by power failure and HW/ rest assertion (the value not cleared by CMD0 reset) and readable.
R/W/E_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and readable.
W/E/_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and not readable.

[Table 28] Extended CSD Register

Name	Field	Size (Bytes)	Cell Type	CSD Slice	CSD Value
					128 GB
Properties Segment					
Reserved[1)]		6	-	[511:506]	-
Extended Security Commands Error	EXT_SECURITY_ERR	1	R	[505]	0x0
Supported Command Sets	S_CMD_SET	1	R	[504]	0x1
HPI features	HPI_FEATURES	1	R	[503]	0x1
Background operations support	BKOPS_SUPPORT	1	R	[502]	0x1
Max packed read commands	MAX_PACKED_READS	1	R	[501]	0x3F
Max packed write commands	MAX_PACKED_WRITES	1	R	[500]	0x3F
Data Tag Support	DATA_TAG_SUPPORT	1	R	[499]	0x1
Tag Unit Size	TAG_UNIT_SIZE	1	R	[498]	0x2
Tag Resources Size	TAG_RES_SIZE	1	R	[497]	0x0
Context management capabilities	CONTEXT_CAPABILITIES	1	R	[496]	0x5
Large Unit size	LARGE_UNIT_SIZE_M1	1	R	[495]	0x7
Extended partitions attribute support	EXT_SUPPORT	1	R	[494]	0x3
Supported modes	SUPPORTED_MODES	1	R	[493]	0x3
FFU features	FFU_FEATURES	1	R	[492]	0x0
Operation codes timeout	OPERATION_CODE_TIME-OUT	1	R	[491]	0x00
FFU Argument	FFU_ARG	4	R	[490:487]	0xC7810000
Barrier support	BARRIER_SUPPORT	1	R	[486]	0x01
Reserved[1)]		177	-	[485:309]	-
CMD Queuing Support	CMDQ_SUPPORT	1	R	[308]	0x1
CMD Queuing Depth	CMDQ_DEPTH	1	R	[307]	0xF
Reserved[1)]		1	-	[306]	-
Number of FW sectors correctly programmed	NUMBER_OF_FW_SEC-TORS_CORRECTLY_PRO-GRAMMED	4	R	[305:302]	0x0
Vendor proprietary health report	VENDOR_PROPRI-ETARY_HEALTH_REPORT	32	R	[301:270]	0x0
Device life time estimation type B	DEVICE_LIFE_TIME_EST_TYP_B	1	R	[269]	0x1
Device life time estimation type A	DEVICE_LIFE_TIME_EST_TYP_A	1	R	[268]	0x1
Pre EOL information	PRE_EOL_INFO	1	R	[267]	0x1
Optimal read size	OPTIMAL_READ_SIZE	1	R	[266]	0x0
Optimal write size	OPTIMAL_WRITE_SIZE	1	R	[265]	0x60
Optimal trim unit size	OPTIMAL_TRIM_UNIT_SIZE	1	R	[264]	0x1
Device version	DEVICE_VERSION	2	R	[263:262]	0x00

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Firmware version	FIRMWARE_VERSION	8	R	[261:254]	Patch Version
Power class for 200MHz, DDR at VCC=3.6V	PWR_CL_DDR_200_360	1	R	[253]	0x0
Cache size	CACHE_SIZE	4	R	[252:249]	0x10000
Generic CMD6 timeout	GENERIC_CMD6_TIME	1	R	[248]	0xA
Power off notification (long) timeout	POWER_OFF_LONG_TIME	1	R	[247]	0x3C
Background operations status	BKOPS_STATUS	1	R	[246]	0x0
Number of correctly programmed sectors	CORRECTLY_PRG_SEC-TORS_NUM	4	R	[245:242]	0x0000
1st initialization time after partitioning	INI_TIMEOUT_AP	1	R	[241]	0x1E
Cache flush policy	CACHE_FLUSH_POLICY	1	R	[240]	0x1
Power class for 52MHz, DDR at 3.6V	PWR_CL_DDR_52_360	1	R	[239]	0x0
Power class for 52MHz, DDR at 1.95V	PWR_CL_DDR_52_195	1	R	[238]	0x0
Power class for 200MHz at V_{CCQ}=1.95V, V_{CC}=3.6V	PWR_CL_200_360	1	R	[237]	0x0
Power class for 200MHz, at V_{CCQ}=1.3V, V_{CC}=3.6V	PWR_CL_200_195	1	R	[236]	0x0
Minimum Write Performance for 8bit at 52MHz in DDR mode	MIN_PERF_DDR_W_8_52	1	R	[235]	0x0
Minimum Read Performance for 8bit at 52MHz in DDR mode	MIN_PERF_DDR_R_8_52	1	R	[234]	0x0
Reserved[1)]		1	-	[233]	-
TRIM Multiplier	TRIM_MULT	1	R	[232]	0x02
Secure Feature support	SEC_FEATURE_SUPPORT	1	R	[231]	0x55
Secure Erase Multiplier	SEC_ERASE_MULT	1	R	[230]	0x1B
Secure TRIM Multiplier	SEC_TRIM_MULT	1	R	[229]	0x11
Boot information	BOOT_INFO	1	R	[228]	0x7
Reserved[1)]		1	-	[227]	-
Boot partition size	BOOT_SIZE_MULT	1	R	[226]	0x20
Access size	ACC_SIZE	1	R	[225]	0x7
High-capacity erase unit size	HC_ERASE_GRP_SIZE	1	R	[224]	0x1
High-capacity erase timeout	ERASE_TIMEOUT_MULT	1	R	[223]	0x1
Reliable write sector count	REL_WR_SEC_C	1	R	[222]	0x1
High-capacity write protect group size	HC_WP_GRP_SIZE	1	R	[221]	0x10
Sleep current (V_{CC})	S_C_VCC	1	R	[220]	0x7
Sleep current (V_{CCQ})	S_C_VCCQ	1	R	[219]	0x7
Production state awareness timeout	PRODUC-TION_STATE_AWARENESS_-TIMEOUT	1	R	[218]	0x0
Sleep/awake timeout	S_A_TIMEOUT	1	R	[217]	0x11
Sleep Notification Timeout	SLEEP_NOTIFICATION_TIME	1	R	[216]	0x7
Sector Count	SEC_COUNT	4	R	[215:212]	0xE8F6000
Secure Write Protect Information	SECURE_WP_INFO	1	R	[211]	0x1
Minimum Write Performance for 8bit at 52MHz	MIN_PERF_W_8_52	1	R	[210]	0x0
Minimum Read Performance for 8bit at 52MHz	MIN_PERF_R_8_52	1	R	[209]	0x0
Minimum Write Performance for 8bit at 26MHz, for 4bit at 52MHz	MIN_PERF_W_8_26_4_52	1	R	[208]	0x0
Minimum Read Performance for 8bit at 26MHz, for 4bit at 52MHz	MIN_PERF_R_8_26_4_52	1	R	[207]	0x0
Minimum Write Performance for 4bit at 26MHz	MIN_PERF_W_4_26	1	R	[206]	0x0

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Minimum Read Performance for 4bit at 26MHz	MIN_PERF_R_4_26	1	R	[205]	0x0
Reserved[1)]		1	-	[204]	-
Power class for 26MHz at 3.6V 1 R	PWR_CL_26_360	1	R	[203]	0x0
Power class for 52MHz at 3.6V 1 R	PWR_CL_52_360	1	R	[202]	0x0
Power class for 26MHz at 1.95V 1 R	PWR_CL_26_195	1	R	[201]	0x0
Power class for 52MHz at 1.95V 1 R	PWR_CL_52_195	1	R	[200]	0x0
Partition switching timing	PARTITION_SWITCH_TIME	1	R	[199]	0x2
Out-of-interrupt busy timing	OUT_OF_INTERRUPT_TIME	1	R	[198]	0xA
I/O Driver Strength	DRIVER_STRENGTH	1	R	[197]	0x1F
Device type	DEVICE_TYPE	1	R	[196]	0x57
Reserved[1)]		1	-	[195]	-
CSD structure	CSD_STRUCTURE	1	R	[194]	0x2
Reserved[1)]		1	-	[193]	-
Extended CSD revision	EXT_CSD_REV	1	R	[192]	0x8
Modes Segment					
Command set	CMD_SET	1	R/W/E_P	[191]	0x0
Reserved[1)]		1	-	[190]	-
Command set revision	CMD_SET_REV	1	R	[189]	0x0
Reserved[1)]		1	-	[188]	-
Power class	POWER_CLASS	1	R/W/E_P	[187]	0x0
Reserved[1)]		1	-	[186]	-
High-speed interface timing	HS_TIMING	1	R/W/E_P	[185]	0x1
Strobe Support	STROBE_SUPPORT	1	R	[184]	0x1
Bus width mode	BUS_WIDTH	1	W/E_P	[183]	0x0
Reserved[1)]		1	-	[182]	-
Erased memory content	ERASED_MEM_CONT	1	R	[181]	0x0
Reserved[1)]		1	-	[180]	-
Partition configuration	PARTITION_CONFIG	1	R/W/E & R/W/E_P	[179]	0x0
Boot config protection	BOOT_CONFIG_PROT	1	R/W & R/W/C_P	[178]	0x0
Boot bus Conditions	BOOT_BUS_CONDITIONS	1	R/W/E	[177]	0x0
Reserved[1)]		1	-	[176]	-
High-density erase group definition	ERASE_GROUP_DEF	1	R/W/E_P	[175]	0x0
Boot write protection status registers	BOOT_WP_STATUS	1	R	[174]	0x0
Boot area write protection register	BOOT_WP	1	R/W & R/W/C_P	[173]	0x0
Reserved[1)]		1	-	[172]	-
User area write protection register	USER_WP	1	R/W, R/W/C_P &R/W/ E_P	[171]	0x0
Reserved[1)]		1	-	[170]	-
FW configuration	FW_CONFIG	1	R/W	[169]	0x0
RPMB Size	RPMB_SIZE_MULT	1	R	[168]	0x80
Write reliability setting register	WR_REL_SET	1	R/W	[167]	0x1F
Write reliability parameter register	WR_REL_PARAM	1	R	[166]	0x14
Start Sanitize operation	SANITIZE_START	1	W/E_P	[165]	0x0
Manually start background operations	BKOPS_START	1	W/E_P	[164]	0x0

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Enable background operations handshake	BKOPS_EN	1	R/W&R/W/E	[163]	0x0
H/W reset function	RST_n_FUNCTION	1	R/W	[162]	0x0
HPI management	HPI_MGMT	1	R/W/E_P	[161]	0x0
Partitioning Support	PARTITIONING_SUPPORT	1	R	[160]	0x7
Max Enhanced Area Size	MAX_ENH_SIZE_MULT	3	R	[159:157]	0x1369
Partitions attribute	PARTITIONS_ATTRIBUTE	1	R/W	[156]	0x0
Partitioning Setting	PARTITION_SETTING_COMPLETED	1	R/W	[155]	0x0
General Purpose Partition Size	GP_SIZE_MULT	12	R/W	[154:143]	0x00
Enhanced User Data Area Size	ENH_SIZE_MULT	3	R/W	[142:140]	0x00
Enhanced User Data Start Address	ENH_START_ADDR	4	R/W	[139:136]	0x00
Reserved[1)]		1	-	[135]	-
Bad Block Management mode	SEC_BAD_BLK_MGMNT	1	R/W	[134]	0x0
Production state awareness	PRODUC-TION_STATE_AWARENESS	1	R/W/E	[133]	0x0
Package Case Temperature is controlled	TCASE_SUPPORT	1	W/E_P	[132]	0x0
Periodic Wake-up	PERIODIC_WAKEUP	1	R/W/E	[131]	0x0
Program CID/CSD in DDR mode support	PROGRAM_CID_CSD_DDR_-SUPPORT	1	R	[130]	0x1
Reserved[1)]		2	-	[129:128]	-
Vendor Mode Configuration	VENDOR_MODE_CONFIG	64	<vendor specific>	[127:64]	-
Native sector size	NATIVE_SECTOR_SIZE	1	R	[63]	0x0
Sector size emulation	USE_NATIVE_SECTOR	1	R/W	[62]	0x0
Sector size	DATA_SECTOR_SIZE	1	R	[61]	0x0
1st initialization after disabling sector size emulation	INI_TIMEOUT_EMU	1	R	[60]	0x0
Class 6 commands control	CLASS_6_CTRL	1	R/W/E_P	[59]	0x0
Number of addressed group to be Released	DYNCAP_NEEDED	1	R	[58]	0x0
Exception events control	EXCEPTION_EVENTS_CTRL	2	R/W/E_P	[57:56]	0x00
Exception events status	EXCEPTION_EVENTS_STA-TUS	2	R	[55:54]	0x00
Extended Partitions Attribute	EXT_PARTITIONS_ATTRI-BUTE	2	R/W	[53:52]	0x00
Context configuration	CONTEXT_CONF	15	R/W/E_P	[51:37]	0x00
Packed command status	PACKED_COMMAND_STA-TUS	1	R	[36]	0x0
Packed command failure index	PACKED_FAILURE_INDEX	1	R	[35]	0x0
Power Off Notification	POWER_OFF_NOTIFICATION	1	R/W/E_P	[34]	0x0
Control to turn the Cache ON/OFF	CACHE_CTRL	1	R/W/E_P	[33]	0x0
Flushing of the cache	FLUSH_CACHE	1	W/E_P	[32]	0x0
Control to turn the Barrier ON/OFF	BARRIER_CTRL	1	R/W	[31]	0x0
Mode config	MODE_CONFIG	1	R/W/E_P	[30]	0x0
Mode operation codes	MODE_OPERATION_CODES	1	W/E_P	[29]	0x0
Reserved[1)]		2	-	[28:27]	-
FFU status	FFU_STATUS	1	R	[26]	0x0
Pre loading data size	PRE_LOADING_DATA_SIZE	4	R/W/E_P	[25:22]	0x00
Max pre loading data size	MAX_PRE_LOADING_DATA_SIZE	4	R	[21:18]	0x00

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Product state awareness enablement	PRODUCT_STATE_AWARENESS_ENABLEMENT	1	R/W/E & R	[17]	0x0
Secure Removal Type	SECURE_REMOVAL_TYPE	1	R/W & R	[16]	0x39
Command Queue Mode Enable	CMDQ_MODE_EN	1	R/W/E_P	[15]	0x0
Reserved[1)]		15	-	[14:0]	-

NOTE :
1) Reserved bits should be read as “0”.

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7.0 DC PARAMETER

7.1 Power Consumption

7.1.1 Active Power Consumption During Operation

[Table 29] Active Power Consumption During Operation

Density	V_{CCQ}	V_{CC}	Unit
128 GB	180	200	mA

NOTE :
Power Measurement conditions: Bus configuration =x8 @HS400.
The measurement for max RMS current is the average RMS current consumption over a period of 100ms.

7.1.2 Standby Power Consumption in Auto Power Saving Mode and Standby State

[Table 30] Standby Power Consumption in Auto Power Saving Mode and Standby State

Density	V_{CCQ}	V_{CC}	Unit
128 GB	120	70	uA

NOTE :
Power Measurement conditions: Bus configuration =x8, No CLK.
Typical value is measured at V_{CC}=3.3V, TA=25°C. Not 100% tested.

7.1.3 Sleep Power Consumption in Sleep State

[Table 31] Sleep Power Consumption in Sleep State

Density	V_{CCQ}	V_{CC}	Unit
128 GB	120	0[1)]	uA

NOTE :
Power Measurement conditions: Bus configuration =x8, No CLK.
1) In auto power saving mode, V_{CC} power can not be turned off. However in sleep mode V_{CC} power can be turned off.

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8.0 AC PARAMETER

8.1 Timing Parameter

[Table 32] Timing Parameter

Timing Parameter		Max Value	Unit
Initialization Time (tINIT)	Normal[1)]	1	s
	After partition setting[2)]	3	s
Read Timeout		100	ms
Write Timeout		350	ms
Erase Timeout		20	ms
Force Erase Timeout		3	min
Secure Erase Timeout		8	s
Secure Trim step1 Timeout		5	s
Secure Trim step2 Timeout		3	s
Trim Timeout		600	ms
Partition Switching Timeout (after Init)		1	ms
Power Off Notification (Short) Timeout		100	ms
Power Off Notification (Long) Timeout		600	ms

NOTE :
1) Normal Initialization Time without partition setting.
2) Initialization Time after partition setting, refer to INI_TIMEOUT_AP in Chapter 6.4 EXT_CSD register.
3) Be advised Timeout Values specified in Table above are for testing purposes under Samsung test pattern only and actual timeout situations may vary.
4) EXCEPTION_EVENT may occur and the actual timeout values may vary due to user environment.

8.2 Previous Bus Timing Parameters for DDR52 and HS200 Mode are defined by JEDEC Standard

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8.3 Bus Timing Specification in HS400 Mode

8.3.1 HS400 Device Input Timing

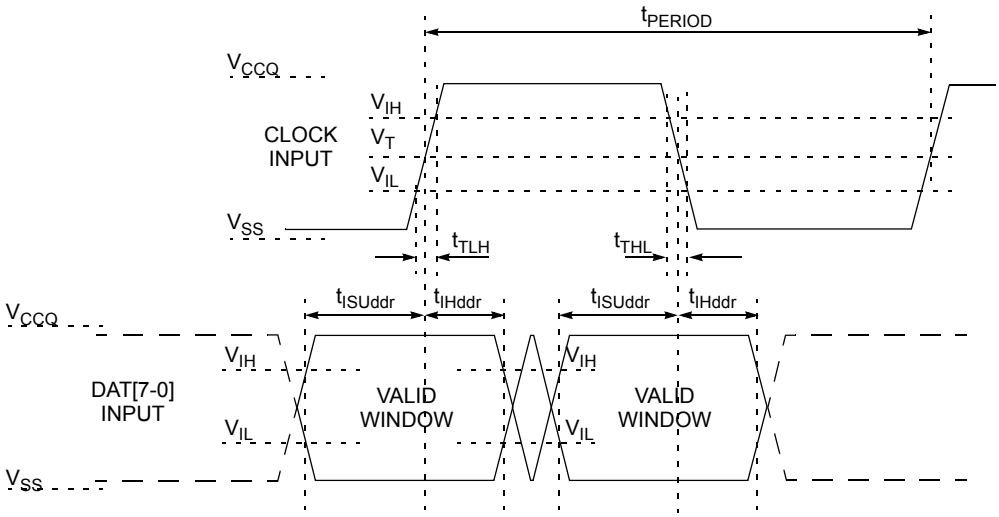


Figure 6. HS400 Device Input Timing

NOTE :
1) t_{ISU} and t_{IH} are measured at V_{IL}(max.) and V_{IH}(min.).
2) V_{IH} denotes V_{IH}(min.) and V_{IL} denotes V_{IL}(max.)

[Table 33] HS400 Device Input Timing

Parameter	Symbol	Min	Max	Unit
Input CLK				
Cycle time data transfer mode	t_{PERIOD}	5		ns
Slew rate	SR	1.125		V/ns
Duty cycle distortion	t_{CKDCD}	0.0	0.3	ns
Minimum pulse width	t_{CKMPW}	2.2		ns
Input DAT (Referenced to CLK)				
Input set-up time	t_{ISUddr}	0.4		ns
Input hold time	t_{IHddr}	0.4		ns
Slew rate	SR	1.125		V/ns

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8.3.2 HS400 Device Output Timing

Data Strobe is used to read data (data read and CRC status response read) in HS400 mode.
The device output value of Data Strobe is “High-Z” when the device is not in outputting data (data read, CRC status response).
Data Strobe is toggled only during data read period.

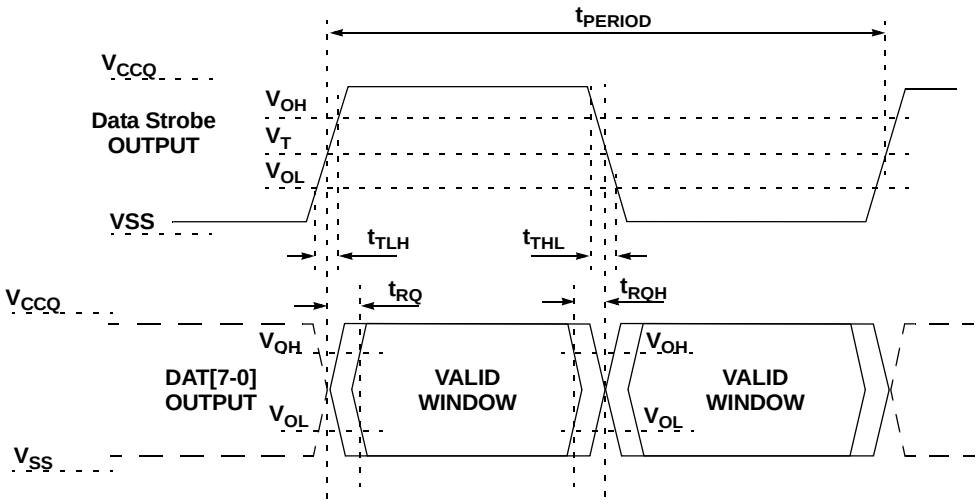


Figure 7. HS400 Device Output Timing

NOTE :
V_{OH} denotes V_{OH}(min.) and V_{OL} denotes V_{OL}(max.).

[Table 34] HS400 Device Output Timing

Parameter	Symbol	Min	Max	Unit
Data Strobe				
Cycle time data transfer mode	t_{PERIOD}	5		ns
Slew rate	SR	1.125		V/ns
Duty cycle distortion	t_{DSDCD}	0.0	0.2	ns
Minimum pulse width	t_{DSMPW}	2.0		ns
Read pre-amble	t_{RPRE}	0.4	-	t_{PERIOD}
Read post-amble	t_{RPST}	0.4	-	t_{PERIOD}
Output DAT (Referenced to Data Strobe)				
Output skew	t_{RQ}	-	0.4	ns
Output hold skew	t_{RQH}	-	0.4	ns
Slew rate	SR	1.125		V/ns

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8.4 Bus Signal Levels

As the bus can be supplied with a variable supply voltage, all signal levels are related to the supply voltage.

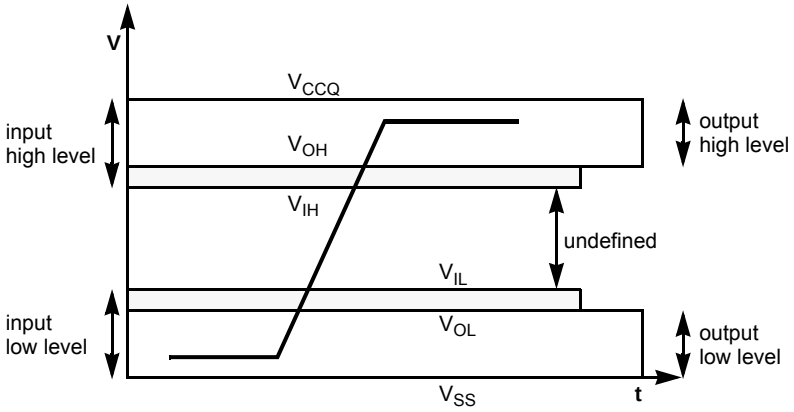


Figure 8. Bus Signal Levels

8.4.1 Open-Drain Mode Bus Signal Level

[Table 35] Open-Drain Bus Signal Level

Parameter	Symbol	Min	Max	Unit	Conditions
Output HIGH voltage	V_{OH}	V_{CCQ} - 0.2	-	V	1)
Output LOW voltage	V_{OL}	-	0.3	V	I_{OL} = 2 mA

NOTE :
1) Because Voh depends on external resistance value (including outside the package), this value does not apply as device specification.
Host is responsible to choose the external pull-up and open drain resistance value to meet Voh Min value.

8.4.2 Push-Pull Mode Bus Signal Level eMMC

The device input and output voltages shall be within the following specified ranges for any V_{CCQ} of the allowed voltage range.

[Table 36] Push-Pull Signal Level—High-Voltage eMMC

Parameter	Symbol	Min	Max	Unit	Conditions
Output HIGH voltage	V_{OH}	0.75*V_{CCQ}	-	V	I_{OH} = -100 uA@V_{CCQ} min
Output LOW voltage	V_{OL}	-	0.125*V_{CCQ}	V	I_{OL} = 100 uA@V_{CCQ} min
Input HIGH voltage	V_{IH}	0.625*V_{CCQ}	V_{CCQ} + 0.3	V	-
Input LOW voltage	V_{IL}	V_{SS} - 0.3	0.25*V_{CCQ}	V	-

[Table 37] Push-Pull Signal Level—1.70 - 1.95 V_{CCQ} Voltage Range

Parameter	Symbol	Min	Max	Unit	Conditions
Output HIGH voltage	V_{OH}	V_{CCQ} - 0.45V	-	V	I_{OH} = -2mA
Output LOW voltage	V_{OL}	-	0.45V	V	I_{OL} = 2mA
Input HIGH voltage	V_{IH}	0.65*V_{CCQ} 1)	V_{CCQ} + 0.3	V	-
Input LOW voltage	V_{IL}	V_{SS} - 0.3	0.35*V_{CCQ} 2)	V	-

NOTE :
1) 0.7*V_{CCQ} for MMC4.3 and older revisions.
2) 0.3*V_{CCQ} for MMC4.3 and older revisions.

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8.5 Bus Signal Line Load

The total capacitance C_L of each line of the eMMC bus is the sum of the bus master capacitance C_{HOST}, the bus capacitance C_{BUS} itself and the capacitance C_{DEVICE} of the eMMC connected to this line:

$$C_L = C_{HOST} + C_{BUS} + C_{DEVICE}$$

The sum of the host and bus capacitances should be under 20pF.

[Table 38] Bus Signal Line Load

Parameter	Symbol	Min	Typ	Max	Unit	Remark
Pull-up resistance for CMD	R_{CMD}	4.7		100	KOhm	to prevent bus floating
Pull-up resistance for DAT0-DAT7	R_{DAT}	10		100	KOhm	to prevent bus floating
Internal pull up resistance DAT1-DAT7	R_{int}	10		150	KOhm	to prevent unconnected lines floating
Single Device capacitance	C_{DEVICE}			12	pF	
Maximum signal line inductance				16	nH	f_{PP} <= 52 MHz

[Table 39] Capacitance and Resistance for HS400 Mode

Parameter	Symbol	Min	Typ	Max	Unit	Remark
Bus signal line capacitance	C_L			13	pF	Single Device
Single Device capacitance	C_{DEVICE}			6	pF	
Pull-down resistance for Data Strobe	$R_{Data\ Strobe}$	10		100	KOhm	

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