IS62C1024AL
IS65C1024AL

128K x 8 LOW POWER CMOS STATIC RAM

DECEMBER 2017

FEATURES

- High-speed access time: 35, 45 ns
- Low active power: 100 mW (typical)
- Low standby power: 20 µW (typical) CMOS standby
- Output Enable ($\overline{OE}$) and two Chip Enable ($\overline{CE1}$ and CE2) inputs for ease in applications
- Fully static operation: no clock or refresh required
- TTL compatible inputs and outputs
- Single 5V (±10%) power supply
- Commercial, Industrial, and Automotive temperature ranges available
- Standard Pin Configuration:
  — 32-pin SOP/ 32-pin TSOP (Type 1)
- Lead free available

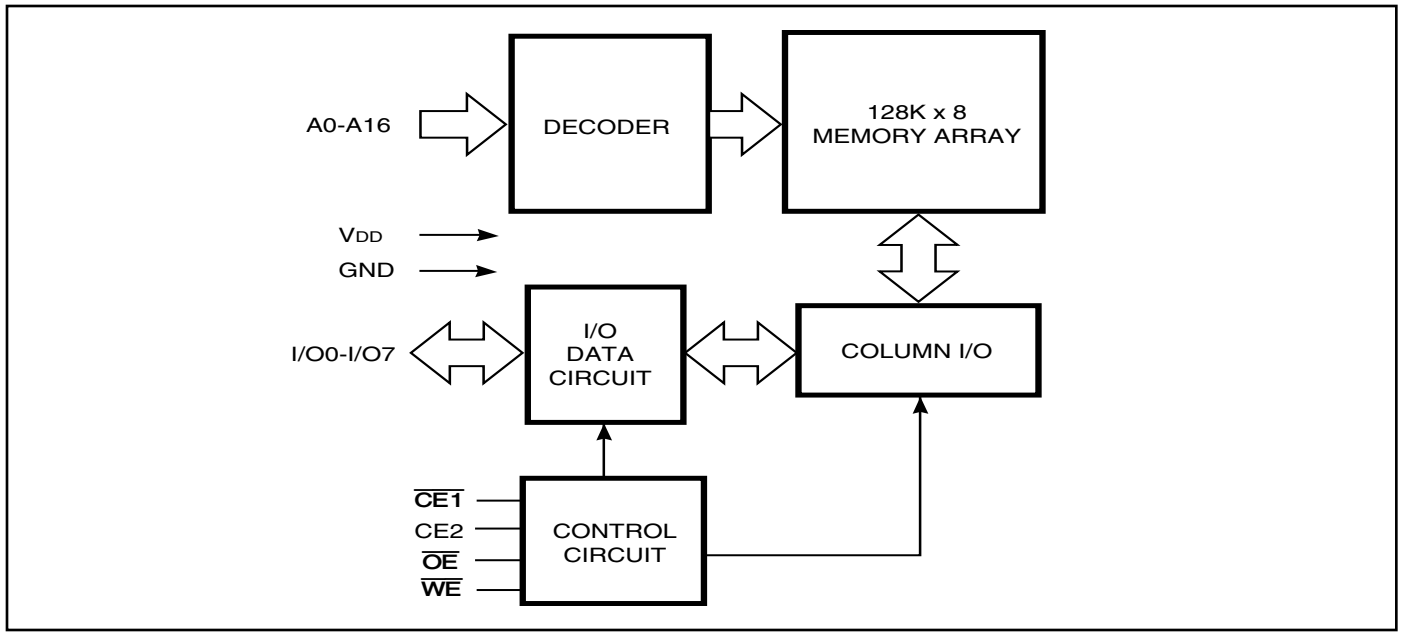
DESCRIPTION

The *ISSI* IS62C1024AL/IS65C1024AL is a low power, 131,072-word by 8-bit CMOS static RAM. It is fabricated using high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields higher performance and low power consumption devices.

When $\overline{CE1}$ is HIGH or CE2 is LOW (deselected), the device assumes a standby mode at which the power dissipation can be reduced by using CMOS input levels.

Easy memory expansion is provided by using two Chip Enable inputs, $\overline{CE1}$ and CE2. The active LOW Write Enable ($\overline{WE}$) controls both writing and reading of the memory.

FUNCTIONAL BLOCK DIAGRAM



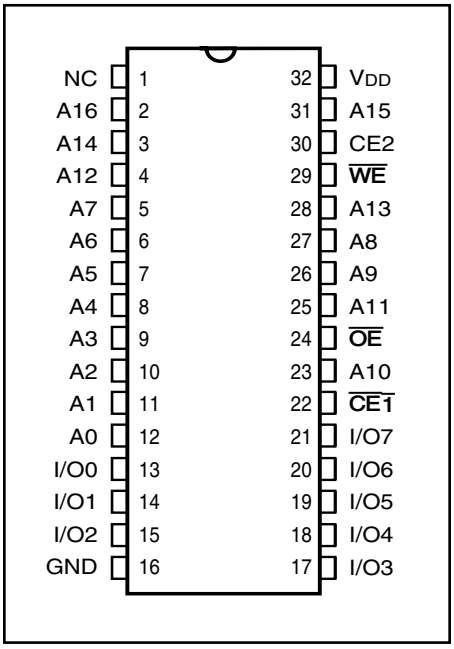
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b.) the user assume all such risks; and
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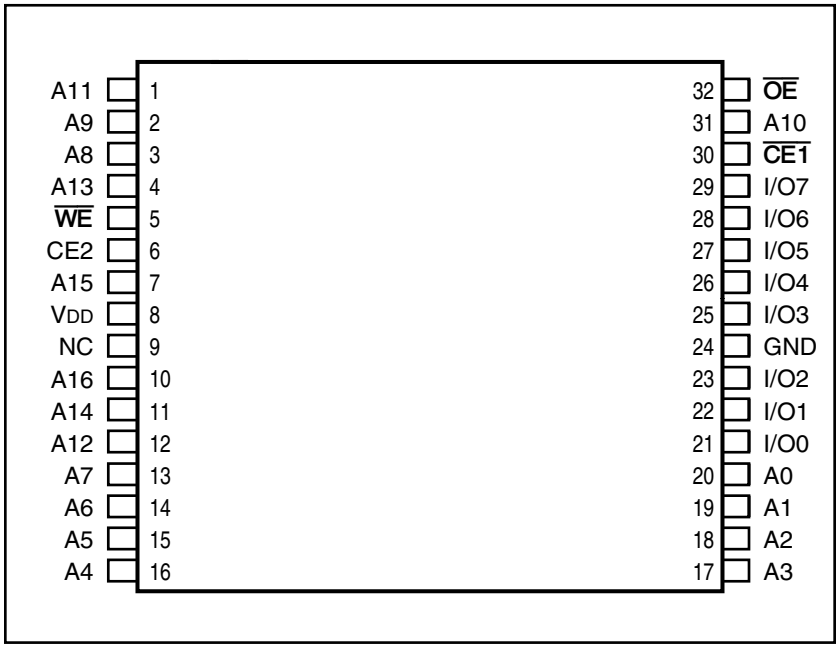
PIN CONFIGURATION

32-Pin SOP



PIN CONFIGURATION

32-Pin TSOP (Type 1)



PIN DESCRIPTIONS

A0-A16	Address Inputs
$\overline{CE1}$	Chip Enable 1 Input
CE2	Chip Enable 2 Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
I/O0-I/O7	Input/Output
V_{DD}	Power
GND	Ground

OPERATING RANGE (IS62C1024AL)

Range	Ambient Temperature	V_{DD}
Commercial	0°C to +70°C	5V ± 10%
Industrial	-40°C to +85°C	5V ± 10%

OPERATING RANGE (IS65C1024AL)

Range	Ambient Temperature	V_{DD}
Automotive	-40°C to +125°C	5V ± 10%

TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CE1}$	CE2	$\overline{OE}$	I/O Operation	V_{DD} Current
Not Selected	X	H	X	X	High-Z	I_{SB1}, I_{SB2}
(Power-down)	X	X	L	X	High-Z	I_{SB1}, I_{SB2}
Output Disabled	H	L	H	H	High-Z	I_{CC}
Read	H	L	H	L	D_{OUT}	I_{CC}
Write	L	L	H	X	D_{IN}	I_{CC}

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ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_{STG}	Storage Temperature	–65 to +125	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current (LOW)	20	mA

Notes:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE[1,2]

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

Notes:
1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, V_{DD} = 5.0V.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions	Options	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{DD} = Min., I_{OH} = –1.0 mA		2.4	—	V
V_{OL}	Output LOW Voltage	V_{DD} = Min., I_{OL} = 2.1 mA		—	0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{DD} + 0.5	V
V_{IL}	Input LOW Voltage[1]			-0.5	0.8	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{DD}	Com. Ind. Auto.	-1 -2 -5	1 2 5	µA
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{DD} $\overline{CE1}$ = V_{IH}, or CE2 = V_{IL}, or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}	Com. Ind. Auto.	-1 -2 -5	1 2 5	µA

Note:
1. V_{IL} (min.) = -0.3V DC; V_{IL} (min.) = -2.0V AC (pulse width -2.0 ns). Not 100% tested.
   V_{IH} (max.) = V_{DD} + 0.3V DC; V_{IH} (max.) = V_{DD} + 2.0V AC (pulse width -2.0 ns). Not 100% tested.

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POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	Test Conditions		-35 ns Min.	-35 ns Max.	-45 ns Min.	-45 ns Max.	Unit
I_{CC}	Average operating Current	$\overline{CE1}$ = V_{IL}, CE2 = V_{IH} V_{IN} = V_{IH} or V_{IL}, $I_{I/O}$= 0 mA, f=0	Com. Ind. Auto.	— —	25 30	 —	 35	mA
I_{CC1}	V_{DD} Dynamic Operating Supply Current	V_{DD} = Max., $\overline{CE1}$ = V_{IL} I_{OUT} = 0 mA, f = f_{MAX} V_{IN} = V_{IH} or V_{IL} CE2 = V_{IH}	Com. Ind. Auto. typ.[2]	— — —	30 35 20	 —	 40	mA
I_{SB1}	TTL Standby Current (TTL Inputs)	V_{DD} = Max., V_{IN} = V_{IH} or V_{IL}, $\overline{CE1}$ ≥ V_{IH}, or CE2 ≤ V_{IL}, f = 0	Com. Ind. Auto.	— —	1 1.5	 —	 2	mA
I_{SB2}	CMOS Standby Current (CMOS Inputs)	V_{DD} = Max., $\overline{CE1}$ ≥ V_{DD} – 0.2V, or CE2 ≤ 0.2V, V_{IN} ≥ V_{DD} – 0.2V, or V_{IN} ≤ V_{SS} + 0.2V, f = 0	Com. Ind. Auto. typ.[2]	— — —	5 10 4	 —	 45	µA

Note:
1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
2. Typical Values are measured at V_{DD} = 5V, T_A = 25°C and not 100% tested.

READ CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	-35 ns Min.	-35 ns Max.	-45 ns Min.	-45 ns Max.	Unit
t_{RC}	Read Cycle Time	35	—	45	—	ns
t_{AA}	Address Access Time	—	35	—	45	ns
t_{OHA}	Output Hold Time	3	—	3	—	ns
t_{ACE1}	$\overline{CE1}$ Access Time	—	35	—	45	ns
t_{ACE2}	CE2 Access Time	—	35	—	45	ns
t_{DOE}	$\overline{OE}$ Access Time	—	10	—	20	ns
t_{LZOE}[2]	$\overline{OE}$ to Low-Z Output	3	—	5	—	ns
t_{HZOE}[2]	$\overline{OE}$ to High-Z Output	0	10	0	15	ns
t_{LZCE1}[2]	$\overline{CE1}$ to Low-Z Output	3	—	5	—	ns
t_{LZCE2}[2]	CE2 to Low-Z Output	3	—	5	—	ns
t_{HZCE}[2]	$\overline{CE1}$ or CE2 to High-Z Output	0	10	0	15	ns

Notes:
1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0.6 to 2.4V and output loading specified in Figure 1a.
2. Tested with the load in Figure 1b. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

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AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0.6V to 2.4V
Input Rise and Fall Times	5 ns
Input and Output Timing and Reference Level	1.5V
Output Load	See Figures 1a and 1b

AC TEST LOADS

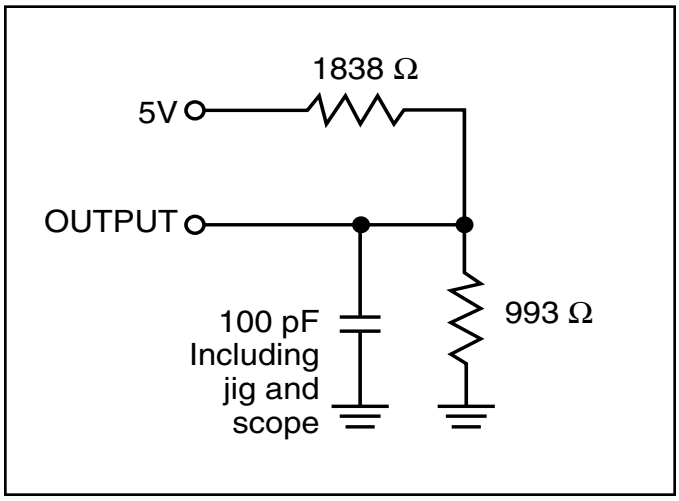


Figure 1a.

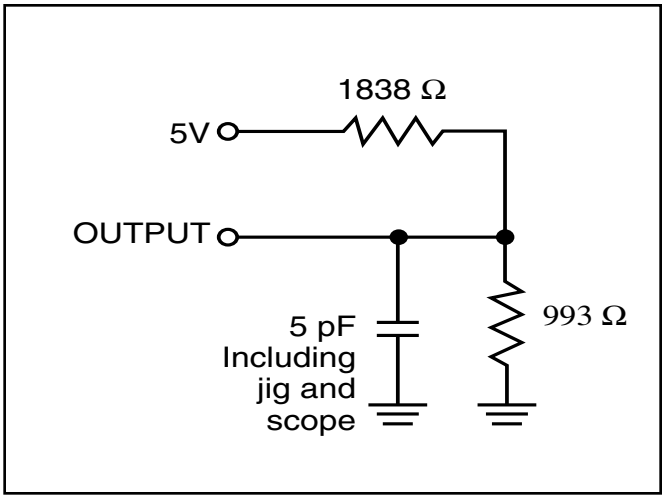
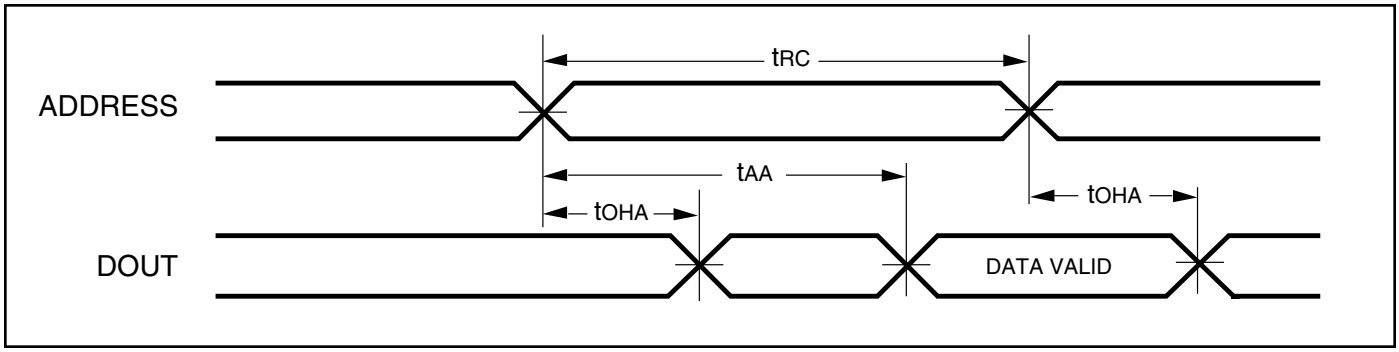


Figure 1b.

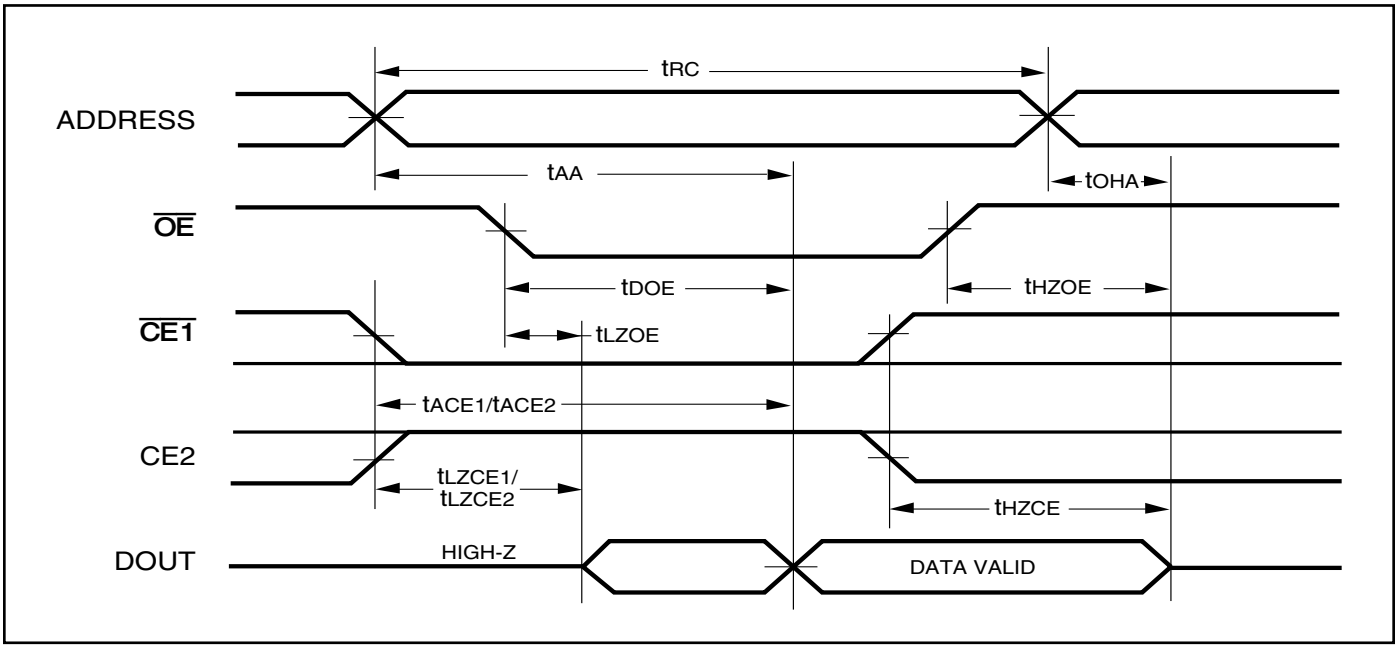
AC WAVEFORMS

READ CYCLE NO. 1[1,2]



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READ CYCLE NO. 2[1,3]



Notes:
1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CE1}$ = V_{IL}, CE2 = V_{IH}.
3. Address is valid prior to or coincident with $\overline{CE1}$ LOW and CE2 HIGH transitions.

WRITE CYCLE SWITCHING CHARACTERISTICS[1,3] (Over Operating Range, Standard and Low Power)

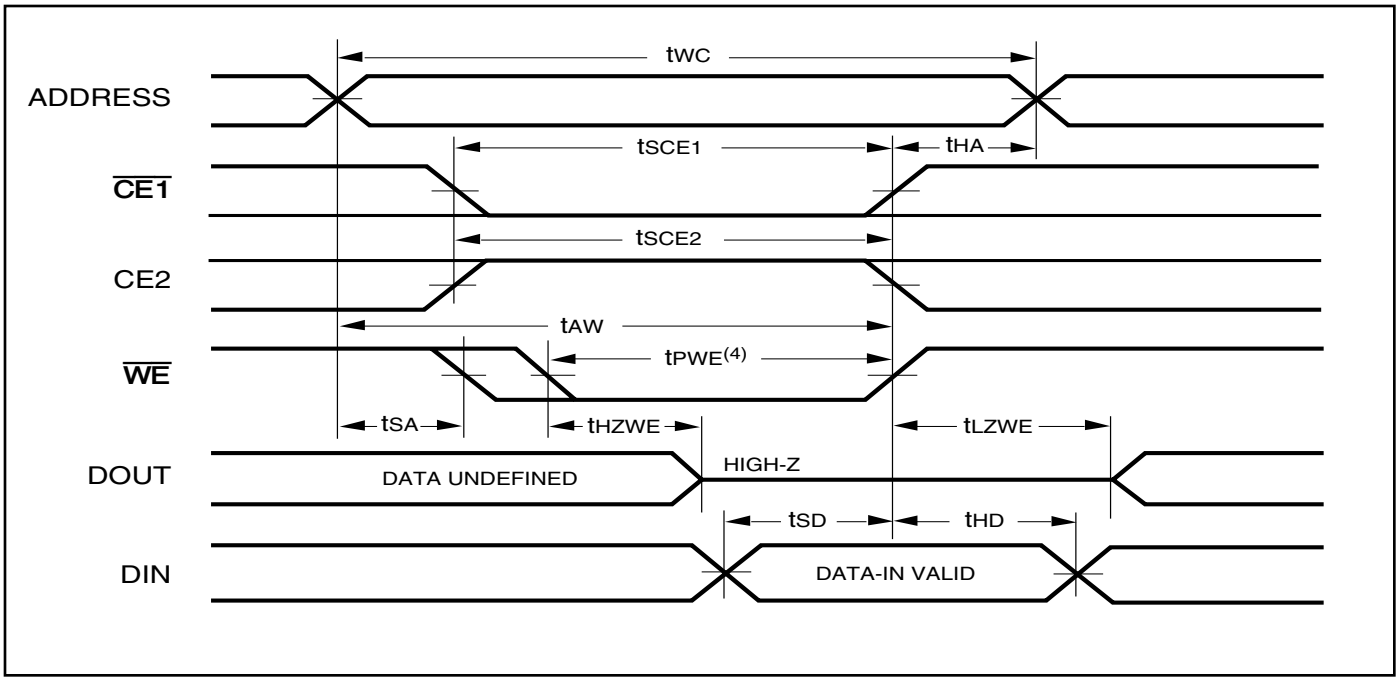
		-35 ns		-45 ns		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
t_{WC}	Write Cycle Time	35	—	45	—	ns
t_{SCE1}	$\overline{CE1}$ to Write End	25	—	35	—	ns
t_{SCE2}	CE2 to Write End	25	—	35	—	ns
t_{AW}	Address Setup Time to Write End	25	—	35	—	ns
t_{HA}	Address Hold from Write End	0	—	0	—	ns
t_{SA}	Address Setup Time	0	—	0	—	ns
t_{PWE}[4]	$\overline{WE}$ Pulse Width	25	—	35	—	ns
t_{SD}	Data Setup to Write End	20	—	25	—	ns
t_{HD}	Data Hold from Write End	0	—	0	—	ns
t_{HZWE}[2]	$\overline{WE}$ LOW to High-Z Output	—	10	—	15	ns
t_{LZWE}[2]	$\overline{WE}$ HIGH to Low-Z Output	3	—	5	—	ns

Notes:
1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0.6 to 2.4V and output loading specified in Figure 1a.
2. Tested with the load in Figure 1b. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of $\overline{CE1}$ LOW, CE2 HIGH and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
4. Tested with $\overline{OE}$ HIGH.

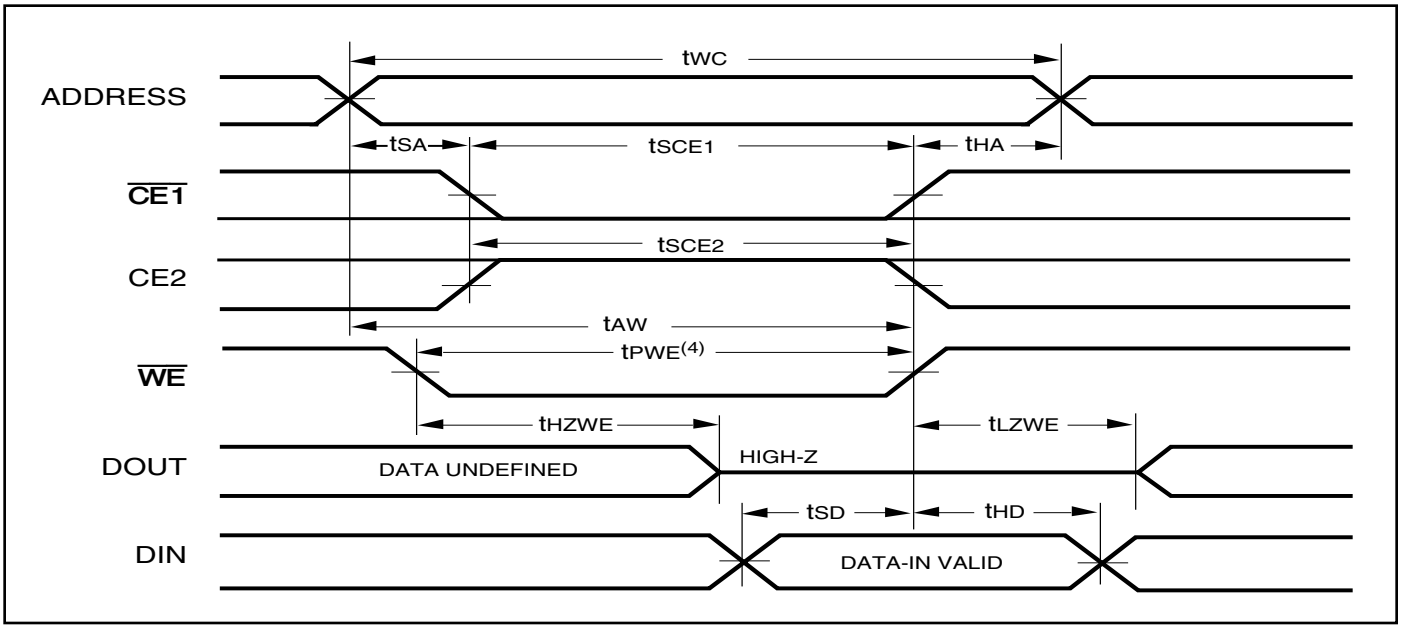
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AC WAVEFORMS

WRITE CYCLE NO. 1 ($\overline{WE}$ Controlled)[1,2]



WRITE CYCLE NO. 2 ($\overline{CE1}$, CE2 Controlled)[1,2]



Notes:
1. The internal write time is defined by the overlap of $\overline{CE1}$ LOW, CE2 HIGH and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High-Z state if $\overline{OE}$ = V_{IH}.

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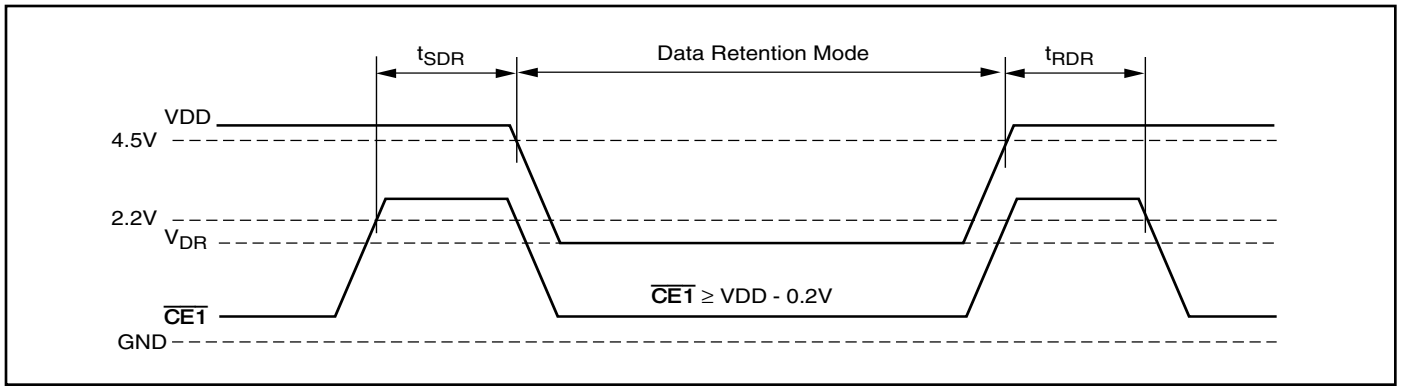
DATA RETENTION SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
V_{DR}	V_{DD} for Data Retention	See Data Retention Waveform		2.0		5.5	V
I_{DR}	Data Retention Current	V_{DD} = 2.0V, $\overline{CE1} \geq V_{DD} - 0.2V$	Com.	—	—	5	µA
		or CE2 ≤ 0.2V	Ind.	—	—	10	
		$V_{IN} \geq V_{DD} - 0.2V$, or $V_{IN} \leq V_{SS} + 0.2V$	Auto.	—	—	45	
t_{SDR}	Data Retention Setup Time	See Data Retention Waveform		0		—	ns
t_{RDR}	Recovery Time	See Data Retention Waveform		t_{RC}		—	ns

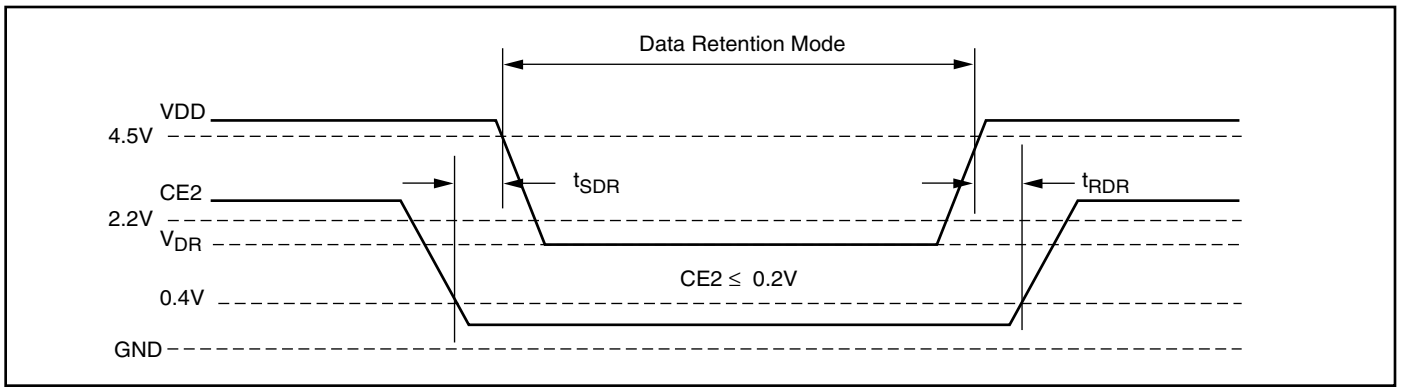
Note:

1. Typical Values are measured at V_{DD} = 5V, T_A = 25°C and not 100% tested.

DATA RETENTION WAVEFORM ($\overline{CE1}$ Controlled)



DATA RETENTION WAVEFORM (CE2 Controlled)



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Industrial Range: –40°C to +85°C

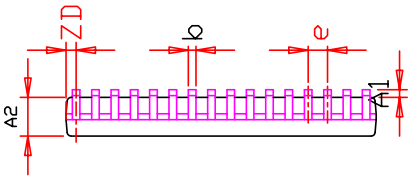
Speed (ns)	Order Part No.	Package
35	IS62C1024AL-35QLI	Plastic SOP, Lead-free
35	IS62C1024AL-35TLI	TSOP, Type 1, Lead-free

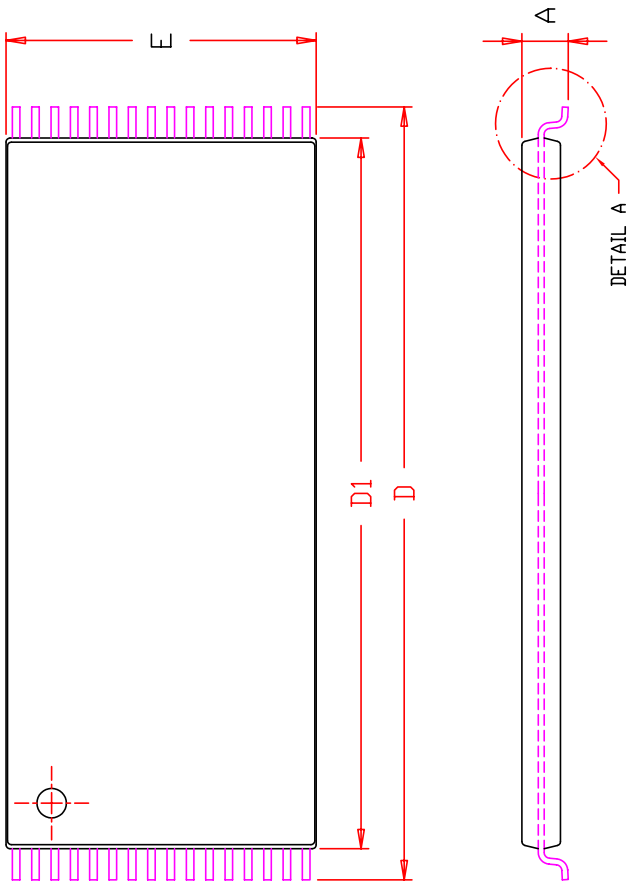
ORDERING INFORMATION: IS65C1024AL
Automotive Range: -40°C to +125°C

Speed (ns)	Order Part No.	Package
45	IS65C1024AL-45QLA3	Plastic SOP, Lead-free
45	IS65C1024AL-45TLA3	TSOP, Type 1, Lead-free

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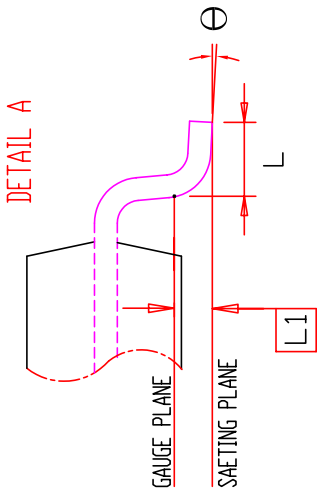
SYMBOL	DIMENSION IN MM		
	MIN	NOM	MAX
A	1.00	—	1.20
A1	0.05	—	0.20
A2	0.95	1.00	1.05
b	0.17	—	0.27
D	19.80	20.00	20.20
D1	18.30	18.40	18.50
E	7.80	8.00	8.20
e		0.50 BSC.	
L	0.40	—	0.70
L1		0.25 BSC.	
ZD		0.25 REF.	
θ	0	5°	8°





NOTE :

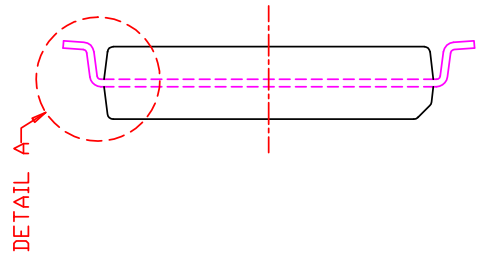
1. Controlling dimension : mm
2. Dimension D1 adn E do not include mold protrusion .
3. Dimension b does not include dambar protrusion/intrusion.
4. Formed leads shall be planar with respect to one another within 0.1mm at the seating plane after final test.

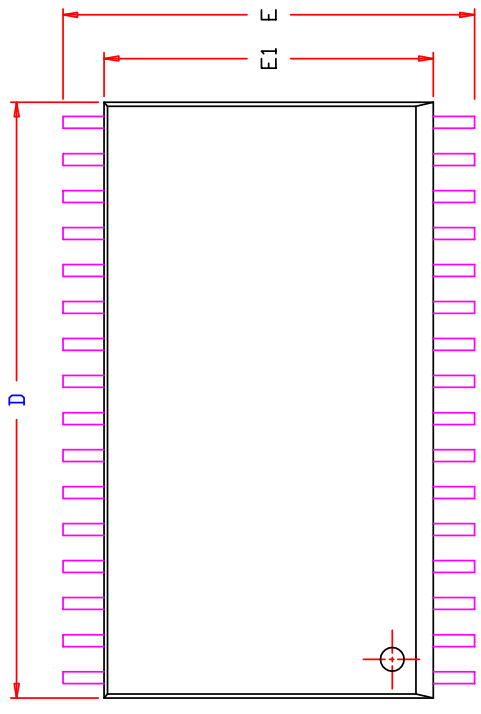


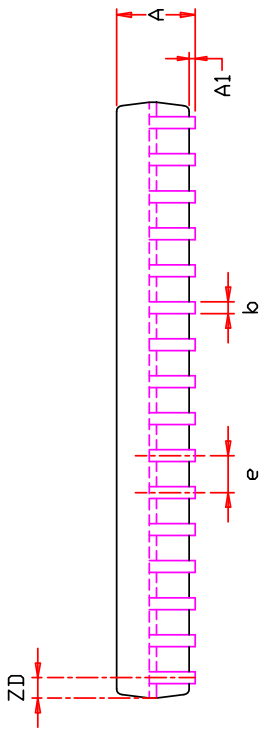
ISSI	TITLE	32L 8x20mm TSOP-1 Package Outline	REV.	E	DATE	06/08/2006

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SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	2.62	—	3.05	0.103	—	0.120
A1	0.05	—	0.30	0.002	—	0.012
b	0.33	—	0.51	0.013	—	0.020
D	20.24	—	20.75	0.797	—	0.817
E	13.79	—	14.45	0.543	—	0.569
E1	11.18	—	11.43	0.440	—	0.450
e	1.27 BSC.			0.050 BSC.		
L	0.38	—	1.27	0.015	—	0.050
L1	0.25 BSC.			0.010 BSC.		
ZD	0.725 REF.			0.029 REF.		
θ	0	—	8°	0	—	8°

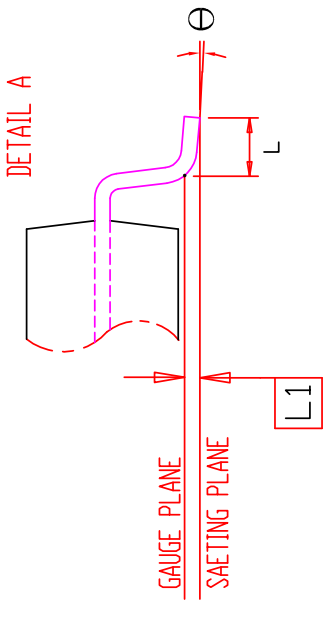






NOTE:

1. CONTROLLING DIMENSION : MM
2. DIMENSION D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.



	TITLE	REV.	DATE
ISSI	32L 450mil SOP Package Outline	F	09/23/2013

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