Advanced

GT24C512B

2-WIRE

512K Bits

Serial EEPROM

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1. Features

- Two-Wire Serial Interface, I²C™ Compatible
  - Bi-directional data transfer protocol
- Wide-voltage Operation
  - V_{CC} = 1.7V to 5.5V
- Speed: 1 MHz (1.7V)
- Standby current (max.): 1 μA, 1.7V
- Operating current (max.): 1 mA, 1.7V
- Hardware Data Protection
  - Write Protect Pin
- Sequential & Random Read Features
- Memory organization: 65,536 x 8 bits
- Page Size: 128 bytes
- Page write mode
  - Up to 128 bytes per page write
- Self timed write cycle with auto clear: 5ms (max.)
- Filtered inputs for noise suppression
- With ECC function
- ESD-HBM: 8000V
- High-reliability
  - Endurance: 4 million cycles
  - Data retention: 100 years
- Industrial temperature grades
- Packages: SOIC 150mil/208mil, TSSOP and UDFN
- Lead-free, RoHS, Halogen free, Green

2. General Description

The GT24C512B are EEPROM devices that use the industrial standard 2-wire interface for communications. The GT24C512B contains a memory array of 512K-bits (65,536x8), which is organized in 128-byte per page.

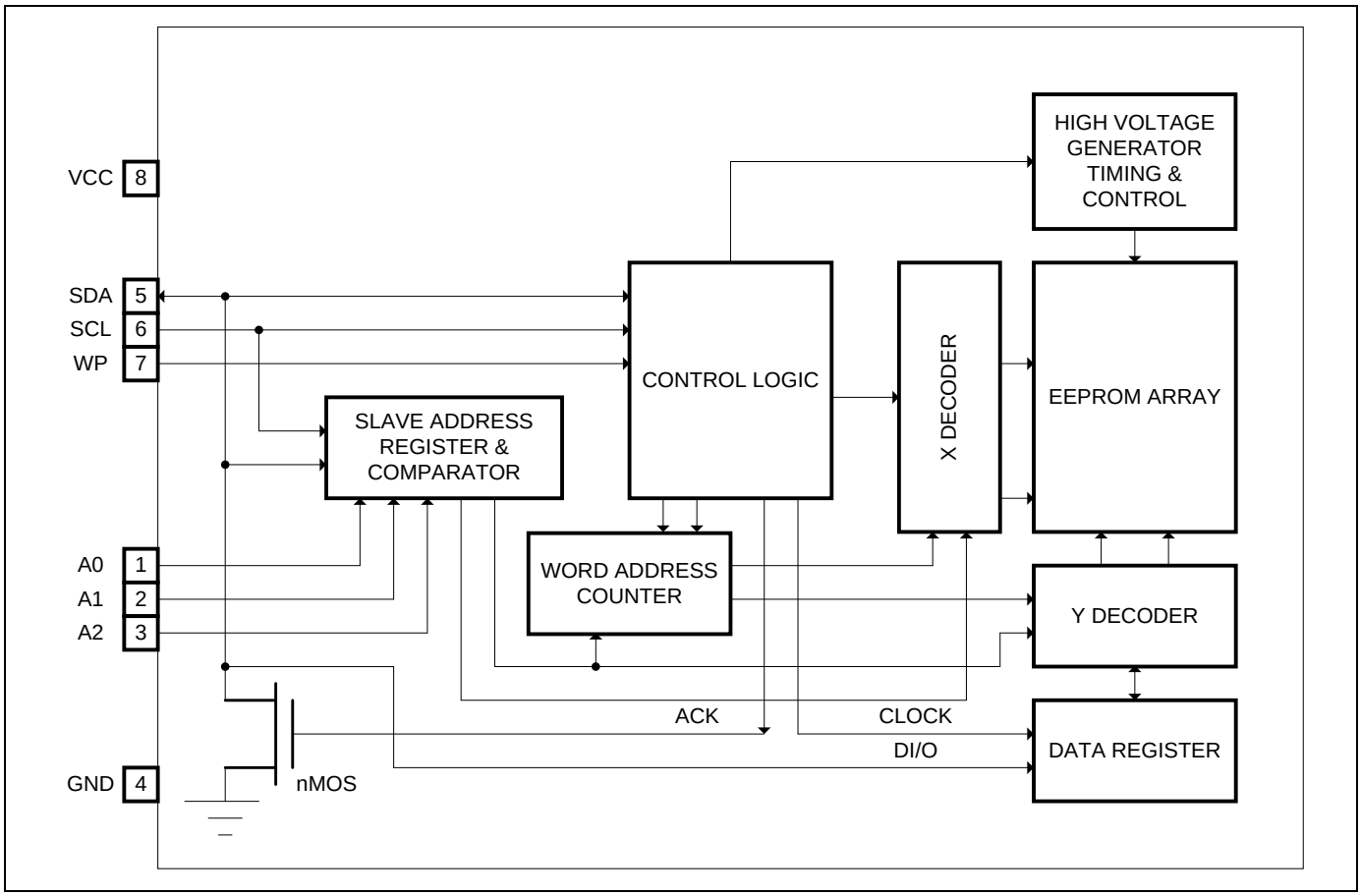
The EEPROM can operate in a wide voltage range from 1.7V to 5.5V which fits most application. This product can provide a low-power 2-wire EEPROM solution. The device is offered in Lead-free, RoHS, halogen free or Green. The available package types are 8-pin SOIC 150mil/208mil, TSSOP and UDFN.

The GT24C512B is compatible with the industrial standard 2-wire bus protocol. If in case the bus is not responded, a new sent Op-code command will reset the bus and the device will respond correctly. The simple bus consists of the Serial Clock wire (SCL) and the Serial Data wire (SDA). Utilizing such bus protocol, a Master device, such as a microcontroller, can usually control one or more Slave devices, alike this GT24C512B. The bit stream over the SDA line includes a series of bytes, which identifies a particular Slave device, an instruction, an address within that Slave device, and a series of data, if appropriate. The GT24C512B also has a Write Protect pin (WP) to allow blocking any write operations over specified memory area.

Under no circumstance, the device will be hung up. In order to refrain the state machine entering into a wrong state during power-up sequence or a power toggle off-on condition, a power on reset circuit is embedded. During power-up, the device does not respond to any instructions until the supply voltage (V_{CC}) has reached an acceptable stable level above the reset threshold voltage. Once V_{CC} passes the power on reset threshold, the device is reset and enters into the Standby mode. This would also avoid any inadvertent Write operations during power-up stage. During power-down process, the device will enter into standby mode, once V_{CC} drops below the power on reset threshold voltage. In addition, the device will be in standby mode after receiving the Stop command, provided that no internal write operation is in progress. Nevertheless, it is illegal to send a command unless the V_{CC} is within its operating level.

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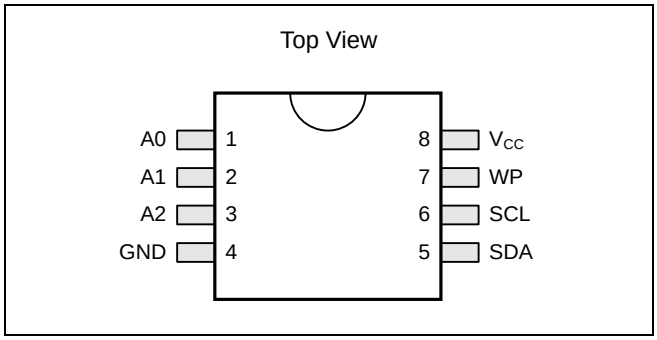
3. Functional Block Diagram



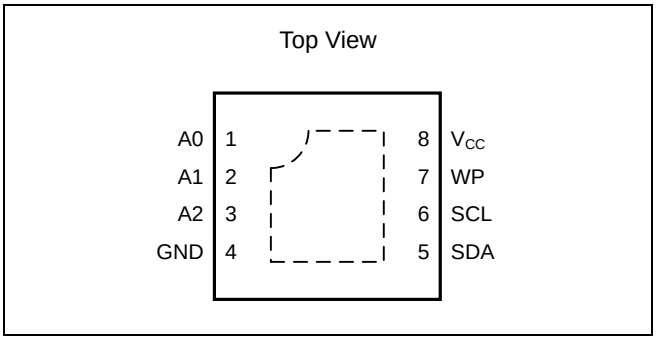
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4. Pin Configuration

4.1 8-Pin SOIC, TSSOP



4.2 8-Lead UDFN



4.3 Pin Definition

Pin No.	Pin Name	I/O	Definition
1	A0	I	Device Address Input
2	A1	I	Device Address Input
3	A2	I	Device Address Input
4	GND	-	Ground
5	SDA	I/O	Serial Address and Data input and Data out put
6	SCL	I	Serial Clock Input
7	WP	I	Write Protect Input
8	V_{CC}	-	Power Supply

4.4 Pin Descriptions

SCL

This input clock pin is used to synchronize the data transfer to and from the device.

SDA

The SDA is a bi-directional pin used to transfer addresses and data into and out of the device. The SDA pin is an open drain output and can be wired with other open drain or open collector outputs. However, the SDA pin requires a pull-up resistor connected to the power supply.

A0, A1, A2

The A0, A1 and A2 are the device address inputs.

Typically, the A0, A1, and A2 pins are for hardware addressing and a total of 8 devices can be connected on a single bus system. When A0, A1, and A2 are left floating, the inputs are defaulted to zero.

WP

WP is the Write Protect pin. While the WP pin is connected to the power supply of GT24C512B, the entire array becomes Write Protected (i.e. the device becomes Read only). When WP is tied to Ground or left floating, the normal write operations are allowed.

Note: WP cannot be powered on earlier than Vcc, and the amplitude of WP cannot be greater than Vcc.

V_{CC}

Supply voltage

GND

Ground of supply voltage

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5. Device Operation

The GT24C512B serial interface supports communications using industrial standard 2-wire bus protocol, such as I^2C.

5.1 2-WIRE Bus

The two-wire bus is defined as Serial Data (SDA), and Serial Clock (SCL). The protocol defines any device that sends data onto the SDA bus as a transmitter, and the receiving devices as receivers. The bus is controlled by Master device that generates the SCL, controls the bus access, and generates the Start and Stop conditions. The GT24C512B is the Slave device.

5.2 The Bus Protocol

Data transfer may be initiated only when the bus is not busy.

During a data transfer, the SDA line must remain stable whenever the SCL line is high. Any changes in the SDA line while the SCL line is high will be interpreted as a Start or Stop condition.

The state of the SDA line represents valid data after a Start condition. The SDA line must be stable for the duration of the High period of the clock signal. The data on the SDA line may be changed during the Low period of the clock signal. There is one clock pulse per bit of data. Each data transfer is initiated with a Start condition and terminated by a Stop condition.

5.3 Start Condition

The Start condition precedes all commands to the device and is defined as a High to Low transition of SDA when SCL is High. The EEPROM monitors the SDA and SCL lines and will not respond until the Start condition is met.

5.4 Stop Condition

The Stop condition is defined as a Low to High transition of SDA when SCL is High. All operations must end with a Stop condition.

5.5 Acknowledge

After a successful data transfer, each receiving device is required to generate an ACK. The Acknowledging device pulls down the SDA line.

5.6 Reset

The GT24C512B contains a reset function in case the 2-wire bus transmission on is accidentally interrupted (e.g. a power loss), or needs to be terminated mid-stream. The reset is initiated when the Master device creates a Start condition. To do this, it may be necessary for the Master device to monitor the SDA line while cycling the SCL up to nine times. (For each clock signal transition to High, the Master checks for a High level on SDA.)

5.7 Standby Mode

While in standby mode, the power consumption is minimal. The GT24C512B enters into standby mode during one of the following conditions: a) After Power-up, while no Op-code is sent; b) After the completion of an operation and followed by the Stop signal, provided that the previous operation is not Write related; or c) After the completion of any internal write operations.

5.8 Device Addressing

The Master begins a transmission on by sending a Start condition, then sends the address of the particular Slave devices to be communicated. The Slave device address is 8 bits format as shown in Figure. 5-5.

The four most significant bits of the Slave address are fixed (1010) for GT24C512B.

The next three bits, A0, A1 and A2, of the Slave address are specifically related to EEPROM. Up to eight GT24C512B units can be connected to the 2-wire bus.

The last bit of the Slave address specifies whether a Read or Write operation is to be performed. When this bit is set to 1, Read operation is selected. While it is set to 0, Write operation is selected.

After the Master transmits the Start condition and Slave address byte appropriately, the associated 2-wire Slave device, GT24C512B, will respond with ACK on the SDA line. Then GT24C512B will pull down the SDA on the ninth clock cycle, signaling that it received the eight bits of data.

The GT24C512B then prepares for a Read or Write operation by monitoring the bus.

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5.9 Write Operation

5.9.1 Byte Write

In the Byte Write mode, the Master device sends the Start condition and the Slave address information (with the R/W set to Zero) to the Slave device. After the Slave generates an ACK, the Master sends the byte address that is to be written into the address pointer of the GT24C512B. After receiving another ACK from the Slave, the Master device transmits the data byte to be written into the address memory location. The GT24C512B acknowledges once more and the Master generates the Stop condition, at which time the device begins its internal programming cycle. While this internal cycle is in progress, the device will not respond to any request from the Master device.

5.9.2 Page Write

The GT24C512B is capable of 128-byte Page-Write operation. A Page-Write is initiated in the same manner as a Byte Write, but instead of terminating the internal Write cycle after the first data word is transferred, the Master device can transmit up to 127 more bytes. After the receipt of each data word, the EEPROM responds immediately with an ACK on SDA line, and the seven lower order data word address bits are internally incremented by one, while the higher order bits of the data word address remain constant. If a byte address is incremented from the last byte of a page, it returns to the first byte of that page. If the Master device should transmit more than 128 bytes prior to issuing the Stop condition, the address counter will “roll over,” and the previously written data will be overwritten. Once all 128 bytes are received and the Stop condition has been sent by the Master, the internal programming cycle begins. At this point, all received data is written to the GT24C512B in a single Write cycle. All inputs are disabled until completion of the internal Write cycle.

5.9.3 Acknowledge (ACK) Polling

The disabling of the inputs can be used to take advantage of the typical Write cycle time. Once the Stop condition is issued to indicate the end of the host's Write operation, the GT24C512B initiates the internal Write cycle. ACK polling can be initiated immediately. This involves issuing the Start condition followed by the Slave address for a Write operation. If the EEPROM is still busy with the Write operation, no ACK will be returned. If the GT24C512B has completed the Write operation, an ACK will be returned and the host can then proceed with the next Read or Write operation.

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5.10 Read Operation

Read operations are initiated in the same manner as Write operations, except that the (R/W) bit of the Slave address is set to “1”. There are three Read operation options: current address read, random address read and sequential read.

5.10.1 Current Address Read

The GT24C512B contains an internal address counter which maintains the address of the last byte accessed, incremented by one. When the EEPROM receives the Slave Addressing Byte with a Read operation (R/W bit set to “1”), it will respond an ACK and transmit the 8-bit data byte stored at address location n+1. The Master should not acknowledge the transfer but should generate a Stop condition so the GT24C512B discontinues transmission. The address “roll over” during read is from the last byte of the last memory page, to the first byte of the first page. The address “roll over” during write is from the last byte of the current page to the first byte of the same page. (Refer to Figure 5-8. Current Address Read Diagram.)

5.10.2 Random Address Read

Selective Read operations allow the Master device to select at random any memory location for a Read operation. The Master device first performs a 'dummy' Write operation by sending the Start condition, Slave address and byte address of the location it wishes to read. After the GT24C512B acknowledges the byte address, the Master device resends the Start condition and the Slave address, this time with the R/W bit set to one. The EEPROM then responds with its ACK and sends the data requested. The Master device does not send an ACK but will generate a Stop condition. (Refer to Figure 5-9. Random Address Read Diagram.)

5.10.3 Sequential Read

Sequential Reads can be initiated as either a Current Address Read or Random Address Read. After the GT24C512B sends the initial byte sequence, the Master device now responds with an ACK indicating it requires additional data from the GT24C512B. The EEPROM continues to output data for each ACK received. The Master device terminates the sequential Read operation by pulling SDA High (no ACK) indicating the last data word to be read, followed by a Stop condition. The data output is sequential, with the data from address n followed by the data from address n+1,n+2 ... etc. The address counter increments by one automatically, allowing the entire memory contents to be serially read during sequential Read operation. When the memory address boundary of the array is reached, the address counter “rolls over” to address 0, and the device continues to output data. (Refer to Figure 5-10. Sequential Read Diagram).

5.11 ECC (Error Correction Code) and Write cycling

The Error Correction Code (ECC) is an internal logic function which is transparent for the I2C communication protocol.

The ECC logic is implemented on each group of four EEPROM bytes [1]. Inside a group, if a single bit out of the four bytes happens to be erroneous during a Read operation, the ECC detects this bit and replaces it with the correct value. The read reliability is therefore much improved.

Even if the ECC function is performed on groups of four bytes, a single byte can be written independently. In this case, the ECC function also writes the three other bytes located in the same group [1]. As a consequence, the maximum cycling budget is defined at group level and the cycling can be distributed over the 4 bytes of the group: the sum of the cycles seen by byte0, byte1, byte2 and byte3 of the same group must remain below the maximum value defined in 6.4 Reliability.

Note: 1. A group of four bytes is located at addresses [4*N, 4*N+1, 4*N+2, 4*N+3], where N is an integer.

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5.12 Diagrams

Figure 5-1. Typical System Bus Configuration

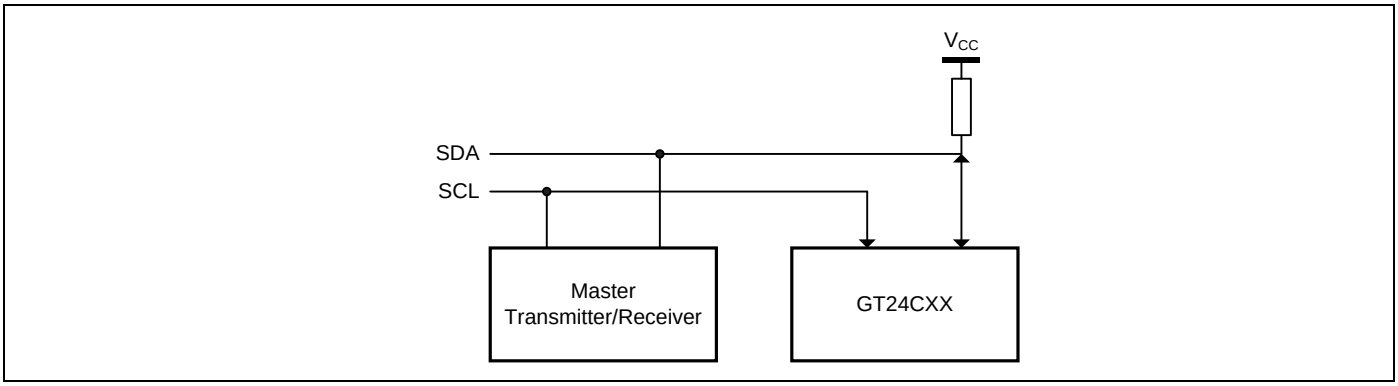


Figure 5-2. output Acknowledge

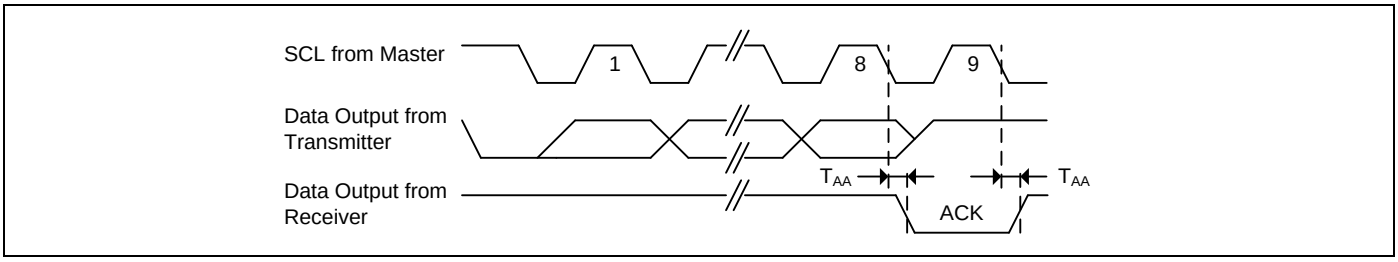
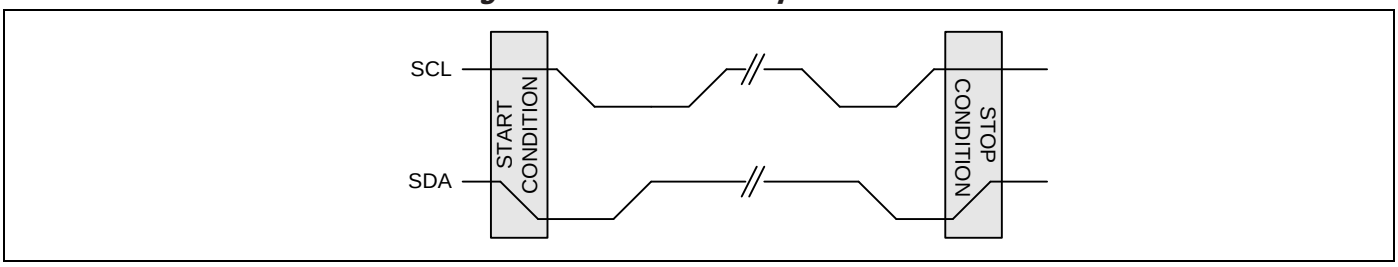


Figure 5-3. Start and Stop Conditions



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Figure 5-4. Data Validity Protocol

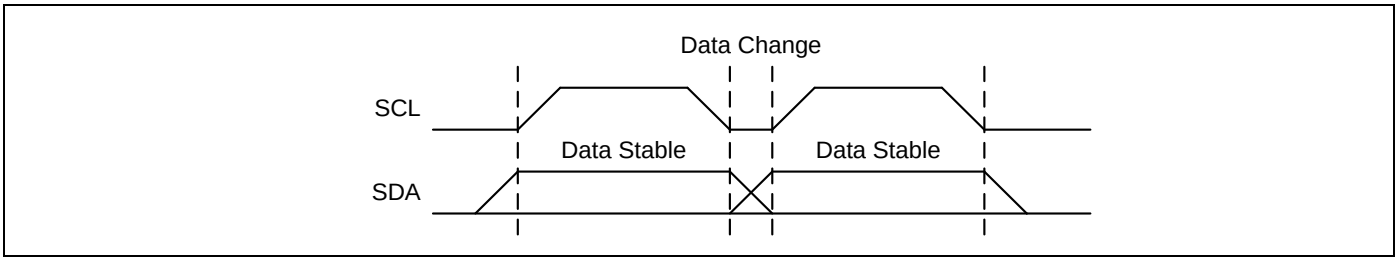


Figure 5-5. Slave Address

Bit	7	6	5	4	3	2	1	0
	1	0	1	0	A2	A1	A0	R/$\overline{W}$

Figure 5-6. Byte Write

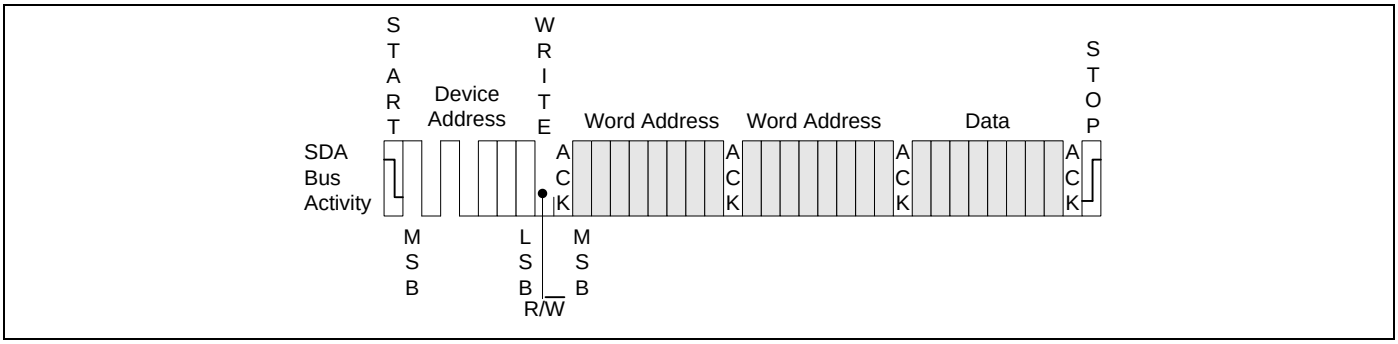
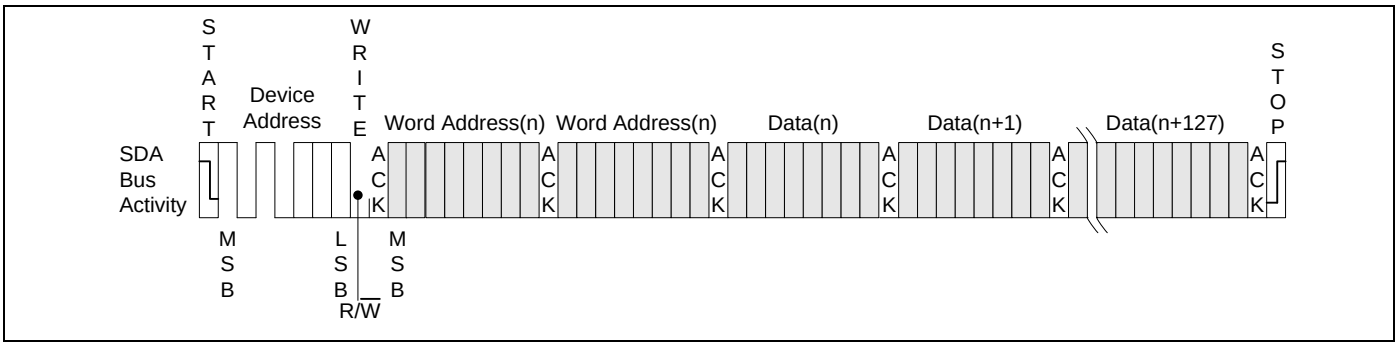


Figure 5-7. Page Write



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Figure 5-8. Current Address Read

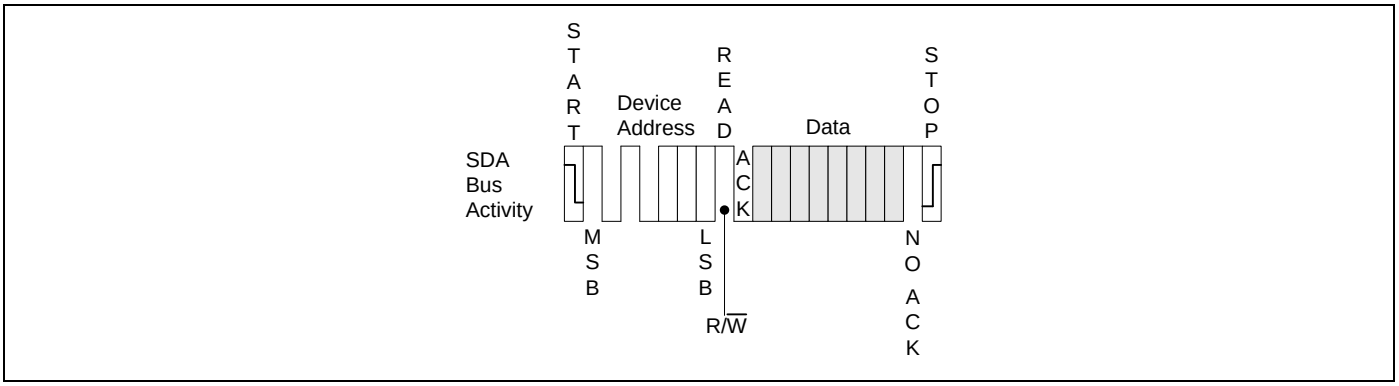


Figure 5-9. Random Address Read

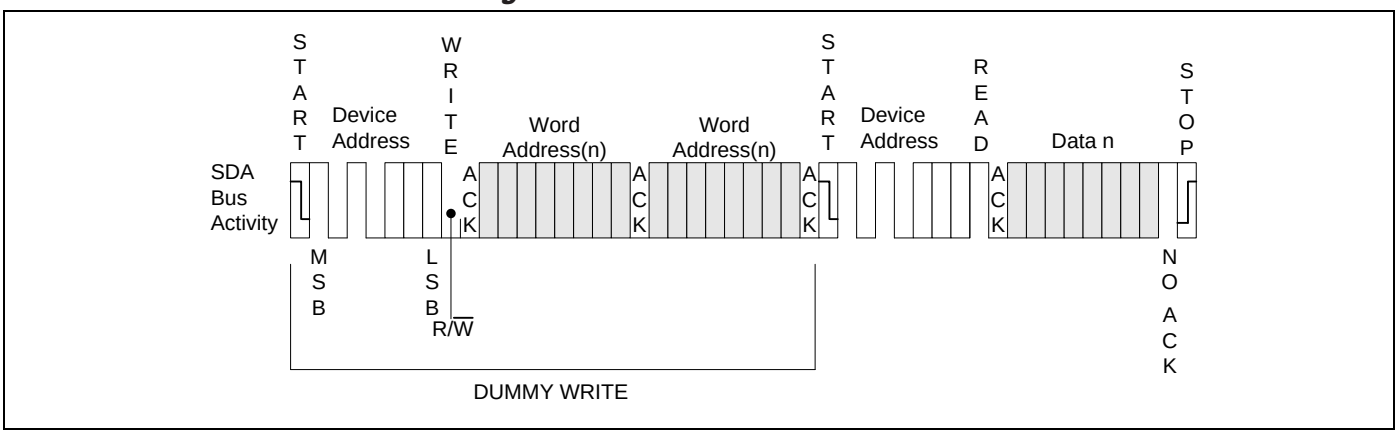
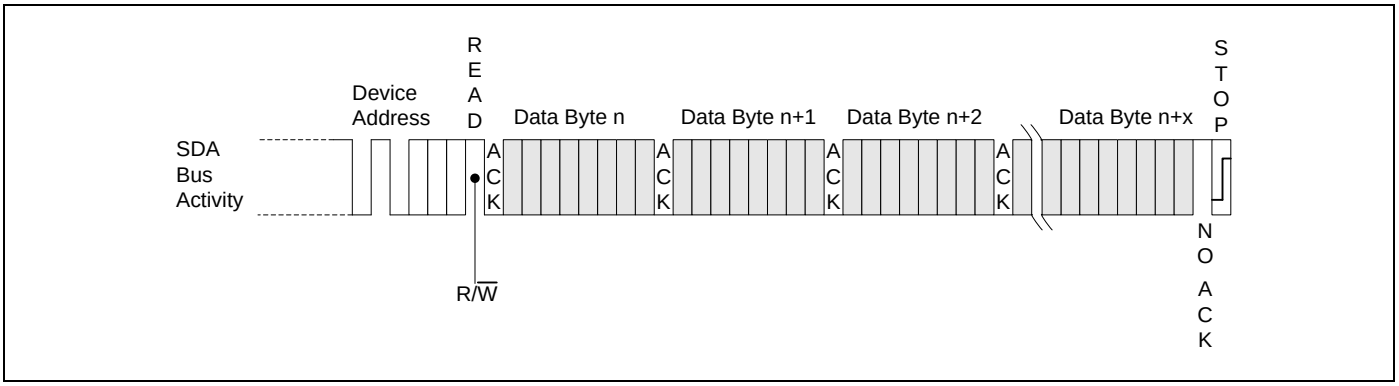


Figure 5-10. Sequential Read



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5.12 Timing Diagrams

Figure 5-11. Bus Timing

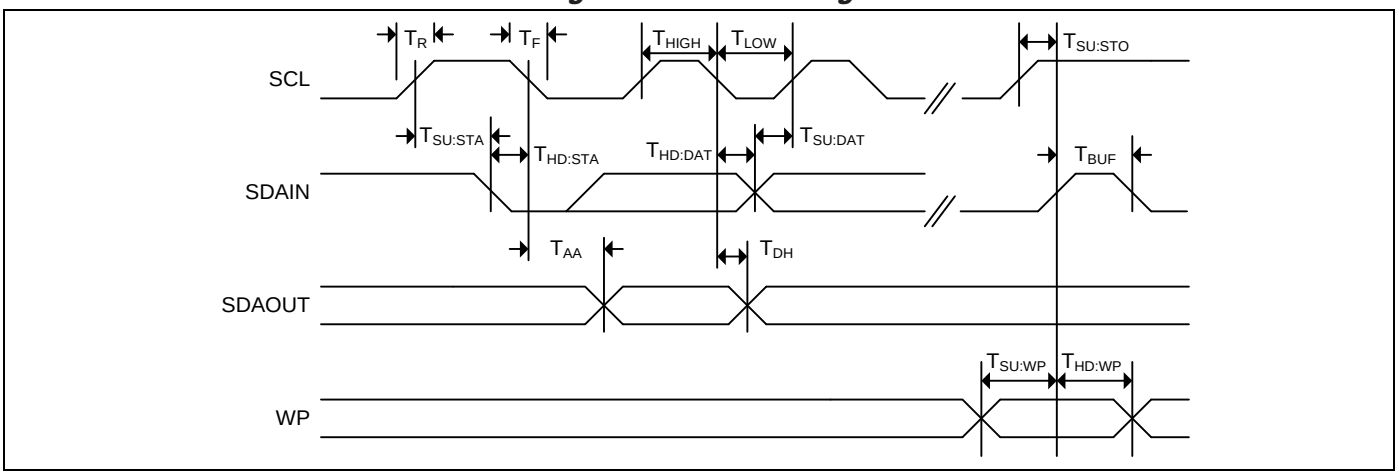
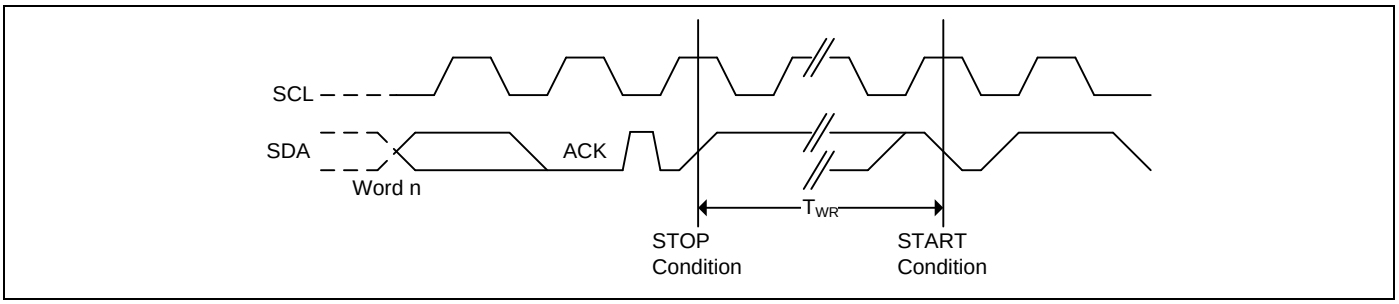


Figure 5-12. Write Cycle Timing



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6. Electrical Characteristics

6.1 Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	-0.5 to V_{CC} + 1	V
V_P	Voltage on Any Pin	–0.5 to V_{CC} + 1	V
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–65 to +150	°C
I_{OUT}	Output Current	5	mA

Note: Stress greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

6.2 Operating Range

Range	Ambient Temperature (T_A)	V_{CC}
Industrial	–40°C to +85°C	1.7V to 5.5V

Note: Giantec offers Industrial grade for Commercial applications (0°C to +70°C).

6.3 Capacitance

Symbol	Parameter[1, 2]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
$C_{I/O}$	Input / Output Capacitance	$V_{I/O}$ = 0V	8	pF

Notes: [1] Tested initially and after any design or process changes that may affect these parameters and not 100% tested.

[2] Test conditions: T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V.

6.4 Reliability

Ambient Temperature (TA)	Symbol	Parameter	Min.	Unit
Ta=+25°C	End	Endurance	4 million	Program / Erase Cycles
	DR	Data Retention	100	Years

Note: [1] The write cycle endurance is defined for group of four bytes located at addresses [4*N, 4*N+1, 4*N+2, 4*N+3] where N is an integer. The Write cycle endurance is defined by characterization and qualification.

[2] A Write cycle is executed when either a Page Write or a Byte write instruction is decoded. When using the Byte Write or the Page Write, refer also to 5.11 ECC (Error Correction Code) and Write cycling.

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6.5 DC Electrical Characteristic

Industrial: T_A = –40°C to +85°C, V_{CC} = 1.7V ~ 5.5V

Symbol	Parameter[1]	Vcc	Test Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage			1.7		5.5	V
V_{IH}	Input High Voltage(WP and A0, A1, A2)			0.7*V_{CC}		V_{CC}+0.5	V
	Input High Voltage(SCL and SDA)			0.7*V_{CC}		V_{CC}+0.5	V
V_{IL}	Input Low Voltage			-0.5		0.3* V_{CC}	V
I_{LI}	Input Leakage Current	5 V	V_{IN} = V_{CC} max	--		2	μA
I_{LO}	Output Leakage Current	5V		--		2	μA
V_{OL1}	Output Low Voltage	1.7V	I_{OL} = 0.15 mA	—		0.2	V
V_{OL2}	Output Low Voltage	3V	I_{OL} = 2.1 mA	—		0.4	V
I_{SB1}	Standby Current	1.7V	V_{IN} = V_{CC} or GND	—	0.2	1	μA
I_{SB2}	Standby Current	5.5V	V_{IN} = V_{CC} or GND	—	0.5	1	μA
I_{CC1}	Read Current	1.7V	Read at 400KHz	—		0.5	mA
		5.5V	Read at 1 MHz			1.0	mA
I_{CC2}	Write Current	1.7V	Write at 400KHz			0.8	mA
			Write at 1 MHz	—		1.0	mA
		5.5V	Write at 1 MHz			1.2	mA

Note: The parameters are characterized but not 100% tested.

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6.5 AC Electrical Characteristic

Industrial: T_A = –40°C to +85°C, Supply voltage = 1.7V to 5.5V

Symbol	Parameter [1] [2]	1.7V≤V_{CC}<5.5V		1.7V≤V_{CC}<5.5V		Unit
		Min.	Max.	Min.	Max.	
F_{SCL}	SCK Clock Frequency		400		1000	KHz
T_{LOW}	Clock Low Period	1200	—	400	—	ns
T_{HIGH}	Clock High Period	600	—	400	—	ns
T_R	Rise Time (SCL and SDA)	—	300	—	300	ns
T_F	Fall Time (SCL and SDA)	—	300	—	100	ns
$T_{SU:STA}$	Start Condition Setup Time	600	—	200	—	ns
$T_{SU:STO}$	Stop Condition Setup Time	600	—	200	—	ns
$T_{HD:STA}$	Start Condition Hold Time	600	—	200	—	ns
$T_{SU:DAT}$	Data In Setup Time	100	—	40	—	ns
$T_{HD:DAT}$	Data In Hold Time	0	—	0	—	ns
T_{AA}	Clock to Output Access time (SCL Low to SDA Data Out Valid)	100	900	50	400	ns
T_{DH}	Data Out Hold Time (SCL Low to SDA Data Out Change)	100	—	50	—	ns
T_{WR}	Write Cycle Time	—	5	—	5	ms
T_{BUF}	Bus Free Time Before New Transmission	1000	—	400	—	ns
$T_{SU:WP}$	WP pin Setup Time	600	—	400		ns
$T_{HD:WP}$	WP pin Hold Time	1200	—	1200	—	ns
T	Noise Suppression Time	—	100	—	50	ns

Notes: [1] The parameters are characterized but not 100% tested.

[2] AC measurement conditions:

R_L (connects to V_{CC}): 1.3 kΩ (2.5V, 5.0V), 10 kΩ (1.7V)

C_L = 100 pF

Input pulse voltages: 0.3*V_{CC} to 0.7*V_{CC}

Input rise and fall times: ≤ 50 ns

Timing reference voltages: half V_{CC} level

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7. Ordering Information

Industrial Grade: -40°C to +85°C, Lead-free

Voltage Range	Part Number*	Package (8-pin)*
1.7V to 5.5V	GT24C512B-2GLI-TR	150-mil SOIC
	GT24C512B-2WLI-TR	208-mil SOIC
	GT24C512B-2ZLI-TR	3 x 4.4 mm TSSOP
	GT24C512B-2UDLI-TR	2 x 3 x 0.55 mm UDFN

*

1. Contact Giantec Sales Representatives for availability and other package information.
2. The product is packed in tape and reel “-TR” (4K per reel), except UDFN is 5K per reel.
3. Refer to Giantec website for related declaration document on lead free, RoHS, halogen free or Green, whichever is applicable.
4. Giantec offers Industrial grade for Commercial applications (0°C to +70°C).

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8. Top Markings

8.1 150-mil SOIC Package

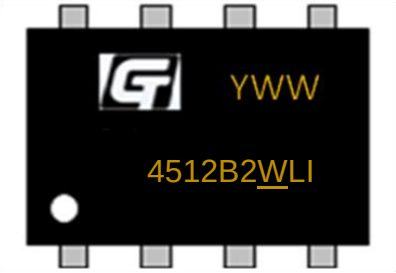


G: Giantec Logo

4512B2GLI: GT24C512B-2GLI-TR

YWW: Date Code, Y=year, WW=week

8.2 208-mil SOIC Package



G: Giantec Logo

4512B2WLI: GT24C512B-2WLI-TR

YWW: Date Code, Y=year, WW=week

8.3 TSSOP Package



GT: Giantec Logo

4512B2ZLI: GT24C512B-2ZLI-TR

YWW: Date Code, Y=year, WW=week

8.4 UDFN Package



GT: Giantec Logo

49B: GT24C512B-2UDLI-TR

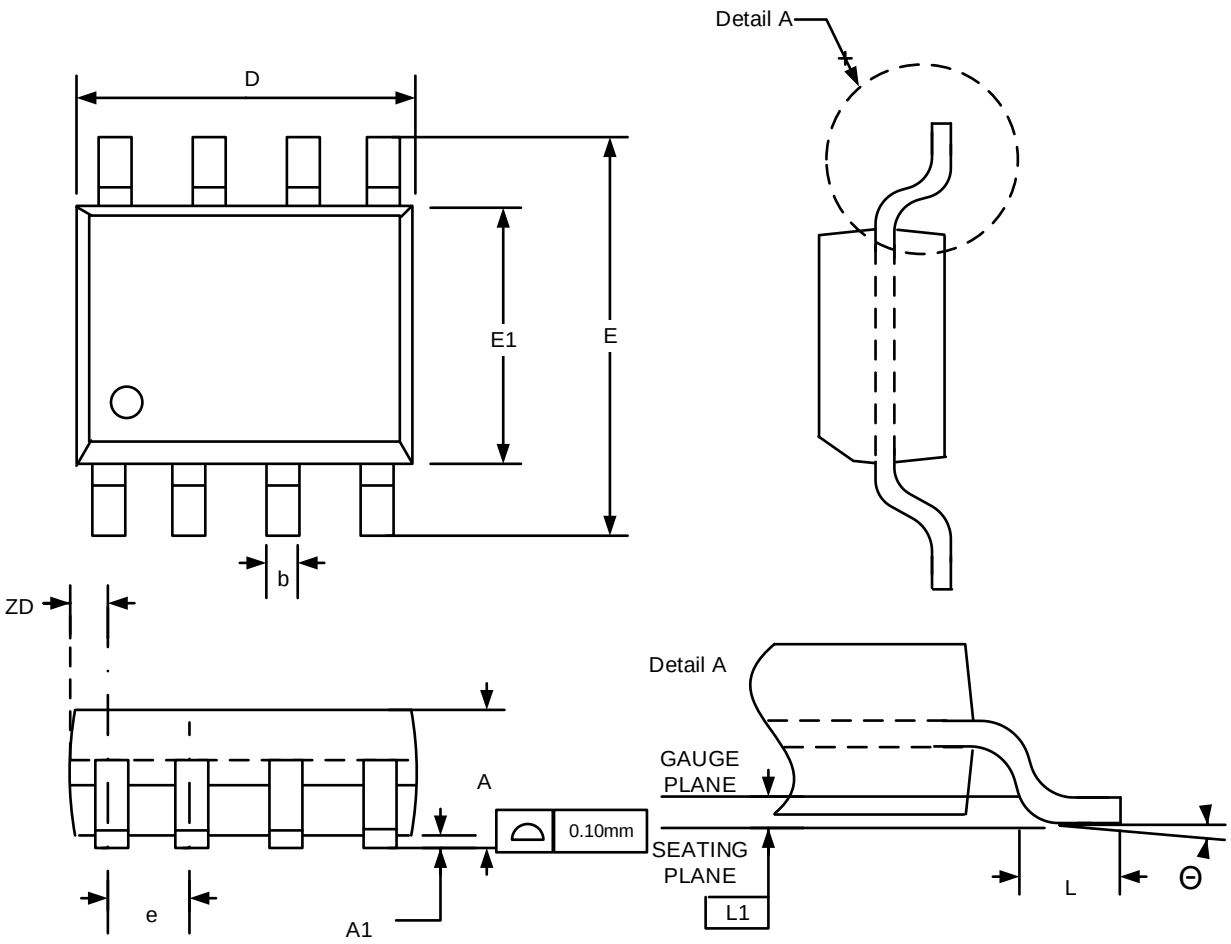
YWW: Date Code, Y=year, WW=week

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9. Package Information

9.1 150-mil SOIC

8L 150mil SOIC Package Outline



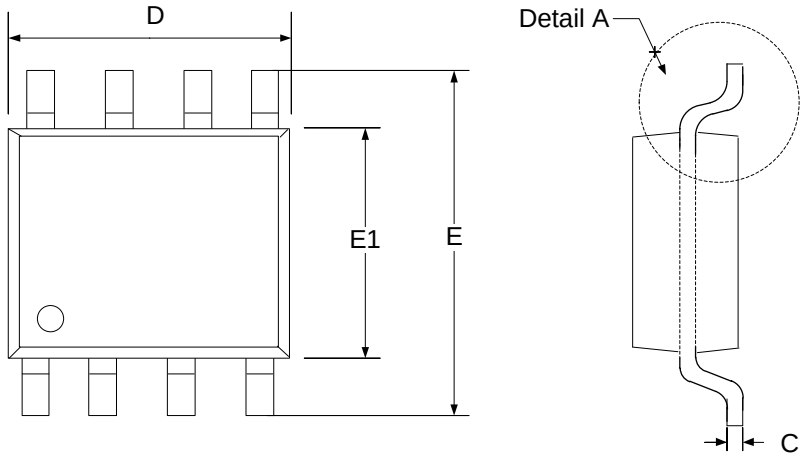
SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	--	1.75	0.053	--	0.069
A1	0.10	--	0.25	0.004	--	0.010
b	0.33	--	0.51	0.013	--	0.020
D	4.80	--	5.00	0.189	--	0.197
E	5.80	--	6.20	0.228	--	0.244
E1	3.80	--	4.00	0.150	--	0.157
e	1.27 BSC.			0.050 BSC.		
L	0.38	--	1.27	0.015		0.050
L1	0.25 BSC.			0.010 BSC.		
ZD	0.545 REF.			0.021 REF.		
Θ	0	--	8°	0	--	8°

Note:
1. Controlling Dimension:MM
2. Dimension D and E1 do not include Mold protrusion
3. Dimension b does not include dambar protrusion/intrusion.
4. Refer to Jedec standard MS-012
5. Drawing is not to scale

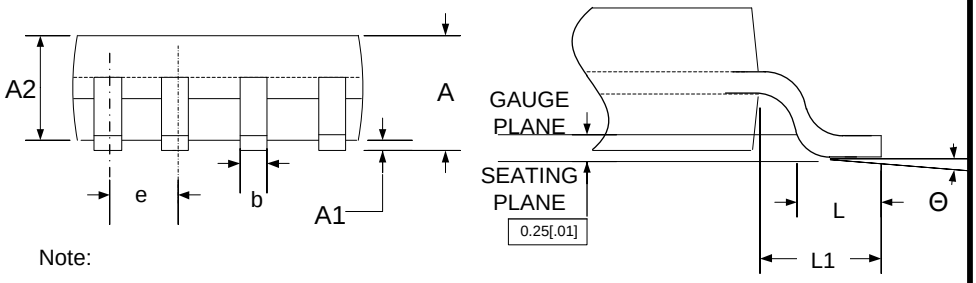
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9.2 208-mil SOIC

8L 208mil SOIC Package Outline



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	--	--	2.15	--	--	0.085
A1	0.05	--	0.25	0.002	--	0.010
A2	1.70	--	1.90	0.067	--	0.075
b	0.36	--	0.50	0.014	--	0.020
c	0.19	--	0.25	0.007	--	0.010
D	5.13	--	5.33	0.202	--	0.210
E	7.70	--	8.10	0.303	--	0.319
E1	5.18	--	5.38	0.204	--	0.212
e	1.27 BSC.			0.050 BSC.		
L	0.50	--	0.80	0.020	--	0.031
L1	1.21	--	1.41	0.048	--	0.056
Θ	0	--	8°	0	--	8°



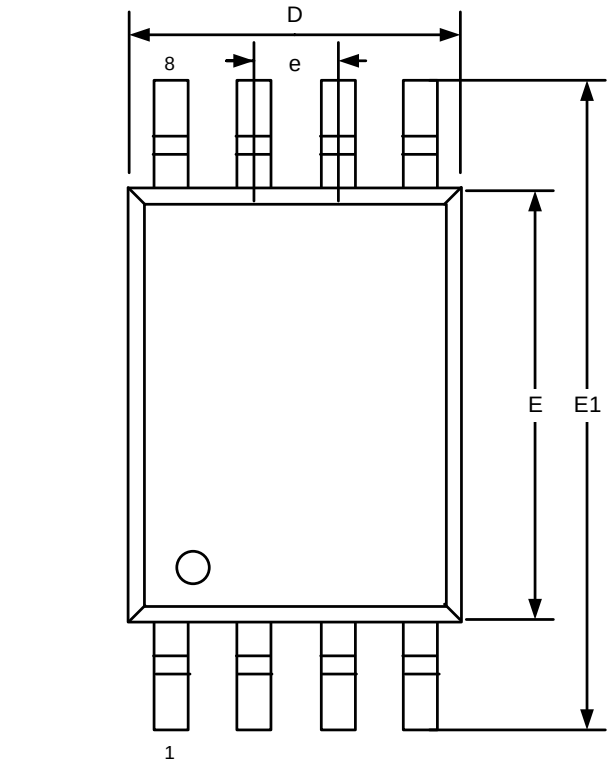
Note:

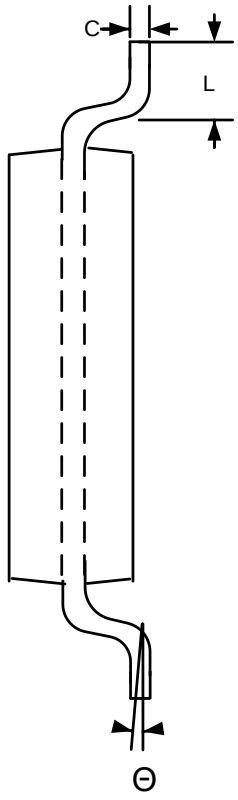
1. Controlling Dimension:MM
2. Dimension D and E1 do not include Mold protrusion
3. Dimension b does not include dambar protrusion/intrusion.
4. Refer to Jedec standard MS-012
5. Drawing is not to scale

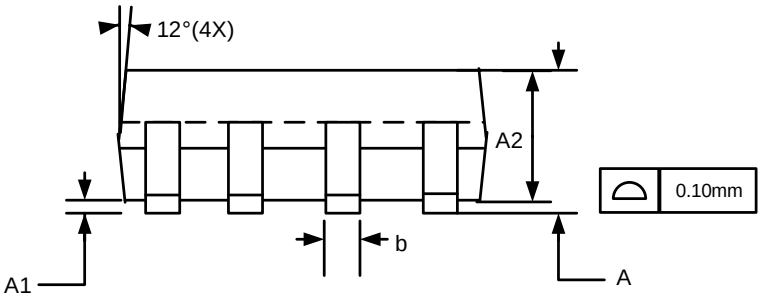
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9.3 TSSOP

8L 3x4.4mm TSSOP Package Outline







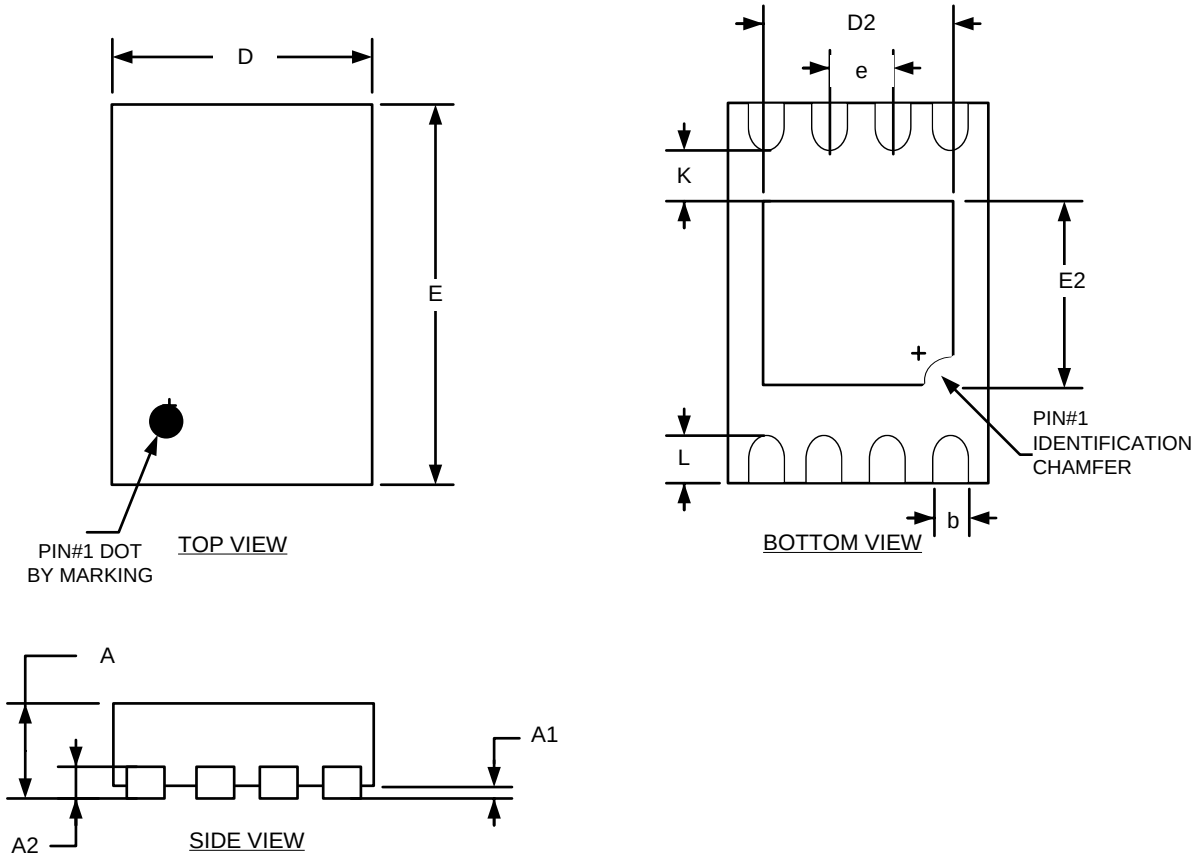
Note:
1. Controlling Dimension:MM
2. Dimension D and E do not include Mold protrusion
3. Dimension b does not include dambar protrusion/intrusion
4. Refer to Jedec standard MO-153 AA
5. Drawing is not to scale
6. Package may have exposed tie bar.

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	--	--	1.20	--	--	0.047
A1	0.05	--	0.15	0.002	--	0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19	--	0.30	0.007	--	0.012
c	0.09	--	0.20	0.004	--	0.008
D	2.90	3.00	3.10	0.114	0.118	0.122
E	4.30	4.40	4.50	0.169	0.173	0.177
E1	6.20	6.40	6.60	0.244	0.252	0.230
e		0.65 BSC			0.026 BSC	
L	0.45	0.60	0.75	0.018	0.024	0.030
Θ	0	--	8°	0	--	8°

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9.4 UDFN

8L 2x3mm UDFN Package Outline



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.50	0.55	0.60	0.020	0.022	0.024
A1	0.00	--	0.05	0.000	--	0.002
b	0.18	0.25	0.30	0.007	0.010	0.012
A2	0.152 REF			0.006 REF		
D	2.00 BSC			0.079 BSC		
D2	1.25	1.40	1.50	0.049	0.055	0.059
E	3.00 BSC			0.118 BSC		
E2	1.15	1.30	1.40	0.045	0.051	0.055
e	0.50 BSC.			0.020 BSC.		
K	0.40	--	--	0.016	--	--
L	0.20	0.30	0.40	0.008	0.012	0.016

Note:

1. Controlling Dimension:MM
2. Drawing is not to scale

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10. Revision History

Revision	Date	Descriptions
A0	Jul. 2016	Initial version
A1	Jan.2017	ECC updated
A2	May.2019	Optimize DC table power limit
A3	Jul. 2019	Update TSSOP POD and VIL in DC table
A4	Mar. 2020	Update VIHmax in DC table
A5	Mar. 2022	Add ESD data
A6	Jun.2022	Add AC Electrical Characteristic Notes
A7	Sep. 2022	Update Logo and other
A8	Dec. 2022	Add 208-mil SOIC package
A9	Oct. 2024	Update WP notes in section 4.5

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