GD9Fx4GxF3A
GD9Fx8GxE3A
GD9FxAGxD3A

DATASHEET

4G-bit/8G-bit/16G-bit 2K+64BPage Size

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1. FEATURES

- Single level cell technology
- ONFI 1.0 Compatible
- Power Supply Voltage
  - VCC/VCCQ = 1.7 ~ 1.95v(GD9FS)
  - VCC/VCCQ = 2.7 ~ 3.6v (GD9FU)
- Memory Cell Organization
  - Page size:
    X8: 2K + 64bytes
    X16: 1K + 32words
  - Block size: 64 pages
    X8: 128K + 4K bytes
    X16: 64K + 2K words
  - Plane size: 2048 blocks
  - Device size:
    4Gb: 4096 blocks
    8Gb: 8192 blocks
    16Gb: 16384 blocks
- Page Read / Program time
  - Random Read Time (tR): 25us Max.
  - Sequential Access Time
    3.3v Device: 20ns Min.
    1.8v Device:25ns Min.
  - Page Program(tPROG): 300us Typ.
- Block Erase
  - Block Erase Time(tBERS): 3ms Typ.
- Operating Current
  - Read(Typ): 15mA
  - Program(Typ): 15mA
  - Erase(Typ): 15mA
  - Standby(Max):50uA (CMOS)
- Reliability
  - P/E cycles with ECC: 100K
  - Data retention: 10 Years
- ECC Requirement
  - 4bit/512 bytes
- Operating Temperature
  - Industrial: -40C ~ 85C
  - Industrial: -40C ~ 105C
- Chip Enable Don't Care Option
- Security
  - OTP area
  - UID
- Package
  - TSOPI48 12mm x 20mm
  - FBGA63 9mm x 11mm

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2. GENERAL DESCRIPTION

GigaDevice GD9Fx4GxF3A/GD9Fx8GxE3A/GD9FxAGxD3A is 4Gbit/8Gbit/16Gbit capacity. A program operation can be performed in typical tPROG on the whole page and an erase operation can be performed in typical tBERS on each block. Data in the page can be read out at tRC cycle time per byte. The I/O pins serve as the ports for address and data input/output as well as command input. GD9Fx4GxF3A/GD9Fx8GxE3A/GD9FxAGxD3A provides extended reliability of 100K program/erase cycles with ECC (Error Correcting Code).

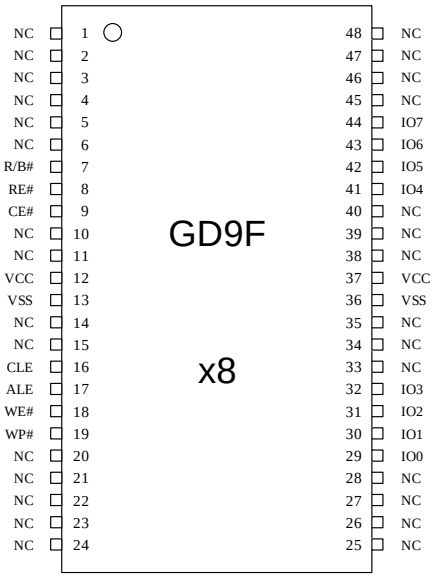
2.1 Product List

PART NUMBER	ORGANIZATION	VCC RANGE	PACKAGE
GD9FS4G8F3A	512M x 8bit	1.7v ~ 1.95v	TSOP48/ FBGA63
GD9FS4G6F3A	256M x 16bit	1.7v ~ 1.95v	TSOP48/ FBGA63
GD9FU4G8F3A	512M x 8bit	2.7v ~ 3.6v	TSOP48/ FBGA63
GD9FU4G6F3A	256M x 16bit	2.7v ~ 3.6v	TSOP48/ FBGA63
GD9FS8G8E3A	1G x 8bit	1.7v ~ 1.95v	TSOP48/ FBGA63
GD9FS8G6E3A	512M x 16bit	1.7v ~ 1.95v	TSOP48/ FBGA63
GD9FU8G8E3A	1G x 8bit	2.7v ~ 3.6v	TSOP48/ FBGA63
GD9FU8G6E3A	512M x 16bit	2.7v ~ 3.6v	TSOP48/ FBGA63
GD9FSAG8D3A	2G x 8bit	1.7v ~ 1.95v	TSOP48
GD9FSAG6D3A	1G x 16bit	1.7v ~ 1.95v	TSOP48
GD9FUAG8D3A	2G x 8bit	2.7v ~ 3.6v	TSOP48
GD9FUAG6D3A	1G x 16bit	2.7v ~ 3.6v	TSOP48

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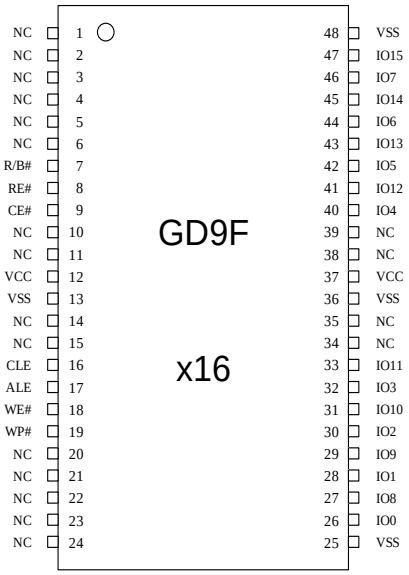
3. PACKAGE

3.1 TSOPI-48



TOP View

Figure3- 1-a: TSOP48 x8 device package figures



TOP View

Figure3- 1-b: TSOP48 x16 device package figures

3.2 FBGA-63

	1	2	3	4	5	6	7	8	9	10
A	NC	NC							NC	NC
B	NC								NC	NC
C			WP#	ALE	VSS	CE#	WE#	R/B#		
D			NC	RE#	CLE	NC	NC	NC		
E			NC	NC	NC	NC	NC	NC		
F			NC	NC	NC	NC	NC	NC		
G			NC	NC	NC	NC	NC	NC		
H			NC	IO0	NC	NC	NC	VCC		
J			NC	IO1	NC	VCC	IO5	IO7		
K			VSS	IO2	IO3	IO4	IO6	VSS		
L	NC	NC							NC	NC
M	NC	NC							NC	NC

TOP View

Figure3- 2_a: 63-FBGA x8 device ball location figures

	1	2	3	4	5	6	7	8	9	10
A	NC	NC							NC	NC
B	NC								NC	NC
C			WP#	ALE	VSS	CE#	WE#	R/B#		
D			NC	RE#	CLE	NC	NC	NC		
E			NC	NC	NC	NC	NC	NC		
F			NC	NC	NC	NC	NC	NC		
G			NC	NC	NC	IO13	IO15	NC		
H			IO8	IO0	IO10	IO12	IO14	VCC		
J			IO9	IO1	IO11	VCC	IO5	IO7		
K			VSS	IO2	IO3	IO4	IO6	VSS		
L	NC	NC							NC	NC
M	NC	NC							NC	NC

TOP View

Figure3- 2_b: 63-FBGA x16 device ball location figures

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4. BLOCK DIAGRAM

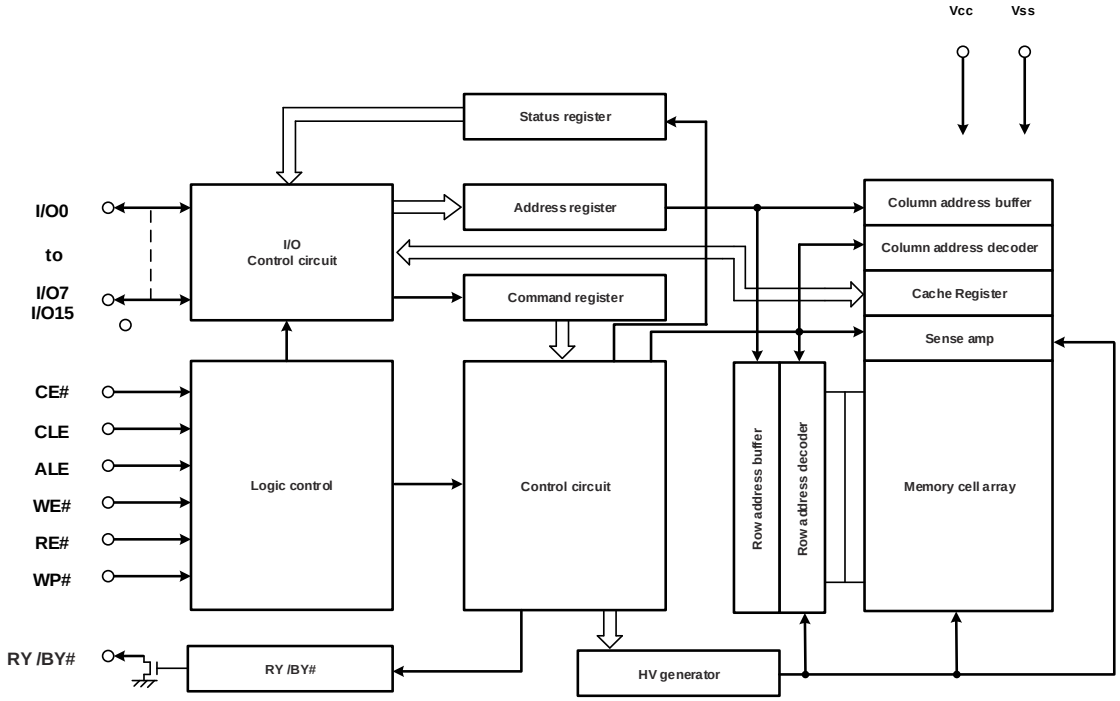


Figure 4-1: Block Diagram figures

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PIN DESCRIPTION

Signal Name	Input/ Output	Description
R/B#	**O**	Ready/Busy：Open drain output to indicate the target status, low to indicate that one or more operations are in progress.
RE#	**I**	Read Enable：Enables serial data output, active low.
CE#	**I**	Chip Enable：When high and the target is in the ready state, the target goes into a low-power standby state. When low, the target is selected.
CLE	**I**	Command Latch Enable：Enable signal to load a command into the target on the rising edge of WE#, active high.
ALE	**I**	Address Latch Enable：Enable signal to load an address into the target on the rising edge of WE#, active high.
WE#	**I**	Write Enable：Data, Commands, and Addresses are latched on the rising edge of WE#.
WP#	**I**	Write Protect：Low to disable Flash array program and erase operations.
IO0 ~ IO7	**I/O**	I/O Port, bits 0-7：8-bit wide bidirectional port for transferring address, command, and data to and from the device.
IO8 ~ IO15	**I/O**	I/O Port, bits 8-15：Upper 8 bits for the 16-bit wide bidirectional port used to transfer data to and from the device.
VCC	**I**	Power：Power supply to the device.
VSS	**I**	Ground：Power supply ground.
NC	**-**	No Connection：Lead is not internally connected.

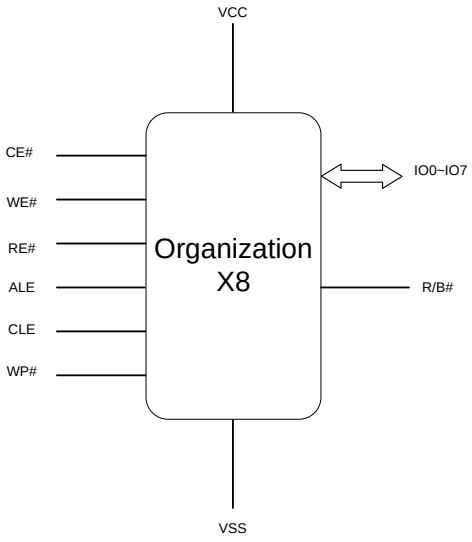


Figure 4-2_a: x8 device figures

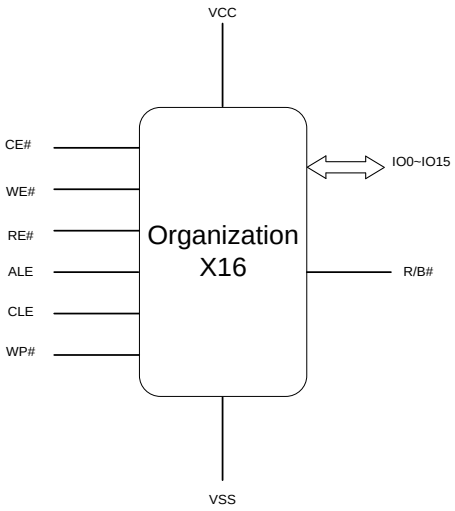


Figure 4-2_b: x16 device figures

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5. ARRAY ORGANIZATION

Each device has			Each block has	Each page has	
16Gb	8Gb	4Gb			
2G+64M	1G+32M	512M+16M	128K+4K	2K+64	bytes
16384x 64	8192 x 64	4096 x 64	64	-	pages
16384	8192	4096	-	-	blocks

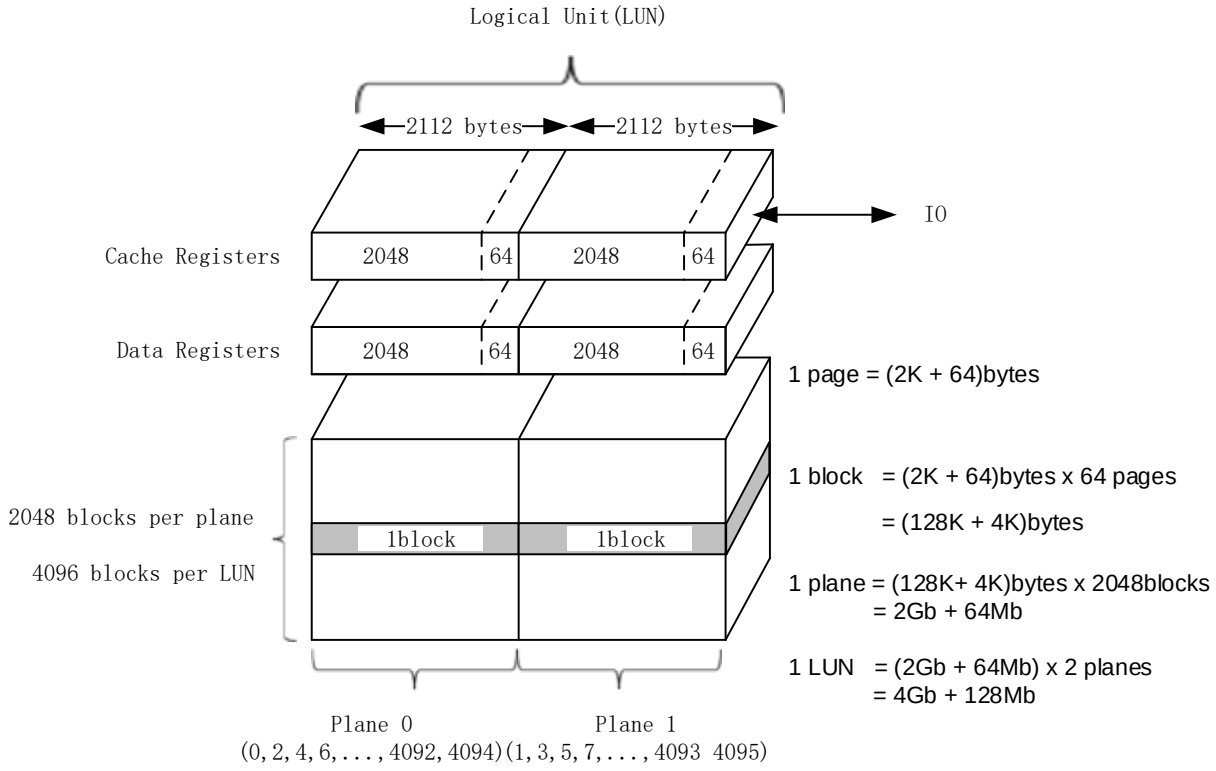


Figure 5-1: Array Organization figures

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5.1 Addressing (X8)

Bus Cycle	IO0	IO1	IO2	IO3	IO4	IO5	IO6	IO7
1st Cycle	A0	A1	A2	A3	A4	A5	A6	A7
2nd Cycle	A8	A9	A10	A11	L	L	L	L
3rd Cycle	A12	A13	A14	A15	A16	A17	A18	A19
4th Cycle	A20	A21	A22	A23	A24	A25	A26	A27
5th Cycle	A28	A29	A30	A31	L	L	L	L

A0-A11: column address in the page
A12-A17: page address in the block
A18: plane address (for multi-plane operations) / block address (for normal operations)
A18-A29: block address
A30-A31: LUN address

Note: For 4Gb, A30/A31 is Low; For 8Gb, A31 is Low

5.2 Addressing (X16)

Bus Cycle	IO0	IO1	IO2	IO3	IO4	IO5	IO6	IO7
1st Cycle	A0	A1	A2	A3	A4	A5	A6	A7
2nd Cycle	A8	A9	A10	L	L	L	L	L
3rd Cycle	A11	A12	A13	A14	A15	A16	A17	A18
4th Cycle	A19	A20	A21	A22	A23	A24	A25	A26
5th Cycle	A27	A28	A29	A30	L	L	L	L

A0-A10: column address in the page
A11-A16: page address in the block
A17: plane address (for multi-plane operations) / block address (for normal operations)
A17-A28: block address
A29-A30: LUN address

Note: For 4Gb, A29/A30 is Low; For 8Gb, A30 is Low

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5.3 Factory Defect Mapping

The Flash array is not presumed to be pristine, and a number of defects that makes the blocks unusable may be present. Invalid blocks shall be sorted out from normal blocks by software.

5.3.1. Device Requirements

If a block is defective, the manufacturer shall mark the block as defective by setting the Defective Block Marking, as shown in Figure of “Area marked in first or last page of block indicating defect”, of the last page of the defective block to a value of non-FFh. The Defective Block Marking is located on the first byte of user data area or the first byte of spare data area in the pages within a block.

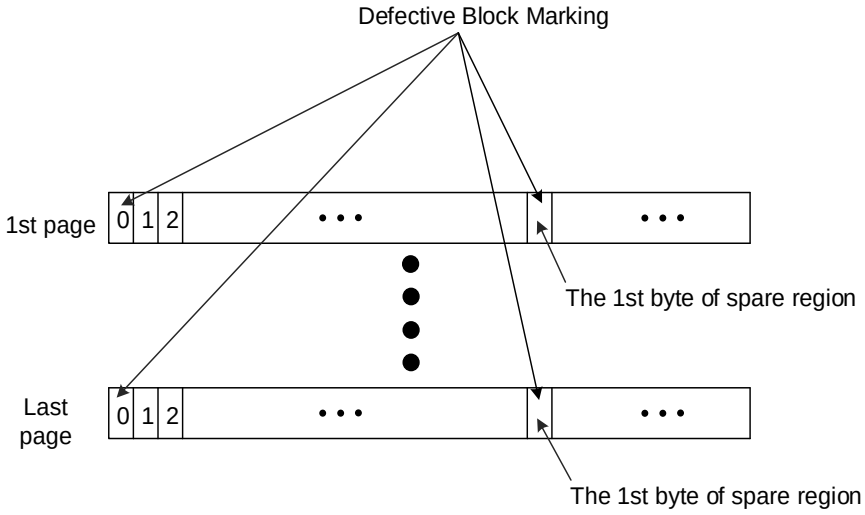


Figure 5-2: area marked in first or last page of block indicating defect sequential figures

5.3.2. Host Requirements

The host shall not erase or program blocks marked as defective by the manufacturer, and any attempt to do so yields indeterminate results.

Figure of “Flow chart to create initial invalid block table” outlines the flow chart how to create an initial invalid block table. It should be performed by the host to create the initial bad block table prior to performing any erase or programming operations on the target. The 1st byte of both main and spare region in non-defective blocks are read FFh with ECC enabled on the controller. A defective block is indicated by the majority of bits being read non-FFh in the Defective Block Marking location of either the first page or last page of the block. The host shall check the Defective Block Marking location of both the first and last past page of each block to verify the block is valid prior to any erase or program operations on that block.

NOTE: Over the lifetime use of a NAND device, the Defective Block Marking of defective blocks may encounter read disturbs that cause bit changes. The initial defect marks by the manufacturer may change value over the lifetime of the device, and are expected to be read by the host and used to create a bad block table during initial use of the part.

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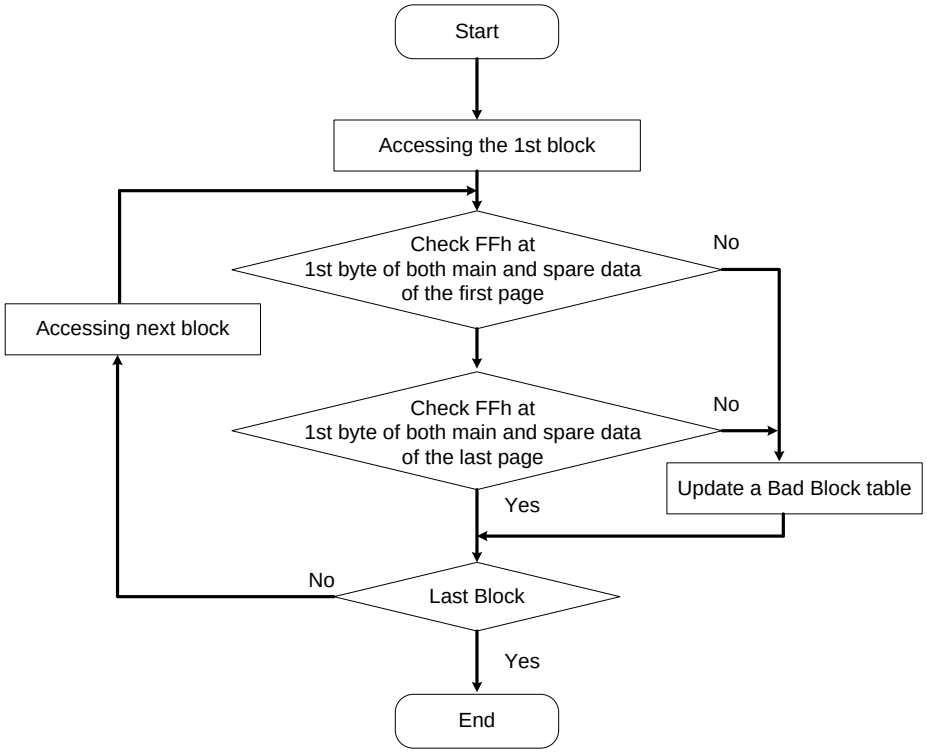


Figure 5-3: flow chart to create initial invalid block table sequential figures

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6. COMMAND SET

Function	1st	2nd	3rd	4th	During busy
Page read	00H	30H	--	--	No
Read for copy-back	00H	35H	--	--	No
Special read for copy back	00H	36H	--	--	No
Random data output (change column address)	05H	E0H	--	--	No
Random data output(change row address)	06H	E0H	--	--	No
Cache read start	31H	--	--	--	No
Cache read random	00H	31H	--	--	No
Cache read end	3FH	--	--	--	No
Read id	90H	--	--	--	No
Read status register	70H	--	--	--	Yes
Read status enhanced (ONFI)	78H	--	--	--	Yes
Page program start / Cache program end	80H	10H	--	--	No
Random data input	85H	--	--	--	No
Copy back program	85H	10H	--	--	No
Cache program start	80H	15H	--	--	No
Block erase	60H	D0H	--	--	No
Reset	FFH	--	--	--	Yes
Reset LUN	FAH	--	--	--	Yes
Page re-program	8BH	10H	--	--	No
Read parameter page	ECH	--	--	--	No
Read unique ID	EDH	--	--	--	No
Get Features	EEH	--	--	--	No
Set Features	EFH	--	--	--	No
Get LUN Features	D4H	--	--	--	No
Set LUN Features	D5H	--	--	--	No
Multi-Plane program	80H	11H	80/81H	10H	No
Multi-Plane re-program	8BH	11H	8BH	10H	No
Multi-Plane cache program	80H	11H	80/81H	15H	
	80H	11H	80/81H	10H	No
Multi-Plane copy back program	85H	11H	85H	10H	No
Multi-Plane block erase	60H	60H	D0H		No
Multi-Plane block erase (ONFI)	60H	D1H	60H	D0H	No
Read page two-plane	00H	32H	00H	30H	No
Read for two-plane copy back	00H	32H	00H	35H	No

Note: 1. read status, read ID, get feature are always output on IO[7:0].

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7. BUS OPERATION

The bus on the device is multiplexed. Data I/O, addresses, and commands all share the same pins. I/O [15:8] are used only for data in the x16 configuration. Addresses and commands are always supplied on I/O [7:0].

The command sequence typically consists of a COMMAND LATCH cycle, address input cycles, and one or more data cycles, either READ or WRITE.

There are several standard bus operations that control the device. These are Command Input, Address Input, Data Input, Data Output, Write Protect, and Standby.

CLE	ALE	CE#	WE#	RE#	WP#	MODE
H	L	L	Rising	H	X	Command input for read mode
L	H	L	Rising	H	X	Address input for read mode
H	L	L	Rising	H	H	Command input for write mode
L	H	L	Rising	H	H	Address input for write cycle
L	L	L	Rising	H	H	Data input
L	L	L	H	Falling	X	Sequential read and data output
L	L	X	H	H	X	During read(busy)
X	X	X	X	X	H	During program/Erase(busy)
X	X	X	X	X	L	Write protect
X	X	H	X	X	0V / VCC	Standby

Notes:

1. X can be VIL or VIH. H = Logic level HIGH. L = Logic level LOW.
2. WP# should be biased to CMOS high or CMOS low for stand-by mode.
3. WE# and RE# during Read Busy must be keep on high to prevent unplanned command/address/data input or to avert unintended data out. In this time, only Reset and Read Status can be input to the device.

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7.1 Command Input Cycle

Command Input bus operation is used to give a command to the memory device. Commands are accepted with Chip Enable low, Command Latch Enable High, Address Latch Enable low and Read Enable High and latched on the rising edge of Write Enable. Moreover for commands that starts a modify operation (write/erase) the Write Protect pin must be high.

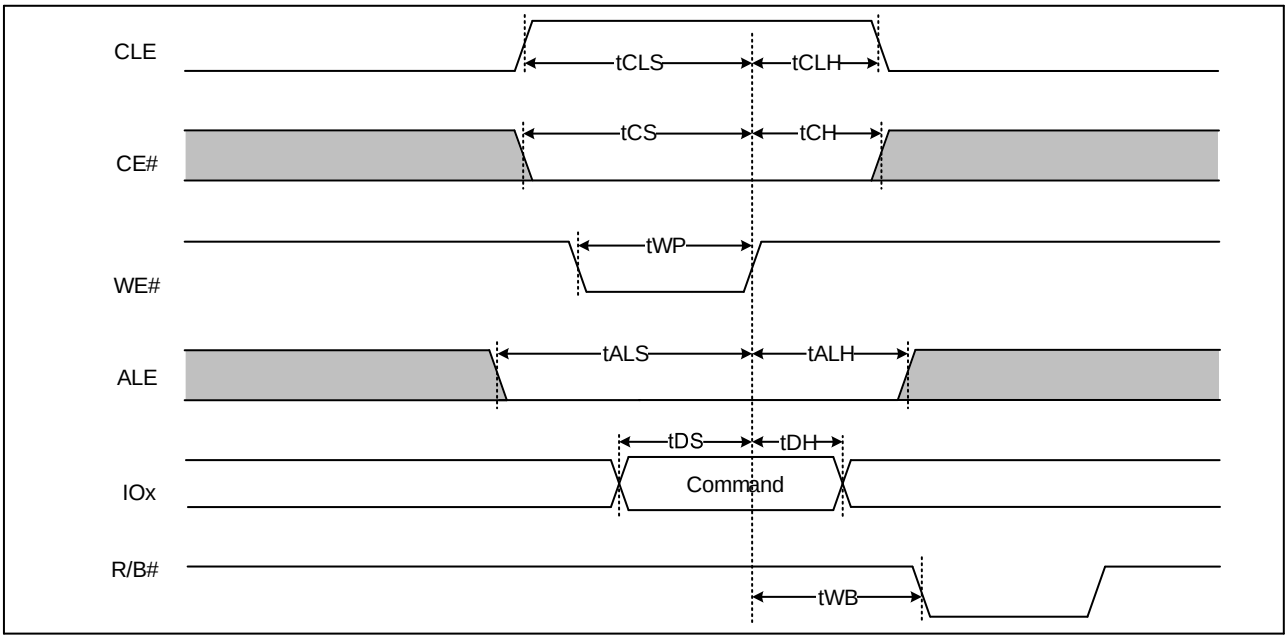


Figure 7-1: Command Input Cycle figures

7.2 Address Input Cycle

Address Input bus operation allows the insertion of the memory address. Addresses are accepted with Chip Enable low, Address Latch Enable High, Command Latch Enable low and Read Enable High and latched on the rising edge of Write Enable. Moreover for commands that starts a modify operation (write/erase) the Write Protect pin must be high.

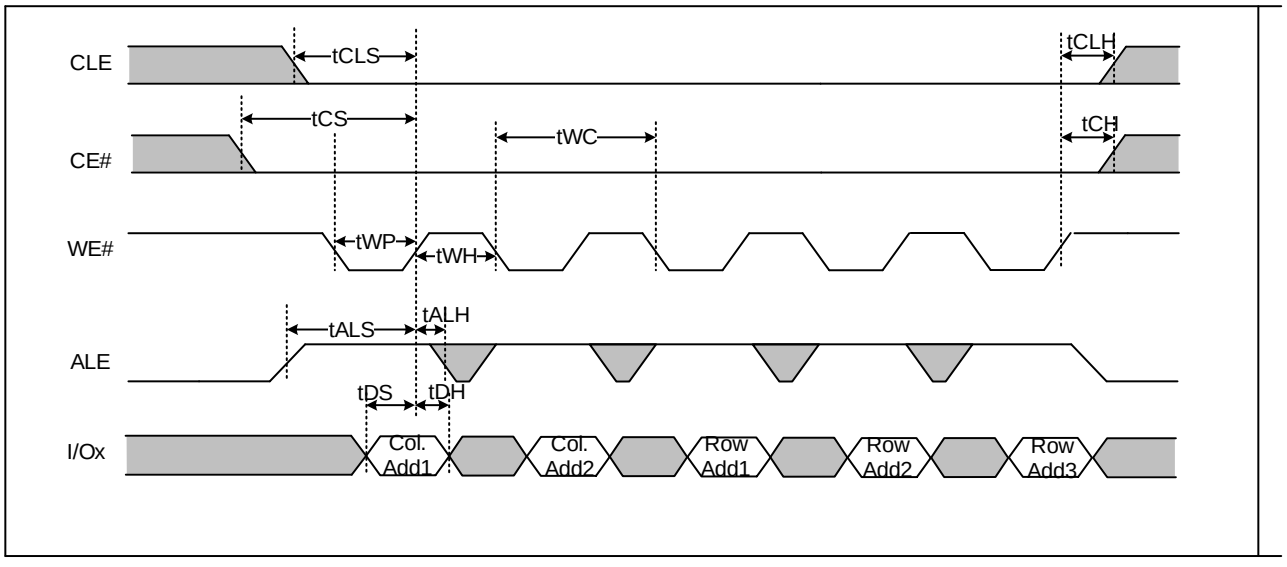


Figure 7-2: Address Input Cycle figures

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7.3 Data Input Cycle

Data Input bus operation allows to feed to the device the data to be programmed. The data insertion is serially and timed by the Write Enable cycles. Data are accepted only with Chip Enable low, Address Latch Enable low, Command Latch Enable low, Read Enable High, and Write Protect High and latched on the rising edge of Write Enable.

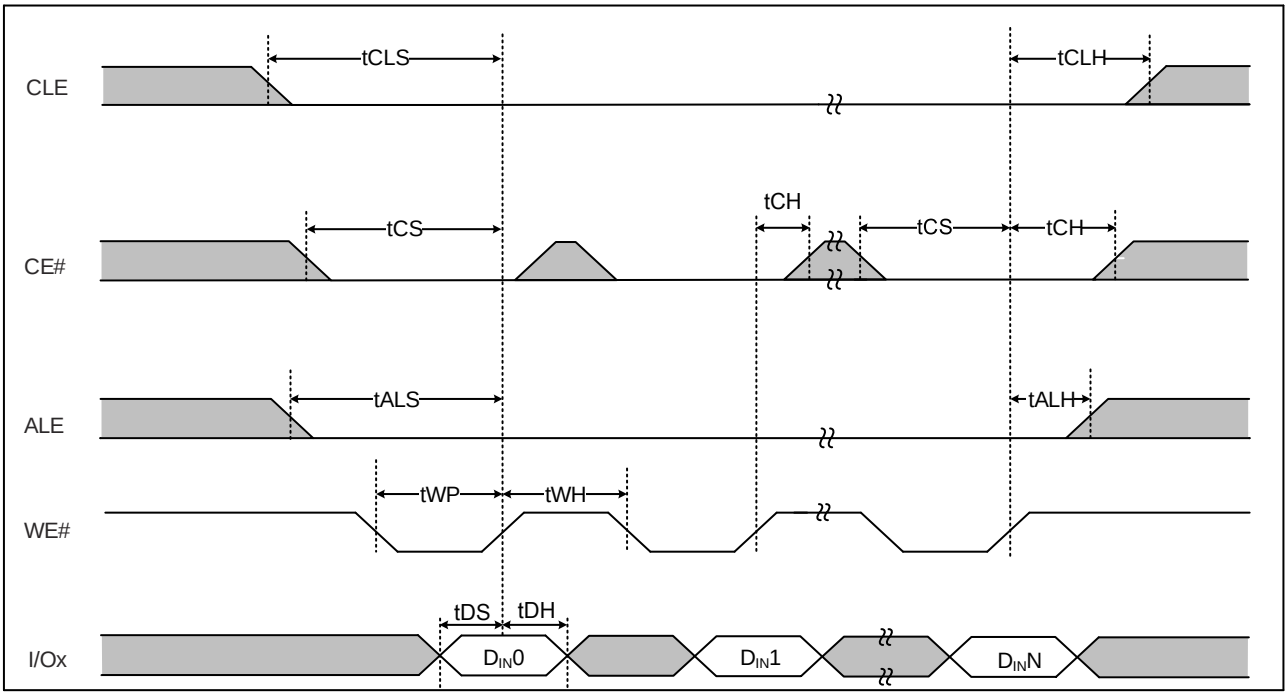


Figure 7-3: Data Input Cycle figures

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7.4 Data Output Cycle

Data Output bus operation allows to output data from the device. The data output cycle is serially and timed by the Read Enable cycles. Data output may be used with CE# don't care. However, if CE# don't care is used tCEA and tCOH timing requirements shall be met by the host.

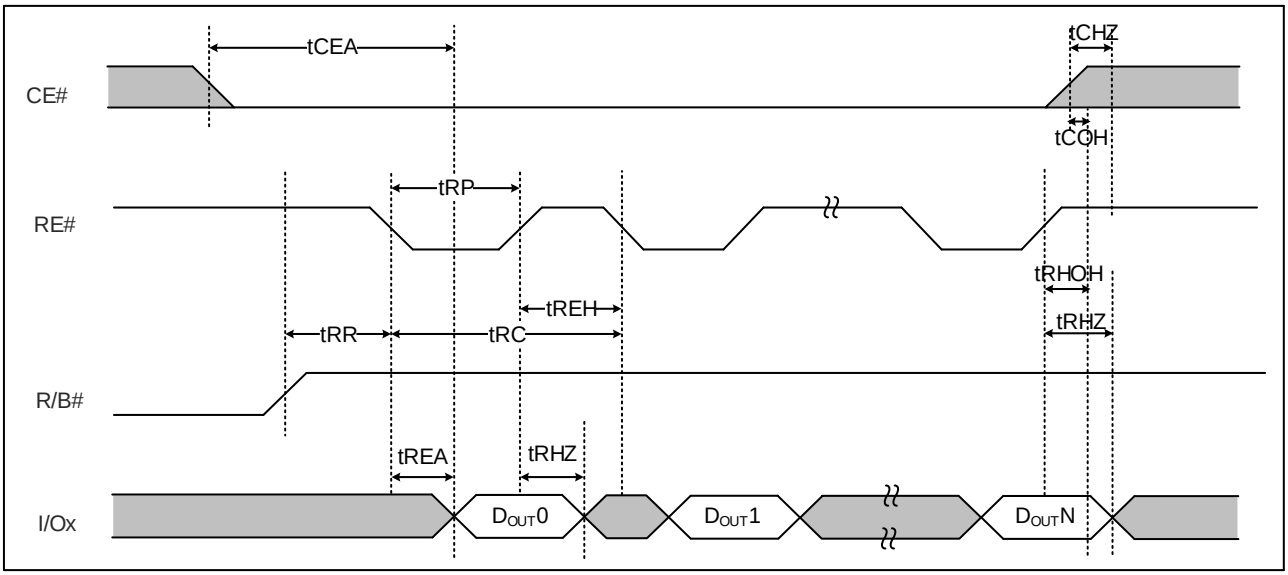


Figure 7-4_a: Data Output Cycle figures

If the host side uses a sequential access time (tRC) of less than 30ns, the data can be latched on the next falling edge of RE# as the waveform of EDO (Extended data output) mode.

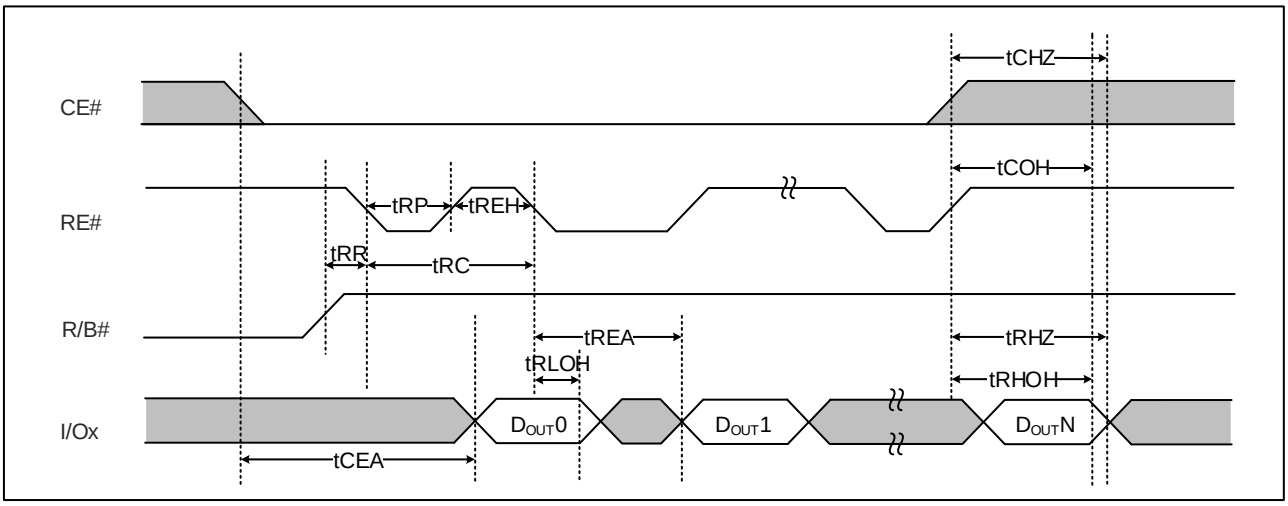


Figure 7-4_b: Data Output Cycle figures

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7.5 Write Protect

The Erase and Program Operations are automatically reset when WP# goes Low. The operations are enabled and disabled as follows.

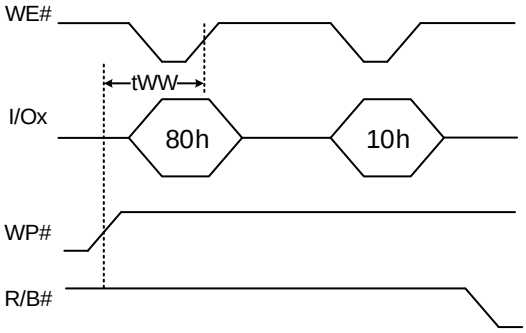


Figure7-5_a: Write Protect Disable with program figures

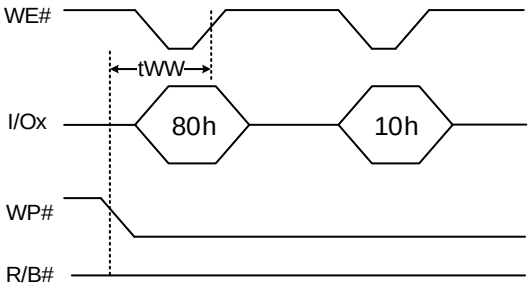


Figure 7-5_b: Write Protect Enable with program figures

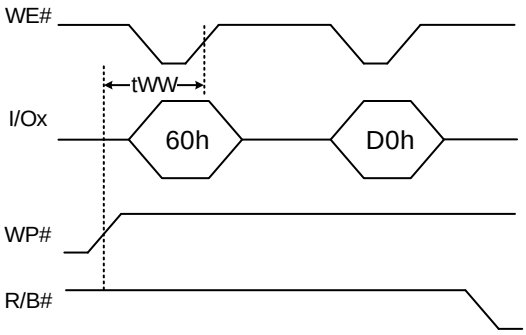


Figure 7-5_c: Write Protect Disable with erase figures

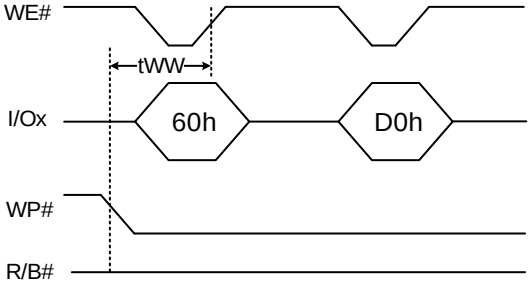


Figure 7-5_d: Write Protect Enable with erase figures

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8. OPERATION DESCRIPTION

8.1 Page Read Operation

8.1.1 Common Page Read (00H-30H)

Read is initiated by writing 00H-30H to the command register along with five address cycles. After initial power up, the first page of the first block has been read to cache ready for random read out.

The system controller can detect the completion of this data transfer (tR) by analyzing the output of R/B# pin or read status command. Once the data in a page is loaded into the cache registers, they may be read out in tRC by sequentially toggle RE#. The repetitive high to low transitions of the RE# clock make the device output the data starting from the selected column address up to the last column address.

After the last data has been read out, CE# may be pulled up for some time to end the read operation, while during the RE# toggle cycle, CE# may be don't care when RE# is high. The CE# Don't Care feature may simplify the system interface, which allows controller to directly download the code from flash device, and the CE# transitions will not stop the read operation during the latency time.

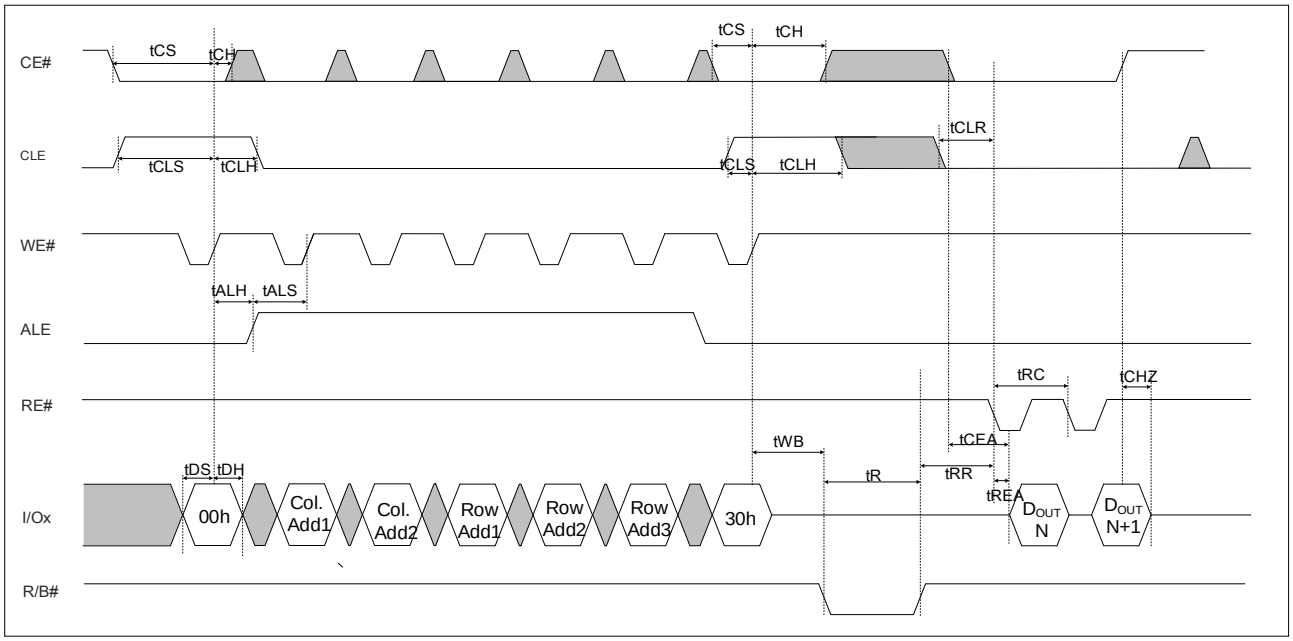


Figure 8-1: Common Page Read figures

8.1.2 Random Data Output (05H-E0H)

The device may output random data in a page instead of the consecutive sequential data by input random data output command (05H-E0H). The column address of next data, which is going to be out, may be changed to the address which follows random data output command. Random data output can be operated multiple times regardless of how many times it is done in a page, Random data output shall only be issued when the device is in a read idle condition.

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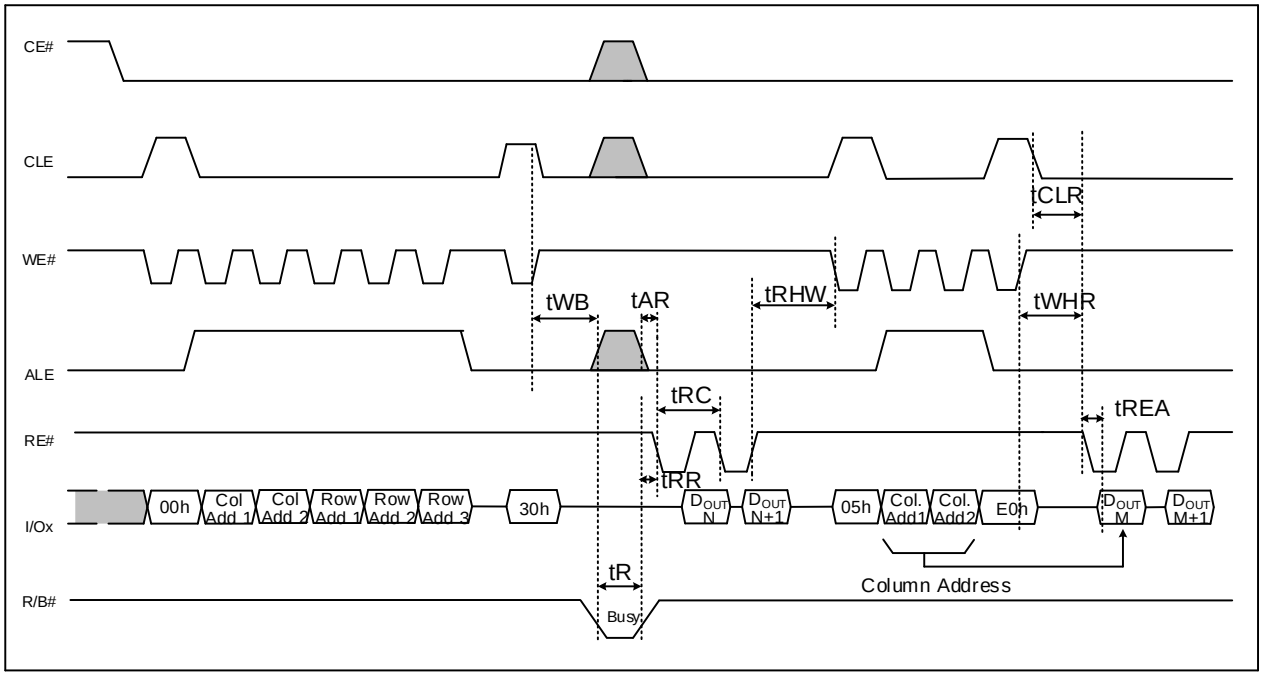


Figure 8-2: Random Data Output figures

Note: the address followed 05h can be only 2bytes cycle.

8.1.3 Random Data Output Enhanced (06H-E0H)

The device may output random data in a page instead of the consecutive sequential data by input random data output command (06H-E0H). The row address and column address of next data, which is going to be out, may be changed to the address which follows random data output command. Random data output can be operated multiple times regardless of how many times it is done in a page. Random data output enhanced shall only be issued when the device is in a read idle condition.

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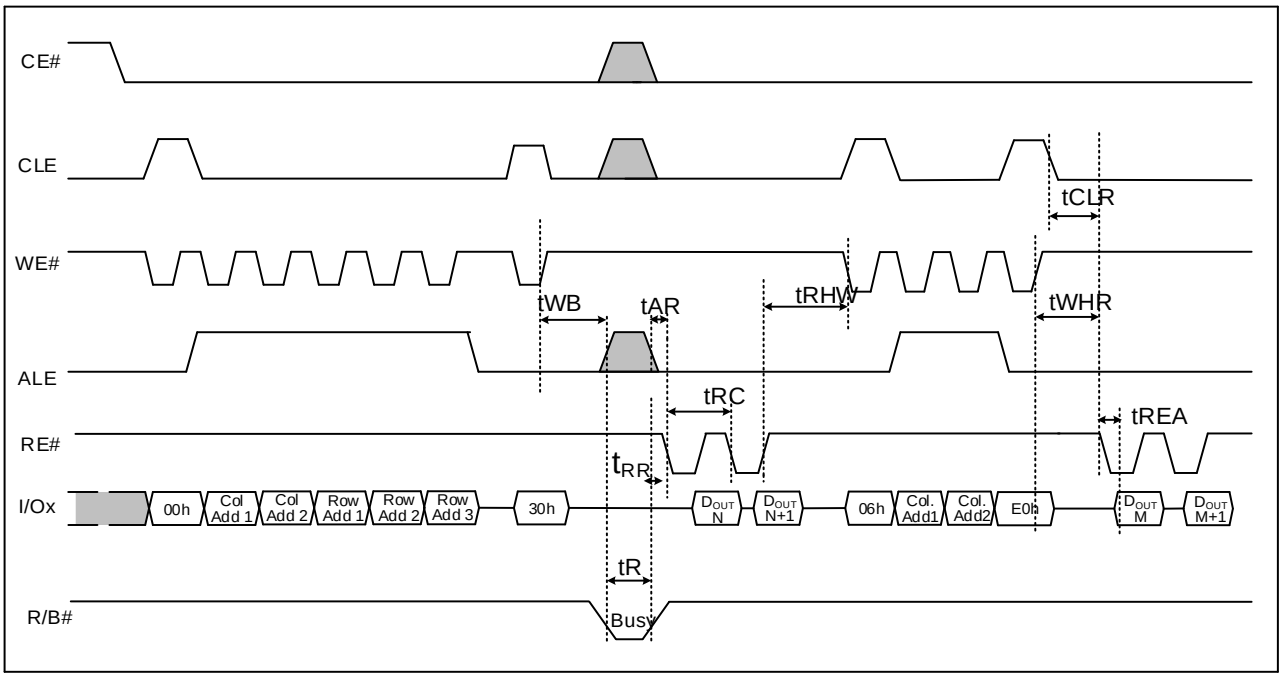


Figure 8-3: Random Data Output sequential figures

Note: the address followed 06h can be 2bytes cycle or 5 bytes cycle.

8.1.4 Cache Read Operation (31H/3FH)

The Cache Read function permits a page to be read from the cache register while another page is simultaneously read from the Flash array. A Read Page command shall be issued prior to the initial sequential or random Read Cache command in a read cache sequence. A Read Cache command shall be issued prior to a Read Cache End (3FH) command being issued. The Cache Read function may be issued after the Read function is complete. The host may enter the address of the next page to be read from the Flash array. Data output always begins at column address 00H. If the host does not enter an address to retrieve, the next sequential page is read, when the Read Cache function is issued. After the operation is begun R/B# is set to high (ready) and the host may begin to read the data from the previous Read or Read Cache function. Issuing an additional Read Cache function copies the data most recently read from the array into the cache register. When no more pages are to be read, the final page is copied into the cache register by issuing the 3FH command.

The host may begin to read data from the cache register when R/B# is set to high (ready). When the 31H and 3FH commands are issued, R/B# shall be cleared to low (busy) until the page has finished being copied from the Flash array.

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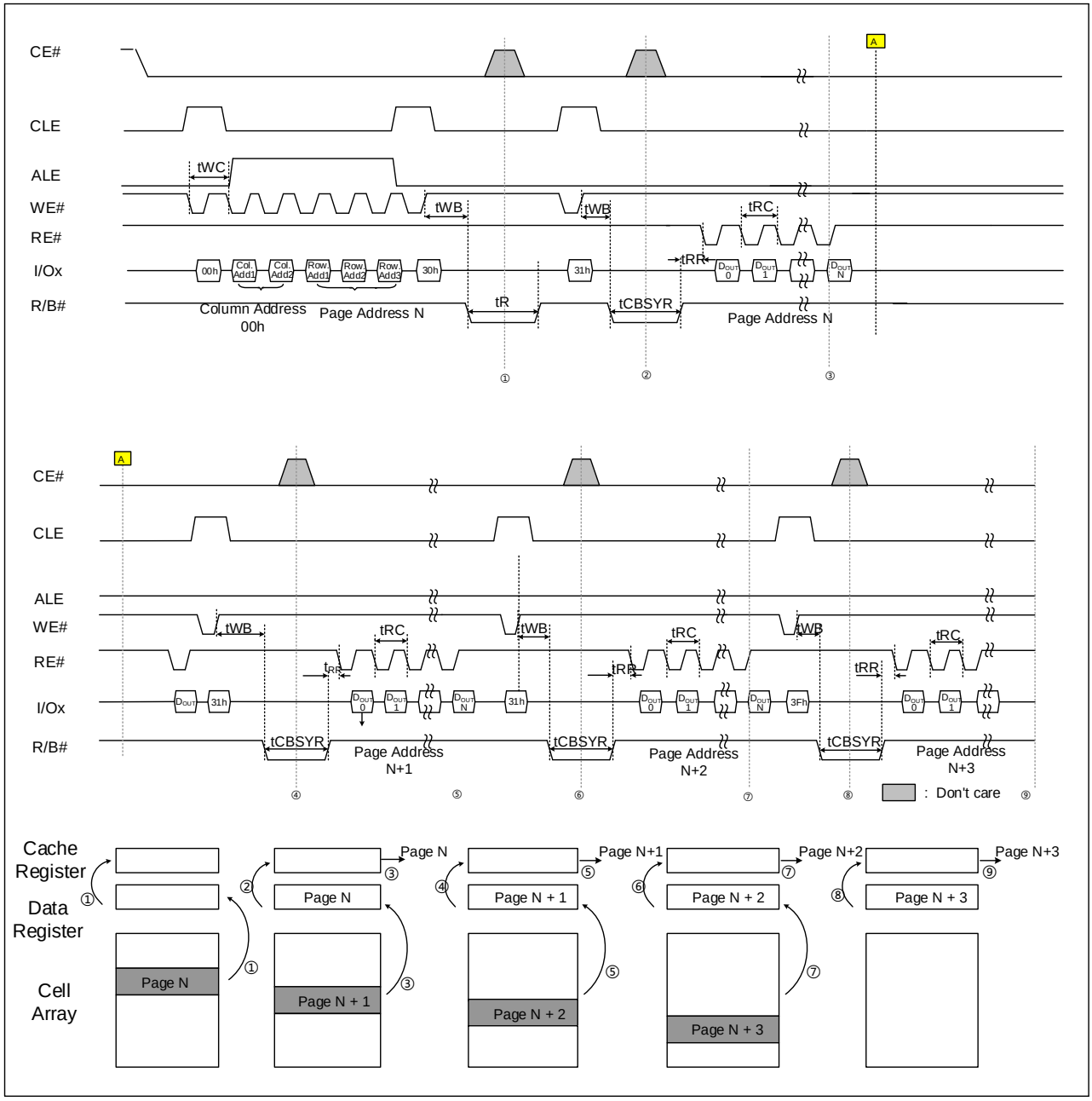


Figure 8-4: Cache Read Operation figures

Note:

C1-C2 : Column address of the page to retrieve. C1 is the least significant byte.

R1-R2 : Row address of the page to retrieve. R1 is the least significant byte.

D0-Dn : Data bytes/words read from page requested by the original Read or the previous cache operation.

8.1.5 Cache Read Random (00H-31H)

The Cache Read Random operation allows the random page to be read-out with cache operation not just for consecutive page only.

After issuing the 00h command, the column and row address should be given for the start page selection, and followed by the 30h command for address confirmation. The column address is ignored in the cache read random operation. And then,

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the Cache Read Random operation starts after a latency time tR and following a 00h command with the selected page address and following a 31h command, the data can be read-out after the latency time of tCBSYR. After the previous selected page data out, a new selected page address can be given by writing the 00h-31h command set again. The Cache Read Random command is also valid for the consecutive page cross block.

The Random Data Output (05h-E0h) command can be used to change the column address of the data being output from the cache register. When no more pages are to be read, the final page is copied into the cache register by issuing the 3FH command in one block.

The host may begin to read data from the cache register when R/B# is set to high (ready). When the 31H and 3FH commands are issued, R/B# shall be cleared to low (busy) until the page has finished being copied from the Flash array.

Status Register can be checked after the Read Status command (70h) is issued. IO6 behaves the same as R/B# pin, IO5 indicates the internal chip operation. “0” means the chip is in internal operation and “1” means the chip is idle. Command 00h should be given to return to the cache read operation.

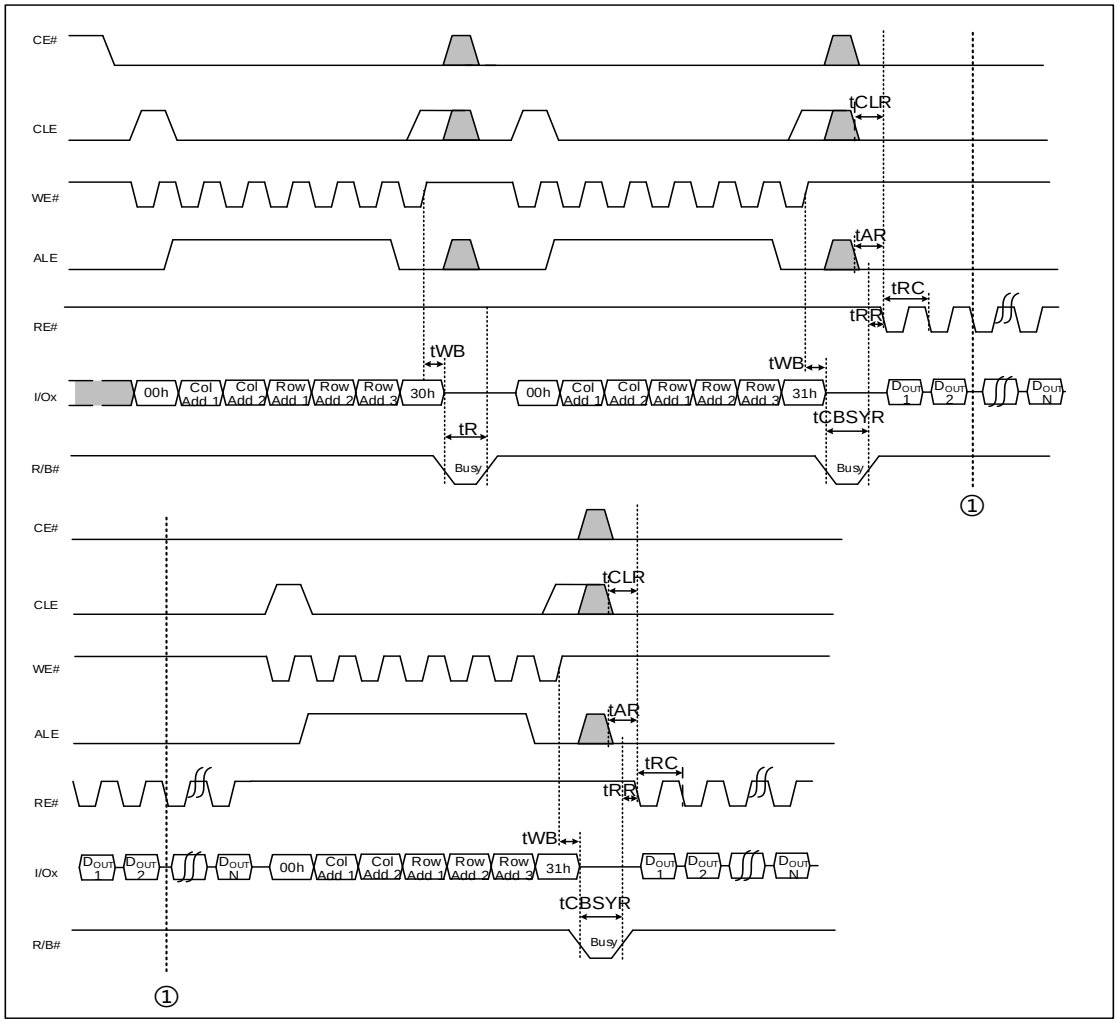


Figure 8-5: Cache Read Random Figure

8.1.6 Read for copy back (00H-35H)

The Copy-Back Read is configured to efficiently rewrite data stored in a page without data reloading when no error within the page is found. The data is read out only at cache register for copy-back program.

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Though it is not required, it is recommended that the host read the data out of the device to verify the data prior to issuing the Copy-Back Program (85h-10h) command to prevent the propagation of data errors.

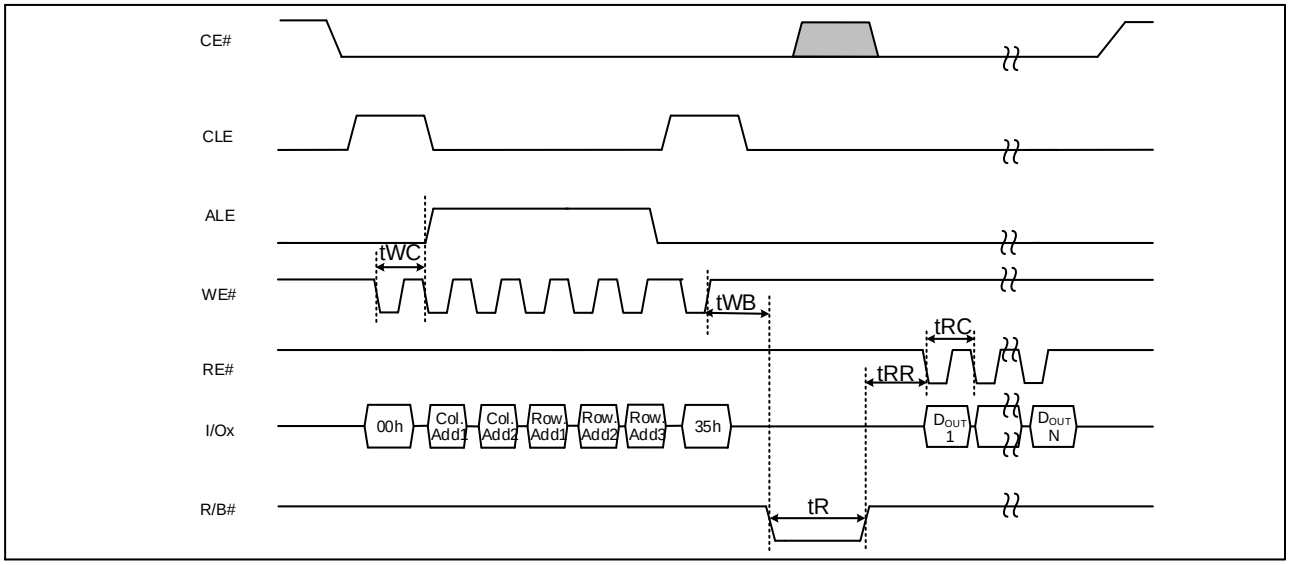


Figure8-6: Copy-Back read sequential figures

8.1.7 Special read for copy back (00H-36H)

If copy back read is triggered with confirm command "36h" instead "35h", copy-back read from target page(s) will be executed with an increased internal voltage.

This special feature is used in order to try to recover incorrigible ECC read errors. It shall be used ONLY if ECC read errors have occurred in the source page using "standard read" or "standard read for copy back" sequences.

Before the copy-back read confirm command (36H) is issued, all other features described in standard copy-back remain valid.

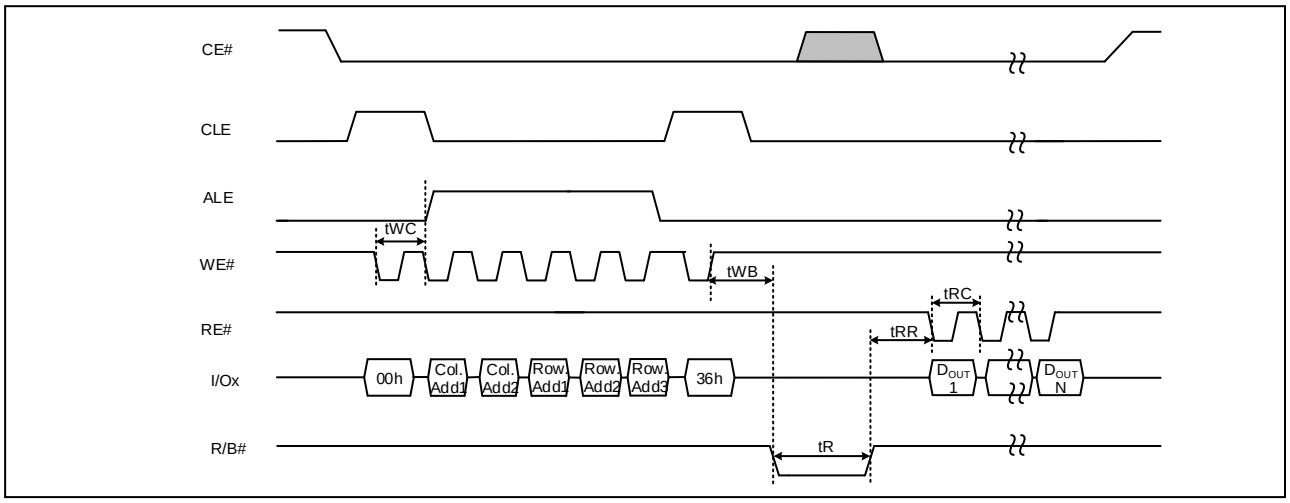


Figure8-7: Special read for copy-back sequential figures

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8.1.8 Read Two Plane (00H-32H-00H-30H)

The Two-Plane Page Read operation is an extension of the Page Read operation. The device supporting Two-plane page read operation also allows multi Random data-output from each plane(i.e. Two-Plane Random Data Output) once multi-pages from each plane are loaded to cache registers. With the primary command, R/B# returns to ready in a short time (i.e. tDBSY) after the first command 32h since it does not load data from a selected page, and the selected page data of each plane are transferred to the cache registers in less than tR after command 30h. When setting page addresses of each plane, the page addresses shall be identical although block addresses differ.

The Two-plane addresses shall be set in a consecutive manner from a lower address plane to a higher address plane and the same plane address shall not be set twice within a set of address setting sequence for the Two-Plane Page Read Operation. Starting plane address should be Plane0.

Once the data is loaded into the cache registers, the data on the first plane can be read out by issuing the Two-Plane Random Data Output command. The data on the other plane can be also read out using the identical command sequences. follow figure define Two-plane Page Read and Two-Plane Random Data Output behavior and timings.

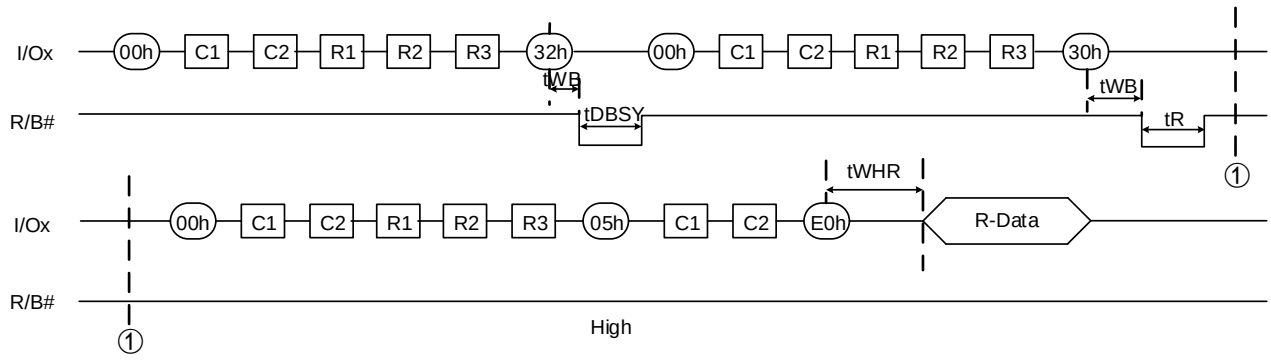


Figure 8-8: Read Two Plane sequential figures

8.1.9 Read for Two-Plane Copy Back (00H-32H-00H-35H)

Two-Plane Copy-Back Program operation is executed two sets of commands, Two-Plane Read for Copy-Back and Two-Plane Copy-Back Program. The Two-plane addresses shall be set in a consecutive manner from a lower address plane to a higher address plane and the same plane address shall not be set twice within a set of address setting sequence for the Two-Plane Copy-Back Program Operation. Starting plane address shall be Plane0.

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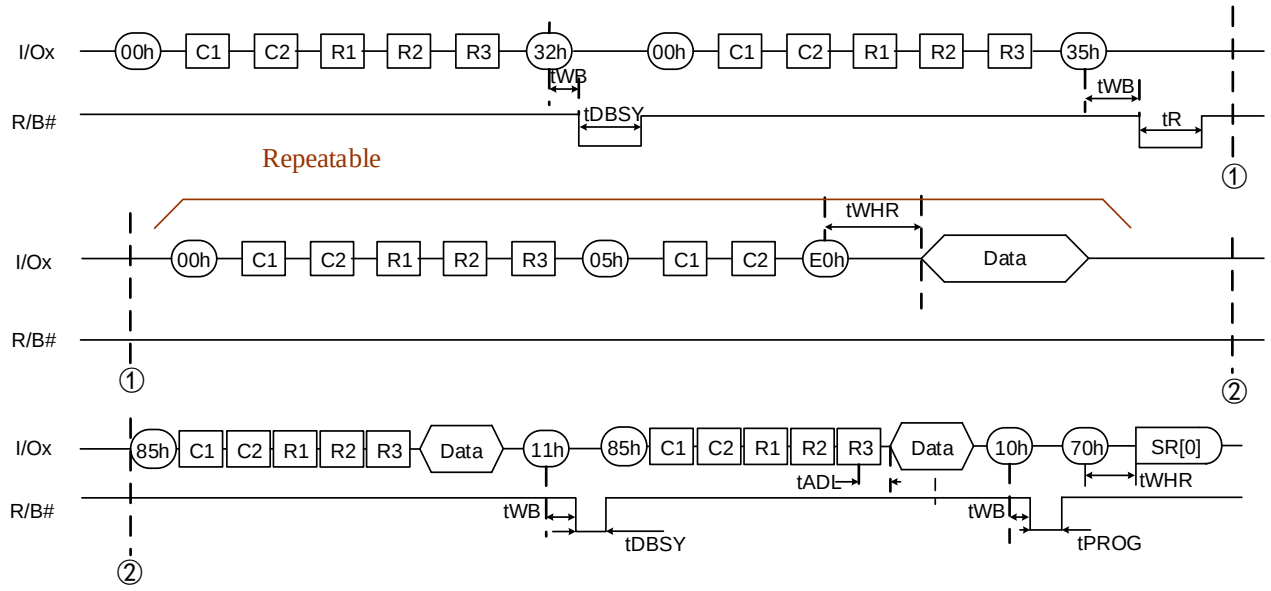


Figure 8-9: Read for Two-Plane Copy Back sequential figures

Note: the data followed 85h command is optional.

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8.2 Page Program Operation

8.2.1 Common Page Program (80H-10H)

The device is programmed basically on a page basis, but it does allow multiple partial pages programming of a word or consecutive bytes up to whole page program cycle. The number of consecutive partial page programming operation within the same page without an intervening erase operation must not exceed NOP.

The page address for programming must be done in sequential order in a block.

A page program cycle consists of a serial data loading period in which up to whole page data may be loaded into the cache register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell.

The serial data loading period begins by inputting the Serial Data Input command (80h), followed by the five cycle address inputs and then serial data loading. The words other than those to be programmed do not need to be loaded.

The Page Program Confirm command (10h) initiates the programming process. Writing 10h alone without previously entering the serial data will not initiate the programming process. The internal write state controller automatically executes the algorithms and timings necessary for program and verify, thereby freeing the system controller for other tasks. Once the program process starts, the Read Status command may be issued to read the status register.

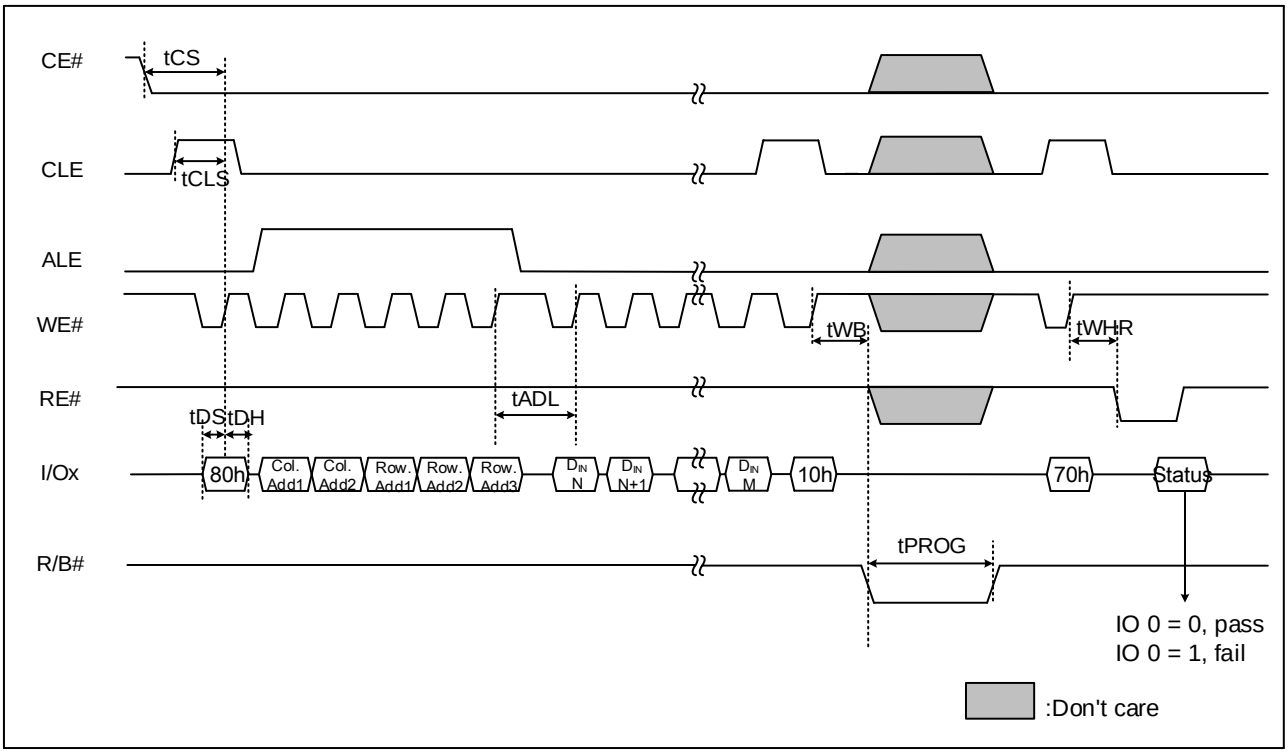


Figure 8-10: Common Page Program figures

8.2.2 Page Program Operation with Random Data Input (85H)

The device supports random data input in a page. The column address of next data, which will be entered, may be changed to the address which follows random data input command (85H). Random data input may be operated multiple times regardless of how many times it is done in a page.

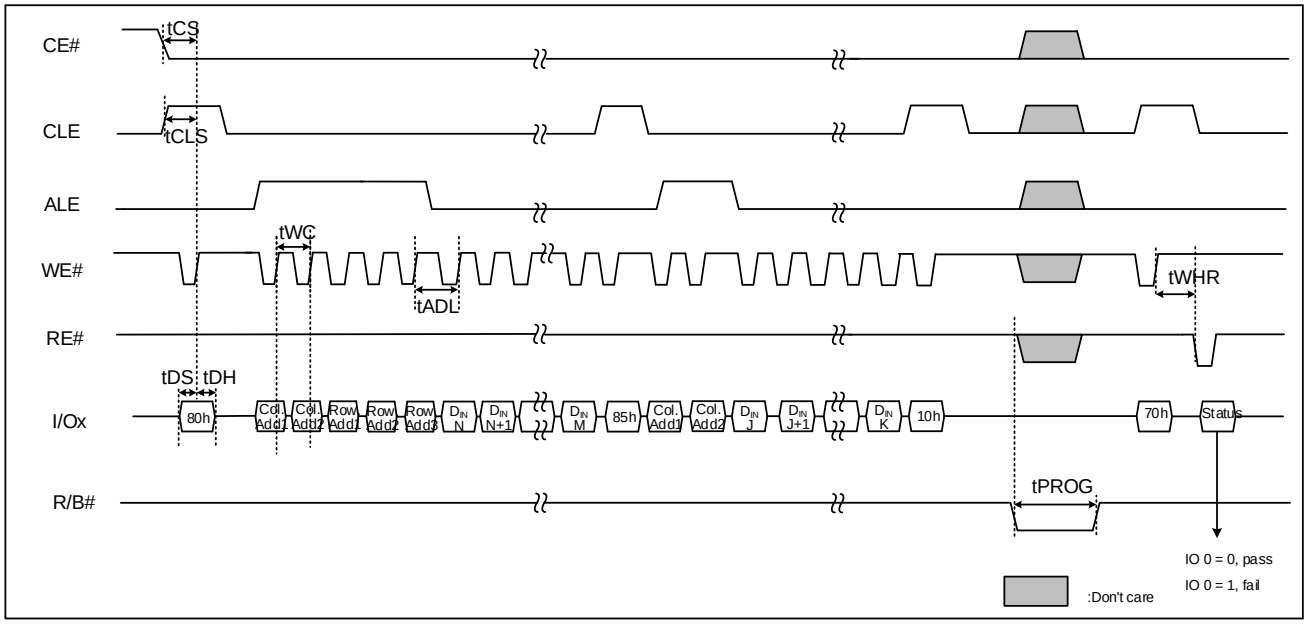


Figure 8-11: Page Program Operation with Random Data Input figures

8.2.3 Page Re-program (8BH-10H)

It was also highlighted that page program may result in a fail, which can be detected by Read Status Register. In this event, it implements the innovative feature of “page re-program”. This command allows the re-programming of the same pattern of the (failed) page into another memory location. The command sequence initiates with re-program setup (8BH), followed by the five cycle address inputs of the target page. If the target pattern for the destination page is not changed compared to the page, the program confirm can be issued (10H) without any data input cycle.

On the other hand, if the pattern bound for the target page is different from that of the previous page, data in cycles can be issued before program confirm “10H”

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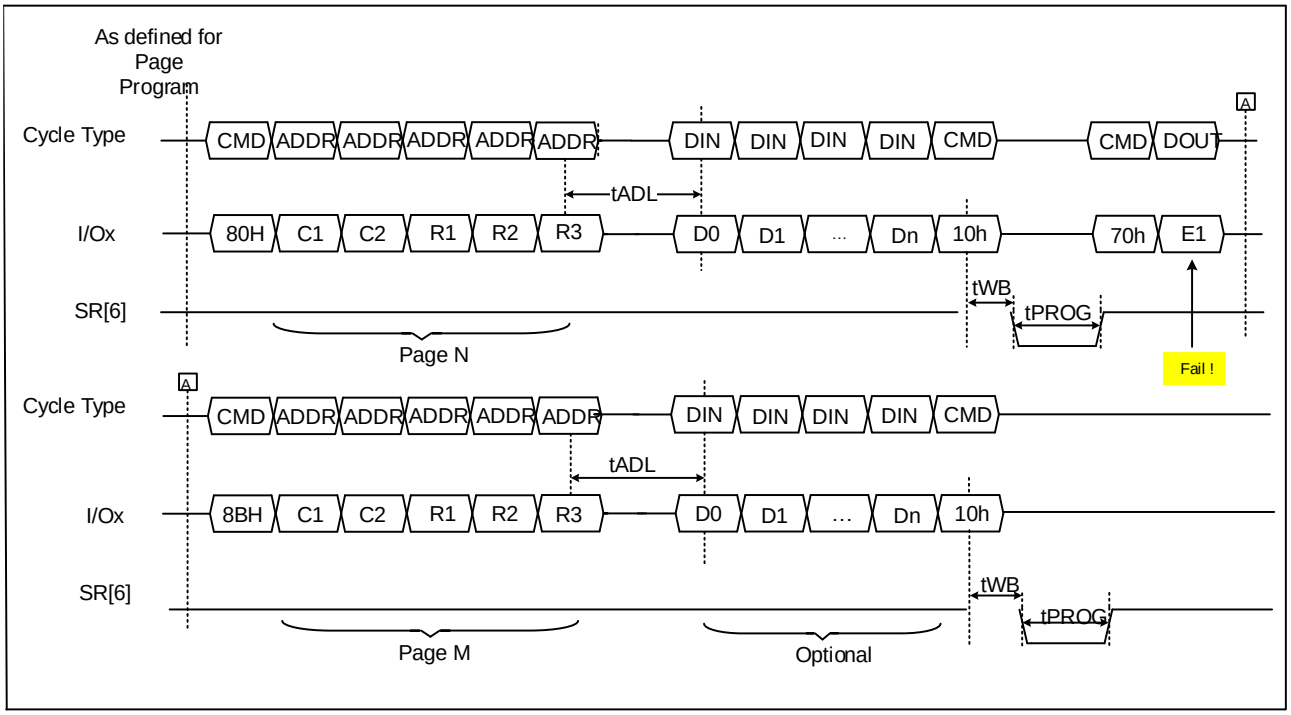


Figure 8-12: Page Re-program figures

Note: the data followed 8BH is optional.

8.2.4 Cache Program Operation (80H-15H)

Cache Program is an extension of Page Program, which is executed with one page cache registers, and is available only within a block. Since the device has one page of cache registers, serial data input may be executed while data stored in data registers are programmed into memory cell.

After writing the first set of data up to one page into the selected cache registers, Cache Program command (15H) instead of actual Page Program (10H) is inputted to make cache registers free and to start internal program operation. To transfer data from cache registers to data registers, the device remains in Busy state for a short period of time (tCBSYW) and has its cache registers ready for the next data-input while the internal programming gets started with the data loaded into data registers. Read Status command (70H) may be issued to find out when cache registers become ready by polling the Cache-Busy status bit (I/O6). Pass/fail status of only the previous page is available upon the return to Ready state. When the next set of data is loaded with the Cache Program command, tCBSYW is affected by the progress of pending internal programming. The programming of the cache registers is initiated only when the pending program cycle is finished and the data registers are available for the transfer of data from cache registers. The status bit (I/O5) for internal Ready/Busy may be polled to identify the completion of internal programming. If, after tCBSYW, the host wants to wait for the PROGRAM CACHE operation to complete, without issuing the PROGRAM PAGE (80h-10h) command, the host should monitor ARDY until it is 1. The host should then check the status of the FAIL and FAILC bits.

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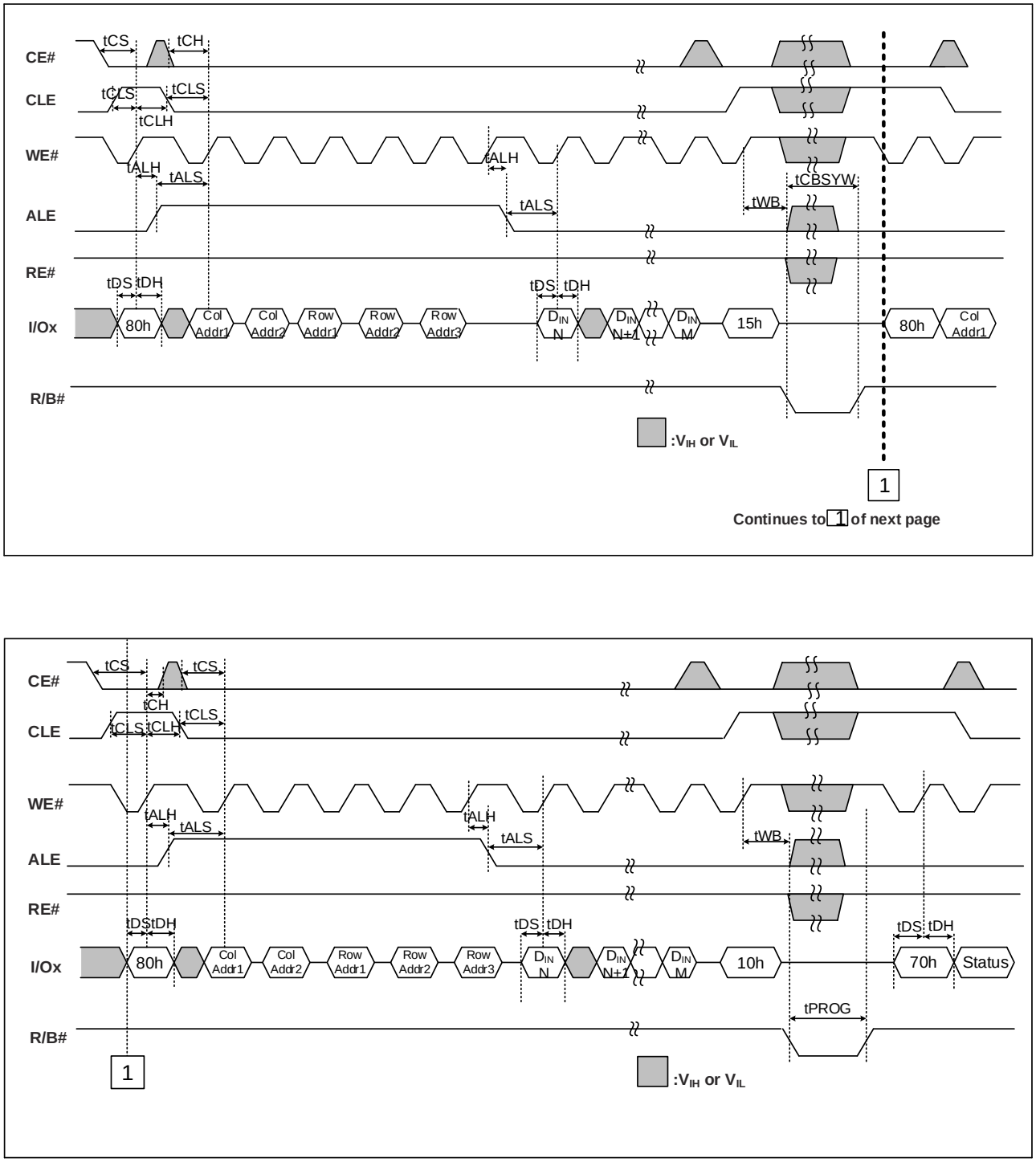


Figure 8-13: Cache Program Operation figures

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8.2.5 Copy-Back Program with Random Data Input (85H-10H)

The copy-back program is configured to quickly and efficiently rewrite data stored in one page without utilizing an external memory. Since the time-consuming cycles of serial access and re-loading cycles are removed, the system performance is improved.

The benefit is especially obvious when a portion of a block is updated and the rest of the block is also needed to be copied to the newly assigned free block.

The operation for performing a copy-back program is a sequential execution of page-read without serial access and copying-program with the address of destination page. A read operation with “35h”command and the address of the source page moves the whole page bytes data into the internal cache register. As soon as the device returns to Ready state, optional data read-out is allowed by toggling RE#, or Copy Back command (85H) with the address cycles of destination page may be written. The Program Confirm command (10H) is required to actually begin the programming operation. Data input cycle for modifying a portion or multiple distant portions of the source page is allowed. When there is a program-failure at Copy-Back operation, error is reported by pass/fail status. But, if Copy-Back operations are accumulated over time, bit error due to charge loss is not checked by external error detection/correction scheme.

Please note that Random Data Input (with/without data) is entered before Program Confirm command (10H) after Random Data output.

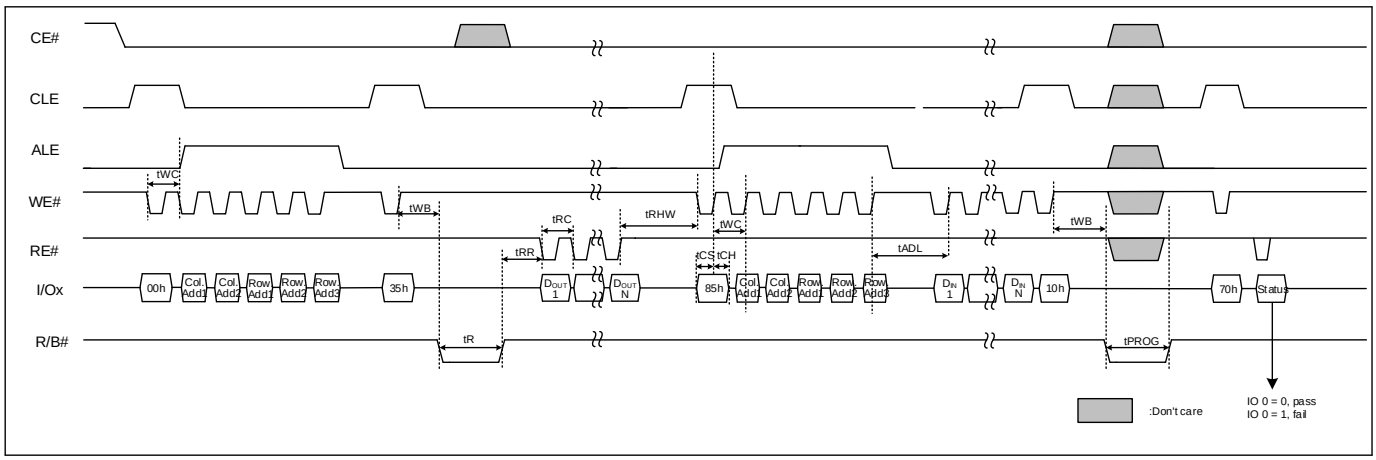


Figure 8-14: Copy-Back Program with Random Data Input figures

Note: the data followed with 85h command is optional

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8.2.6 Multi-Plane Program (80H-11H-80/81H-10H)

Device supports multiple plane program: it is possible to program 2 pages in parallel, one per each plane.
A multiple plane program cycle consists of a double serial data loading period in which up to one page data may be loaded into the cache registers, followed by a non-volatile programming period where the loaded data is programmed into the memory cell. The serial data loading period begins with inputting the Serial Data Input command (80h), followed by the five cycle address inputs and serial data for the 1st page. The device supports random data input exactly same as in the case of page program operation. The Dummy Page Program Confirm command (11h) stops 1st page data input and devices becomes busy for a short time (tDBSY).
Once it has become ready again, either the traditional "81h" or the ONFI "80h" command must be issued, followed by 2nd page address (5 cycles) and its serial data input. Program Confirm command (10h) makes parallel programming of both pages to start. Follow figure describe the sequences.
User can check operation status by monitoring RB# pin or reading status register commands (70h or 78h), as if it were a normal page program: read status register command is also available during Dummy Busy time (tDBSY).
In case of fail in any of 1st and 2nd page program, fail bit of status register will be set however, in order to know which page failed, ONFI 1.0 "Read Status Enhanced" command (78h) must be issued for further info.
Starting plane address should be Plane0.

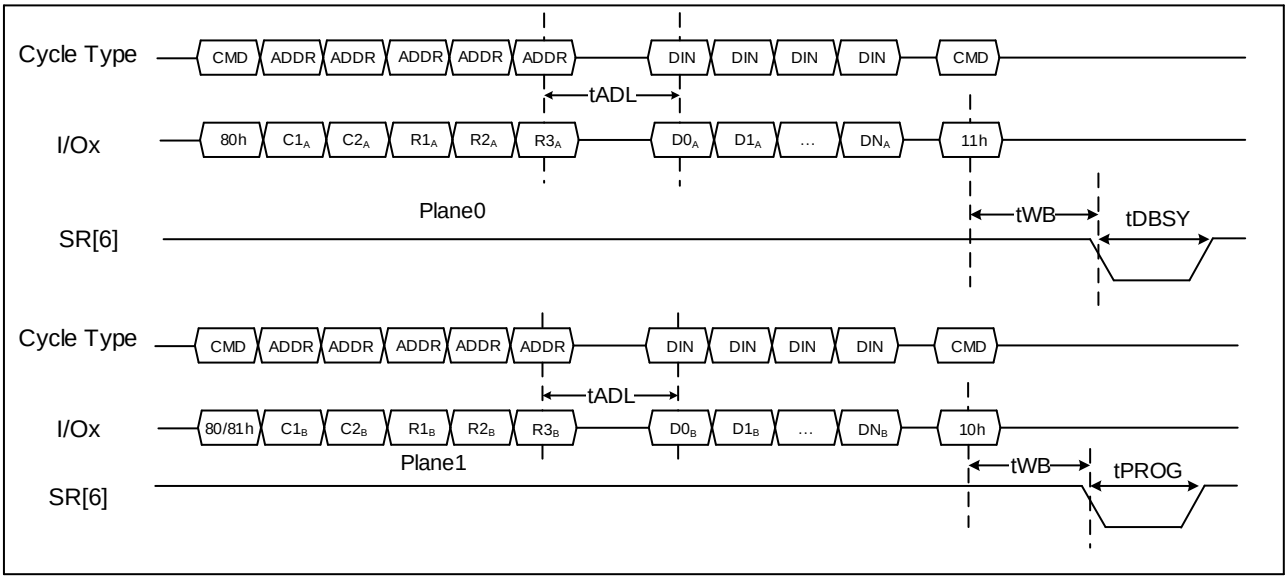


Figure 8-15:Multi-Plane Program sequential figures

In figure, the 80/81h is compatible traditional/ONFI multi-plane program.

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8.2.7 Multi-Plane Re-Program (8BH-11H-8BH-10H)

The operation is similar with multi-plane page program, the only different is use the 8BH substitute the command 80H, the data input is optional.

Starting plane address should be Plane0.

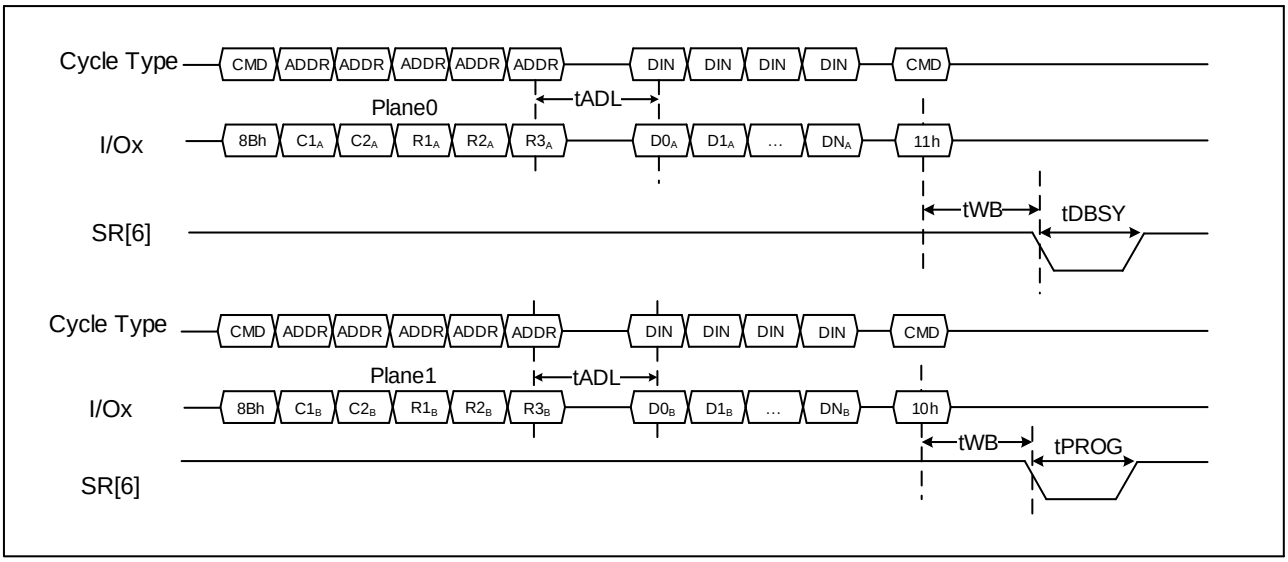


Figure 8-16:Multi-Plane Re-Program sequential figures

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8.2.8 Multi-Plane Cache Program (80H-11H-80/81H-15H-80H-11H-80/81H-10H)

The device supports multi-plane cache program, which enables high program throughput by programming two pages in parallel while exploiting the data and cache registers of both planes to implement cache program.

User can check operation status by R/B# pin or read status register commands (70h or 78h) If user opts for 70h, Status register read will provide a "global" information about the operation in the two planes.

More in detail:

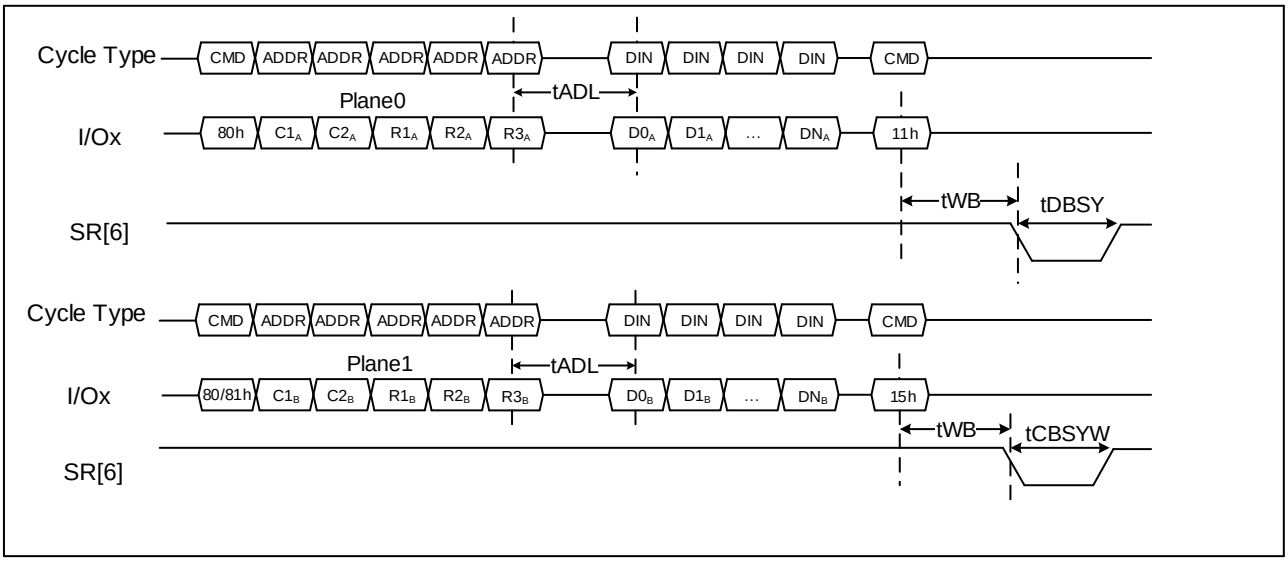
a) I/O6 indicates when both cache registers are ready to accept new data.

b) I/O5 indicates when the cell programming of the current cache registers is complete

c) I/O1 identifies if the previous pages in both planes (pages N-1) have been successfully programmed or not. The latter can be polled upon I/O6 status bit changing to "1".

d) I/O0 identifies if any error has been detected by the program / erase controller while programming the two pages N. The latter can be polled upon I/O5 status bit changing to "1". If the system monitor the progress of the operation only with R/B#, the last pages of the target program sequence must be programmed with Page Program Confirm command (10h). If the Cache Program command (15h) is used instead, the status bit I/O5 must be polled to find out if the last programming is finished before starting any other operation.

Starting plane address should be Plane0.



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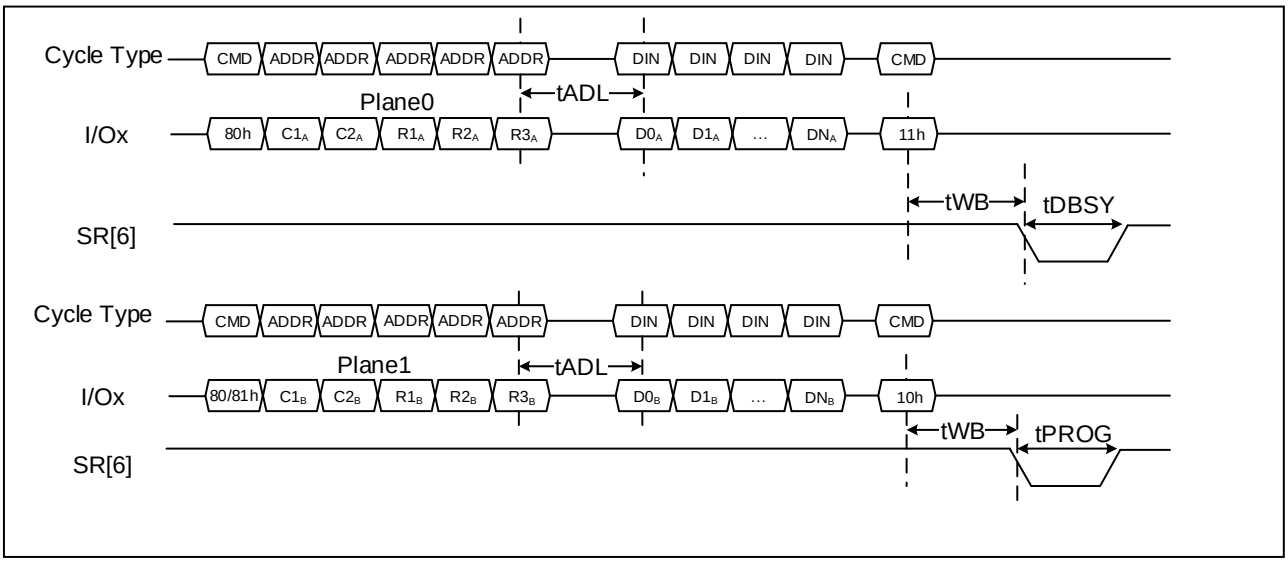


Figure 8-17: Multi-Plane Cache Program sequential figures

8.2.9 Multi-Plane Copy Back Program (85H-11H-85H-10H)

The Two-Plane Copy-Back Program is an extension of the Copy-back Program. As for page program, device supports Multi-plane copy back program with exactly same sequence and limitations. Multi-plane copy back program must be preceded by 2 single page read for copy back command sequences. Starting plane address should be Plane0.

Multi-plane copy back cannot cross plane boundary, the contents of the source page of one device plane can be copied only to a destination page of the same plane.

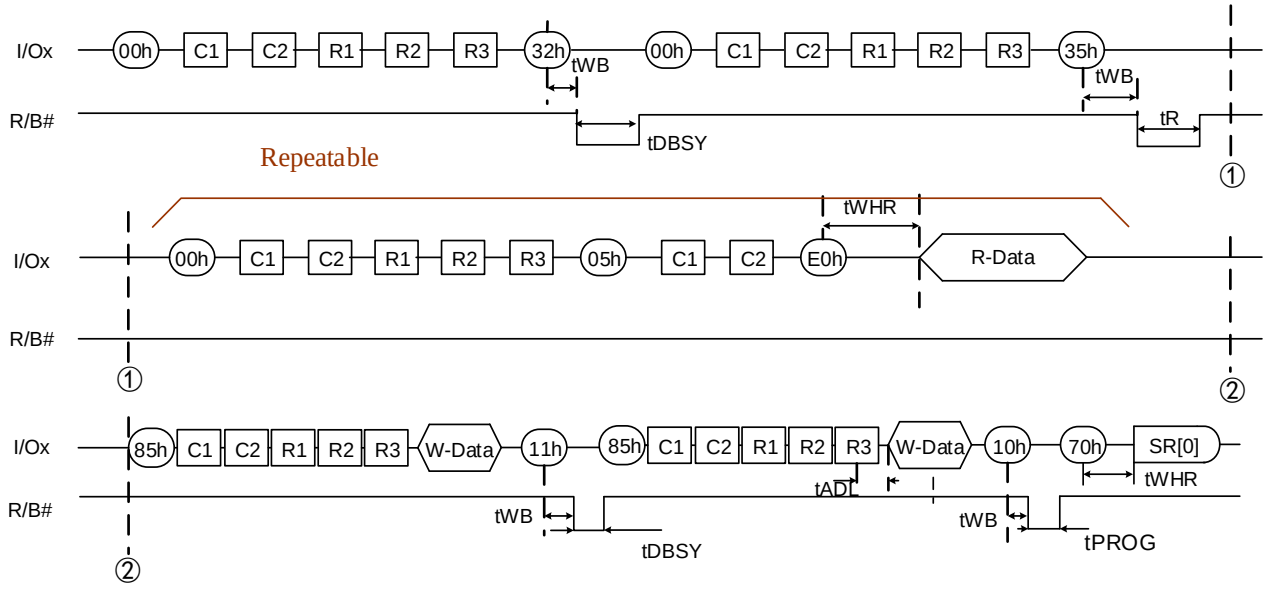


Figure 8-18: Multi-Plane Copy Back Program sequential figures

Note: the data followed with 85h command is optional.

8.3 Block Erase Operation

8.3.1 Common Block Erase Operation (60H-D0H)

The Erase operation is done on a block basis. Block address loading is accomplished in three cycles initiated by an Erase Setup command (60H). Row Address is valid while Column Addresses ignored. The Erase Confirm command (D0H) following the block address loading initiates the internal erasing process. At the rising edge of WE# after the erase confirm command input, the internal write controller handles erase and erase verify. Once the erase process starts, the Read Status Register command may be entered to read the status register. The system controller can detect the completion of an erase by monitoring the R/B# output, or the Status bit (I/O6) of the Status Register. Only the Read Status command and Reset command are valid while erasing is in progress. When the erase operation is completed, the Write Status Bit (I/O 0) may be checked.

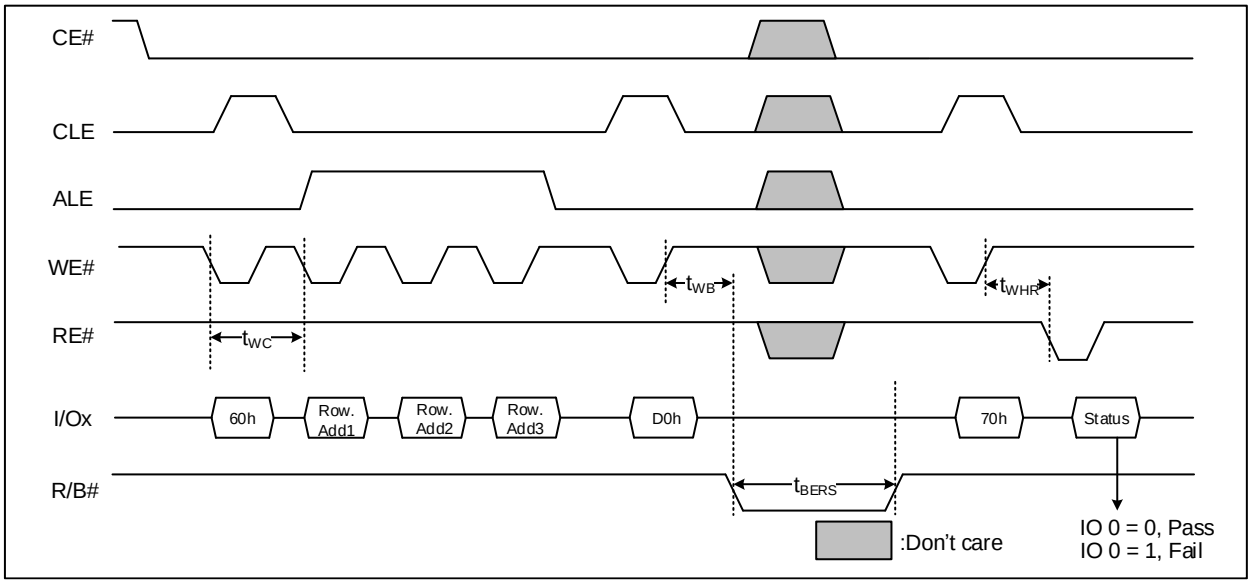


Figure 8-19: Common Block Erase Operation figures

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8.3.2 Multi-Plane Block Erase Operation (60H-60H-D0H)

Multi-plane Block Erase allows the erase of two blocks in parallel, one block per memory plane.

The Block erase setup command (60h) must be repeated two times, followed by 1st and 2nd block address respectively (3 cycles each). As for block erase, D0h command makes embedded operation start. In this case, multi-plane erase does not need any Dummy Busy Time between 1st and 2nd block insertion and should obey the multi-plane operation rule.

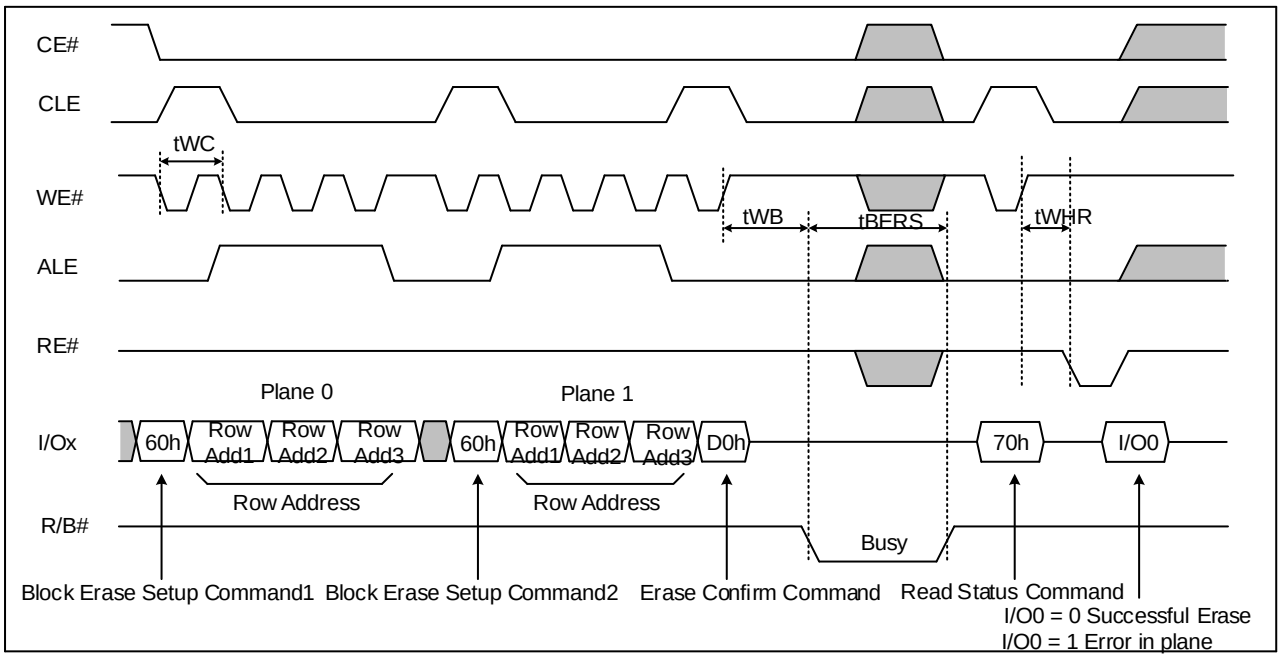


Figure 8-20: Multi-Plane Block Erase Operation sequential figures

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8.3.3 Multi-Plane Block Erase Operation-ONFI (60H-D1H)

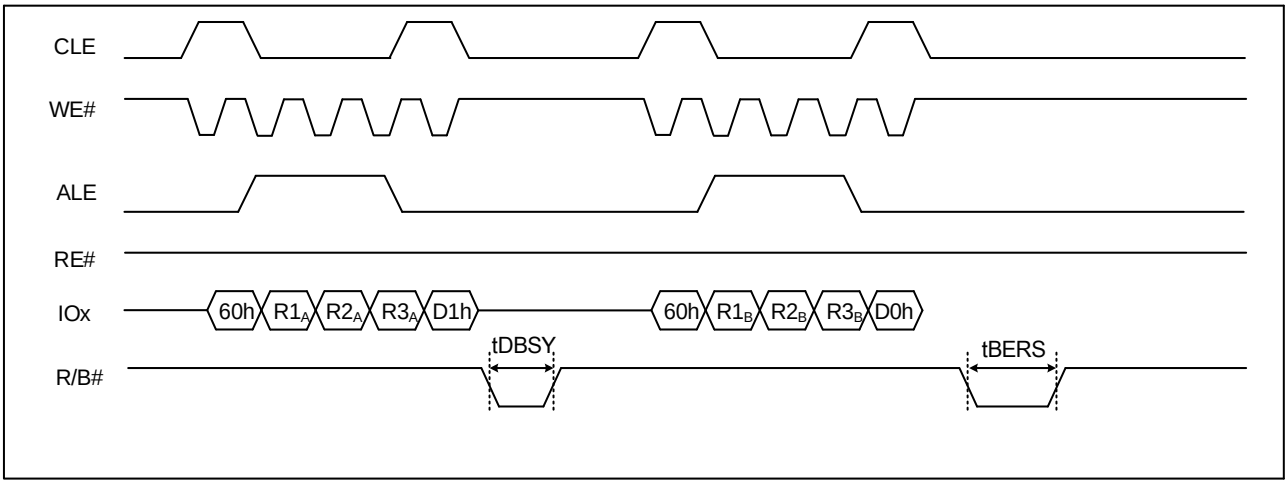


Figure 8-21: Multi-plane Block Erase Operation-ONFI sequential figures

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8.4 Reset (FFH)

8.4.1 Reset (FFH)

The device offers a reset feature, executed by writing FFH to the command register. When the device is in busy state during random read, program or erase mode, the reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The command register is cleared to wait for the next command, and the Status Register is cleared to value E0h when R/B# is high and WP# is high. If the device is already in reset state a new reset command will be accepted by the command register. The R/B# pin will change to low for tRST after the Reset command is written.

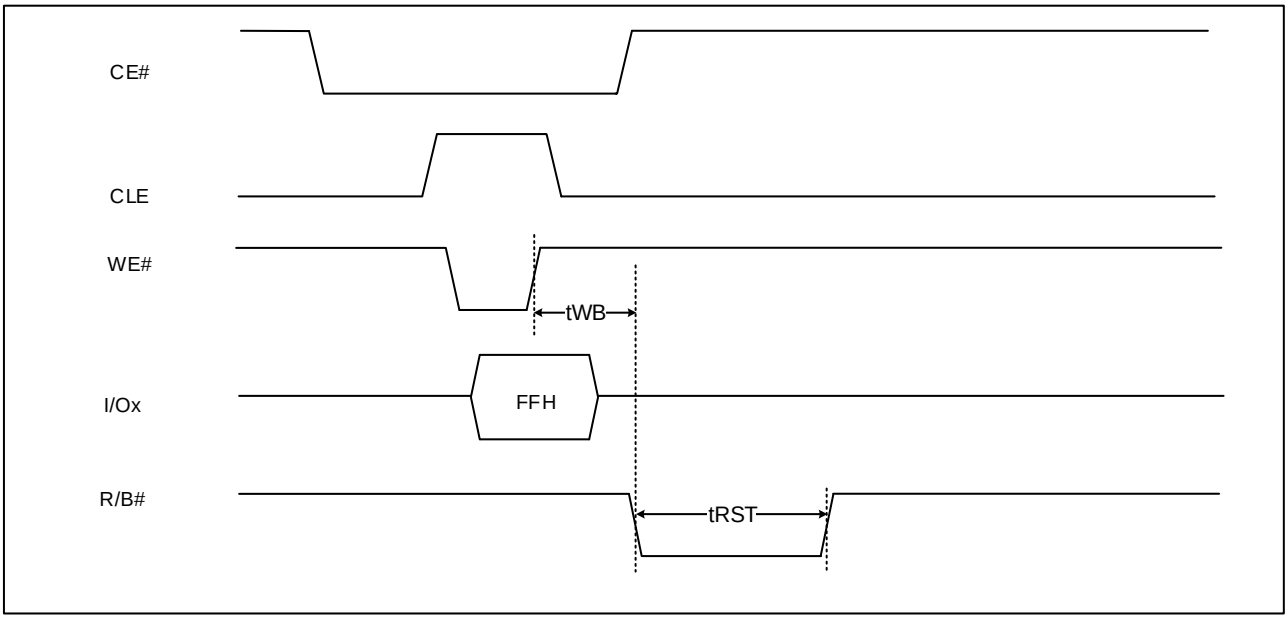


Figure 8-22: Reset (FFH) figures

8.4.2 Reset LUN (FAH)

A certain LUN within a target can be reset by command FAh followed by row address, Row address are required to set a LUN to be reset, follow figure define the reset LUN behavior and timings.

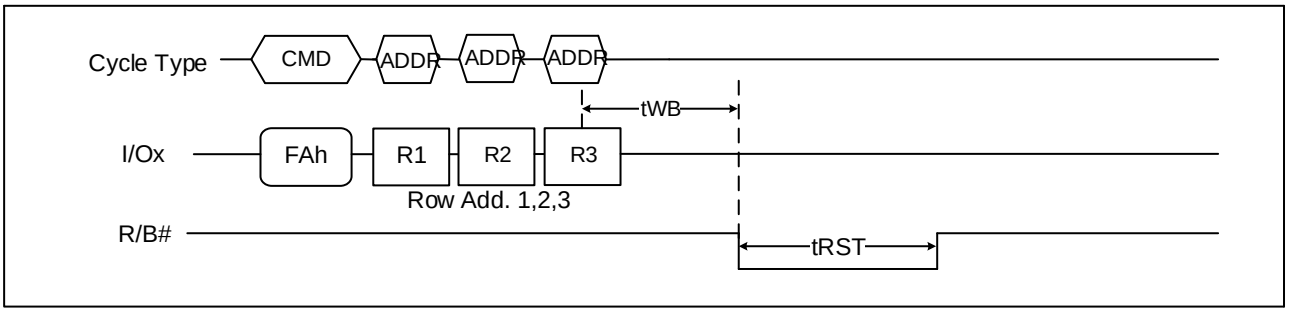


Figure 8-23: Reset LUN sequential figures

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8.5 Read Device Information

8.5.1 Read ID and ONFI Signature (90H)

The device contains a product identification mode, initiated by writing 90H to the command register, followed by an address input of 00H. Five read cycles sequentially output the manufacturer code, and the device code and other information, respectively. The command register remains in Read ID mode until further commands are issued to.

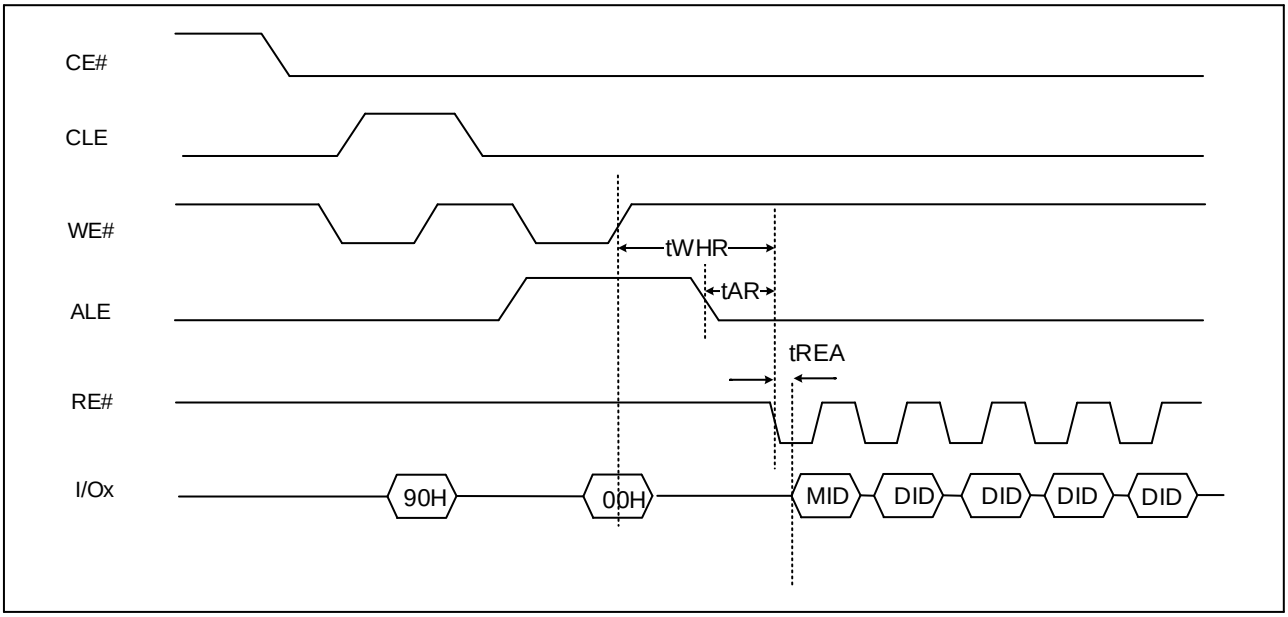


Figure 8-24: Read ID figures

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ID Definition Table

Byte	Description
1st Byte	Manufacturer Code (MID)
2nd Byte	Device Code (DID)
3rd Byte	Internal Chip Number, Cell Type, Number of Simultaneously Programmed Pages, Interleaved Program, Write Cache
4th Byte	Page size, Block size, Spare size, Organization
5th Byte	ECC & Plane

Read ID Data Table

Part Number	VCC	Bus Width	MID(1st)	DID(2nd)	3rd	4th	5th
GD9FU4G8F3A	3.3v	x8	C8H	DCH	90H	95H	56H
GD9FU4G6F3A	3.3v	x16	C8H	CCH	90H	D5H	56H
GD9FS4G8F3A	1.8v	x8	C8H	ACH	90H	15H	56H
GD9FS4G6F3A	1.8v	x16	C8H	BCH	90H	55H	56H
GD9FU8G8E3A	3.3v	x8	C8H	D3H	D1H	95H	5AH
GD9FU8G6E3A	3.3v	x16	C8H	C3H	D1H	D5H	5AH
GD9FS8G8E3A	1.8v	x8	C8H	A3H	D1H	15H	5AH
GD9FS8G6E3A	1.8v	x16	C8H	B3H	D1H	55H	5AH
GD9FUAG8D3A	3.3v	x8	C8H	D5H	D2H	95H	5EH
GD9FUAG6D3A	3.3v	x16	C8H	C5H	D2H	D5H	5EH
GD9FSAG8D3A	1.8v	x8	C8H	A5H	D2H	15H	5EH
GD9FSAG6D3A	1.8v	x16	C8H	B5H	D2H	55H	5EH

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3rd Byte of Device Identifier Description

3rd Cycle	Description	IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0
Internal Chip Number	1							0	0
	2							0	1
	4							1	0
	8							1	1
Cell Type	2 Level Cell					0	0		
	4 Level Cell					0	1		
	8 Level Cell					1	0		
	16 Level Cell					1	1		
Number of Simultaneously Programmed Pages	1			0	0				
	2			0	1				
	4			1	0				
	8			1	1				
Interleaved Program Between Multiple Die	Not Supported		0						
	Supported		1						
Write Cache (Cache Programming)	Not Supported	0							
	Supported	1							

4th Byte of Device Identifier Description

4th Cycle	Description	IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0
Page Size (without Spare Area)	1KB							0	0
	2KB							0	1
	4KB							1	0
	8KB							1	1
Size of spare area (byte per 512-byte)	16						1		
Serial Access Time	25ns	0				0			
	20ns	1				0			
Block Size (Without Spare Area)	64KB			0	0				
	128KB			0	1				
	256KB			1	0				
	512KB			1	1				
Organization	x8		0						
	x16		1						

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5th Byte of ECC & Plane

5th Cycle	Description	IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0
ECC Level	1							0	0
	2							0	1
	4							1	0
	8							1	1
Plane Number per CE#	1					0	0		
	2					0	1		
	4					1	0		
	8					1	1		
Reserved			1	0	1				
Internal ECC	ECC disabled	0							
	ECC enabled	1							

To retrieve the ONFI signature, the command 90H together with an address of 20H shall be entered. The ONFI signature is the ASCII encoding of ‘ONFI’ where ‘O’ = 4FH, ‘N’ = 4EH, ‘F’ = 46H, and ‘I’ = 49H. Reading beyond four bytes yields indeterminate values.

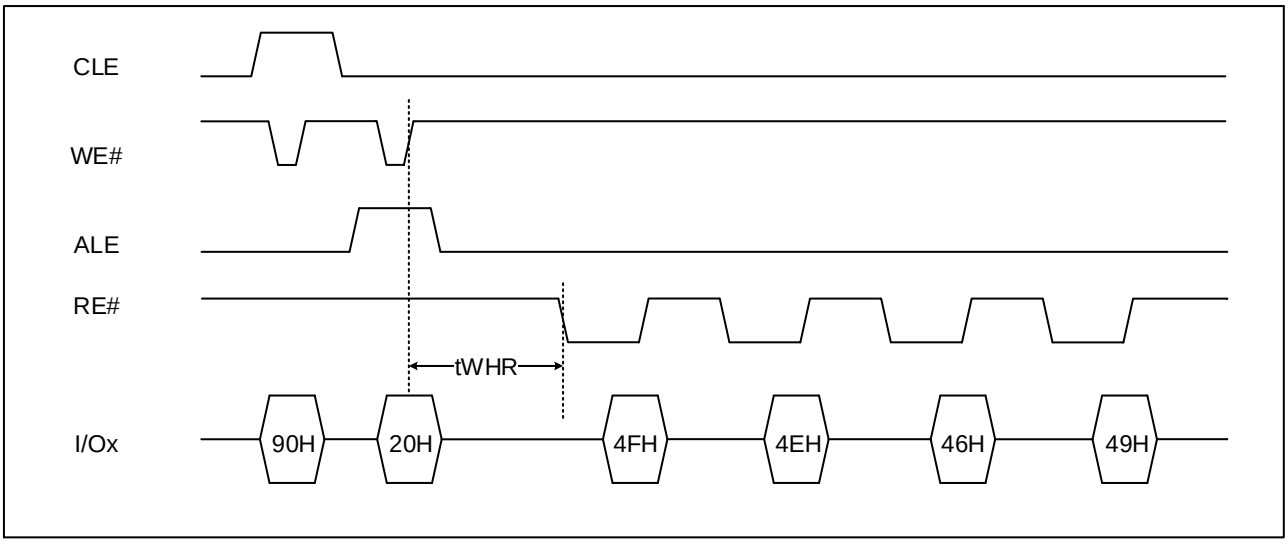


Figure 8-25: Read ONFI Signature figures

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8.5.2 Read Unique ID (EDH)

The Read Unique ID function is used to retrieve the 16 byte unique ID (UID) for the device. The unique ID when combined with the device manufacturer shall be unique.

The UID data may be stored within the Flash array. To allow the host to determine if the UID is without bit errors, the UID is returned with its complement. If the XOR of the UID and its bit-wise complement is all ones, then the UID is valid. To accommodate robust retrieval of the UID in the case of bit errors, sixteen copies of the UID and the corresponding complement shall be stored by the target. For example, reading bytes 32-63 returns to the host another copy of the UID and its complement.

To change the data output location, it is recommended to use the Random Data Out command set (05H-E0H).The Status Read command (70H) can be used to check the completion. To continue the read operation, a following read command (00h) to re-enable the data out is necessary.

Bytes	Value
0-15	UID
16-31	UID complement (bit-wise)

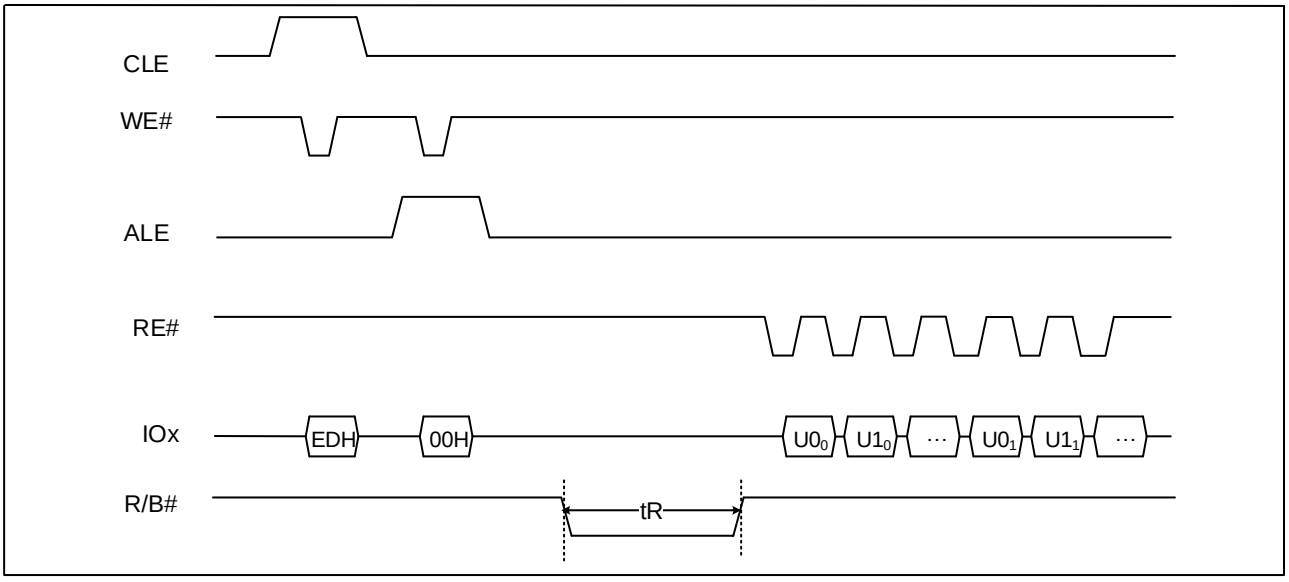


Figure 8-26: Read Unique ID figures

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8.5.3 Read Parameter Page (ECH)

The Read Parameter Page function retrieves the data structure that describes the chip's organization, features, timings- and other behavioral parameters. This data structure enables the host processor to automatically recognize the NAND Flash configuration of a device. A minimum of three copies of the parameter page are stored in the device. The Random Data Read command (05H-E0H) can be issued during execution of the read parameter page to read specific portion-soft the parameter page. The Read Status command (70H) may be used to check the status of read parameter page during execution. After completion of the Read Status command, 00H is issued by the host on the command line to continue with the data output flow for the Read Parameter Page command.

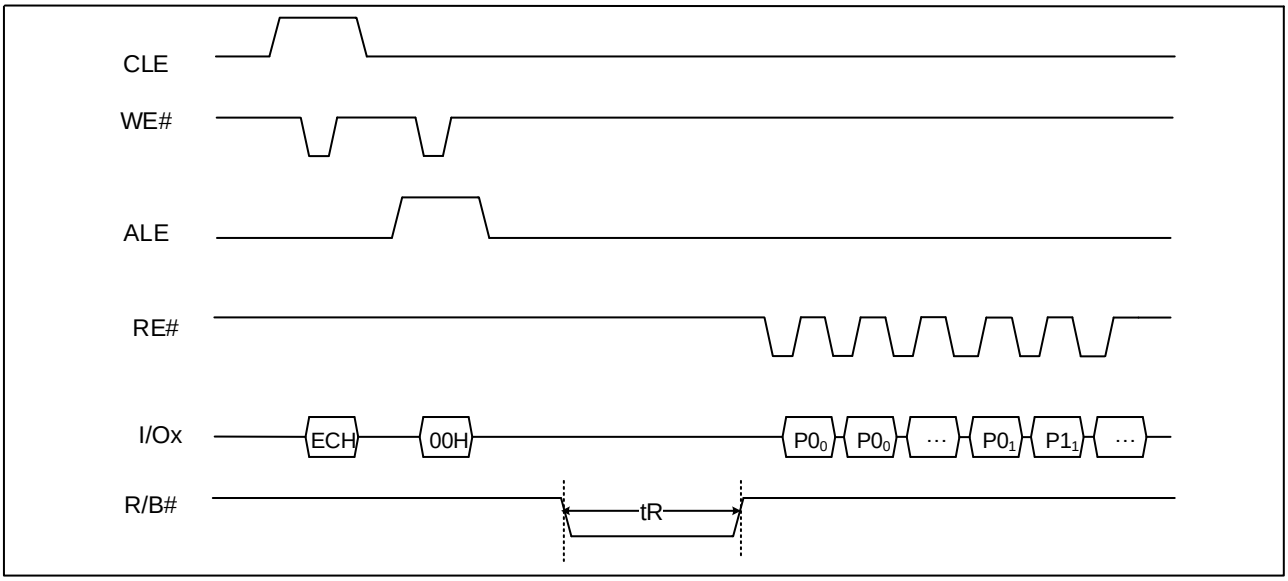


Figure 8-27: Read Parameter Page figures

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Byte	O/M	Description	4Gb	8Gb	16Gb
0-3	M	Parameter page signature Byte 0: 4FH, “O” Byte 1: 4EH, “N” Byte 2: 46H, “F” Byte 3: 49H, “I”	4FH 4EH 46H 49H	4FH 4EH 46H 49H	4FH 4EH 46H 49H
4-5	M	Revision number 2-15 Reserved (0) 1 1 = supports ONFI version 1.0 0 Reserved (0)	02H 00H	02H 00H	02H 00H
6-7	M	Features supported 5-15 Reserved (0) 4 1 = supports odd to even page Copy back 3 1 = supports interleaved operations 2 1 = supports non-sequential page programming 1 1 = supports multiple LUN operations 0 1 = supports 16-bit data bus width	18H(X8)/ 19H(X16) 00H	1AH(X8)/ 1BH(X16) 00H	1AH(X8)/ 1BH(X16) 00H
8-9	M	Optional commands supported 6-15 Reserved (0) 5 1 = supports Read Unique ID 4 1 = supports Copy−back 3 1 = supports Read Status Enhanced 2 1 = supports Get Features and Set Features 1 1 = supports Read Cache Integrity 0 1 = supports Page Cache Program command	3FH 00H	3FH 00H	3FH 00H
10-31		Reserved (0)	00H … 00H	00H … 00H	00H … 00H
		Manufacturer Information block			
32-43	M	Device manufacturer (12 ASCII characters)“GIGADEVICE”	47H 49H 47H 41H 44H 45H 56H 49H 43H 45H 20H 20H	47H 49H 47H 41H 44H 45H 56H 49H 43H 45H 20H 20H	47H 49H 47H 41H 44H 45H 56H 49H 43H 45H 20H 20H

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<table>
<tr><td>44-63</td><td>M</td><td>Device model (20 ASCII characters)
<table><tr><th>Device Model</th><th>ORGANIZATION</th><th>VCC RANGE</th></tr><tr><td>GD9FU4G8F3A</td><td>512M x 8bit</td><td>2.7v ~ 3.6v</td></tr><tr><td>GD9FU4G6F3A</td><td>256M x 16bit</td><td>2.7v ~ 3.6v</td></tr><tr><td>GD9FS4G8F3A</td><td>512M x 8bit</td><td>1.7v ~ 1.95v</td></tr><tr><td>GD9FS4G6F3A</td><td>256M x 16bit</td><td>1.7v ~ 1.95v</td></tr><tr><td>GD9FU8G8E3A</td><td>1G x 8bit</td><td>2.7v ~ 3.6v</td></tr><tr><td>GD9FU8G6E3A</td><td>512M x 16bit</td><td>2.7v ~ 3.6v</td></tr><tr><td>GD9FS8G8E3A</td><td>1G x 8bit</td><td>1.7v ~ 1.95v</td></tr><tr><td>GD9FS8G6E3A</td><td>512M x 16bit</td><td>1.7v ~ 1.95v</td></tr><tr><td>GD9FUAG8D3A</td><td>2G x 8bit</td><td>2.7v ~ 3.6v</td></tr><tr><td>GD9FUAG6D3A</td><td>1G x 16bit</td><td>2.7v ~ 3.6v</td></tr><tr><td>GD9FSAG8D3A</td><td>2G x 8bit</td><td>1.7v ~ 1.95v</td></tr><tr><td>GD9FSAG6D3A</td><td>1G x 16bit</td><td>1.7v ~ 1.95v</td></tr></table></td><td>47H
44H
39H
46H
53H/55H
(1.8V/3.3V)
34H
47H
38H/36H
(X8/X16)
46H
33H
41H
20H
20H
20H
20H
20H
20H
20H
20H</td><td>47H
44H
39H
46H
53H/55H
(1.8V/3.3V)
38H
47H
38H/36H
(X8/X16)
45H
33H
41H
20H
20H
20H
20H
20H
20H
20H
20H</td><td>47H
44H
39H
46H
53H/55H
(1.8V/3.3V)
41H
47H
38H/36H
(X8/X16)
44H
33H
41H
20H
20H
20H
20H
20H
20H
20H
20H</td></tr>
<tr><td>64</td><td>M</td><td>JEDEC manufacturer ID“C8”</td><td>C8H</td><td>C8H</td><td>C8H</td></tr>
<tr><td>65-66</td><td>O</td><td>Date code</td><td>00H
00H</td><td>00H
00H</td><td>00H
00H</td></tr>
<tr><td>67-79</td><td></td><td>Reserved</td><td>00H
00H
00H</td><td>00H
00H
00H</td><td>00H
00H
00H</td></tr>
<tr><td></td><td></td><td>Memory organization block</td><td></td><td></td><td></td></tr>
<tr><td>80-83</td><td>M</td><td>Number of data bytes per page</td><td>00H
08H
00H
00H</td><td>00H
08H
00H
00H</td><td>00H
08H
00H
00H</td></tr>
<tr><td>84-85</td><td>M</td><td>Number of spare bytes per page</td><td>40H
00H</td><td>40H
00H</td><td>40H
00H</td></tr>
<tr><td>86-89</td><td>M</td><td>Number of data bytes per partial page</td><td>00H
02H
00H
00H</td><td>00H
02H
00H
00H</td><td>00H
02H
00H
00H</td></tr>
<tr><td>90-91</td><td>M</td><td>Number of spare bytes per partial page</td><td>10H
00H</td><td>10H
00H</td><td>10H
00H</td></tr>
<tr><td>92-95</td><td>M</td><td>Number of pages per block</td><td>40H
00H
00H</td><td>40H
00H
00H</td><td>40H
00H
00H</td></tr>
</table>

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			00H	00H	00H
96-99	M	Number of blocks per logical unit (LUN)	00H 10H 00H 00H	00H 10H 00H 00H	00H 10H 00H 00H
100	M	Number of logical units (LUNs)	01H	02H	04H
101	M	Number of address cycles 4-7 Column address cycles 0-3 Row address cycles	23H	23H	23H
102	M	Number of bits per cell	01H	01H	01H
103-104	M	Bad blocks maximum per LUN	50H 00H	50H 00H	50H 00H
105-106	M	Block endurance	01H 05H	01H 05H	01H 05H
107	M	Guaranteed valid blocks at beginning of target	08H	08H	08H
108-109	M	Block endurance for guaranteed valid blocks	00H 00H	00H 00H	00H 00H
110	M	Number of programs per page	04H	04H	04H
111	M	Partial programming attributes 5-7 Reserved 4 1 = partial page layout is partial page data followed by partial page spare 1-3 Reserved 0 1 = partial page programming has constraints	00H	00H	00H
112	M	Number of bits ECC correct ability	04H	04H	04H
113	M	Number of interleaved address bits 4-7 Reserved (0) 0-3 Number of interleaved address bits	01H	01H	01H
114	O	Interleaved operation attributes 4-7 Reserved (0) 3 1 = Address restrictions for program cache 2 1 = program cache supported 1 1 = no block address restrictions 0 1= Overlapped / concurrent interleaving support	0EH	0EH	0EH
115-127		Reserved	00H … 00H	00H … 00H	00H … 00H
		Electrical parameters block			
128	M	I/O capacitance	06H	10H	20H

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129-130	M	Timing mode support 6-15 Reserved (0) 5 1 = supports timing mode 5 4 1 = supports timing mode 4 3 1 = supports timing mode 3 2 1 = supports timing mode 2 1 1 = supports timing mode 1 0 1 = supports timing mode 0, shall be 1	3FH(3.3V)/ 1FH(1.8V) 00H	3FH(3.3V)/ 1FH(1.8V) 00H	3FH(3.3V)/ 1FH(1.8V) 00H
131-132	O	Program cache timing mode support 6-15 Reserved (0) 5 1 = supports timing mode 5 4 1 = supports timing mode 4 3 1 = supports timing mode 3 2 1 = supports timing mode 2 1 1 = supports timing mode 1 0 1 = supports timing mode 0,	3FH(3.3V)/ 1FH(1.8V) 00H	3FH(3.3V)/ 1FH(1.8V) 00H	3FH(3.3V)/ 1FH(1.8V) 00H
133-134	M	tPROG Maximum page program time (us)	58H 02H	58H 02H	58H 02H
135-136	M	tBERS Maximum block erase time (us)	10H 27H	10H 27H	10H 27H
137-138	M	tR Maximum page read time (us)	19H 00H	19H 00H	19H 00H
139-140	M	tCCS Minimum Change Column setup time (ns) (N/A)	2CH 01H	2CH 01H	2CH 01H
141-163		Reserved	00H	00H	00H
		Vendor block			
164-165	M	Vendor specific Revision number	00H	00H	00H
166-253		Vendor specific	00H	00H	00H
254-255	M	Integrity CRC			
		Redundant parameter pages			
256-511	M	Value of bytes 0-255			
512-767	M	Value of bytes 0-255			
768+	O	Additional redundant parameter pages			

Notes:

1. “O” Stands for Optional, “M” for Mandatory
2. The Integrity CRC (Cycling Redundancy Check) field is used to verify that the contents of the parameters page were transferred correctly to the host. Please refer to ONFI 1.0 specifications for details.

   The CRC shall be calculated using the following 16-bit generator polynomial: $G(X) = X16 + X15 + X2 + 1$, This polynomial in hex may be represented as 8005h.

3. The CRC value shall be initialized with a value of 4F4Eh before the calculation begins. There is no XOR applied to the final CRC value after it is calculated. There is no reversal of the data bytes or the CRC calculated value.

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Parameter page CRC value table

Device Model	ORGANIZATION	VCC RANGE	CRC value B254/B255
GD9FS4G8F3A	512M x 8bit	1.7v ~ 1.95v	F8H/59H
GD9FS4G6F3A	256M x 16bit	1.7v ~ 1.95v	D0H/9AH
GD9FU4G8F3A	512M x 8bit	2.7v ~ 3.6v	B8H/A8H
GD9FU4G6F3A	256M x 16bit	2.7v ~ 3.6v	90H/6BH
GD9FS8G8E3A	1G x 8bit	1.7v ~ 1.95v	AFH/6EH
GD9FS8G6E3A	512M x 16bit	1.7v ~ 1.95v	87H/ADH
GD9FU8G8E3A	1G x 8bit	2.7v ~ 3.6v	EFH/9FH
GD9FU8G6E3A	512M x 16bit	2.7v ~ 3.6v	C7H/5CH
GD9FSAG8D3A	2G x 8bit	1.7v ~ 1.95v	16H/00H
GD9FSAG6D3A	1G x 16bit	1.7v ~ 1.95v	3EH/C3H
GD9FUAG8D3A	2G x 8bit	2.7v ~ 3.6v	56H/F1H
GD9FUAG6D3A	1G x 16bit	2.7v ~ 3.6v	7EH/32H

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8.6 Read Status (70H)

The device contains a Status Register which may be read to find out whether an operation is completed and whether the program or erase operation is completed successfully. After writing 70H command to the command register, a read cycle outputs the content of the Status Register to the I/O pins on the falling edge of CE# or RE#, whichever occurs last. This allows the system to poll the progress of each device in multiple memory connections even when R/B# pins are common-wired. RE# or CE# does not need to be toggled for updated status. The command register remains in Status Read mode until further commands are issued to it. Therefore, if the status register is read during a random read cycle, the read command (00h) should be given before starting read cycles.

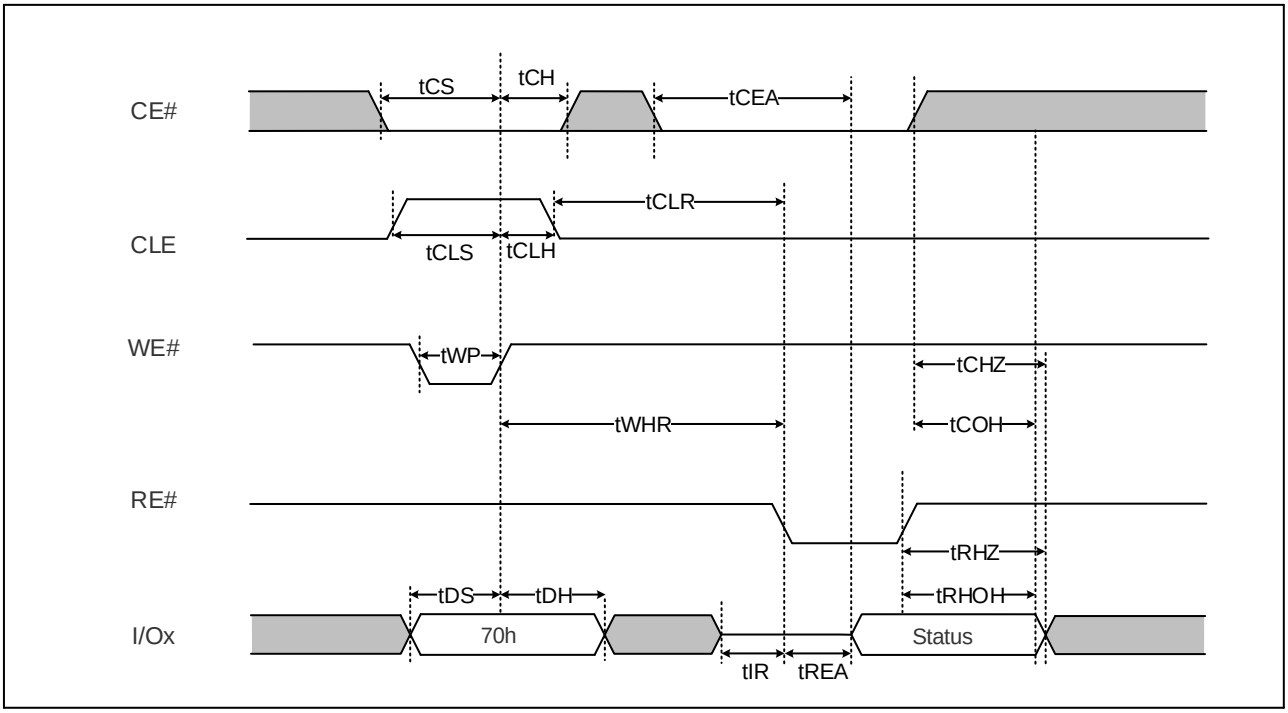


Figure 8-28: Read Status figures

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I/O No.	Page Program	Block Erase	Cache Program	Read	Cache Read	Definition
I/O0	Pass/Fail	Pass/Fail	Pass/Fail(N)	-	-	FAIL N Page Pass : 0 Fail : 1
I/O1	-	-	Pass/Fail(N-1)	-	-	FAILC N-1 Page Pass : 0 Fail : 1
I/O2	-	-	-	-	-	Don't Care
I/O3	-	-	-	-	-	Don't Care
I/O4	-	-	-	-	-	Don't Care
I/O5	Ready/Busy	Ready/Busy	Ready/Busy	Ready/Busy	Ready/Busy	ARDY Ready/Busy for Array Operation Busy : 0 Ready : 1
I/O6	Ready/Busy	Ready/Busy	Ready/Busy	Ready/Busy	Ready/Busy	RDY Ready/Busy Busy : 0 Ready : 1
I/O7	Write Protect	Write Protect	Write Protect	Write Protect	Write Protect	WP# Protected:0 Not Protected:1

Notes:

1. I/O0: This bit is only valid for Program and Erase operations. During Cache Program operations, this bit is only valid when I/O5 is set to 1.
2. I/O1: This bit is only valid for cache program operations. This bit is not valid until after the second 15h command or the 10h command has been transferred in a Cache program sequence.
3. I/O5: If set to one, then there is no array operation in progress. If cleared to zero, then there is a command being processed (I/O6 is cleared to zero) or an array operation in progress.
4. I/O6: When cache operations are in use, then this bit indicates whether another command can be accepted, and I/O5 indicates whether the operation is complete.
5. I/O7: the bit indicates if the block is protected, which include WP# protection and other protection.

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8.7 Read Status Enhanced – ONFI (78H)

Read Status Enhanced is an additional feature used to retrieve the status value for a previous Operation in the following cases:

- On a specific die of a multi-die stack configurations (single CE#), in case of concurrent operations

When the die are stacked (*) to form DDP or QDP (single CE#), it is possible to run a first operation on the first die, then activate a concurrent operation on the second (or third or fourth) device. (Examples: Erase while Read, Read while Program, etc.)

- On a specific plane in case of multi-plane operations in the same die.

Follow figure defines the Read Status Enhanced behavior and timings. Writing 78h to the command register, followed by three row address cycles containing the page, block, and LUN addresses.

The command register remains in Status Read mode until further commands are issued.

Read Status Enhanced command is prohibited during the reset (FFH) command and when OTP mode is enable.

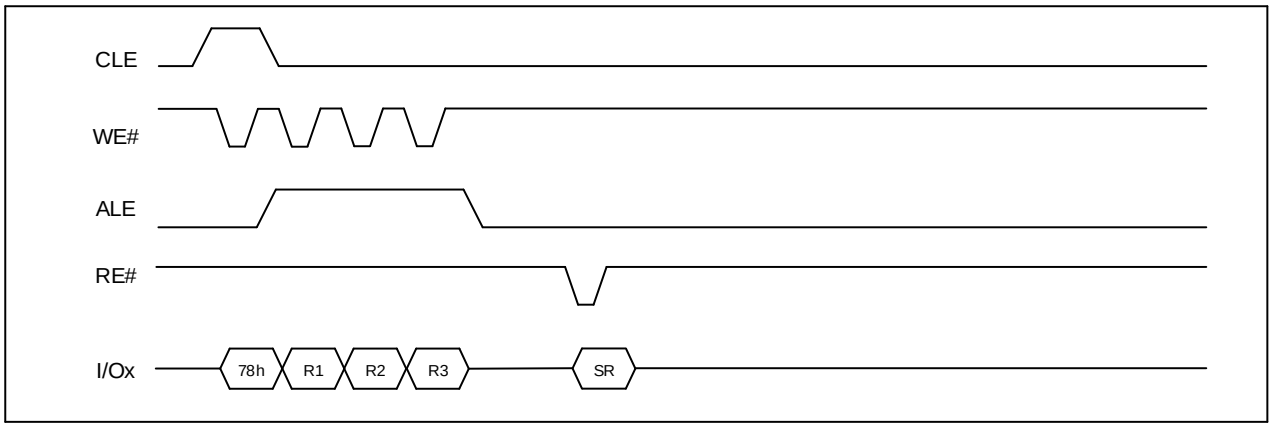


Figure 8-29: Read Status Enhanced-ONFI sequential figures

Note: SR, status register

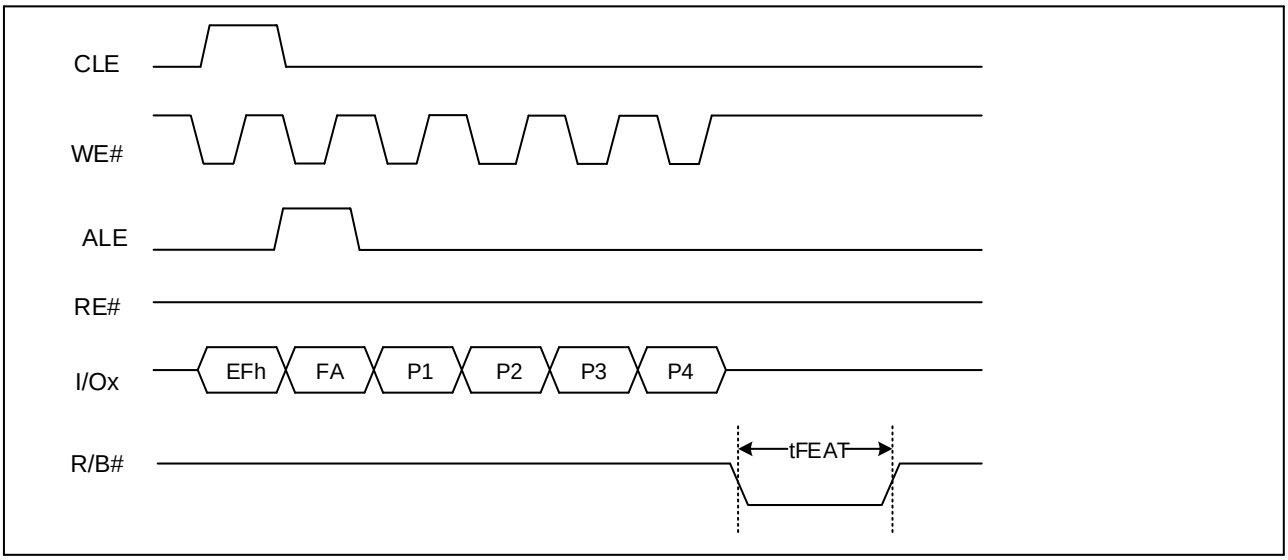
R1/R2/R3: row address for status read.

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8.8 Set Feature (EFH)

Users may set particular features using 'Set Feature' operation. Once a feature is set by users, it shall not be changed until the device is powered off or setting is changed by users. Figure of "Set Feature Sequence" defines the Set Features behavior and timings and follow Table defines features that users can change. These settings are not retained across the power off. Note that FFh command is not allowed during SET FEATURE sequence.

The NAND device may remain the current feature set until next power cycle since the feature set data is volatile. However, the reset command (FFh) cannot reset the current feature setting unless otherwise specified in the features table



Note: FA, feature address

Figure 8-30: Set Feature (EFH) sequential figures

Table Feature address define

Command cycle	Feature address	Description
EFH	10h	Output Driver strength setting
	Other	Reserved

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Table Feature address 10h: Output Driver strength setting

Feature parameter	Option	IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0	value	Note
P1	Overdrive2	0	0	0	0	0	0	0	0	00h	1
	Overdrive1	0	0	0	0	0	0	0	1	01h	
	Normal	0	0	0	0	0	0	1	0	02h	
	Under drive	0	0	0	0	0	0	1	1	03h	
P2	Reserved	0	0	0	0	0	0	0	0	00h	
P3	Reserved	0	0	0	0	0	0	0	0	00h	
P4	Reserved	0	0	0	0	0	0	0	0	00h	

Note1: Default is 00h

See follow Output Drive Strength Impedance Values table for details. Output Driver Strength Settings

Setting	Driver Strength	VCC
Overdrive 2	2.0x	3.3V/1.8V
Overdrive 1	1.4x	
Normal	1.0x	
Under drive	0.5x	

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8.9 Get Feature (EEH)

Users find how the target is set through 'Get Feature' command. The function shall return the current setting information. (Including modifications that may have been previously made with the Set Features function). If a host starts to read the first byte of data (i.e. P1 value), the host shall complete reading all four bytes of data before issuing another command (including Read Status or Read Status Enhanced). Follow figure of "Get Feature Sequence" defines the Get Features behavior and timings.

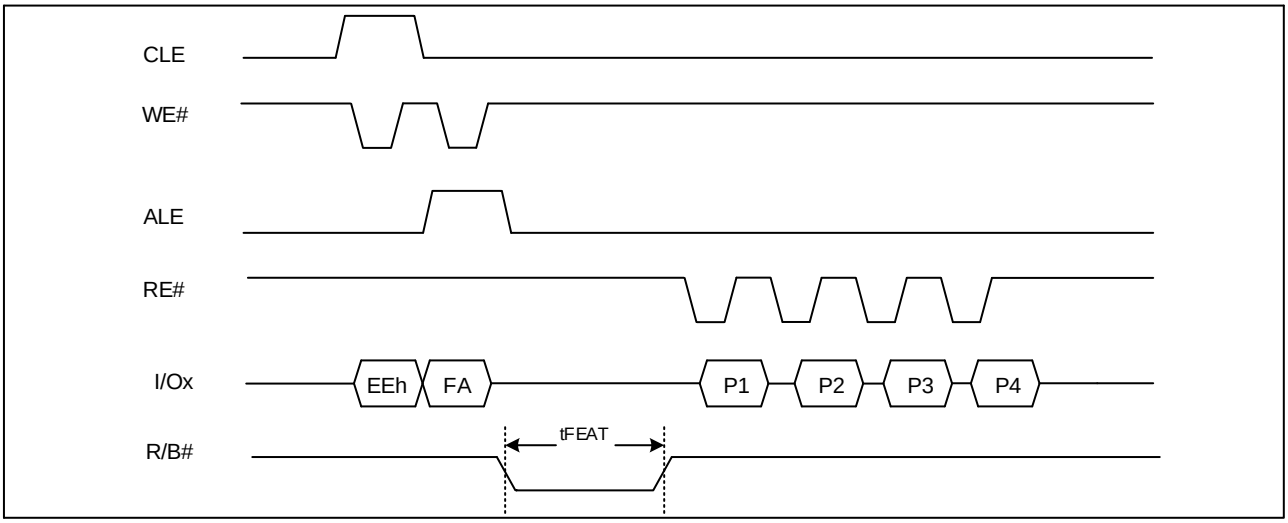


Figure 8-31: Get Feature (EEH) sequential figures

P1~P4 is the returned information with get feature command, which is same as the content of set feature command.

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8.10 Set LUN Feature (D5H)

The LUN Set Features (D5h) command functions the same as the target level Set Features (EFH) command except only the addressed LUNs settings are modified. .

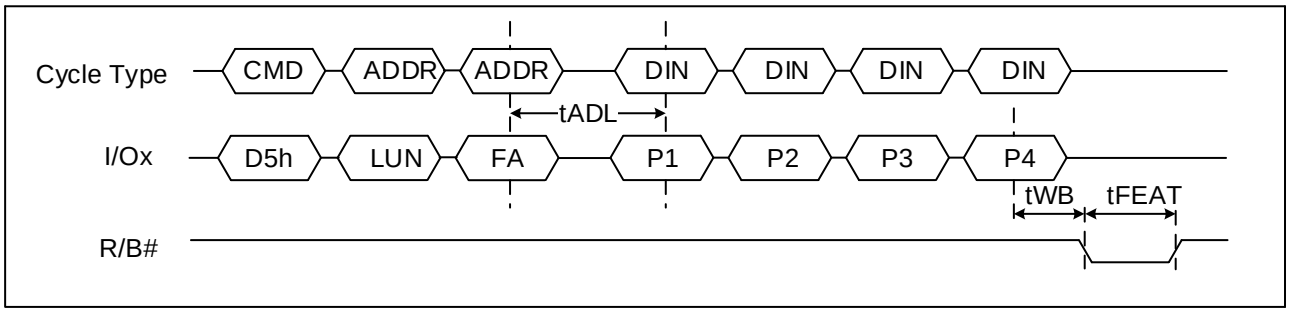


Figure 8-32: Set LUN Feature sequential figures

LUN Address: LUN 0 = 00h, LUN 1 = 01h, LUN 2 = 02h, LUN 3 = 03h.

FA Feature address identifying feature to modify settings for.

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8.11 Get LUN Feature (D4H)

The LUN Get Features (D4h) command functions the same as the target level Get Features (EEh) command except only the addressed LUNs settings are returned.

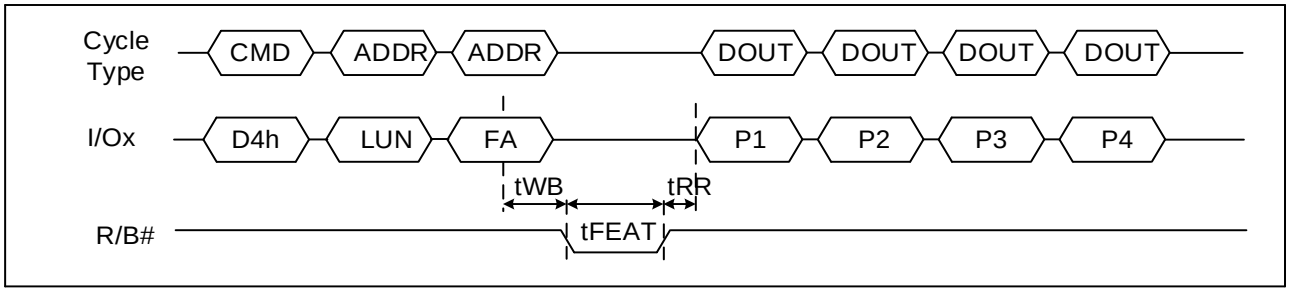


Figure 8-33: Get LUN Feature sequential figures

LUN Address: LUN 0 = 00h, LUN 1 = 01h, LUN 2 = 02h, LUN 3 = 03h.

FA Feature address identifying feature to modify settings for.

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8.12 Ready/Busy# (R/B#)

The device has a Ready/Busy output that provides method of indicating the completion of a page program, erase, copy-back and random read completion. The R/B# pin is normally high and goes to low when the device is busy (after a reset, read, program, and erase operation). It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more R/B# outputs to be Or-tied. Because pull-up resistor value is related to tR (R/B#), an appropriate value can be obtained with the following reference below chart. Its value can be determined by the following guidance.

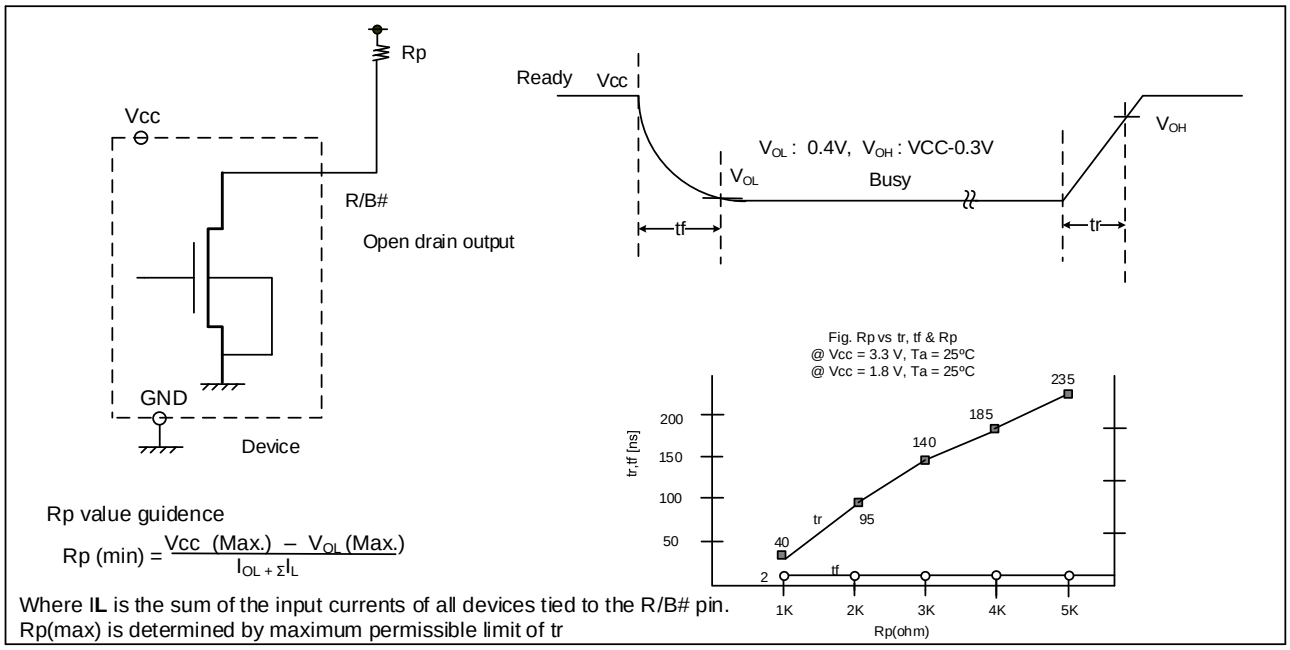


Figure 8- 41: Ready/Busy figures

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8.13 Data Protection & Power on/off Sequence

The device is designed to offer protection from any involuntary program/erase during power-transitions. WP# pin provides hardware protection and is recommended to be kept at V_{IL} during power-up and power-down.

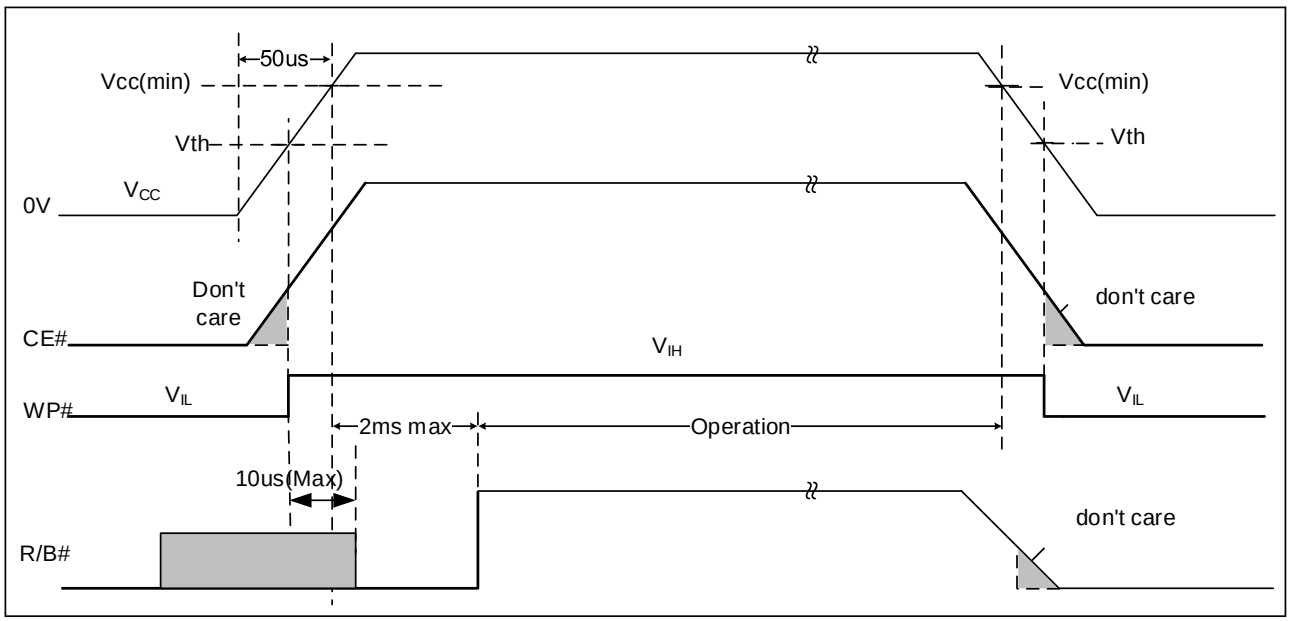


Figure 8-42_a: Data protection and Power on/off (3.3V Device)

Note: Vth=2.5v

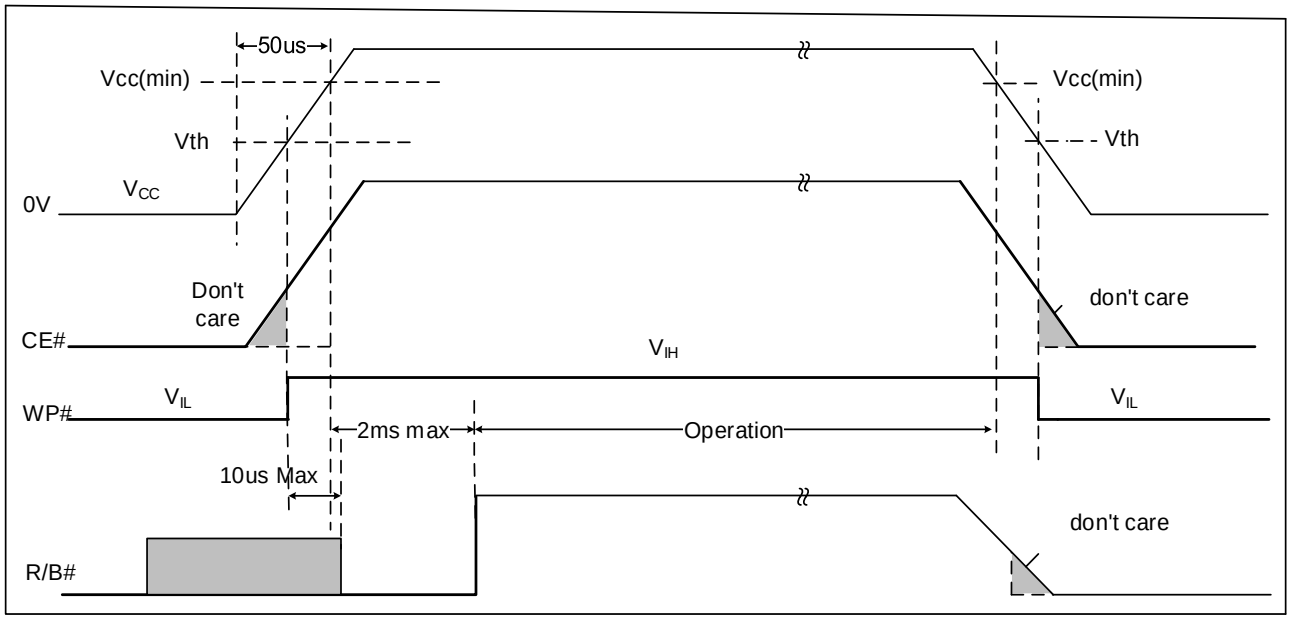


Figure 8-42_b: Data protection and Power on/off (1.8V Device)

Note: Vth=1.55v

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8.14 Multi-Plane Operation Limitation

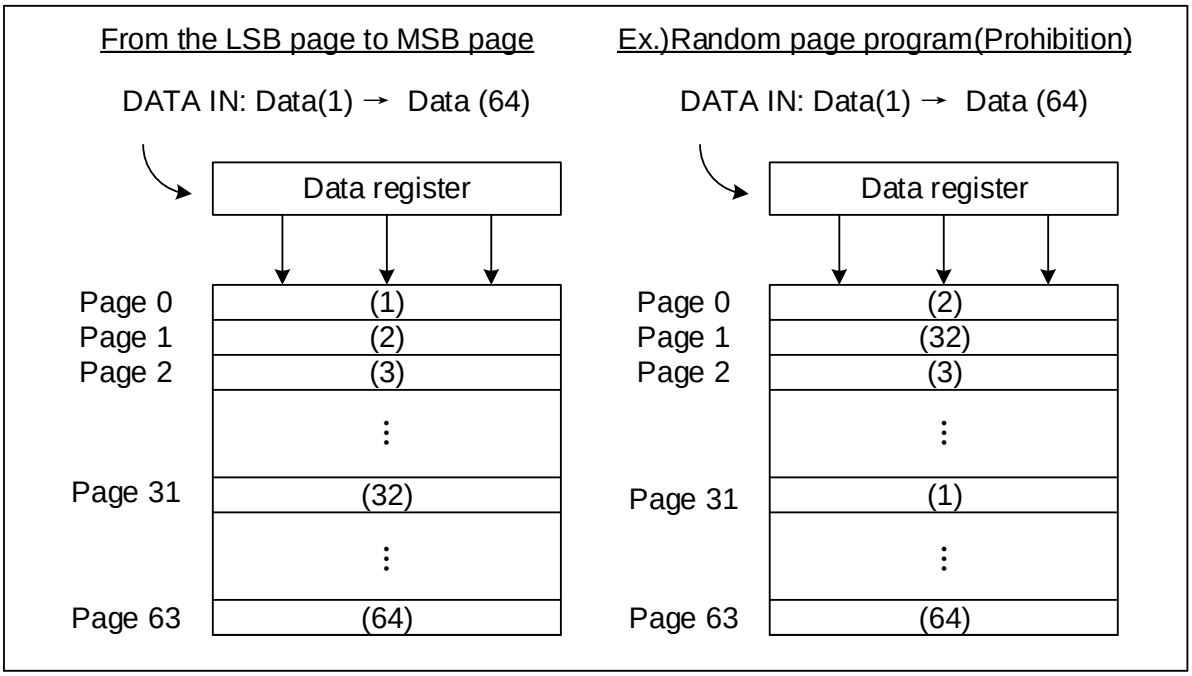
Multi-plane commands require an address per operational plane. For a given multi-plane operation, these addresses are subject to the following requirements:

- Multi-plane operation should in the same LUN.
- The plane address bits must be different for each issued address.
- The page address bits must be identical for each issued address.
- Multi-plane copy back cannot cross plane boundaries.

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8.15 Addressing for program operation

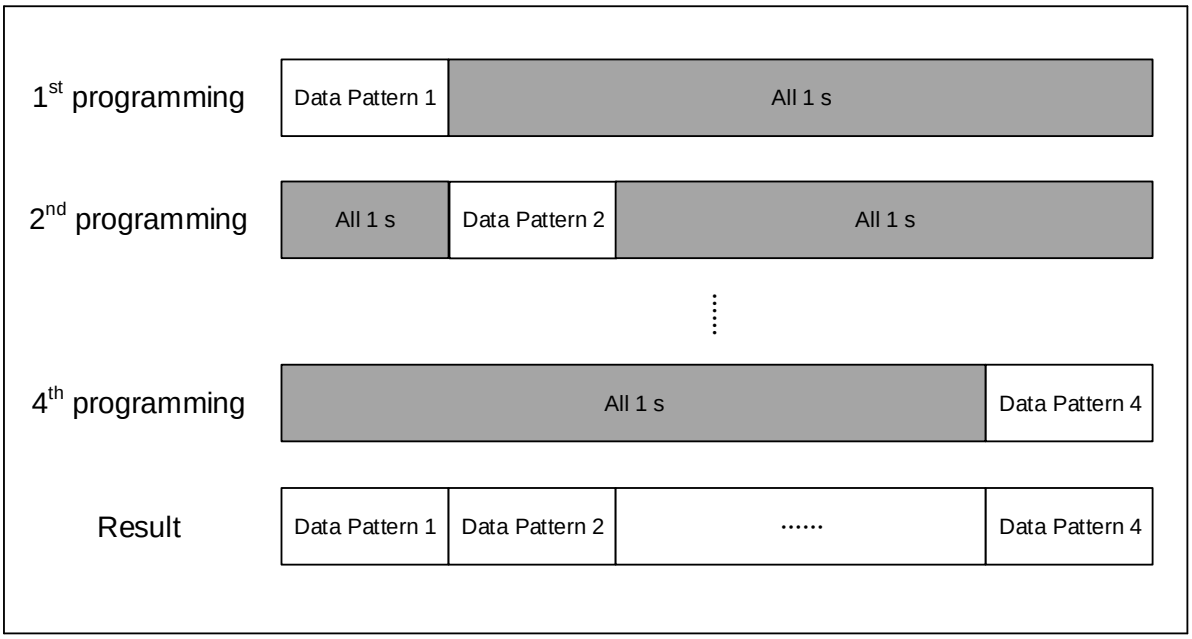
Within a block, the pages must be programmed consecutively from the LSB (least significant bit) page of the block to MSB (most significant bit) page of the block. Random page address programming is prohibited.



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8.16 Several programming cycles on the same page (Partial Page Program)

Each segment can be programmed individually as follows:



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9. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to VSS	VIN/OUT	-0.6 to VCC+0.4	V
	VCC(3.3V)	-0.6 to + 4.0	
	VCC(1.8V)	-0.6 to + 2.5	
Temperature Under Bias	TBIAS	-50 to +125	°C
Storage Temperature	TSTG	-65 to +150	°C

Notes:

1. Minimum DC voltage is -0.6V on input/output pins.
2. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

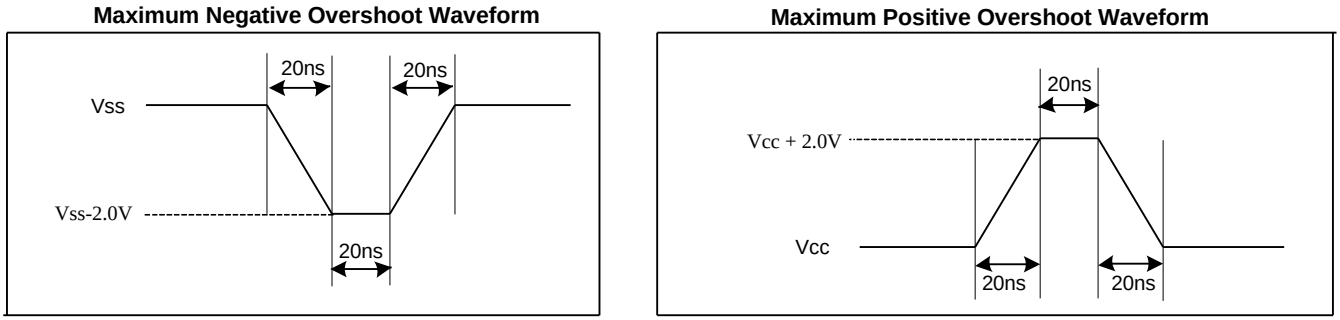


Figure 9-1. Input Test Waveform and Measurement Level

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10. VALID BLOCKS

	Capacity	Min	Max	Unit
Valid Block Number	4Gb	4016	4096	Blocks
	8Gb	8032	8192	Blocks
	16Gb	16064	16384	Blocks

Notes:

1. The 1st block is guaranteed to be a valid block with ECC at the time of shipment.
2. Invalid blocks are one that contains one or more bad bits. The device may contain invalid blocks upon shipment.

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11. DC CHARACTERISTICS

(T= -40℃~105℃, VCC=1.7~2.0V/2.7~3.6V)

Parameter		Symbol	Test Conditions	1.7v ~ 1.95v/2.7v ~ 3.6v			Unit
				Min	Typ.	Max	
Power on current per LUN		I_{CC0}				50	mA
Operating Current per LUN	Page Read with Serial Access	I_{CC1}	tRC=Min, CE#=V_{IL}, I_{OUT}=0mA	-	15	30	mA
	Program	I_{CC2}	-	-	15	30	
	Erase	I_{CC3}	-	-	15	30	
Standby Current (CMOS) per LUN for 85°		I_{SB}	CE#=VCC-0.2, WP#=0V/VCC	-	10	50	μA
Standby Current (CMOS) per LUN for 105°		I_{SB}	CE#=VCC-0.2, WP#=0V/VCC	-	10	100	
Input Leakage Current		I_{LI}	V_{IN}=0 to VCC(max)	-	-	±10	
Output Leakage Current		I_{LO}	V_{OUT}=0 to VCC(max)	-	-	±10	
Input High Voltage		V_{IH}	-	0.8xVCC	-	VCC+0.3	V
Input Low Voltage		V_{IL}	-	-0.3	-	0.2xVCC	
Output High Voltage Level		V_{OH}	I_{OH}=-400μA	VCC-0.3	-	-	
Output Low Voltage Level		V_{OL}	I_{OL}=2.1mA	-	-	0.4	
Output Low Current(R/B#)		$I_{OL(R/B\#)}$	V_{OL}=0.4V	3/8	4/10	-	mA

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12. AC CHARACTERISTICS

12.1 Test Condition

(Ta=-40 to 105°C VCC=1.7V~1.95V /2.7V~3.6V)

Parameter	GD9Fx4GF3A/GD9Fx8GE3A/GD9FxAGD3A
Input Pulse Levels	0V to VCC
Input Rise and Fall Times	5ns
Input and Output Timing Levels	VCC/2
Output Load	1 TTL GATE and CL=30pF for 1.8v and CL=50pF for 3.3v

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12.2 Capacitance (TA=25°C, F=1.0MHz)

Parameter for 4Gb	Symbol	Test condition	Min	Max	Unit
Input/Output Capacitance	CI/O	V_{IL}=0V	-	6	pF
Input Capacitance	CIN	V_{IN}=0V	-	8	pF

Notes:

1. Capacitance is periodically sampled and not 100% tested.
2. Capacitance (CI/O and CIN) for 8Gb is 16pF and Capacitance (CI/O and CIN) for 16Gb is 32pF

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12.3 AC Timing Characteristics

Parameter	Symbol	3.3V		1.8V		
		Min	Max	Min	Max	
CE# setup time	tCS	15	-	20	-	ns
CE# hold time	tCH	5	-	5	-	ns
CLE setup time	tCLS	12	-	12	-	ns
CLE Hold time	tCLH	5	-	5	-	ns
ALE setup time	tALS	10	-	10	-	ns
ALE hold time	tALH	5	-	5	-	ns
Data setup time	tDS	7	-	10	-	ns
Data hold time	tDH	5	-	5	-	ns
Write cycle time	tWC	20	-	25	-	ns
WE# pulse width	tWP	10	-	12	-	ns
WE# high hold time	tWH	7	-	10	-	ns
Address to data loading time	tADL	100	-	100	-	ns
WE# high to busy	tWB	-	100	-	100	ns
Ready to RE# low	tRR	20	-	20	-	ns
CLE to RE# delay	tCLR	10	-	10	-	ns
ALE to RE# delay	tAR	10	-	10	-	ns
Read cycle time	tRC	20	-	25	-	ns
RE# pulse width	tRP	10	-	12	-	ns
RE# high hold time	tREH	7	-	10	-	ns
RE# access time	tREA	-	18	-	22	ns
CE# access time	tCEA	-	23	-	25	ns
RE# high to output high Z	tRHZ	-	100	-	100	ns
CE# high to output high Z	tCHZ	-	50	-	50	ns
CE# high to output hold	tCOH	15	-	15	-	ns
RE# high to output hold	tRHOH	15	-	15	-	ns
RE# low to output hold	tRLOH	3	-	3	-	ns
Output Hi-Z to RE# Low	tIR	0	-	0	-	ns
RE# high to WE# low	tRHW	100	-	100	-	ns
WE# high to RE# low	tWHR	80	-	80	-	ns
Write protect time	tWW	100	-	100	-	ns
Feature access time	tFEAT		1		1	us

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12.4 Performance Characteristics

Parameter		Symbol	Min	Typ.	Max	Unit
Data transfer from cell to register		tR			25	us
Program Time		tPROG	-	300	600	μs
Read Cache busy time		tCBSYR		5	tR	μs
Cache Program short busy time		tCBSYW		5	tPROG	μs
Dummy busy time		tDBSY		0.5	1	us
Number of Partial Program Cycles in the Same Page		NOP	-	-	4	cycles
Block Erase Time		tBERS	-	3	10	ms
Device resetting time	Read	tRST			10	us
	Program				20	us
	Erase				500	us

Note:

1.Typical value is measured at VCC=3.3V, TA=25℃(3.3V Device) or VCC=1.8 V, TA=25℃(1.8V Device).

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13. PACKAGE INFORMATION

13.1 TSOPI-48

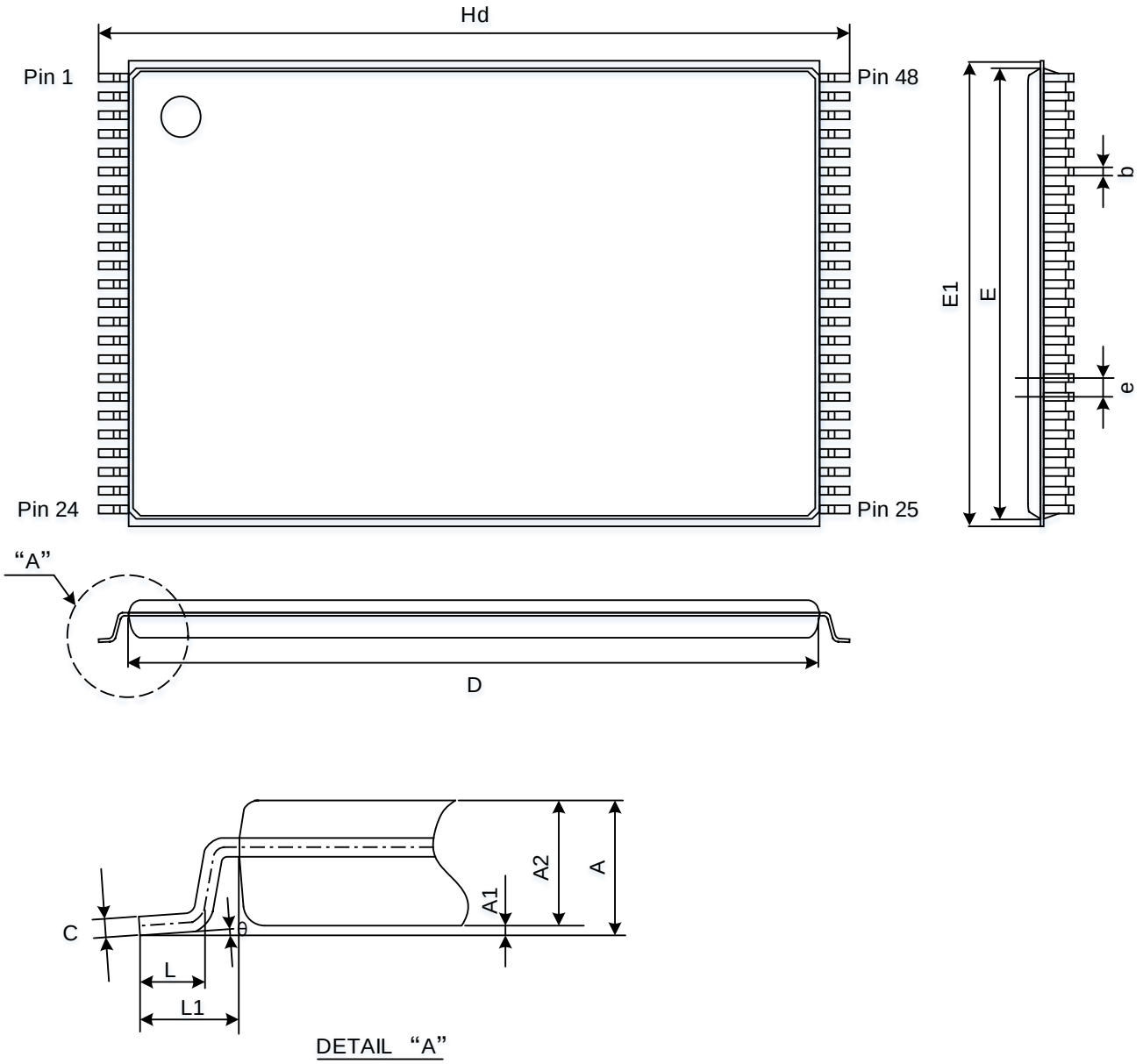


Figure 13-1: TSOPI-48 figures

Dimensions

Symbol / Unit		A	A1	A2	c	b	D	Hd	E	E1	e	L	L1	θ
mm	Min	-	0.05	0.90	0.09	0.14	18.30	19.80	11.90	-	0.50	0.425	0.60	0
	Nom	-	0.10	1.00	0.15	0.22	18.40	20.00	12.00	-		0.525	0.80	-
	Max	1.20	0.15	1.10	0.20	0.30	18.50	20.20	12.10	12.40		0.625	1.00	7

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Note：

1. Tolerance of the dimension should be ±0.1 unless otherwise specified.
2. Corner radius should be less than ±0.1R unless otherwise specified (excluding outer lead).
3. Tolerance of the angles should be ±0.5 degree unless otherwise specified.
4. The mold surface should have a finish 8±2S without luster.
   Trace of knockout pin and the ahaded portion of detail “A” should be polish surface.
5. Discrepancies between upper and lower molding cavity should be less than 0.05 of the package.
6. Mold flush should be less than 0.2mm.

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13.2 FBGA-63

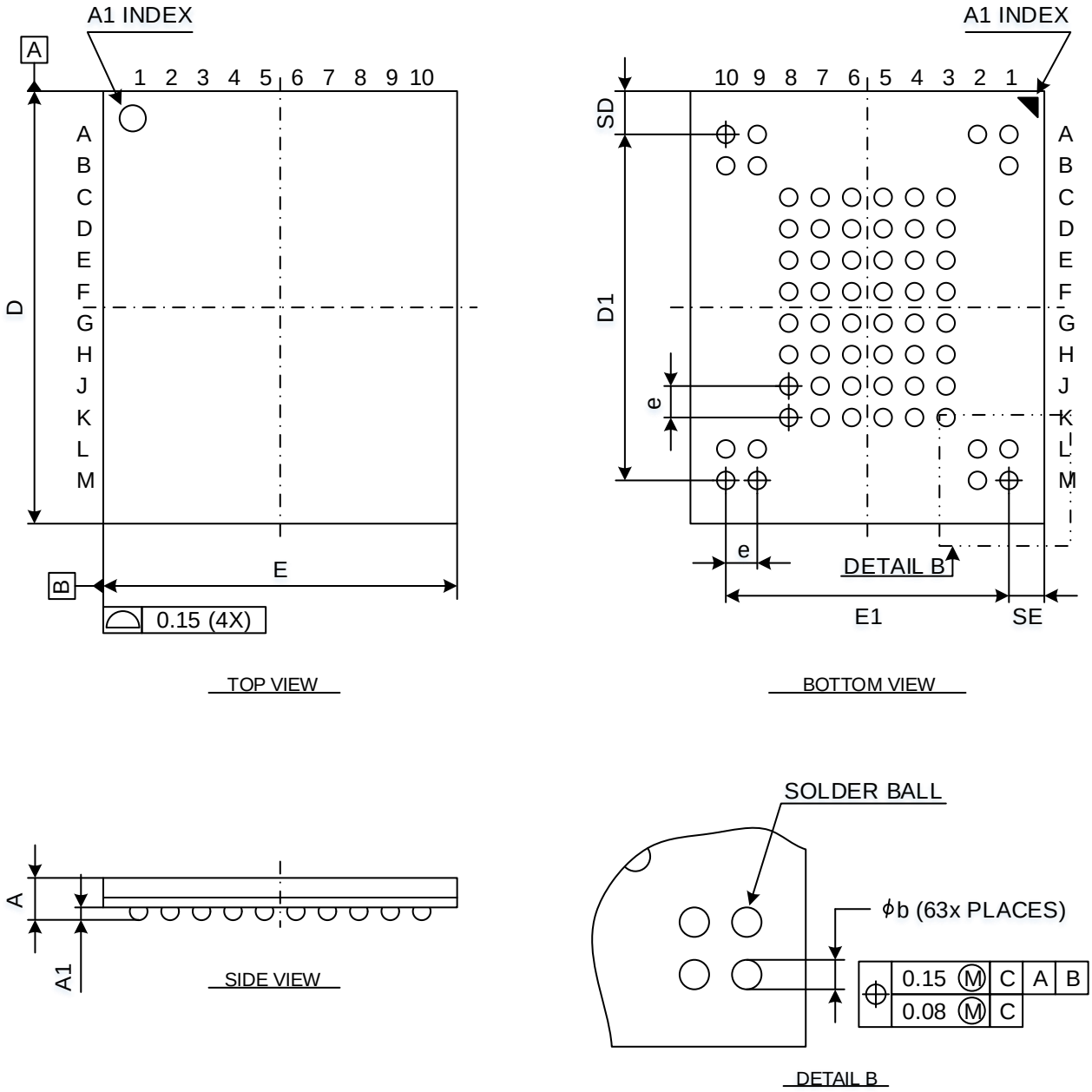


Figure 13-2: FBGA-63 figures

Dimensions

Symbol / Unit		A	A1	b	E	E1	D	D1	e	SD	SE
mm	Min	-	0.25	0.40	8.90	7.20 BSC	10.90	8.80 BSC	0.80 BSC	1.10 TYP	0.90 TYP
	Nom	-	0.30	0.45	9.00		11.00				
	Max	1.00	0.35	0.50	9.10		11.10				

Note：

1. Controlling dimension: millimeter.
2. The diameter of pre-reflow solder ball is ø0.42mm (0.40mm SMO).

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14. Part Numbering Information

GD	9F	U	4G	8	F	2	A	M	G	I
1	2	3	4	5	6	7	8	9	10	11

1. GD

2. Memory Type

9F: Parallel NAND

3. Power Supply

	VCCQ	VCC
U	2.7v ~ 3.6v	2.7v ~ 3.6v
S	1.7v ~ 1.95v	1.7v ~ 1.95v

4. Density:

1G: 1Gb
2G: 2Gb
4G: 4Gb
8G: 8Gb
AG: 16Gb

5. Organization

8: x8
6: x16

6. NAND Type:

F: SLC, 1Die, 1CE#, 1R/B#
E: SLC, 2Die, 1CE#, 1R/B#
D: SLC, 4Die, 1CE#, 1R/B#

7. Function Mode:

2: Spare size is 128bytes;
3: Spare size is 64bytes

8. Process Generation:

A: A GEN
B: B GEN

9. Package

M: TSOPI-48
L: FBGA-63
W: Wafer

10. Package Material & Packing

G: Lead & Halogen Free
W: Wafer

11. Temperature Grade

I: Industrial (-40C ~ 85C)
F: Industrial+ (-40C ~ 85C)
J: Industrial (-40C ~ 105C)

Note: (1) Industrial+: F grade has implemented additional test flows to ensure higher product quality than I grade.

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15. Revision History

Version No.	History Description	Page	Date
1.0	Initial Release		2020-01-20
1.1	Update the AC timing tADL from 300ns to 100ns	73	2020-06-30
1.2	Modify Figure 8-14 D-Out to D-IN Remove Interleaved Die Operation Description from DS.	31 59	2020-09-04

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