GD5F2GQ5xExxG

DATASHEET

2G-bit 2K+128BPageSize with E Version

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Email:sales@manduic.com
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1 FEATURE

◆ 2Gb SLC NAND Flash

◆2048-Byte+128-Byte Physical Page Size(1)
- Internal ECC Off (ECC_EN=0):
  2048-Byte+128-Byte Full Access
- Internal ECC On (ECC_EN=1, default):
  Program: 2048-Byte+64-Byte
  Read: 2048-Byte+128-Byte

◆ Standard, Dual, Quad SPI,DTR
- Standard SPI: SCLK, CS#, SI, SO, WP#, HOLD#
- Dual SPI: SCLK, CS#, SIO0, SIO1, WP#, HOLD#
- Quad SPI: SCLK, CS#, SIO0, SIO1, SIO2, SIO3
- DTR(Double Transfer Rate) Read : SCLK, CS#, SIO0, SIO1, SIO2, SIO3, DQS

◆ High Speed Clock Frequency
- 3.3V: 104MHz for fast read with 30pF load
- 1.8V: 80MHz for fast read with 30pF load
- 3.3V: Quad I/O Data transfer up to 416Mbits/s
- 1.8V: Quad I/O Data transfer up to 320Mbits/s

◆ Software/Hardware Write Protection
- Write protect all/portion of memory via software
- Register protection with WP# Pin

◆ Single Power Supply Voltage
- Full voltage range for 1.8V: 1.7V ~ 2.0V
- Full voltage range for 3.3V: 2.7V ~ 3.6V

◆ Advanced security Features
- 8K-Byte OTP Region

◆ Program/Erase/Read Speed
- Page Program time: 300us typical
- Block Erase time: 3ms typical
- Page read time: 60us maximum

◆ Low Power Consumption
- 30mA maximum active current
- 50uA maximum standby current

◆ Enhanced access performance
- 2Kbyte cache for fast random read
- Cache read and cache program

◆ Advanced Feature for NAND
- Factory good block0

◆ Reliability- Factory good block0
- P/E cycles with ECC: 100K
- Data retention: 10 Years

◆ Internal ECC
- 4bits /528Byte

Note (1): 2048Byte+128Byte Page Size can accommodate more advanced ECC algorithm by user's choice, even though the internal 4-bit ECC algorithm only requires 64-Byte spare area.

(2): Internal 4-bit ECC is set to on (ECC_EN=1) as shipment default, it can be disabled by setting ECC_EN=0.
- When Internal ECC is enabled, user can only program the first 64-Byte portion of the entire 128-Byte spare area, and the rest 64-Byte spare area cannot be programed. User can still read the entire 128-Byte spare area.
- When Internal ECC is disabled, user can read and program the entire 128-Byte spare area.

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2 GENERAL DESCRIPTION

SPI (Serial Peripheral Interface) NAND Flash provides an ultra-cost effective while high density non-volatile memory storage solution for embedded systems, based on an industry-standard NAND Flash memory core. It is an attractive alternative to SPI-NOR and standard parallel NAND Flash, with advanced features.

- Total pin count is 8, including VCC and GND
- Density 2Gb
- Superior write performance and cost per bit over SPI-NOR
- Significant low cost than parallel NAND

This low-pin-count NAND Flash memory follows the industry-standard serial peripheral interface, and always remains the same pin out from one density to another. The command sets resemble common SPI-NOR command sets, modified to handle NAND specific functions and added new features. GigaDevice SPI NAND is an easy-to-integrate NAND Flash memory, with specified designed features to ease host management:

- **User-selectable internal ECC**. ECC parity is generated internally during a page program operation. When a page is read to the cache register, the ECC parity is detected and corrects the errors when necessary. The device outputs corrected data and returns an ECC error status.
- **Internal data move or copy back with internal ECC**. The device can be easily refreshed and manage garbage collection task, without need of shift in and out of data. This command string can only be used on blocks with the same parity attribute.
- **Power on Read with internal ECC**. The device will automatically read first page of fist block to cache after power on, then host can directly read data from cache for easy boot. Also the data is promised correct by internal ECC when ECC enabled.

It is programmed and read in page-based operations, and erased in block-based operations. Data is transferred to or from the NAND Flash memory array, page by page, to a data register and a cache register. The cache register is closest to I/O control circuits and acts as a data buffer for the I/O data; the data register is closest to the memory array and acts as a data buffer for the NAND Flash memory array operation. The cache register functions as the buffer memory to enable page and random data READ/WRITE and copy back operations. These devices also use a SPI status register that reports the status of device operation.

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2.1 Product List

Please contact GigaDevice regional sales for the latest product selection and available form factors

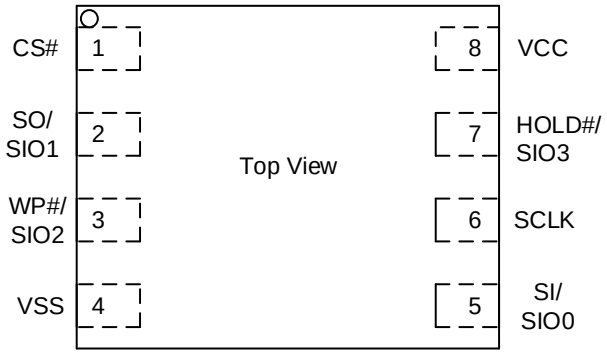
Product Number	Density	Voltage	Package Type	Temperature
GD5F2GQ5REYIG	2Gbit	1.7V to 2.0V	WSON8(8*6mm)	-40℃ to 85℃
GD5F2GQ5REBIG	2Gbit	1.7V to 2.0V	TFBGA24(5*5 Ball Array)	-40℃ to 85℃
GD5F2GQ5REZIG	2Gbit	1.7V to 2.0V	TFBGA24(4*6 Ball Array)	-40℃ to 85℃
GD5F2GQ5UEYIG	2Gbit	2.7V to 3.6V	WSON8(8*6mm)	-40℃ to 85℃
GD5F2GQ5UEBIG	2Gbit	2.7V to 3.6V	TFBGA24(5*5 Ball Array)	-40℃ to 85℃
GD5F2GQ5UEZIG	2Gbit	2.7V to 3.6V	TFBGA24(4*6 Ball Array)	-40℃ to 85℃
GD5F2GQ5REYFG*	2Gbit	1.7V to 2.0V	WSON8(8*6mm)	-40℃ to 85℃
GD5F2GQ5REBFG*	2Gbit	1.7V to 2.0V	TFBGA24(5*5 Ball Array)	-40℃ to 85℃
GD5F2GQ5REZFG*	2Gbit	1.7V to 2.0V	TFBGA24(4*6 Ball Array)	-40℃ to 85℃
GD5F2GQ5UEYFG*	2Gbit	2.7V to 3.6V	WSON8(8*6mm)	-40℃ to 85℃
GD5F2GQ5UEBFG*	2Gbit	2.7V to 3.6V	TFBGA24(5*5 Ball Array)	-40℃ to 85℃
GD5F2GQ5UEZFG*	2Gbit	2.7V to 3.6V	TFBGA24(4*6 Ball Array)	-40℃ to 85℃
GD5F2GQ5REYJG	2Gbit	1.7V to 2.0V	WSON8(8*6mm)	-40℃ to 105℃
GD5F2GQ5REBJG	2Gbit	1.7V to 2.0V	TFBGA24(5*5 Ball Array)	-40℃ to 105℃
GD5F2GQ5REZJG	2Gbit	1.7V to 2.0V	TFBGA24(4*6 Ball Array)	-40℃ to 105℃
GD5F2GQ5UEYJG	2Gbit	2.7V to 3.6V	WSON8(8*6mm)	-40℃ to 105℃
GD5F2GQ5UEBJG	2Gbit	2.7V to 3.6V	TFBGA24(5*5 Ball Array)	-40℃ to 105℃
GD5F2GQ5UEZJG	2Gbit	2.7V to 3.6V	TFBGA24(4*6 Ball Array)	-40℃ to 105℃

Note: (1) Industrial+: F grade has implemented additional test flows to ensure higher product quality than I grade.

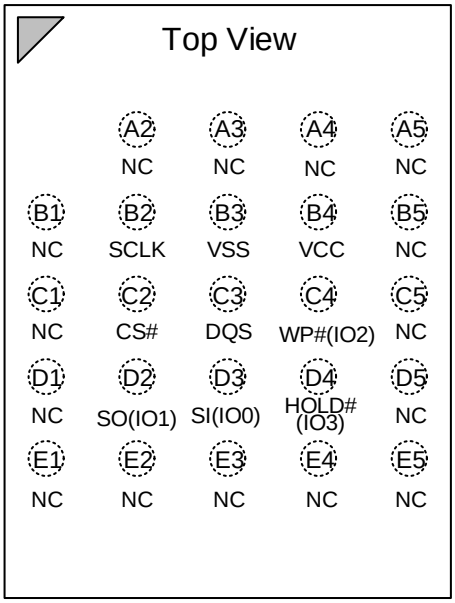
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2.2 CONNECTION DIAGRAM

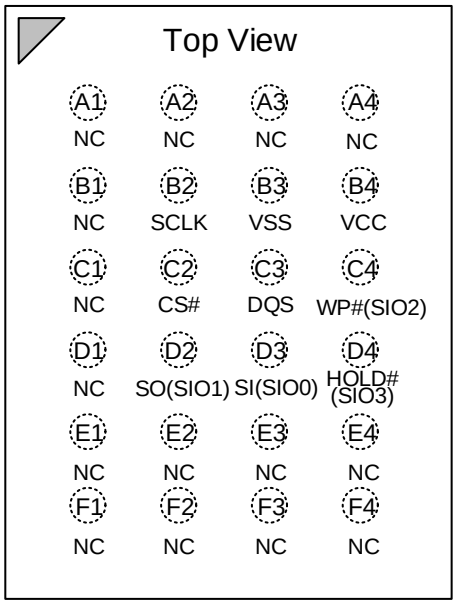
Figure 2-1.Connect Diagram



8‐LEAD WSON



24-BALL TFBGA (5x5 ball array)



24-BALL TFBGA (4x6 ball array)

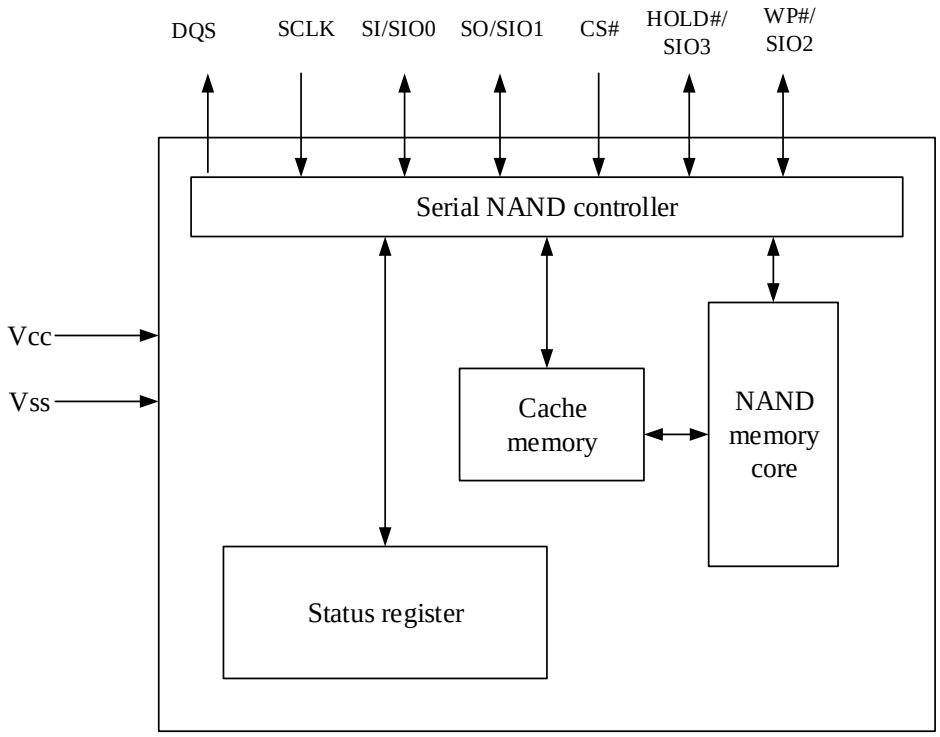
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2.3 PIN DESCRIPTION

Pin Name	I/O	Description
CS#	**I**	Chip Select input, active low
SO/SIO1	**I/O**	Serial Data Output / Serial Data Input Output 1
WP#/SIO2	**I/O**	Write Protect, active low / Serial Data Input Output 2
VSS	**Ground**	Ground
SI/SIO0	**I/O**	Serial Data Input / Serial Data Input Output 0
SCLK	**I**	Serial Clock input
HOLD# /SIO3	**I/O**	Hold Input/Serial Data Input Output 3
DQS (only for BGA24)	**O**	Data Strobe Signal Output
VCC	**Supply**	Power Supply
NC		Not Connect, Not internal connection; can be driven or floated.

2.4 BLOCK DIAGRAM

Figure 2-2.Block Diagram



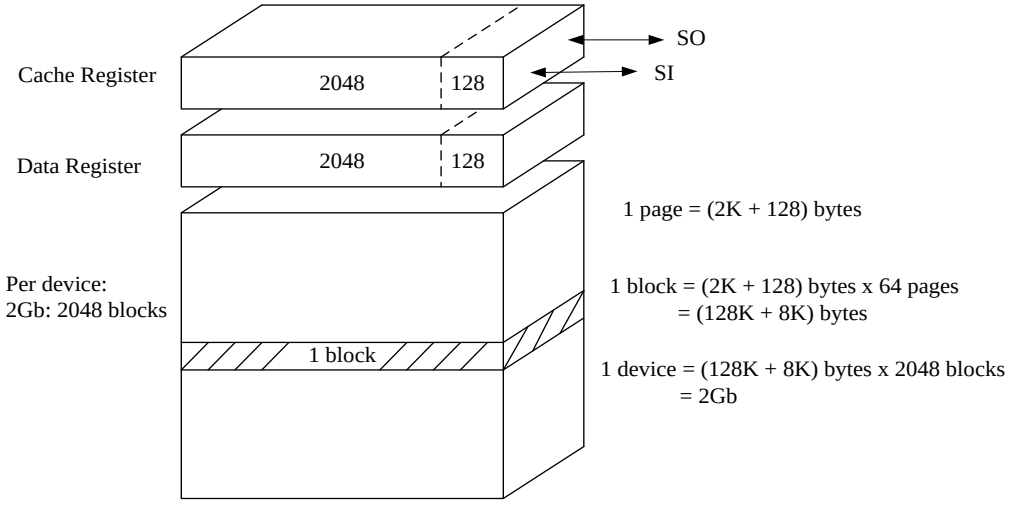
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3 ARRAY ORGANIZATION

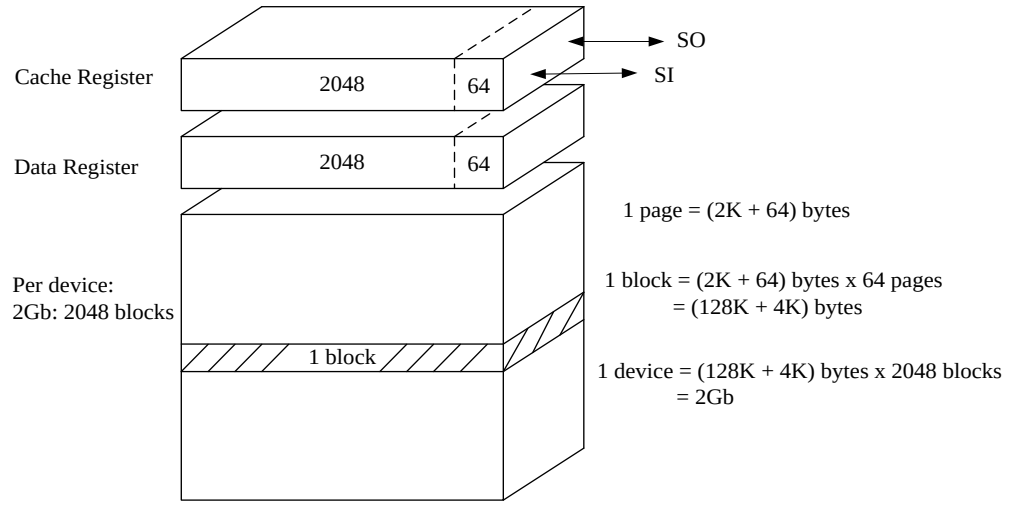
Table 3-1.Array Organization

Each device has	Each block has	Each page has	
2Gb			
256M+16M	128K+8K	2K+128	bytes
2048 x 64	64	-	pages
2048	-	-	blocks

Figure 3-1. Array Organization



Internal ECC = OFF



Internal ECC = ON

Note:

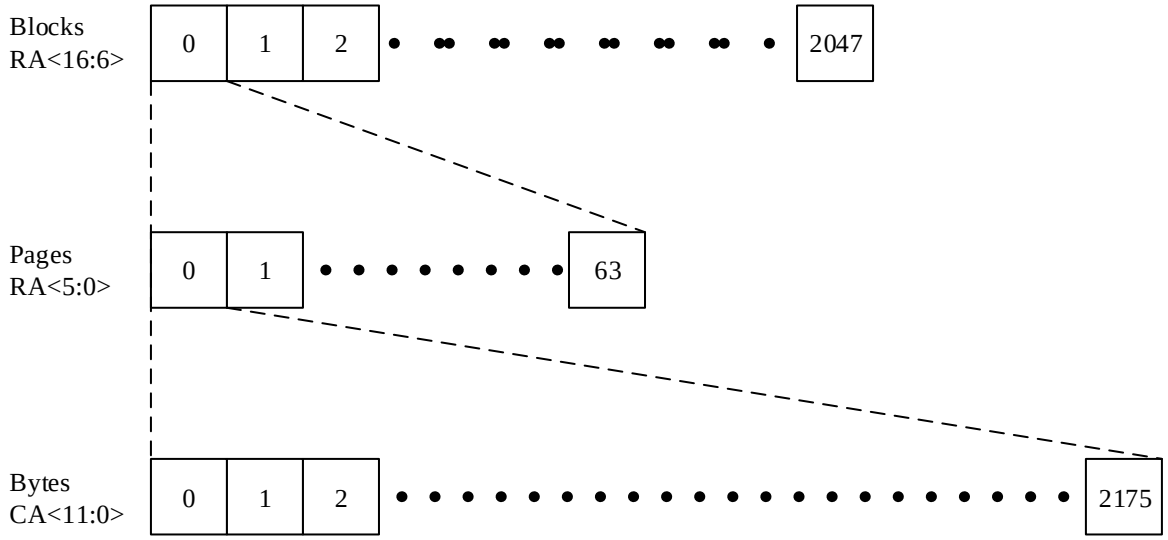
1.When Internal ECC is enabled，user can program the first 64 bytes of the entire 128 bytes spare area and the last 64 bytes of the whole spare area cannot be programed，user can read the entire 128 Byte spare area.

2.When Internal ECC is disabled，user can read and program the entire 128 bytes spare area.

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4 MEMORY MAPPING

For 2G



Note:

1. CA: Column Address. The 12-bit address is capable of addressing from 0 to 4095 bytes; however, only bytes 0 through 2175 are valid. Bytes 2176 through 4095 of each page are “out of bounds,” do not exist in the device, and cannot be addressed.
2. RA: Row Address. RA<5:0>selects a page inside a block, and RA<16:6>selects a block.

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5 DEVICE OPERATION

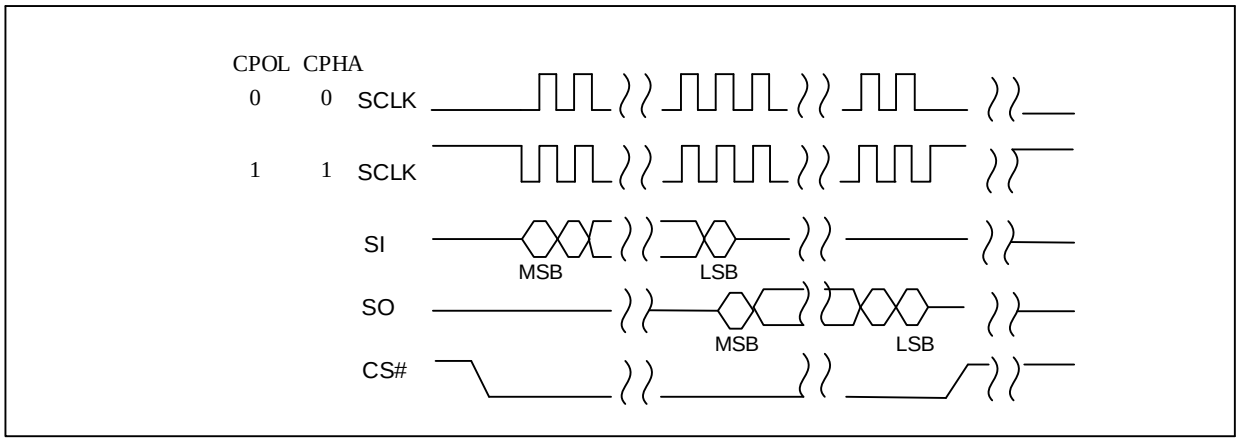
5.1 SPI Modes

SPI NAND supports two SPI modes:

- CPOL = 0, CPHA = 0 (Mode 0)
- CPOL = 1, CPHA = 1 (Mode 3)

Input data is latched on the rising edge of SCLK and data shifts out on the falling edge of SCLK for both modes. All timing diagrams shown in this data sheet are mode 0. See Figure5-1 for more details.

Figure 5-1. SPI Modes Timing Diagram



Note: While CS# is HIGH, keep SCLK at VCC or GND (determined by mode 0 or mode 3). Do not toggle SCLK until CS# is driven LOW.

We recommend that the user pull CS# to high when user don't use SPI flash, otherwise the flash is always in the read state, which is not good for flash.

When CS# is high and SCLK at VCC or GND state, the device is in idle state.

Standard SPI

SPI NAND Flash features a standard serial peripheral interface on 4 signals bus: Serial Clock (SCLK), Chip Select (CS#), Serial Data Input (SI) and Serial Data Output (SO).

Dual SPI

SPI NAND Flash supports Dual SPI operation when using the x2 and dual IO commands. These commands allow data to be transferred to or from the device at two times the rate of the standard SPI. When using the Dual SPI command the SI and SO pins become bidirectional I/O pins: SIO0 and SIO1.

Quad SPI

SPI NAND Flash supports Quad SPI operation when using the x4 and Quad IO commands. These commands allow data to be transferred to or from the device at four times the rate of the standard SPI. When using the Quad SPI command the SI and SO pins become bidirectional I/O pins: SIO0 and SIO1, and WP# and HOLD# pins become SIO2 and SIO3.

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DTR Quad SPI

The device supports DTR Quad SPI operation when using the “DTR Quad I/O Fast Read” command.

These command allow data to be transferred to or from the device at eight times the rate of the standard SPI, and data output will be latched on both rising and falling edges of the serial clock. When using the DTR Quad SPI command the SI and SO pins become bidirectional I/O pins: IO0 and IO1, and WP# and HOLD# pins become IO2 and IO3. DTR Quad SPI commands require the Quad Enable bit (QE) in Status Register to be enable. The device has the DQS pin (Only for BGA24 Package). A data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver

5.2 HOLD Mode

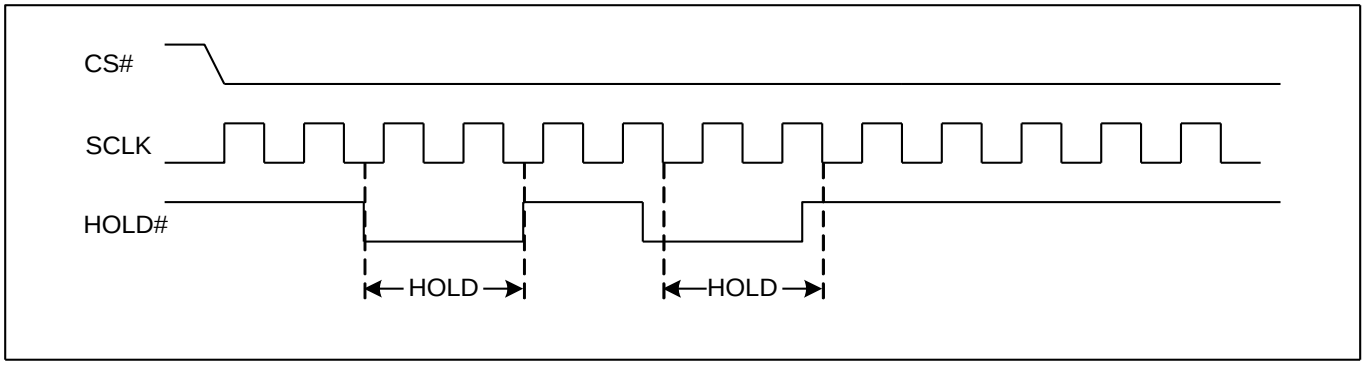
The HOLD# function is only available when QE=0. If QE=1, the HOLD# functions is disabled, the pin acts as dedicated data I/O pin.

The HOLD# signal goes low to stop any serial communications with the device, but doesn’t stop the operation of write status register, programming, or erasing in progress.

The operation of HOLD, need CS# keep low, and starts on falling edge of the HOLD# signal, with SCLK signal being low (if SCLK is not being low, HOLD operation will not start until SCLK being low). The HOLD condition ends on rising edge of HOLD# signal with SCLK being low (If SCLK is not being low, HOLD operation will not end until SCLK being low).

The SO is high impedance, both SI and SCLK don’t care during the HOLD operation, if CS# drives high during HOLD operation, it will reset the internal logic of the device. To re-start communication with chip, the HOLD# must be at high and then CS# must be at low.

Figure5-2. Hold Condition



5.3 Write Protection

SPI NAND provides Hardware Protection Mode besides the Software Mode. Write Protect (WP#) prevents the block lock bits (BP0, BP1, BP2 and INV, CMP) from being over written. If the BRWD bit is set to 1 and WP# is LOW, the block protect bits cannot be altered.

To enable the Write Protection, the Quad Enable bit (QE) of feature (B0[0]) must be set to 0.

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5.4 Power Off Timing

Please do not turn off the power before Write/Erase operation is complete. Avoid using the device when the battery is low. Power shortage and/or power failure before Write/Erase operation is complete will cause loss of data and/or damage to data.

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6 COMMANDS DESCRIPTION

Table 6-1. Commands Set

Command Name	Byte1	Byte2	Byte3	Byte4	Byte5	Byte6	Byte 7
Write Enable	06H						
Write Disable	04H						
Get Features	0FH	A7-A0	D7-D0	Wrap(8)			
Set Feature	1FH	A7-A0	D7-D0				
Page Read (to cache)	13H	A23-A16	A15-A8	A7-A0			
Next Page Read (to cache)	31H						
Next Page Cache Read Random	13H	A23-A16	A15-A8	A7-A0	31H		
Last Page Read (to cache)	3FH						
Read From Cache	03H/0BH	A15-A8	A7-A0(2)	Dummy(1)	D7-D0		
Read From Cache x 2	3BH	A15-A8	A7-A0(2)	Dummy(1)	D7-D0		
Read From Cache x 4	6BH	A15-A8	A7-A0(2)	Dummy(1)	D7-D0		
Read From Cache Dual IO	BBH	A15-A8	A7-A0(2)	Dummyx2(1)	D7-D0		
Read From Cache Quad IO	EBH	A15-A8	A7-A0(2)	Dummyx4(1)	D7-D0		
Read From Cache Quad I/O DTR	EEH	A31-A24	A23-A16	A15-A8	A7-A0(2)	Dummy x8(1)	D7-D0
Read ID(4)	9FH	Dummy	MID	DID			
Read parameter page	13H	00H	00H	04H			
Read UID	13H	00H	00H	06H			
Program Load	02H	A15-A8	A7-A0(3)	D7-D0	Next byte		
Program Load x4	32H	A15-A8	A7-A0(3)	D7-D0	Next byte		
Program Execute	10H	A23-A16	A15-A8	A7-A0			
Program Execute Background	10H	A23-A16	A15-A8	A7-A0	15H		
Program Load Random Data	84H(6)	A15-A8	A7-A0(3)	D7-D0	Next byte		
Program Load Random Data x4	C4H/34H(6)	A15-A8	A7-A0(3)	D7-D0	Next byte		
Block Erase(128K)	D8H	A23-A16	A15-A8	A7-A0			
Reset(5)	FFH						
Enable Power on Reset	66h						
Power on Reset(7)	99h						

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Note:

1. The dummy has 8 clock.
   03H/0BH/3BH/6BH has 1 byte dummy. BBH has 2 bytes dummy.
   EBH has 4 bytes dummy. EEH has 8 bytes dummy.
2. The A15-A0 (03H/0BH/3BH/6BH) has 16 clock, include 4 clock dummy.
   The A15-A0 (BBH) has 8 clock, include 2 clock dummy.
   The A15-A0 (EBH) has 4 clock, include 1 clock dummy.
   The A31-A0 (EEH) has 4 clock, include 2.5 clock dummy.
3. The A15-A0 has 16 clock, include 4 clock dummy.
4. MID is Manufacture ID (C8h for GigaDevice), DID is Device ID.
5. Reset command:

• Reset will reset PAGE READ/PROGRAM/ERASE operation.
• Reset will reset status register bits P_FAIL/E_FAIL/WEL/OIP/CBSY/ECCS/ECCSE.

6. Those commands are only available in Internal Data Move operation.
7. Power on reset:
   Retrieve status register and data in cache to power on status.
8. The output would be updated by real-time, until CS# is driven high.

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7 WRITE OPERATIONS

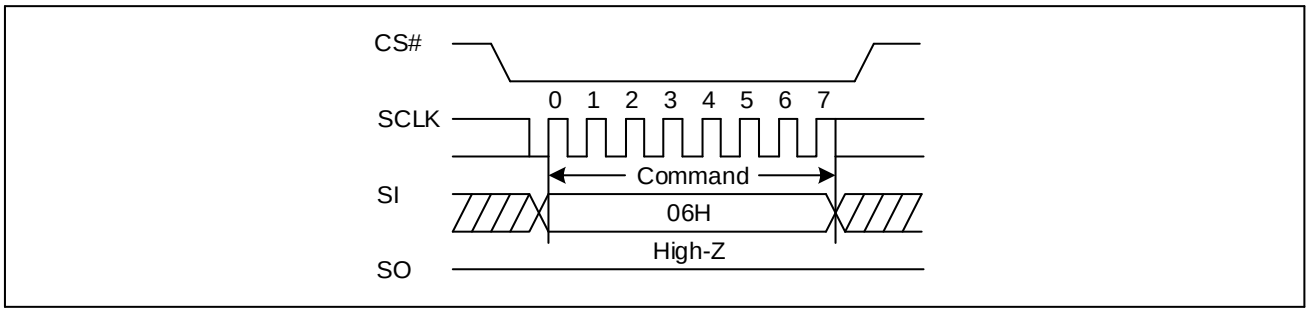
7.1 Write Enable (WREN) (06H)

The Write Enable (WREN) command is for setting the Write Enable Latch (WEL) bit. The Write Enable Latch (WEL) bit must be set prior to following operations that change the contents of the memory array:

- Page program
- OTP program/OTP protection
- Block erase

The WEL bit can be cleared after a reset command.

Figure 7-1.Write Enable Timing Diagram

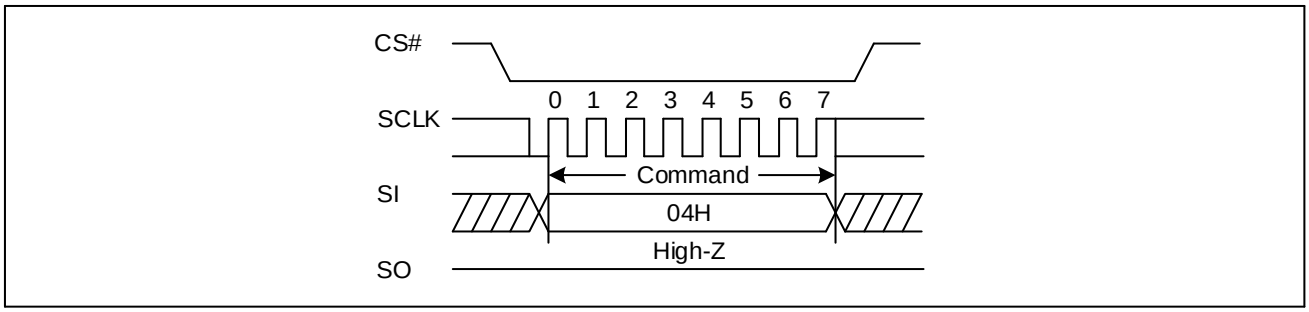


7.2 Write Disable (WRDI) (04H)

The Write Disable command is for resetting the Write Enable Latch (WEL) bit. The WEL bit is reset by following condition:

- Page program
- OTP program/OTP protection
- Block erase

Figure 7-2.Write Disable Timing Diagram



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8 READ OPERATIONS

8.1 Page Read

The PAGE READ (13H) command transfers the data from the NAND Flash array to the cache register. The command sequence is as follows:

- 13H (PAGE READ to cache)
- 0FH (GET FEATURES command to read the status)
- 03H or 0BH (Read from cache)/3BH (Read from cache x2)/6BH (Read from cache x4)/BBH/EBH/EEH (Read from cache DTR x4)

The PAGE READ command requires a 24-bit address. After the block/page addresses are registered, the device starts the transfer from the main array to the cache register, and is busy for tRD time. During this time, the GET FEATURE (0FH) command can be issued to monitor the status. Followed the page read operation, the RANDOM DATA READ (03H/0BH/3BH/6BH/EEH) command must be issued in order to read out the data from cache. The output data starts at the initial address specified in the command, once it reaches the ending boundary of whole page section, the output will wrap around from the beginning boundary until CS# is pulled high to terminate this operation. Refer waveforms to view the entire READ operation.

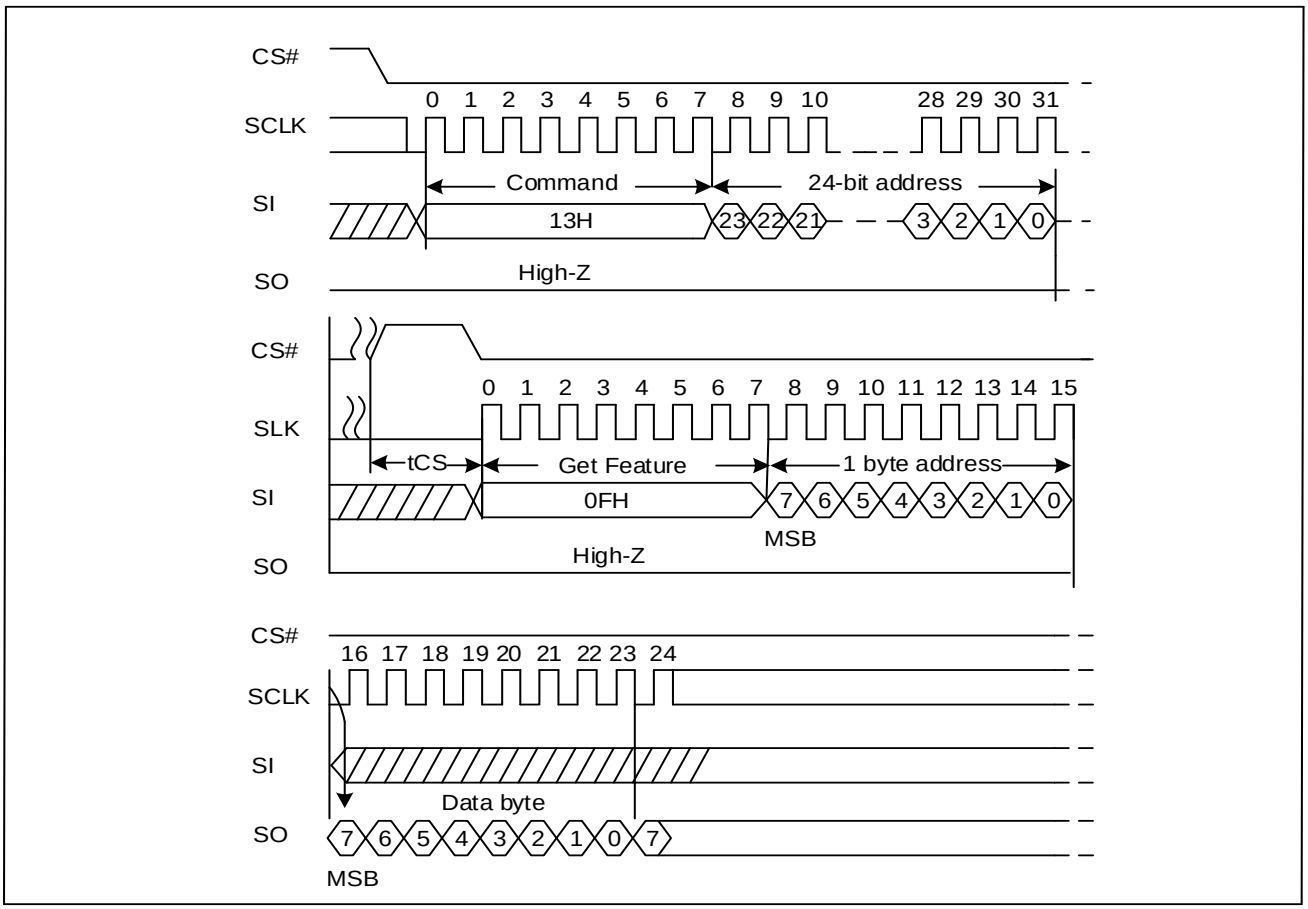
Note: The command 6BH (Read from cache x4)/EBH/EEH (Read from cache DTR x4) is only available with the QE enable.

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8.2 Page Read to Cache (13H)

The command page read to cache is read the data from flash array to cache register.

Figure 8-1.Page Read to cache Timing Diagram



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8.3 Cache Read Function (31H/3FH)

A “Cache Read” function has been implemented in SPI series to improve the overall read throughput. It is possible to transfer the data from array to the Data Register simultaneously while a Read Data command is being performed to read out data from the Cache Register.

When multiple pages of data is to be read out sequentially, the host should issue a “Page Read to Cache (13h)” command followed by a Page Address which specifies the starting page of the data(1). Once the command is accepted, the host should use “Get Feature (0Fh)” to check the OIP bit value to determine if the internal operation has completed or not.

Prior to issuing a Read Data command (i.e. 03h/0Bh/3Bh/6Bh/BBh/EBh) to read out the data in the Cache Register, the host can issue a “Next Page Cache Read (31h)” command to initiate the Cache Read operation. There is not necessary to provide any Page Address since the device will automatically increment the Page Address specified earlier by “Page Read to Cache (13h)” instruction. After the “Next Page Cache Read” (31h) command issued, the device starts to transfer data from data register to cache register for tCBSYR. After tCBSYR, CBSY bit (through GET FEATURE command to check this status bit) goes to 1 from 0.

While the device is transferring the next page array data to the Data Register, the host can now use Read From Cache command to shift out the current page data inside the Cache Register. Once CBSY bit becomes 0, the host can issue a Read Data command to shift out the Cache Register data, then issue “Next Page Cache Read (31h)” again to read the next page in the array.

If the current page address is the last page of a block or the last page of the data being read out, the host should issue “Last Page Cache Read (3Fh)” instead of “Next Page Cache Read (31h)”, and proceed with the last Read from cache command. If the data being read out is more than one block, another “Page Read to Cache (13h)” command is needed to specify the first page of the next block and initiate the “Cache Read” operation again in the next block.

Table 8-1.Cache Read instruction description

Instruction	Command Code	Description
Next Page Cache Read	31h	Issue prior to current page “Read From Cache” and read next page data into Data Register.
Next Page Cache Read Random	13h+addr+31h	Issue prior to current page “Read From Cache” and read special page data into Data Register.
Last Page Cache Read	3Fh	Issue prior to last page “Read From Cache” at the end of a block or the end of the data being read.

Notes:

1. Upon powered up, SPI NAND will automatically load Block-0/Page-0 data into the Cache Register. If this is the starting page of the data that is to be read out, it is not necessary to issue a “Page Read to Cache (13h)” command to initiate the “Cache Read” operation.
2. Before issuing 31h/3Fh, CBSY bit must be checked to make sure CBSY=0, device is not performing any internal operations.

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The command sequence is as follows:

• 13H (PAGE READ to cache)

• 0FH (GET FEATURES command to read the status until OIP status bit is changed from 1 to 0)

• 31H (NEXT PAGE CACHE READ command to transfer data from data register to cache register and kick off the next page transfer from array to data register)

• 0FH (GET FEATURES command to read the status until CBSY=0)

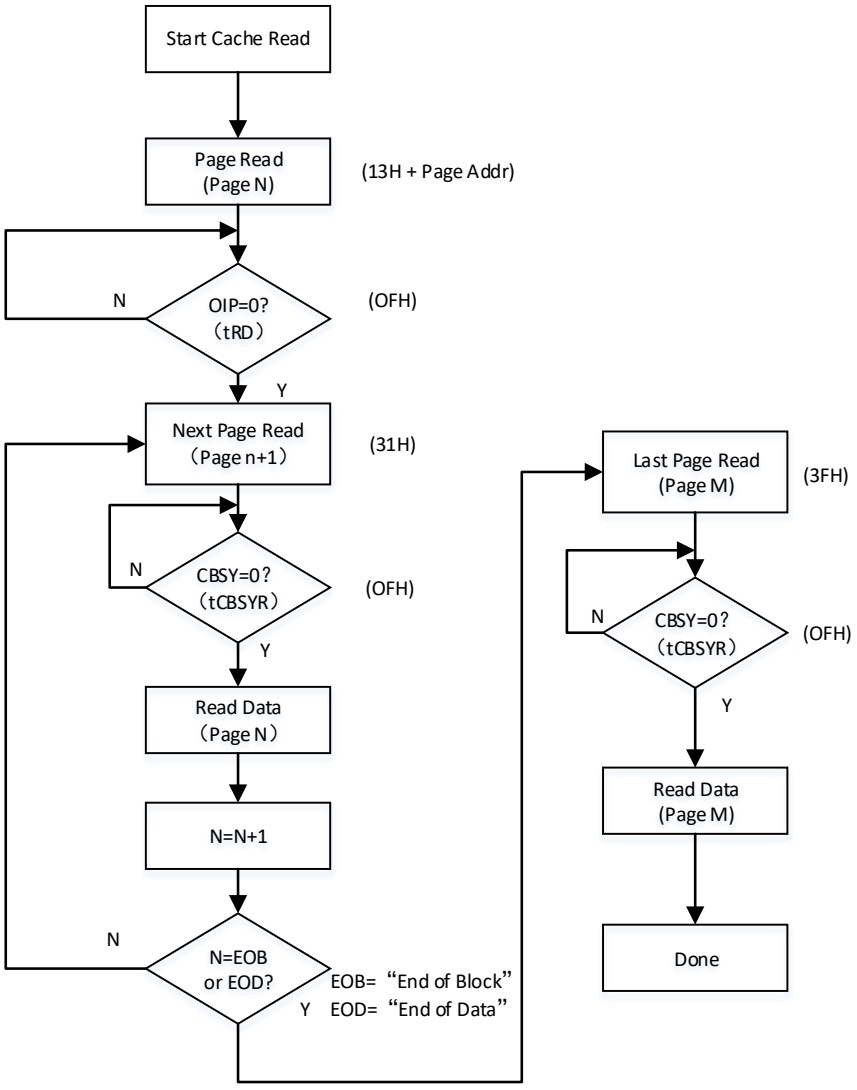
• 03H or 0BH (Read from cache)/3BH (Read from cache x2)/6BH (Read from cache x4)/BBH/EBH/EEH (Read from cache DTR x4)

• 3FH (LAST PAGE CACHE READ command to end the read page cache sequence and copy a last page from the data register to cache register)

• 0FH (GET FEATURES command to read the status until CBSY=0)

• 03H or 0BH (Read from cache)/3BH (Read from cache x2)/6BH (Read from cache x4)/BBH/EBH/EEH (Read from cache DTR x4)

Figure 8-2.Cache Read operation flow chart



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Figure 8-3.Page Read to Cache Timing Diagram

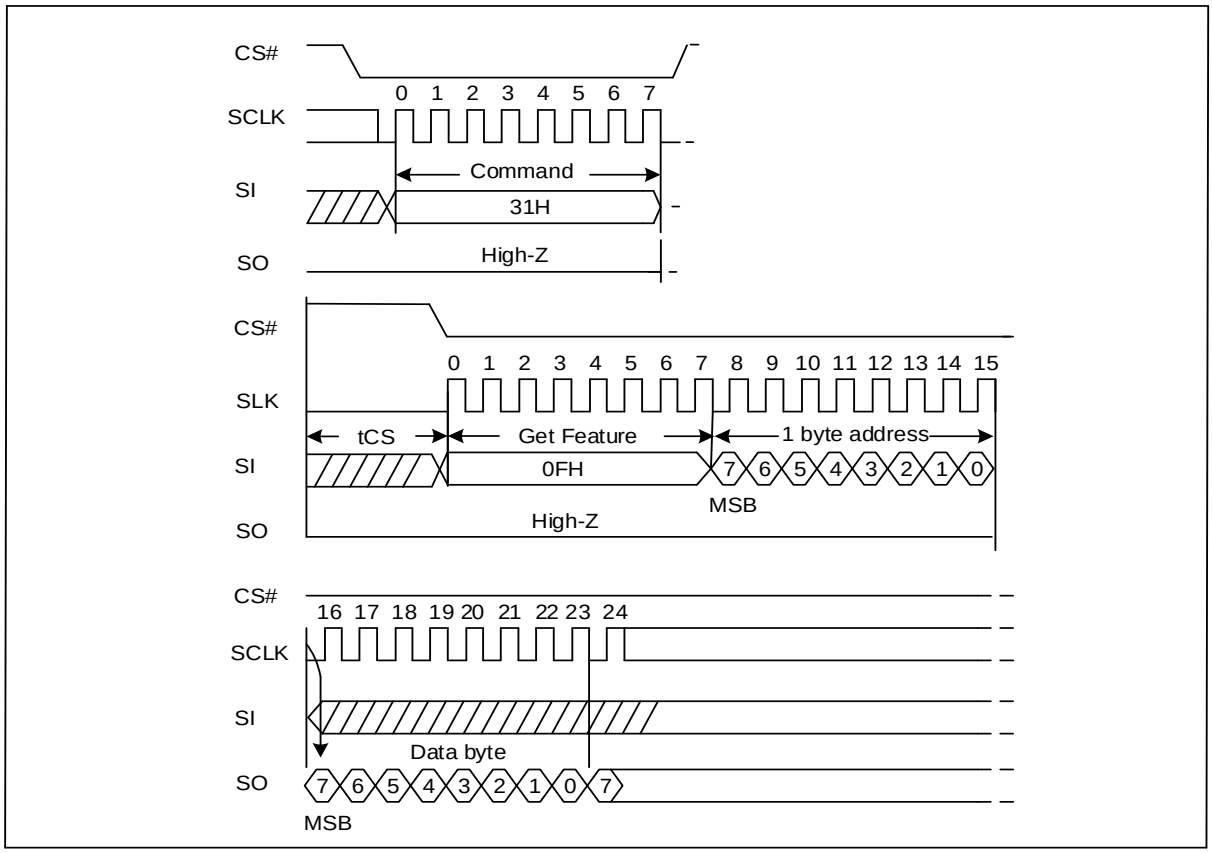


Figure 8-4.Page Read to Cache Timing Diagram

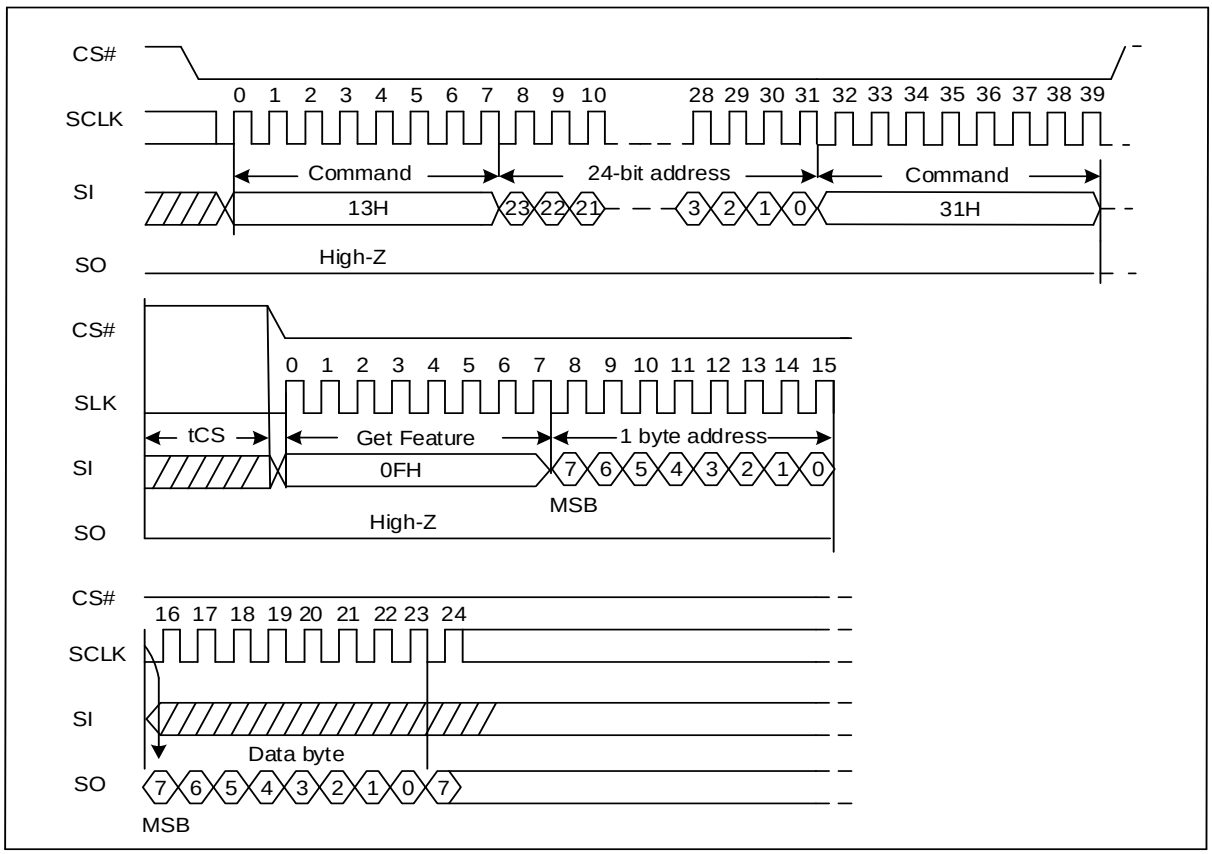
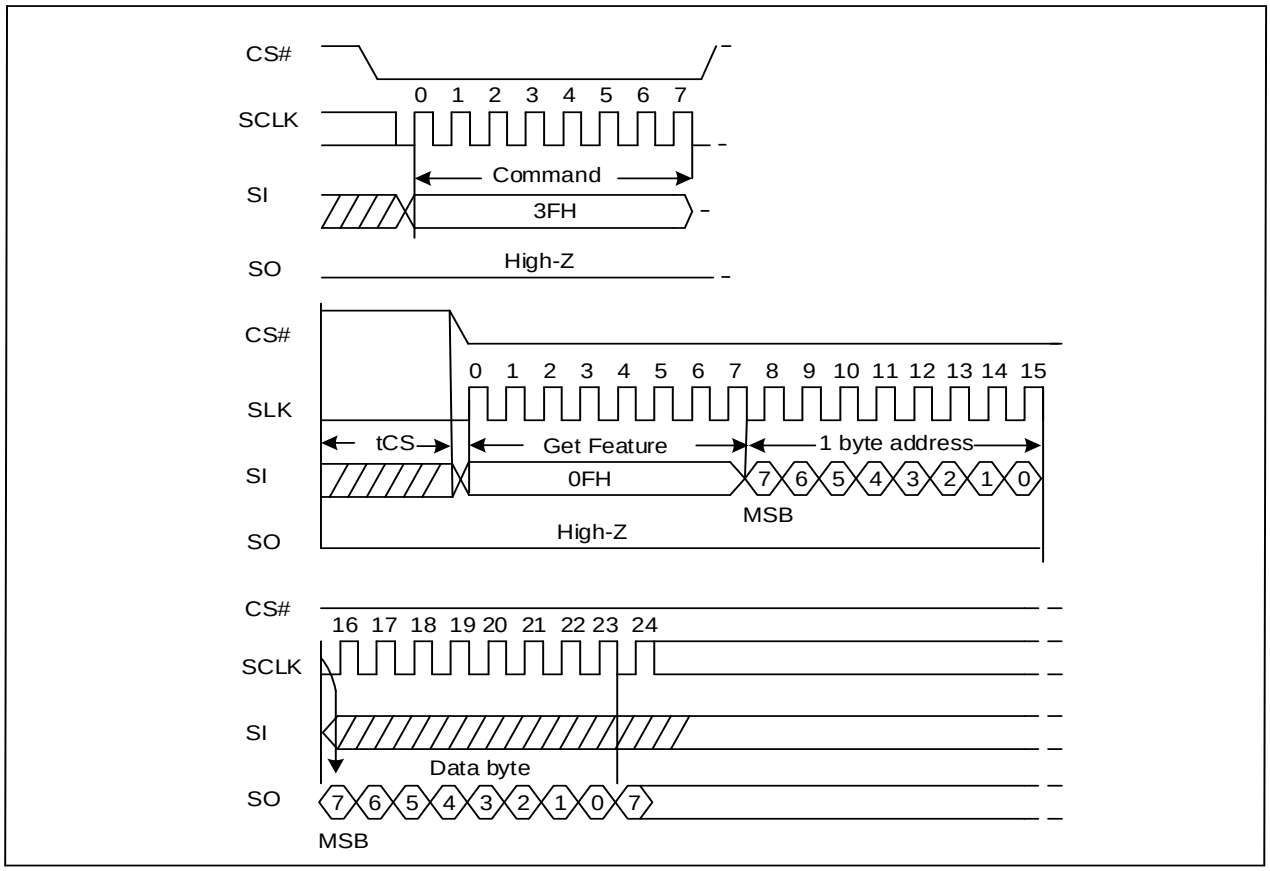
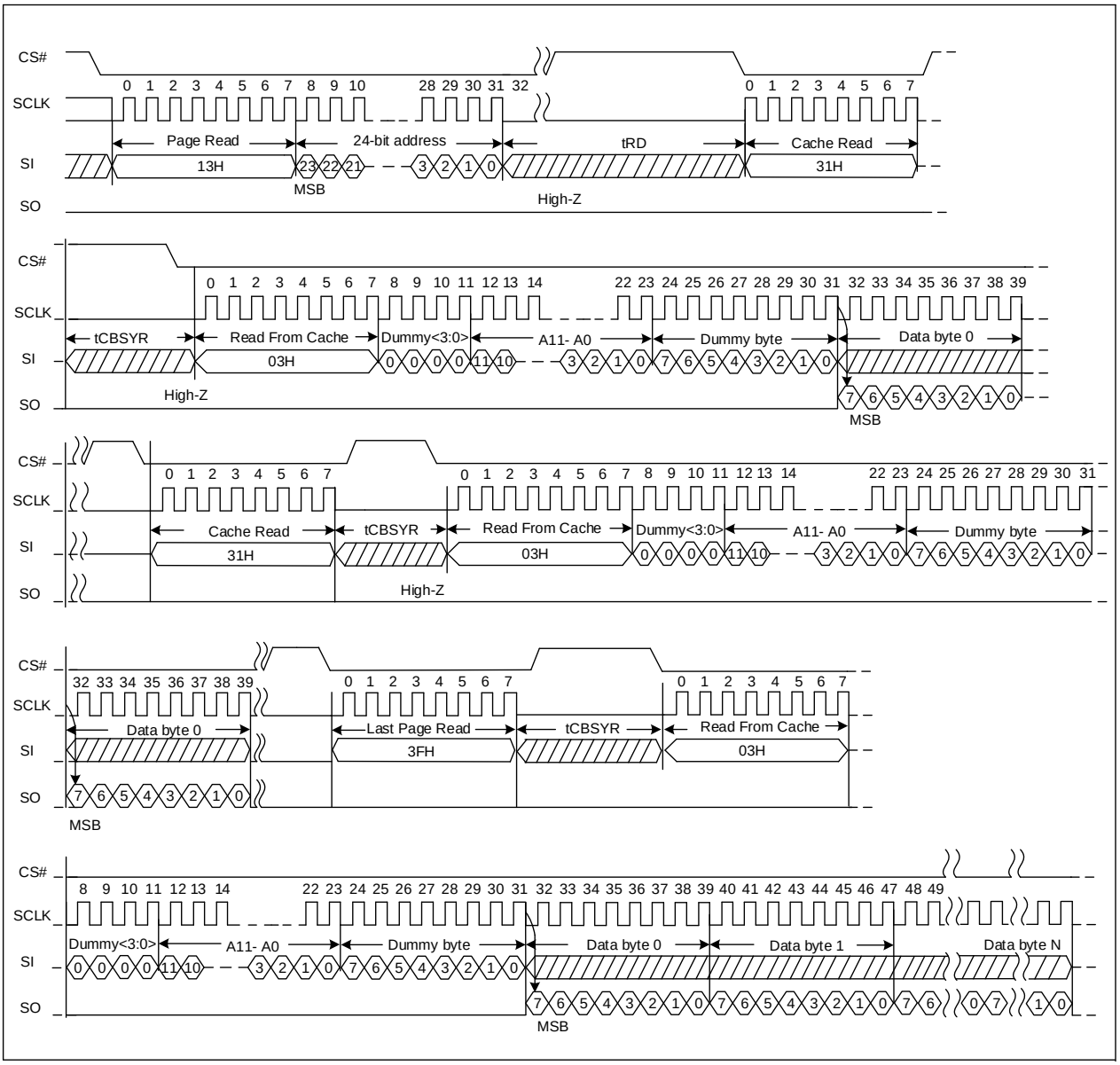


Figure 8-5.Page Read to Cache Timing Diagram



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Figure 8-6.Page Read to Cache Timing Diagram



Note：

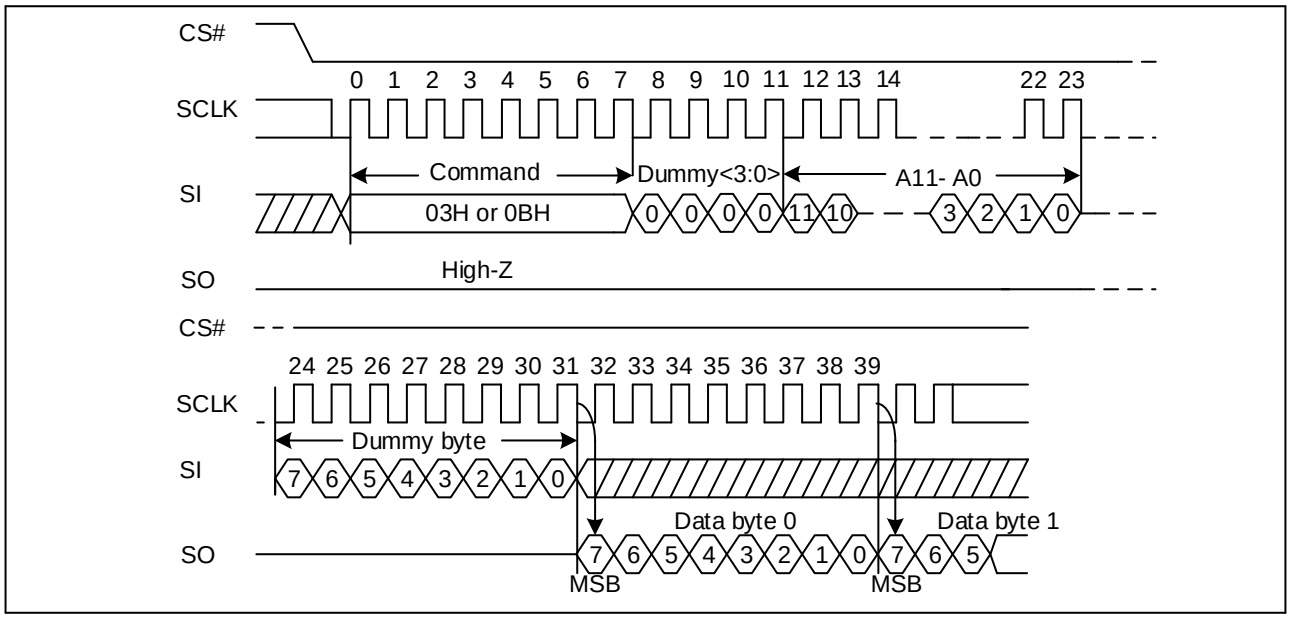
1. Command 03h/0Bh/3Bh/6Bh/BBh/EBh is available to read out the data in the Cache Register.
2. For high speed performance, we recommend to use EBh to read out the data in the Cache Register. (Please refer to 8.8 Read From Cache Quad IO)
3. We recommend to use GET FEATURES command (0Fh) to read the status until CBSY=0.

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8.4 Read From Cache (03H or 0BH)

The command sequence is shown below.

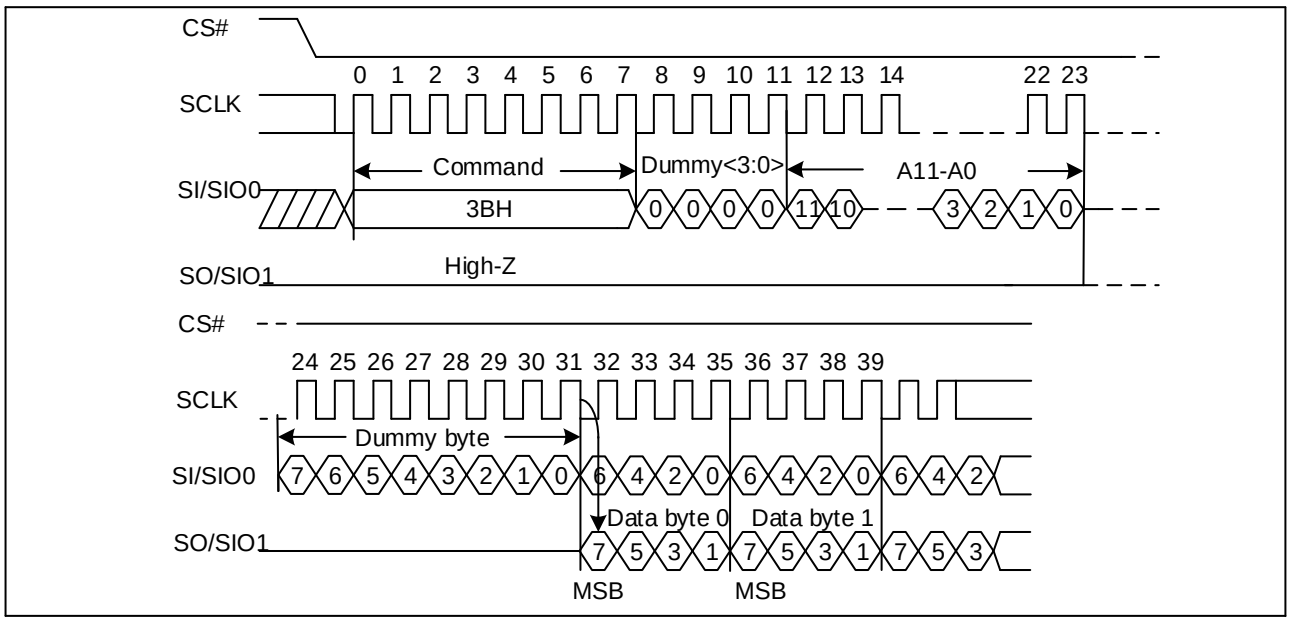
Figure 8-7.Read From Cache Timing Diagram



8.5 Read From Cache x2 (3BH)

The command sequence is shown below.

Figure 8-8.Read From Cache x2 Timing Diagram

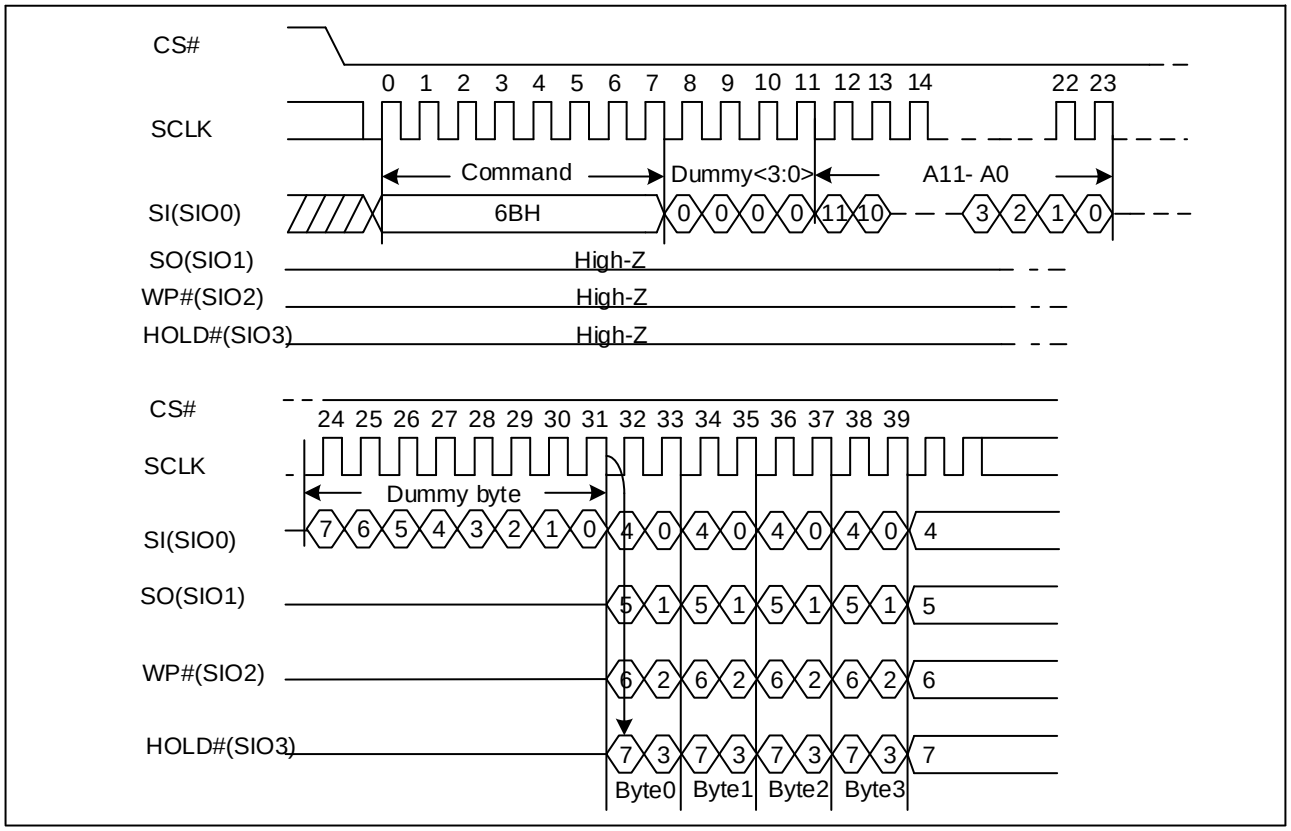


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8.6 Read From Cache x4 (6BH)

The Quad Enable bit (QE) of feature (B0[0]) must be set to enable the read from cache x4 command. The command sequence is shown below.

Figure 8-9.Read From Cache x4 Timing Diagram

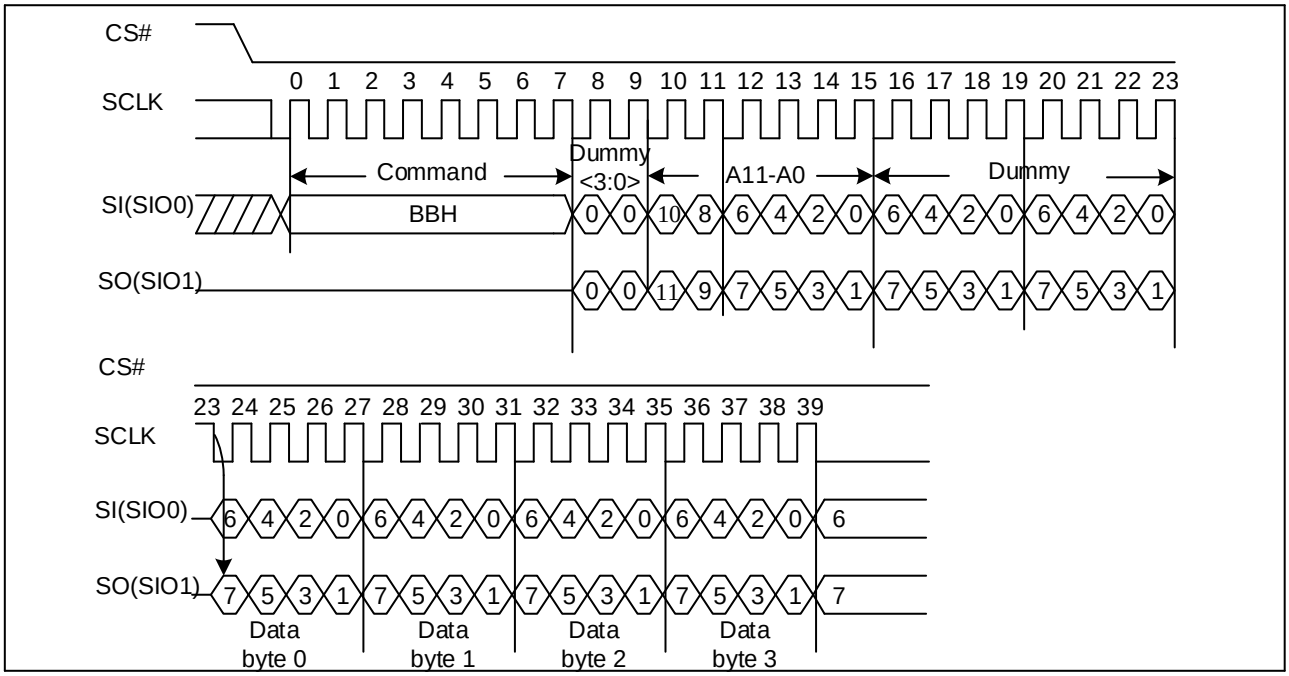


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8.7 Read From Cache Dual IO (BBH)

The Read from Cache Dual I/O command (BBH) is similar to the Read form Cache x2 command (3BH) but with the capability to input the 4 Dummy bits, followed by a 12-bit column address for the starting byte address and dummy bytes by SIO0 and SIO1, each bit being latched in during the rising edge of SCLK, then the cache contents are shifted out 2-bit per clock cycle from SIO0 and SIO1. The first address byte can be at any location. The address increments automatically to the next higher address after each byte of data shifted out. The command sequence is shown below.

Figure 8-10.Read From Cache Dual IO Timing Diagram

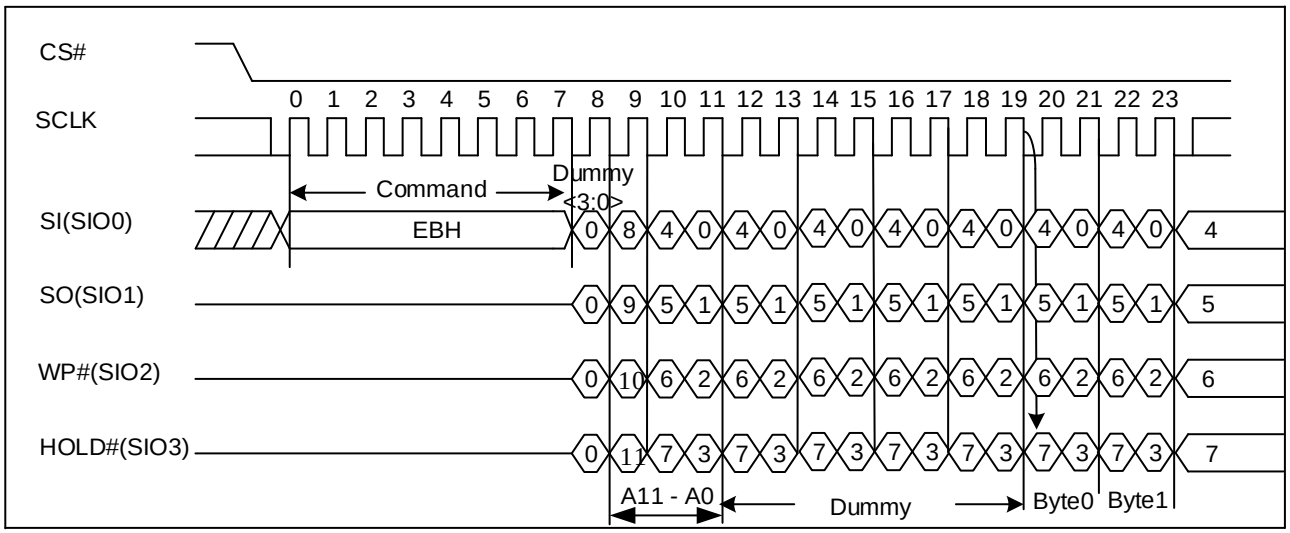


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8.8 Read From Cache Quad IO (EBH)

The Read from Cache Quad IO command is similar to the Read from Cache x4 command but with the capability to input the 4 dummy bits, followed a 12-bit column address for the starting byte address and dummy bytes by SIO0, SIO1, SIO3, SIO4, each bit being latched in during the rising edge of SCLK, then the cache contents are shifted out 4-bit per clock cycle from SIO0, SIO1, SIO2, SIO3. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The Quad Enable bit (QE) of feature (B0[0]) must be set to enable the read from cache quad IO command. The command sequence is shown below.

Figure 8-11.Read From Cache Quad IO Timing Diagram



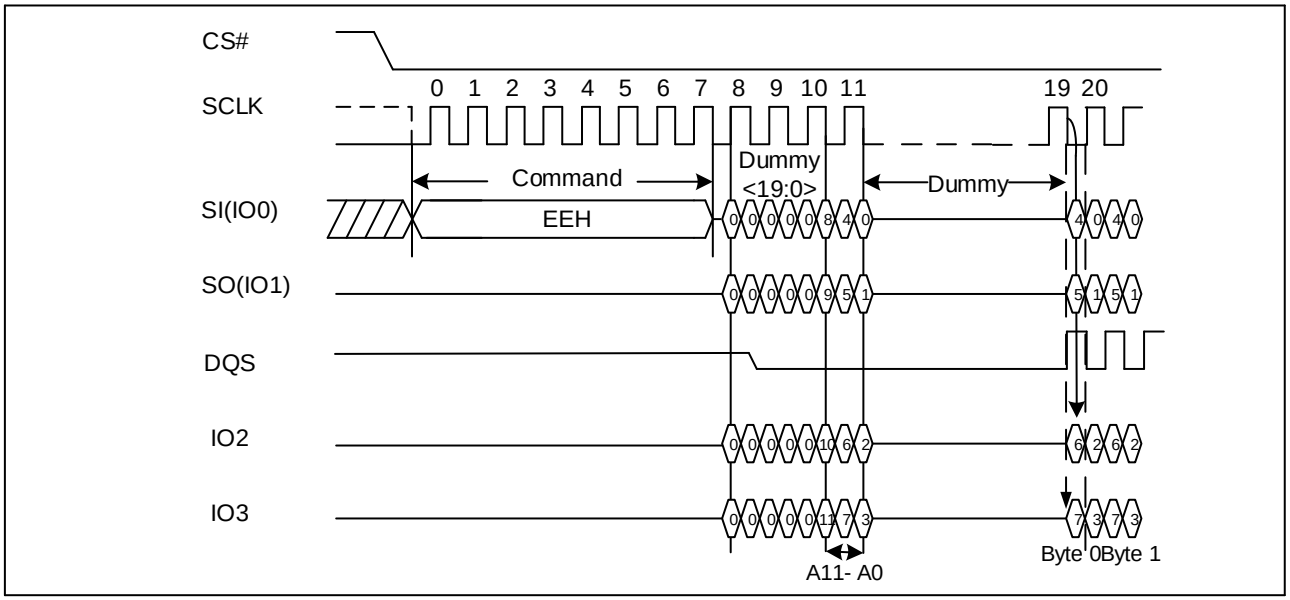
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8.9 Read From Cache Quad I/O DTR (EEH)

The DTR QIO command enables Double Transfer Rate throughput on quad I/O of Serial Flash in read mode. A Quad Enable (QE) bit of status Register must be set to "1" before sending the DTR QIO command. The address (interleave on 4 I/O pins) is latched on both rising and falling edge of SCLK, and data (interleave on 4 I/O pins) shift out on both rising and falling edge of SCLK. The 8-bit address can be latched-in at one clock, and 8-bit data can be read out at one clock, which means four bits at rising edge of clock, the other four bits at falling edge of clock.

The first address Byte can be at any location. The address is automatically increased to the next higher address after each Byte data is shifted out, so the whole page can be read out at a single DTR QIO command. The address counter rolls over to 0 when the highest address has been reached.

Figure 8-12.Read From Cache Quad I/O DTR Timing Diagram



Note:

Please contact GigaDevice when there is a need to use the EEh command for DTR.

The max clock rate for DTR depends on the tCLQV (clock to data output valid). Per datasheet, with output load capacitance of 30pf, the tCLQV is about 11ns. This will limit the max rate to 45Mhz.

However, in general, most of PCB designs have output loading much less than 30pf. Lower output loading will in turn shorten the tCLQV and result in higher max clock rate.

GigaDevice recommend customers measure the tCLQV and then set the clock rate to match the SPI host data sampling data setup time and hold time.

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8.10 Read ID (9FH)

The READ ID command is used to identify the NAND Flash device.

• With address 00H, the READ ID command outputs the Manufacturer ID and the device ID. See Table 8-2 for details.

Figure 8-13.Read ID Timing Diagram

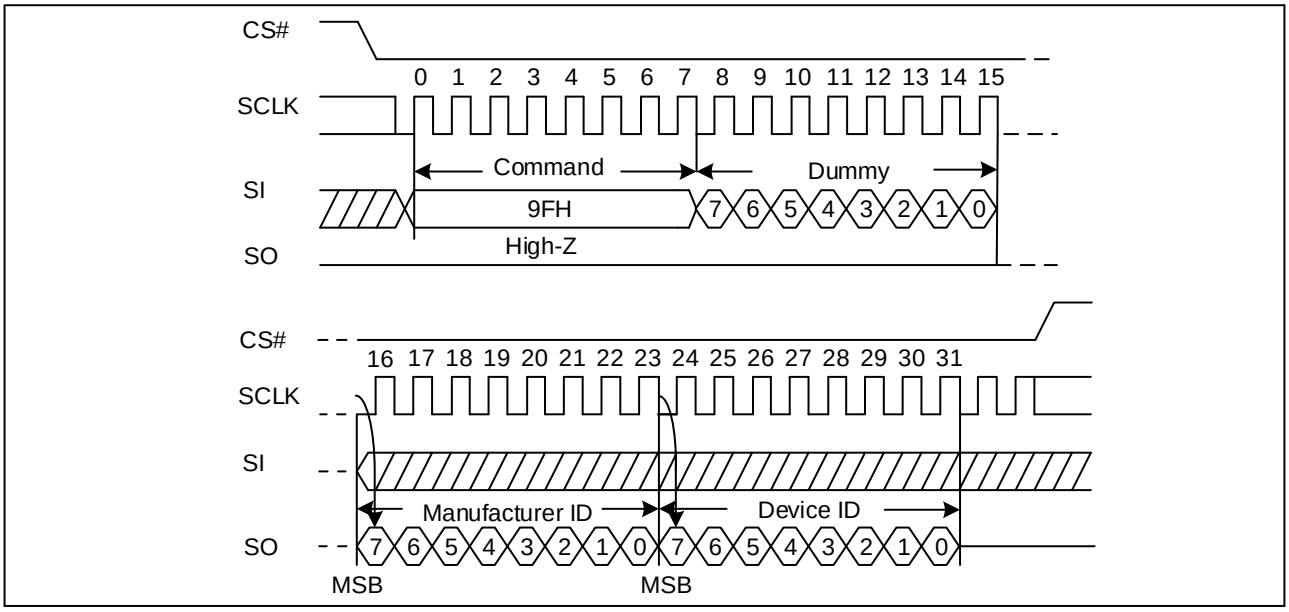


Table 8-2. READ ID Table

Part No	MID	DID1
GD5F2GQ5UExxG	C8H	52H
GD5F2GQ5RExxG	C8H	42H

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8.11 Read UID

The Read Unique ID function is used to retrieve the 16 byte unique ID (UID) for the device. The unique ID when combined with the device manufacturer shall be unique.

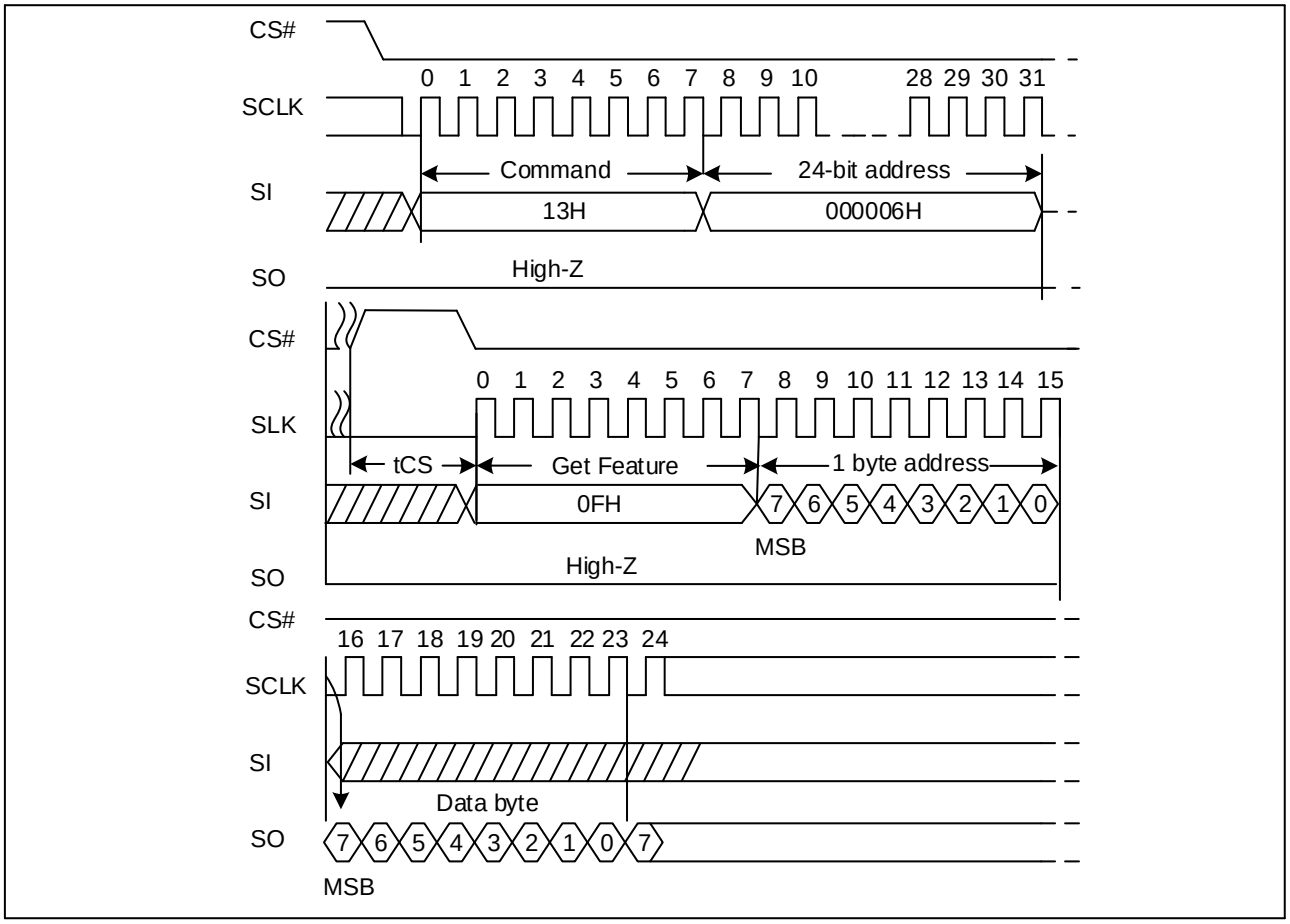
The UID data may be stored within the Flash array. To allow the host to determine if the UID is without bit errors, the UID is returned with its complement. If the XOR of the UID and its bit-wise complement is all ones, then the UID is valid. To accommodate robust retrieval of the UID in the case of bit errors, sixteen copies of the UID and the corresponding complement are stored by the target. For example, reading byte 32-63 returns to the host another copy of the UID and its complement.

Bytes	Value
0-15	UID
16-31	UID complement (bit-wise)

Sequence is as follows:

1. Use Set Feature command to set B0 register, to enable OTP_EN.
2. Use Get Feature command to get data from B0 register and check if the OTP_EN is enable.
3. Use Page Read to Cache (13h) command with address 24'h000006h, read data from array to cache.
4. Use 0FH (GET FEATURES command) read the status.
5. User can use Read from cache command (03H/0BH), read 16 bytes UID from cache.

Figure 8-14.Read UID to cache and Get Feature command Timing Diagram



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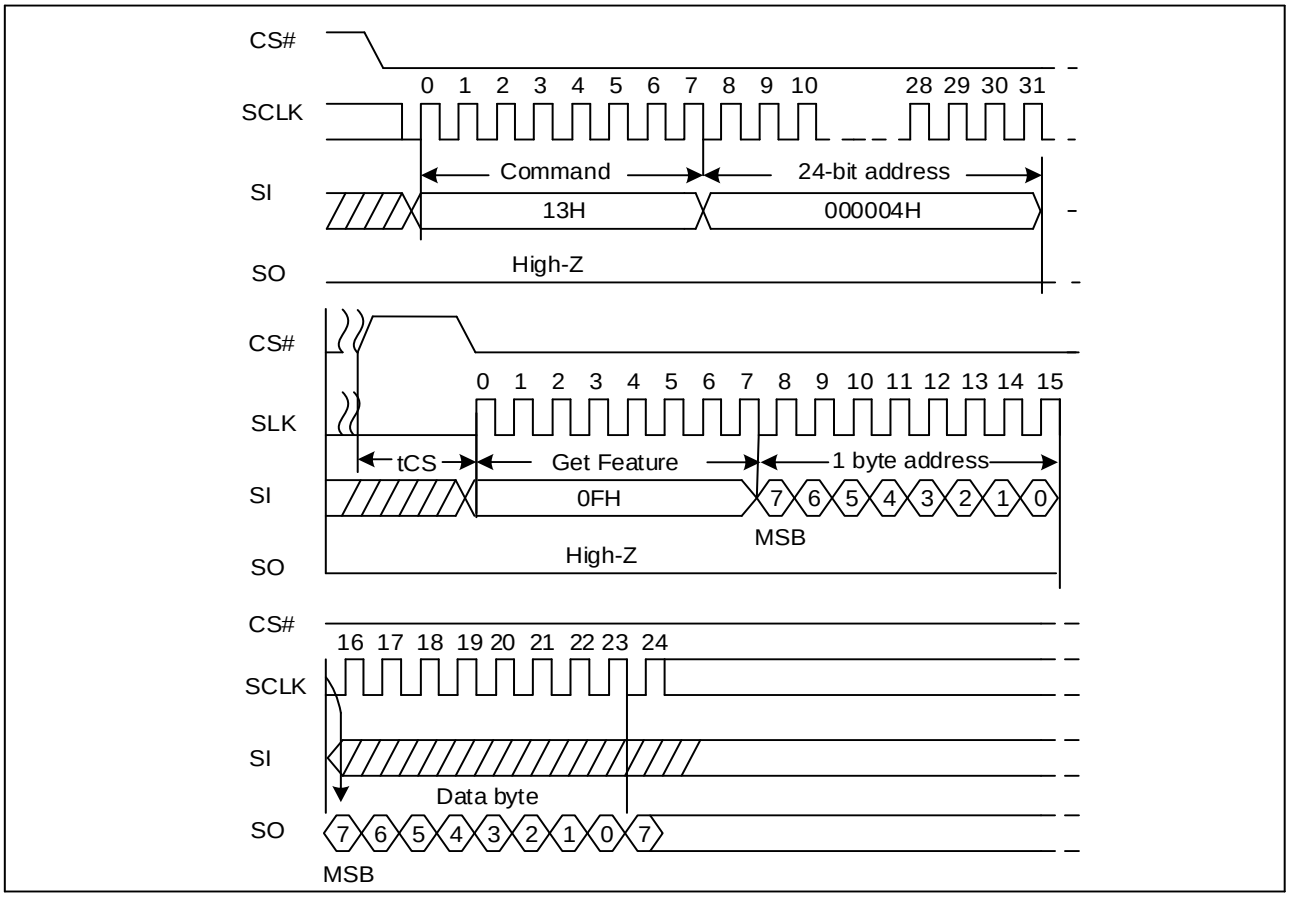
8.12 Read Parameter Page

The Read Parameter Page function retrieves the data structure that describes the chip's organization, features, timing and other behavioral parameters. This data structure enables the host processor to automatically recognize the SPI-NAND Flash configuration of a device. A minimum of three copies of the parameter page are stored in the device. The Read from Cache command can be used to change the location of data output.

Sequences as follows:

1. Use Set Feature command to set B0 register, to enable OTP_EN.
2. Use Get Feature command to get data from B0 register and check if the OTP_EN is enable.
3. Use Page Read to Cache (13h) command with address 24'h000004. Load parameter page from array to cache.
4. Use 0Fh (GET FEATURES command) read the status
5. User can use Read from cache command (03h/0Bh), read parameter page from cache.

Figure 8-15.Read parameter page to cache and Get Feature command Timing Diagram



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Parameter page table as follow

<table>
<tr><th>Byte</th><th>O/M</th><th>Description</th><th>3.3V/1.8V</th></tr>
<tr><td>0-3</td><td>M</td><td>Parameter page signature
Byte 0: 4FH, “O”
Byte 1: 4EH, “N”
Byte 2: 46H, “F”
Byte 3: 49H, “I”</td><td>4FH
4EH
46H
49H</td></tr>
<tr><td>4-5</td><td>M</td><td>Revision number
0-15 Reserved (0)</td><td>00H
00H</td></tr>
<tr><td>6-7</td><td>M</td><td>Features supported
0-15 Reserved (0)</td><td>00H
00H</td></tr>
<tr><td>8-9</td><td>M</td><td>Reserved (0)</td><td>00H
00H</td></tr>
<tr><td>10-31</td><td></td><td>Reserved (0)</td><td>00H
…
00H</td></tr>
<tr><td></td><td></td><td>Manufacturer Information block</td><td></td></tr>
<tr><td>32-43</td><td>M</td><td>Device manufacturer (12 ASCII characters)“GIGADEVICE ”</td><td>47H
49H
47H
41H
44H
45H
56H
49H
43H
45H
20H
20H</td></tr>
<tr><td>44-63</td><td>M</td><td>Device model (20 ASCII characters)
<table>
<tr><th>Device Model</th><th>ORGANIZATION</th><th>VCC RANGE</th></tr>
<tr><td>“GD5F2GQ5U”</td><td>X4</td><td>2.7v ~ 3.6v</td></tr>
<tr><td>“GD5F2GQ5R”</td><td>X4</td><td>1.7v ~ 2.0v</td></tr>
</table></td><td>47H
44H
35H
46H
32H
47H
51H
35H
55H/52H
20H
20H
20H
20H
20H
20H</td></tr>
</table>

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			20H 20H 20H 20H 20H
64	M	JEDEC manufacturer ID“C8”	C8H
65-66	O	Date code	00H 00H
67-79		Reserved	00H 00H 00H
		Memory organization block	
80-83	M	Number of data bytes per page	00H 08H 00H 00H
84-85	M	Number of spare bytes per page	80H 00H
86-89	M	Number of data bytes per partial page	00H 02H 00H 00H
90-91	M	Number of spare bytes per partial page	20H 00H
92-95	M	Number of pages per block	40H 00H 00H 00H
96-99	M	Number of blocks per logical unit	00H 08H 00H 00H
100	M	Number of logical units	01H
101	M	Reserved	00H
102	M	Number of bits per cell	01H
103-104	M	Bad blocks maximum per logical unit	28H 00H
105-106	M	Block endurance	01H 05H
107	M	Guaranteed valid blocks at beginning of target	01H
108-109	M	Block endurance for guaranteed valid blocks	00H 00H

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110	M	Number of programs per page	04H
111	M	Partial programming attributes 5-7 Reserved 4 1 = partial page layout is partial page data followed by partial page spare 1-3 Reserved 0 1 = partial page programming has constraints	00H
112	M	Number of bits ECC correctability	00H
113	M	Number of interleaved address bits 4-7 Reserved (0) 0-3 Number of interleaved address bits	00H
114	O	Interleaved operation attributes 4-7 Reserved (0) 3 Address restrictions for program cache 2 1 = program cache supported 1 1 = no block address restrictions 0 Overlapped / concurrent interleaving support	00H
115-127		Reserved	00H … 00H
		Electrical parameters block	
128	M	I/O capacitance	06H
129-130	M	IO clock support 3-1 5 Reserved (0) 2 1 = supports 80MHz 1 1 = supports 104MHz 0 1 = supports 120MHz	02H/04H 00H
131-132	O	Reserved (0)	00H 00H
133-134	M	tPROG Maximum page program time (us)	58H 02H
135-136	M	tBERS Maximum block erase time (us)	88H 13H
137-138	M	tR Maximum page read time (us)	3CH 00H
139-140	M	Reserved	00H 00H
141-163		Reserved	00H
		Vendor block	
164-165	M	Vendor specific Revision number	00H
166-253		Vendor specific	00H
254-255	M	Integrity CRC	Set on test
		Redundant parameter pages	
256-511	M	Value of bytes 0-255	

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512-767	M	Value of bytes 0-255	
768+	O	Additional redundant parameter pages	

Notes:

1. “O” Stands for Optional, “M” for Mandatory
2. The Integrity CRC (Cycling Redundancy Check) field is used to verify that the contents of the parameters page were transferred correctly to the host. Please refer to ONFI 1.0 specifications for details. The CRC shall be calculated using the following 16-bit generator polynomial: $G(X) = X^{16} + X^{15} + X^2 + 1$，This polynomial in hex may be represented as 8005h.

3. The CRC value shall be initialized with a value of 4F4Eh before the calculation begins. There is no XOR applied to the final CRC value after it is calculated. There is no reversal of the data bytes or the CRC calculated value.

Device Model	ORGANIZATION	VCC RANGE	CRC value B254/B255
“GD5F2GQ5UxxxG”	X4	2.7v ~ 3.6v	5BH/05H
“GD5F2GQ5RxxxG”	X4	1.7v ~ 2.0v	96H/48H

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9 PROGRAM OPERATIONS

9.1 Page Program

The PAGE PROGRAM operation sequence programs 1 byte to whole page bytes of data within a page. The page program sequence is as follows:

- 02H (PROGRAM LOAD)/32H (PROGRAM LOAD x4)
- 06H (WRITE ENABLE)
- 10H (PROGRAM EXECUTE)
- 0FH (GET FEATURE command to read the status)

Firstly, a PROGRAM LOAD (02H/32H) command is issued. PROGRAM LOAD consists of an 8-bit Op code, followed by 4 dummy bits and a 12-bit column address, then the data bytes to be programmed. The Program address should be in sequential order in a block. The data bytes are loaded into a cache register that is whole page long. If more than one page data are loaded, then those additional bytes are ignored by the cache register. The command sequence ends when CS# goes from LOW to HIGH. Figure 9-1 shows the PROGRAM LOAD operation. Secondly, prior to performing the PROGRAM EXECUTE operation, a WRITE ENABLE (06H) command must be issued. As with any command that changes the memory contents, the WRITE ENABLE must be executed in order to set the WEL bit. If this command is not issued, then the rest of the program sequence is ignored.

Note:

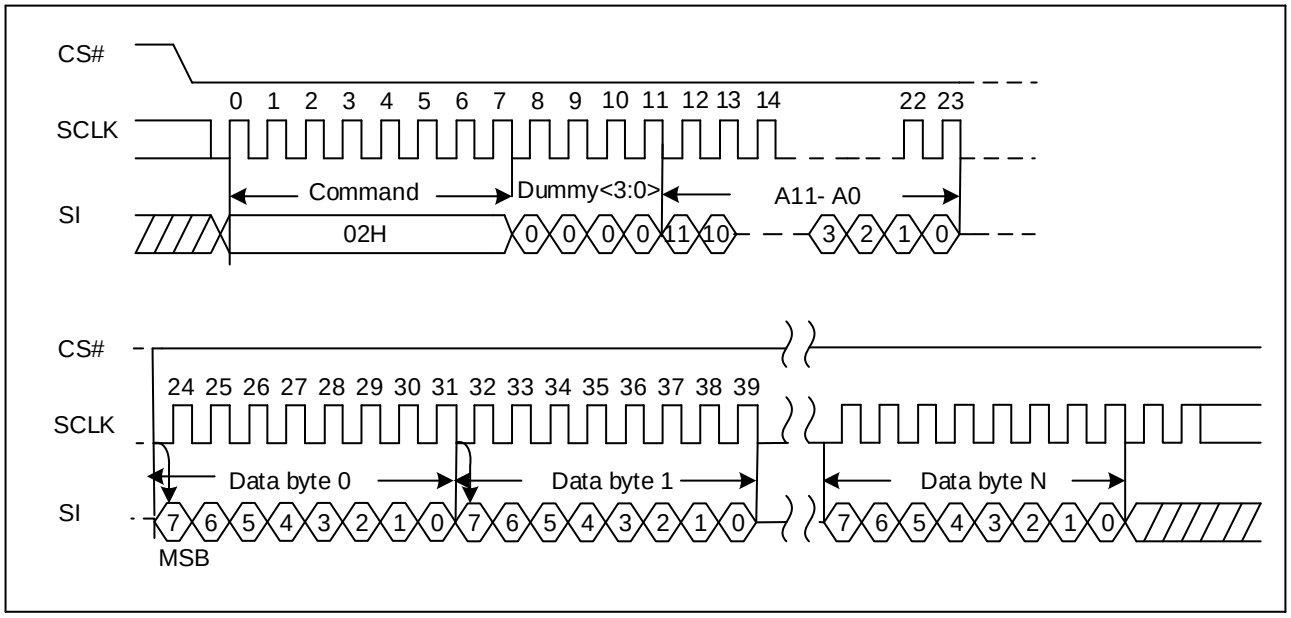
1. The contents of Cache Register doesn’t reset when Program Random Load (84h) command and RESET (FFh) command.
2. When Program Execute (10h) command was issued just after Program Load (02h) command, the 0xFF is output to the address that data was not loaded by Program Load (02h) command.
3. When Program Execute (10h) command was issued just after Program Load Random Data (84h) command, the contents of Cache Register is output to the NAND array.
4. The Program address should be in sequential order in a block.
5. Program Load x4 is only available with the QE enable.

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9.2 Program Load (PL) (02H)

The command sequence is shown below.

Figure 9-1. Program Load Timing Diagram



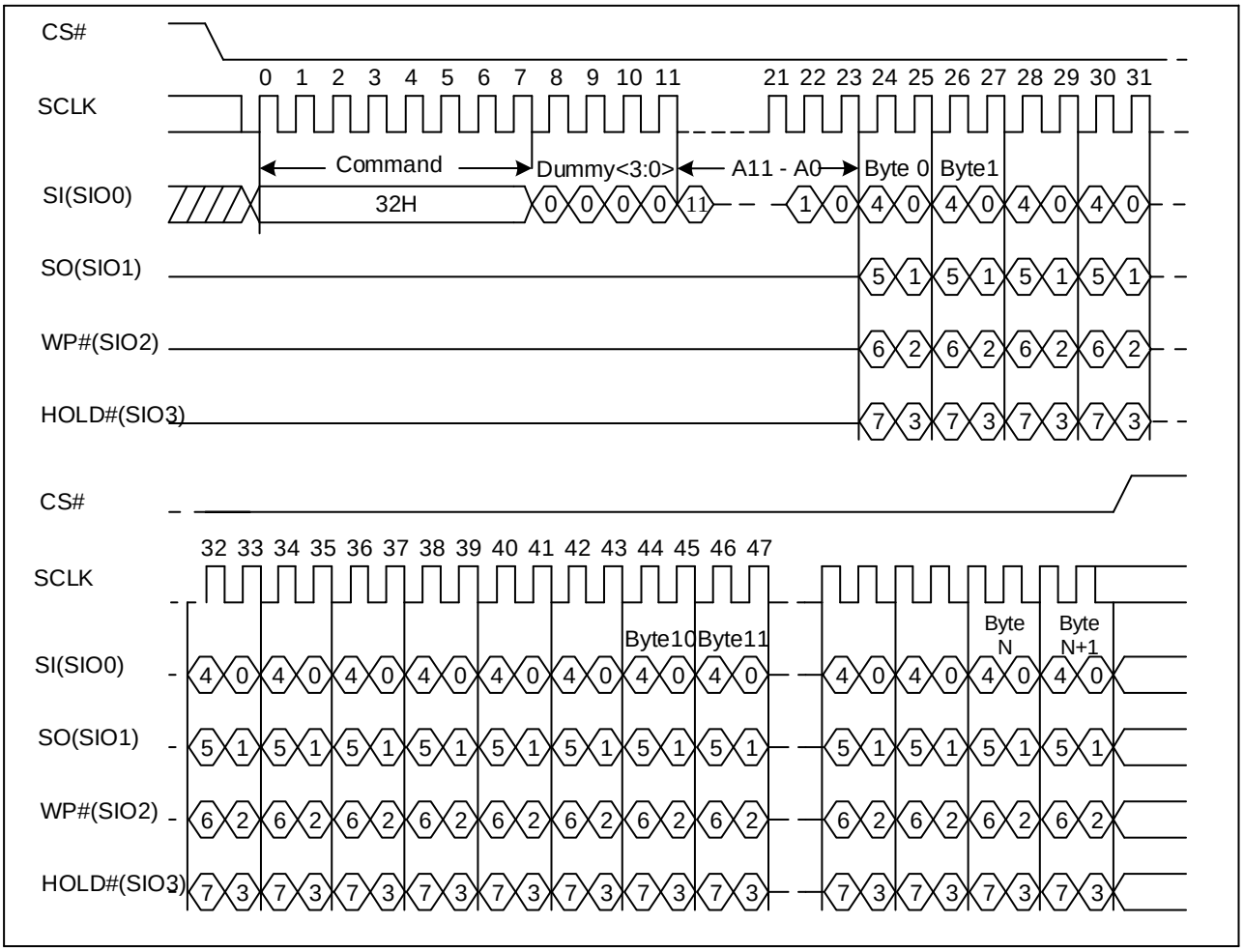
Note: When internal ECC disabled the Data Byte is 2176, when internal ECC enabled the Data Byte is 2112.

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9.3 Program Load x4 (PL x4) (32H)

The Program Load x4 command (32H) is similar to the Program Load command (02H) but with the capability to input the data bytes by four pins: SIO0, SIO1, SIO2, and SIO3. The Quad Enable bit (QE) of feature (B0[0]) must be set to enable the program load x4 command. The command sequence is shown below.

Figure 9-2. Program Load x4 Timing Diagram



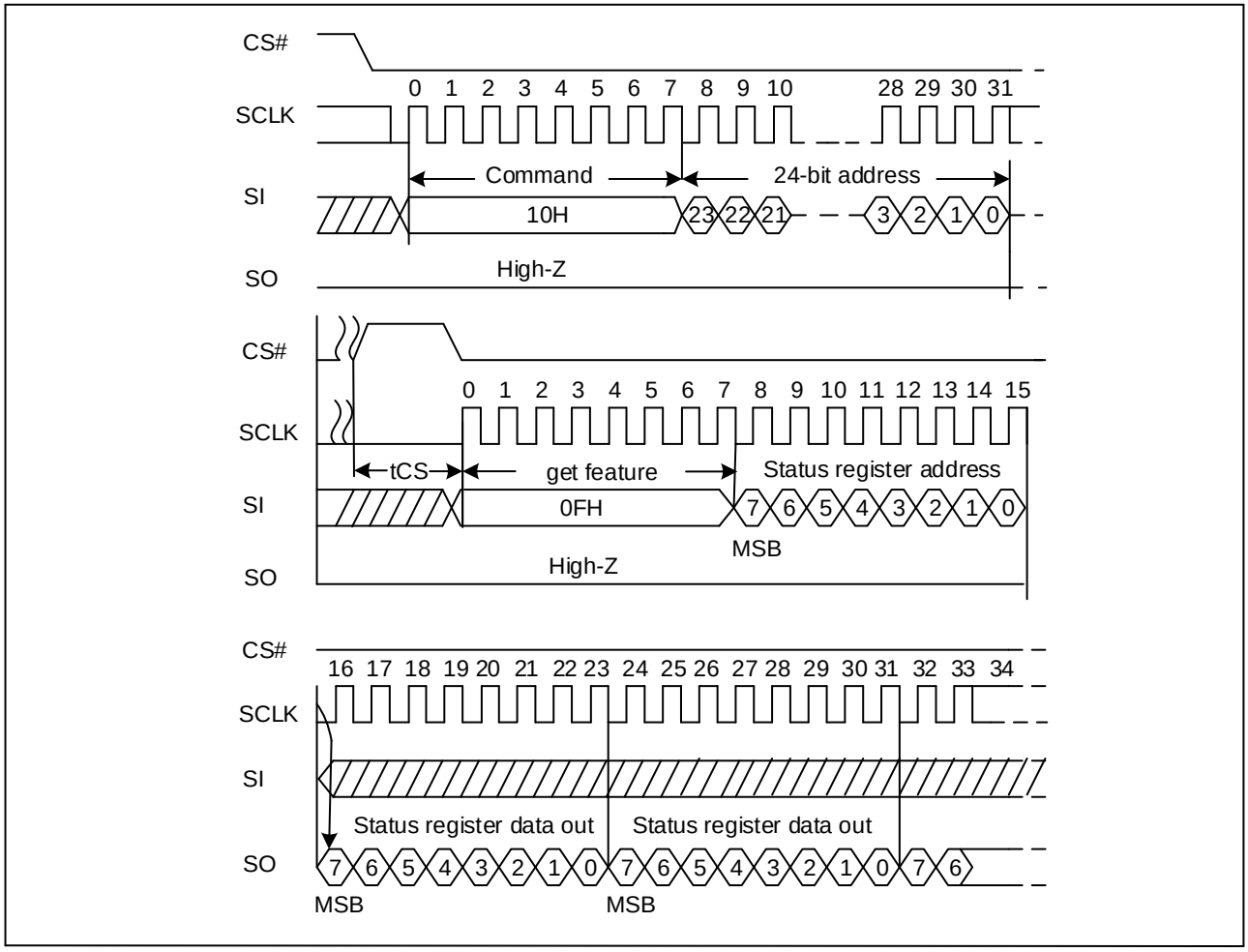
Note: When internal ECC disabled the Data Byte is 2176, when internal ECC enabled the Data Byte is 2112.

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9.4 Program Execute (PE) (10H)

After the data is loaded, a PROGRAM EXECUTE (10H) command must be issued to initiate the transfer of data from the cache registers to the main array. PROGRAM EXECUTE consists of an 8-bit Op code, followed by a 24-bit address. After the page/block address is registered, the memory device starts the transfer from the cache register to the main array, and is busy for tPROG time. This operation shown in Figure 9-3. During this busy time, the status register can be polled to monitor the status of the operation (refer to Status Register). When the operation completes successfully, the next series of data can be loaded with the PROGRAM LOAD command.

Figure 9-3. Program Execute Timing Diagram



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9.5 Program Execute Background (10h + address + 15h)

A “Cache Program” function has been implemented in SPI series to improve the overall program throughput. It is possible to program the data from Data Register to array the simultaneously while a Load Data command is being performed to write data to the Cache Register.

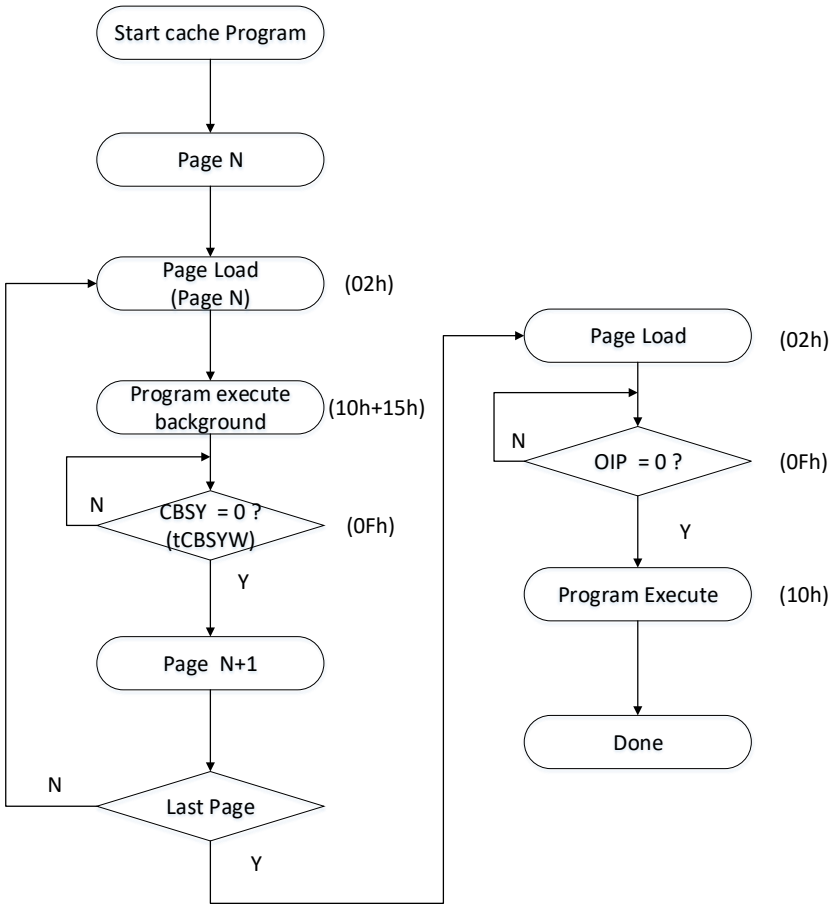
When multiple pages of data is to be program sequentially, the host should issue a “Program Load (02h)” command followed by a Column Address and data written. When the command is accepted, the host should use Program Execute Background（10h+address+15h）to initial the internal program operation, then the CBSY becomes 1.

Once the CBSY becomes 0, user can issue again the “Program Load (02h)” command followed by a Page Address and data written. Then user can send Program Execute Background command to continue the cache program.

When the last page of one block to be program and the OIP bit is 0, the program execute command (10h+address) should be used to finish the last program operation.

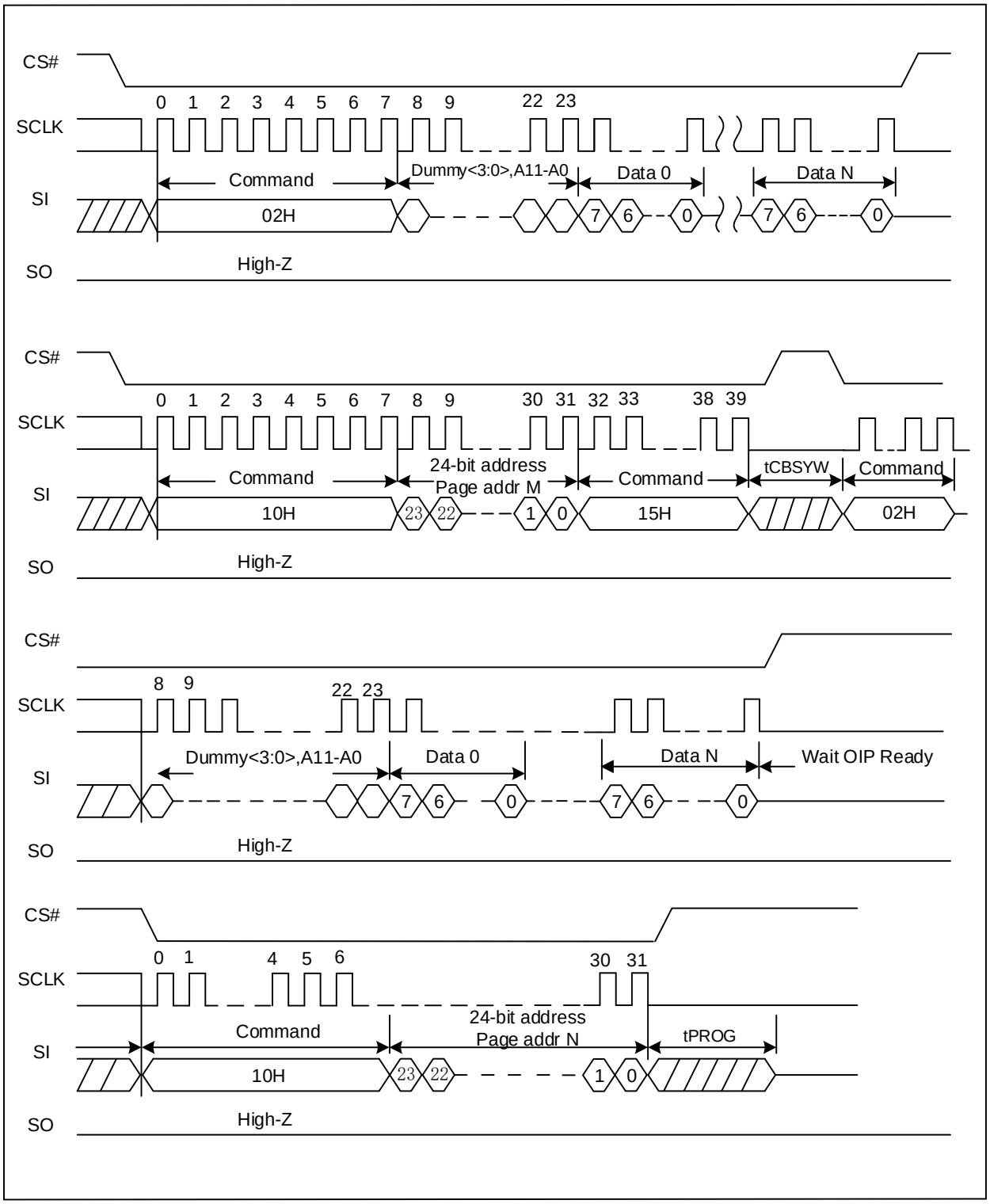
The program execute command (10h+address+15h) is allowed to cross blocks before reaching the last block.

Figure 9-4. Program Execute Background Operation Flow Chart



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Figure 9-5. Program Execute Background Timing



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9.6 Internal Data Move

The INTERNAL DATA MOVE command sequence programs or replaces data in a page with existing data. The INTERNAL DATA MOVE command sequence is as follows:

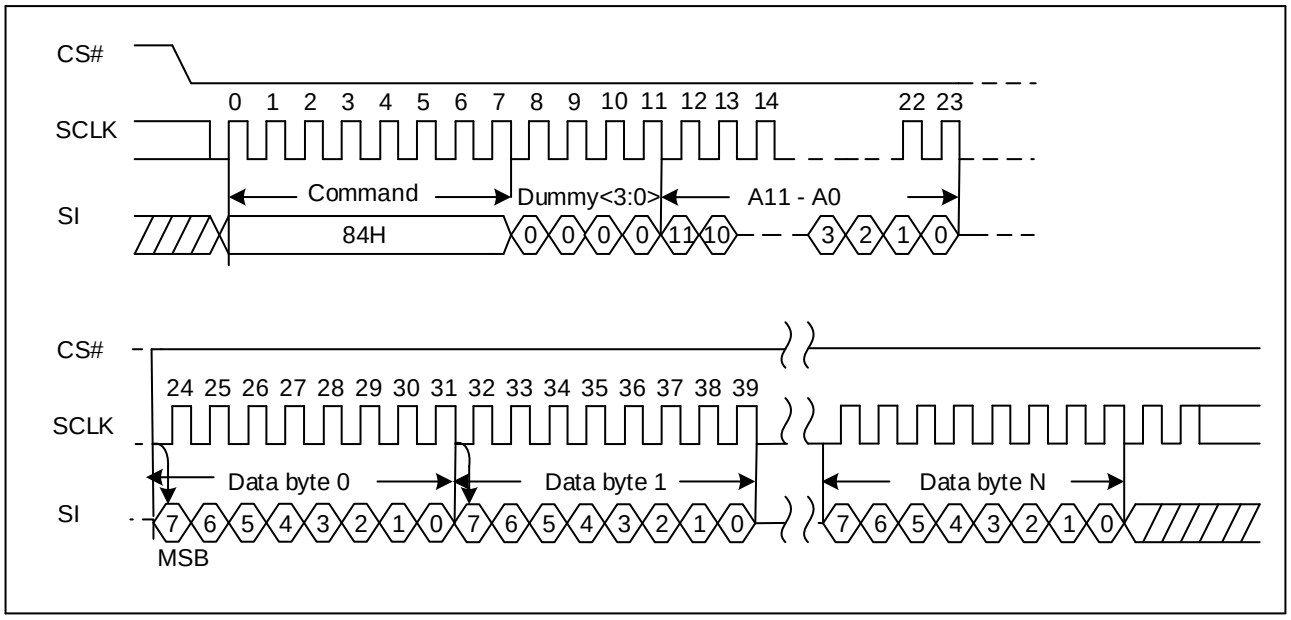
- 13H (PAGE READ to cache)
- Optional 84H/C4H/34H (PROGRAM LOAD RANDOM DATA)
- 06H (WRITE ENABLE)
- 10H (PROGRAM EXECUTE)
- 0FH (GET FEATURE command to read the status)

Prior to performing an internal data move operation, the target page content must be read out into the cache register by issuing a PAGE READ (13H) command. The PROGRAM LOAD RANDOM DATA (84H/C4H) command can be issued, if user wants to update bytes of data in the page. New data is loaded in the 12-bit column address. If the random data is not sequential, another PROGRAM LOAD RANDOM DATA (84H/C4H) command must be issued with the new column address. After the data is loaded, the WRITE ENABLE command must be issued, and then PROGRAMEXECUTE (10H) command can be issued to start the programming operation. Only the block with the same parity attribute can use the command.

9.7 Program Load Random Data (84H)

This command consists of an 8-bit Op code, followed by 4 dummy bits, and a 12-bit column address. New data is loaded in the column address provided with the 12 bits. If the random data is not sequential, then another PROGRAM LOAD RANDOM DATA (84H) command must be issued with a new column address, see Figure 9-6 for details. This command is only available during internal data move sequence.

Figure 9-6. Program Load Random Data Timing Diagram

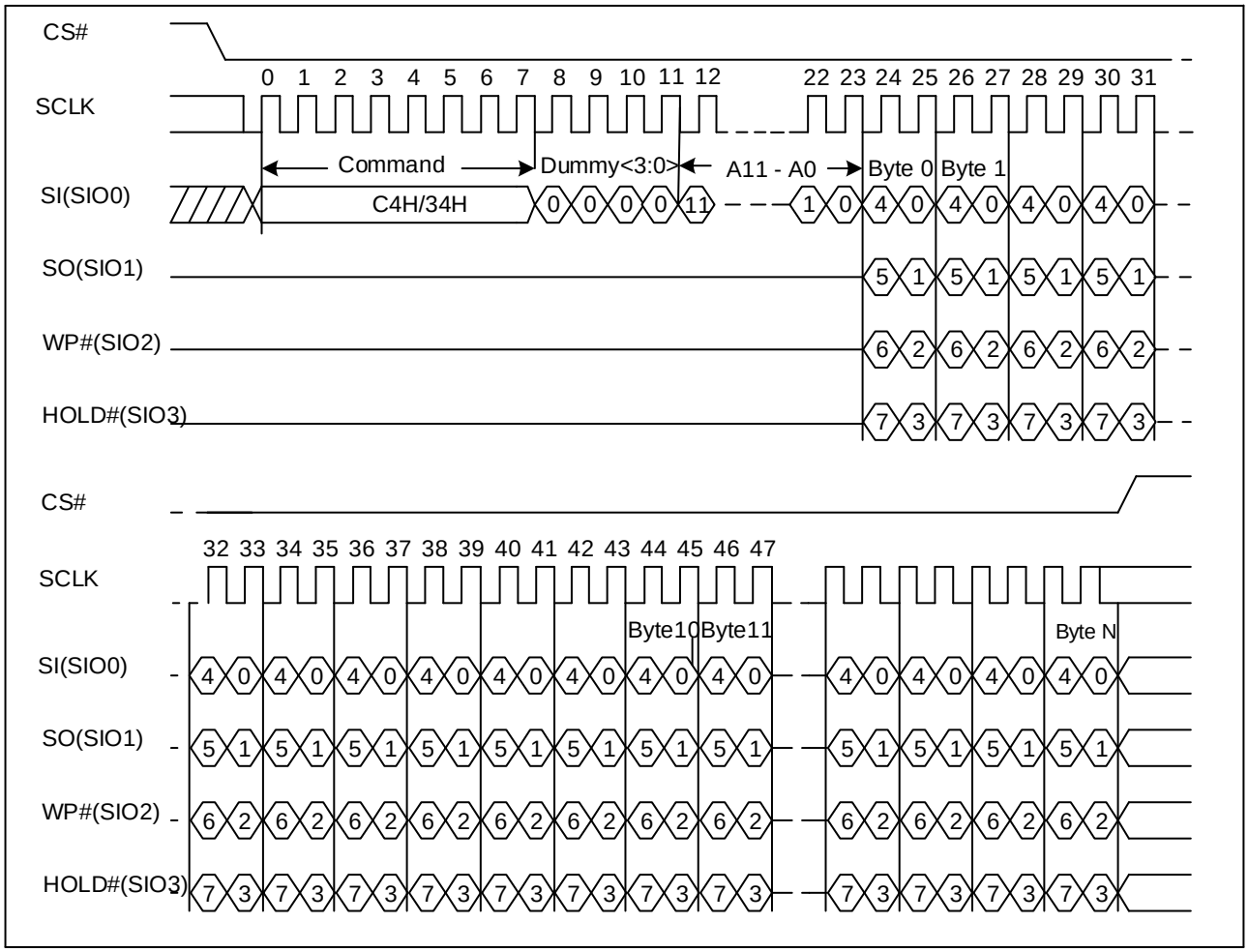


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9.8 Program Load Random Data x4 (C4H/34H)

The Program Load Random Data x4 command (C4H/34H) is similar to the Program Load Random Data command (84H) but with the capability to input the data bytes by four pins: SIO0, SIO1, SIO2, and SIO3. The command sequence is shown below. The Quad Enable bit (QE) of feature (B0[0]) must be set to enable for the program load random data x4 command. See Figure 9-7 for details. Those two commands are only available during internal data move sequence.

Figure 9-7. Program Load Random Data x4 Timing Diagram



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10 ERASE OPERATIONS

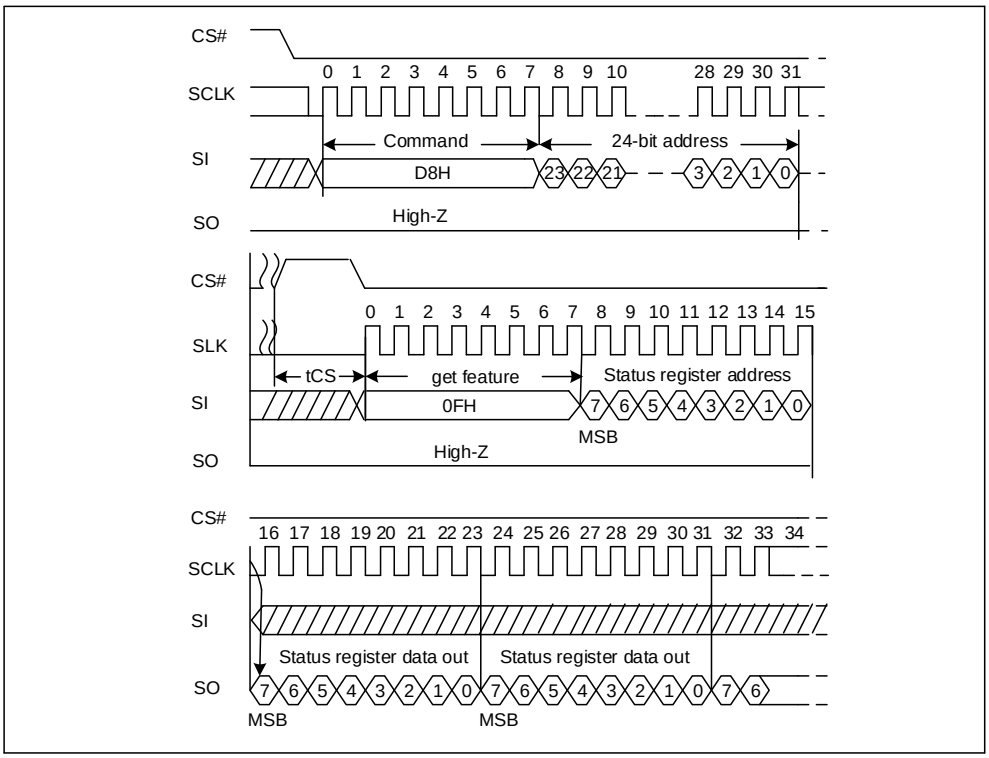
10.1 Block Erase (D8H)

The BLOCK ERASE (D8H) command is used to erase at the block level. The BLOCK ERASE command (D8H) operates on one block at a time. The command sequence for the BLOCK ERASE operation is as follows:

- 06H (WRITE ENBALE command)
- D8H (BLOCK ERASE command)
- 0FH (GET FEATURES command to read the status register)

Prior to performing the BLOCK ERASE operation, the WRITE ENABLE (06H) command must be issued. As with any command that changes the memory contents, the WRITE ENABLE command must be executed in order to set the WEL bit. If the WRITE ENABLE command is not issued, then the rest of the erase sequence is ignored. The WRITE ENABLE command must be followed by the BLOCK ERASE (D8H) command. This command requires a 24-bit address. After the row address is registered, the control logic automatically controls timing and erase-verify operations. The device is busy for tBERS time during the BLOCK ERASE operation. The GET FEATURES (0FH) command can be used to monitor the status of the operation.

Figure10-1. Block Erase Timing Diagram



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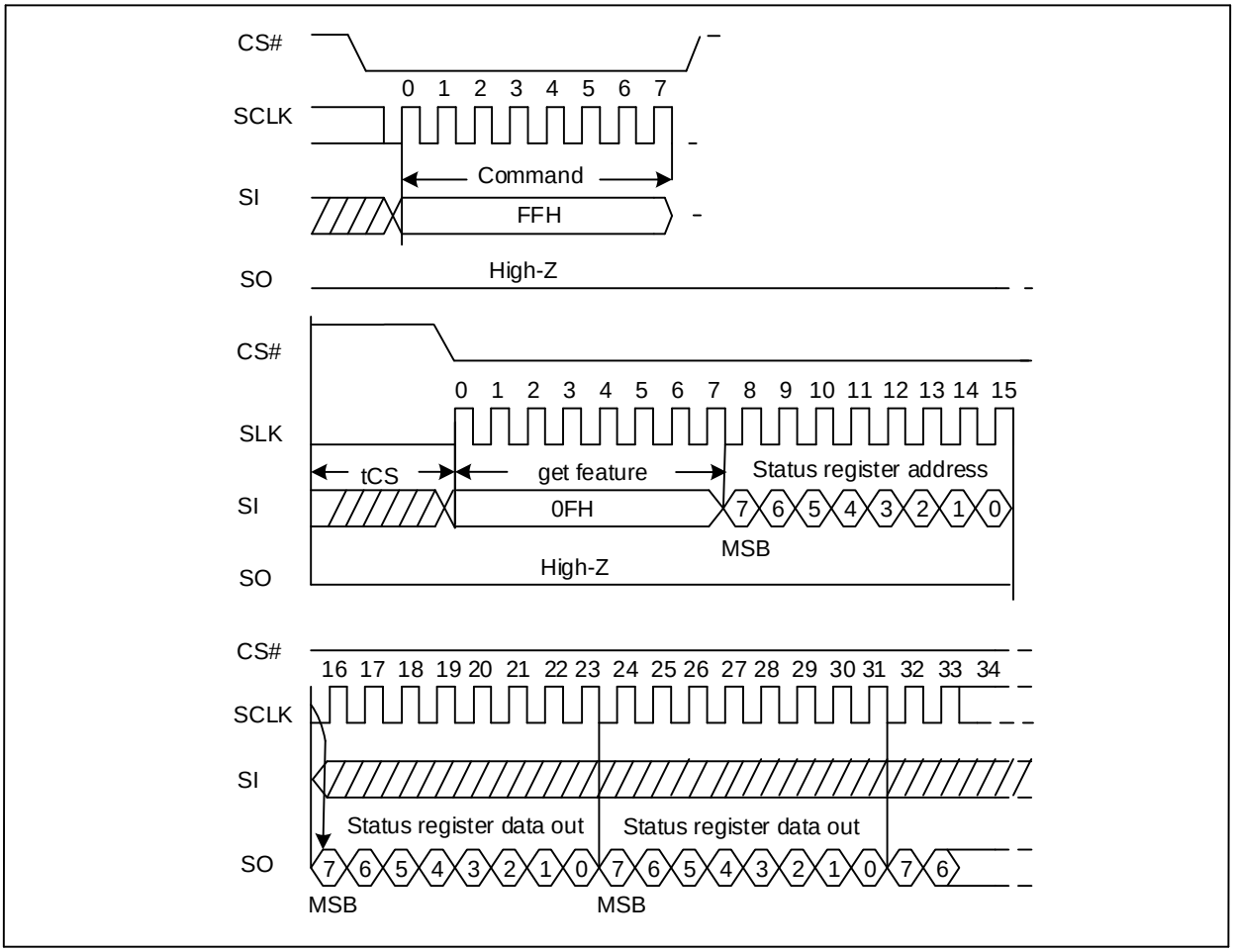
11 RESET OPERATIONS

11.1 Soft Reset (FFH)

The RESET (FFH) command stops all operations and the status. For example, in case of a program or erase or read operation, the reset command can make the device enter the idle state.

During a cache program or cache read, a reset can also stops the previous operation and the pending operation.

Figure11-1. Reset Timing Diagram



Note: The Register bit value after soft reset refers to Table 12-2.Register bit Descriptions.

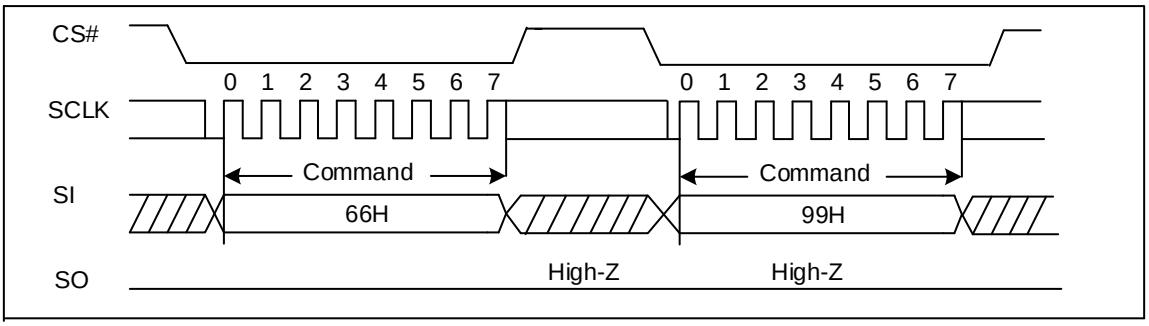
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11.2 Enable Power on Reset (66H) and Power on Reset (99H)

If the Power on Reset command is accepted, any on-going internal operation will be terminated and the device will return to its default power-on state and lose all the current feature settings.

The “Enable Reset (66H)” and the “Reset (99H)” commands can be issued in SPI mode. The “Reset (99H)” command sequence as follow: CS# goes low -> Sending Enable Reset command ->CS# goes high ->CS# goes low.->Sending Reset command ->CS# goes high. Once the Reset command is accepted by the device, the device will take approximately tVSL to reset. During this period, no command will be accepted.

Figure11-2. Reset Timing Diagram



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12 FEATURE OPERATIONS

12.1 Get Features (0FH) and Set Features (1FH)

The GET FEATURES (0FH) and SET FEATURES (1FH) commands are used to monitor the device status and alter the device behavior. These commands use a 1-byte feature address to determine which feature is to be read or modified. Feature such as OTP can be enabled or disabled by setting specific feature bits (shown in the below table).The status registers (C0H/F0H) is mostly read, except WEL, which is a writable bit with the WRITE ENABLE (06H) command.

When a feature (A0H/B0H/D0H) is set, it remains active until the device is power cycled or the feature is written to. Unless otherwise specified in the following table, once the device is set, it remains set, even if a RESET (FFH) command is issued.

Table 12-1. Features Settings

Register	Addr.	7	6	5	4	3	2	1	0
Protection	A0H	BRWD	Reserved	BP2	BP1	BP0	INV	CMP	Reserved
Feature	B0H	OTP_PRT	OTP_EN	Reserved	ECC_EN	Reserved	Reserved	Reserved	QE
Status	C0H	Reserved	Reserved	ECCS1	ECCS0	P_FAIL	E_FAIL	WEL	OIP
Feature	D0H	Reserved	DS_IO[1]	DS_IO[0]	Reserved	Reserved	Reserved	Reserved	Reserved
Status	F0H	Reserved	Reserved	ECCSE1	ECCSE0	BPS	Reserved	Reserved	CBSY

Note: If BRWD is enabled and WP# is LOW, then the block lock register cannot be changed.

If QE is enabled, the quad IO operations can be executed.

All the reserved bits must be held low when the feature is set.

These registers A0H/B0H/D0H are write/read type, and Registers C0H/F0H are read only.

The Register Bit default value after power-up refers to Table 12-2.Register Bit Descriptions.

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Table 12-2. Register Bit Descriptions

Bit	Bit Name	After Power up or Power on Reset(66H-99H)	After Reset command (FFH)	Description
BRWD	Block register write disable	0	No Change	Which is used combined with WP#, If BRWD is high enabled and WP# is LOW, then the Protection register cannot be changed
BP2 BP1 BP0 INV CMP	Block Protection bits	1 1 1 0 0	No Change	Used combination, refer to chapter Block Protection
OTP_PRT OTP_EN	OTP Region bits	0 0 Before OTP Set	No Change	Used combination, refer to chapter OTP Region
ECC_EN	ECC Enable Latch	1	No Change	The device offers data corruption protection by offering optional internal ECC. READs and PROGRAMs with internal ECC can be enabled or disabled by setting feature bit ECC_EN. ECC is enabled by default when device powered on, so the default READ and PROGRAM commands operate with internal ECC in the “active” state when ECC enable.
QE	The Quad Enable bit	0	No Change	This bit indicates that whether the quad IO operations can be executed. If QE is set to 1, the quad IO operations can be executed.
ECCS0 ECCS1 ECCSE0 ECCSE1	ECC Status	Page 0 Status	0 0 0 0	ECCS provides ECC status as the following table. ECCS and ECCSE are set to 00b either following a RESET, or at the beginning of the READ. They are then updated after the device completes a valid READ operation. ECCS and ECCSE are invalid if internal ECC is disabled (via a SET FEATURES command to reset ECC_EN to 0). After power-on RESET, ECC status is set to reflect the contents of block 0, page 0.
P_FAIL	Program Fail	0	0	This bit indicates that a program failure has occurred (P_FAIL =1). It will also be set if the user attempts to program a protected region, including the OTP area. This bit is cleared during the PROGRAM EXECUTE command sequence or a RESET command (P_FAIL = 0).
E_FAIL	Erase Fail	0	0	This bit indicates that an erase failure has occurred (E_FAIL = 1). It will also be set if the user attempts to erase a locked region. This bit is cleared (E_FAIL = 0) at the start of the BLOCK ERASE command sequence or the RESET command.

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WEL	Write Enable Latch	0	0	This bit indicates the current status of the write enable latch (WEL) and must be set (WEL = 1), prior to issuing a PROGRAM EXECUTE or BLOCK ERASE command. It is set by issuing the WRITE ENABLE command. WEL can also be disabled (WEL = 0), by issuing the WRITE DISABLE command.
OIP	Operation In Progress	0	0	This bit is set (OIP = 1) when a PROGRAM EXECUTE, PAGE READ, BLOCK ERASE, or RESET command is executing, indicating the device is busy. When the bit is 0, the interface is in the ready state.
DS_IO[0] DS_IO[1]	Driven Strength register	0 0	No Change	IO driver strength setting. Default is 00b.
BPS	Block Protection Status	1	No Change	Block protection status BPS is 1, selected block is protected BPS is 0, selected block is unprotected.
CBSY	Cache Busy status bit	0	0	CBSY is to indicate whether cache is busy, non-available for data read or data load. This bit is the status, which indicates if the cache is busy or ready, 1 is busy, 0 is ready.

Figure12-1. Get Features Timing Diagram

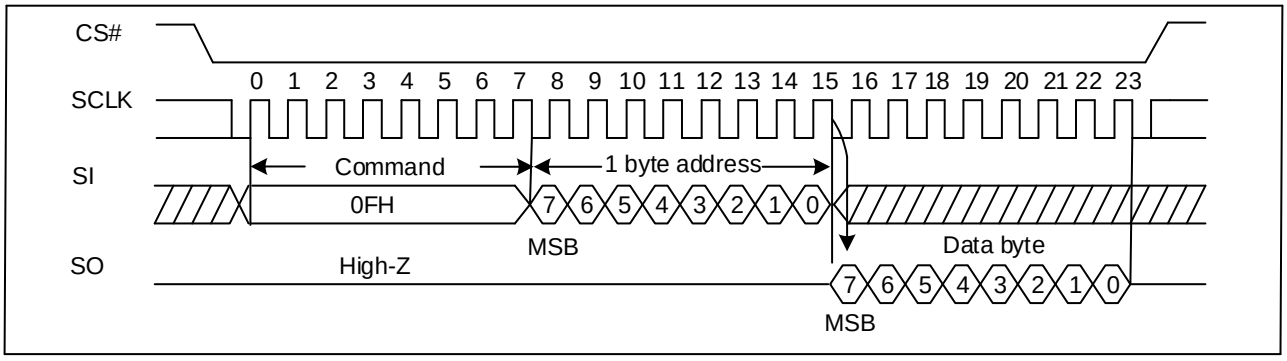
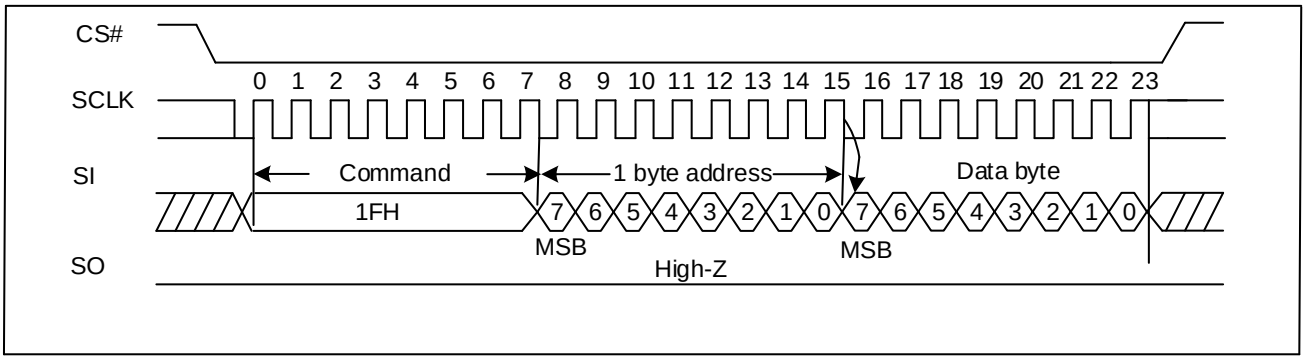


Figure12-2. Set Features Timing Diagram



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12.2 Status Register and Driver Register

The NAND Flash device has the status registers (C0H/F0H) that software can read during the device operation for operation state query. The status register can be read by issuing the GET FEATURES (0FH) command, followed by the feature address C0H or F0H (see FEATURE OPERATION). The Output Driver Register can be set and read by issuing the SET FEATURE (0FH) and GET FEATURE command followed by the feature address D0H (see FEATURE OPERATION).

Table 12-3.ECC Error Bits Descriptions

ECCS1	ECCS0	ECCSE1	ECCSE0	Description
0	0	x	x	No bit errors were detected during the previous read algorithm
0	1	0	0	Bit errors(=1) were detected and corrected
0	1	0	1	Bit errors (=2) were detected and corrected.
0	1	1	0	Bit errors (=3) were detected and corrected.
0	1	1	1	Bit errors (=4) were detected and corrected.
1	1	x	x	Reserved
1	0	x	x	Bit errors greater than ECC capability(4 bits) and not corrected

12-4.Driver Register Bits Descriptions

DS_IO[1]	DS_IO[0]	Driver Strength
0	0	100%
0	1	75%
1	0	50%
1	1	25%

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12.3 OTP Region

The serial device offers a protected, One-Time Programmable NAND Flash memory area. 4 full pages are available on the device. Customers can use the OTP area as they prefer, like programming serial numbers, or other data, for permanent storage. When delivered from factory, feature bit OTP_PRT is 0. To access the OTP feature, the user must set feature bits OTP_EN/OTP_PRT by SET FEATURES command. When the OTP is ready for access, only pages 00h–03H can be programmed in sequential order by PROGRAM LOAD (02H) and PROGRAM EXECUTE (10H) commands (when not yet protected), and read out by PAGE READ (13H) command and output data by READ from CACHE(03H/0BH/3BH/6BH).

Table 12-5.OTP States

OTP_PRT	OTP_EN	State
x	0	Normal Operation
0	1	Access OTP region, read and program data
1	1	1. When the device power on state OTP_PRT is 0, user can set feature bit OTP_PRT and OTP_EN to 1, then issue PROGRAM EXECUTE (10H) to lock OTP, and after that OTP_PRT will permanently remain 1. 2. When the device power on state OTP_PRT is 1, user can only read the OTP region data

Note: The OTP space cannot be erased and after it has been protected, it cannot be programmed again, please use this function carefully.

Access to OTP data

- Issue the SET FEATURES command (1FH)
- Set feature bit OTP_EN
- Issue the PAGE PROGRAM (only when OTP_PRT is 0) or PAGE READ command

Protect OTP region

Only when the following steps are completed, the OTP_PRT will be set and users can get this feature out with 0FH command.

- Issue the SET FEATURES command (1FH)
- Set feature bit OTP_EN and OTP_PRT
- 06H (WRITE ENABLE)
- Issue the PROGRAM EXECUTE (10H) command.

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12.4 Assistant Bad Block Management

As a NAND Flash, the device may have blocks that are invalid when shipped from the factory, and a minimum number of valid blocks (NVB) of the total available blocks are specified. An invalid block is one that contains at least one page that has more bad bits than can be corrected by the minimum required ECC. Additional bad blocks may develop with use. However, the total number of available blocks will not fall below NVB during the endurance life of the product.

Although NAND Flash memory devices may contain bad blocks, they can be used reliably in systems that provide bad-block management and error-correction algorithms, which ensure data integrity. Internal circuitry isolates each block from other blocks, so the presence of a bad block does not affect the operation of the rest of the NAND Flash array.

NAND Flash devices are shipped from the factory erased. The factory identifies invalid blocks before shipping by programming the Bad Block Mark (00h) to the first spare area location in each bad block. This method is compliant with ONFI Factory Defect Mapping requirements. See the following table for the bad-block mark.

System software should initially check the first spare area location for non-FFH data on the first page of each block prior to performing any program or erase operations on the NAND Flash device. A bad-block table can then be created, enabling system software to map around these areas. Factory testing is performed under worst-case conditions. Because invalid blocks may be marginal, it may not be possible to recover the bad-block marking if the block is erased.

To simplify the system requirement and guard the data integration, GigaDevice SPI NAND provides assistant Management options as below.

Table 12-6. Bad Block Mark information (2Gb)

Description	Requirement
Minimum number of valid blocks (NVB)	2008
Total available blocks per die	2048
First spare area location	Byte 2048
Bad-block mark	00h(use non FFH to check)

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12.5 Block Protection

The block lock feature provides the ability to protect the entire device, or ranges of blocks, from the PROGRAM and ERASE operations. After power-up, the device is in the “locked” state, i.e., feature bits BP0, BP1and BP2 are set to 1, INV, CMP and BRWD are set to 0. To unlock all the blocks, or a range of blocks, the SET FEATURES command must be issued to alter the state of protection feature bits. When BRWD is set and WP# is LOW, none of the writable protection feature bits can be set. Also, when a PROGRAM/ERASE command is issued to a locked block, status bit OIP remains 0. When an ERASE command is issued to a locked block, the erase failure, status bit E_FAIL set to 1. When a PROGRAM command is issued to a locked block, program failure, status bit P_FAIL set to 1.

To enable the Write Protection (WP#), the Quad Enable bit (QE) of feature (B0[0]) must be set to 0.

Table 12-7. Block Lock Register Block Protect Bits (2Gb)

CMP	INV	BP2	BP1	BP0	Protect Row Address	Protect Rows
					2Gb	
x	x	0	0	0	NONE	None—all unlocked
0	0	0	0	1	1F800h ~ 1FFFFh	Upper 1/64 locked
0	0	0	1	0	1F000h ~ 1FFFFh	Upper 1/32 locked
0	0	0	1	1	1E000h ~ 1FFFFh	Upper 1/16 locked
0	0	1	0	0	1C000h ~ 1FFFFh	Upper 1/8 locked
0	0	1	0	1	18000h ~ 1FFFFh	Upper 1/4 locked
0	0	1	1	0	10000h ~ 1FFFFh	Upper 1/2 locked
x	x	1	1	1	0000h ~ 1FFFFh	All locked (default)
0	1	0	0	1	0000h ~7FFh	Lower 1/64 locked
0	1	0	1	0	0000h ~FFFh	Lower 1/32 locked
0	1	0	1	1	0000h ~ 1FFFh	Lower 1/16 locked
0	1	1	0	0	0000h ~ 3FFFh	Lower 1/8 locked
0	1	1	0	1	0000h ~ 7FFFh	Lower 1/4 locked
0	1	1	1	0	0000h ~ FFFFh	Lower 1/2 locked
1	0	0	0	1	0000h ~ 1F7FFh	Lower 63/64 locked
1	0	0	1	0	0000h ~ 1EFFFh	Lower31/32 locked
1	0	0	1	1	0000h ~ 1DFFFh	Lower 15/16 locked
1	0	1	0	0	0000h ~ 1BFFFh	Lower7/8 locked
1	0	1	0	1	0000h ~ 17FFFh	Lower3/4 locked
1	0	1	1	0	0000h ~ 003Fh	Block0
1	1	0	0	1	0800h ~ 1FFFFh	Upper 63/64 locked
1	1	0	1	0	1000h ~ 1FFFFh	Upper31/32 locked
1	1	0	1	1	2000h ~ 1FFFFh	Upper 15/16 locked
1	1	1	0	0	4000h ~ 1FFFFh	Upper7/8 locked
1	1	1	0	1	8000h ~ 1FFFFh	Upper3/4 locked
1	1	1	1	0	0000h ~ 003Fh	Block0

When WP# is not LOW, user can issue bellows commands to alter the protection states as want.

- Issue SET FEATURES register write (1FH)
- Issue the feature bit address (A0h) and the feature bits combination as the table

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12.6 Internal ECC

The device offers data corruption protection by offering optional internal ECC. READs and PROGRAMs with internal ECC can be enabled or disabled by setting feature bit ECC_EN. ECC is enabled by default when device powered on, so the default READ and PROGRAM commands operate with internal ECC in the “active” state when ECC enable.

To enable/disable ECC, perform the following command sequence:

- Issue the SET FEATURES command (1FH) to set the feature bit ECC_EN:
  1. To enable ECC, Set ECC_EN to 1.
  2. To disable ECC, Clear ECC_EN to 0.

During a PROGRAM operation, the device calculates an ECC code on the 2k page in the cache register, before the page is written to the NAND Flash array.

During a READ operation, the page data is read from the array to the cache register, where the ECC code is calculated and compared with the ECC code value read from the array. If error bits are detected (error bits≤4 bits), the error is corrected in the cache register. Only corrected data is output on the I/O bus. The ECC status bit indicates whether or not the error correction was successful. The ECC Protection table below shows the ECC protection scheme used throughout a page.

The ECC protection format as follow:

- User meta data I is not protected by internal ECC and User meta data II is protected by internal ECC.

Any data wrote to the ECC parity data area are ignored when ECC enabled.

Table 12-8. The Distribution of ECC Segment and Spare Area in a Page

Main Area(2KB)				Spare Area(128B)							
User data				User meta data(I+II)				ECC Parity Data			
Main0	Main1	Main2	Main3	Spare0	Spare1	Spare2	Spare3	Spare0	Spare1	Spare2	Spare3
(512B)	(512B)	(512B)	(512B)	(4B+12B)	(4B+12B)	(4B+12B)	(4B+12B)	(16B)	(16B)	(16B)	(16B)

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Table 12-9. ECC Protection and Spare Area

Min Byte Address	Max Byte Address	ECC Protected	Area	Description
000H	1FFH	Yes	Main 0	User data 0
200H	3FFH	Yes	Main 1	User data 1
400H	5FFH	Yes	Main 2	User data 2
600H	7FFH	Yes	Main 3	User data 3
800H	803H	No	Spare 0	User meta 0 data I
804H	80FH	Yes	Spare 0	User meta 0 data II
810H	813H	No	Spare 1	User meta 1 data I
814H	81FH	Yes	Spare 1	User meta 1 data II
820H	823H	No	Spare 2	User meta 2 data I
824H	82FH	Yes	Spare 2	User meta 2 data II
830H	833H	No	Spare 3	User meta 3 data I
834H	83FH	Yes	Spare 3	User meta 3 data II
840H	84FH	Yes	Spare 0	ECC Parity Data
850H	85FH	Yes	Spare 1	ECC Parity Data
860H	86FH	Yes	Spare 2	ECC Parity Data
870H	87FH	Yes	Spare 3	ECC Parity Data

Note

1. 800H is reserved for initial bad block mark, and please check the initial bad block mark with internal ECC off.
2. When Internal ECC is enabled, user cannot program the Address 840H~87FH but user can read the Address 840H~87FH.
3. When Internal ECC is disabled, the whole page area is open for user. And we recommend the user to provide external ECC protection.

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13 POWER ON TIMING

Figure13-1. Power on Timing Sequence

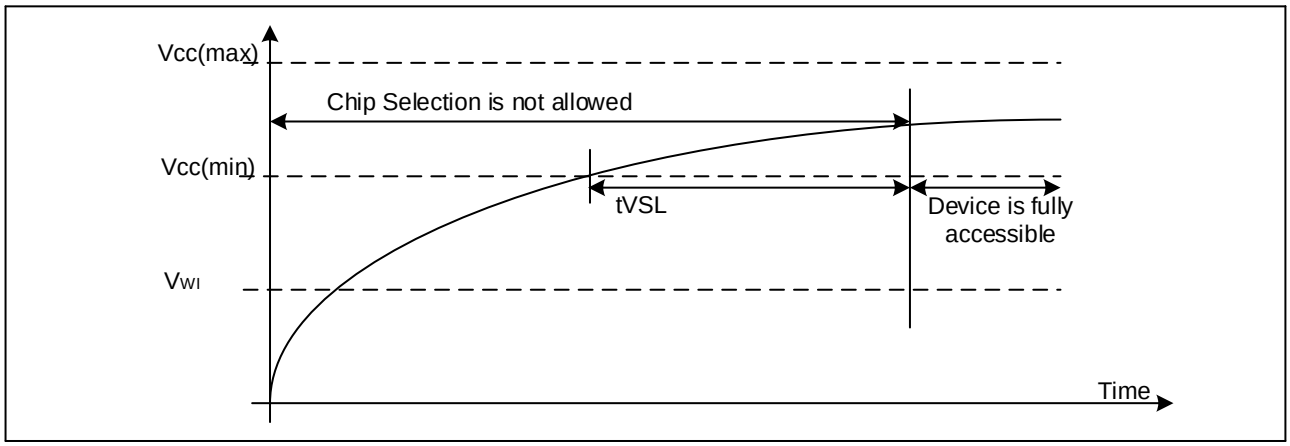


Table 13-1. Power-On Timing and Write Inhibit Threshold for 1.8V/3.3V

Symbol	Parameter		Min	Max	Unit
tVSL	VCC(min) To CS# Low		1		ms
VWI	Write Inhibit Voltage	1.8V		1.4	V
		3.3V		2.5	

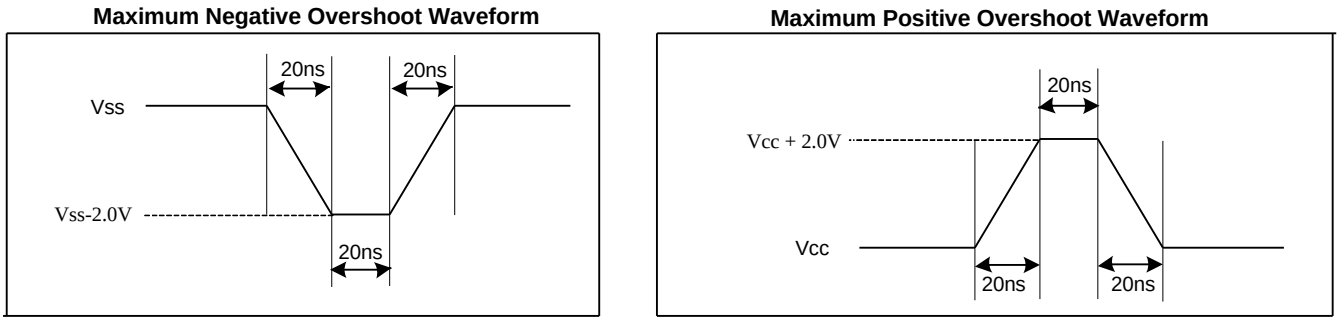
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14 ABSOLUTE MAXIMUM RATINGS

Table 14-1.Absolute Maximum Ratings

Parameter	Value	Unit
Ambient Operating Temperature	-40 to 105	℃
Storage Temperature	-65 to 150	℃
Applied Input / Output Voltage	-0.6 to VCC+0.4	V
VCC(3.3V)	-0.6 to 4.0	V
VCC(1.8V)	-0.6 to 2.5	V

Figure14-1. Input Test Waveform and Measurement Level

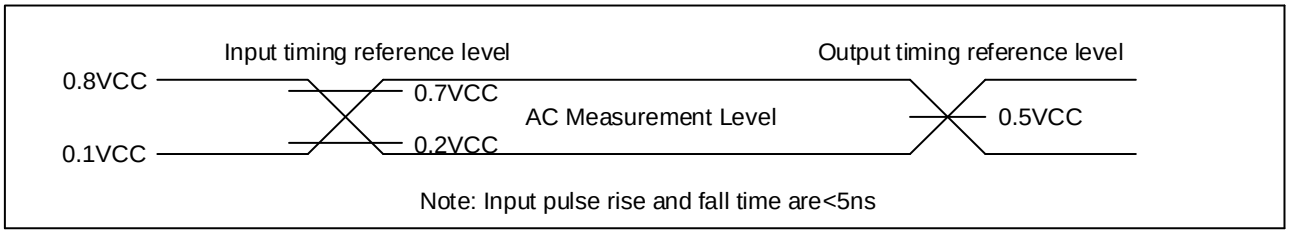


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15 CAPACITANCE MEASUREMENT CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
CIN	Input Capacitance			6	pF	VIN=0V
COUT	Output Capacitance			8	pF	VOUT=0V
C_L	Load Capacitance		30		pF	
	Input Rise And Fall time			5	ns	
	Input Pulse Voltage	0.1VCC to 0.8VCC			V	
	Input Timing Reference Voltage	0.2VCC to 0.7VCC			V	
	Output Timing Reference Voltage	0.5VCC			V	

Figure15-1. Input Test Waveform and Measurement Level



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16 DC CHARACTERISTIC

(T= -40℃~105℃, VCC=1.7~2.0V/2.7~3.6V)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit.
I_{LI}	Input Leakage Current				±2	μA
I_{LO}	Output Leakage Current				±2	μA
I_{CC1}	Standby Current	CS#=VCC, V_{IN}=VCC or VSS			50	μA
I_{CC2}	Operating Current (Read)	CLK=0.1VCC / 0.9VCC at 104MHz, Q=Open(*1,*2,*4 I/O)			30	mA
		CLK=0.1VCC / 0.9VCC at 80MHz, Q=Open(*1,*2,*4 I/O)			30	mA
I_{CC3}	Operating Current (Program)				30	mA
I_{CC4}	Operating Current (Erase)				30	mA
V_{IL}	Input Low Voltage		-0.5		0.2VCC	V
V_{IH}	Input High Voltage		0.8VCC		VCC+0.4	V
V_{OL}	Output Low Voltage	I_{OL} =1.6mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} =-100μA	VCC-0.2			V

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17 AC CHARACTERISTICS

(T= -40℃~105℃, VCC=1.7~2.0V/2.7~3.6V, C_L=30pF)

Symbol	Parameter	1.8V		3.3V		Unit.
		Min.	Max.	Min.	Max.	
FC1	Serial Clock Frequency		80		104	MHz
FC2*	Serial Clock Frequency for DTR		45		45	MHZ
tCH	Serial Clock High Time	4		4		ns
tCL	Serial Clock Low Time	4		4		ns
tCLCH	Serial Clock Rise Time (Slew Rate)	0.2		0.2		V/ns
tCHCL	Serial Clock Fall Time (Slew Rate)	0.2		0.2		V/ns
tCHSH	CS# Active Hold Time	5		5		ns
tSHCH	CS# Not Active Setup Time	5		5		ns
tSLCH	CS# Active Setup Time	7		5		ns
tCHSL	CS# Not Active Hold Time	5		5		ns
tSHSL/tCS	CS# High Time	20		20		ns
tSHQZ	Output Disable Time		20		20	ns
tCLQX	Output Hold Time	2		2		ns
tDVCH	Data In Setup Time	2		2		ns
tCHDX	Data In Hold Time	2		2		ns
tHLCH	Hold# Low Setup Time (relative to Clock)	5		5		ns
tHHCH	Hold# High Setup Time (relative to Clock)	5		5		ns
tCHHL	Hold# High Hold Time (relative to Clock)	5		5		ns
tCHHH	Hold# Low Hold Time (relative to Clock)	5		5		ns
tHLQZ	Hold# Low To High-Z Output		15		15	ns
tHHQX	Hold# High To Low-Z Output		15		15	ns
tCLQV	Clock Low To Output Valid		11		9	ns
tWHSL	WP# Setup Time Before CS# Low	20		20		ns
tSHWL	WP# Hold Time After CS# High	100		100		ns

Note:

Please contact GigaDevice when there is a need to use the EEh command for DTR.

The max clock rate for DTR depends on the tCLQV (clock to data output valid). Per datasheet, with output load capacitance of 30pf, the tCLQV is about 11ns. This will limit the max rate to 45Mhz.

However, in general, most of PCB designs have output loading much less than 30pf. Lower output loading will in turn shorten the tCLQV and result in higher max clock rate.

GigaDevice recommend customers measure the tCLQV and then set the clock rate to match the SPI host data sampling data setup time and hold time.

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18 PERFORMANCE AND TIMING

Symbol	Parameter	Min.	Typ.	Max.	Unit.
tRST	CS# High To Next Command After Reset(FFh)			500	us
tRD	Read From Array			25	us
tRD_ECC	Read From Array with ECC		45	60	us
tPROG	Page Programming Time		300	600	us
tPROG_ECC	Page Programming Time with ECC		400	600	us
tBERS	Block Erase Time		3	5	ms
tCBSYW	Cache busy time for Cache Program		5	tPROG	us
tCBSYW_ECC	Cache busy time for Cache Program with ECC		30	tPROG_ECC	us
tCBSYR	Cache busy time for Cache Read		5	tRD	us
tCBSYR_ECC	Cache busy time for Cache Read with ECC		30	tRD_ECC	us

Figure18-1. Serial Input Timing

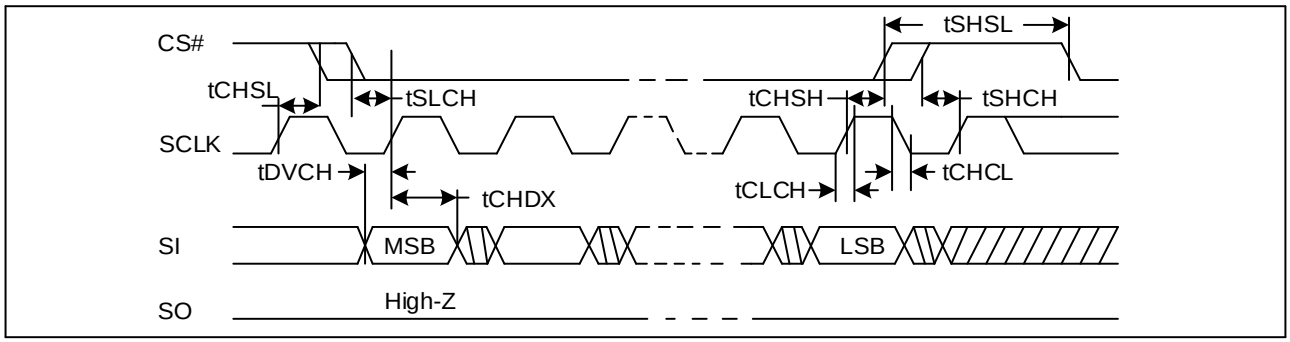
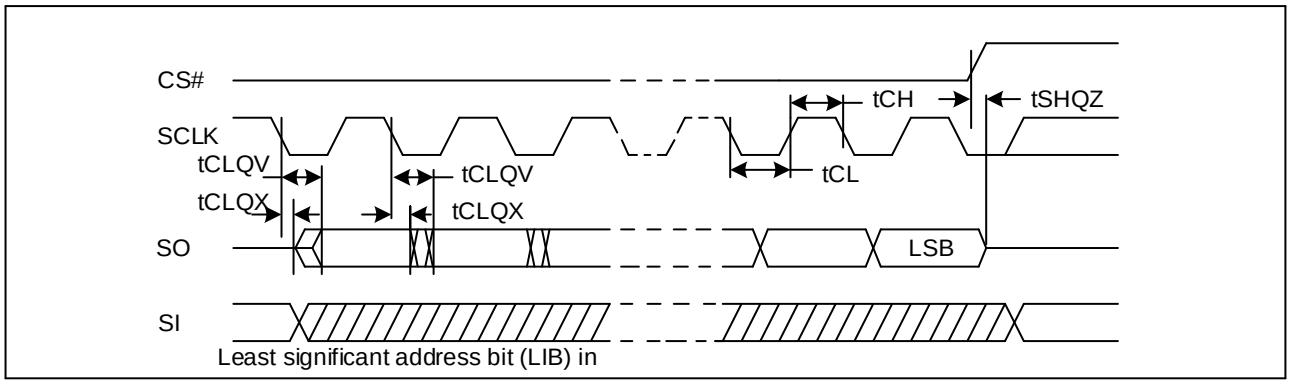
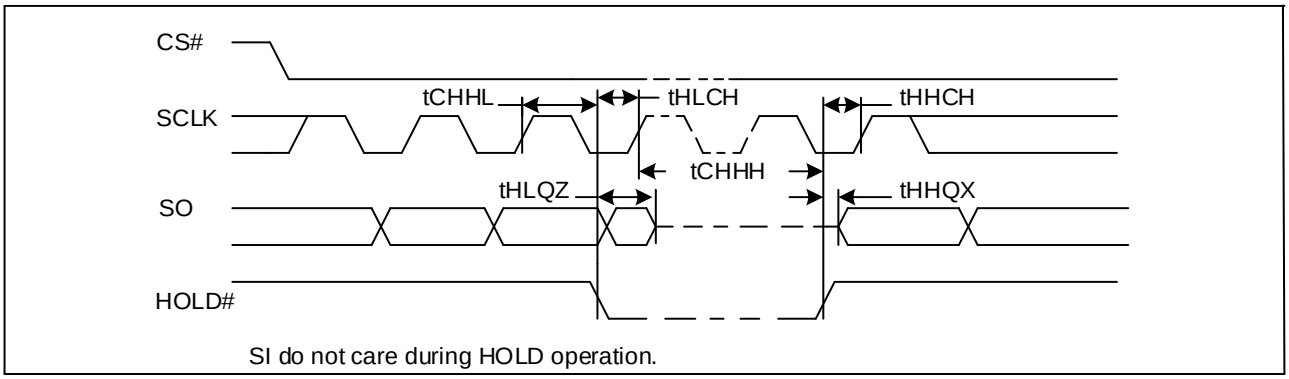


Figure18-2. Output Timing



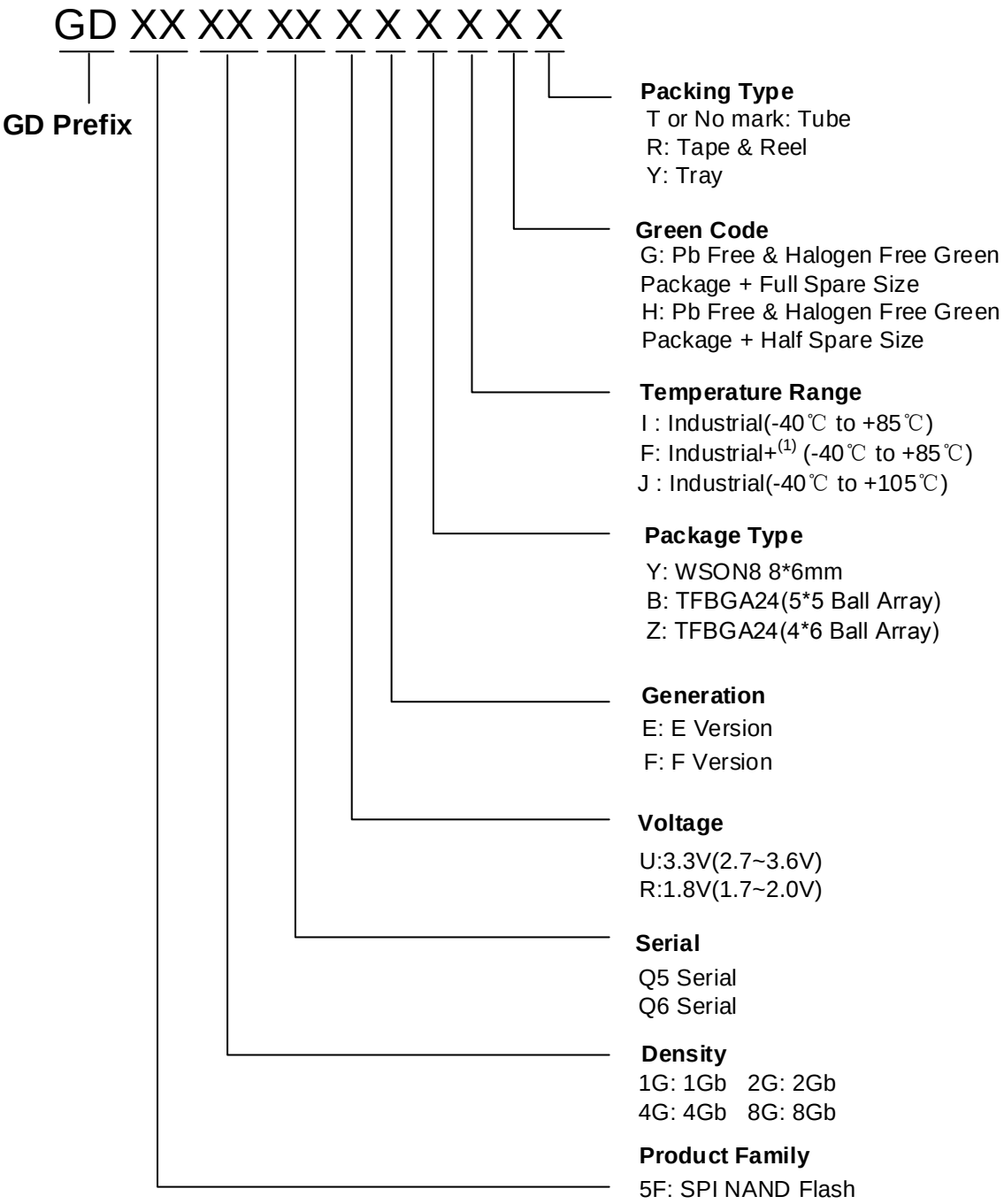
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Figure18-3. Hold Timing



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19 ORDERING INFORMATION

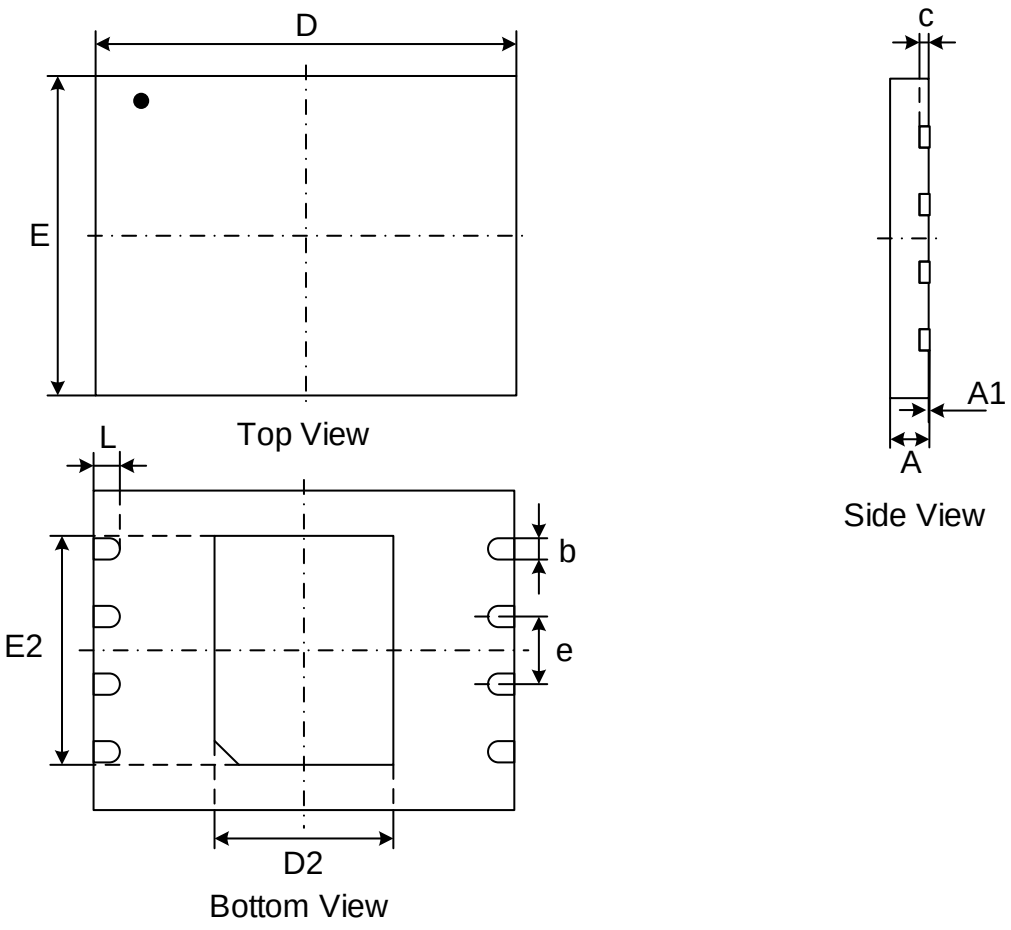


Note: (1) Industrial+: F grade has implemented additional test flows to ensure higher product quality than I grade.

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20 PACKAGE INFORMATION

Figure 20-1.WSON8 (8*6mm)

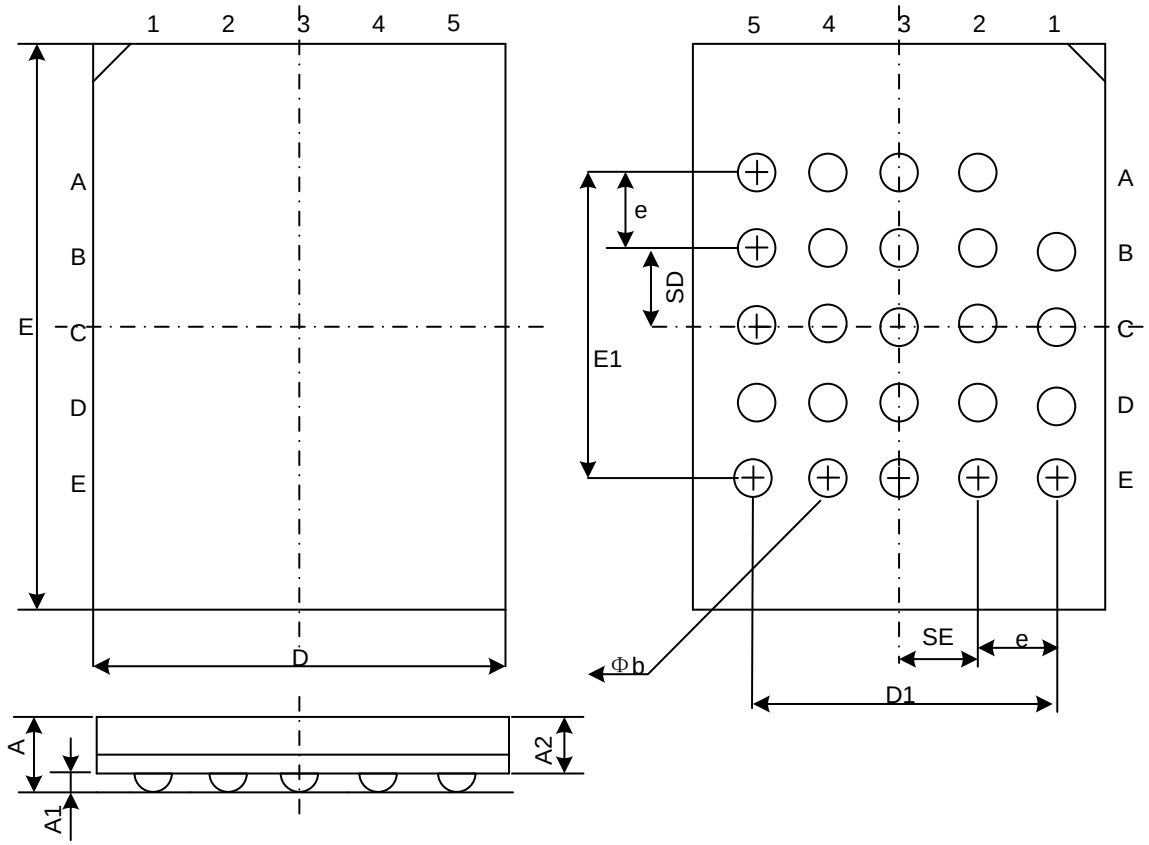


Dimensions

Symbol / Unit		A	A1	c	b	D	D2	E	E2	e	L
mm	Min	0.70	0.00	0.180	0.35	7.90	3.30	5.90	4.20	1.27	0.45
	Nom	0.75	0.02	0.203	0.40	8.00	3.40	6.00	4.30		0.50
	Max	0.80	0.05	0.250	0.45	8.10	3.50	6.10	4.40		0.55
Inch	Min	0.028	0	0.007	0.014	0.311	0.130	0.232	0.165	0.05	0.018
	Nom	0.030	0.001	0.008	0.016	0.315	0.134	0.236	0.169		0.020
	Max	0.032	0.002	0.010	0.018	0.319	0.138	0.240	0.173		0.022

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Figure 20-2.TFBGA-24BALL (5*5-1 ball array)



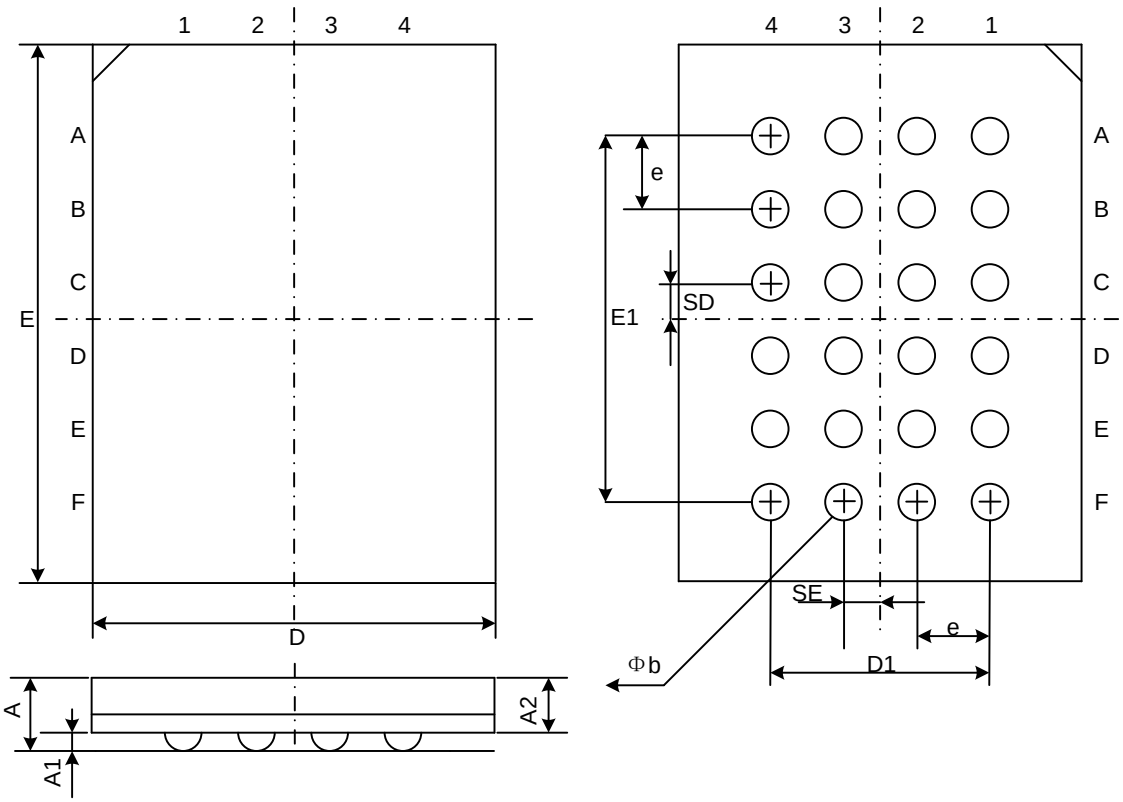
Dimensions

Symbol / Unit		A	A1	A2	b	D	D1	E	E1	e	SE	SD
mm	Min		0.25		0.35	5.90	4.00 BSC	7.90	4.00 BSC	1.00 BSC	1.00 TYP	1.00 TYP
	Nom		0.30	0.85	0.40	6.00		8.00				
	Max	1.20	0.35		0.45	6.10		8.10				
Inch	Min		0.010		0.014	0.232	0.157 BSC	0.311	0.157 BSC	0.039 BSC	0.039 TYP	0.039 TYP
	Nom		0.012	0.033	0.016	0.236		0.315				
	Max	0.047	0.014		0.018	0.240		0.319				

Note：Both package length and width do not include mold flash.

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Figure20-3. TFBGA-24BALL (4*6 ball array)



Dimensions

Symbol / Unit		A	A1	A2	b	D	D1	E	E1	e	SE	SD
mm	Min		0.25	0.70	0.35	5.90	3.00 BSC	7.90	5.00 BSC	1.00 BSC	0.50 TYP	0.50 TYP
	Nom		0.30	0.80	0.40	6.00		8.00				
	Max	1.20	0.35	0.85	0.45	6.10		8.10				
Inch	Min		0.010	0.028	0.014	0.232	0.118 BSC	0.311	0.197 BSC	0.039 BSC	0.020 TYP	0.020 TYP
	Nom		0.012	0.031	0.016	0.236		0.315				
	Max	0.047	0.014	0.034	0.018	0.240		0.319				

Note: Both the package length and width do not include the mold flash.

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21 REVISION HISTORY

Version No	Description	Page Number	Date
1.0	Initial Release		2019-08-01
1.1	Modify the 03H command description in Figure 8-6.Page Read to Cache Timing Diagram. Add Note in Figure 8-6 Page Read to Cache Timing Diagram about Read From Cache command. Modify the “P_FAIL” “E_FAIL” default value after power up from ‘Page 0’ to ‘0’.	25 25 51	2019-08-13
1.2	Add Note of EEH DTR command in 8.9 & 17 AC Characterisitcs.. Modify the descriptions of Industrial+ F grade in Ordering information. Modify the descriptions of FFH command. Add the Register bit value after reset command (FFH). Move Table 12.2 Register bit description to 12.1 Modify the Figure 3-1 Array Organization.	29/61 7/64 16/46 49/50 49 10	2019-08-27
1.3	Add tCBSYR_ECC and tCBSYW_ECC in 18 Performance and Timing.	62	2019-09-11
1.4	Update the tSLCH Value from 5ns to 7ns for 1.8V. Update the tVSL Value from 5ms to 1ms. Update the VWI Value from 1.7V to 1.4V.	61 57 57	2019-11-15
1.5	Update the tRD_ECC Max Value from 50us to 60us Add Industrial 105° product Modify the Storage Temperature to -65℃~150℃ Update the 8.12 Parameter Page Table Byte137/138 and recalculate the CRC Byte 254/255	62 7 58 35/36	2020-03-09

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