GigaDevice Semiconductor Inc.

GD32L233xx
Arm® Cortex®-M23 32-bit MCU

Datasheet

Revision 1.1

(Apr. 2022)

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1. General description

The GD32L233xx device belongs to the value line of GD32 MCU family. It is a new 32-bit general-purpose microcontroller based on the ARM® Cortex®-M23 core. The Cortex-M23 processor is an energy-efficient processor with a very low gate count. It is intended to be used for microcontroller and deeply embedded applications that require an area-optimized processor. The processor delivers high energy efficiency through a small but powerful instruction set and extensively optimized design, providing high-end processing hardware including a single-cycle multiplier and a 17-cycle divider.

The GD32L233xx device incorporates the ARM® Cortex®-M23 32-bit processor core operating at up to 64 MHz frequency with Flash accesses 0~3 wait states to obtain maximum efficiency. It provides up to 256 KB embedded Flash memory and up to 32 KB SRAM memory. An extensive range of enhanced I/Os and peripherals connected to two APB buses. The devices offer one 12-bit ADC and two comparators, up to four general 16-bit timers, two basic timers, and a 32-bit low power timer, as well as standard and advanced communication interfaces: up to two SPIs, three I2Cs, two USARTs, two UARTs, an I2S, and an LPUART.

The device operates from a 1.71 to 3.63 V power supply and available in -40 to +85 °C temperature range. Several power saving modes provide the flexibility for maximum optimization between wakeup latency and power consumption, an especially important consideration in low power applications.

The above features make the GD32L233xx devices suitable for a wide range of applications, especially in areas such as industrial control, motor drives, user interface, power monitor and alarm systems, consumer and handheld equipment, gaming and GPS, E-bike and so on.



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2. Device overview

2.1. Device information

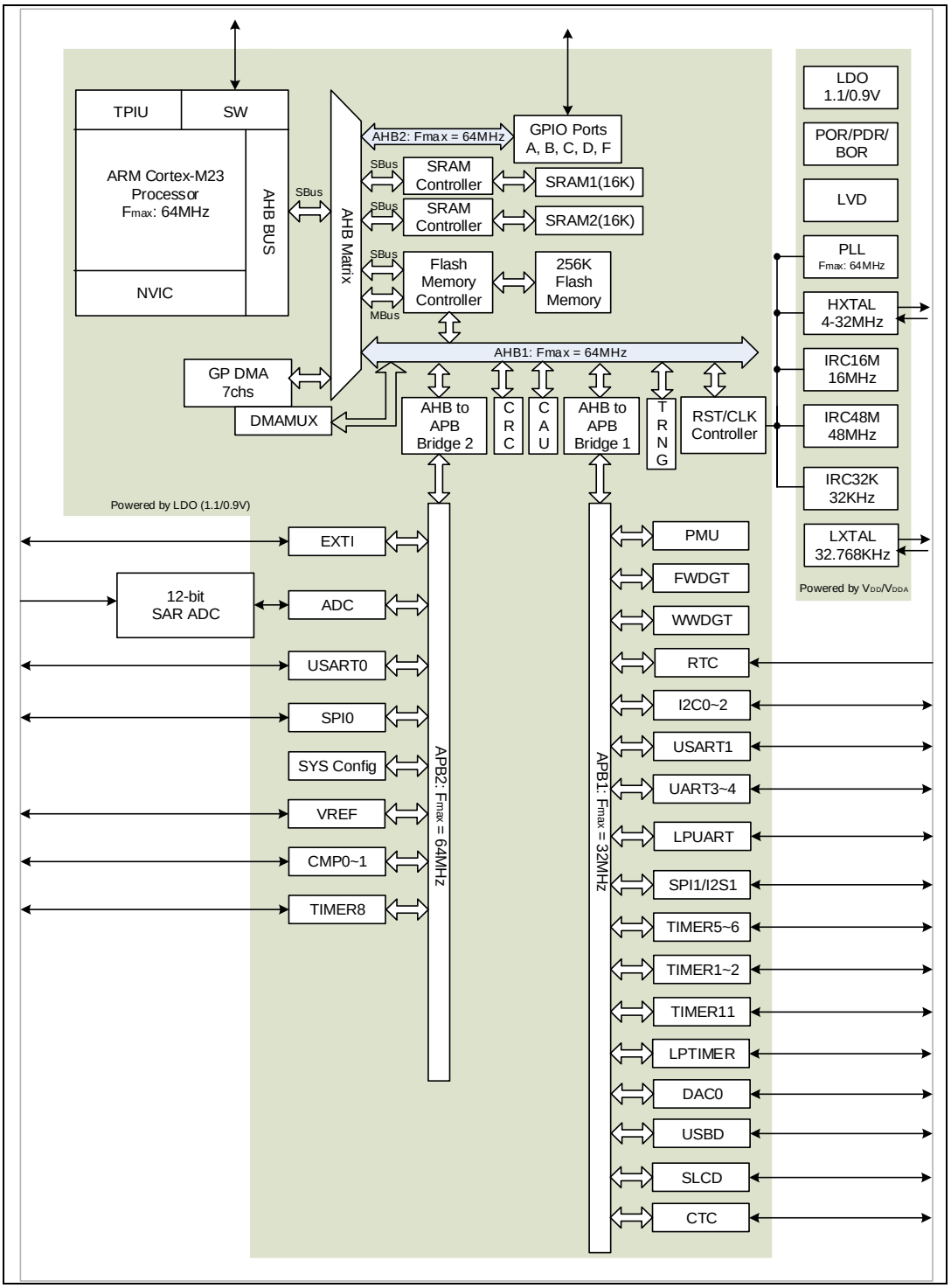
Table 2-1. GD32L233xx devices features and peripheral list

Part Number		GD32L233xx									
		K8Q6	KBQ6	K8T6	KBT6	C8T6	CBT6	CCT6	R8T6	RBT6	RCT6
FLASH (KB)		64	128	64	128	64	128	256	64	128	256
SRAM (KB)		16	24	16	24	16	24	32	16	24	32
Timers	General timer(16-bit)	3 (1, 2, 8)	3 (1, 2, 8)	3 (1, 2, 8)	3 (1, 2, 8)	3 (1, 2, 8)	4 (1, 2, 8, 11)	4 (1, 2, 8, 11)	3 (1, 2, 8)	4 (1, 2, 8, 11)	4 (1, 2, 8, 11)
	Low power timer(32-bit)	1	1	1	1	1	1	1	1	1	1
	SysTick	1	1	1	1	1	1	1	1	1	1
	Basic timer(16-bit)	2 (5, 6)	2 (5, 6)	2 (5, 6)	2 (5, 6)	2 (5, 6)	2 (5, 6)	2 (5, 6)	2 (5, 6)	2 (5, 6)	2 (5, 6)
	Watchdog	2	2	2	2	2	2	2	2	2	2
	RTC	1	1	1	1	1	1	1	1	1	1
Connectivity	UART	1 (3)	1 (3)	1 (3)	1 (3)	1 (3)	2 (3, 4)	2 (3, 4)	1 (3)	2 (3, 4)	2 (3, 4)
	USART	2 (0, 1)	2 (0, 1)	2 (0, 1)	2 (0, 1)	2 (0, 1)	2 (0, 1)	2 (0, 1)	2 (0, 1)	2 (0, 1)	2 (0, 1)
	LPUART	1	1	1	1	1	1	1	1	1	1
	I2C	2 (0-1)	2 (0-1)	2 (0-1)	2 (0-1)	2 (0-1)	2 (0-1)	2 (0-1)	3 (0-2)	3 (0-2)	3 (0-2)
	SPI/I2S	2/1 (0-1)/(1)	2/1 (0-1)/(1)	2/1 (0-1)/(1)	2/1 (0-1)/(1)	2/1 (0-1)/(1)	2/1 (0-1)/(1)	2/1 (0-1)/(1)	2/1 (0-1)/(1)	2/1 (0-1)/(1)	2/1 (0-1)/(1)
	USBD	1	1	1	1	1	1	1	1	1	1
GPIO		29	29	27	27	43	43	43	59	59	59
ADC	Units	1	1	1	1	1	1	1	1	1	1
	Channels (External)	10	10	10	10	10	10	10	16	16	16
	Channels (Internal)	4	4	4	4	4	4	4	4	4	4
DAC		1	1	1	1	1	1	1	1	1	1
CMP		2	2	2	2	2	2	2	2	2	2
SLCD		0	0	0	0	0	0	0	1	1	1
Package		QFN32		LQFP32		LQFP48			LQFP64		

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2.2. Block diagram

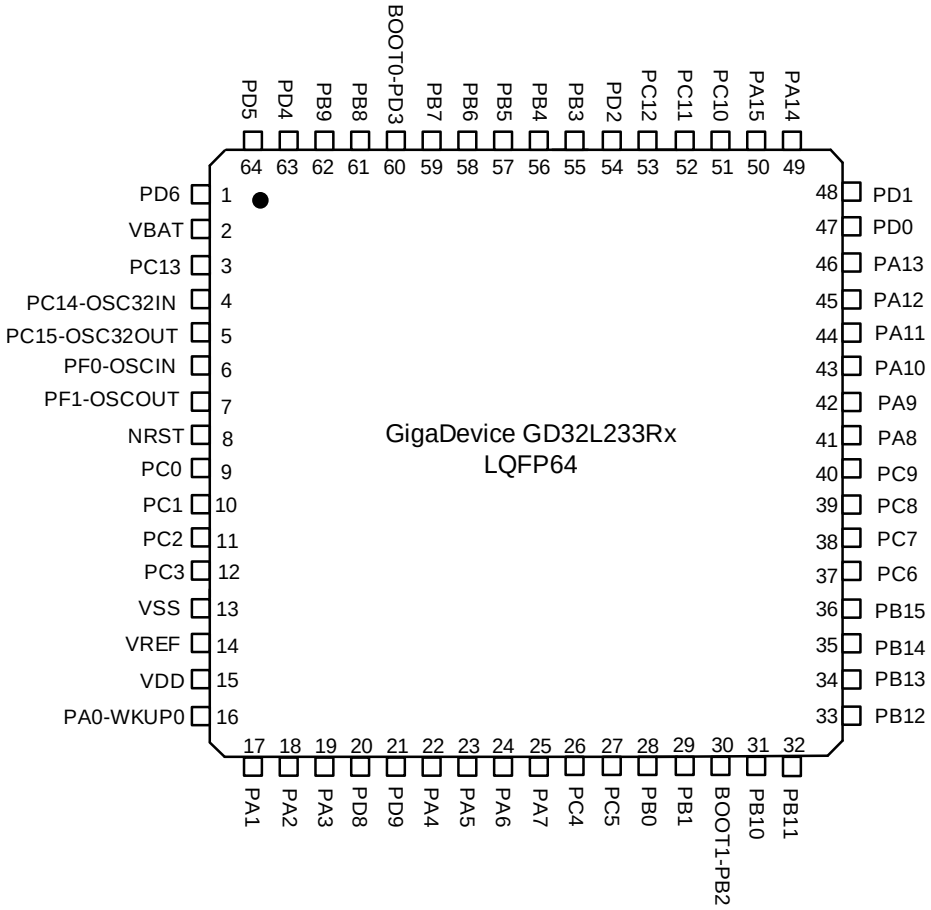
Figure 2-1. GD32L233xx block diagram



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2.3. Pinouts and pin assignment

Figure 2-2. GD32L233Rx LQFP64 pinouts



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Figure 2-3. GD32L233Cx LQFP48 pinouts

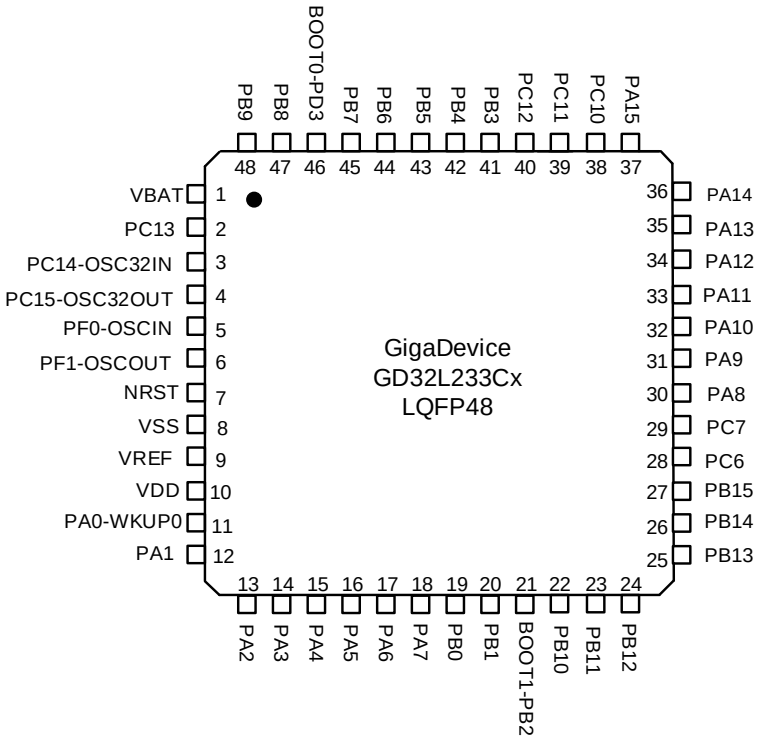
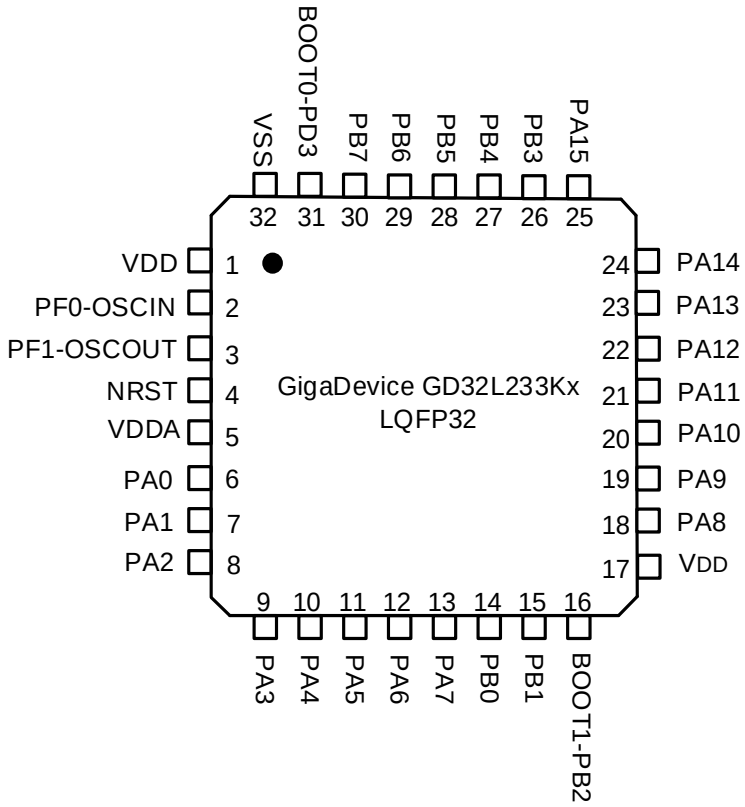
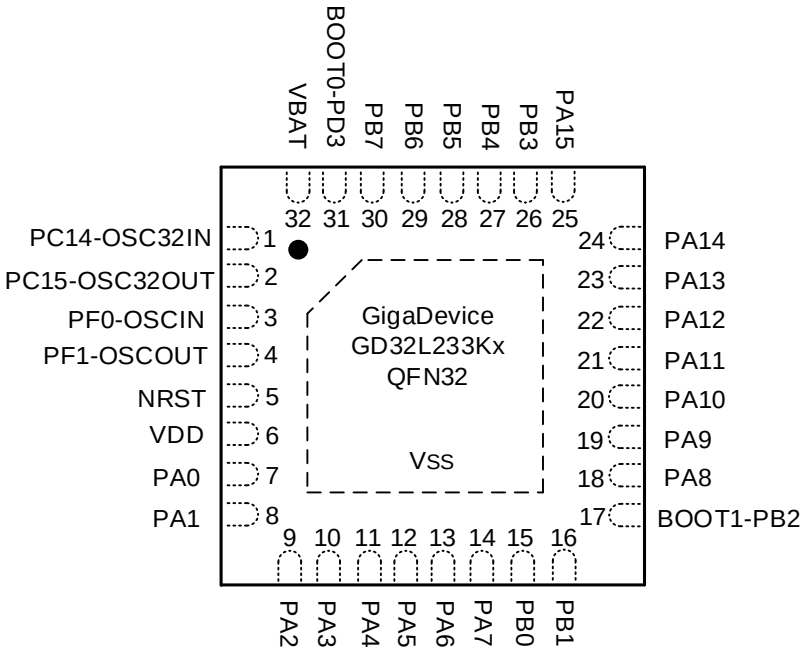


Figure 2-4. GD32L233Kx LQFP32 pinouts



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Figure 2-5. GD32L233Kx QFN32 pinouts



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2.4. Memory map

Table 2-2. GD32L233xx memory map

Pre-defined Regions	Bus	ADDRESS	Peripherals
		0xE000 0000 - 0xE00F FFFF	Cortex®-M23 internal peripherals
External Device		0xA000 0000 - 0xDFFF FFFF	Reserved
External RAM		0x60000000 - 0x9FFFFFFF	Reserved
Peripherals	AHB1	0x5006 1000 - 0x5FFF FFFF	Reserved
		0x5006 0C00 - 0x5006 0FFF	Reserved
		0x5006 0800 - 0x5006 0BFF	TRNG
		0x5006 0400 - 0x5006 07FF	Reserved
		0x5006 0000 - 0x5006 03FF	CAU
		0x5005 0400 - 0x5005 FFFF	Reserved
		0x5005 0000 - 0x5005 03FF	Reserved
		0x5004 0000 - 0x5004 FFFF	Reserved
		0x5000 0000 - 0x5003 FFFF	Reserved
	AHB2	0x4800 1800 - 0x4FFF FFFF	Reserved
		0x4800 1400 - 0x4800 17FF	GPIOF
		0x4800 1000 - 0x4800 13FF	Reserved
		0x4800 0C00 - 0x4800 0FFF	GPIOD
		0x4800 0800 - 0x4800 0BFF	GPIOC
		0x4800 0400 - 0x4800 07FF	GPIOB
		0x4800 0000 - 0x4800 03FF	GPIOA
	AHB1	0x4002 4400 - 0x47FF FFFF	Reserved
		0x4002 4000 - 0x4002 43FF	Reserved
		0x4002 3400 - 0x4002 3FFF	Reserved
		0x4002 3000 - 0x4002 33FF	CRC
		0x4002 2400 - 0x4002 2FFF	Reserved
		0x4002 2000 - 0x4002 23FF	FMC
		0x4002 1400 - 0x4002 1FFF	Reserved
		0x4002 1000 - 0x4002 13FF	RCU
		0x4002 0C00 - 0x4002 0FFF	Reserved
		0x4002 0800 - 0x4002 0BFF	DMAMUX
		0x4002 0400 - 0x4002 07FF	Reserved
		0x4002 0000 - 0x4002 03FF	DMA
	APB2	0x4001 8000 - 0x4001 FFFF	Reserved
		0x4001 7C00 - 0x4001 7FFF	CMP
		0x4001 5C00 - 0x4001 7BFF	Reserved
		0x4001 5800 - 0x4001 5BFF	DBG
		0x4001 5000 - 0x4001 57FF	Reserved
		0x4001 4C00 - 0x4001 4FFF	TIMER8

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Pre-defined Regions	Bus	ADDRESS	Peripherals
		0x4001 3C00 - 0x4001 4BFF	Reserved
		0x4001 3800 - 0x4001 3BFF	USART0
		0x4001 3400 - 0x4001 37FF	Reserved
		0x4001 3000 - 0x4001 33FF	SPI0
		0x4001 2C00 - 0x4001 2FFF	Reserved
		0x4001 2800 - 0x4001 2BFF	Reserved
		0x4001 2400 - 0x4001 27FF	ADC
		0x4001 0800 - 0x4001 23FF	Reserved
		0x4001 0400 - 0x4001 07FF	EXTI
		0x4001 0000 - 0x4001 03FF	SYSCFG + VREF
	APB1	0x4000 CC00 - 0x4000 FFFF	Reserved
		0x4000 C800 - 0x4000 CBFF	CTC
		0x4000 C400 - 0x4000 C7FF	Reserved
		0x4000 C000 - 0x4000 C3FF	I2C2
		0x4000 9800 - 0x4000 BFFF	Reserved
		0x4000 9400 - 0x4000 97FF	LPTIMER
		0x4000 8400 - 0x4000 93FF	Reserved
		0x4000 8000 - 0x4000 83FF	LPUART
		0x4000 7C00 - 0x4000 7FFF	Reserved
		0x4000 7800 - 0x4000 7BFF	Reserved
		0x4000 7400 - 0x4000 77FF	DAC0
		0x4000 7000 - 0x4000 73FF	PMU
		0x4000 6400 - 0x4000 6FFF	Reserved
		0x4000 6000 - 0x4000 63FF	USBD RAM (512 bytes)
		0x4000 5C00 - 0x4000 5FFF	USBD
		0x4000 5800 - 0x4000 5BFF	I2C1
		0x4000 5400 - 0x4000 57FF	I2C0
		0x4000 5000 - 0x4000 53FF	UART4
		0x4000 4C00 - 0x4000 4FFF	UART3
		0x4000 4800 - 0x4000 4BFF	Reserved
		0x4000 4400 - 0x4000 47FF	USART1
		0x4000 4000 - 0x4000 43FF	Reserved
		0x4000 3C00 - 0x4000 3FFF	Reserved
		0x4000 3800 - 0x4000 3BFF	SPI1/I2S1
		0x4000 3400 - 0x4000 37FF	Reserved
		0x4000 3000 - 0x4000 33FF	FWDGT
		0x4000 2C00 - 0x4000 2FFF	WWDGT
		0x4000 2800 - 0x4000 2BFF	RTC
		0x4000 2400 - 0x4000 27FF	SLCD
		0x4000 2000 - 0x4000 23FF	Reserved

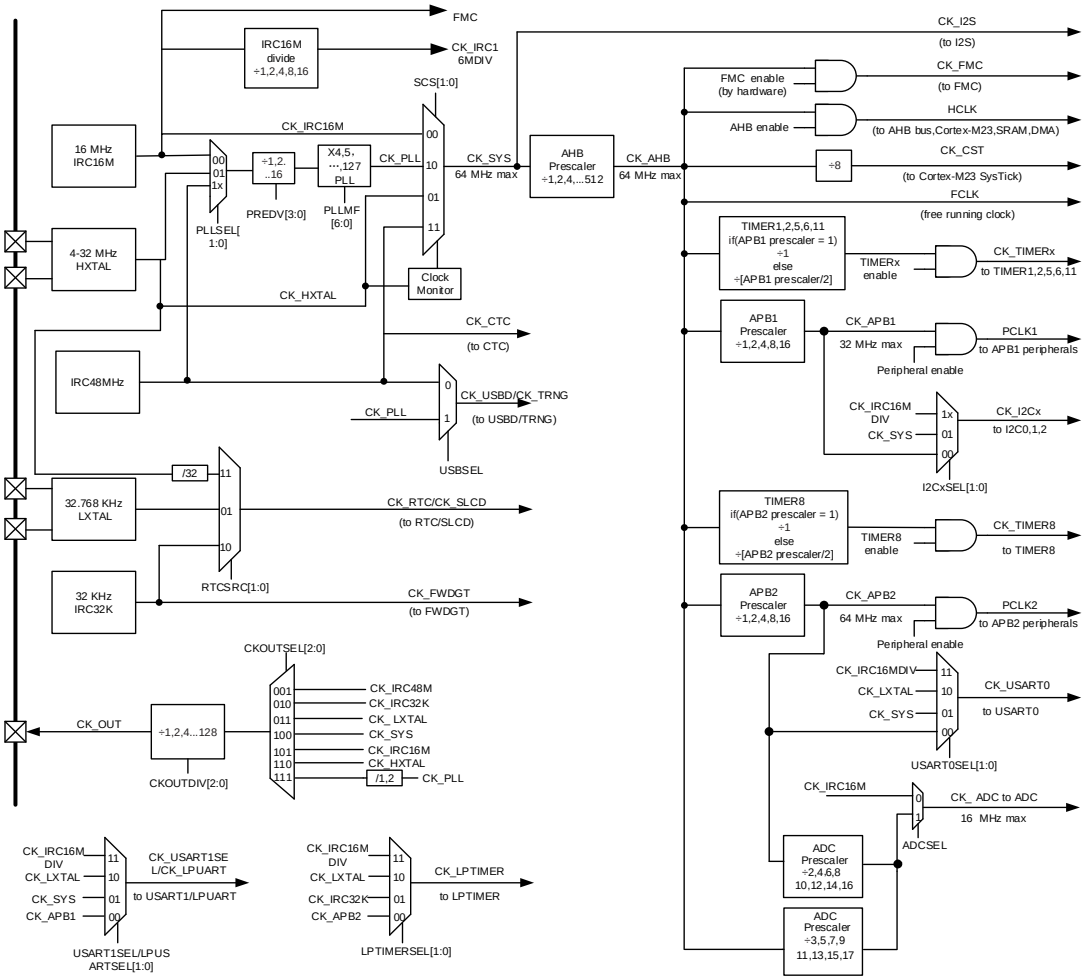
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Pre-defined Regions	Bus	ADDRESS	Peripherals
		0x4000 1C00 - 0x4000 1FFF	Reserved
		0x4000 1800 - 0x4000 1BFF	TIMER11
		0x4000 1400 - 0x4000 17FF	TIMER6
		0x4000 1000 - 0x4000 13FF	TIMER5
		0x4000 0800 - 0x4000 0FFF	Reserved
		0x4000 0400 - 0x4000 07FF	TIMER2
		0x4000 0000 - 0x4000 03FF	TIMER1
		0x4000 0000 - 0x4000 03FF	Reserved
SRAM		0x2000 8000 - 0x3FFF FFFF	Reserved
		0x2000 5000 - 0x2000 7FFF	SRAM1(16KB)
		0x2000 4000 - 0x2000 4FFF	
		0x2000 2000 - 0x2000 3FFF	SRAM0(16KB)
		0x2000 1000 - 0x2000 1FFF	
		0x2000 0000 - 0x2000 0FFF	
Code		0x1FFF F810 - 0x1FFF FFFF	Reserved
		0x1FFF F800 - 0x1FFF F80F	Option bytes(16B)
		0x1FFF D000- 0x1FFF F7FF	System memory(10KB)
		0x1FFF 7200 - 0x1FFF CFFF	Reserved
		0x1FFF 7000 - 0x1FFF 71FF	OTP(512B)
		0x1000 0000 - 0x1FFF 6FFF	Reserved
		0x0804 0000 - 0x0FFF FFFF	Reserved
		0x0802 0000 - 0x0803 FFFF	Main Flash memory(256KB)
		0x0801 0000 - 0x0801 FFFF	
		0x0800 0000 - 0x0800 FFFF	
		0x0001 0000 - 0x07FF FFFF	Reserved
		0x0000 0000 - 0x0000 FFFF	Aliased to Flash or system memory

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2.5. Clock tree

Figure 2-6. GD32L233xx clock tree



Note:

The TIMERs are clocked by the clock divided from CK_APB2 and CK_APB1. The frequency of TIMERs clock is equal to CK_APBx (APB prescaler is 1), twice the CK_APBx (APB prescaler is not 1).

Legend:

HXTAL: High speed crystal oscillator

LXTAL: Low speed crystal oscillator

IRC16M: Internal 16M RC oscillator

IRC48M: Internal 48M RC oscillator

IRC32K: Internal 32K RC oscillator

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2.6. Pin definitions

2.6.1. GD32L233Rx LQFP64 pin definitions

Table 2-3. GD32L233Rx LQFP64 pin definitions

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
PD6	1	I/O	5VT	Default: PD6 Alternate: USART1_RX, EVENTOUT, SPI0_MOSI, LPTIMER_IN1 Additional: VSLCD
VBAT	2	P		Default: VBAT
PC13	3	I/O		Default: PC13 Alternate: EVENTOUT Additional: RTC_TAMP0, RTC_OUT, RTC_TS, WKUP1
PC14-OSC32IN	4	I/O		Default: PC14 Alternate: EVENTOUT Additional: OSC32IN
PC15-OSC32OUT	5	I/O		Default: PC15 Alternate: EVENTOUT Additional: OSC32OUT
PF0-OSCIN	6	I/O		Default: OSCIN Alternate: EVENTOUT, SPI1_NSS, I2S1_WS Additional: PF0
PF1-OSCOUT	7	I/O		Default: OSCOUT Alternate: EVENTOUT, SPI1_SCK, I2S1_CK Additional: PF1
NRST	8	I/O		Default: NRST
PC0	9	I/O		Default: PC0 Alternate: SEG18, I2C2_SCL, LPUART_RX, LPTIMER_IN0, EVENTOUT Additional: ADC_IN10
PC1	10	I/O		Default: PC1 Alternate: SEG19, I2C2_SDA, LPUART_TX, LPTIMER_OUT, EVENTOUT Additional: ADC_IN11
PC2	11	I/O		Default: PC2 Alternate: SPI1_MISO, I2S1_MCK, SEG20, EVENTOUT, LPTIMER_IN1 Additional: ADC_IN12
PC3	12	I/O		Default: PC3 Alternate: SPI1_MOSI, I2S1_SD, SEG21, LPTIMER

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Pin Name	Pins	Pin Type[1]	I/O Level[2]	Functions description
				_ETI0, EVENTOUT Additional: ADC_IN13
VSS	13	P		Default: VSS
VREF	14	P		Default: VREF
VDD	15	P		Default: VDD
PA0	16	I/O		Default: PA0 Alternate: USART1_CTS, TIMER1_CH0_ETI, CMP0_OUT, EVENTOUT, UART3_TX Additional: WKUP0, ADC_IN0, RTC_TAMP1, CMP0_IM4
PA1	17	I/O		Default: PA1 Alternate: USART1_RTS, TIMER1_CH1, I2C0_SMBA, SPI0_SCK, SEG0, EVENTOUT, UART3_RX Additional: ADC_IN1, CMP0_IP
PA2	18	I/O		Default: PA2 Alternate: USART1_TX, TIMER8_CH0, TIMER1_CH2, SPI0_IO2, CMP1_OUT, LPUART_TX, SEG1, EVENTOUT Additional: ADC_IN2, CMP1_IM4, RTC_TAMP2, WKUP2
PA3	19	I/O		Default: PA3 Alternate: USART1_RX, TIMER8_CH1, TIMER1_CH3, SPI0_IO3, LPUART_RX, SEG2, EVENTOUT Additional: ADC_IN3, CMP1_IP0
PD8	20	I/O	5VT	Default: PD8 Alternate: LPTIMER_ETI0, LPUART_TX, EVENTOUT, SEG30
PD9	21	I/O	5VT	Default: PD9 Alternate: LPTIMER_IN0, LPUART_RX, EVENTOUT, SEG31
PA4	22	I/O		Default: PA4 Alternate: SPI0_NSS, USART1_CK, SPI1_NSS, I2S1_WS, LPTIMER_OUT, EVENTOUT Additional: ADC_IN4, DAC_OUT
PA5	23	I/O		Default: PA5 Alternate: SPI0_SCK, TIMER1_CH0_ETI, LPTIMER_ETI0, EVENTOUT Additional: ADC_IN5
PA6	24	I/O		Default: PA6 Alternate: SPI0_MISO, TIMER2_CH0, LPTIMER_IN0, CMP0_OUT, LPUART_CTS, SEG3, EVENTOUT Additional: ADC_IN6
PA7	25	I/O		Default: PA7

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Pin Name	Pins	Pin Type[1]	I/O Level[2]	Functions description
				Alternate: SPI0_MOSI, TIMER2_CH1, LPTIMER_ETI0, I2C2_SCL, CMP1_OUT, SEG4, EVENTOUT Additional: ADC_IN7
PC4	26	I/O		Default: PC4 Alternate: LPUART_TX, USART0_TX, TIMER1_CH0_ETI, SEG22, EVENTOUT Additional: ADC_IN14
PC5	27	I/O		Default: PC5 Alternate: LPUART_RX, USART0_RX, TIMER1_CH1, SEG23, EVENTOUT Additional: ADC_IN15
PB0	28	I/O		Default: PB0 Alternate: TIMER2_CH2, LPTIMER_OUT, SPI0_NSS, CMP0_OUT, SEG5, EVENTOUT Additional: ADC_IN8, VREF_OUT
PB1	29	I/O		Default: PB1 Alternate: TIMER2_CH3, LPUART_RTS, LPTIMER_IN0, SEG6, EVENTOUT Additional: ADC_IN9, VREF_OUT
BOOT1-PB2	30	I/O	5VT	Default: BOOT1 Alternate: LPTIMER_OUT, EVENTOUT, RTC_OUT Additional: PB2, WKUP3
PB10	31	I/O	5VT	Default: PB10 Alternate: SPI1_SCK, I2S1_CK, LPUART_TX, I2C1_SCL, LPUART_RX, TIMER1_CH2, CMP0_OUT, SEG10, EVENTOUT
PB11	32	I/O	5VT	Default: PB11 Alternate: LPUART_RX, I2C1_SDA, LPUART_TX, TIMER1_CH3, CMP1_OUT, SEG11, EVENTOUT
PB12	33	I/O	5VT	Default: PB12 Alternate: SPI1_NSS, I2S1_WS, I2C1_SMBA, LPUART_RTS, SEG12, EVENTOUT
PB13	34	I/O	5VT	Default: PB13 Alternate: CK_OUT, SPI1_SCK, I2S1_CK, LPUART_CTS, I2C1_SCL, SEG13, EVENTOUT
PB14	35	I/O	5VT	Default: PB14 Alternate: SPI1_MISO, LPUART_RTS, I2C1_SDA, TIMER11_CH0[3], SEG14, EVENTOUT, RTC_OUT
PB15	36	I/O	5VT	Default: PB15 Alternate: SPI1_MOSI, I2S1_SD, TIMER11_CH1[3], SEG15, EVENTOUT Additional: RTC_REFIN
PC6	37	I/O	5VT	Default: PC6

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Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
				Alternate: I2S1_MCK, TIMER2_CH0, SEG24, EVENTOUT Additional: WKUP4
PC7	38	I/O	5VT	Default: PC7 Alternate: TIMER2_CH1, SEG25, EVENTOUT
PC8	39	I/O	5VT	Default: PC8 Alternate: TIMER2_CH2, I2C2_SDA, SEG26, EVENTOUT
PC9	40	I/O	5VT	Default: PC9 Alternate: TIMER2_CH3, I2C2_SCL, SEG27, EVENTOUT
PA8	41	I/O	5VT	Default: PA8 Alternate: USART0_CK, CK_OUT, LPTIMER_OUT, I2C2_SMBA, COM0, EVENTOUT, CTC_SYNC Additional: VCORE
PA9	42	I/O	5VT	Default: PA9 Alternate: CK_OUT, USART0_TX, I2C0_SCL, COM1, EVENTOUT, LPTIMER_IN1
PA10	43	I/O	5VT	Default: PA10 Alternate: USART0_RX, I2C0_SDA, COM2, EVENTOUT
PA11	44	I/O	5VT	Default: PA11 Alternate: CMP0_OUT, USART0_CTS, SPI0_MISO, EVENTOUT Additional: USBDM
PA12	45	I/O	5VT	Default: PA12 Alternate: CMP1_OUT, USART0_RTS, SPI0_MOSI, EVENTOUT Additional: USBDP
PA13	46	I/O	5VT	Default: SWDIO Alternate: LPUART_RX, I2C0_SCL, USART0_TX, SPI0_IO2, SPI0_NSS, EVENTOUT Additional: PA13
PD0	47	I/O	5VT	Default: PD0 Alternate: SPI1_NSS, I2S1_WS, LPTIMER_OUT, USART1_CK, EVENTOUT, CTC_SYNC
PD1	48	I/O	5VT	Default: PD1 Alternate: SPI1_SCK, I2S1_CK, SPI1_MISO, USART1_CTS, EVENTOUT
PA14	49	I/O	5VT	Default: SWCLK Alternate: LPUART_TX, USART1_TX, I2C0_SDA, USART0_RX, SPI0_IO3, SPI1_NSS, I2S1_WS, EVENTOUT

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Pin Name	Pins	Pin Type[1]	I/O Level[2]	Functions description
				Additional: PA14
PA15	50	I/O	5VT	Default: PA15 Alternate: SPI1_NSS, I2S1_WS, TIMER1_CH0_ETI, SPI0_NSS, USART1_RX, SEG17, EVENTOUT
PC10	51	I/O	5VT	Default: PC10 Alternate: UART3_TX, LPUART_TX, SPI1_SCK, I2S1_CK, SEG28, COM4, EVENTOUT
PC11	52	I/O	5VT	Default: PC11 Alternate: UART3_RX, LPUART_RX, SPI1_MISO, SEG29, COM5, EVENTOUT
PC12	53	I/O	5VT	Default: PC12 Alternate: UART4_TX[3], SPI1_MOSI, I2S1_SD, SEG30, COM6, EVENTOUT
PD2	54	I/O	5VT	Default: PD2 Alternate: LPUART_RTS, TIMER2_ETI, UART4_RX[3], SEG31, COM7, EVENTOUT
PB3	55	I/O	5VT	Default: PB3 Alternate:UART4_TX[3], SPI1_SCK, I2S1_CK, TIMER1_CH1, SPI0_SCK, USART0_RTS, SEG7, EVENTOUT, LPTIMER_IN1 Additional: CMP1_IM6
PB4	56	I/O	5VT	Default: PB4 Alternate: UART4_RX[3], SPI1_MISO, TIMER2_CH0, SPI0_MISO, USART0_CTS, SEG8, EVENTOUT Additional: CMP1_IP1
PB5	57	I/O		Default: PB5 Alternate: LPTIMER_IN0, I2C0_SMBA, SPI1_MOSI, I2S1_SD, TIMER2_CH1, SPI0_MOSI, USART0_CK, CMP1_OUT, SEG9, EVENTOUT Additional: CMP1_IP2
PB6	58	I/O	5VT	Default: PB6 Alternate: LPTIMER_ETI0, I2C1_SCL, I2C0_SCL, USART0_TX, SPI0_IO2, EVENTOUT Additional: CMP1_IP3
PB7	59	I/O	5VT	Default: PB7 Alternate: I2C1_SDA, I2C0_SDA, USART0_RX, SPI0_IO3, EVENTOUT Additional: CMP1_IP4
BOOT0-PD3	60	I/O		Default: BOOT0 Alternate: USART1_CTS, SPI1_MISO, I2S1_MCK Additional: PD3
PB8	61	I/O	5VT	Default: PB8

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Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
				Alternate: I2C1_SCL, I2C0_SCL, CMP0_OUT, SEG16, EVENTOUT
PB9	62	I/O	5VT	Default: PB9 Alternate: I2C1_SDA, SPI1_NSS, I2S1_WS, I2C0_SDA, CMP1_OUT, COM3, EVENTOUT
PD4	63	I/O	5VT	Default: PD4 Alternate: SPI1_MOSI, I2S1_SD, USART1_RTS, EVENTOUT, SEG28
PD5	64	I/O	5VT	Default: PD5 Alternate: USART1_TX, EVENTOUT, SPI0_MISO, SEG29

Note:

(1) Type: I = input, O = output, A = analog, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

(3) Functions are available on GD32L233RB/C devices only.

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2.6.2. GD32L233Cx LQFP48 pin definitions

Table 2-4. GD32L233Cx LQFP48 pin definitions

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
VBAT	1	P		Default: VBAT
PC13	2	I/O		Default: PC13 Alternate: EVENTOUT Additional: RTC_TAMP0, RTC_OUT, RTC_TS, WKUP1
PC14-OSC32IN	3	I/O		Default: PC14 Alternate: EVENTOUT Additional: OSC32IN
PC15-OSC32OUT	4	I/O		Default: PC15 Alternate: EVENTOUT Additional: OSC32OUT
PF0-OSCIN	5	I/O		Default: OSCIN Alternate: EVENTOUT, SPI1_NSS, I2S1_WS Additional: PF0
PF1-OSCOUT	6	I/O		Default: OSCOUT Alternate: EVENTOUT, SPI1_SCK, I2S1_CK Additional: PF1
NRST	7	I/O		Default: NRST
VSS	8	P		Default: VSS
VREF	9	P		Default: VREF
VDD	10	P		Default: VDD
PA0	11	I/O		Default: PA0 Alternate: USART1_CTS, TIMER1_CH0_ETI, CMP0_OUT, EVENTOUT, UART3_TX Additional: WKUP0, ADC_IN0, RTC_TAMP1, CMP0_IM4
PA1	12	I/O		Default: PA1 Alternate: USART1_RTS, TIMER1_CH1, I2C0_SMBA, SPI0_SCK, EVENTOUT, UART3_RX Additional: ADC_IN1, CMP0_IP
PA2	13	I/O		Default: PA2 Alternate: USART1_TX, TIMER8_CH0, TIMER1_CH2, SPI0_IO2, CMP1_OUT, LPUART_TX, EVENTOUT Additional: ADC_IN2, CMP1_IM4, RTC_TAMP2, WKUP2
PA3	14	I/O		Default: PA3 Alternate: USART1_RX, TIMER8_CH1, TIMER1_CH3, SPI0_IO3, LPUART_RX, EVENTOUT

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Pin Name	Pins	Pin Type[1]	I/O Level[2]	Functions description
				Additional: ADC_IN3, CMP1_IP0
PA4	15	I/O		Default: PA4 Alternate: SPI0_NSS, USART1_CK, SPI1_NSS, I2S1_WS, LPTIMER_OUT, EVENTOUT Additional: ADC_IN4, DAC_OUT
PA5	16	I/O		Default: PA5 Alternate: SPI0_SCK, TIMER1_CH0_ETI, LPTIMER_ETI0, EVENTOUT Additional: ADC_IN5
PA6	17	I/O		Default: PA6 Alternate: SPI0_MISO, TIMER2_CH0, LPTIMER_IN0, CMP0_OUT, LPUART_CTS, EVENTOUT Additional: ADC_IN6
PA7	18	I/O		Default: PA7 Alternate: SPI0_MOSI, TIMER2_CH1, LPTIMER_ETI0, CMP1_OUT, EVENTOUT Additional: ADC_IN7
PB0	19	I/O		Default: PB0 Alternate: TIMER2_CH2, LPTIMER_OUT, SPI0_NSS, CMP0_OUT, EVENTOUT Additional: ADC_IN8, VREF_OUT
PB1	20	I/O		Default: PB1 Alternate: TIMER2_CH3, LPUART_RTS, LPTIMER_IN0, EVENTOUT Additional: ADC_IN9, VREF_OUT
BOOT1-PB2	21	I/O	5VT	Default: BOOT1 Alternate: LPTIMER_OUT, EVENTOUT, RTC_OUT Additional: PB2, WKUP3
PB10	22	I/O	5VT	Default: PB10 Alternate: SPI1_SCK, I2S1_CK, LPUART_TX, I2C1_SCL, LPUART_RX, TIMER1_CH2, CMP0_OUT, EVENTOUT
PB11	23	I/O	5VT	Default: PB11 Alternate: LPUART_RX, I2C1_SDA, LPUART_TX, TIMER1_CH3, CMP1_OUT, EVENTOUT
PB12	24	I/O	5VT	Default: PB12 Alternate: SPI1_NSS, I2S1_WS, I2C1_SMBA, LPUART_RTS, EVENTOUT
PB13	25	I/O	5VT	Default: PB13 Alternate: CK_OUT, SPI1_SCK, I2S1_CK, LPUART_CTS, I2C1_SCL, EVENTOUT
PB14	26	I/O	5VT	Default: PB14 Alternate: SPI1_MISO, LPUART_RTS, I2C1_SDA, T

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Pin Name	Pins	Pin Type[1]	I/O Level[2]	Functions description
				IMER11_CH0[3], EVENTOUT, RTC_OUT
PB15	27	I/O	5VT	Default: PB15 Alternate: SPI1_MOSI, I2S1_SD, TIMER11_CH1[3], EVENTOUT Additional: RTC_REFIN
PC6	28	I/O	5VT	Default: PC6 Alternate: I2S1_MCK, TIMER2_CH0, EVENTOUT Additional: WKUP4
PC7	29	I/O	5VT	Default: PC7 Alternate: TIMER2_CH1, EVENTOUT
PA8	30	I/O	5VT	Default: PA8 Alternate: USART0_CK, CK_OUT, LPTIMER_OUT, EVENTOUT, CTC_SYNC Additional: VCORE
PA9	31	I/O	5VT	Default: PA9 Alternate: CK_OUT, USART0_TX, I2C0_SCL, EVENTOUT, LPTIMER_IN1
PA10	32	I/O	5VT	Default: PA10 Alternate: USART0_RX, I2C0_SDA, EVENTOUT
PA11	33	I/O	5VT	Default: PA11 Alternate: CMP0_OUT, USART0_CTS, SPI0_MISO, EVENTOUT Additional: USBDM
PA12	34	I/O	5VT	Default: PA12 Alternate: CMP1_OUT, USART0_RTS, SPI0_MOSI, EVENTOUT Additional: USBDP
PA13	35	I/O	5VT	Default: SWDIO Alternate: LPUART_RX, I2C0_SCL, USART0_TX, SPI0_IO2, SPI0_NSS, EVENTOUT Additional: PA13
PA14	36	I/O	5VT	Default: SWCLK Alternate: LPUART_TX, USART1_TX, I2C0_SDA, USART0_RX, SPI0_IO3, SPI1_NSS, I2S1_WS, EVENTOUT Additional: PA14
PA15	37	I/O	5VT	Default: PA15 Alternate: SPI1_NSS, I2S1_WS, TIMER1_CH0_ETI, SPI0_NSS, USART1_RX, EVENTOUT
PC10	38	I/O	5VT	Default: PC10 Alternate: UART3_TX, LPUART_TX, SPI1_SCK, I2S1_CK, EVENTOUT
PC11	39	I/O	5VT	Default: PC11

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Pin Name	Pins	Pin Type[1]	I/O Level[2]	Functions description
				Alternate: UART3_RX, LPUART_RX, SPI1_MISO, EVENTOUT
PC12	40	I/O	5VT	Default: PC12 Alternate: UART4_TX[3], SPI1_MOSI, I2S1_SD, EVENTOUT
PB3	41	I/O	5VT	Default: PB3 Alternate:UART4_TX[3], SPI1_SCK, I2S1_CK, TIMER1_CH1, SPI0_SCK, USART0_RTS, EVENTOUT, LPTIMER_IN1 Additional: CMP1_IM6
PB4	42	I/O	5VT	Default: PB4 Alternate: UART4_RX[3], SPI1_MISO, TIMER2_CH0, SPI0_MISO, USART0_CTS, EVENTOUT Additional: CMP1_IP1
PB5	43	I/O		Default: PB5 Alternate: LPTIMER_IN0, I2C0_SMBA, SPI1_MOSI, I2S1_SD, TIMER2_CH1, SPI0_MOSI, USART0_CK, CMP1_OUT, EVENTOUT Additional: CMP1_IP2
PB6	44	I/O	5VT	Default: PB6 Alternate: LPTIMER_ETI0, I2C1_SCL, I2C0_SCL, USART0_TX, SPI0_IO2, EVENTOUT Additional: CMP1_IP3
PB7	45	I/O	5VT	Default: PB7 Alternate: I2C1_SDA, I2C0_SDA, USART0_RX, SPI0_IO3, EVENTOUT Additional: CMP1_IP4
BOOT0-PD3	46	I/O		Default: BOOT0 Alternate: USART1_CTS, SPI1_MISO, I2S1_MCK Additional: PD3
PB8	47	I/O	5VT	Default: PB8 Alternate: I2C1_SCL, I2C0_SCL, CMP0_OUT, EVENTOUT
PB9	48	I/O	5VT	Default: PB9 Alternate: I2C1_SDA, SPI1_NSS, I2S1_WS, I2C0_SDA, CMP1_OUT, EVENTOUT

Note:

(1) Type: I = input, O = output, A = analog, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

(3) Functions are available on GD32L233CB/C devices only.

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2.6.3. GD32L233Kx LQFP32 pin definitions

Table 2-5. GD32L233Kx LQFP32 pin definitions

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
VDD	1	P		Default: VDD
PF0-OSCIN	2	I/O		Default: OSCIN Alternate: EVENTOUT, SPI1_NSS, I2S1_WS Additional: PF0
PF1-OSCOUT	3	I/O		Default: OSCOUT Alternate: EVENTOUT, SPI1_SCK, I2S1_CK Additional: PF1
NRST	4	I/O		Default: NRST
VDDA	5	P		Default: VDDA
PA0	6	I/O		Default: PA0 Alternate: USART1_CTS, TIMER1_CH0_ETI, CMP0_OUT, EVENTOUT, UART3_TX Additional: WKUP0, ADC_IN0, RTC_TAMP1, CMP0_IM4
PA1	7	I/O		Default: PA1 Alternate: USART1_RTS, TIMER1_CH1, I2C0_SMBA, SPI0_SCK, EVENTOUT, UART3_RX Additional: ADC_IN1, CMP0_IP
PA2	8	I/O		Default: PA2 Alternate: USART1_TX, TIMER8_CH0, TIMER1_CH2, SPI0_IO2, CMP1_OUT, LPUART_TX, EVENTOUT Additional: ADC_IN2, CMP1_IM4, RTC_TAMP2, WKUP2
PA3	9	I/O		Default: PA3 Alternate: USART1_RX, TIMER8_CH1, TIMER1_CH3, SPI0_IO3, LPUART_RX, EVENTOUT Additional: ADC_IN3, CMP1_IP0
PA4	10	I/O		Default: PA4 Alternate: SPI0_NSS, USART1_CK, SPI1_NSS, I2S1_WS, LPTIMER_OUT, EVENTOUT Additional: ADC_IN4, DAC_OUT
PA5	11	I/O		Default: PA5 Alternate: SPI0_SCK, TIMER1_CH0_ETI, LPTIMER_ETI0, EVENTOUT Additional: ADC_IN5
PA6	12	I/O		Default: PA6 Alternate: SPI0_MISO, TIMER2_CH0, LPTIMER_IN0, CMP0_OUT, LPUART_CTS, EVENTOUT

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Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
				Additional: ADC_IN6
PA7	13	I/O		Default: PA7 Alternate: SPI0_MOSI, TIMER2_CH1, LPTIMER_ETI0, CMP1_OUT, EVENTOUT Additional: ADC_IN7
PB0	14	I/O		Default: PB0 Alternate: TIMER2_CH2, LPTIMER_OUT, SPI0_NSS, CMP0_OUT, EVENTOUT Additional: ADC_IN8, VREF_OUT
PB1	15	I/O		Default: PB1 Alternate: TIMER2_CH3, LPUART_RTS, LPTIMER_IN0, EVENTOUT Additional: ADC_IN9, VREF_OUT
BOOT1-PB2	16	I/O	5VT	Default: BOOT1 Alternate: LPTIMER_OUT, EVENTOUT, RTC_OUT Additional: PB2, WKUP3
VDD	17	P		Default: VDD
PA8	18	I/O	5VT	Default: PA8 Alternate: USART0_CK, CK_OUT, LPTIMER_OUT, EVENTOUT, CTC_SYNC Additional: VCORE
PA9	19	I/O	5VT	Default: PA9 Alternate: CK_OUT, USART0_TX, I2C0_SCL, EVENTOUT, LPTIMER_IN1
PA10	20	I/O	5VT	Default: PA10 Alternate: USART0_RX, I2C0_SDA, EVENTOUT
PA11	21	I/O	5VT	Default: PA11 Alternate: CMP0_OUT, USART0_CTS, SPI0_MISO, EVENTOUT Additional: USBDM
PA12	22	I/O	5VT	Default: PA12 Alternate: CMP1_OUT, USART0_RTS, SPI0_MOSI, EVENTOUT Additional: USBDP
PA13	23	I/O	5VT	Default: SWDIO Alternate: LPUART_RX, I2C0_SCL, USART0_TX, SPI0_IO2, SPI0_NSS, EVENTOUT Additional: PA13
PA14	24	I/O	5VT	Default: SWCLK Alternate: LPUART_TX, USART1_TX, I2C0_SDA, USART0_RX, SPI0_IO3, SPI1_NSS, I2S1_WS, EVENTOUT Additional: PA14

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Pin Name	Pins	Pin Type[1]	I/O Level[2]	Functions description
PA15	25	I/O	5VT	Default: PA15 Alternate: SPI1_NSS, I2S1_WS, TIMER1_CH0_ETI, SPI0_NSS, USART1_RX, EVENTOUT
PB3	26	I/O	5VT	Default: PB3 Alternate: SPI1_SCK, I2S1_CK, TIMER1_CH1, SPI0_SCK, USART0_RTS, EVENTOUT, LPTIMER_IN1 Additional: CMP1_IM6
PB4	27	I/O	5VT	Default: PB4 Alternate: SPI1_MISO, TIMER2_CH0, SPI0_MISO, USART0_CTS, EVENTOUT Additional: CMP1_IP1
PB5	28	I/O		Default: PB5 Alternate: LPTIMER_IN0, I2C0_SMBA, SPI1_MOSI, I2S1_SD, TIMER2_CH1, SPI0_MOSI, USART0_CK, CMP1_OUT, EVENTOUT Additional: CMP1_IP2
PB6	29	I/O	5VT	Default: PB6 Alternate: LPTIMER_ETI0, I2C1_SCL, I2C0_SCL, USART0_TX, SPI0_IO2, EVENTOUT Additional: CMP1_IP3
PB7	30	I/O	5VT	Default: PB7 Alternate: I2C1_SDA, I2C0_SDA, USART0_RX, SPI0_IO3, EVENTOUT Additional: CMP1_IP4
BOOT0-PD3	31	I/O		Default: BOOT0 Alternate: USART1_CTS, SPI1_MISO, I2S1_MCK Additional: PD3
VSS	32	P		Default: VSS

Note:

(1) Type: I = input, O = output, A = analog, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

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2.6.4. GD32L233Kx QFN32 pin definitions

Table 2-6. GD32L233Kx QFN32 pin definitions

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
PC14-OSC32IN	1	I/O		Default: PC14 Alternate: EVENTOUT Additional: OSC32IN
PC15-OSC32OUT	2	I/O		Default: PC15 Alternate: EVENTOUT Additional: OSC32OUT
PF0-OSCIN	3	I/O		Default: OSCIN Alternate: EVENTOUT, SPI1_NSS, I2S1_WS Additional: PF0
PF1-OSCOUT	4	I/O		Default: OSCOUT Alternate: EVENTOUT, SPI1_SCK, I2S1_CK Additional: PF1
NRST	5	I/O		Default: NRST
VDD	6	P		Default: VDD
PA0	7	I/O		Default: PA0 Alternate: USART1_CTS, TIMER1_CH0_ETI, CMP0_OUT, EVENTOUT, UART3_TX Additional: WKUP0, ADC_IN0, RTC_TAMP1, CMP0_IM4
PA1	8	I/O		Default: PA1 Alternate: USART1_RTS, TIMER1_CH1, I2C0_SMBA, SPI0_SCK, EVENTOUT, UART3_RX Additional: ADC_IN1, CMP0_IP
PA2	9	I/O		Default: PA2 Alternate: USART1_TX, TIMER8_CH0, TIMER1_CH2, SPI0_IO2, CMP1_OUT, LPUART_TX, EVENTOUT Additional: ADC_IN2, CMP1_IM4, RTC_TAMP2, WKUP2
PA3	10	I/O		Default: PA3 Alternate: USART1_RX, TIMER8_CH1, TIMER1_CH3, SPI0_IO3, LPUART_RX, EVENTOUT Additional: ADC_IN3, CMP1_IP0
PA4	11	I/O		Default: PA4 Alternate: SPI0_NSS, USART1_CK, SPI1_NSS, I2S1_WS, LPTIMER_OUT, EVENTOUT Additional: ADC_IN4, DAC_OUT
PA5	12	I/O		Default: PA5 Alternate: SPI0_SCK, TIMER1_CH0_ETI, LPTIMER_

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Pin Name	Pins	Pin Type[1]	I/O Level[2]	Functions description
				ETI0, EVENTOUT Additional: ADC_IN5
PA6	13	I/O		Default: PA6 Alternate: SPI0_MISO, TIMER2_CH0, LPTIMER_IN0, CMP0_OUT, LPUART_CTS, EVENTOUT Additional: ADC_IN6
PA7	14	I/O		Default: PA7 Alternate: SPI0_MOSI, TIMER2_CH1, LPTIMER_ETI0, CMP1_OUT, EVENTOUT Additional: ADC_IN7
PB0	15	I/O		Default: PB0 Alternate: TIMER2_CH2, LPTIMER_OUT, SPI0_NSS, CMP0_OUT, EVENTOUT Additional: ADC_IN8, VREF_OUT
PB1	16	I/O		Default: PB1 Alternate: TIMER2_CH3, LPUART_RTS, LPTIMER_IN0, EVENTOUT Additional: ADC_IN9, VREF_OUT
BOOT1-PB2	17	I/O	5VT	Default: BOOT1 Alternate: LPTIMER_OUT, EVENTOUT, RTC_OUT Additional: PB2, WKUP3
PA8	18	I/O	5VT	Default: PA8 Alternate: USART0_CK, CK_OUT, LPTIMER_OUT, EVENTOUT, CTC_SYNC Additional: VCORE
PA9	19	I/O	5VT	Default: PA9 Alternate: CK_OUT, USART0_TX, I2C0_SCL, EVENTOUT, LPTIMER_IN1
PA10	20	I/O	5VT	Default: PA10 Alternate: USART0_RX, I2C0_SDA, EVENTOUT
PA11	21	I/O	5VT	Default: PA11 Alternate: CMP0_OUT, USART0_CTS, SPI0_MISO, EVENTOUT Additional: USBDM
PA12	22	I/O	5VT	Default: PA12 Alternate: CMP1_OUT, USART0_RTS, SPI0_MOSI, EVENTOUT Additional: USBDP
PA13	23	I/O	5VT	Default: SWDIO Alternate: LPUART_RX, I2C0_SCL, USART0_TX, SPI0_IO2, SPI0_NSS, EVENTOUT Additional: PA13
PA14	24	I/O	5VT	Default: SWCLK

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Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
				Alternate: LPUART_TX, USART1_TX, I2C0_SDA, USART0_RX, SPI0_IO3, SPI1_NSS, I2S1_WS, EVENTOUT Additional: PA14
PA15	25	I/O	5VT	Default: PA15 Alternate: SPI1_NSS, I2S1_WS, TIMER1_CH0_ETI, SPI0_NSS, USART1_RX, EVENTOUT
PB3	26	I/O	5VT	Default: PB3 Alternate: SPI1_SCK, I2S1_CK, TIMER1_CH1, SPI0_SCK, USART0_RTS, EVENTOUT, LPTIMER_IN1 Additional: CMP1_IM6
PB4	27	I/O	5VT	Default: PB4 Alternate: SPI1_MISO, TIMER2_CH0, SPI0_MISO, USART0_CTS, EVENTOUT Additional: CMP1_IP1
PB5	28	I/O		Default: PB5 Alternate: LPTIMER_IN0, I2C0_SMBA, SPI1_MOSI, I2S1_SD, TIMER2_CH1, SPI0_MOSI, USART0_CK, CMP1_OUT, EVENTOUT Additional: CMP1_IP2
PB6	29	I/O	5VT	Default: PB6 Alternate: LPTIMER_ETI0, I2C1_SCL, I2C0_SCL, USART0_TX, SPI0_IO2, EVENTOUT Additional: CMP1_IP3
PB7	30	I/O	5VT	Default: PB7 Alternate: I2C1_SDA, I2C0_SDA, USART0_RX, SPI0_IO3, EVENTOUT Additional: CMP1_IP4
BOOT0-PD3	31	I/O		Default: BOOT0 Alternate: USART1_CTS, SPI1_MISO, I2S1_MCK Additional: PD3
VBAT	32	P		Default: VBAT

Note:

(1) Type: I = input, O = output, A = analog, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

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2.6.5. GD32L233xx pin alternate functions

Table 2-7. Port A alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9
PA0		TIMER1_CH0_ETI					CMP0_OUT	USART1_CTS	UART3_TX	EVENTOUT
PA1		TIMER1_CH1		SEG0(2)	I2C0_SMBA	SPI0_SCK		USART1_RTS	UART3_RX	EVENTOUT
PA2		TIMER1_CH2	TIMER8_CH0	SEG1(2)		SPI0_IO2	CMP1_OUT	USART11_TX	LPUART_TX	EVENTOUT
PA3		TIMER1_CH3	TIMER8_CH1	SEG2(2)		SPI0_IO3		USART1_RX	LPUART_RX	EVENTOUT
PA4			LPTIMER_OUT			SPI0_NSS	SPI1_NSS/I2S1_WS	USART1_CK		EVENTOUT
PA5		TIMER1_CH0_ETI	LPTIMER_ETI0			SPI0_SCK				EVENTOUT
PA6		TIMER2_CH0	LPTIMER_IN0	SEG3(2)		SPI0_MISO	CMP0_OUT		LPUART_CTS	EVENTOUT
PA7		TIMER2_CH1	LPTIMER_ETI0	SEG4(2)	I2C2_SCL(2)	SPI0_MOSI	CMP1_OUT			EVENTOUT
PA8	CK_OUT		LPTIMER_OUT	COM0(2)	I2C2_SMBA(2)			USART0_CK	CTC_SYNC	EVENTOUT
PA9	CK_OUT		LPTIMER_IN1	COM1(2)	I2C0_SCL			USART0_TX		EVENTOUT
PA10				COM2(2)	I2C0_SDA			USART0_RX		EVENTOUT
PA11						SPI0_MISO	CMP0_OUT	USART0_CTS		EVENTOUT
PA12						SPI0_MOSI	CMP1_OUT	USART0_RTS		EVENTOUT
PA13	SWDIO		LPUART_RX		I2C0_SCL	SPI0_IO2	SPI0_NSS	USART0_TX		EVENTOUT
PA14	SWCLK		LPUART_TX		I2C0_SDA	SPI0_IO3	SPI1_NSS/I2S1_WS	USART0_RX	USART1_TX	EVENTOUT
PA15		TIMER1_CH0_ETI		SEG17(2)		SPI0_NSS	SPI1_NSS/I2S1_WS	USART1_RX		EVENTOUT

Table 2-8. Port B alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9
PB0		TIMER2_CH2	LPTIMER_OUT	SEG5(2)		SPI0_NSS	CMP0_OUT			EVENTOUT
PB1		TIMER2_CH3	LPTIMER_IN0	SEG6(2)					LPUART_RTS	EVENTOUT
PB2	RTC_OUT		LPTIMER_OUT							EVENTOUT
PB3		TIMER1_CH1	LPTIMER_IN1	SEG7(2)		SPI0_SCK	SPI1_SCK/I2S1_CK	USART0_RTS	UART4_TX(1)	EVENTOUT
PB4		TIMER2_CH0		SEG8(2)		SPI0_MISO	SPI1_MISO	USART0_CTS	UART4_RX(1)	EVENTOUT
PB5		TIMER2_CH1	LPTIMER_IN0	SEG9(2)	I2C0_SMBA	SPI0_MOSI	SPI1_MOSI/I2S1_SD	USART0_CK	CMP1_OUT	EVENTOUT
PB6			LPTIMER_ETI0		I2C0_SCL	SPI0_IO2		USART0_TX	I2C1_SCL	EVENTOUT
PB7					I2C0_SDA	SPI0_IO3		USART0_RX	I2C1_SDA	EVENTOUT
PB8				SEG16(2)	I2C0_SCL		CMP0_OUT		I2C1_SCL	EVENTOUT
PB9				COM3(2)	I2C0_SDA	SPI1_NSS/I2S1_	CMP1_OUT		I2C1_SDA	EVENTOUT

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Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9
						WS				
PB10		TIMER1_CH2		SEG10(2)	I2C1_SCL	SPI1_SCK/I2S1_CK	CMP0_OUT	LPUART_TX	LPUART_RX	EVENTOUT
PB11		TIMER1_CH3		SEG11(2)	I2C1_SDA		CMP1_OUT	LPUART_RX	LPUART_TX	EVENTOUT
PB12				SEG12(2)	I2C1_SMBA		SPI1_NSS/I2S1_WS		LPUART_RTS	EVENTOUT
PB13	CK_OUT			SEG13(2)	I2C1_SCL		SPI1_SCK/I2S1_CK		LPUART_CTS	EVENTOUT
PB14	RTC_OUT		TIMER11_CH0(1)	SEG14(2)	I2C1_SDA		SPI1_MISO		LPUART_RTS	EVENTOUT
PB15			TIMER11_CH1(1)	SEG15(2)			SPI1_MOSI/I2S1_SD			EVENTOUT

Table 2-9. Port C alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9
PC0			LPTIMER_IN0	SEG18(2)	I2C2_SCL(2)				LPUART_RX	EVENTOUT
PC1			LPTIMER_OUT	SEG19(2)	I2C2_SDA(2)				LPUART_TX	EVENTOUT
PC2			LPTIMER_IN1	SEG20(2)		SPI1_MISO	I2S1_MCK			EVENTOUT
PC3			LPTIMER_ETI0	SEG21(2)		SPI1_MOSI/I2S1_SD				EVENTOUT
PC4		TIMER1_CH0_ETI		SEG22(2)				USART0_TX	LPUART_TX	EVENTOUT
PC5		TIMER1_CH1		SEG23(2)				USART0_RX	LPUART_RX	EVENTOUT
PC6		TIMER2_CH0		SEG24(2)		I2S1_MCK				EVENTOUT
PC7		TIMER2_CH1		SEG25(2)						EVENTOUT
PC8		TIMER2_CH2		SEG26(2)	I2C2_SDA(2)					EVENTOUT
PC9		TIMER2_CH3		SEG27(2)	I2C2_SCL(2)					EVENTOUT
PC10				SEG28(2)/COM4(2)		SPI1_SCK/I2S1_CK		UART3_TX	LPUART_TX	EVENTOUT
PC11				SEG29(2)/COM5(2)		SPI1_MISO		UART3_RX	LPUART_RX	EVENTOUT
PC12				SEG30(2)/COM6(2)		SPI1_MOSI/I2S1_SD		UART4_TX(1)		EVENTOUT
PC13										EVENTOUT
PC14										EVENTOUT
PC15										EVENTOUT

Table 2-10. Port D alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9
PD0			LPTIMER_OUT				SPI1_NSS/I2S1_WS	USART1_CK	CTC_SYNC	EVENTOUT
PD1						SPI1_MISO	SPI1_SCK/I2S1_C	USART1_CTS		EVENTOUT

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Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9
							K			
PD2		TIMER2_ETI		SEG31(2) /COM7(2)				UART4_RX(1)	LPUART_RTS	EVENTOUT
PD3						SPI1_MISO	I2S1_MCK	USART1_CTS		
PD4				SEG28(2)		SPI1_MOSI/I2S1_SD		USART1_RTS		EVENTOUT
PD5				SEG29(2)		SPI0_MISO		USART1_TX		EVENTOUT
PD6			LPTIMER_IN1			SPI0_MOSI		USART1_RX		EVENTOUT
PD8			LPTIMER_ETI0	SEG30(2)					LPUART_TX	EVENTOUT
PD9			LPTIMER_IN0	SEG31(2)					LPUART_RX	EVENTOUT

Table 2-11. Port F alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9
PF0						SPI1_NSS/I2S1_WS				EVENTOUT
PF1						SPI1_SCK/I2S1_CK				EVENTOUT

Note:

(1) Functions are available on GD32L233RC/RB/CC/CB devices only.

(2) Functions are available on GD32L233Rx devices only.

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3. Functional description

3.1. Arm® Cortex®-M23 core

The Cortex-M23 processor is an energy-efficient processor with a very low gate count. It is intended to be used for microcontroller and deeply embedded applications that require an area-optimized processor. The processor is highly configurable enabling a wide range of implementations from those requiring memory protection and powerful trace technology to cost sensitive devices requiring minimal area, while delivering outstanding computational performance and an advanced system response to interrupts.

32-bit ARM® Cortex®-M23 processor core

- Up to 64 MHz operation frequency.
- Single-cycle multiplication and hardware divider.
- Ultra-low power, energy-efficient operation.
- Excellent code density.
- Integrated Nested Vectored Interrupt Controller (NVIC).
- 24-bit SysTick timer.

The Cortex®-M23 processor is based on the ARMv8-M architecture and supports both Thumb and Thumb-2 instruction sets. Some system peripherals listed below are also provided by Cortex®-M23:

- Internal Bus Matrix connected with AHB master, Serial Wire Debug Port and Single-cycle IO port.
- Nested Vectored Interrupt Controller (NVIC).
- Breakpoint Unit(BPU).
- Data Watchpoint and Trace (DWT).
- Serial Wire Debug Port.

3.2. Embedded memory

- Up to 256 Kbytes of Flash memory.
- Up to 32 Kbytes of SRAM with hardware parity checking.

256 Kbytes of inner Flash memory, and 32 Kbytes of inner SRAM at most is available for storing programs and data, and Flash is accessed (read) at CPU clock speed with 0~3 wait states. ***Table 2-2. GD32L233xx memory map*** shows the memory map of the GD32L233xx series of devices, including code, SRAM, peripheral, and other pre-defined regions.

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3.3. Clock, reset and supply management

- Internal 16 MHz factory-trimmed RC and external 4 to 32 MHz crystal oscillator.
- Internal 48 MHz factory-trimmed RC.
- Internal 32 KHz RC calibrated oscillator and external 32.768 KHz crystal oscillator.
- Integrated system clock PLL.
- 1.71 to 3.63 V application supply and I/Os.
- Supply Supervisor: POR (Power On Reset), PDR (Power Down Reset), and low voltage detector (LVD).

The Clock Control Unit (CCTL) provides a range of oscillator and clock functions. These include speed internal RC oscillator and external crystal oscillator, high speed and low speed two types. Several prescalers allow the frequency configuration of the AHB and two APB domains. The maximum frequency of the AHB, APB2 and APB1 domains is 64 MHz/64 MHz/32 MHz. See ***Figure 2-6. GD32L233xx clock tree*** for details on the clock tree.

The Reset Control Unit (RCU) controls three kinds of reset: system reset resets the processor core and peripheral IP components. Power-on reset (POR) and power-down reset (PDR) are always active, and ensures proper operation starting from 1.60 V and down to 1.56V. The device remains in reset mode when V_{DD} is below a specified threshold. The embedded low voltage detector (LVD) monitors the power supply, compares it to the voltage threshold and generates an interrupt as a warning message for leading the MCU into security.

Power supply schemes:

- V_{DD} range: 1.71 to 3.63 V, external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SS} is 0 V.
- V_{DDA} range: 1.71 to 3.63 V, external analog power supplies for ADC, reset blocks, RCs and PLL.
- V_{BAK} range: 1.71 to 3.63 V, power supply for RTC unit, LXTAL oscillator, BPOR, and two pads, including PC13 to PC15 when V_{DD} is not present.

3.4. Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from main Flash memory (default).
- Boot from system memory.
- Boot from on-chip SRAM.

In default condition, boot from main Flash memory is selected. The boot loader is located in the internal boot ROM memory (system memory). It is used to reprogram the Flash

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memory by using USART0 (PA9 and PA10) or USART1 (PA2 and PA3) or USBD (PA11 and PA12).

3.5. Power saving modes

The MCU supports ten kinds of power saving modes to achieve even lower power consumption. They are Run, Run1, Run2, Sleep, Sleep1, Sleep2, Deep-sleep, Deep-sleep 1, Deep-sleep 2 and Standby mode. These operating modes reduce the power consumption and allow the application to achieve the best balance between the CPU operating time, speed and power consumption.

- **Run mode**
  After system reset/ power reset or wakeup from standby mode, the MCU enters Run mode. And the NPLDO (normal power LDO) works in 1.1V mode.
- **Run1 mode**
  When in Run mode, the NPLDO should be selected as 0.9V by configuring the LDOVS bits in PMU_CTL0. In this mode, the system clock frequency should not exceed 16MHz.
- **Run2 mode**
  When in Run mode or Run1 mode, the NPLDO can be selected as 0.9V by configuring the LDOVS bits in PMU_CTL0. The LDNP in PMU_CTL0 register should be configured to select the low-dirver mode. In this mode, the system clock frequency should not exceed 2MHz.
- **Sleep mode**
  The Sleep mode is corresponding to the SLEEPING mode of the Cortex®-M23. In Sleep mode, only clock of Cortex®-M23 is off. To enter the Sleep mode, it is only necessary to clear the SLEEPDEEP bit in the Cortex®-M23 System Control Register, and execute a WFI or WFE instruction. If the Sleep mode is entered by executing a WFI instruction, any interrupt can wake up the system. If it is entered by executing a WFE instruction, any wakeup event can wake up the system (If SEVONPEND is 1, any interrupt can wake up the system, refer to Cortex®-M33 Technical Reference Manual). The mode offers the lowest wakeup time as no time is wasted in interrupt entry or exit.
- **Sleep1 mode**
  The Sleep1 mode is corresponding to the SLEEPING mode of the Cortex®-M23 When in Run1 mode. The NPLDO should be selected as 0.9V by configuring the LDOVS bits in PMU_CTL0.
- **Sleep2 mode**
  The Sleep2 mode is corresponding to the SLEEPING mode of the Cortex®-M23 When in Run2 mode. The NPLDO should be selected as 0.9V by configuring the LDOVS bits in PMU_CTL0. The LDNP in PMU_CTL0 should be configured to select the low-dirver mode.
- **Deep-sleep mode**
  The Deep-sleep mode is based on the SLEEPDEEP mode of the Cortex®-M23. In

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Deep-sleep mode, all clocks in the 1.1V domain are off, and all of IRC16M, IRC48M, HXTAL and PLLs are disabled. The contents of SRAM and registers are preserved. The NPLDO can operate normally or in low driver mode depending on the LDNPDSP bit in the PMU_CTL0 register. Before entering the Deep-sleep mode, it is necessary to set the SLEEPDEEP bit in the Cortex®-M23 System Control Register, and set LPMOD bits to “00” in the PMU_CTL0 register. Then, the device enters the Deep-sleep mode after a WFI or WFE instruction is executed. If the Deep-sleep mode is entered by executing a WFI instruction, any interrupt from EXTI lines can wake up the system. If it is entered by executing a WFE instruction, any wakeup event from EXTI lines can wake up the system (If SEVONPEND is 1, any interrupt from EXTI lines can wake up the system, refer to Cortex®-M23 Technical Reference Manual). When exiting the Deep-sleep mode, the IRC16M is selected as the system clock. Notice that an additional wakeup delay will be incurred if the LDO operates in low driver mode.

- **Deep-sleep 1 mode**

  The Deep-sleep 1 mode is based on the SLEEPDEEP mode of the Cortex®-M23. In Deep-sleep 1 mode, all clocks in the 1.1V domain are off, and all of IRC16M, IRC48M, HXTAL and PLLs are disabled. The LPLDO (low power LDO) can operate normally instead of NPLDO. Before entering the Deep-sleep 1 mode, it is necessary to set the SLEEPDEEP bit in the Cortex®-M23 System Control Register, set LPMOD bits to “01” in the PMU_CTL0 register. Then, the device enters the Deep-sleep 1 mode after a WFI or WFE instruction is executed. If the Deep-sleep 1 mode is entered by executing a WFI instruction, any interrupt from EXTI lines can wake up the system. If it is entered by executing a WFE instruction, any wakeup event from EXTI lines can wake up the system (If SEVONPEND is 1, any interrupt from EXTI lines can wake up the system, refer to Cortex®-M23 Technical Reference Manual). When exiting the Deep-sleep 1 mode, the IRC16M is selected as the system clock. Waking up from Deep-sleep 1 mode needs an additional delay to wakeup NPLDO.

- **Deep-sleep 2 mode**

  The Deep-sleep 2 mode is based on the SLEEPDEEP mode of the Cortex®-M23. In Deep-sleep 2 mode, all clocks in the 1.1V domain are off, and all of IRC16M, IRC48M, HXTAL and PLLs are disabled. The power of COREOFF0/SRAM1/COREOFF1 domain is cut off. The contents of COREOFF0/SRAM1/COREOFF1 domain are lost. The LPLDO can operate normally instead of NPLDO. Before entering the Deep-sleep 2 mode, it is necessary to set the SLEEPDEEP bit in the Cortex®-M23 System Control Register, set LPMOD bits to “10” in the PMU_CTL0 register. Then, the device enters the Deep-sleep 2 mode after a WFI or WFE instruction is executed. If the Deep-sleep 2 mode is entered by executing a WFI instruction, any interrupt from EXTI lines can wake up the system. If it is entered by executing a WFE instruction, any wakeup event from EXTI lines can wake up the system (If SEVONPEND is 1, any interrupt from EXTI lines can wake up the system, refer to Cortex®-M23 Technical Reference Manual). When exiting the Deep-sleep 2 mode, the IRC16M is selected as the system clock. Waking up from Deep-sleep 2 mode needs an additional delay to wakeup NPLDO.

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- **Standby mode**

  The Standby mode is based on the SLEEPDEEP mode of the Cortex®-M23, too. In Standby mode, the whole 1.1V domain is power off, the NPLDO/LPLDO is shut down, and all of IRC16M, IRC48M, HXTAL and PLLs are disabled. Before entering the Standby mode, it is necessary to set the SLEEPDEEP bit in the Cortex®-M23 System Control Register, and set the LPMOD bits to “11” in the PMU_CTL0 register, and clear WUF bit in the PMU_CS register. Then, the device enters the Standby mode after a WFI or WFE instruction is executed, and the STBF status flag in the PMU_CS register indicates that the MCU has been in Standby mode. There are four wakeup sources for the Standby mode, including the external reset from NRST pin, the RTC alarm/time stamp/tamper/auto wakeup events, the FWDGT reset, and the rising edge on WKUP pins. The Standby mode achieves the lowest power consumption, but spends longest time to wake up. Besides, the contents of SRAM and registers in 1.1V power domain are lost in Standby mode. When exiting from the Standby mode, a power-on reset occurs and the Cortex®-M23 will execute instruction code from the 0x00000000 address.

3.6. Clock trim controller (CTC)

- Three external reference signal source: GPIO, LXTAL clock, USBD_SOF.
- Provide software reference sync pulse.
- Automatically trimmed by hardware without any software action.
- 16 bits trim counter with reference signal source capture and reload.
- 8 bits clock trim base value to frequency evaluation and automatically trim.

The Clock Trim Controller (CTC) is used to trim internal 48MHz RC oscillator (IRC48M) automatically by hardware. If using IRC48M clock to USBD, the IRC48M must be 48 MHz with 500ppm. The internal oscillator without such a high degree of accuracy needs to be trimmed. The CTC unit trim the frequency of the IRC48M based on an external accurate reference signal source. It can automatically adjust the trim value to provide a precise IRC48M clock.

3.7. General-purpose inputs/outputs (GPIOs)

- Up to 59 fast GPIOs, all mappable on 16 external interrupt lines.
- Analog input/output configurable.
- Alternate function input/output configurable.

There are up to 59 general purpose I/O pins (GPIO) in GD32L233xx, named PA0 ~ PA15, PB0 ~ PB15, PC0 ~ PC15, PD0~PD6, PD8~PD9, PF0~ PF1 to implement logic input/output functions. Each GPIO port has related control and configuration registers to satisfy the requirements of specific applications. The external interrupts on the GPIO pins of the device have related control and configuration registers in the Interrupt/Event

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Controller Unit (EXTI).The GPIO ports are pin-shared with other alternative functions (AFs) to obtain maximum flexibility on the package pins.

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), input, peripheral alternate function or analog mode. Most of the GPIO pins are shared with digital or analog alternate functions.

3.8. CRC calculation unit (CRC)

- Supports 7/8/16/32 bit data input.
- For 7(8)/16/32 bit input data length, the calculation cycles are 1/2/4 AHB clock cycles.
- Free 8-bit register is unrelated to calculation and can be used for any other goals by any other peripheral devices.
- User configurable polynomial value and size.

A cyclic redundancy check (CRC) is an error-detecting code commonly used in digital networks and storage devices to detect accidental changes to raw data. This CRC calculation unit can be used to calculate 7/8/16/32 bit CRC code within user configurable polynomial.

3.9. True Random number generator (TRNG)

- About 40 periods of TRNG_CLK are needed between two consecutive random numbers.
- Disable TRNG module will reduce the chip power consumption.
- 32-bit random value seed is generated from analog noise, so the random number is a true random number.

The true random number generator (TRNG) module can generate a 32-bit random value by using continuous analog noise.

3.10. Direct memory access controller (DMA)

- 7 channels for DMA controller.
- DMA request from DMAMAX: peripherals (Timers, ADC, DAC, SPIs, I2S, I2Cs, USARTs, CAU and LPUART) and request generator.

The flexible general-purpose DMA controllers provide a hardware method of transferring data between peripherals and/or memory without intervention from the CPU, thereby increasing system performance by off-loading the MCU from copying large amounts of data and avoiding frequent interrupts to serve peripherals needing more data or having available data. Three types of access method are supported: peripheral to memory, memory to peripheral, memory to memory.

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Each channel is connected to flexible hardware DMA requests. The priorities of DMA channel requests are determined by software configuration and hardware channel number. Transfer size of source and destination are independent and configurable.

3.11. DMA request multiplexer (DMAMUX)

- 7 channels for DMAMUX request multiplexer.
- 4 channels for DMAMUX request generator.
- Support 21 trigger inputs and 21 synchronization inputs.

DMAMUX is a transmission scheduler for DMA requests. The DMAMUX request multiplexer is used for routing a DMA request line between the peripherals / generated DMA request (from the DMAMUX request generator) and the DMA controller. Each DMAMUX request multiplexer channel selects a unique DMA request line, unconditionally or synchronously with events from its DMAMUX synchronization inputs. The DMA request is pending until it is served by the DMA controller which generates a DMA acknowledge signal (the DMA request signal is de-asserted).

3.12. Analog to digital converter (ADC)

- 12-bit SAR ADC's conversion rate is up to 1.07 MSPS.
- Hardware oversampling ratio adjustable from 2x to 256x improves resolution to 16-bit.
- Input voltage range: V_{SS}/V_{SSA} to V_{DD}/V_{DDA}.
- Temperature sensor.

A 12-bit multi-channel ADC is integrated in the device. It has a total of 20 multiplexed channels: up to 16 external channels, 1 channel for internal temperature sensor (V_{SENSE}), 1 channel for internal reference voltage (V_{REFINT}), 1 channel for external battery power supply (V_{BAT}), and 1 channel for LCD voltage (V_{SLCD}). The input voltage range is between V_{SS}/V_{SSA} and V_{DD}/V_{DDA}. An on-chip hardware oversampling scheme improves performance while off-loading the related computational burden from the CPU. The analog watchdog allows the application to detect whether the input voltage goes outside the user-defined higher or lower thresholds. A configurable channel management block can be used to perform conversions in single, continuous, scan or discontinuous mode to support more advanced use.

The ADC can be triggered from the events generated by the general level 0 timers (TIMERx, x=1, 2) and the general level 1 timers (TIMERx, x=8, 11) with internal connection. The temperature sensor can be used to generate a voltage that varies linearly with temperature. It is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage in a digital value.

To ensure a high accuracy on ADC, the independent power supply V_{DDA} is implemented

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to achieve better performance of analog circuits. V_{DDA} can be externally connected to V_{DD} through the external filtering circuit that avoids noise on V_{DDA}.

3.13. Digital to analog converter (DAC)

- One12-bit DAC with one output channel.
- 8-bit or 12-bit mode in conjunction with the DMA controller.
- Support references from internal 2.5 V precision reference or external V_{REF} pin.

The 12-bit buffered DAC is used to generate variable analog outputs. The DAC channels can be triggered by the timer or EXTI with DMA support. The maximum output value of the DAC is V_{REF}.

3.14. Real time clock (RTC)

- Independent binary-coded decimal (BCD) format timer/counter with five 32-bit backup registers.
- Calendar with sub-second, second, minute, hour, week day, day, month and year automatically correction.
- Alarm function with wake up from deep-sleep and standby mode capability.
- On-the-fly correction for synchronization with master clock. Digital calibration with 0.95 ppm resolution for compensation of quartz crystal inaccuracy.

The real time clock is an independent timer which provides a set of continuously running counters in backup registers to provide a real calendar function, and provides an alarm interrupt or an expected interrupt. It is not reset by a system or power reset, or when the device wakes up from standby mode. In the RTC unit, there are two prescalers used for implementing the calendar and other functions. One prescaler is a 7-bit asynchronous prescaler and the other is a 15-bit synchronous prescaler.

3.15. Timers and PWM generation

- Up to four 16-bit general timers (TIMER1, TIMER2, TIMER8, TIMER11), two 16-bit basic timer (TIMER5, TIMER6), and one 32-bit low power timer (LPTIMER).
- Up to 4 independent channels of PWM, output compare or input capture for each general timer and external trigger input.
- Encoder interface controller with two inputs using quadrature decoder.
- Two 24-bit SysTick timers down counter.
- 2 watchdog timers (free watchdog timer and window watchdog timer).

The LPTIMER is a 32-bit timer and it is able to keep running in all power modes except for Standby mode with its diversity of clock sources. The LPTIMER provides one PWM out and also supports an encoder interface with two inputs using quadrature decoder.

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The general timer can be used for a variety of purposes including general time, input signal pulse width measurement or output waveform generation such as a single pulse generation or PWM output, up to 4 independent channels for input capture/output compare. TIMER1 and TIMER2 are based on a 16-bit auto-reload up/down/center-aligned counter and a 16-bit prescaler. TIMER8 and TIMER11 is based on a 16-bit auto-reload up counter and a 16-bit prescaler. The general timer also supports an encoder interface with two inputs using quadrature decoder.

The basic timer TIMER5 and TIMER6, are mainly used as a simple 16-bit time base.

The GD32L233xx have two watchdog peripherals, free watchdog timer and window watchdog timer. They offer a combination of high safety level, flexibility of use and timing accuracy.

The free watchdog timer includes a 12-bit down-counting counter and an 8-stage prescaler. It is clocked from an independent 32 KHz internal RC and as it operates independently of the main clock, it can operate in deep-sleep and standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management.

The window watchdog is based on a 7-bit down counter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early wakeup interrupt capability and the counter can be frozen in debug mode.

The SysTick timer is dedicated for OS, but could also be used as a standard down counter. The features are shown below:

- A 24-bit down counter.
- Auto reload capability.
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source.

3.16. Universal synchronous/asynchronous receiver transmitter (USART/UART)

- Up to two USARTs and two UARTs with operating frequency up to 8 MBits/s.
- Supports both asynchronous and clocked synchronous serial communication modes.
- IrDA SIR encoder and decoder support.
- LIN break generation and detection.
- ISO 7816-3 compliant smart card interface.
- Dual clock domain.
- Wake up from Deep-sleep mode.

The USART (USART0, USART1) and UART (UART3, UART4) are used to translate data between parallel and serial interfaces, provides a flexible full duplex data exchange using

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synchronous or asynchronous transfer. It is also commonly used for RS-232 standard communication. The USART/UART includes a programmable baud rate generator which is capable of dividing the system clock to produce a dedicated clock for the USART/UART transmitter and receiver. The USART/UART also supports DMA function for high speed data communication.

3.17. Universal asynchronous receiver transmitter (LPUART)

- Maximum speed up to 21 MBits/s.
- Supports asynchronous serial communication modes.
- Supports hardware modem operations (CTS/RTS) and RS485 drive.
- Dual clock domain.
- Wake up from Deep-sleep mode.

The Low-power universal Asynchronous Receiver/Transmitter (LPUART) provides a flexible serial data exchange interface with a limited power consumption. LPUART can perform asynchronous serial communication even with low power consumption. Data frames can be transferred in full duplex or half duplex mode, asynchronously through this interface. A programmable baud rate generator divides the clock to produces a dedicated wide range baudrate clock for the LPUART transmitter and receiver.

3.18. Inter-integrated circuit (I2C)

- Support both master and slave mode with a frequency up to 1 MHz (Fast mode plus).
- Provide arbitration function, optional PEC (packet error checking) generation and checking.
- Supports 7-bit and 10-bit addressing mode and general call addressing mode.
- Multiple 7-bit slave addresses (2 address, 1 with configurable mask).
- SMBus 3.0 and PMBus 1.3 compatible.
- Wakeup from Deep-sleep / Deep-sleep1 / Deep-sleep2 mode on I2C address match (only in I2C2).
- Wakeup from Deep-sleep1 / Deep-sleep2 mode on I2C address match (in I2C0 and I2C1).

The I2C interface is an internal circuit allowing communication with an external I2C interface which is an industry standard two line serial interface used for connection to external hardware. These two serial lines are known as a serial data line (SDA) and a serial clock line (SCL). The I2C module provides different data transfer rates: up to 100 KHz in standard mode, up to 400 KHz in the fast mode and up to 1 MHz in the fast mode plus. The I2C module also has an arbitration detect function to prevent the situation where more than one master attempts to transmit data to the I2C bus at the same time. A CRC-8 calculator is also provided in I2C interface to perform packet error checking for I2C data.

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3.19. Serial peripheral interface (SPI)

- Up to two SPI interfaces with a frequency of up to 16 MHz.
- Support both master and slave mode.
- Hardware CRC calculation and transmit automatic CRC error checking.
- Separate transmit and receive 32-bit FIFO with DMA capability (only in SPI0).
- Data frame size can be 4 to 16 bits (only in SPI0).
- Quad-SPI configuration available in master mode (only in SPI0).

The SPI interface uses 4 pins, among which are the serial data input and output lines (MISO & MOSI), the clock line (SCK) and the slave select line (NSS). All SPIs can be served by the DMA controller. The SPI interface may be used for a variety of purposes, including simplex synchronous transfers on two lines with a possible bidirectional data line or reliable communication using CRC checking. Quad-SPI master mode is also supported in SPI0.

3.20. Inter-IC sound (I2S)

- Sampling frequency from 8 KHz to 192 KHz.
- Support either master or slave mode.

The Inter-IC sound (I2S) bus provides a standard communication interface for digital audio applications by 4-wire serial lines. GD32L233xx contain an I2S-bus interface that can be operated with 16/32 bit resolution in master or slave mode, pin multiplexed with SPI1. The audio sampling frequency from 8 KHz to 192 KHz is supported.

3.21. Cryptographic acceleration Unit (CAU)

- Supports DES, TDES or AES (128, 192, or 256) algorithms.
- DES/TDES supports Electronic codebook (ECB) or Cipher block chaining (CBC) mode.
- AES supports 128bits-key, 192bits-key or 256 bits-key.
- AES supports Electronic codebook (ECB), Cipher block chaining (CBC) mode, Counter mode (CTR) mode, Galois/counter mode (GCM), Galois message authentication code mode (GMAC), Counter with CBC-MAC (CCM), Cipher Feedback mode (CFB) and Output Feedback mode (OFB).
- DMA transfer for incoming and outgoing data is supported.

The Cryptographic Acceleration Unit supports acceleration of DES, TDES or AES (128, 192, or 256) algorithms. The DES/TDES supports Electronic codebook (ECB) or Cipher block chaining (CBC) mode. The AES supports Electronic codebook (ECB), Cipher block chaining (CBC) mode, Counter mode (CTR) mode, Galois/counter mode (GCM), Galois message authentication code mode (GMAC), Counter with CBC-MAC (CCM), Cipher

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Feedback mode (CFB) and Output Feedback mode (OFB).

3.22. Segment LCD controller (SLCD)

- Configurable frame frequency.
- Blinking of individual segments or all segments.
- Supports Static, 1/2, 1/3, 1/4, 1/6 and 1/8 duty.
- Supports 1/2, 1/3 and 1/4 bias.
- Double buffer up to 8x32 bits registers to store SLCD_DATAx.
- The contrast can also be adjusted by configuring dead time.
- Optional voltage output driver for enhance SLCD driving capability.

The SLCD controller directly drives LCD displays by creating the AC segment and common voltage signals automatically. It can drive the monochrome passive liquid crystal display (LCD) which composed of a plurality of segments (pixels or complete symbols) that can be converted to visible or invisible. The SLCD controller can support up to 32 segments and 8 commons.

3.23. Comparators (CMP)

- Two fast rail-to-rail low-power comparators with software configurable.
- Programmable reference voltage (internal or external I/O).

Two Comparators (CMP) is implemented within the device. It can wake up from deep-sleep mode to generate interrupts and breaks for the timers and also can be combined as a window comparator. The internal voltage reference is also connected to ADC_IN17 input channel of the ADC.

3.24. Universal serial bus full-speed device interface (USBD)

- USB 2.0 full-speed device controller.
- Support USB 2.0 Link Power Management.
- Dedicated 512-byte SRAM used for data packet buffer.
- Support embedded pull-up on the DP line.
- Integrated USB PHY.

The Universal Serial Bus full-speed device interface (USBD) module contains a full-speed internal USB PHY and no more external PHY chip is needed. USBD supports all the four types of transfer (control, bulk, interrupt and isochronous) defined in USB 2.0 protocol. USBD supports 8 USB bidirectional endpoints that can be individually configured.

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3.25. Debug mode

- Serial wire debug port (SW-DP).

Debug capabilities can be accessed by a debug tool via Serial Wire (SW - Debug Port).

3.26. Package and operation temperature

- LQFP64 (GD32L233RxT6), LQFP48 (GD32L233CxT6), LQFP32 (GD32L233KxT6) and QFN32 (GD32L233KxQ6).
- Operation temperature range: -40°C to +85°C (industrial level)

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4 Electrical characteristics

4.1 Absolute maximum ratings

The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 4-1. Absolute maximum ratings(1)(4)

Symbol	Parameter	Min	Max	Unit
V_{DD}	External voltage range(2)	V_{SS} - 0.3	V_{SS} + 3.63	V
V_{DDA}	External analog supply voltage	V_{SSA} - 0.3	V_{SSA} + 3.63	V
V_{IN}	Input voltage on 5V tolerant pin(3)	V_{SS} - 0.3	V_{DD} + 3.63	V
	Input voltage on other I/O	V_{SS} - 0.3	3.63	V
$\lvert\Delta V_{DDx}\rvert$	Variations between different V_{DD} power pins	—	50	mV
$\lvert V_{SSX} - V_{SS}\rvert$	Variations between different ground pins	—	50	mV
I_{IO}	Maximum current for GPIO pins	—	±25	mA
T_A	Operating temperature range	-40	+85	°C
P_D	Power dissipation at T_A = 85°C of LQFP64	—	733	mW
	Power dissipation at T_A = 85°C of LQFP48	—	574	
	Power dissipation at T_A = 85°C of LQFP32	—	724	
	Power dissipation at T_A = 85°C of QFN32	—	940	
T_{STG}	Storage temperature range	-65	+150	°C
T_J	Maximum junction temperature	—	+125	°C

(1) Guaranteed by design, not tested in production.

(2) All main power and ground pins should be connected to an external power source within the allowable range.

(3) V_{IN} maximum value cannot exceed 5.5 V.

(4) It is recommended that V_{DD} and V_{DDA} are powered by the same source. The maximum difference between V_{DD} and V_{DDA} does not exceed 300 mV during power-up and operation.

4.2 Operating conditions characteristics

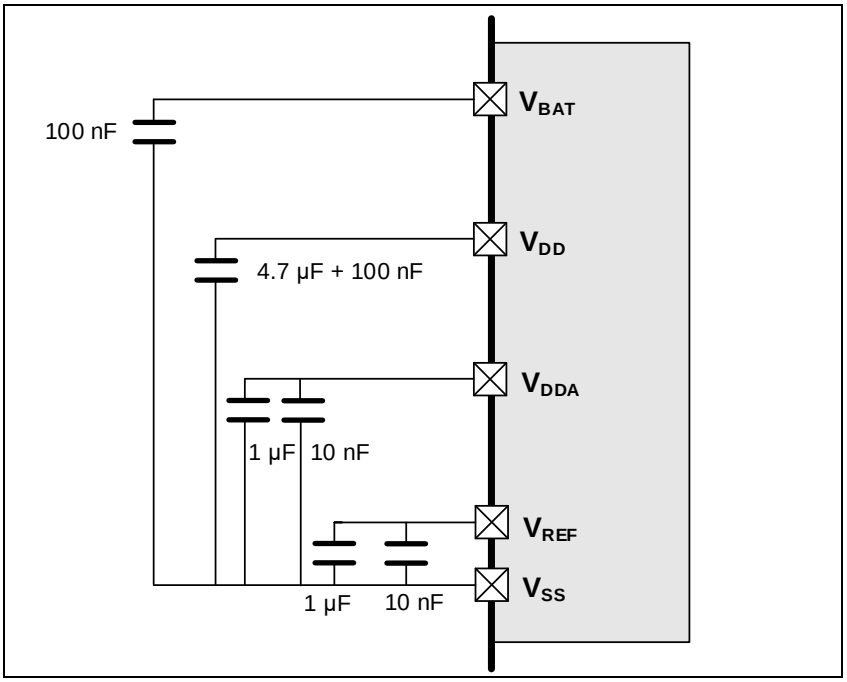
Table 4-2. DC operating conditions

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
V_{DD}	Supply voltage	—	1.71	3.3	3.63	V
V_{DDA}	Analog supply voltage	—	1.71	3.3	3.63	V
V_{BAT}	Battery supply voltage	—	1.71	3.3	3.63	V

(1) Based on characterization, not tested in production.

Figure 4-1. Recommended power supply decoupling capacitors(1)

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(1) All decoupling capacitors need to be as close as possible to the pins on the PCB board.

Table 4-3. Clock frequency(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK1}	AHB1 clock frequency	—	0	64	MHz
f_{HCLK2}	AHB2 clock frequency	—	0	64	MHz
f_{APB1}	APB1 clock frequency	—	0	32	MHz
f_{APB2}	APB2 clock frequency	—	0	64	MHz

(1) Guaranteed by design, not tested in production.

Table 4-4. Operating conditions at Power up/ Power down(1)

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	—	0	∞	us/v
	V_{DD} fall time rate		50	∞	

(1) Guaranteed by design, not tested in production.

Table 4-5. Start-up timings of Operating conditions(1)

Symbol	Parameter	Conditions	Typ	Unit
$t_{start-up}$	Start-up time	Clock source from HXTAL	1.24	ms
		Clock source from IRC16M	16.6	us

(1) Based on characterization, not tested in production.
(2) After power-up, the start-up time is the time between the rising edge of NRST high and the first I/O instruction conversion in SystemInit function.
(3) PLL is off.

Table 4-6. Power saving mode wakeup timings characteristics(1) (2)

Symbol	Parameter	Typ	Unit
t_{Sleep}	Wakeup from Sleep mode	1.29	us
	Wakeup from Sleep 1 mode (NPLDO=0.9V)	1.30	
	Wakeup from Sleep 2 mode (NPLDO=0.9V and	1.32	

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Symbol	Parameter	Typ	Unit
	NPLDO in Low-driver mode)		
$t_{Deep-sleep}$	Wakeup from Deep-sleep mode (NPLDO in normal driver mode)	9.95	
	Wakeup from Deep-sleep mode (NPLDO in low driver mode)	9.93	
	Wakeup from Deep-sleep 1 mode	13.74	
	Wakeup from Deep-sleep 2 mode	15.50	
$t_{Standby}$	Wakeup from Standby mode	20.92	

(1) Based on characterization, not tested in production.

(2) The wakeup time is measured from the wakeup event to the point at which the application code reads the first instruction under the below conditions: V_{DD} = V_{DDA} = 3.3 V, IRC16M = System clock = 16MHz.

4.3 Power consumption

The power measurements specified in the tables represent that code with data executing from on-chip Flash with the following specifications.

Table 4-7. Power consumption characteristics(2)(3)

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Unit
I_{DD}+I_{DDA}	Supply current (Run mode)	V_{DD} = 3.3 V, HXTAL = 8 MHz, System clock = 64 MHz, All peripherals enabled	—	9.38	—	mA
		V_{DD} = 3.3 V, HXTAL = 8 MHz, System clock = 64 MHz, All peripherals disabled	—	4.39	—	
		V_{DD} = 3.3 V, HXTAL = 8 MHz, System clock = 48 MHz, All peripherals enabled	-—	7.23	-—	
		V_{DD} = 3.3 V, HXTAL = 8 MHz, System clock = 48 MHz, All peripherals disabled	—	3.46	—	
		V_{DD} = 3.3 V, HXTAL = 8 MHz, System clock = 36 MHz, All peripherals enabled	—	5.06	—	
		V_{DD} = 3.3 V, HXTAL = 8 MHz, System clock = 36 MHz, All peripherals disabled	-—	2.2	-—	
		V_{DD} = 3.3 V, HXTAL = 8 MHz, System clock = 24 MHz, All peripherals enabled	—	4.47	—	
		V_{DD} = 3.3 V, HXTAL = 8 MHz, System clock = 24 MHz, All peripherals disabled	—	2.54	—	
		V_{DD} = 3.3 V, HXTAL = 8 MHz, System clock = 16 MHz, All peripherals enabled	-—	3.24	-—	
		V_{DD} = 3.3 V, HXTAL = 8 MHz, System clock = 16 MHz, All peripherals disabled	—	1.92	—	
		V_{DD} = 3.3 V, HXTAL = 8 MHz, System clock = 8 MHz, All peripherals enabled	—	1.98	—	
		V_{DD} = 3.3 V, HXTAL = 8 MHz, System clock = 8 MHz, All peripherals disabled	-—	1.29	-—	
		V_{DD} = 3.3 V, HXTAL = 8 MHz, System clock = 4 MHz, All peripherals enabled	—	1.36	—	

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Symbol	Parameter	Conditions	Min	Typ(1)	Max	Unit
		V_{DD} = 3.3 V, HXTAL = 8 MHz, System clock = 4 MHz, All peripherals disabled	—	0.96	—	
		V_{DD} = 3.3 V, HXTAL = 8 MHz, System clock = 2 MHz, All peripherals enabled	—	1.04	—	
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 2 MHz, All peripherals disabled	—	0.81	—	
		V_{DD} = 3.3 V, HXTAL = 4 MHz, System clock = 1 MHz, All peripherals enabled	—	0.9	—	
		V_{DD} = 3.3 V, HXTAL = 4 MHz, System clock = 1 MHz, All peripherals disabled	—	0.75	—	
	Supply current (Run 1 mode)	V_{DD} = 3.3 V, IRC16M = 16 MHz, HCLK = 16 MHz, All peripherals enabled	—	1.91	—	mA
		V_{DD} = 3.3 V, IRC16M = 16 MHz, HCLK = 16 MHz, All peripherals disabled	—	0.77	—	
		V_{DD} = 3.3 V, IRC16M = 16 MHz, HCLK = 8 MHz, All peripherals enabled	—	1.29	—	
		V_{DD} = 3.3 V, IRC16M = 16 MHz, HCLK = 8 MHz, All peripherals disabled	—	0.69	—	
		V_{DD} = 3.3 V, IRC16M = 16 MHz, HCLK = 4 MHz, All peripherals enabled	—	0.8	—	
		V_{DD} = 3.3 V, IRC16M = 16 MHz, HCLK = 4 MHz, All peripherals disabled	—	0.47	—	
		V_{DD} = 3.3 V, IRC16M = 16 MHz, HCLK = 2 MHz, All peripherals enabled	—	0.56	—	
		V_{DD} = 3.3 V, IRC16M = 16 MHz, HCLK = 2 MHz, All peripherals disabled	—	0.36	—	
		V_{DD} = 3.3 V, IRC16M = 16 MHz, HCLK = 1 MHz, All peripherals enabled	—	0.43	—	
		V_{DD} = 3.3 V, IRC16M = 16 MHz, HCLK = 1 MHz, All peripherals disabled	—	0.3	—	
	Supply current (Run 2 mode)	V_{DD} = 3.3 V, HXTAL = 16 MHz, HCLK = 2 MHz, All peripherals enabled	—	0.45	—	
		V_{DD} = 3.3 V, HXTAL = 16 MHz, HCLK = 2 MHz, All peripherals disabled	—	0.25	—	
		V_{DD} = 3.3 V, HXTAL = 16 MHz, HCLK = 1 MHz, All peripherals enabled	—	0.35	—	
		V_{DD} = 3.3 V, HXTAL = 16 MHz, HCLK = 1 MHz, All peripherals disabled	—	0.22	—	
	Supply current (Sleep mode)	V_{DD} = 3.3 V, HXTAL = 8 MHz, CPU clock off, System clock = 64 MHz, All peripherals enabled	—	7.73	—	mA

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Symbol	Parameter	Conditions	Min	Typ(1)	Max	Unit
		V_{DD} = 3.3 V, HXTAL = 8 MHz, CPU clock off, System clock = 64 MHz, All peripherals disabled	—	2.33	—	
		V_{DD} = 3.3 V, HXTAL = 8 MHz, CPU clock off, System clock = 48 MHz, All peripherals enabled	—	5.99	—	
		V_{DD} = 3.3 V, HXTAL = 8 MHz, CPU clock off, System clock = 48 MHz, All peripherals disabled	—	1.92	—	
		V_{DD} = 3.3 V, HXTAL = 8 MHz, CPU clock off, System clock = 36 MHz, All peripherals enabled	—	4.68	—	
		V_{DD} = 3.3 V, HXTAL = 8 MHz, CPU clock off, System clock = 36 MHz, All peripherals disabled	—	1.6	—	
		V_{DD} = 3.3 V, HXTAL = 8 MHz, CPU clock off, System clock = 24 MHz, All peripherals enabled	—	3.38	—	
		V_{DD} = 3.3 V, HXTAL = 8 MHz, CPU clock off, System clock = 24 MHz, All peripherals disabled	—	1.29	—	
		V_{DD} = 3.3 V, HXTAL = 8 MHz, CPU clock off, System clock = 16 MHz, All peripherals enabled	—	2.51	—	
		V_{DD} = 3.3 V, HXTAL = 8 MHz, CPU clock off, System clock = 16 MHz, All peripherals disabled	—	1.09	—	
		V_{DD} = 3.3 V, HXTAL = 8 MHz, CPU clock off, System clock = 8 MHz, All peripherals enabled	—	1.62	—	
		V_{DD} = 3.3 V, HXTAL = 8 MHz, CPU clock off, System clock = 8 MHz, All peripherals disabled	—	0.86	—	
		V_{DD} = 3.3 V, HXTAL = 8 MHz, CPU clock off, System clock = 4 MHz, All peripherals enabled	—	1.18	—	
		V_{DD} = 3.3 V, HXTAL = 8 MHz, CPU clock off, System clock = 4 MHz, All peripherals disabled	—	0.75	—	
		V_{DD} = 3.3 V, HXTAL = 8 MHz, CPU clock off, System clock = 2 MHz, All peripherals enabled	—	0.94	—	

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Symbol	Parameter	Conditions	Min	Typ(1)	Max	Unit
		V_{DD} = 3.3 V, HXTAL = 8 MHz, CPU clock off, System clock = 2 MHz, All peripherals disabled	—	0.7	—	
		V_{DD} = 3.3 V, HXTAL = 4 MHz, CPU clock off, System clock = 1 MHz, All peripherals enabled	-—	0.86	-—	
		V_{DD} = 3.3 V, HXTAL = 4 MHz, CPU clock off, System clock = 1 MHz, All peripherals disabled	—	0.7	—	
	Supply current (Sleep 1 mode)	V_{DD} = 3.3 V, IRC16M = 16 MHz, CPU clock off, HCLK = 16 MHz, All peripherals enabled	—	1.74	—	
		V_{DD} = 3.3 V, IRC16M = 16 MHz, CPU clock off, HCLK = 16 MHz, All peripherals disabled	-—	0.52	-—	
		V_{DD} = 3.3 V, IRC16M = 16 MHz, CPU clock off, HCLK = 8 MHz, All peripherals enabled	—	1.03	—	
		V_{DD} = 3.3 V, IRC16M = 16 MHz, CPU clock off, HCLK = 8 MHz, All peripherals disabled	—	0.38	—	
		V_{DD} = 3.3 V, IRC16M = 16 MHz, CPU clock off, HCLK = 4 MHz, All peripherals enabled	—	0.67	—	
		V_{DD} = 3.3 V, IRC16M = 16 MHz, CPU clock off, HCLK = 4 MHz, All peripherals disabled	-—	0.31	-—	
		V_{DD} = 3.3 V, IRC16M = 16 MHz, CPU clock off, HCLK = 2 MHz, All peripherals enabled	—	0.49	—	
		V_{DD} = 3.3 V, IRC16M = 16 MHz, CPU clock off, HCLK = 2 MHz, All peripherals disabled	—	0.28	—	
		V_{DD} = 3.3 V, IRC16M = 16 MHz, CPU clock off, HCLK = 1 MHz, All peripherals enabled	-—	0.4	-—	
		V_{DD} = 3.3 V, IRC16M = 16 MHz, CPU clock off, HCLK = 1 MHz, All peripherals disabled	—	0.26	—	
	Supply current (Sleep 2 mode)	V_{DD} = 3.3 V, IRC16M = 16 MHz, CPU clock off, HCLK = 2 MHz, All peripherals enabled	—	0.43	—	mA
		V_{DD} = 3.3 V, IRC16M = 16 MHz, CPU clock off, HCLK = 2 MHz, All peripherals disabled	—	0.22	—	
		V_{DD} = 3.3 V, IRC16M = 16 MHz, CPU clock off, HCLK = 1 MHz, All peripherals enabled	—	0.34	—	
		V_{DD} = 3.3 V, IRC16M = 16 MHz, CPU clock off, HCLK = 1 MHz, All peripherals disabled	—	0.21	—	
	Supply current (Deep-sleep mode)	V_{DD} = 3.3 V, NPLDO in Low driver mode, IRC40K off, RTC off, All GPIOs analog mode	—	40.09	—	μA

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Symbol	Parameter	Conditions	Min	Typ(1)	Max	Unit
	Supply current (Deep-sleep 1 mode)	V_{DD} = 3.3 V, NPLDO off, LPLDO on, IRC40K off, RTC off, All GPIOs analog mode	—	3.144	—	
	Supply current (Deep-sleep 2 mode)	V_{DD} = 3.3 V, NPLDO off, LPLDO on, COREOFF0/SRAM1/COREOFF1 off, IRC40K off, RTC off, All GPIOs analog mode	—	1.702	—	
	Supply current (Standby mode)	V_{DD} = 3.3 V, LXTAL off, IRC32K off, RTC off	—	0.442	—	μA
$I_{LXTAL+RTC}$	LXTAL+RTC current	V_{DD} off, V_{BAT} = 3.6V, LXTAL on with external crystal, RTC on, Higher driving	—	1.22	—	μA
		V_{DD} off, V_{BAT} = 3.3V, LXTAL on with external crystal, RTC on, Higher driving	—	1.09	—	μA
		V_{DD} off, V_{BAT} = 2.6V, LXTAL on with external crystal, RTC on, Higher driving	—	0.93	—	μA
		V_{DD} off, V_{BAT} = 1.71V, LXTAL on with external crystal, RTC on, Higher driving	—	0.79	—	μA
		V_{DD} off, V_{BAT} = 3.6V, LXTAL on with external crystal, RTC on, Medium High driving	—	1.09	—	μA
		V_{DD} off, V_{BAT} = 3.3V, LXTAL on with external crystal, RTC on, Medium High driving	—	0.97	—	μA
		V_{DD} off, V_{BAT} = 2.6V, LXTAL on with external crystal, RTC on, Medium High driving	—	0.8	—	μA
		V_{DD} off, V_{BAT} = 1.71V, LXTAL on with external crystal, RTC on, Medium High driving	—	0.66	—	μA
		V_{DD} off, V_{BAT} = 3.6V, LXTAL on with external crystal, RTC on, Medium Low driving	—	0.92	—	μA
		V_{DD} off, V_{BAT} = 3.3V, LXTAL on with external crystal, RTC on, Medium Low driving	—	0.79	—	μA
		V_{DD} off, V_{BAT} = 2.6V, LXTAL on with external crystal, RTC on, Medium Low driving	—	0.63	—	μA
		V_{DD} off, V_{BAT} = 1.71V, LXTAL on with external crystal, RTC on, Medium Low driving	—	0.49	—	μA
		V_{DD} off, V_{BAT} = 3.6V, LXTAL on with external crystal, RTC on, Low driving	—	0.87	—	μA
		V_{DD} off, V_{BAT} = 3.3V, LXTAL on with	—	0.74	—	μA

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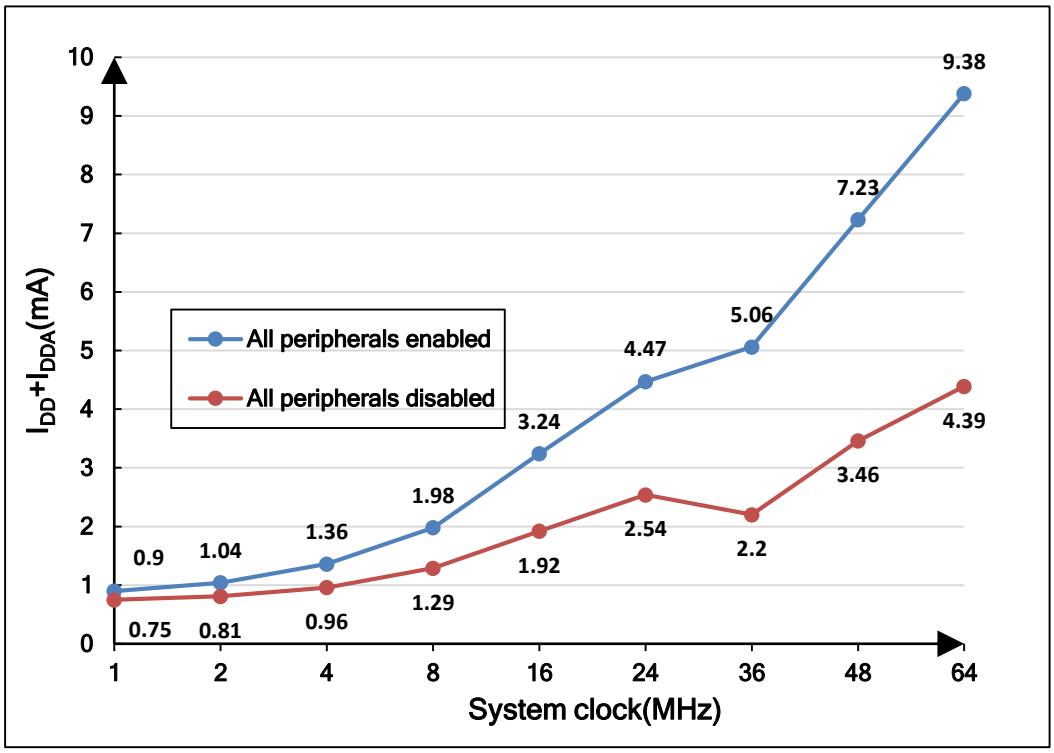
Symbol	Parameter	Conditions	Min	Typ(1)	Max	Unit
		external crystal, RTC on, Low driving				
		V_{DD} off, V_{BAT} = 2.6V, LXTAL on with external crystal, RTC on, Low driving	—	0.57	—	μA
		V_{DD} off, V_{BAT} = 1.71V, LXTAL on with external crystal, RTC on, Low driving	—	0.43	—	μA

(1) Based on characterization, not tested in production.

(2) When analog peripheral blocks such as ADCs, HXTAL, LXTAL, IRC8M, or IRC40K are ON, an additional power consumption should be considered.

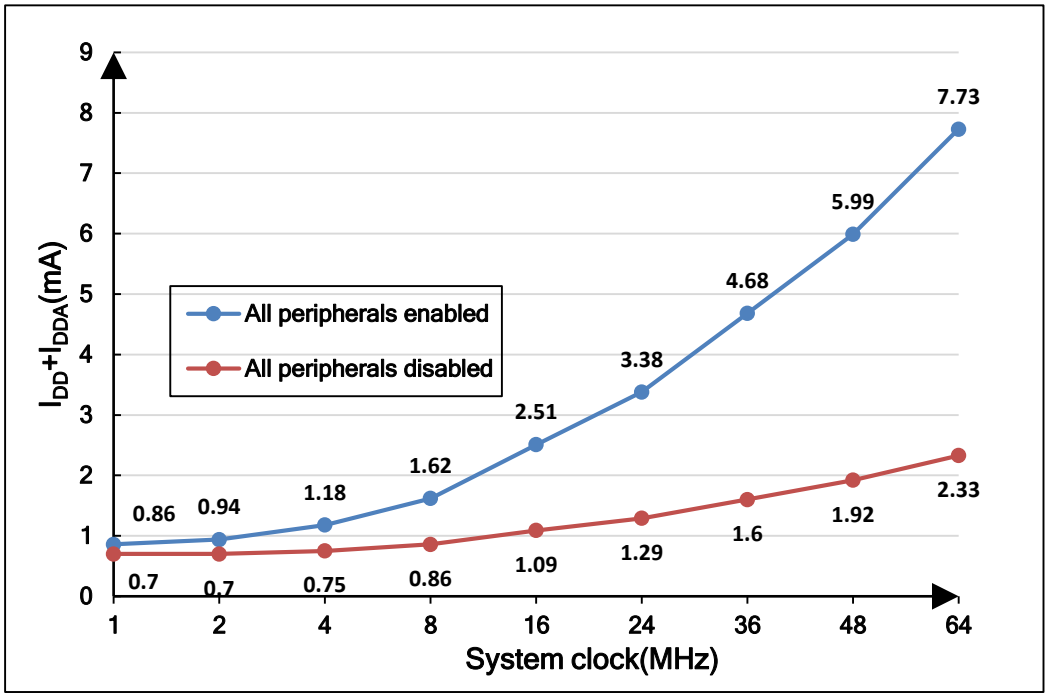
(3) The system clock 36MHZ (inclusive) to 64MHZ (inclusive) adopts FMC_WAIT_STATE_1, the system clock 24MHZ (inclusive) to 1MHZ (inclusive) adopts FMC_WAIT_STATE_0.

Figure 4-2. Typical supply current consumption in Run mode



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Figure 4-3. Typical supply current consumption in Sleep mode



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4.4 EMC characteristics

EMS (electromagnetic susceptibility) includes ESD (Electrostatic discharge, positive and negative) and FTB (Burst of Fast Transient voltage, positive and negative) testing result is given in ***Table 4-8. EMS characteristics***, based on the EMS levels and classes compliant with IEC 61000 series standard.

Table 4-8. EMS characteristics(1)

Symbol	Parameter	Conditions	Level/Class
V_{ESD}	Voltage applied to all device pins to induce a functional disturbance	V_{DD} = 3.3 V, LQFP64, f_{HCLK} = 64 MHz conforms to IEC 61000-4-2	3A
V_{FTB}	Fast transient voltage burst applied to induce a functional disturbance through 100 pF on V_{DD} and V_{SS} pins	V_{DD} = 3.3 V, LQFP64, f_{HCLK} = 64 MHz conforms to IEC 61000-4-4	4A

(1) Based on characterization, not tested in production.

EMI (Electromagnetic Interference) emission test result is given in the ***Table 4-9. EMI characteristics***(1), The electromagnetic field emitted by the device are monitored while an application, executing EEMBC code, is running. The test is compliant with SAE J1752-3:2017 standard which specifies the test board and the pin loading.

Table 4-9. EMI characteristics(1)

Symbol	Parameter	Conditions	Tested frequency band	Max vs. [f_{HXTAL}/f_{HCLK}] 8/64 MHz	Unit
S_{EMI}	Peak level	V_{DD} = 3.6 V, T_A = +25 °C, LQFP64, f_{HCLK} = 64 MHz, conforms to SAE J1752-3:2017	0.15 MHz to 30 MHz	-11.89	dBµV
			30 MHz to 130 MHz	-1.54	
			130 MHz to 1 GHz	3.05	

(1) Based on characterization, not tested in production.

4.5 Power supply supervisor characteristics

Table 4-10. Power supply supervisor characteristics(1)

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{LVD}(1)	Low Voltage Detector Threshold	LVDT[2:0] = 000, rising edge	—	2.15	—	V
		LVDT[2:0] = 000, falling edge	—	2.05	—	V
		LVDT[2:0] = 001, rising edge	—	2.30	—	V
		LVDT[2:0] = 001, falling edge	—	2.20	—	V
		LVDT[2:0] = 010, rising edge	—	2.45	—	V
		LVDT[2:0] = 010, falling edge	—	2.35	—	V
		LVDT[2:0] = 011, rising edge	—	2.60	—	V
		LVDT[2:0] = 011, falling edge	—	2.50	—	V
		LVDT[2:0] = 100, rising edge	—	2.75	—	V
		LVDT[2:0] = 100, falling edge	—	2.65	—	V
		LVDT[2:0] = 101, rising edge	—	2.90	—	V
		LVDT[2:0] = 101, falling edge	—	2.80	—	V
		LVDT[2:0] = 110, rising edge	—	3.00	—	V
		LVDT[2:0] = 110, falling edge	—	2.90	—	V
$V_{LVDhyst}$(2)	LVD hysteresis	—	—	100	—	mV
V_{BOR0}	Brown-out reset threshold 0	rising edge	—	1.60	—	V
		falling edge	—	1.56	—	
V_{BOR1}	Brown-out reset threshold 1	rising edge	—	2.10	—	V
		falling edge	—	2.00	—	
V_{BOR2}	Brown-out reset threshold 2	rising edge	—	2.30	—	V
		falling edge	—	2.20	—	
V_{BOR3}	Brown-out reset threshold 3	rising edge	—	2.60	—	V
		falling edge	—	2.50	—	
V_{BOR4}	Brown-out reset threshold 4	rising edge	—	2.90	—	V
		falling edge	—	2.80	—	
V_{POR}(1)	Power on reset threshold	—	1.56	1.60	1.63	V
V_{PDR}(1)	Power down reset threshold		1.52	1.56	1.59	V
$V_{PDRhyst}$(2)	PDR hysteresis		—	40	—	mV
$t_{RSTTEMPO}$(2)	Reset temporization		—	550	—	us

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

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4.6 Electrical sensitivity

The device is strained in order to determine its performance in terms of electrical sensitivity. Electrostatic discharges (ESD) are applied directly to the pins of the sample. Static latch-up (LU) test is based on the two measurement methods.

Table 4-11. ESD characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	JS-001-2017	—	—	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	JS-002-2018	—	—	500	V

(1) Based on characterization, not tested in production.

Table 4-12. Static latch-up characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
LU	I-test	JESD78	—	—	±200	mA
	V_{supply} over voltage		—	—	5.4	V

(1) Based on characterization, not tested in production.

4.7 External clock characteristics

Table 4-13. High speed external clock (HXTAL) generated from a crystal/ceramic characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HXTAL}(1)	Crystal or ceramic frequency	V_{DD} = 3.3 V	4	8	48	MHz
R_F(2)	Feedback resistor	V_{DD} = 3.3 V	—	400	—	kΩ
C_{HXTAL}(2) (3)	Recommended matching capacitance on OSCIN and OSCOUT	—	—	20	30	pF
$Ducy_{(HXTAL)}$(2)	Crystal or ceramic duty cycle	—	30	50	70	%
g_m(2)	Oscillator transconductance	Startup	—	20	—	mA/V
$I_{DD(HXTAL)}$ (1)	Crystal or ceramic operating current	V_{DD} = 3.3 V	—	0.32	—	mA
$t_{SUHXTAL}$(1)	Crystal or ceramic startup time	V_{DD} = 3.3 V	—	1.27	—	ms

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

(3) $C_{HXTAL1} = C_{HXTAL2} = 2*(C_{LOAD} - C_S)$, For C_{HXTAL1} and C_{HXTAL2}, it is recommended matching capacitance on OSCIN and OSCOUT. For C_{LOAD}, it is crystal/ceramic load capacitance, provided by the crystal or ceramic manufacturer. For C_S, it is PCB and MCU pin stray capacitance.

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Table 4-14. High speed external user clock characteristics (HXTAL in bypass mode)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HXTAL_ext}(1)	External clock source or oscillator frequency	V_{DD} = 3.3 V	1	8	50	MHz
V_{HXTALH}(2)	OSCIN input pin high level voltage	V_{DD} = 3.3 V	0.7 V_{DD}	—	V_{DD}	V
V_{HXTALL}(2)	OSCIN input pin low level voltage		V_{SS}	—	0.3 V_{DD}	
$t_{H/L(HXTAL)}$ (2)	OSCIN high or low time	—	5	—	—	ns
$t_{R/F(HXTAL)}$(2)	OSCIN rise or fall time	—	—	—	10	
C_{IN}(2)	OSCIN input capacitance	—	—	5	—	pF
$Ducy_{(HXTAL)}$ (2)	Duty cycle	—	30	50	70	%

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

Table 4-15. Low speed external clock (LXTAL) generated from a crystal/ceramic characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LXTAL}(1)	Crystal or ceramic frequency	V_{DD} = 3.3 V	—	32.768	—	kHz
C_{LXTAL}(2)(3)	Recommended matching capacitance on OSC32IN and OSC32OUT	—	—	10	—	pF
$Ducy_{(LXTAL)}$(2)	Crystal or ceramic duty cycle	—	30	—	70	%
g_m(2)	Oscillator transconductance	Lower driving capability	—	3.6	—	μA/V
		Medium low driving capability	—	4.8	—	
		Medium high driving capability	—	8.4	—	
		Higher driving capability	—	10.8	—	
$I_{DDLXTAL}$ (1)	Crystal or ceramic operating current	Lower driving capability	—	332	—	nA
		Medium low driving capability	—	392	—	
		Medium high driving capability	—	562	—	
		Higher driving capability	—	692	—	
$t_{SULXTAL}$(1)(4)	Crystal or ceramic startup time	V_{DD} = 3.3 V	—	0.32	—	s

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

(3) $C_{LXTAL1} = C_{LXTAL2} = 2*(C_{LOAD} - C_S)$, For C_{LXTAL1} and C_{LXTAL2}, it is recommended matching capacitance on OSC32IN and OSC32OUT. For C_{LOAD}, it is crystal/ceramic load capacitance, provided by the crystal or ceramic manufacturer. For C_S, it is PCB and MCU pin stray capacitance.

(4) $t_{SULXTAL}$ is the startup time measured from the moment it is enabled (by software) to the 32.768 kHz oscillator stabilization flags is SET. This value varies significantly with the crystal manufacturer.

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Table 4-16. Low speed external user clock characteristics (LXTAL in bypass mode)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LXTAL_ext}(1)	External clock source or oscillator frequency	V_{DD} = 3.3 V	—	32.768	1000	kHz
V_{LXTALH}(2)	OSC32IN input pin high level voltage	V_{DD} = 3.3 V	0.7 V_{DD}	—	V_{DD}	V
V_{LXTALL}(2)	OSC32IN input pin low level voltage		V_{SS}	—	0.3 V_{DD}	
$t_{H/L(LXTAL)}$ (2)	OSC32IN high or low time	—	250	—	—	ns
$t_{R/F(LXTAL)}$ (2)	OSC32IN rise or fall time	—	—	—	50	
C_{IN}(2)	OSC32IN input capacitance	—	—	5	—	pF
$Ducy_{(LXTAL)}$ (2)	Duty cycle	—	30	50	70	%

(1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.

4.8 Internal clock characteristics

Table 4-17. High speed internal clock (IRC16M) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{IRC16M}	High Speed Internal Oscillator (IRC16M) frequency	V_{DD} = V_{DDA} = 3.3 V	—	16	—	MHz
ACC_{IRC16M}	IRC16M oscillator Frequency accuracy, Factory-trimmed	V_{DD} = V_{DDA} = 3.3 V, T_A = -40 °C ~ +85 °C	—	-1.5 to 1.5(1)	—	%
		V_{DD} = V_{DDA} = 3.3 V	-1.0	—	+1.0	%
	IRC16M oscillator Frequency accuracy, User trimming step(1)	—	—	0.3(1)	—	%
D_{IRC16M}(2)	IRC16M oscillator duty cycle	V_{DD} = V_{DDA} = 3.3 V	45	50	55	%
$I_{DDIRC16M}$(1)	IRC16M oscillator operating current	V_{DD} = V_{DDA} = 3.3 V, f_{IRC8M} = 16 MHz	—	110	—	μA
$t_{SUIRC16M}$(1)	IRC16M oscillator startup time	V_{DD} = V_{DDA} = 3.3 V, f_{IRC8M} = 16 MHz	—	0.75	—	μs

(1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.

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Table 4-18. Low speed internal clock (IRC32K) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{IRC32K}	Low Speed Internal oscillator (IRC32K) frequency	V_{DD} = V_{DDA} = 3.3 V, T_A = -40~85 °C(2)		31.7 to 32.3		kHz
		V_{DD} = V_{DDA} = 3.3 V	30		35	
$I_{DDAIRC32K}$(2)	IRC32K oscillator operating current	V_{DD} = V_{DDA} = 3.3 V	—	160	—	nA
$t_{SUIRC32K}$(2)	IRC32K oscillator startup time	V_{DD} = V_{DDA} = 3.3 V	—	40	—	μs

(1) Guaranteed by design, not tested in production.

(2) Based on characterization, not tested in production.

Table 4-19. High speed internal clock (IRC48M) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{IRC48M}	High Speed Internal Oscillator (IRC48M) frequency	V_{DD} = V_{DDA} = 3.3 V	—	48	—	MHz
ACC_{IRC48M}	IRC48M oscillator Frequency accuracy, Factory-trimmed	V_{DD} = V_{DDA} = 3.3 V, T_A = -40 °C ~ +85 °C	—	-3.3 to -0.25(1)	—	%
		V_{DD} = V_{DDA} = 3.3 V	-2.0	—	+2.0	%
	IRC48M oscillator Frequency accuracy, User trimming step	—	—	0.12	—	%
D_{IRC48M}(2)	IRC48M oscillator duty cycle	V_{DD} = V_{DDA} = 3.3 V	45	50	55	%
$I_{DDAIRC48M}$(1)	IRC48M oscillator operating current	V_{DD} = V_{DDA} = 3.3 V, f_{IRC28M} = 48 MHz	—	327	—	μA
$t_{SUIRC48M}$(1)	IRC48M oscillator startup time	V_{DD} = V_{DDA} = 3.3 V, f_{IRC28M} = 48 MHz	—	1.8	—	μs

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

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4.9 PLL characteristics

Table 4-20. PLL characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLLIN}(1)	PLL input clock frequency	—	2	—	16	MHz
f_{PLLOUT}(2)	PLL output clock frequency	—	16	—	64	MHz
f_{VCO}(2)	PLL VCO output clock frequency	—	—	—	64	MHz
t_{LOCK}(2)	PLL lock time	—	—	—	200	μs
I_{DD}(1)	Current consumption on V_{DD}	VCO freq = 64 MHz	—	400	—	μA
$Jitter_{PLL}$(3)	Cycle to cycle Jitter（rms）	System clock	—	120	—	ps
	Cycle to cycle Jitter（peak to peak）		—	900	—	

(1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.
(3) Value given with main PLL running.

4.10 Memory characteristics

Table 4-21. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PE_{CYC}(1)	Number of guaranteed program /erase cycles before failure (Endurance)	T_A = -40 °C ~ +85 °C	10	—	—	kcycles
t_{RET}(1)	Data retention time	10k cycles at T_A = 85 °C	10	—	—	years
t_{PROG}(2)	Word programming time	T_A = -40 °C ~ + 85 °C	—	37.5	—	μs
t_{ERASE}(2)	Page erase time	T_A = -40 °C ~ + 85 °C	—	11	—	ms
t_{MERASE}(2)	Mass erase time	T_A = -40 °C ~ + 85°C	—	12	—	ms

(1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.

4.11 NRST pin characteristics

Table 4-22. NRST pin characteristics

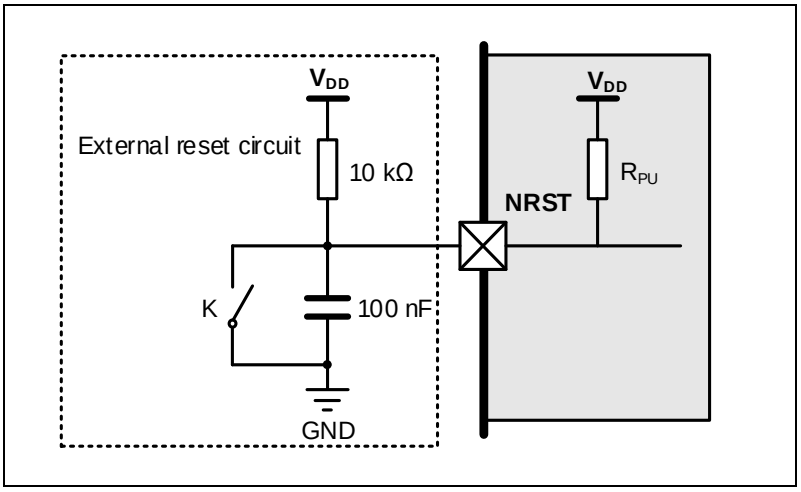
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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$ (1)	NRST Input low level voltage	1.71 V ≤ V_{DD} = V_{DDA} ≤ 3.63 V	-0.5	—	0.35 V_{DD}	V
$V_{IH(NRST)}$ (1)	NRST Input high level voltage		0.65 V_{DD}	—	V_{DD} + 0.5	
V_{hyst}(1)	Schmidt trigger Voltage hysteresis		—	400	—	mV
R_{pu}(2)	Pull-up equivalent resistor	—	—	40	—	kΩ

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

Figure 4-4. Recommended external NRST pin circuit



4.12 VREF buffer characteristics

Table 4-23. VREF buffer characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}(1)	Analog Supply Voltage	—	2.7	3.3	3.63	V
V_{REF}	Output Reference Voltage	V_{DDA} = 3.3 V	2.49	2.50	2.51	V
		All V_{DDA}, All Temp(2)	2.47	2.50	2.53	
PSRR(1)	Power Supply Rejection	DC (I_O = 0)	—	57	—	dB
		DC (I_O = 200 μA)	—	57	—	
T_{SU}(1)	Setup Time	C_L = 1 μF + 10 nF	—	—	200	μs
I_{LOAD_R}(1)	Load Regulation	I_{LOAD} from 0 to 200 μA	—	5	—	μV/μA
C_{LOAD}(1)	Load Capacitor	—	—	1	—	μF
TRIM(1)	Trim Step	—	—	3	—	mV

(1). Guaranteed by design, not tested in production.

(2). Based on characterization, not tested in production.

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4.13 GPIO characteristics

Table 4-24. I/O port DC characteristics(1)(3)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Standard IO Low level input voltage	1.71 V ≤ V_{DD} = V_{DDA} ≤ 3.63 V	—	—	0.3 V_{DD}	V
	5V-tolerant IO Low level input voltage	1.71 V ≤ V_{DD} = V_{DDA} ≤ 3.63 V	—	—	0.3 V_{DD}	
V_{IH}	Standard IO High level input voltage	1.71 V ≤ V_{DD} = V_{DDA} ≤ 3.63 V	0.7 V_{DD}	—	—	
	5 V-tolerant IO High level input voltage	1.71 V ≤ V_{DD} = V_{DDA} ≤ 3.63 V	0.7 V_{DD}	—	—	
V_{OL} (IO_speed=50MHz)	Low level output voltage for an IO Pin (I_{IO} = +8 mA)	V_{DD} = 1.71 V	—	0.26	—	V
		V_{DD} = 3.3 V	—	0.13	—	
		V_{DD} = 3.6 V	—	0.13	—	
	(I_{IO} = +10 mA)	V_{DD} = 1.71 V	—	0.20	—	
	Low level output voltage for an IO Pin (I_{IO} = +20 mA)	V_{DD} = 3.3 V	—	0.33	—	
		V_{DD} = 3.6 V	—	0.32	—	
V_{OH} (IO_speed=50MHz)	High level output voltage for an IO Pin (I_{IO} = +8 mA)	V_{DD} = 1.71V	—	1.46	—	
		V_{DD} = 3.3 V	—	3.15	—	
		V_{DD} = 3.6 V	—	3.45	—	
	(I_{IO} = +10 mA)	V_{DD} = 1.71 V	—	1.38	—	V
	High level output voltage for an IO Pin (I_{IO} = +20 mA)	V_{DD} = 3.3 V	—	2.91	—	
		V_{DD} = 3.6 V	—	3.22	—	
V_{OL} (IO_speed=10MHz)	(I_{IO} = +4 mA)	V_{DD} = 1.71 V	—	0.31	—	V
	Low level output voltage for an IO Pin (I_{IO} = +8 mA)	V_{DD} = 3.3 V	—	0.36	—	
		V_{DD} = 3.6 V	—	0.35	—	
	Low level output voltage for an IO Pin (I_{IO} = +15 mA)	V_{DD} = 1.71 V	—	—	—	
		V_{DD} = 3.3 V	—	0.73	—	
		V_{DD} = 3.6 V	—	0.70	—	
V_{OH} (IO_speed=10MHz)	(I_{IO} = +4 mA)	V_{DD} = 1.71 V	—	1.33	—	V
	High level output voltage for an IO Pin (I_{IO} = +8 mA)	V_{DD} = 3.3 V	—	2.87	—	
		V_{DD} = 3.6 V	—	3.19	—	
	High level output voltage for an IO Pin (I_{IO} = +15 mA)	V_{DD} = 1.71 V	—	—	—	
		V_{DD} = 3.3 V	—	2.42	—	
		V_{DD} = 3.6 V	—	2.78	—	
V_{OL}	(I_{IO} = +1 mA)	V_{DD} = 1.71 V	—	0.32	—	V

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
(IO_speed=2MHz)	Low level output voltage for an IO Pin (I_{IO} = +4 mA)	V_{DD} = 3.3 V	—	0.55	—	
		V_{DD} = 3.6 V	—	0.53	—	
V_{OH} (IO_speed=2MHz)	(I_{IO} = +1 mA)	V_{DD} = 1.71 V	—	1.32	—	
	High level output voltage for an IO Pin (I_{IO} = +4 mA)	V_{DD} = 3.3 V	—	2.65	—	
		V_{DD} = 3.6 V	—	2.99	—	
R_{PU}(2)	Internal pull-up resistor	—	—	40	—	kΩ
R_{PD}(2)	Internal pull-down resistor	—	—	40	—	kΩ

(1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.
(3) All pins except PC13 / PC14 / PC15. Since PC13 to PC15 are supplied through the Power Switch, which can only be obtained by a small current, the speed of GPIOs PC13 to PC15 should not exceed 2 MHz when they are in output mode(maximum load: 30 pF).

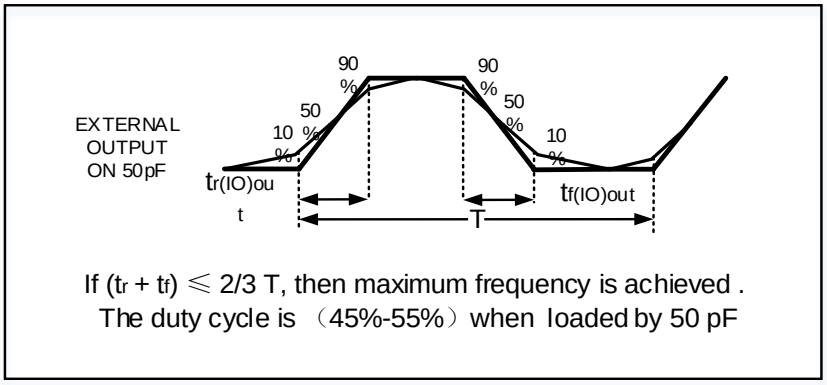
Table 4-25. I/O port AC characteristics(1)

GPIOx_OSPD[1:0] bit value(2)	Parameter	Conditions	Max	Unit
GPIOx_OSPD->OSPDy[1:0] = X0 （IO_Speed = 2 MHz）	Maximum frequency	1.71 ≤ V_{DD} ≤ 3.63 V, C_L = 10 pF	6	MHz
		1.71 ≤ V_{DD} ≤ 3.63 V, C_L = 30 pF	5	
		1.71≤ V_{DD} ≤ 3.63 V, C_L = 50 pF	4	
GPIOx_OSPD->OSPDy[1:0] = 01 （IO_Speed = 10 MHz）	Maximum frequency	1.71 ≤ V_{DD} ≤ 3.63 V, C_L = 10 pF	17	MHz
		1.71 ≤ V_{DD} ≤ 3.63 V, C_L = 30 pF	14	
		1.71 ≤ V_{DD} ≤ 3.63 V, C_L = 50 pF	12	
GPIOx_OSPD->OSPDy[1:0] = 11 （IO_Speed = 50 MHz）	Maximum frequency	1.71 ≤ V_{DD} ≤ 3.63 V, C_L = 10 pF	81	MHz
		1.71 ≤ V_{DD} ≤ 3.63 V, C_L = 30 pF	72	
		1.71 ≤ V_{DD} ≤ 3.63 V, C_L = 50 pF	60	

(1) Based on characterization, not tested in production.
(2) The I/O speed is configured using the GPIOx_OSPD->OSPDy [1:0] bits. Refer to the GD32L233 user manual which is selected to set the GPIO port output speed.

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Figure 4-5. I/O port AC characteristics definition



4.14 ADC characteristics

Table 4-26. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}(1)	Operating voltage	—	1.8	3.3	3.6	V
V_{IN}(1)	ADC input voltage range	—	0	—	V_{DDA}	V
f_{ADC}(1)	ADC clock	—	0.125	—	16	MHz
f_S(1)	Sampling rate	12-bit	0.008	—	1.067	MSPS
		10-bit	0.009	—	1.23	
		8-bit	0.011	—	1.45	
		6-bit	0.013	—	1.78	
V_{AIN}1)	Analog input voltage	16 external; 4 internal	0	—	V_{DDA}	V
R_{AIN}(2)	External input impedance	See ***Equation 1***	—	—	513.6	kΩ
R_{ADC}(2)	Input sampling switch resistance	—	—	—	0.5	kΩ
C_{ADC}(2)	Input sampling capacitance	No pin/pad capacitance included	—	—	3	pF
t_{CAL}(2)	Calibration time	f_{ADC} = 16 MHz	—	13.4	—	µs
t_s(2)	Sampling time	f_{ADC} = 16 MHz	0.156	—	14.97	µs
t_{CONV}(2)	Total conversion time(including sampling time)	12-bit	—	15	—	1/f_{ADC}
		10-bit	—	13	—	
		8-bit	—	11	—	
		6-bit	—	9	—	
$I_{DDA(ADC)}$	ADC consumption from V_{DDA}	f_S = 1M	—	133	—	uA
		f_S = 0.5M	—	77	—	
		f_S = 10k	—	17.5	—	
$I_{DDV(ADC)}$	ADC consumption from V_{REFP}	f_S = 1M	—	14.7	—	uA
		f_S = 0.5M	—	7.6	—	
		f_S = 10k	—	0.4	—	
t_{SU}(2)	Startup time	—	—	5	—	us

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(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

Equation 1: R_{AIN} max formula $R_{AIN} < \frac{T_s}{f_{ADC} * C_{ADC} * \ln(2^{N+2})} - R_{ADC}$

The formula above (***Equation 1***) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

Table 4-27. ADC R_{AIN} max for f_{ADC} = 16 MHz(1)

T_s(cycles)	t_s(μs)	R_{AINmax} (kΩ)
2.5	0.16	4.8
7.5	0.47	15.6
13.5	0.85	28.4
28.5	1.79	60.6
41.5	2.60	88.5
55.5	3.47	118.6
71.5	4.47	153.0
239.5	14.97	513.6

(1) Based on characterization, not tested in production.

Table 4-28. ADC dynamic accuracy at f_{ADC} = 16 MHz(1)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ENOB	Effective number of bits	f_{ADC} = 16 MHz	10.8	11.2	—	bits
SNDR	Signal-to-noise and distortion ratio	V_{DDA} = V_{REF+} = 3.3 V	66.7	69.1	—	dB
SNR	Signal-to-noise ratio	Input Frequency = 20 kHz	66.9	69.3	—	
THD	Total harmonic distortion		—	-82	-78	

(1) Based on characterization, not tested in production.

Table 4-29. ADC static accuracy at f_{ADC} = 16 MHz(1)

Symbol	Parameter	Test conditions	Typ	Max	Unit
Offset	Offset error	f_{ADC} = 16 MHz V_{DDA} = V_{REF+} = 3.3 V	—	—	LSB
DNL	Differential linearity error		±0.6	±1	
INL	Integral linearity error		±0.8	±1.5	

(1) Based on characterization, not tested in production.

Table 4-30. ADC dynamic accuracy at f_{ADC} = 16 MHz(1)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ENOB	Effective number of bits	f_{ADC} = 16 MHz	10.7	11.2	—	bits
SNDR	Signal-to-noise and distortion ratio	V_{DDA} = 3.3V V_{REF+} = 2.5 V	66.2	69.1	—	dB
SNR	Signal-to-noise ratio		66.4	69.3	—	
THD	Total harmonic distortion	Input Frequency = 20 kHz	—	-82	-78	

(1) Based on characterization, not tested in production.

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Table 4-31. ADC static accuracy at f_{ADC} = 16 MHz(1)

Symbol	Parameter	Test conditions	Typ	Max	Unit
Offset	Offset error	f_{ADC} = 16 MHz, V_{DDA} = 3.3V V_{REF+} = 2.5 V	—	—	LSB
DNL	Differential linearity error		±0.6	±1	
INL	Integral linearity error		±0.8	±1.5	

(1) Based on characterization, not tested in production.

Table 4-32. ADC dynamic accuracy at f_{ADC} = 16 MHz(1)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ENOB	Effective number of bits	f_{ADC} = 16 MHz, V_{DDA} = V_{REF+} = 1.8 V Input Frequency = 20 kHz	10.5	10.8	—	bits
SNDR	Signal-to-noise and distortion ratio		64.9	66.7	—	dB
SNR	Signal-to-noise ratio		65.1	66.9	—	
THD	Total harmonic distortion		—	-71	-68	

(1) Based on characterization, not tested in production.

Table 4-33. ADC static accuracy at f_{ADC} = 16 MHz(1)

Symbol	Parameter	Test conditions	Typ	Max	Unit
Offset	Offset error	f_{ADC} = 16 MHz, V_{DDA} = V_{REF+} = 1.8 V	—	—	LSB
DNL	Differential linearity error		±0.8	±1	
INL	Integral linearity error		±1	±1.5	

(1) Based on characterization, not tested in production.

4.15 DAC characteristics

Table 4-34. DAC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}(1)	Operating voltage	—	1.71	3.3	3.63	V
V_{REF+}(2)	Positive Reference Voltage	—	1.71	—	V_{DDA}	V
V_{REF-}(2)	Negative Reference Voltage	—	—	V_{SSA}	—	V
R_{LOAD}(2)	Resistive load	Resistive load with buffer ON	5	—	—	kΩ
Ro(2)	Impedance output	Impedance output with buffer OFF	—	—	15	kΩ
C_{LOAD}(2)	Capacitive load	Capacitive load with buffer ON	—	—	50	pF
DAC_OUT min(2)	Lower DAC_OUT voltage	Lower DAC_OUT voltage with buffer ON	0.2	—	—	V
		Lower DAC_OUT voltage with buffer OFF	0.5	—	—	mV
DAC_OUT max(2)	Higher DAC_OUT voltage	Higher DAC_OUT voltage with buffer ON	—	—	V_{DDA}-0.2	V
		Higher DAC_OUT voltage with buffer OFF	—	—	V_{DDA}-1LSB	V
I_{DDA}(1)	DAC current consumption in quiescent mode	With no load, middle code(0x800) on the input,	—	400	—	μA

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		V_{REFP} = 3.3 V				
$I_{DDVREF+}$(1)	DAC current consumption in quiescent mode	With no load, middle code(0x800) on the input, V_{REFP} = 3.3 V	—	114	—	μA
DNL(1)	Differential non linearity	10-bit configuration	—	—	±0.5	LSB
		12-bit configuration	—	—	±2	
INL(1)	Integral non linearity	10-bit configuration	—	—	±1	LSB
		12-bit configuration	—	—	±4	
Offset(1)	Offset error	DAC in 12-bit mode	—	—	±12	LSB
GE(1)	Gain error	DAC in 12-bit mode	—	±0.5	—	%
$T_{setting}$(1)	Settling time	C_{LOAD} ≤ 50 pF, R_{LOAD} ≥ 5 kΩ	—	0.5	—	μs
T_{wakeup}(2)	Wakeup from off state	—	—	5	—	μs
Update rate(2)	Max frequency for a correct DAC_OUT change from code i to i±1LSB	C_{LOAD} ≤ 50 pF, R_{LOAD} ≥ 5 kΩ	—	—	4	MS/s
PSRR(2)	Power supply rejection ratio(to V_{DDA})	No R_{Load}, C_{LOAD}=50 pF	—	-80	—	dB

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

4.16 Temperature sensor characteristics

Table 4-35. Temperature sensor characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OFF}	Uncalibrated Offset	T_A = 30°C	—	1022.8	—	mV
E_{OFF}(1)	Uncalibrated Offset Error	T_A = 30°C	—	2	—	mV
M	Slope	—	—	3.3	—	mV/°C
E_M(1)	Slope Error	—	—	30	—	μV/°C
LIN(3)	Linearity	T_A = -40 °C to 85 °C	—	-0.4 to1.2	—	°C
t_{ON}	Turn-on Time	—	—	—	—	μs
ETOT(2)(3)	Temp Sensor Error Using Typical Slope and Factory-Calibrated Offset	T_A = -40 °C to 85 °C	-3.5	—	4.7	°C

(1) Represents one standard deviation from the mean.

(2) The factory-calibrated offset value is stored in the read-only area of flash in locations 0x1FFFF7F8.

(3) Based on characterization, not tested in production.

4.17 Comparators characteristics

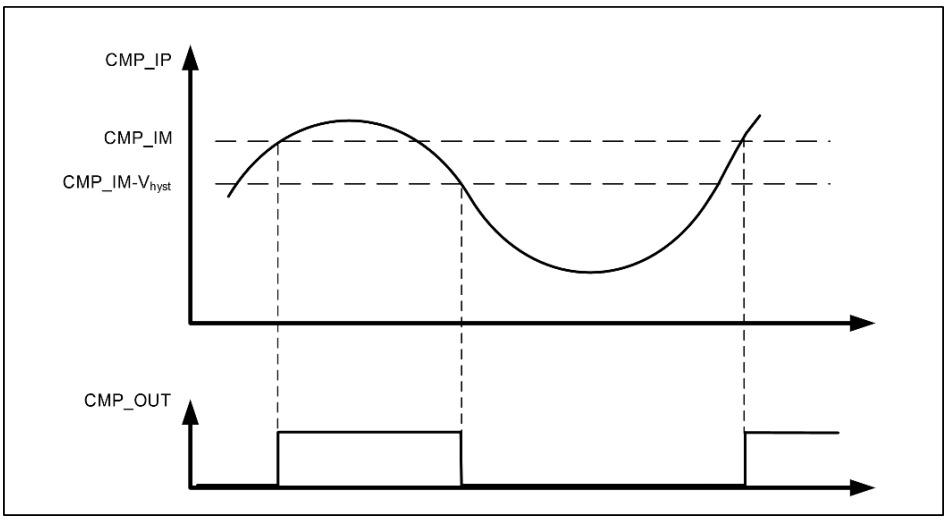
Table 4-36. CMP characteristics(1)

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Operating voltage	—	1.71	3.3	3.63	V
V_{IN}	Input voltage range	—	0	—	V_{DDA}	V
V_{BG}	Scaler input voltage	—	—	0.8	—	V
V_{SC}	Scaler offset voltage	—	—	±5	—	mV
I_{DDA}(SCALER)	Scaler static consumption from V_{DDA}	BEN=0 (bridge disable)	—	200	—	nA
		BEN=1 (bridge enable)	—	0.8	—	μA
t_{START_SCALER}	Scaler startup time	—	—	100	—	μs
t_D	Propagation delay for 200 mV step with 100 mV overdrive	Ultra low power mode	—	3.63	—	μs
		Medium power mode	—	0.18	—	μs
		High speed power mode	—	55	—	ns
I_{DD}	Current consumption	Ultra low power mode	—	0.5	—	μA
		Medium power mode	—	4.7	—	
		High speed power mode	—	47	—	
V_{offset}	Offset error	—	—	±5	—	mV
V_{hyst}	Hysteresis Voltage	No Hysteresis	—	0	—	mV
		Low Hysteresis	—	8	—	
		Medium Hysteresis	—	16	—	
		High Hysteresis	—	32	—	

(1) Based on characterization, not tested in production.

Figure 4-6. CMP hysteresis



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4.18 TIMER characteristics

Table 4-37. TIMER characteristics (1)

Symbol	Parameter	Conditions	Min	Max	Unit
t_{res}	Timer resolution time	—	1	—	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 64 MHz	15.6	—	ns
f_{EXT}	Timer external clock frequency	—	0	$f_{TIMERxCLK}/2$	MHz
		$f_{TIMERxCLK}$ = 64 MHz	0	32	MHz
RES	Timer resolution	—	—	16	bit
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected	—	1	65536	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 64 MHz	0.0156	1024	μs
t_{MAX_COUNT}	Maximum possible count	—	—	65536 × 65536	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 64 MHz	—	67.11	s

(1) Guaranteed by design, not tested in production.

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4.19 SLCD controller characteristics

Table 4-38. SLCD controller characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{SLCD}	SLCD external voltage		—	—	3.63	V
V_{SLCD0}	SLCD internal reference voltage 0		—	2.65	—	
V_{SLCD1}	SLCD internal reference voltage 1		—	2.80	—	
V_{SLCD2}	SLCD internal reference voltage 2		—	2.92	—	
V_{SLCD3}	SLCD internal reference voltage 3		—	3.08	—	
V_{SLCD4}	SLCD internal reference voltage 4		—	3.23	—	
V_{SLCD5}	SLCD internal reference voltage 5		—	3.37	—	
V_{SLCD6}	SLCD internal reference voltage 6		—	3.52	—	
V_{SLCD7}	SLCD internal reference voltage 7		—	3.67	—	
Cext	V_{SLCD} external capacitance	Buffer OFF (VODEN=0 is SLCD_CTL register)	0.2	—	2	uF
		Buffer ON (VODEN=1 is SLCD_CTL register)	1	—	2	
I_{SLCD}(2)	Supply current from VDD at V_{DD} = 2.2 V	Buffer OFF (VODEN=0 is SLCD_CTL register)	—	3.2	—	uA
	Supply current from VDD at V_{DD} = 3.0 V	Buffer OFF (VODEN=0 is SLCD_CTL register)	—	2.4	—	
I_{VSLCD}	Supply current from V_{SLCD} (V_{SLCD} = 3.0 V)	Buffer OFF (VODEN = 0, PULSE = 0)	—	0.5	—	uA
		Buffer ON (VODEN = 1, 1/2 Bias)	—	0.65	—	
		Buffer ON (VODEN = 1, 1/3 Bias)	—	0.8	—	
		Buffer ON (VODEN = 1, 1/4 Bias)	—	0.95	—	
R_{HN}	Total High Resistor value for Low drive resistive network		—	—	—	MΩ
R_{LN}	Total Low Resistor value for High drive resistive network		—	—	—	kΩ
V_{44}	Segment/Common highest level voltage		—	V_{SLCD}	—	V
V_{34}	Segment/Common 3/4 level voltage		—	3/4V_{SLCD}	—	
V_{23}	Segment/Common 2/3 level voltage		—	2/3V_{SLCD}	—	
V_{12}	Segment/Common 1/2 level voltage		—	1/2V_{SLCD}	—	
V_{13}	Segment/Common 1/3 level voltage		—	1/3V_{SLCD}	—	
V_{14}	Segment/Common 1/4 level voltage		—	1/4V_{SLCD}	—	
V_0	Segment/Common lowest level voltage		—	0	—	

(1) Guaranteed by design, not tested in production.

(2) SLCD enabled with 3V internal step-up active,1/8 duty,1/4 bias, division ratio= 64, all pixels active, no SLCD connected.

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4.20 I2C characteristics

Table 4-39. I2C characteristics(1)(2)(3)

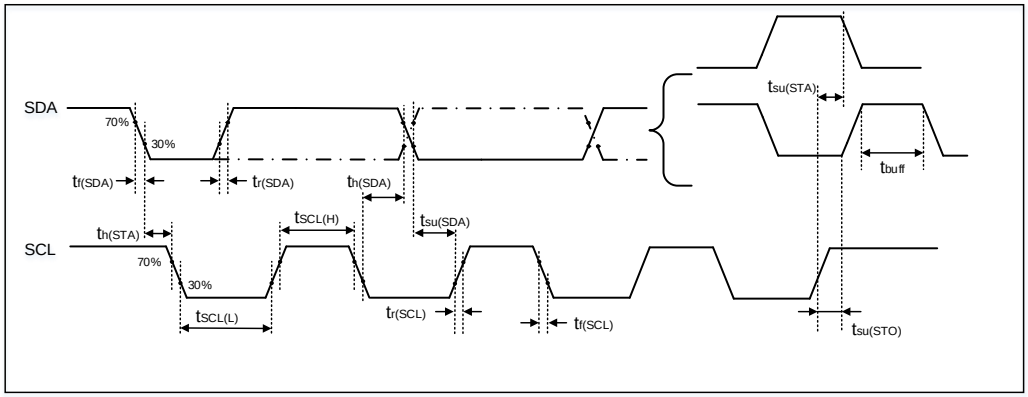
Symbol	Parameter	Conditions	Standard mode		Fast mode		Fast mode plus		Unit
			Min	Max	Min	Max	Min	Max	
$t_{SCL(H)}$	SCL clock high time	—	4.0	—	0.6	—	0.2	—	μs
$t_{SCL(L)}$	SCL clock low time	—	4.7	—	1.3	—	0.5	—	μs
$t_{su(SDA)}$	SDA setup time	—	250	—	100	—	50	—	ns
$t_{h(SDA)}$	SDA data hold time	—	0(3)	3450	0	900	0	450	ns
$t_{r(SDA/SCL)}$	SDA and SCL rise time	—	—	1000	—	300	—	120	ns
$t_{f(SDA/SCL)}$	SDA and SCL fall time	—	—	300	—	300	—	120	ns
$t_{h(STA)}$	Start condition hold time	—	4.0	—	0.6	—	0.26	—	μs
$t_{s(STA)}$	Repeated Start condition setup time	—	4.7	—	0.6	—	0.26	—	μs
$t_{s(STO)}$	Stop condition setup time	—	4.0	—	0.6	—	0.26	—	μs
t_{buff}	Stop to Start condition time (bus free)	—	4.7	—	1.3	—	0.5	—	μs

(1) Guaranteed by design, not tested in production.

(2) To ensure the standard mode I2C frequency, f_{PCLK1} must be at least 2 MHz. To ensure the fast mode I2C frequency, f_{PCLK1} must be at least 4 MHz. To ensure the fast mode plus I2C frequency, f_{PCLK1} must be at least a multiple of 10 MHz.

(3) The device should provide a data hold time of 300 ns at least in order to bridge the undefined region of the falling edge of SCL.

Figure 4-7. I2C bus timing diagram



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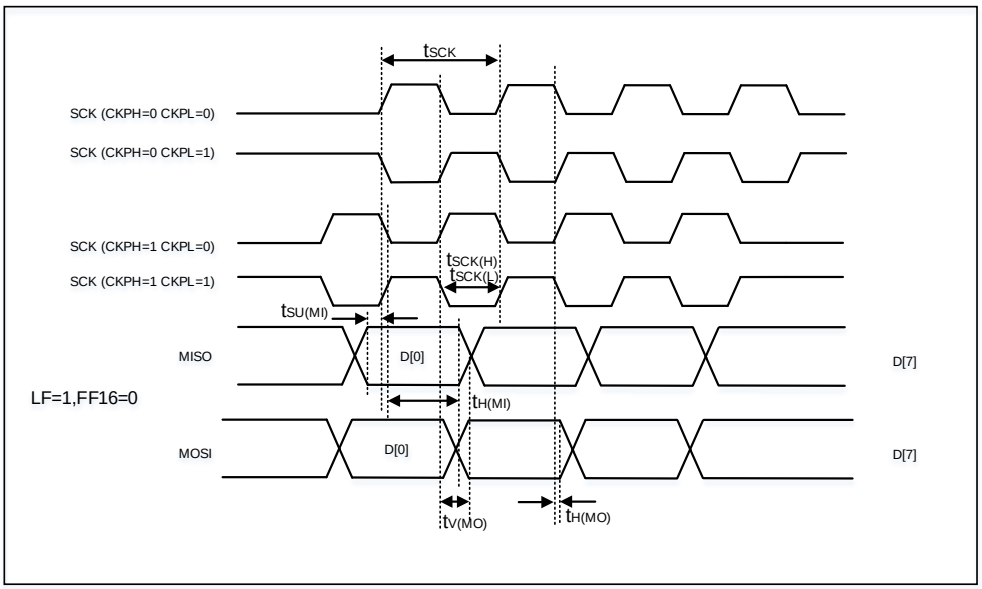
4.21 SPI characteristics

Table 4-40. Standard SPI characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency	—	—	—	16	MHz
$t_{sck(H)}$	SCK clock high time	Master mode, f_{PCLKx} = 64 MHz, presc = 4	—	20	—	ns
$t_{sck\ (L)}$	SCK clock low time	Master mode, f_{PCLKx} = 64 MHz, presc = 4	—	20	—	ns
SPI master mode						
$t_{V(MO)}$	Data output valid time	—	—	—	10	ns
$t_{SU(MI)}$	Data input setup time	—	1	—	—	ns
$t_{H(MI)}$	Data input hold time	—	0	—	—	ns
SPI slave mode						
$t_{SU(NSS)}$	NSS enable setup time	—	0	—	—	ns
$t_{H(NSS)}$	NSS enable hold time	—	1	—	—	ns
$t_{A(SO)}$	Data output access time	—	—	8	—	ns
$t_{DIS(SO)}$	Data output disable time	—	—	9	—	ns
$t_{V(SO)}$	Data output valid time	—	—	9	—	ns
$t_{SU(SI)}$	Data input setup time	—	0	—	—	ns
$t_{H(SI)}$	Data input hold time	—	1	—	—	ns

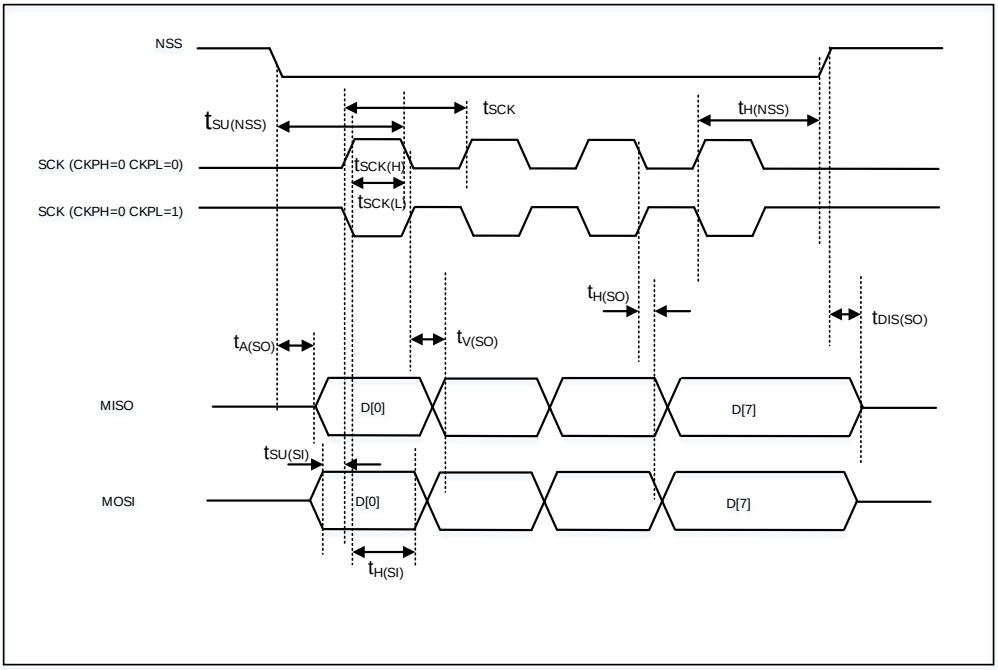
(1) Based on characterization, not tested in production.

Figure 4-8. SPI timing diagram - master mode



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Figure 4-9. SPI timing diagram - slave mode



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4.22 I2S characteristics

Table 4-41. I2S characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CK}	Clock frequency	Master mode (data: 16 bits, Audio frequency = 96 kHz)	—	6.25	—	MHz
		Slave mode	—	—	12.5	
t_H	Clock high time	—	—	80	—	ns
t_L	Clock low time		—	80	—	ns
$t_{V(WS)}$	WS valid time	Master mode	—	3	—	ns
$t_{H(WS)}$	WS hold time	Master mode	—	3	—	ns
$t_{SU(WS)}$	WS setup time	Slave mode	0	—	—	ns
$t_{H(WS)}$	WS hold time	Slave mode	3	—	—	ns
$Ducy_{(sck)}$	I2S slave input clock duty cycle	Slave mode	—	50	—	%
$t_{SU(SD_MR)}$	Data input setup time	Master mode	1	—	—	ns
$t_{SU(SD_SR)}$	Data input setup time	Slave mode	0	—	—	ns
$t_{H(SD_MR)}$	Data input hold time	Master receiver	0	—	—	ns
$t_{H(SD_SR)}$		Slave receiver	1	—	—	ns
$t_{V(SD_ST)}$	Data output valid time	Slave transmitter (after enable edge)	—	—	10	ns
$t_{H(SD_ST)}$	Data output hold time	Slave transmitter (after enable edge)	3	—	—	ns
$t_{V(SD_MT)}$	Data output valid time	Master transmitter (after enable edge)	—	—	10	ns
$t_{H(SD_MT)}$	Data output hold time	Master transmitter (after enable edge)	0	—	—	ns

(1) Based on characterization, not tested in production.

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Figure 4-10. I2S timing diagram - master mode

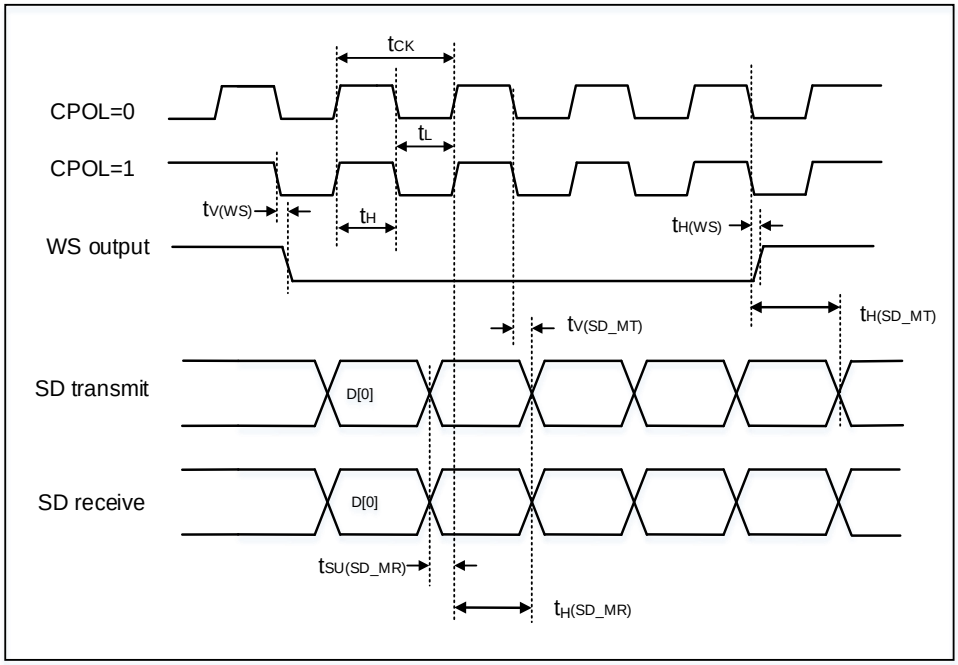
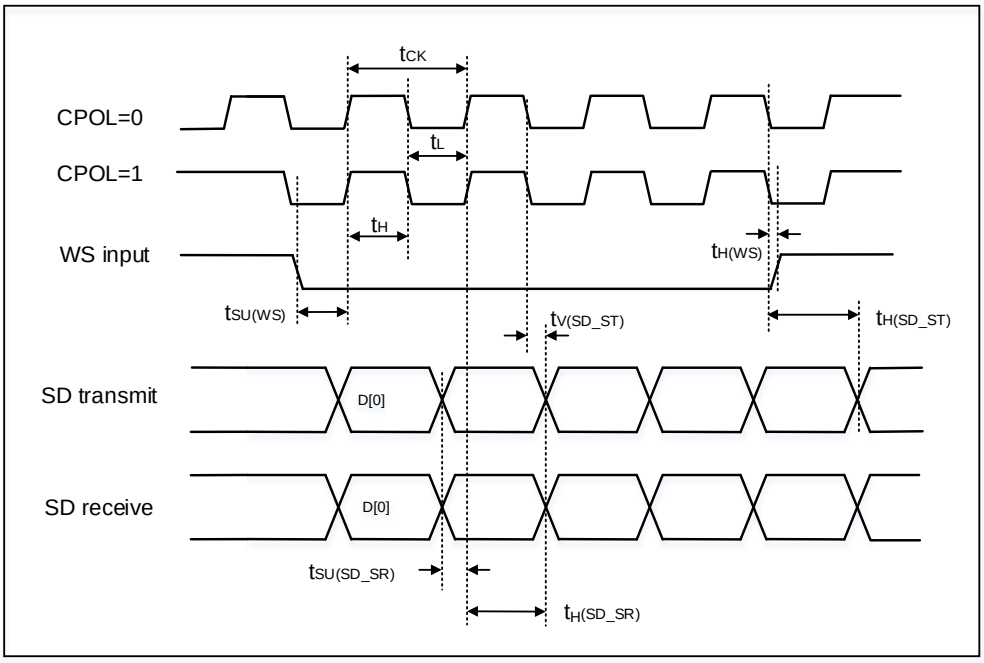


Figure 4-11. I2S timing diagram - slave mode



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4.23 USART/LPUART characteristics

Table 4-42. USART/LPUART characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency	f_{PCLKx} = 64 MHz	—	—	32	MHz
$t_{SCK(H)}$	SCK clock high time	f_{PCLKx} = 64 MHz	15.625	—	—	ns
$t_{SCK(L)}$	SCK clock low time	f_{PCLKx} = 64 MHz	15.625	—	—	ns

(1) Guaranteed by design, not tested in production.

4.24 USBD characteristics

Table 4-43. USBD startup time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	USBD startup time	1	μs

(1) Guaranteed by design, not tested in production.

Table 4-44. USBD DC electrical characteristics

Symbol		Parameter	Conditions	Min	Typ	Max	Unit
Input levels(1)	V_{DD}	USBD operating voltage	—	3.0	—	3.63	V
	V_{DI}	Differential input sensitivity	—	0.2	—	—	
	V_{CM}	Differential common mode range	Includes V_{DI} range	0.8	—	2.5	
	V_{SE}	Single ended receiver threshold	—	0.8	—	2.0	
Output levels (2)	V_{OL}	Static output level low	R_L of 1.0 kΩ to 3.63 V	—	—	0.3	V
	V_{OH}	Static output level high	R_L of 15 kΩ to V_{SS}	2.8	3.3	3.63	
R_{PU}(2)		USBDP	V_{IN} = V_{SS}	1.2	1.5	1.8	KΩ

(1) Guaranteed by design, not tested in production.

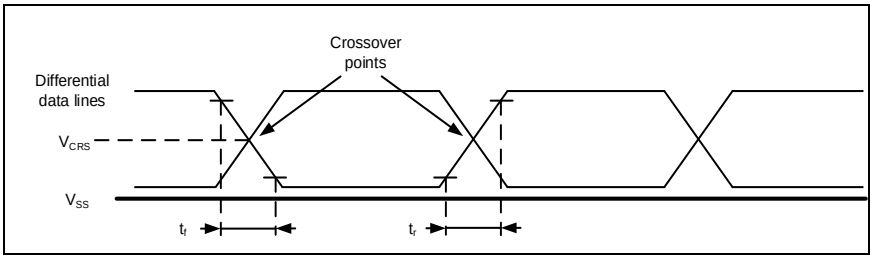
(2) Based on characterization, not tested in production.

Table 4-45. USBD full speed-electrical characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_R	Rise time	C_L = 50 pF	4	5	20	ns
t_F	Fall time	C_L = 50 pF	4	5	20	ns
t_{RFM}	Rise/ fall time matching	t_R / t_F	90	—	111	%
V_{CRS}	Output signal crossover voltage	—	1.09	—	2.0	V

(1) Guaranteed by design, not tested in production.

Figure 4-12. USBD timings: definition of data signal rise and fall time



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4.25 WDGT characteristics

Table 4-46. FWDGT min/max timeout period at 32 kHz (IRC32K)(1)

Prescaler divider	PSC[2:0] bits	Min timeout RLD[11:0]= 0x000	Max timeout RLD[11:0]= 0xFFF	Unit
1/4	000	0.03125	511.90625	ms
1/8	001	0.03125	1023.78125	
1/16	010	0.03125	2047.53125	
1/32	011	0.03125	4095.03125	
1/64	100	0.03125	8190.03125	
1/128	101	0.03125	16380.03125	
1/256	110 or 111	0.03125	32760.03125	

(1) Guaranteed by design, not tested in production.

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Table 4-47. WWDGT min-max timeout value at 32 MHz (f_{PCLK1})(1)

Prescaler divider	PSC[3:0]	Min timeout value CNT[6:0] = 0x40	Unit	Max timeout value CNT[6:0] = 0x7F	Unit
1/1	0000	128	µs	8.192	ms
1/2	0001	256		16.384	
1/4	0010	512		32.768	
1/8	0011	1.024	ms	65.536	
1/16	0100	2.048		131.072	
1/32	0101	4.096		262.144	
1/64	0110	8.192		524.288	
1/128	0111	16.384		1048.576	
1/256	1000	32.768		2097.152	
1/512	1001	65.536		4194.304	
1/1024	1010	131.072		8388.608	
1/2048	1011	262.144		16777.216	
1/4096	1100	524.288		33554.432	
1/8192	1101	1048.576		67108.864	
1/1	1110	128	µs	4.096	
1/1	1111	128		4.096	

(1) Guaranteed by design, not tested in production.

4.26 Parameter conditions

Unless otherwise specified, all values given for V_{DD} = V_{DDA} = 3.3 V, T_A = 25 ℃.

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5 Package information

5.1 LQFP64 package outline dimensions

Figure 5-1. LQFP64 package outline

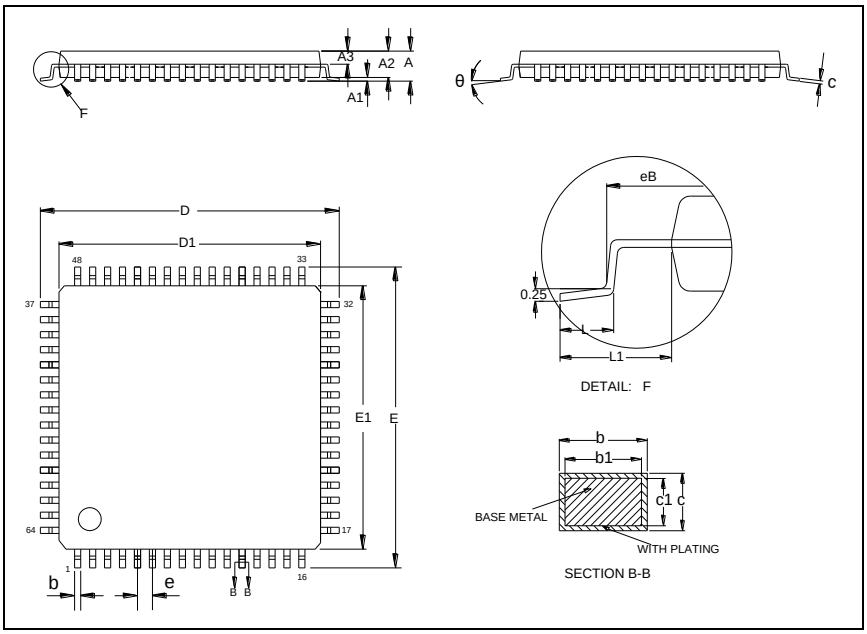


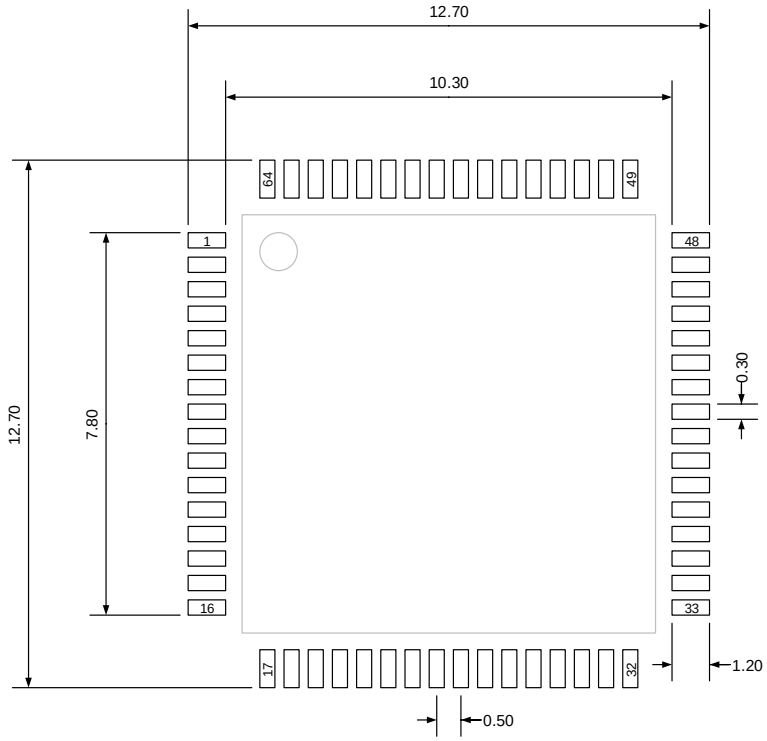
Table 5-1. LQFP64 package dimensions

Symbol	Min	Typ	Max
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	—	0.26
b1	0.17	0.20	0.23
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
E	11.80	12.00	12.20
E1	9.90	10.00	10.10
e	—	0.50	—
eB	11.25	—	11.45
L	0.45	—	0.75
L1	—	1.00	—
θ	0°	—	7°

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(Original dimensions are in millimeters)

Figure 5-2. LQFP64 recommended footprint



(Original dimensions are in millimeters)

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5.2 LQFP48 package outline dimensions

Figure 5-3. LQFP48 package outline

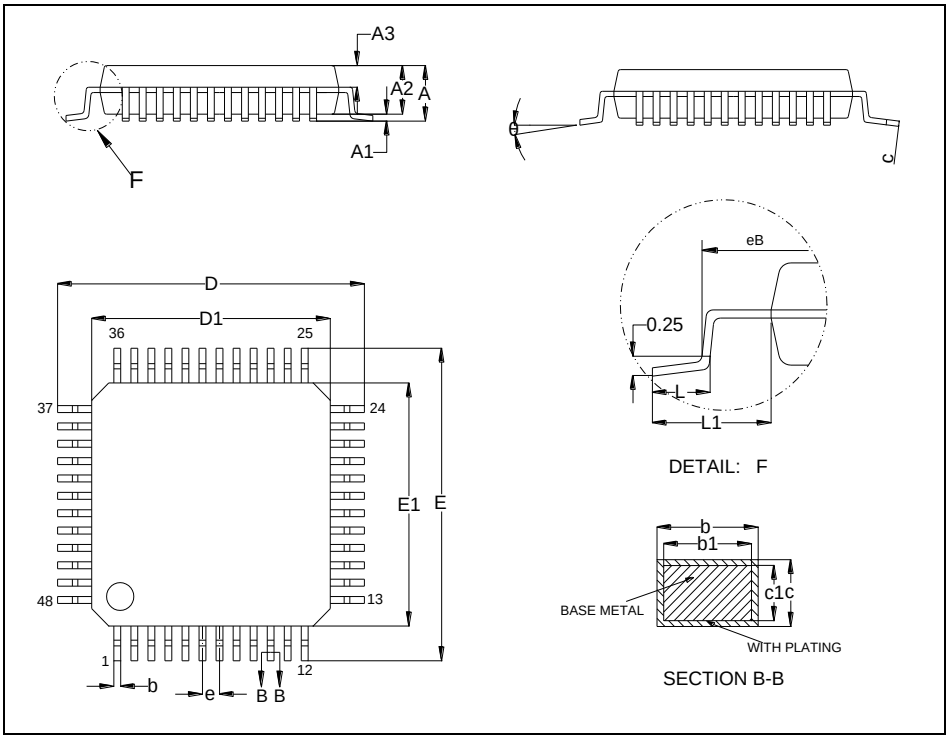


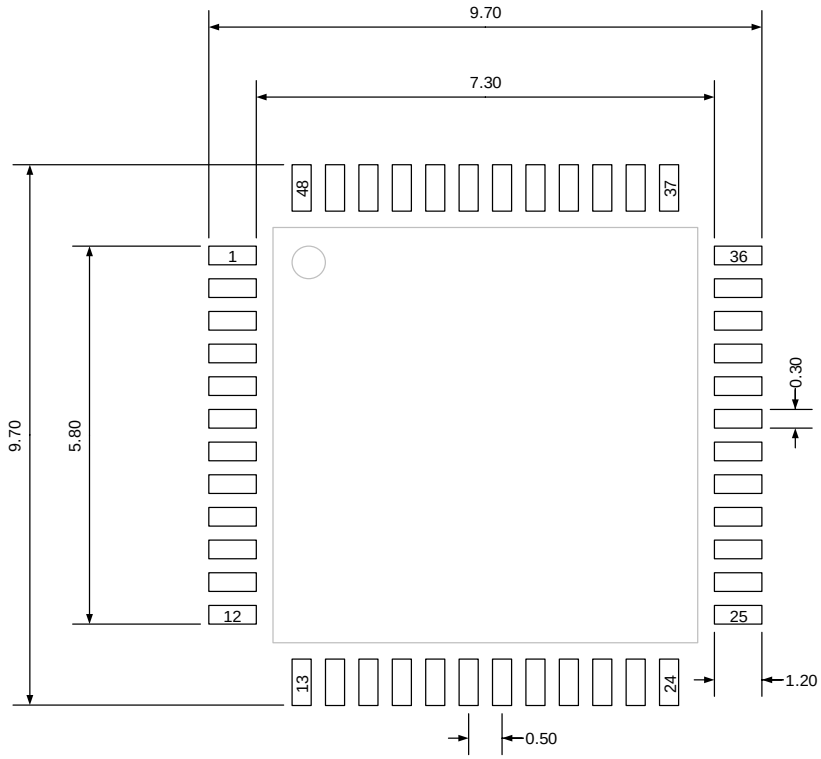
Table 5-2. LQFP48 package dimensions

Symbol	Min	Typ	Max
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	—	0.26
b1	0.17	0.20	0.23
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	—	0.50	—
eB	8.10	—	8.25
L	0.45	—	0.75
L1	—	1.00	—
θ	0°	—	7°

(Original dimensions are in millimeters)

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Figure 5-4. LQFP48 recommended footprint



(Original dimensions are in millimeters)

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5.3 LQFP32 package outline dimensions

Figure 5-5. LQFP32 package outline

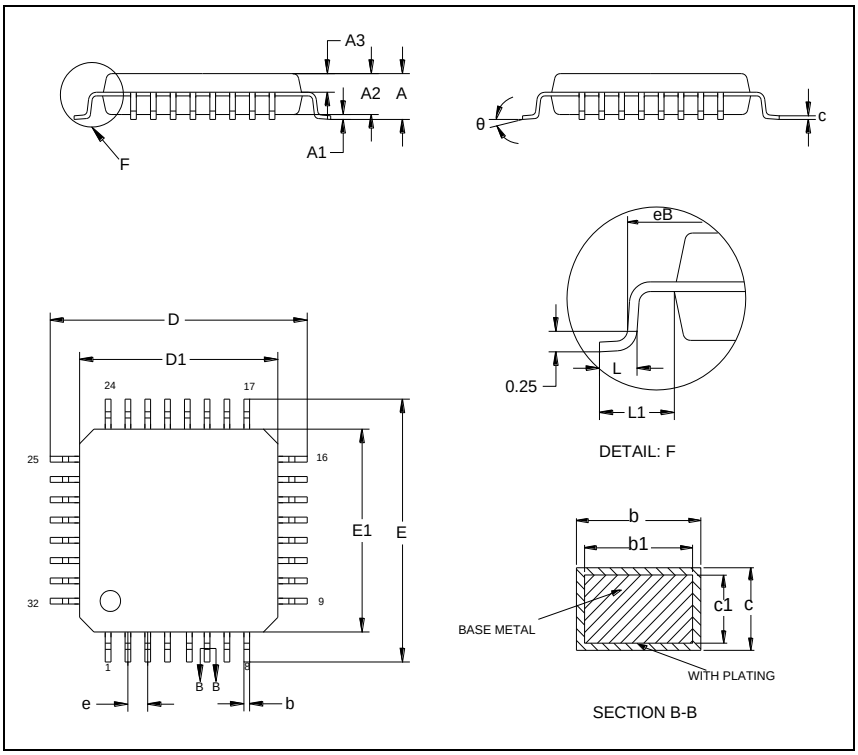


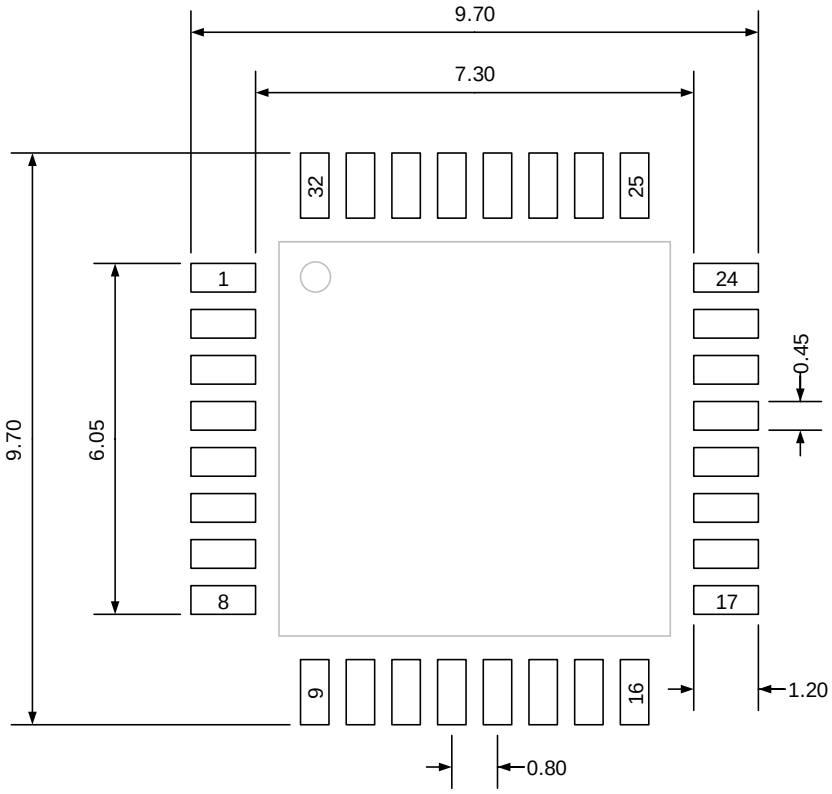
Table 5-3. LQFP32 package dimensions

Symbol	Min	Typ	Max
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.33	—	0.41
b1	0.32	0.35	0.38
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	—	0.80	—
eB	8.10	—	8.25
L	0.45	—	0.75
L1	—	1.00	—
θ	0°	—	7°

(Original dimensions are in millimeters)

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Figure 5-6. LQFP32 recommended footprint



(Original dimensions are in millimeters)

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5.4 QFN32 package outline dimensions

Figure 5-7. QFN32 package outline

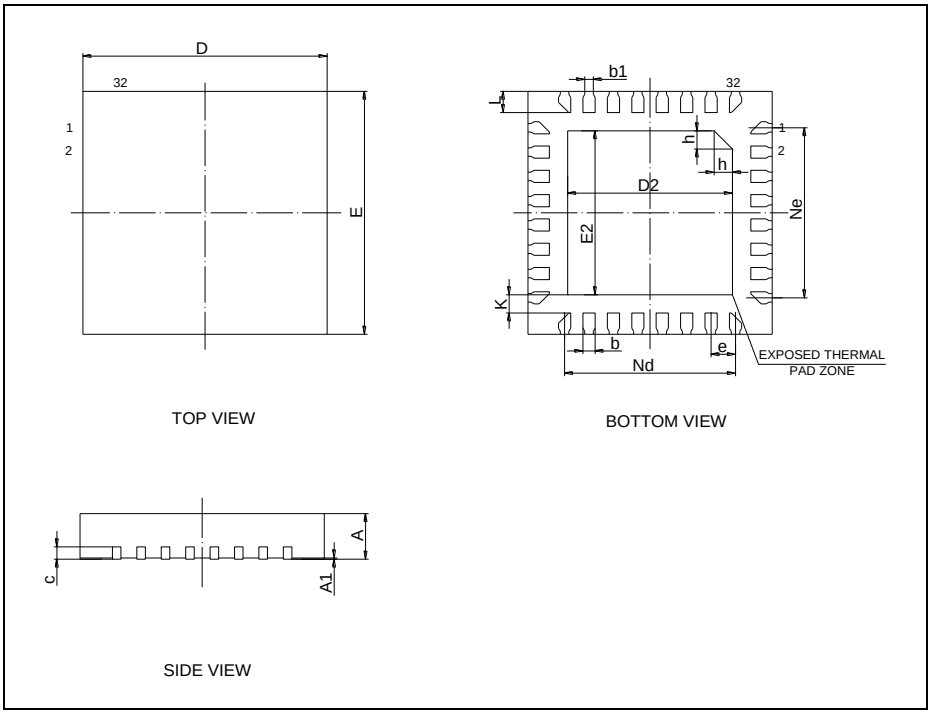


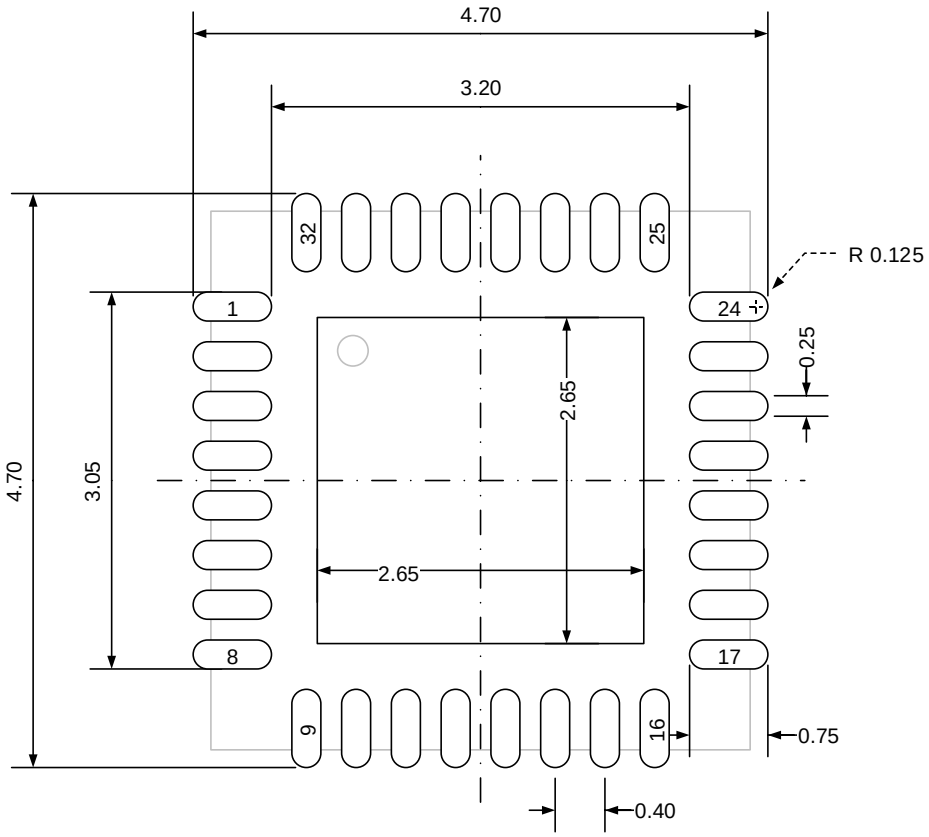
Table 5-4. QFN32 package dimensions

Symbol	Min	Typ	Max
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.15	0.20	0.25
b1	—	0.14	—
c	—	0.20	—
D	3.90	4.00	4.10
D2	2.60	2.70	2.80
E	3.90	4.00	4.10
E2	2.60	2.70	2.80
e	—	0.40	—
h	0.25	0.30	0.35
K	—	0.30	—
L	0.30	0.35	0.40
Nd	—	2.80	—
Ne	—	2.80	—

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Figure 5-8. QFN32 recommended footprint



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5.5 Thermal characteristics

Thermal resistance is used to characterize the thermal performance of the package device, which is represented by the Greek letter "θ". For semiconductor devices, thermal resistance represents the steady-state temperature rise of the chip junction due to the heat dissipated on the chip surface.

θ_{JA}: Thermal resistance, junction-to-ambient.

θ_{JB}: Thermal resistance, junction-to-board.

θ_{JC}: Thermal resistance, junction-to-case.

Ψ_{JB}: Thermal characterization parameter, junction-to-board.

Ψ_{JT}: Thermal characterization parameter, junction-to-top center.

$$\theta_{JA}=(T_J-T_A)/P_D \quad (5\text{-}1)$$

$$\theta_{JB}=(T_J-T_B)/P_D \quad (5\text{-}2)$$

$$\theta_{JC}=(T_J-T_C)/P_D \quad (5\text{-}3)$$

Where, T_J = Junction temperature.

T_A = Ambient temperature

T_B = Board temperature

T_C = Case temperature which is monitoring on package surface

P_D = Total power dissipation

θ_{JA} represents the resistance of the heat flows from the heating junction to ambient air. It is an indicator of package heat dissipation capability. Lower θ_{JA} can be considerate as better overall thermal performance. θ_{JA} is generally used to estimate junction temperature.

θ_{JB} is used to measure the heat flow resistance between the chip surface and the PCB board.

θ_{JC} represents the thermal resistance between the chip surface and the package top case. θ_{JC} is mainly used to estimate the heat dissipation of the system (using heat sink or other heat dissipation methods outside the device package).

Table 5-6. Package thermal characteristics(1)

Symbol	Condition	Package	Value	Unit
θ_{JA}	Natural convection, 2S2P PCB	LQFP64	54.57	°C/W
		LQFP48	69.64	
		LQFP32	55.26	
		QFN32	42.57	
θ_{JB}	Cold plate, 2S2P PCB	LQFP64	35.08	°C/W
		LQFP48	43.16	

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Symbol	Condition	Package	Value	Unit
		LQFP32	26.24	
		QFN32	19.21	
θ_{JC}	Cold plate, 2S2P PCB	LQFP64	18.11	°C/W
		LQFP48	25.36	
		LQFP32	25.23	
		QFN32	19.10	
Ψ_{JB}	Natural convection, 2S2P PCB	LQFP64	35.41	°C/W
		LQFP48	47.75	
		LQFP32	32.03	
		QFN32	19.18	
Ψ_{JT}	Natural convection, 2S2P PCB	LQFP64	1.10	°C/W
		LQFP48	2.45	
		LQFP32	2.06	
		QFN32	0.62	

(1) Thermal characteristics are based on simulation, and meet JEDEC specification.

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6 Ordering information

Table 6-1. Part ordering code for GD32L233xx devices

Ordering code	Flash (KB)	Package	Package type	Temperature operating range
GD32L233RCT6	256	LQFP64	Green	Industrial -40°C to +85°C
GD32L233RBT6	128	LQFP64	Green	Industrial -40°C to +85°C
GD32L233R8T6	64	LQFP64	Green	Industrial -40°C to +85°C
GD32L233CCT6	256	LQFP48	Green	Industrial -40°C to +85°C
GD32L233CBT6	128	LQFP48	Green	Industrial -40°C to +85°C
GD32L233C8T6	64	LQFP48	Green	Industrial -40°C to +85°C
GD32L233KBT6	128	LQFP32	Green	Industrial -40°C to +85°C
GD32L233K8T6	64	LQFP32	Green	Industrial -40°C to +85°C
GD32L233KBQ6	128	QFN32	Green	Industrial -40°C to +85°C
GD32L233K8Q6	64	QFN32	Green	Industrial -40°C to +85°C

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7 Revision history

Table 7-1. Revision history

Revision No.	Description	Date
1.0	Initial Release	Oct.19, 2021
1.1	1. Modify description in ***Debug mode.*** 2. Modify description in ***Embedded memory.*** 3. Add EMI parameter in ***Table 4-9. EMI characteristics(1).*** 4. Modify table 4-17 and table 4-19 5. Modify power consumption value in ***Table 4-7. Power consumption characteristics(2)(3)*** 6. Update QFN32 recommended footprint figure.	Apr.13 2022

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