GigaDevice Semiconductor Inc.

GD32F527xx
Arm® Cortex®-M33 32-bit MCU

Datasheet

Revision 1.8

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1. General description

The GD32F527xx device belongs to the high performance line of GD32 MCU family. It is a new 32-bit general-purpose microcontroller based on the Arm® Cortex®-M33 core. The Cortex®-M33 processor is a 32-bit processor that possesses low interrupt latency and low-cost debug. The characteristics of integrated and advanced make the Cortex®-M33 processor suitable for market products that require microcontrollers with high performance and low power consumption. The processor is based on the ARMv8 architecture and supports a powerful and scalable instruction set including general data processing I/O control tasks, advanced data processing bit field manipulations and DSP.

The GD32F527xx device incorporates the Arm® Cortex®-M33 32-bit processor core operating at 200 MHz frequency with Flash security protection to prevent illegal code/data access. It provides up to 7680 KB of main Flash memory, 512KB SRAM (SRAM0, SRAM1, SRAM2), 512KB ADDSRAM and 64KB TCMSRAM memory. Both FLASH and SRAM have ECC capabilities. An extensive range of enhanced I/Os and peripherals connected to two APB buses. The devices offer up to three 12-bit 2.6 MSPS ADCs, up to eight general 16-bit timers, two 16-bit PWM advanced timers, two 32-bit general timers, and two 16-bit basic timers, as well as standard and advanced communication interfaces: up to six SPIs, six I2Cs, four USARTs and four UARTs, two I2Ss, two CAN-FDs, a USBHS, a USBFS, an ENET and a SDIO. Additional peripherals as digital camera interface (DCI), EXMC interface with SDRAM extension support, TFT-LCD Interface (TLI), Image Processing Accelerator (IPA) and Serial Audio Interface (SAI), are included.

The GD32F527xx is designed with a comprehensive set of system security features. System security features cover several aspects, including firmware intellectual property protection, device private data protection, and service execution assurance. Users can realize information security through the security functions of trusted code area protection, password area protection, Secure boot, debugging security, etc.

The device operates from a 1.71V to 3.6V power supply and available in –40 to +105 °C temperature range for grade 7 devices. Three power saving modes provide the flexibility for maximum optimization of power consumption, an especially important consideration in low power applications.

The above features make GD32F527xx devices suitable for a wide range of interconnection and advanced applications, especially in areas such as industrial control, consumer and handheld equipment, embedded modules, human machine interface, security and alarm systems, energy storage system, graphic display, audio player, automotive navigation, drone, IoT and so on.





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2. Device overview

2.1. Device information

Table 2-1. GD32F527xx devices features and peripheral list

Part Number			GD32F527xx					
			ZMT7	ZST7	VMT7	VST7	RMT7	RST7
FLASH (KB)	BANK0	Code area	1536	2048	1536	2048	1536	2048
		Data area	512	0	512	0	512	0
	BANK1	Data area	2048	2048	2048	2048	2048	2048
	BANK1_Ex	Data area	0	3584	0	3584	0	3584
	Total		4096	7680	4096	7680	4096	7680
SRAM (KB)			1024	512	1024	512	1024	512
TCMSRAM (KB)			64	64	64	64	64	64
Timers	General timer (16-bit)		8 (2-3,8-13)	8 (2-3,8-13)	8 (2-3,8-13)	8 (2-3,8-13)	8 (2-3,8-13)	8 (2-3,8-13)
	General timer (32-bit)		2 (1,4)	2 (1,4)	2 (1,4)	2 (1,4)	2 (1,4)	2 (1,4)
	Advanced timer(16-bit)		2 (0,7)	2 (0,7)	2 (0,7)	2 (0,7)	2 (0,7)	2 (0,7)
	Basic timer (16-bit)		2 (5,6)	2 (5,6)	2 (5,6)	2 (5,6)	2 (5,6)	2 (5,6)
	SysTick		1	1	1	1	1	1
	Watchdog		2	2	2	2	2	2
	RTC		1	1	1	1	1	1
Connectivity	USART		4	4	4	4	4	4
	UART		4	4	4	4	2	2
	I2C		6	6	3	3	3	3
	SPI/I2S		6/2 (0-5)/(1-2)	6/2 (0-5)/(1-2)	5/2 (0-4)/(1-2)	5/2 (0-4)/(1-2)	3/2 (0-2)/(1-2)	3/2 (0-2)/(1-2)
	SDIO		1	1	1	1	1	1
	CAN		2xFD	2xFD	2xFD	2xFD	2xFD	2xFD
	USBFS		1	1	1	1	1	1
	USBHS		1	1	1	1	1	1

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Part Number		GD32F527xx					
		ZMT7	ZST7	VMT7	VST7	RMT7	RST7
	ENET	1	1	1	1	1	1
	TLI	1	1	1	1	0	0
	DCI	1	1	1	1	1	1
SAI		1	1	1	1	0	0
EXMC/SDRAM		1/1	1/1	1/0	1/0	0/0	0/0
IPA		1	1	1	1	0	0
CAU		1	1	1	1	1	1
HAU		1	1	1	1	1	1
TRNG		1	1	1	1	1	1
PKCAU		1	1	1	1	1	1
12bit ADC	Units	3	3	3	3	3	3
	Channels	24	24	16	16	16	16
DAC	Units	1	1	1	1	1	1
	Channels	2	2	2	2	2	2
GPIO		114	114	82	82	51	51
Package		LQFP144		LQFP100		LQFP64	

Table 2-2. GD32F527xx devices features and peripheral list (Cont.)

Part Number			GD32F527xx			
			IMT7	IST7	IMK7	ISK7
FLASH (KB)	BANK0	Code area	1536	2048	1536	2048
		Data area	512	0	512	0
	BANK1	Data area	2048	2048	2048	2048
	BANK1_Ex	Data area	0	3584	0	3584
	Total		4096	7680	4096	7680
SRAM (KB)			1024	512	1024	512
TCMSRAM (KB)			64	64	64	64
Timers	General timer (16-bit)		8 (2-3,8-13)	8 (2-3,8-13)	8 (2-3,8-13)	8 (2-3,8-13)
	General timer (32-bit)		2 (1,4)	2 (1,4)	2 (1,4)	2 (1,4)
	Advanced		2	2	2	2

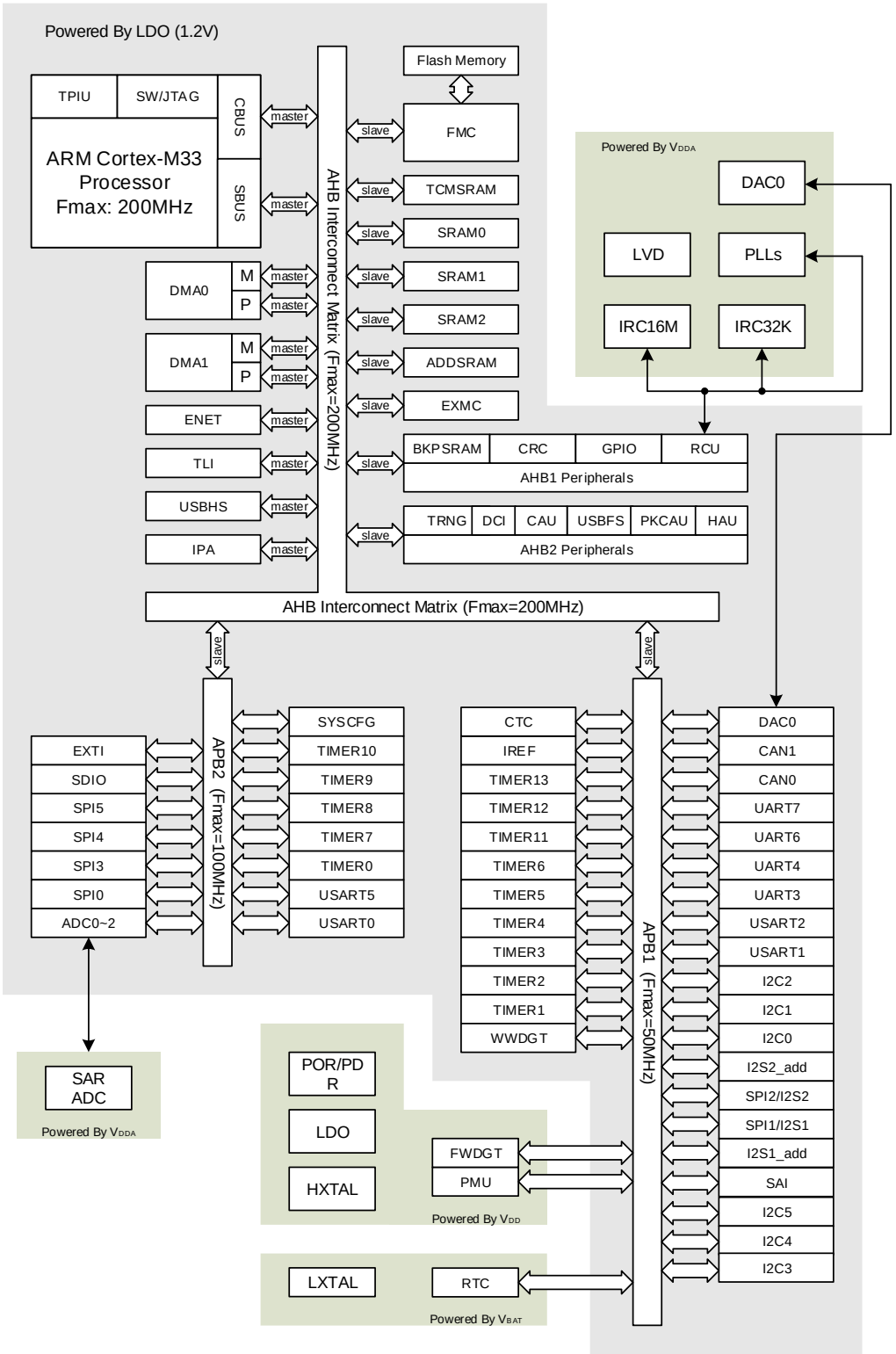
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Part Number		GD32F527xx			
		IMT7	IST7	IMK7	ISK7
	timer(16-bit)	(0,7)	(0,7)	(0,7)	(0,7)
	Basic timer (16-bit)	2 (5,6)	2 (5,6)	2 (5,6)	2 (5,6)
	SysTick	1	1	1	1
	Watchdog	2	2	2	2
	RTC	1	1	1	1
Connectivity	USART	4	4	4	4
	UART	4	4	4	4
	I2C	6	6	6	6
	SPI/I2S	6/2 (0-5)/(1-2)	6/2 (0-5)/(1-2)	6/2 (0-5)/(1-2)	6/2 (0-5)/(1-2)
	SDIO	1	1	1	1
	CAN	2xFD	2xFD	2xFD	2xFD
	USBFS	1	1	1	1
	USBHS	1	1	1	1
	ENET	1	1	1	1
	TLI	1	1	1	1
	DCI	1	1	1	1
SAI		1	1	1	1
EXMC/SDRAM		1/1	1/1	1/1	1/1
IPA		1	1	1	1
CAU		1	1	1	1
HAU		1	1	1	1
TRNG		1	1	1	1
PKCAU		1	1	1	1
12bit ADC	Units	3	3	3	3
	Channels	24	24	24	24
DAC	Units	1	1	1	1
	Channels	2	2	2	2
GPIO		140	140	140	140
Package		LQFP176		BGA176	

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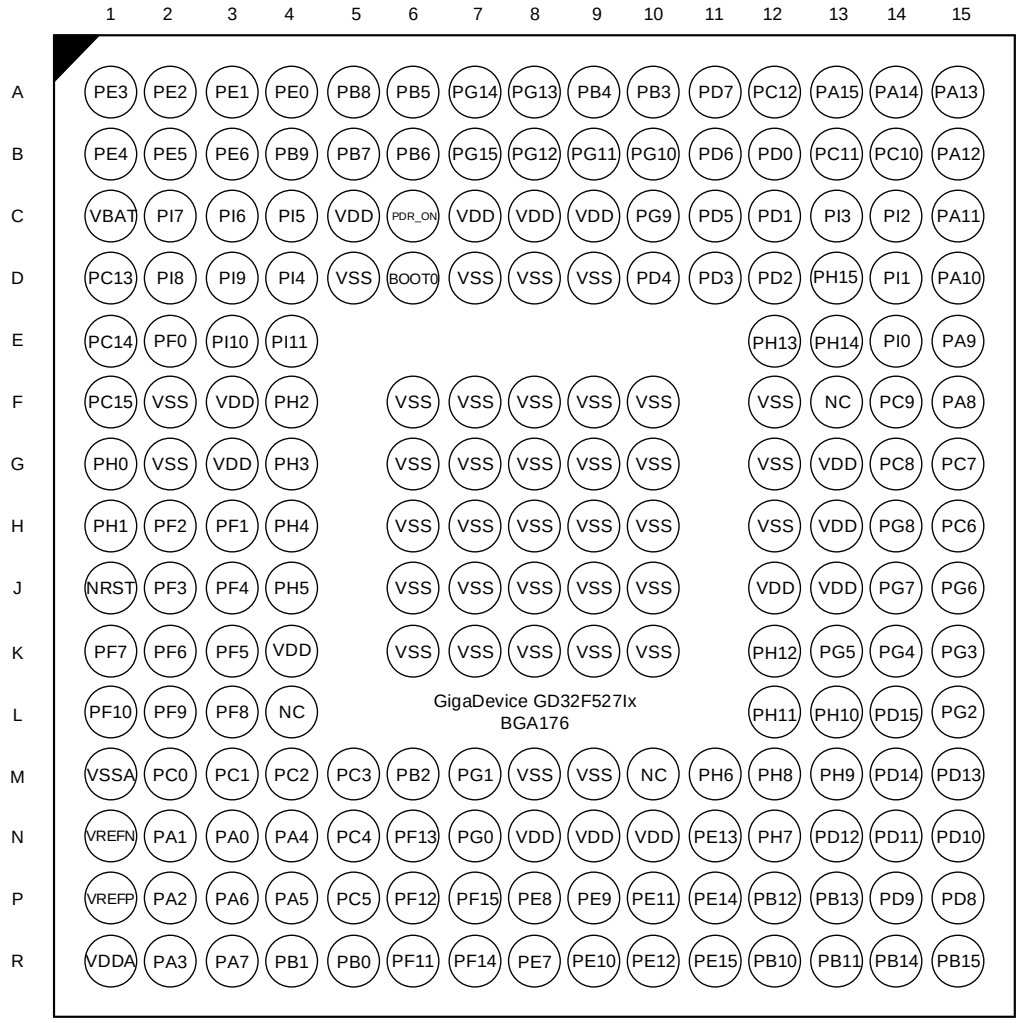
2.2. Block diagram

Figure 2-1. GD32F527xx block diagram



2.3. Pinouts and pin assignment

Figure 2-2. GD32F527Ix BGA176 pinouts



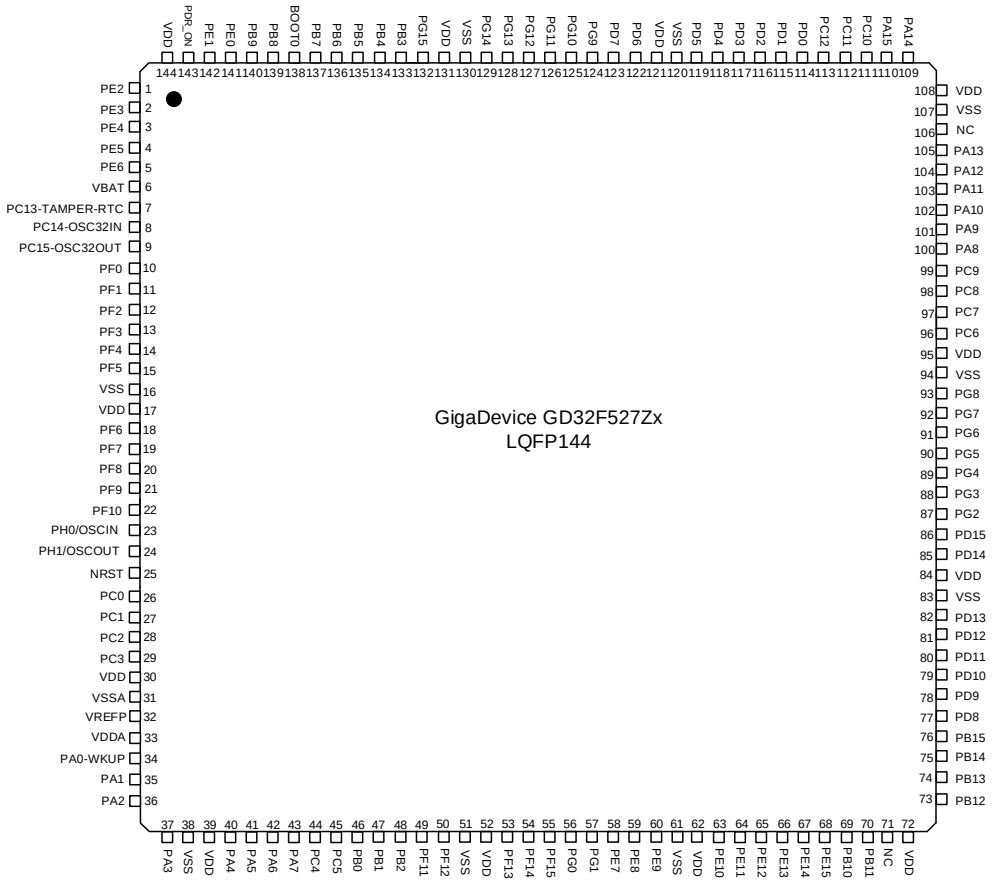
Note: The pin count of the BGA176 package is 176+25 (with an additional 25 VSS pins).

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Figure 2-3. GD32F527Ix LQFP176 pinouts



Figure 2-4. GD32F527Zx LQFP144 pinouts



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Figure 2-5. GD32F527Vx LQFP100 pinouts

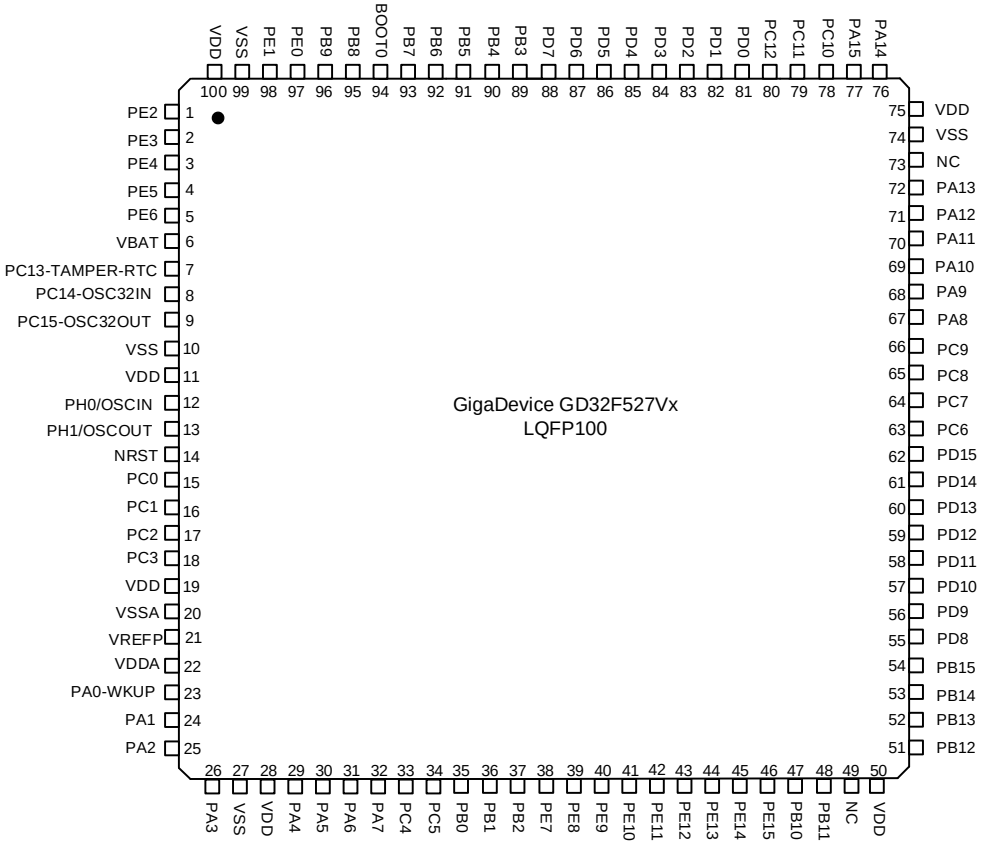
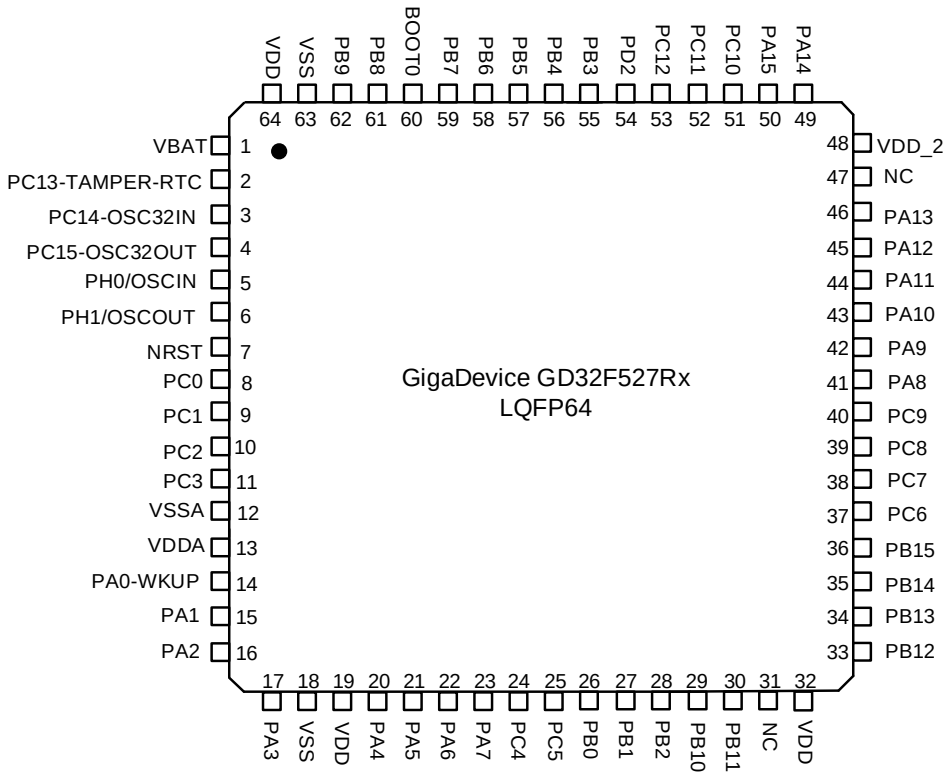


Figure 2-6. GD32F527Rx LQFP64 pinouts



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2.4. Memory map

Table 2-3. GD32F527xx memory map

Pre-defined Regions	Bus	Address	Peripherals
External Device	AHB matrix	0xC000 0000 - 0xDFFF FFFF	EXMC - SDRAM
		0xA000 1000 - 0xBFFF FFFF	Reserved
		0xA000 0000 - 0xA000 0FFF	EXMC - SWREG
External RAM		0x9000 0000 - 0x9FFF FFFF	EXMC - PC CARD
		0x7000 0000 - 0x8FFF FFFF	EXMC - NAND
		0x6000 0000 - 0x6FFF FFFF	EXMC – NOR / PSRAM / SRAM
Peripheral	AHB2	0x5006 3000 - 0x5FFF FFFF	Reserved
		0x5006 1000 - 0x5006 2FFF	PKCAU
		0x5006 0C00 - 0x5006 0FFF	Reserved
		0x5006 0800 - 0x5006 0BFF	TRNG
		0x5006 0400 - 0x5006 07FF	HAU
		0x5006 0000 - 0x5006 03FF	CAU
		0x5005 0400 - 0x5005 FFFF	Reserved
		0x5005 0000 - 0x5005 03FF	DCI
		0x5004 0000 - 0x5004 FFFF	Reserved
		0x5000 0000 - 0x5003 FFFF	USBFS
	AHB1	0x4008 0000 - 0x4FFF FFFF	Reserved (AHB1)
		0x4004 0000 - 0x4007 FFFF	USBHS
		0x4002 BC00 - 0x4003 FFFF	Reserved
		0x4002 B000 - 0x4002 BBFF	IPA
		0x4002 A000 - 0x4002 AFFF	Reserved
		0x4002 8000 - 0x4002 9FFF	ENET
		0x4002 6800 - 0x4002 7FFF	Reserved
		0x4002 6400 - 0x4002 67FF	DMA1
		0x4002 6000 - 0x4002 63FF	DMA0
		0x4002 5000 - 0x4002 5FFF	Reserved
		0x4002 4000 - 0x4002 4FFF	BKPSRAM
		0x4002 3C00 - 0x4002 3FFF	FMC
		0x4002 3800 - 0x4002 3BFF	RCU
		0x4002 3400 - 0x4002 37FF	Reserved
		0x4002 3000 - 0x4002 33FF	CRC
		0x4002 2C00 - 0x4002 2FFF	Reserved
		0x4002 2800 - 0x4002 2BFF	Reserved
		0x4002 2400 - 0x4002 27FF	Reserved
		0x4002 2000 - 0x4002 23FF	GPIOI
		0x4002 1C00 - 0x4002 1FFF	GPIOH

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Pre-defined Regions	Bus	Address	Peripherals
		0x4002 1800 - 0x4002 1BFF	GPIOG
		0x4002 1400 - 0x4002 17FF	GPIOF
		0x4002 1000 - 0x4002 13FF	GPIOE
		0x4002 0C00 - 0x4002 0FFF	GPIOD
		0x4002 0800 - 0x4002 0BFF	GPIOC
		0x4002 0400 - 0x4002 07FF	GPIOB
		0x4002 0000 - 0x4002 03FF	GPIOA
	APB2	0x4001 8400 - 0x4001 FFFF	Reserved
		0x4001 8000 - 0x4001 83FF	Reserved
		0x4001 7C00 - 0x4001 7FFF	Reserved
		0x4001 7800 - 0x4001 7BFF	Reserved
		0x4001 7400 - 0x4001 77FF	Reserved
		0x4001 7000 - 0x4001 73FF	Reserved
		0x4001 6C00 - 0x4001 6FFF	Reserved
		0x4001 6800 - 0x4001 6BFF	TLI
		0x4001 5C00 - 0x4001 67FF	Reserved
		0x4001 5800 - 0x4001 5BFF	SAI
		0x4001 5400 - 0x4001 57FF	SPI5
		0x4001 5000 - 0x4001 53FF	SPI4
		0x4001 4C00 - 0x4001 4FFF	Reserved
		0x4001 4800 - 0x4001 4BFF	TIMER10
		0x4001 4400 - 0x4001 47FF	TIMER9
		0x4001 4000 - 0x4001 43FF	TIMER8
		0x4001 3C00 - 0x4001 3FFF	EXTI
		0x4001 3800 - 0x4001 3BFF	SYSCFG
		0x4001 3400 - 0x4001 37FF	SPI3
		0x4001 3000 - 0x4001 33FF	SPI0
		0x4001 2C00 - 0x4001 2FFF	SDIO
		0x4001 2800 - 0x4001 2BFF	Reserved
		0x4001 2400 - 0x4001 27FF	Reserved
		0x4001 2000 - 0x4001 23FF	ADC
		0x4001 1C00 - 0x4001 1FFF	Reserved
		0x4001 1800 - 0x4001 1BFF	Reserved
		0x4001 1400 - 0x4001 17FF	USART5
		0x4001 1000 - 0x4001 13FF	USART0
		0x4001 0C00 - 0x4001 0FFF	Reserved
		0x4001 0800 - 0x4001 0BFF	Reserved
		0x4001 0400 - 0x4001 07FF	TIMER7
		0x4001 0000 - 0x4001 03FF	TIMER0
	APB1	0x4000 C800 - 0x4000 FFFF	Reserved
		0x4000 C400 - 0x4000 C7FF	IREF

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		0x4000 C000 - 0x4000 C3FF	Reserved
		0x4000 9000 - 0x4000 BFFF	Reserved
		0x4000 8C00 - 0x4000 8FFF	CAN SRAM 1k-2k bytes
		0x4000 8800 - 0x4000 8BFF	I2C5
		0x4000 8400 - 0x4000 87FF	I2C4
		0x4000 8000 - 0x4000 83FF	I2C3
		0x4000 7C00 - 0x4000 7FFF	UART7
		0x4000 7800 - 0x4000 7BFF	UART6
		0x4000 7400 - 0x4000 77FF	DAC0
		0x4000 7000 - 0x4000 73FF	PMU
		0x4000 6C00 - 0x4000 6FFF	CTC
		0x4000 6800 - 0x4000 6BFF	CAN1
		0x4000 6400 - 0x4000 67FF	CAN0
		0x4000 6000 - 0x4000 63FF	CAN SRAM 0-1k bytes
		0x4000 5C00 - 0x4000 5FFF	I2C2
		0x4000 5800 - 0x4000 5BFF	I2C1
		0x4000 5400 - 0x4000 57FF	I2C0
		0x4000 5000 - 0x4000 53FF	UART4
		0x4000 4C00 - 0x4000 4FFF	UART3
		0x4000 4800 - 0x4000 4BFF	USART2
		0x4000 4400 - 0x4000 47FF	USART1
		0x4000 4000 - 0x4000 43FF	I2S2_add
		0x4000 3C00 - 0x4000 3FFF	SPI2/I2S2
		0x4000 3800 - 0x4000 3BFF	SPI1/I2S1
		0x4000 3400 - 0x4000 37FF	I2S1_add
		0x4000 3000 - 0x4000 33FF	FWDGT
		0x4000 2C00 - 0x4000 2FFF	WWDGT
		0x4000 2800 - 0x4000 2BFF	RTC
		0x4000 2400 - 0x4000 27FF	Reserved
		0x4000 2000 - 0x4000 23FF	TIMER13
		0x4000 1C00 - 0x4000 1FFF	TIMER12
		0x4000 1800 - 0x4000 1BFF	TIMER11
		0x4000 1400 - 0x4000 17FF	TIMER6
		0x4000 1000 - 0x4000 13FF	TIMER5
		0x4000 0C00 - 0x4000 0FFF	TIMER4
		0x4000 0800 - 0x4000 0BFF	TIMER3
		0x4000 0400 - 0x4000 07FF	TIMER2
		0x4000 0000 - 0x4000 03FF	TIMER1
SRAM		0x2010 0000 - 0x3FFF FFFF	Reserved
		0x2008 0000 - 0x200F FFFF	ADDSRAM (512KB)
		0x2005 0000 - 0x2007 FFFF	SRAM2(192KB)

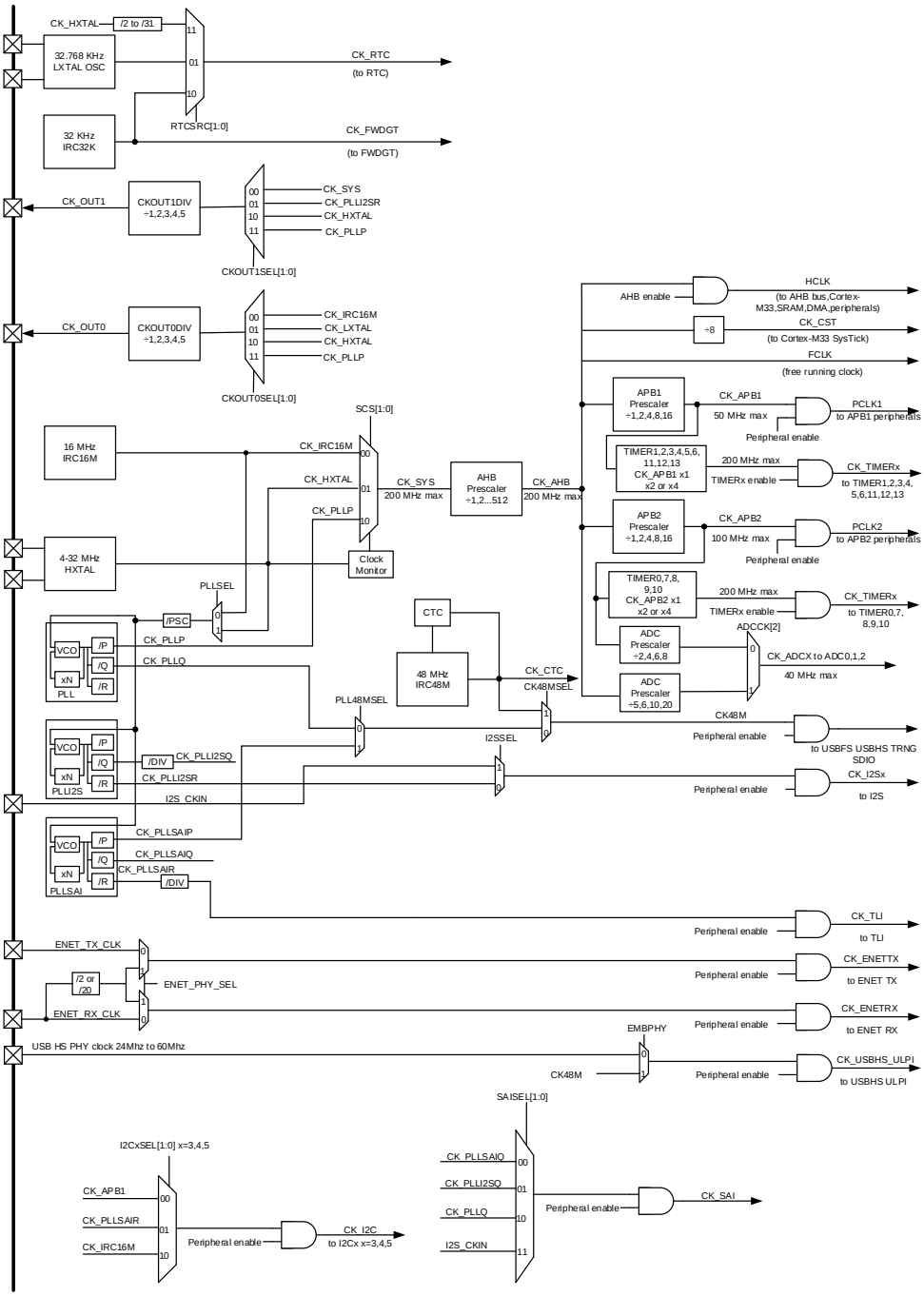
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Pre-defined Regions	Bus	Address	Peripherals
		0x2004 0000 - 0x2004 FFFF	SRAM1(64KB)
		0x2000 0000 - 0x2003 FFFF	SRAM0(256KB)
Code		0x1FFF C010 - 0x1FFF FFFF	Reserved
		0x1FFF C000 - 0x1FFF C00F	Option bytes Block (Bank0 option)
		0x1FFF B000 - 0x1FFF BFFF	Reserved
		0x1FFF 7880 - 0x1FFF AFFF	Reserved
		0x1FFF 7840 - 0x1FFF 787F	OTP0 Block (lock)
		0x1FFF 7800 - 0x1FFF 783F	OTP0 Block (data)
		0x1FFF 0000 - 0x1FFF 77FF	Boot loader(30KB)
		0x1FFE C010 - 0x1FFE FFFF	Reserved
		0x1FFE C000 - 0x1FFE C00F	Option bytes Block (Bank1 option)
		0x1FF2 0230 - 0x1FFE BFFF	Reserved
		0x1FF2 0210 - 0x1FF2 022F	OTP Block2 (lock)
		0x1FF2 0200 - 0x1FF2 020F	OTP Block1 (lock)
		0x1FF2 0000 - 0x1FF2 01FF	OTP Block2 (data)
		0x1FF0 0000 - 0x1FF1 FFFF	OTP Block1 (data)
		0x1001 0000 - 0x1FEF FFFF	Reserved
		0x1000 0000 - 0x1000 FFFF	TCMSRAM (64KB)
		0x0880 0000 - 0x0FFF FFFF	Reserved
		0x0840 0000 - 0x0877 FFFF	Main Flash(Bank1_Ex 3584kB)
		0x0820 0000 - 0x083F FFFF	Main Flash(Bank1 2MB)
		0x0800 0000 - 0x081F FFFF	Main Flash(Bank0 2MB)
		0x0030 0000 - 0x07FF FFFF	Aliased to the boot device
		0x0010 0000 - 0x002F FFFF	
		0x0002 0000 - 0x000F FFFF	
		0x0000 0000 - 0x0001 FFFF	

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2.5. Clock tree

Figure 2-7. GD32F527xx clock tree



Legend:

HXTAL: High speed crystal oscillator

LXTAL: Low speed crystal oscillator

IRC16M: Internal 16M RC oscillators

IRC32K: Internal 32K RC oscillator

IRC48M: Internal 48M RC oscillators

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2.6. Pin definitions

2.6.1. GD32F527Ix LQFP176 pin definitions

Table 2-4. GD32F527Ix LQFP176 pin definitions

GD32F527Ix LQFP176				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PE2	1	I/O	5VT	Default: PE2 Alternate: SPI3_SCK, SAI0_MCLK_0, ETH_MII_TXD3, EXMC_A23, EVENTOUT
PE3	2	I/O	5VT	Default: PE3 Alternate: SAI0_SD_1, EXMC_A19, EVENTOUT
PE4	3	I/O	5VT	Default: PE4 Alternate: SPI3_NSS, SAI0_FS_0, EXMC_A20, DCI_D4, TLI_B0, EVENTOUT
PE5	4	I/O	5VT	Default: PE5 Alternate: TIMER8_CH0, SPI3_MISO, SAI0_SCK_0, SPI0_MISO, EXMC_A21, DCI_D6, TLI_G0, EVENTOUT
PE6	5	I/O	5VT	Default: PE6 Alternate: TIMER8_CH1, SPI3_MOSI, SAI0_SD_0, EXMC_A22, DCI_D7, TLI_G1, EVENTOUT
VBAT	6	P	-	Default: VBAT
PI8	7	I/O	5VT	Default: PI8 Alternate: EVENTOUT Additional: RTC_TAMP1, RTC_TAMP0, RTC_TS
PC13-TAMPER-RTC	8	I/O	5VT	Default: PC13 Alternate: SPI0_SCK, EVENTOUT Additional: RTC_TAMP0, RTC_OUT, RTC_TS
PC14-OSC32IN	9	I/O	5VT	Default: PC14 Alternate: EVENTOUT Additional: OSC32IN
PC15-OSC32OUT	10	I/O	5VT	Default: PC15 Alternate: EVENTOUT Additional: OSC32OUT
PI9	11	I/O	5VT	Default: PI9 Alternate: CAN0_RX, EXMC_D30, TLI_VSYNC, EVENTOUT
PI10	12	I/O	5VT	Default: PI10 Alternate: ETH_MII_RX_ER, EXMC_D31, TLI_HSYNC, EVENTOUT
PI11	13	I/O	5VT	Default: PI11 Alternate: USBHS_ULPI_DIR, EVENTOUT
VSS	14	P	-	Default: VSS
VDD	15	P	-	Default: VDD
PF0	16	I/O	5VT	Default: PF0 Alternate: I2C1_SDA, EXMC_A0, CTC_SYNC, I2C4_SDA,

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Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				EVENTOUT
PF1	17	I/O	5VT	Default: PF1 Alternate: I2C1_SCL, EXMC_A1, I2C4_SCL, EVENTOUT
PF2	18	I/O	5VT	Default: PF2 Alternate: I2C1_SMBA, EXMC_A2, I2C4_SMBA, EVENTOUT
PF3	19	I/O	5VT	Default: PF3 Alternate: I2C1_TXFRAME, SPI2_NSS, EXMC_A3, EVENTOUT Additional: ADC2_IN9
PF4	20	I/O	5VT	Default: PF4 Alternate: EXMC_A4, EVENTOUT Additional: ADC2_IN14
PF5	21	I/O	5VT	Default: PF5 Alternate: EXMC_A5, EVENTOUT Additional: ADC2_IN15
VSS	22	P		Default: VSS
VDD	23	P		Default: VDD
PF6	24	I/O	5VT	Default: PF6 Alternate: TIMER9_CH0, SPI4_NSS, SAI0_SD_1, UART6_RX, EXMC_NIORD, EVENTOUT Additional: ADC2_IN4
PF7	25	I/O	5VT	Default: PF7 Alternate: TIMER10_CH0, SPI4_SCK, SAI0_MCLK_1, UART6_TX, EXMC_NREG, EVENTOUT Additional: ADC2_IN5
PF8	26	I/O	5VT	Default: PF8 Alternate: SPI4_MISO, SAI0_SCK_1, TIMER12_CH0, EXMC_NIOWR, EVENTOUT Additional: ADC2_IN6
PF9	27	I/O	5VT	Default: PF9 Alternate: SPI4_MOSI, SAI0_FS_1, TIMER13_CH0, EXMC_CD, EVENTOUT Additional: ADC2_IN7
PF10	28	I/O	5VT	Default: PF10 Alternate: EXMC_INTR, DCI_D11, TLI_DE, I2C5_SMBA, EVENTOUT Additional: ADC2_IN8
PH0/OSCIN	29	I/O	5VT	Default: PH0 Alternate: EVENTOUT Additional: OSCIN
PH1/OSCOUT	30	I/O	5VT	Default: PH1 Alternate: EVENTOUT Additional: OSCOUT
NRST	31	-		Default: NRST

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Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PC0	32	I/O	5VT	Default: PC0 Alternate: SAI0_MCLK_1, USBHS_ULPI_STP, EXMC_SDNWE, TIMER7_CH2_ON, EVENTOUT Additional: ADC012_IN10
PC1	33	I/O	5VT	Default: PC1 Alternate: SPI2_MOSI, I2S2_SD, SAI0_SD_0, SPI1_MOSI, I2S1_SD, ETH_MDC, EVENTOUT Additional: ADC012_IN11
PC2	34	I/O	5VT	Default: PC2 Alternate: SPI1_MISO, I2S1_ADD_SD, USBHS_ULPI_DIR, ETH_MII_TXD2, EXMC_SDNE0, EVENTOUT Additional: ADC012_IN12
PC3	35	I/O	5VT	Default: PC3 Alternate: SPI1_MOSI, I2S1_SD, USBHS_ULPI_NXT, ETH_MII_TX_CLK, EXMC_SDCKE0, EVENTOUT Additional: ADC012_IN13
VDD	36	P		Default: VDD
VSSA	37	P		Default: VSSA
VREFP	38	P	-	Default: VREFP
VDDA	39	P	-	Default: VDDA
PA0-WKUP	40	I/O	5VT	Default: PA0 Alternate: TIMER1_CH0, TIMER1_ETI, TIMER4_CH0, TIMER7_ETI, USART1_CTS, UART3_TX, ETH_MII_CRS, EVENTOUT Additional: ADC012_IN0, WKUP
PA1	41	I/O	5VT	Default: PA1 Alternate: TIMER1_CH1, TIMER4_CH1, SPI3_MOSI, USART1_RTS, UART3_RX, ETH_MII_RX_CLK, ETH_RMII_REF_CLK, EVENTOUT Additional: ADC012_IN1
PA2	42	I/O	5VT	Default: PA2 Alternate: TIMER1_CH2, TIMER4_CH2, TIMER8_CH0, I2S_CKIN, USART1_TX, ETH_MDIO, EVENTOUT Additional: ADC012_IN2
PH2	43	I/O	5VT	Default: PH2 Alternate: ETH_MII_CRS, EXMC_SDCKE0, TLI_R0, EVENTOUT
PH3	44	I/O	5VT	Default: PH3 Alternate: ETH_MII_COL, EXMC_SDNE0, TLI_R1, I2C1_TXFRAME, EVENTOUT
PH4	45	I/O	5VT	Default: PH4 Alternate: I2C1_SCL, USBHS_ULPI_NXT, SPI5_IO3, SPI5_SCK, EVENTOUT
PH5	46	I/O	5VT	Default: PH5 Alternate: I2C1_SDA, SPI4_NSS, EXMC_SDNWE,

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Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				EVENTOUT
PA3	47	I/O	5VT	Default: PA3 Alternate: TIMER1_CH3, TIMER4_CH3, TIMER8_CH1, I2S1_MCK, SAI0_FS_0, USART1_RX, USBHS_ULPI_D0, ETH_MII_COL, TLI_B5, I2C3_SDA, EVENTOUT Additional: ADC012_IN3
NC	48	-	-	-
VDD	49	P	-	Default: VDD
PA4	50	I/O		Default: PA4 Alternate: SPI0_NSS, SPI2_NSS, I2S2_WS, USART1_CK, USBHS_SOF, DCI_HSYNC, TLI_VSYNC, TIMER7_CH1_ON, EVENTOUT Additional: ADC01_IN4, DAC0_OUT0
PA5	51	I/O		Default: PA5 Alternate: TIMER1_CH0, TIMER1_ETI, TIMER7_CH0_ON, SPI0_SCK, USBHS_ULPI_CK, EVENTOUT Additional: ADC01_IN5, DAC0_OUT1
PA6	52	I/O	5VT	Default: PA6 Alternate: TIMER0_BRKIN, TIMER2_CH0, TIMER7_BRKIN, SPI0_MISO, I2S1_MCK, TIMER12_CH0, SDIO_CMD, DCI_PIXCLK, TLI_G2, SPI4_NSS, EVENTOUT Additional: ADC01_IN6
PA7	53	I/O	5VT	Default: PA7 Alternate: TIMER0_CH0_ON, TIMER2_CH1, TIMER7_CH0_ON, SPI0_MOSI, TIMER13_CH0, ETH_MII_RX_DV, ETH_RMII_CRS_DV, EXMC_SDNWE, EVENTOUT Additional: ADC01_IN7
PC4	54	I/O	5VT	Default: PC4 Alternate: ETH_MII_RXD0, ETH_RMII_RXD0, EXMC_SDNE0, EVENTOUT Additional: ADC01_IN14
PC5	55	I/O	5VT	Default: PC5 Alternate: USART2_RX, ETH_MII_RXD1, ETH_RMII_RXD1, EXMC_SDCKE0, EVENTOUT Additional: ADC01_IN15
PB0	56	I/O	5VT	Default: PB0 Alternate: TIMER0_CH1_ON, TIMER2_CH2, TIMER7_CH1_ON, SPI4_SCK, SPI2_MOSI, I2S2_SD, TLI_R3, USBHS_ULPI_D1, ETH_MII_RXD2, SDIO_D1, EVENTOUT Additional: ADC01_IN8, IREF
PB1	57	I/O	5VT	Default: PB1 Alternate: TIMER0_CH2_ON, TIMER2_CH3,

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Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				TIMER7_CH2_ON, SPI4_NSS, TLI_R6, USBHS_ULPI_D2, ETH_MII_RXD3, SDIO_D2, EVENTOUT, TIMER0_CH2 Additional: ADC01_IN9
PB2	58	I/O	5VT	Default: BOOT1 Alternate: TIMER1_CH3, SAI0_SD_0, SPI2_MOSI, I2S2_SD, USBHS_ULPI_D4, SDIO_CK, EVENTOUT
PF11	59	I/O	5VT	Default: PF11 Alternate: SPI4_MOSI, EXMC_SDNRAS, DCI_D12, I2C5_SCL, EVENTOUT
PF12	60	I/O	5VT	Default: PF12 Alternate: EXMC_A6, I2C5_SDA, EVENTOUT
VSS	61	P		Default: VSS
VDD	62	P		Default: VDD
PF13	63	I/O	5VT	Default: PF13 Alternate: EXMC_A7, I2C3_SMBA, EVENTOUT
PF14	64	I/O	5VT	Default: PF14 Alternate: EXMC_A8, I2C3_SCL, SPI1_MOSI, EVENTOUT
PF15	65	I/O	5VT	Default: PF15 Alternate: EXMC_A9, I2C3_SDA, TIMER0_CH3, EVENTOUT
PG0	66	I/O	5VT	Default: PG0 Alternate: EXMC_A10, I2C3_SDA, TIMER0_CH3_ON, EVENTOUT
PG1	67	I/O	5VT	Default: PG1 Alternate: EXMC_A11, I2C3_SCL, TIMER7_CH2, EVENTOUT
PE7	68	I/O	5VT	Default: PE7 Alternate: TIMER0_ETI, UART6_RX, EXMC_D4, TIMER0_CH1, EVENTOUT
PE8	69	I/O	5VT	Default: PE8 Alternate: TIMER0_CH0_ON, UART6_TX, EXMC_D5, SPI5_IO2, USART2_TX, EVENTOUT
PE9	70	I/O	5VT	Default: PE9 Alternate: TIMER0_CH0, EXMC_D6, EVENTOUT
VSS	71	P	-	Default: VSS
VDD	72	P	-	Default: VDD
PE10	73	I/O	5VT	Default: PE10 Alternate: TIMER0_CH1_ON, EXMC_D7, EVENTOUT
PE11	74	I/O	5VT	Default: PE11 Alternate: TIMER0_CH1, SPI3_NSS, SPI4_NSS, EXMC_D8, TLI_G3, EVENTOUT
PE12	75	I/O	5VT	Default: PE12 Alternate: TIMER0_CH2_ON, SPI3_SCK, SPI4_SCK, EXMC_D9, TLI_B4, EVENTOUT
PE13	76	I/O	5VT	Default: PE13 Alternate: TIMER0_CH2, SPI3_MISO, SPI4_MISO,

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Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				EXMC_D10, TLI_DE, EVENTOUT
PE14	77	I/O	5VT	Default: PE14 Alternate: TIMER0_CH3, SPI3_MOSI, SPI4_MOSI, EXMC_D11, TLI_PIXCLK, EVENTOUT
PE15	78	I/O	5VT	Default: PE15 Alternate: TIMER0_BRKIN, EXMC_D12, TLI_R7, EVENTOUT
PB10	79	I/O	5VT	Default: PB10 Alternate: TIMER1_CH2, I2C1_SCL, SPI1_SCK, I2S1_CK, I2S2_MCK, USART2_TX, USBHS_ULPI_D3, ETH_MII_RX_ER, SDIO_D7, TLI_G4, EVENTOUT
PB11	80	I/O	5VT	Default: PB11 Alternate: TIMER1_CH3, I2C1_SDA, I2S_CKIN, USART2_RX, USBHS_ULPI_D4, ETH_MII_TX_EN, ETH_RMII_TX_EN, TLI_G5, EVENTOUT
NC	81	-	-	-
VDD	82	P	-	Default: VDD
PH6	83	I/O	5VT	Default: PH6 Alternate: I2C1_SMBA, SPI4_SCK, TIMER11_CH0, ETH_MII_RXD2, EXMC_SDNE1, DCI_D8, EVENTOUT
PH7	84	I/O	5VT	Default: PH7 Alternate: I2C2_SCL, SPI4_MISO, ETH_MII_RXD3, EXMC_SDCKE1, DCI_D9, EVENTOUT
PH8	85	I/O	5VT	Default: PH8 Alternate: I2C2_SDA, EXMC_D16, DCI_HSYNC, TLI_R2, I2C3_SMBA, EVENTOUT
PH9	86	I/O	5VT	Default: PH9 Alternate: I2C2_SMBA, TIMER11_CH1, EXMC_D17, DCI_D0, TLI_R3, EVENTOUT
PH10	87	I/O	5VT	Default: PH10 Alternate: TIMER4_CH0, EXMC_D18, DCI_D1, TLI_R4, I2C2_TXFRAME, EVENTOUT
PH11	88	I/O	5VT	Default: PH11 Alternate: TIMER4_CH1, EXMC_D19, DCI_D2, TLI_R5, I2C3_SCL, EVENTOUT
PH12	89	I/O	5VT	Default: PH12 Alternate: TIMER4_CH2, EXMC_D20, DCI_D3, TLI_R6, I2C3_SDA, EVENTOUT
VSS	90	P	-	Default: VSS
VDD	91	P	-	Default: VDD
PB12	92	I/O	5VT	Default: PB12 Alternate: TIMER0_BRKIN, I2C1_SMBA, SPI1_NSS, I2S1_WS, SPI3_NSS, USART2_CK, CAN1_RX, USBHS_ULPI_D5, ETH_MII_TXD0, ETH_RMII_TXD0, USBHS_ID, SPI5_MISO, EVENTOUT

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GD32F527Ix LQFP176				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PB13	93	I/O	5VT	Default: PB13 Alternate: TIMER0_CH0_ON, SPI1_SCK, I2S1_CK, SPI3_SCK, USART2_CTS, CAN1_TX, USBHS_ULPI_D6, ETH_MII_TXD1, ETH_RMII_TXD1, I2C1_TXFRAME, EVENTOUT Additional: USBHS_VBUS
PB14	94	I/O	5VT	Default: PB14 Alternate: TIMER0_CH1_ON, TIMER7_CH1_ON, SPI1_MISO, I2S1_ADD_SD, USART2_RTS, TIMER11_CH0, USBHS_DM, EVENTOUT
PB15	95	I/O	5VT	Default: PB15 Alternate: RTC_REFIN, TIMER0_CH2_ON, TIMER7_CH2_ON, SPI1_MOSI, I2S1_SD, TIMER11_CH1, USBHS_DP, EVENTOUT
PD8	96	I/O	5VT	Default: PD8 Alternate: USART2_TX, EXMC_D13, EVENTOUT
PD9	97	I/O	5VT	Default: PD9 Alternate: USART2_RX, EXMC_D14, SPI2_NSS, EVENTOUT
PD10	98	I/O	5VT	Default: PD10 Alternate: USART2_CK, EXMC_D15, TLI_B3, SPI5_SCK, EVENTOUT
PD11	99	I/O	5VT	Default: PD11 Alternate: USART2_CTS, EXMC_A16, EXMC_CLE, EVENTOUT
PD12	100	I/O	5VT	Default: PD12 Alternate: TIMER3_CH0, USART2_RTS, EXMC_A17, EXMC_ALE, TIMER0_CH1, EVENTOUT
PD13	101	I/O	5VT	Default: PD13 Alternate: TIMER3_CH1, EXMC_A18, EVENTOUT
VSS	102	P	-	Default: VSS
VDD	103	P	-	Default: VDD
PD14	104	I/O	5VT	Default: PD14 Alternate: TIMER3_CH2, EXMC_D0, TIMER7_CH1, EVENTOUT
PD15	105	I/O	5VT	Default: PD15 Alternate: TIMER3_CH3, EXMC_D1, CTC_SYNC, USART2_RX, EVENTOUT
PG2	106	I/O	5VT	Default: PG2 Alternate: EXMC_A12, EVENTOUT
PG3	107	I/O	5VT	Default: PG3 Alternate: EXMC_A13, EVENTOUT
PG4	108	I/O	5VT	Default: PG4 Alternate: EXMC_A14, SPI5_NSS, EVENTOUT
PG5	109	I/O	5VT	Default: PG5

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Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Alternate: EXMC_A15, EVENTOUT
PG6	110	I/O	5VT	Default: PG6 Alternate: EXMC_INT1, DCI_D12, TLI_R7, I2C4_SMBA, EVENTOUT
PG7	111	I/O	5VT	Default: PG7 Alternate: USART5_CK, EXMC_INT2, DCI_D13, TLI_PIXCLK, I2C4_SCL, EVENTOUT
PG8	112	I/O	5VT	Default: PG8 Alternate: SPI5_NSS, USART5_RTS, ETH_PPS_OUT, EXMC_SDCLK, I2C4_SDA, EVENTOUT
VSS	113	P	-	Default: VSS
VDD	114	P	-	Default: VDD
PC6	115	I/O	5VT	Default: PC6 Alternate: TIMER2_CH0, TIMER7_CH0, I2S1_MCK, USART5_TX, SDIO_D6, DCI_D0, TLI_HSYNC, TIMER7_CH0_ON, EVENTOUT
PC7	116	I/O	5VT	Default: PC7 Alternate: TIMER2_CH1, TIMER7_CH1, SPI1_SCK, I2S1_CK, I2S2_MCK, USART5_RX, SDIO_D7, DCI_D1, TLI_G6, EVENTOUT
PC8	117	I/O	5VT	Default: PC8 Alternate: TIMER2_CH2, TIMER7_CH2, USART5_CK, SDIO_D0, DCI_D2, EVENTOUT
PC9	118	I/O	5VT	Default: PC9 Alternate: CK_OUT1, TIMER2_CH3, TIMER7_CH3, I2C2_SDA, I2S_CKIN, SDIO_D1, DCI_D3, TIMER0_CH1_ON, EVENTOUT
PA8	119	I/O	5VT	Default: PA8 Alternate: CK_OUT0, TIMER0_CH0, I2C2_SCL, USART0_CK, USBFS_SOF, SDIO_D1, TLI_R6, CTC_SYNC, EVENTOUT
PA9	120	I/O	5VT	Default: PA9 Alternate: TIMER0_CH1, I2C2_SMBA, SPI1_SCK, I2S1_CK, SAI0_SD_1, USART0_TX, SDIO_D2, DCI_D0, EVENTOUT Additional: USBFS_VBUS
PA10	121	I/O	5VT	Default: PA10 Alternate: TIMER0_CH2, SPI4_MOSI, USART0_RX, USBFS_ID, DCI_D1, I2C2_TXFRAME, EVENTOUT
PA11	122	I/O	5VT	Default: PA11 Alternate: TIMER0_CH3, SPI3_MISO, USART0_CTS, USART5_TX, CAN0_RX, USBFS_DM, TLI_R4, EVENTOUT
PA12	123	I/O	5VT	Default: PA12 Alternate: TIMER0_ETI, SPI4_MISO, USART0_RTS, USART5_RX, CAN0_TX, USBFS_DP, TLI_R5, EVENTOUT
PA13	124	I/O	5VT	Default: JTMS, SWDIO, PA13

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Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Alternate: EVENTOUT
NC	125	-	-	-
VSS	126	P	-	Default: VSS
VDD	127	P	-	Default: VDD
PH13	128	I/O	5VT	Default: PH13 Alternate: TIMER7_CH0_ON, CAN0_TX, EXMC_D21, TLI_G2, EVENTOUT
PH14	129	I/O	5VT	Default: PH14 Alternate: TIMER7_CH1_ON, EXMC_D22, DCI_D4, TLI_G3, I2C5_SCL, EVENTOUT
PH15	130	I/O	5VT	Default: PH15 Alternate: TIMER7_CH2_ON, EXMC_D23, DCI_D11, TLI_G4, I2C5_SDA, EVENTOUT
PI0	131	I/O	5VT	Default: PI0 Alternate: TIMER4_CH3, SPI1_NSS, I2S1_WS, EXMC_D24, DCI_D13, TLI_G5, SPI1_NSS, EVENTOUT
PI1	132	I/O	5VT	Default: PI1 Alternate: SPI1_SCK, I2S1_CK, EXMC_D25, DCI_D8, TLI_G6, SPI1_NSS, EVENTOUT
PI2	133	I/O	5VT	Default: PI2 Alternate: TIMER7_CH3, SPI1_MISO, I2S1_ADD_SD, EXMC_D26, DCI_D9, TLI_G7, EVENTOUT
PI3	134	I/O	5VT	Default: PI3 Alternate: TIMER7_ETI, SPI1_MOSI, I2S1_SD, EXMC_D27, DCI_D10, TIMER0_CH0, EVENTOUT
VSS	135	P	-	Default: VSS
VDD	136	P	-	Default: VDD
PA14	137	I/O	5VT	Default: JTCK, SWCLK, PA14 Alternate: EVENTOUT
PA15	138	I/O	5VT	Default: JTDI/PA15 Alternate: TIMER1_CH0, TIMER1_ETI, SPI0_NSS, SPI2_NSS, I2S2_WS, USART0_TX, EVENTOUT
PC10	139	I/O	5VT	Default: PC10 Alternate: SPI2_SCK, I2S2_CK, USART2_TX, UART3_TX, SDIO_D2, DCI_D8, TLI_R2, EVENTOUT
PC11	140	I/O	5VT	Default: PC11 Alternate: I2S2_ADD_SD, SPI2_MISO, USART2_RX, UART3_RX, SDIO_D3, DCI_D4, EVENTOUT
PC12	141	I/O	5VT	Default: PC12 Alternate: I2C1_SDA, SPI2_MOSI, I2S2_SD, USART2_CK, UART4_TX, SDIO_CK, DCI_D9, EVENTOUT
PD0	142	I/O	5VT	Default: PD0 Alternate: SPI3_MISO, SPI2_MOSI, I2S2_SD, CAN0_RX, EXMC_D2, EVENTOUT
PD1	143	I/O	5VT	Default: PD1

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Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Alternate: SPI1_NSS, I2S1_WS, CAN0_TX, EXMC_D3, TIMER7_CH3_ON, EVENTOUT
PD2	144	I/O	5VT	Default: PD2 Alternate: TIMER2_ETI, UART4_RX, SDIO_CMD, DCI_D11, EVENTOUT
PD3	145	I/O	5VT	Default: PD3 Alternate: SPI1_SCK, I2S1_CK, USART1_CTS, EXMC_CLK, DCI_D5, TLI_G7, EVENTOUT
PD4	146	I/O	5VT	Default: PD4 Alternate: USART1_RTS, EXMC_NOE, EVENTOUT, I2C3_SCL
PD5	147	I/O	5VT	Default: PD5 Alternate: USART1_TX, EXMC_NWE, EVENTOUT
VSS	148	P	-	Default: VSS
VDD	149	P	-	Default: VDD
PD6	150	I/O	5VT	Default: PD6 Alternate: SPI2_MOSI, I2S2_SD, SAI0_SD_0, USART1_RX, EXMC_NWAIT, DCI_D10, TLI_B2, TIMER0_CH2_ON, EVENTOUT
PD7	151	I/O	5VT	Default: PD7 Alternate: USART1_CK, EXMC_NE0, EXMC_NCE1, EVENTOUT
PG9	152	I/O	5VT	Default: PG9 Alternate: USART5_RX, EXMC_NE1, EXMC_NCE2, DCI_VSYNC, EVENTOUT
PG10	153	I/O	5VT	Default: PG10 Alternate: SPI5_IO2, TLI_G3, EXMC_NCE3_0, EXMC_NE2, DCI_D2, TLI_B2, EVENTOUT
PG11	154	I/O	5VT	Default: PG11 Alternate: SPI5_IO3, SPI3_SCK, ETH_MII_TX_EN, ETH_RMII_TX_EN, EXMC_NCE3_1, DCI_D3, TLI_B3, EVENTOUT
PG12	155	I/O	5VT	Default: PG12 Alternate: SPI5_MISO, SPI3_MISO, USART5_RTS, TLI_B4, EXMC_NE3, TLI_B1, EVENTOUT
PG13	156	I/O	5VT	Default: PG13 Alternate: SPI5_SCK, SPI3_MOSI, USART5_CTS, ETH_MII_TXD0, ETH_RMII_TXD0, EXMC_A24, EVENTOUT
PG14	157	I/O	5VT	Default: PG14 Alternate: SPI5_MOSI, SPI3_NSS, USART5_TX, ETH_MII_TXD1, ETH_RMII_TXD1, EXMC_A25, I2C4_SCL, EVENTOUT
VSS	158	P	-	Default: VSS
VDD	159	P	-	Default: VDD
PG15	160	I/O	5VT	Default: PG15

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Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Alternate: USART5_CTS, EXMC_SDNCAS, DCI_D13, I2C5_SMBA, EVENTOUT
PB3	161	I/O	5VT	Default: JTDO, PB3 Alternate: TRACESWO, TIMER1_CH1, SPI0_SCK, SPI2_SCK, I2S2_CK, USART0_RX, I2C1_SDA, EVENTOUT
PB4	162	I/O	5VT	Default: NJTRST Alternate: TIMER2_CH0, SPI0_MISO, SPI2_MISO, I2S2_ADD_SD, I2C2_SDA, SDIO_D0, I2C0_TXFRAME, TIMER7_CH0, EVENTOUT
PB5	163	I/O	5VT	Default: PB5 Alternate: TIMER2_CH1, I2C0_SMBA, SPI0_MOSI, SPI2_MOSI, I2S2_SD, CAN1_RX, USBHS_ULPI_D7, ETH_PPS_OUT, EXMC_SDCKE1, DCI_D10, SPI0_NSS, EVENTOUT
PB6	164	I/O	5VT	Default: PB6 Alternate: TIMER3_CH0, I2C0_SCL, SPI5_MOSI, USART0_TX, CAN1_TX, EXMC_SDNE1, DCI_D5, EVENTOUT
PB7	165	I/O	5VT	Default: PB7 Alternate: TIMER3_CH1, I2C0_SDA, USART0_RX, EXMC_NL, EXMC_NADV, DCI_VSYNC, EVENTOUT
BOOT0	166	I/O		Default: BOOT0
PB8	167	I/O	5VT	Default: PB8 Alternate: TIMER1_CH0, TIMER1_ETI, TIMER3_CH2, TIMER9_CH0, I2C0_SCL, SPI5_NSS, SPI4_MOSI, CAN0_RX, ETH_MII_TXD3, SDIO_D4, DCI_D6, TLI_B6, EVENTOUT
PB9	168	I/O	5VT	Default: PB9 Alternate: TIMER1_CH1, TIMER3_CH3, TIMER10_CH0, I2C0_SDA, SPI1_NSS, I2S1_WS, SAI0_FS_1, CAN0_TX, SDIO_D5, DCI_D7, TLI_B7, EVENTOUT
PE0	169	I/O	5VT	Default: PE0 Alternate: TIMER3_ETI, SPI0_MOSI, UART7_RX, EXMC_NBL0, DCI_D2, EVENTOUT
PE1	170	I/O	5VT	Default: PE1 Alternate: TIMER0_CH1_ON, UART7_TX, EXMC_NBL1, DCI_D3, TIMER7_CH3, EVENTOUT
PDR_ON	171	P	-	Default: PDR_ON(3)
VDD	172	P	-	Default: VDD
PI4	173	I/O	5VT	Default: PI4 Alternate: TIMER7_BRKIN, SPI4_MOSI, EXMC_NBL2, DCI_D5, TLI_B4, EVENTOUT
PI5	174	I/O	5VT	Default: PI5 Alternate: TIMER7_CH0, EXMC_NBL3, DCI_VSYNC, TLI_B5, SPI2_MOSI, I2C5_SCL, EVENTOUT

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Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PI6	175	I/O	5VT	Default: PI6 Alternate: TIMER7_CH1, EXMC_D28, DCI_D6, TLI_B6, EVENTOUT
PI7	176	I/O	5VT	Default: PI7 Alternate: TIMER7_CH2, EXMC_D29, DCI_D7, TLI_B7, I2C5_SDA, EVENTOUT

Notes:

(1) Type: I = input, O = output, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

(3) PDR_ON pin should be pulled up to V_{DD}, refer to ***Figure 4-2. Recommended PDR_ON pin circuit***.

2.6.2. GD32F527Ix BGA176 pin definitions

Table 2-5. GD32F527Ix BGA176 pin definitions(4)

GD32F527Ix BGA176(4)				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PE2	A2	I/O	5VT	Default: PE2 Alternate: SPI3_SCK, SAI0_MCLK_0, ETH_MII_TXD3, EXMC_A23, EVENTOUT
PE3	A1	I/O	5VT	Default: PE3 Alternate: SAI0_SD_1, EXMC_A19, EVENTOUT
PE4	B1	I/O	5VT	Default: PE4 Alternate: SPI3_NSS, SAI0_FS_0, EXMC_A20, DCI_D4, TLI_B0, EVENTOUT
PE5	B2	I/O	5VT	Default: PE5 Alternate: TIMER8_CH0, SPI3_MISO, SAI0_SCK_0, SPI0_MISO, EXMC_A21, DCI_D6, TLI_G0, EVENTOUT
PE6	B3	I/O	5VT	Default: PE6 Alternate: TIMER8_CH1, SPI3_MOSI, SAI0_SD_0, EXMC_A22, DCI_D7, TLI_G1, EVENTOUT
VBAT	C1	P	-	Default: VBAT
PI8	D2	I/O	5VT	Default: PI8 Alternate: EVENTOUT Additional: RTC_TAMP1, RTC_TAMP0, RTC_TS
PC13-TAMPER-RTC	D1	I/O	5VT	Default: PC13 Alternate: SPI0_SCK, EVENTOUT Additional: RTC_TAMP0, RTC_OUT, RTC_TS
PC14-OSC32IN	E1	I/O	5VT	Default: PC14 Alternate: EVENTOUT Additional: OSC32IN

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Pin Name	**Pins**	**Pin Type[1]**	**I/O Level[2]**	**Functions description**
PC15-OSC32OUT	F1	I/O	5VT	Default: PC15 Alternate: EVENTOUT Additional: OSC32OUT
PI9	D3	I/O	5VT	Default: PI9 Alternate: CAN0_RX, EXMC_D30, TLI_VSYNC, EVENTOUT
PI10	E3	I/O	5VT	Default: PI10 Alternate: ETH_MII_RX_ER, EXMC_D31, TLI_HSYNC, EVENTOUT
PI11	E4	I/O	5VT	Default: PI11 Alternate: USBHS_ULPI_DIR, EVENTOUT
VSS	F2	P	-	Default: VSS
VDD	F3	P	-	Default: VDD
PF0	E2	I/O	5VT	Default: PF0 Alternate: I2C1_SDA, EXMC_A0, CTC_SYNC, I2C4_SDA, EVENTOUT
PF1	H3	I/O	5VT	Default: PF1 Alternate: I2C1_SCL, EXMC_A1, I2C4_SCL, EVENTOUT
PF2	H2	I/O	5VT	Default: PF2 Alternate: I2C1_SMBA, EXMC_A2, I2C4_SMBA, EVENTOUT
PF3	J2	I/O	5VT	Default: PF3 Alternate: I2C1_TXFRAME, SPI2_NSS, EXMC_A3, EVENTOUT Additional: ADC2_IN9
PF4	J3	I/O	5VT	Default: PF4 Alternate: EXMC_A4, EVENTOUT Additional: ADC2_IN14
PF5	K3	I/O	5VT	Default: PF5 Alternate: EXMC_A5, EVENTOUT Additional: ADC2_IN15
VSS	G2	P	-	Default: VSS
VDD	G3	P	-	Default: VDD
PF6	K2	I/O	5VT	Default: PF6 Alternate: TIMER9_CH0, SPI4_NSS, SAI0_SD_1, UART6_RX, EXMC_NIORD, EVENTOUT Additional: ADC2_IN4
PF7	K1	I/O	5VT	Default: PF7 Alternate: TIMER10_CH0, SPI4_SCK, SAI0_MCLK_1, UART6_TX, EXMC_NREG, EVENTOUT Additional: ADC2_IN5
PF8	L3	I/O	5VT	Default: PF8 Alternate: SPI4_MISO, SAI0_SCK_1, TIMER12_CH0, EXMC_NIOWR, EVENTOUT

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Pin Name	**Pins**	**Pin Type[1]**	**I/O Level[2]**	**Functions description**
				Additional: ADC2_IN6
PF9	L2	I/O	5VT	Default: PF9 Alternate: SPI4_MOSI, SAI0_FS_1, TIMER13_CH0, EXMC_CD, EVENTOUT Additional: ADC2_IN7
PF10	L1	I/O	5VT	Default: PF10 Alternate: EXMC_INTR, DCI_D11, TLI_DE, I2C5_SMBA, EVENTOUT Additional: ADC2_IN8
PH0/OSCIN	G1	I/O	5VT	Default: PH0, OSCIN Alternate: EVENTOUT Additional: OSCIN
PH1/OSCOUT	H1	I/O	5VT	Default: PH1, OSCOUT Alternate: EVENTOUT Additional: OSCOUT
NRST	J1	-	-	Default: NRST
PC0	M2	I/O	5VT	Default: PC0 Alternate: SAI0_MCLK_1, USBHS_ULPI_STP, EXMC_SDNWE, TIMER7_CH2_ON, EVENTOUT Additional: ADC012_IN10
PC1	M3	I/O	5VT	Default: PC1 Alternate: SPI2_MOSI, I2S2_SD, SAI0_SD_0, SPI1_MOSI, I2S1_SD, ETH_MDC, EVENTOUT Additional: ADC012_IN11
PC2	M4	I/O	5VT	Default: PC2 Alternate: SPI1_MISO, I2S1_ADD_SD, USBHS_ULPI_DIR, ETH_MII_TXD2, EXMC_SDNE0, EVENTOUT Additional: ADC012_IN12
PC3	M5	I/O	5VT	Default: PC3 Alternate: SPI1_MOSI, I2S1_SD, USBHS_ULPI_NXT, ETH_MII_TX_CLK, EXMC_SDCKE0, EVENTOUT Additional: ADC012_IN13
VSSA	M1	P	-	Default: VSSA
VREFN	N1	P	-	Default: VREFN
VREFP	P1	P	-	Default: VREFP
VDDA	R1	P	-	Default: VDDA
PA0-WKUP	N3	I/O	5VT	Default: PA0 Alternate: TIMER1_CH0, TIMER1_ETI, TIMER4_CH0, TIMER7_ETI, USART1_CTS, UART3_TX, ETH_MII_CRS, EVENTOUT Additional: ADC012_IN0, WKUP
PA1	N2	I/O	5VT	Default: PA1 Alternate: TIMER1_CH1, TIMER4_CH1, SPI3_MOSI,

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Pin Name	**Pins**	**Pin Type[1]**	**I/O Level[2]**	**Functions description**
				USART1_RTS, UART3_RX, ETH_MII_RX_CLK, ETH_RMII_REF_CLK, EVENTOUT Additional: ADC012_IN1
PA2	P2	I/O	5VT	Default: PA2 Alternate: TIMER1_CH2, TIMER4_CH2, TIMER8_CH0, I2S_CKIN, USART1_TX, ETH_MDIO, EVENTOUT Additional: ADC012_IN2
PH2	F4	I/O	5VT	Default: PH2 Alternate: ETH_MII_CRS, EXMC_SDCKE0, TLI_R0, EVENTOUT
PH3	G4	I/O	5VT	Default: PH3 Alternate: ETH_MII_COL, EXMC_SDNE0, TLI_R1, I2C1_TXFRAME, EVENTOUT
PH4	H4	I/O	5VT	Default: PH4 Alternate: I2C1_SCL, USBHS_ULPI_NXT, SPI5_IO3, SPI5_SCK, EVENTOUT
PH5	J4	I/O	5VT	Default: PH5 Alternate: I2C1_SDA, SPI4_NSS, EXMC_SDNWE, EVENTOUT
PA3	R2	I/O	5VT	Default: PA3 Alternate: TIMER1_CH3, TIMER4_CH3, TIMER8_CH1, I2S1_MCK, SAI0_FS_0, USART1_RX, USBHS_ULPI_D0, ETH_MII_COL, TLI_B5, I2C3_SDA, EVENTOUT Additional: ADC012_IN3
NC	L4	-	-	-
VDD	K4	P	-	Default: VDD
PA4	N4	I/O		Default: PA4 Alternate: SPI0_NSS, SPI2_NSS, I2S2_WS, USART1_CK, USBHS_SOF, DCI_HSYNC, TLI_VSYNC, TIMER7_CH1_ON, EVENTOUT Additional: ADC01_IN4, DAC0_OUT0
PA5	P4	I/O		Default: PA5 Alternate: TIMER1_CH0, TIMER1_ETI, TIMER7_CH0_ON, SPI0_SCK, USBHS_ULPI_CK, EVENTOUT Additional: ADC01_IN5, DAC0_OUT1
PA6	P3	I/O	5VT	Default: PA6 Alternate: TIMER0_BRKIN, TIMER2_CH0, TIMER7_BRKIN, SPI0_MISO, I2S1_MCK, TIMER12_CH0, SDIO_CMD, DCI_PIXCLK, TLI_G2, SPI4_NSS, EVENTOUT Additional: ADC01_IN6
PA7	R3	I/O	5VT	Default: PA7 Alternate: TIMER0_CH0_ON, TIMER2_CH1, TIMER7_CH0_ON, SPI0_MOSI, TIMER13_CH0, ETH_MII_RX_DV, ETH_RMII_CRS_DV, EXMC_SDNWE,

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Pin Name	**Pins**	**Pin Type[1]**	**I/O Level[2]**	**Functions description**
				EVENTOUT Additional: ADC01_IN7
PC4	N5	I/O	5VT	Default: PC4 Alternate: ETH_MII_RXD0, ETH_RMII_RXD0, EXMC_SDNE0, EVENTOUT Additional: ADC01_IN14
PC5	P5	I/O	5VT	Default: PC5 Alternate: USART2_RX, ETH_MII_RXD1, ETH_RMII_RXD1, EXMC_SDCKE0, EVENTOUT Additional: ADC01_IN15
PB0	R5	I/O	5VT	Default: PB0 Alternate: TIMER0_CH1_ON, TIMER2_CH2, TIMER7_CH1_ON, SPI4_SCK, SPI2_MOSI, I2S2_SD, TLI_R3, USBHS_ULPI_D1, ETH_MII_RXD2, SDIO_D1, EVENTOUT Additional: ADC01_IN8, IREF
PB1	R4	I/O	5VT	Default: PB1 Alternate: TIMER0_CH2_ON, TIMER2_CH3, TIMER7_CH2_ON, SPI4_NSS, TLI_R6, USBHS_ULPI_D2, ETH_MII_RXD3, SDIO_D2, EVENTOUT, TIMER0_CH2 Additional: ADC01_IN9
PB2	M6	I/O	5VT	Default: BOOT1 Alternate: TIMER1_CH3, SAI0_SD_0, SPI2_MOSI, I2S2_SD, USBHS_ULPI_D4, SDIO_CK, EVENTOUT
PF11	R6	I/O	5VT	Default: PF11 Alternate: SPI4_MOSI, EXMC_SDNRAS, DCI_D12, I2C5_SCL, EVENTOUT
PF12	P6	I/O	5VT	Default: PF12 Alternate: EXMC_A6, I2C5_SDA, EVENTOUT
VSS	M8	P	-	Default: VSS
VDD	N8	P	-	Default: VDD
PF13	N6	I/O	5VT	Default: PF13 Alternate: EXMC_A7, I2C3_SMBA, EVENTOUT
PF14	R7	I/O	5VT	Default: PF14 Alternate: EXMC_A8, I2C3_SCL, SPI1_MOSI, EVENTOUT
PF15	P7	I/O	5VT	Default: PF15 Alternate: EXMC_A9, I2C3_SDA, TIMER0_CH3, EVENTOUT
PG0	N7	I/O	5VT	Default: PG0 Alternate: EXMC_A10, I2C3_SDA, TIMER0_CH3_ON, EVENTOUT
PG1	M7	I/O	5VT	Default: PG1 Alternate: EXMC_A11, I2C3_SCL, TIMER7_CH2,

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Pin Name	**Pins**	**Pin Type[1]**	**I/O Level[2]**	**Functions description**
				EVENTOUT
PE7	R8	I/O	5VT	Default: PE7 Alternate: TIMER0_ETI, UART6_RX, EXMC_D4, TIMER0_CH1, EVENTOUT
PE8	P8	I/O	5VT	Default: PE8 Alternate: TIMER0_CH0_ON, UART6_TX, EXMC_D5, SPI5_IO2, USART2_TX, EVENTOUT
PE9	P9	I/O	5VT	Default: PE9 Alternate: TIMER0_CH0, EXMC_D6, EVENTOUT
VSS	M9	P	-	Default: VSS
VDD	N9	P	-	Default: VDD
PE10	R9	I/O	5VT	Default: PE10 Alternate: TIMER0_CH1_ON, EXMC_D7, EVENTOUT
PE11	P10	I/O	5VT	Default: PE11 Alternate: TIMER0_CH1, SPI3_NSS, SPI4_NSS, EXMC_D8, TLI_G3, EVENTOUT
PE12	R10	I/O	5VT	Default: PE12 Alternate: TIMER0_CH2_ON, SPI3_SCK, SPI4_SCK, EXMC_D9, TLI_B4, EVENTOUT
PE13	N11	I/O	5VT	Default: PE13 Alternate: TIMER0_CH2, SPI3_MISO, SPI4_MISO, EXMC_D10, TLI_DE, EVENTOUT
PE14	P11	I/O	5VT	Default: PE14 Alternate: TIMER0_CH3, SPI3_MOSI, SPI4_MOSI, EXMC_D11, TLI_PIXCLK, EVENTOUT
PE15	R11	I/O	5VT	Default: PE15 Alternate: TIMER0_BRKIN, EXMC_D12, TLI_R7, EVENTOUT
PB10	R12	I/O	5VT	Default: PB10 Alternate: TIMER1_CH2, I2C1_SCL, SPI1_SCK, I2S1_CK, I2S2_MCK, USART2_TX, USBHS_ULPI_D3, ETH_MII_RX_ER, SDIO_D7, TLI_G4, EVENTOUT
PB11	R13	I/O	5VT	Default: PB11 Alternate: TIMER1_CH3, I2C1_SDA, I2S_CKIN, USART2_RX, USBHS_ULPI_D4, ETH_MII_TX_EN, ETH_RMII_TX_EN, TLI_G5, EVENTOUT
NC	M10	-	-	-
VDD	N10	P	-	Default: VDD
PH6	M11	I/O	5VT	Default: PH6 Alternate: I2C1_SMBA, SPI4_SCK, TIMER11_CH0, ETH_MII_RXD2, EXMC_SDNE1, DCI_D8, EVENTOUT
PH7	N12	I/O	5VT	Default: PH7

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Pin Name	**Pins**	**Pin Type[1]**	**I/O Level[2]**	**Functions description**
				Alternate: I2C2_SCL, SPI4_MISO, ETH_MII_RXD3, EXMC_SDCKE1, DCI_D9, EVENTOUT
PH8	M12	I/O	5VT	Default: PH8 Alternate: I2C2_SDA, EXMC_D16, DCI_HSYNC, TLI_R2, I2C3_SMBA, EVENTOUT
PH9	M13	I/O	5VT	Default: PH9 Alternate: I2C2_SMBA, TIMER11_CH1, EXMC_D17, DCI_D0, TLI_R3, EVENTOUT
PH10	L13	I/O	5VT	Default: PH10 Alternate: TIMER4_CH0, EXMC_D18, DCI_D1, TLI_R4, I2C2_TXFRAME, EVENTOUT
PH11	L12	I/O	5VT	Default: PH11 Alternate: TIMER4_CH1, EXMC_D19, DCI_D2, TLI_R5, I2C3_SCL, EVENTOUT
PH12	K12	I/O	5VT	Default: PH12 Alternate: TIMER4_CH2, EXMC_D20, DCI_D3, TLI_R6, I2C3_SDA, EVENTOUT
VSS	H12	P	-	Default: VSS
VDD	J12	P	-	Default: VDD
PB12	P12	I/O	5VT	Default: PB12 Alternate: TIMER0_BRKIN, I2C1_SMBA, SPI1_NSS, I2S1_WS, SPI3_NSS, USART2_CK, CAN1_RX, USBHS_ULPI_D5, ETH_MII_TXD0, ETH_RMII_TXD0, USBHS_ID, SPI5_MISO, EVENTOUT
PB13	P13	I/O	5VT	Default: PB13 Alternate: TIMER0_CH0_ON, SPI1_SCK, I2S1_CK, SPI3_SCK, USART2_CTS, CAN1_TX, USBHS_ULPI_D6, ETH_MII_TXD1, ETH_RMII_TXD1, I2C1_TXFRAME, EVENTOUT Additional: USBHS_VBUS
PB14	R14	I/O	5VT	Default: PB14 Alternate: TIMER0_CH1_ON, TIMER7_CH1_ON, SPI1_MISO, I2S1_ADD_SD, USART2_RTS, TIMER11_CH0, USBHS_DM, EVENTOUT
PB15	R15	I/O	5VT	Default: PB15 Alternate: RTC_REFIN, TIMER0_CH2_ON, TIMER7_CH2_ON, SPI1_MOSI, I2S1_SD, TIMER11_CH1, USBHS_DP, EVENTOUT
PD8	P15	I/O	5VT	Default: PD8 Alternate: USART2_TX, EXMC_D13, EVENTOUT
PD9	P14	I/O	5VT	Default: PD9 Alternate: USART2_RX, EXMC_D14, SPI2_NSS,

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Pin Name	**Pins**	**Pin Type[1]**	**I/O Level[2]**	**Functions description**
				EVENTOUT
PD10	N15	I/O	5VT	Default: PD10 Alternate: USART2_CK, EXMC_D15, TLI_B3, SPI5_SCK, EVENTOUT
PD11	N14	I/O	5VT	Default: PD11 Alternate: USART2_CTS, EXMC_A16, EXMC_CLE, EVENTOUT
PD12	N13	I/O	5VT	Default: PD12 Alternate: TIMER3_CH0, USART2_RTS, EXMC_A17, EXMC_ALE, TIMER0_CH1, EVENTOUT
PD13	M15	I/O	5VT	Default: PD13 Alternate: TIMER3_CH1, EXMC_A18, EVENTOUT
VDD	J13	P	-	Default: VDD
PD14	M14	I/O	5VT	Default: PD14 Alternate: TIMER3_CH2, EXMC_D0, TIMER7_CH1, EVENTOUT
PD15	L14	I/O	5VT	Default: PD15 Alternate: TIMER3_CH3, EXMC_D1, CTC_SYNC, USART2_RX, EVENTOUT
PG2	L15	I/O	5VT	Default: PG2 Alternate: EXMC_A12, EVENTOUT
PG3	K15	I/O	5VT	Default: PG3 Alternate: EXMC_A13, EVENTOUT
PG4	K14	I/O	5VT	Default: PG4 Alternate: EXMC_A14, SPI5_NSS, EVENTOUT
PG5	K13	I/O	5VT	Default: PG5 Alternate: EXMC_A15, EVENTOUT
PG6	J15	I/O	5VT	Default: PG6 Alternate: EXMC_INT1, DCI_D12, TLI_R7, I2C4_SMBA, EVENTOUT
PG7	J14	I/O	5VT	Default: PG7 Alternate: USART5_CK, EXMC_INT2, DCI_D13, TLI_PIXCLK, I2C4_SCL, EVENTOUT
PG8	H14	I/O	5VT	Default: PG8 Alternate: SPI5_NSS, USART5_RTS, ETH_PPS_OUT, EXMC_SDCLK, I2C4_SDA, EVENTOUT
VSS	G12	P	-	Default: VSS
VDD	H13	P	-	Default: VDD
PC6	H15	I/O	5VT	Default: PC6 Alternate: TIMER2_CH0, TIMER7_CH0, I2S1_MCK, USART5_TX, SDIO_D6, DCI_D0, TLI_HSYNC, TIMER7_CH0_ON, EVENTOUT

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Pin Name	**Pins**	**Pin Type[1]**	**I/O Level[2]**	**Functions description**
PC7	G15	I/O	5VT	Default: PC7 Alternate: TIMER2_CH1, TIMER7_CH1, SPI1_SCK, I2S1_CK, I2S2_MCK, USART5_RX, SDIO_D7, DCI_D1, TLI_G6, EVENTOUT
PC8	G14	I/O	5VT	Default: PC8 Alternate: TIMER2_CH2, TIMER7_CH2, USART5_CK, SDIO_D0, DCI_D2, EVENTOUT
PC9	F14	I/O	5VT	Default: PC9 Alternate: CK_OUT1, TIMER2_CH3, TIMER7_CH3, I2C2_SDA, I2S_CKIN, SDIO_D1, DCI_D3, TIMER0_CH1_ON, EVENTOUT
PA8	F15	I/O	5VT	Default: PA8 Alternate: CK_OUT0, TIMER0_CH0, I2C2_SCL, USART0_CK, USBFS_SOF, SDIO_D1, TLI_R6, CTC_SYNC, EVENTOUT
PA9	E15	I/O	5VT	Default: PA9 Alternate: TIMER0_CH1, I2C2_SMBA, SPI1_SCK, I2S1_CK, SAI0_SD_1, USART0_TX, SDIO_D2, DCI_D0, EVENTOUT Additional: USBFS_VBUS
PA10	D15	I/O	5VT	Default: PA10 Alternate: TIMER0_CH2, SPI4_MOSI, USART0_RX, USBFS_ID, DCI_D1, I2C2_TXFRAME, EVENTOUT
PA11	C15	I/O	5VT	Default: PA11 Alternate: TIMER0_CH3, SPI3_MISO, USART0_CTS, USART5_TX, CAN0_RX, USBFS_DM, TLI_R4, EVENTOUT
PA12	B15	I/O	5VT	Default: PA12 Alternate: TIMER0_ETI, SPI4_MISO, USART0_RTS, USART5_RX, CAN0_TX, USBFS_DP, TLI_R5, EVENTOUT
PA13	A15	I/O	5VT	Default: JTMS, SWDIO, PA13 Alternate: EVENTOUT
NC	F13	-	-	-
VSS	F12	P	-	Default: VSS
VDD	G13	P	-	Default: VDD
PH13	E12	I/O	5VT	Default: PH13 Alternate: TIMER7_CH0_ON, CAN0_TX, EXMC_D21, TLI_G2, EVENTOUT
PH14	E13	I/O	5VT	Default: PH14 Alternate: TIMER7_CH1_ON, EXMC_D22, DCI_D4, TLI_G3, I2C5_SCL, EVENTOUT
PH15	D13	I/O	5VT	Default: PH15 Alternate: TIMER7_CH2_ON, EXMC_D23, DCI_D11, TLI_G4, I2C5_SDA, EVENTOUT

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Pin Name	**Pins**	**Pin Type[1]**	**I/O Level[2]**	**Functions description**
PI0	E14	I/O	5VT	Default: PI0 Alternate: TIMER4_CH3, SPI1_NSS, I2S1_WS, EXMC_D24, DCI_D13, TLI_G5, SPI1_NSS, EVENTOUT
PI1	D14	I/O	5VT	Default: PI1 Alternate: SPI1_SCK, I2S1_CK, EXMC_D25, DCI_D8, TLI_G6, SPI1_NSS, EVENTOUT
PI2	C14	I/O	5VT	Default: PI2 Alternate: TIMER7_CH3, SPI1_MISO, I2S1_ADD_SD, EXMC_D26, DCI_D9, TLI_G7, EVENTOUT
PI3	C13	I/O	5VT	Default: PI3 Alternate: TIMER7_ETI, SPI1_MOSI, I2S1_SD, EXMC_D27, DCI_D10, TIMER0_CH0, EVENTOUT
VSS	D9	P	-	Default: VSS
VDD	C9	P	-	Default: VDD
PA14	A14	I/O	5VT	Default: JTCK, SWCLK, PA14 Alternate: EVENTOUT
PA15	A13	I/O	5VT	Default: JTDI/PA15 Alternate: TIMER1_CH0, TIMER1_ETI, SPI0_NSS, SPI2_NSS, I2S2_WS, USART0_TX, EVENTOUT
PC10	B14	I/O	5VT	Default: PC10 Alternate: SPI2_SCK, I2S2_CK, USART2_TX, UART3_TX, SDIO_D2, DCI_D8, TLI_R2, EVENTOUT
PC11	B13	I/O	5VT	Default: PC11 Alternate: I2S2_ADD_SD, SPI2_MISO, USART2_RX, UART3_RX, SDIO_D3, DCI_D4, EVENTOUT
PC12	A12	I/O	5VT	Default: PC12 Alternate: I2C1_SDA, SPI2_MOSI, I2S2_SD, USART2_CK, UART4_TX, SDIO_CK, DCI_D9, EVENTOUT
PD0	B12	I/O	5VT	Default: PD0 Alternate: SPI3_MISO, SPI2_MOSI, I2S2_SD, CAN0_RX, EXMC_D2, EVENTOUT
PD1	C12	I/O	5VT	Default: PD1 Alternate: SPI1_NSS, I2S1_WS, CAN0_TX, EXMC_D3, TIMER7_CH3_ON, EVENTOUT
PD2	D12	I/O	5VT	Default: PD2 Alternate: TIMER2_ETI, UART4_RX, SDIO_CMD, DCI_D11, EVENTOUT
PD3	D11	I/O	5VT	Default: PD3 Alternate: SPI1_SCK, I2S1_CK, USART1_CTS, EXMC_CLK, DCI_D5, TLI_G7, EVENTOUT
PD4	D10	I/O	5VT	Default: PD4 Alternate: USART1_RTS, EXMC_NOE, EVENTOUT,

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Pin Name	**Pins**	**Pin Type[1]**	**I/O Level[2]**	**Functions description**
				I2C3_SCL
PD5	C11	I/O	5VT	Default: PD5 Alternate: USART1_TX, EXMC_NWE, EVENTOUT
VSS	D8	P	-	Default: VSS
VDD	C8	P	-	Default: VDD
PD6	B11	I/O	5VT	Default: PD6 Alternate: SPI2_MOSI, I2S2_SD, SAI0_SD_0, USART1_RX, EXMC_NWAIT, DCI_D10, TLI_B2, TIMER0_CH2_ON, EVENTOUT
PD7	A11	I/O	5VT	Default: PD7 Alternate: USART1_CK, EXMC_NE0, EXMC_NCE1, EVENTOUT
PG9	C10	I/O	5VT	Default: PG9 Alternate: USART5_RX, EXMC_NE1, EXMC_NCE2, DCI_VSYNC, EVENTOUT
PG10	B10	I/O	5VT	Default: PG10 Alternate: SPI5_IO2, TLI_G3, EXMC_NCE3_0, EXMC_NE2, DCI_D2, TLI_B2, EVENTOUT
PG11	B9	I/O	5VT	Default: PG11 Alternate: SPI5_IO3, SPI3_SCK, ETH_MII_TX_EN, ETH_RMII_TX_EN, EXMC_NCE3_1, DCI_D3, TLI_B3, EVENTOUT
PG12	B8	I/O	5VT	Default: PG12 Alternate: SPI5_MISO, SPI3_MISO, USART5_RTS, TLI_B4, EXMC_NE3, TLI_B1, EVENTOUT
PG13	A8	I/O	5VT	Default: PG13 Alternate: SPI5_SCK, SPI3_MOSI, USART5_CTS, ETH_MII_TXD0, ETH_RMII_TXD0, EXMC_A24, EVENTOUT
PG14	A7	I/O	5VT	Default: PG14 Alternate: SPI5_MOSI, SPI3_NSS, USART5_TX, ETH_MII_TXD1, ETH_RMII_TXD1, EXMC_A25, I2C4_SCL, EVENTOUT
VSS	D7	P	-	Default: VSS
VDD	C7	P	-	Default: VDD
PG15	B7	I/O	5VT	Default: PG15 Alternate: USART5_CTS, EXMC_SDNCAS, DCI_D13, I2C5_SMBA, EVENTOUT
PB3	A10	I/O	5VT	Default: JTDO, PB3 Alternate: TRACESWO, TIMER1_CH1, SPI0_SCK, SPI2_SCK, I2S2_CK, USART0_RX, I2C1_SDA, EVENTOUT
PB4	A9	I/O	5VT	Default: NJTRST Alternate: TIMER2_CH0, SPI0_MISO, SPI2_MISO,

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GD32F527Ix BGA176[4]				
Pin Name	**Pins**	**Pin Type[1]**	**I/O Level[2]**	**Functions description**
				I2S2_ADD_SD, I2C2_SDA, SDIO_D0, I2C0_TXFRAME, TIMER7_CH0, EVENTOUT
PB5	A6	I/O	5VT	Default: PB5 Alternate: TIMER2_CH1, I2C0_SMBA, SPI0_MOSI, SPI2_MOSI, I2S2_SD, CAN1_RX, USBHS_ULPI_D7, ETH_PPS_OUT, EXMC_SDCKE1, DCI_D10, SPI0_NSS, EVENTOUT
PB6	B6	I/O	5VT	Default: PB6 Alternate: TIMER3_CH0, I2C0_SCL, SPI5_MOSI, USART0_TX, CAN1_TX, EXMC_SDNE1, DCI_D5, EVENTOUT
PB7	B5	I/O	5VT	Default: PB7 Alternate: TIMER3_CH1, I2C0_SDA, USART0_RX, EXMC_NL, EXMC_NADV, DCI_VSYNC, EVENTOUT
BOOT0	D6	I/O	5VT	Default: BOOT0
PB8	A5	I/O	5VT	Default: PB8 Alternate: TIMER1_CH0, TIMER1_ETI, TIMER3_CH2, TIMER9_CH0, I2C0_SCL, SPI5_NSS, SPI4_MOSI, CAN0_RX, ETH_MII_TXD3, SDIO_D4, DCI_D6, TLI_B6, EVENTOUT
PB9	B4	I/O	5VT	Default: PB9 Alternate: TIMER1_CH1, TIMER3_CH3, TIMER10_CH0, I2C0_SDA, SPI1_NSS, I2S1_WS, SAI0_FS_1, CAN0_TX, SDIO_D5, DCI_D7, TLI_B7, EVENTOUT
PE0	A4	I/O	5VT	Default: PE0 Alternate: TIMER3_ETI, SPI0_MOSI, UART7_RX, EXMC_NBL0, DCI_D2, EVENTOUT
PE1	A3	I/O	5VT	Default: PE1 Alternate: TIMER0_CH1_ON, UART7_TX, EXMC_NBL1, DCI_D3, TIMER7_CH3, EVENTOUT
VSS	D5	P	-	Default: VSS
PDR_ON	C6	P	-	Default: PDR_ON[3]
VDD	C5	P	-	Default: VDD
PI4	D4	I/O	5VT	Default: PI4 Alternate: TIMER7_BRKIN, SPI4_MOSI, EXMC_NBL2, DCI_D5, TLI_B4, EVENTOUT
PI5	C4	I/O	5VT	Default: PI5 Alternate: TIMER7_CH0, EXMC_NBL3, DCI_VSYNC, TLI_B5, SPI2_MOSI, I2C5_SCL, EVENTOUT
PI6	C3	I/O	5VT	Default: PI6 Alternate: TIMER7_CH1, EXMC_D28, DCI_D6, TLI_B6,

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Pin Name	**Pins**	**Pin Type[1]**	**I/O Level[2]**	**Functions description**
				EVENTOUT
PI7	C2	I/O	5VT	Default: PI7 Alternate: TIMER7_CH2, EXMC_D29, DCI_D7, TLI_B7, I2C5_SDA, EVENTOUT
VSS	F6	P	-	Default: VSS[4]
VSS	F7	P	-	Default: VSS[4]
VSS	F8	P	-	Default: VSS[4]
VSS	F9	P	-	Default: VSS[4]
VSS	F10	P	-	Default: VSS[4]
VSS	G6	P	-	Default: VSS[4]
VSS	G7	P	-	Default: VSS[4]
VSS	G8	P	-	Default: VSS[4]
VSS	G9	P	-	Default: VSS[4]
VSS	G10	P	-	Default: VSS[4]
VSS	H6	P	-	Default: VSS[4]
VSS	H7	P	-	Default: VSS[4]
VSS	H8	P	-	Default: VSS[4]
VSS	H9	P	-	Default: VSS[4]
VSS	H10	P	-	Default: VSS[4]
VSS	J6	P	-	Default: VSS[4]
VSS	J7	P	-	Default: VSS[4]
VSS	J8	P	-	Default: VSS[4]
VSS	J9	P	-	Default: VSS[4]
VSS	J10	P	-	Default: VSS[4]
VSS	K6	P	-	Default: VSS[4]
VSS	K7	P	-	Default: VSS[4]
VSS	K8	P	-	Default: VSS[4]
VSS	K9	P	-	Default: VSS[4]
VSS	K10	P	-	Default: VSS[4]

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Notes:

(1) Type: I = input, O = output, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

(3) PDR_ON pin should be pulled up to VDD, refer to ***Figure 4-2. Recommended PDR_ON pin circuit***.

(4) The pin count of the BGA176 package is 176+25 (with an additional 25 VSS pins).

2.6.3. GD32F527Zx LQFP144 pin definitions

Table 2-6. GD32F527Zx LQFP144 pin definitions

GD32F527Zx LQFP144				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PE2	1	I/O	5VT	Default: PE2 Alternate: SPI3_SCK, SAI0_MCLK_0, ETH_MII_TXD3, EXMC_A23, EVENTOUT
PE3	2	I/O	5VT	Default: PE3 Alternate: SAI0_SD_1, EXMC_A19, EVENTOUT
PE4	3	I/O	5VT	Default: PE4 Alternate: SPI3_NSS, SAI0_FS_0, EXMC_A20, DCI_D4, TLI_B0, EVENTOUT
PE5	4	I/O	5VT	Default: PE5 Alternate: TIMER8_CH0, SPI3_MISO, SAI0_SCK_0, SPI0_MISO, EXMC_A21, DCI_D6, TLI_G0, EVENTOUT
PE6	5	I/O	5VT	Default: PE6 Alternate: TIMER8_CH1, SPI3_MOSI, SAI0_SD_0, EXMC_A22, DCI_D7, TLI_G1, EVENTOUT
VBAT	6	P	-	Default: VBAT
PC13-TAMPER-RTC	7	I/O	5VT	Default: PC13 Alternate: SPI0_SCK, EVENTOUT Additional: RTC_TAMP0, RTC_OUT, RTC_TS
PC14-OSC32IN	8	I/O	5VT	Default: PC14 Alternate: EVENTOUT Additional: OSC32IN
PC15-OSC32OUT	9	I/O	5VT	Default: PC15 Alternate: EVENTOUT Additional: OSC32OUT
PF0	10	I/O	5VT	Default: PF0 Alternate: I2C1_SDA, EXMC_A0, CTC_SYNC, I2C4_SDA, EVENTOUT
PF1	11	I/O	5VT	Default: PF1 Alternate: I2C1_SCL, EXMC_A1, I2C4_SCL, EVENTOUT
PF2	12	I/O	5VT	Default: PF2 Alternate: I2C1_SMBA, EXMC_A2, I2C4_SMBA, EVENTOUT
PF3	13	I/O	5VT	Default: PF3

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Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Alternate: I2C1_TXFRAME, SPI2_NSS, EXMC_A3, EVENTOUT Additional: ADC2_IN9
PF4	14	I/O	5VT	Default: PF4 Alternate: EXMC_A4, EVENTOUT Additional: ADC2_IN14
PF5	15	I/O	5VT	Default: PF5 Alternate: EXMC_A5, EVENTOUT Additional: ADC2_IN15
VSS	16	P	-	Default: VSS
VDD	17	P	-	Default: VDD
PF6	18	I/O	5VT	Default: PF6 Alternate: TIMER9_CH0, SPI4_NSS, SAI0_SD_1, UART6_RX, EXMC_NIORD, EVENTOUT Additional: ADC2_IN4
PF7	19	I/O	5VT	Default: PF7 Alternate: TIMER10_CH0, SPI4_SCK, SAI0_MCLK_1, UART6_TX, EXMC_NREG, EVENTOUT Additional: ADC2_IN5
PF8	20	I/O	5VT	Default: PF8 Alternate: SPI4_MISO, SAI0_SCK_1, TIMER12_CH0, EXMC_NIOWR, EVENTOUT Additional: ADC2_IN6
PF9	21	I/O	5VT	Default: PF9 Alternate: SPI4_MOSI, SAI0_FS_1, TIMER13_CH0, EXMC_CD, EVENTOUT Additional: ADC2_IN7
PF10	22	I/O	5VT	Default: PF10 Alternate: EXMC_INTR, DCI_D11, TLI_DE, I2C5_SMBA, EVENTOUT Additional: ADC2_IN8
PH0/OSCIN	23	I/O	5VT	Default: PH0, OSCIN Alternate: EVENTOUT Additional: OSCIN
PH1/OSCOUT	24	I/O	5VT	Default: PH1, OSCOUT Alternate: EVENTOUT Additional: OSCOUT
NRST	25	-	-	Default: NRST
PC0	26	I/O	5VT	Default: PC0 Alternate: SAI0_MCLK_1, USBHS_ULPI_STP, EXMC_SDNWE, TIMER7_CH2_ON, EVENTOUT Additional: ADC012_IN10
PC1	27	I/O	5VT	Default: PC1

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Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Alternate: SPI2_MOSI, I2S2_SD, SAI0_SD_0, SPI1_MOSI, I2S1_SD, ETH_MDC, EVENTOUT Additional: ADC012_IN11
PC2	28	I/O	5VT	Default: PC2 Alternate: SPI1_MISO, I2S1_ADD_SD, USBHS_ULPI_DIR, ETH_MII_TXD2, EXMC_SDNE0, EVENTOUT Additional: ADC012_IN12
PC3	29	I/O	5VT	Default: PC3 Alternate: SPI1_MOSI, I2S1_SD, USBHS_ULPI_NXT, ETH_MII_TX_CLK, EXMC_SDCKE0, EVENTOUT Additional: ADC012_IN13
VDD	30	P	-	Default: VDD
VSSA	31	P	-	Default: VSSA
VREFP	32	P	-	Default: VREFP
VDDA	33	P	-	Default: VDDA
PA0-WKUP	34	I/O	5VT	Default: PA0 Alternate: TIMER1_CH0, TIMER1_ETI, TIMER4_CH0, TIMER7_ETI, USART1_CTS, UART3_TX, ETH_MII_CRS, EVENTOUT Additional: ADC012_IN0, WKUP
PA1	35	I/O	5VT	Default: PA1 Alternate: TIMER1_CH1, TIMER4_CH1, SPI3_MOSI, USART1_RTS, UART3_RX, ETH_MII_RX_CLK, ETH_RMII_REF_CLK, EVENTOUT Additional: ADC012_IN1
PA2	36	I/O	5VT	Default: PA2 Alternate: TIMER1_CH2, TIMER4_CH2, TIMER8_CH0, I2S_CKIN, USART1_TX, ETH_MDIO, EVENTOUT Additional: ADC012_IN2
PA3	37	I/O	5VT	Default: PA3 Alternate: TIMER1_CH3, TIMER4_CH3, TIMER8_CH1, I2S1_MCK, SAI0_FS_0, USART1_RX, USBHS_ULPI_D0, ETH_MII_COL, TLI_B5, I2C3_SDA, EVENTOUT Additional: ADC012_IN3
VSS	38	P	-	Default: VSS
VDD	39	P	-	Default: VDD
PA4	40	I/O		Default: PA4 Alternate: SPI0_NSS, SPI2_NSS, I2S2_WS, USART1_CK, USBHS_SOF, DCI_HSYNC, TLI_VSYNC, TIMER7_CH1_ON, EVENTOUT Additional: ADC01_IN4, DAC0_OUT0
PA5	41	I/O		Default: PA5 Alternate: TIMER1_CH0, TIMER1_ETI, TIMER7_CH0_ON,

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Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				SPI0_SCK, USBHS_ULPI_CK, EVENTOUT Additional: ADC01_IN5, DAC0_OUT1
PA6	42	I/O	5VT	Default: PA6 Alternate: TIMER0_BRKIN, TIMER2_CH0, TIMER7_BRKIN, SPI0_MISO, I2S1_MCK, TIMER12_CH0, SDIO_CMD, DCI_PIXCLK, TLI_G2, SPI4_NSS, EVENTOUT Additional: ADC01_IN6
PA7	43	I/O	5VT	Default: PA7 Alternate: TIMER0_CH0_ON, TIMER2_CH1, TIMER7_CH0_ON, SPI0_MOSI, TIMER13_CH0, ETH_MII_RX_DV, ETH_RMII_CRS_DV, EXMC_SDNWE, EVENTOUT Additional: ADC01_IN7
PC4	44	I/O	5VT	Default: PC4 Alternate: ETH_MII_RXD0, ETH_RMII_RXD0, EXMC_SDNE0, EVENTOUT Additional: ADC01_IN14
PC5	45	I/O	5VT	Default: PC5 Alternate: USART2_RX, ETH_MII_RXD1, ETH_RMII_RXD1, EXMC_SDCKE0, EVENTOUT Additional: ADC01_IN15
PB0	46	I/O	5VT	Default: PB0 Alternate: TIMER0_CH1_ON, TIMER2_CH2, TIMER7_CH1_ON, SPI4_SCK, SPI2_MOSI, I2S2_SD, TLI_R3, USBHS_ULPI_D1, ETH_MII_RXD2, SDIO_D1, EVENTOUT Additional: ADC01_IN8, IREF
PB1	47	I/O	5VT	Default: PB1 Alternate: TIMER0_CH2_ON, TIMER2_CH3, TIMER7_CH2_ON, SPI4_NSS, TLI_R6, USBHS_ULPI_D2, ETH_MII_RXD3, SDIO_D2, EVENTOUT, TIMER0_CH2 Additional: ADC01_IN9
PB2	48	I/O	5VT	Default: BOOT1 Alternate: TIMER1_CH3, SAI0_SD_0, SPI2_MOSI, I2S2_SD, USBHS_ULPI_D4, SDIO_CK, EVENTOUT
PF11	49	I/O	5VT	Default: PF11 Alternate: SPI4_MOSI, EXMC_SDNRAS, DCI_D12, I2C5_SCL, EVENTOUT
PF12	50	I/O	5VT	Default: PF12 Alternate: EXMC_A6, I2C5_SDA, EVENTOUT
VSS	51	P	-	Default: VSS
VDD	52	P	-	Default: VDD
PF13	53	I/O	5VT	Default: PF13 Alternate: EXMC_A7, I2C3_SMBA, EVENTOUT
PF14	54	I/O	5VT	Default: PF14 Alternate: EXMC_A8, I2C3_SCL, SPI1_MOSI, EVENTOUT

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Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PF15	55	I/O	5VT	Default: PF15 Alternate: EXMC_A9, I2C3_SDA, TIMER0_CH3, EVENTOUT
PG0	56	I/O	5VT	Default: PG0 Alternate: EXMC_A10, I2C3_SDA, TIMER0_CH3_ON, EVENTOUT
PG1	57	I/O	5VT	Default: PG1 Alternate: EXMC_A11, I2C3_SCL, TIMER7_CH2, EVENTOUT
PE7	58	I/O	5VT	Default: PE7 Alternate: TIMER0_ETI, UART6_RX, EXMC_D4, TIMER0_CH1, EVENTOUT
PE8	59	I/O	5VT	Default: PE8 Alternate: TIMER0_CH0_ON, UART6_TX, EXMC_D5, SPI5_IO2, USART2_TX, EVENTOUT
PE9	60	I/O	5VT	Default: PE9 Alternate: TIMER0_CH0, EXMC_D6, EVENTOUT
VSS	61	P	-	Default: VSS
VDD	62	P	-	Default: VDD
PE10	63	I/O	5VT	Default: PE10 Alternate: TIMER0_CH1_ON, EXMC_D7, EVENTOUT
PE11	64	I/O	5VT	Default: PE11 Alternate: TIMER0_CH1, SPI3_NSS, SPI4_NSS, EXMC_D8, TLI_G3, EVENTOUT
PE12	65	I/O	5VT	Default: PE12 Alternate: TIMER0_CH2_ON, SPI3_SCK, SPI4_SCK, EXMC_D9, TLI_B4, EVENTOUT
PE13	66	I/O	5VT	Default: PE13 Alternate: TIMER0_CH2, SPI3_MISO, SPI4_MISO, EXMC_D10, TLI_DE, EVENTOUT
PE14	67	I/O	5VT	Default: PE14 Alternate: TIMER0_CH3, SPI3_MOSI, SPI4_MOSI, EXMC_D11, TLI_PIXCLK, EVENTOUT
PE15	68	I/O	5VT	Default: PE15 Alternate: TIMER0_BRKIN, EXMC_D12, TLI_R7, EVENTOUT
PB10	69	I/O	5VT	Default: PB10 Alternate: TIMER1_CH2, I2C1_SCL, SPI1_SCK, I2S1_CK, I2S2_MCK, USART2_TX, USBHS_ULPI_D3, ETH_MII_RX_ER, SDIO_D7, TLI_G4, EVENTOUT
PB11	70	I/O	5VT	Default: PB11 Alternate: TIMER1_CH3, I2C1_SDA, I2S_CKIN, USART2_RX, USBHS_ULPI_D4, ETH_MII_TX_EN, ETH_RMII_TX_EN, TLI_G5, EVENTOUT
NC	71	-	-	-

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Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
VDD	72	P	-	Default: VDD
PB12	73	I/O	5VT	Default: PB12 Alternate: TIMER0_BRKIN, I2C1_SMBA, SPI1_NSS, I2S1_WS, SPI3_NSS, USART2_CK, CAN1_RX, USBHS_ULPI_D5, ETH_MII_TXD0, ETH_RMII_TXD0, USBHS_ID, SPI5_MISO, EVENTOUT
PB13	74	I/O	5VT	Default: PB13 Alternate: TIMER0_CH0_ON, SPI1_SCK, I2S1_CK, SPI3_SCK, USART2_CTS, CAN1_TX, USBHS_ULPI_D6, ETH_MII_TXD1, ETH_RMII_TXD1, I2C1_TXFRAME, EVENTOUT Additional: USBHS_VBUS
PB14	75	I/O	5VT	Default: PB14 Alternate: TIMER0_CH1_ON, TIMER7_CH1_ON, SPI1_MISO, I2S1_ADD_SD, USART2_RTS, TIMER11_CH0, USBHS_DM, EVENTOUT
PB15	76	I/O	5VT	Default: PB15 Alternate: RTC_REFIN, TIMER0_CH2_ON, TIMER7_CH2_ON, SPI1_MOSI, I2S1_SD, TIMER11_CH1, USBHS_DP, EVENTOUT
PD8	77	I/O	5VT	Default: PD8 Alternate: USART2_TX, EXMC_D13, EVENTOUT
PD9	78	I/O	5VT	Default: PD9 Alternate: USART2_RX, EXMC_D14, SPI2_NSS, EVENTOUT
PD10	79	I/O	5VT	Default: PD10 Alternate: USART2_CK, EXMC_D15, TLI_B3, SPI5_SCK, EVENTOUT
PD11	80	I/O	5VT	Default: PD11 Alternate: USART2_CTS, EXMC_A16, EXMC_CLE, EVENTOUT
PD12	81	I/O	5VT	Default: PD12 Alternate: TIMER3_CH0, USART2_RTS, EXMC_A17, EXMC_ALE, TIMER0_CH1, EVENTOUT
PD13	82	I/O	5VT	Default: PD13 Alternate: TIMER3_CH1, EXMC_A18, EVENTOUT
VSS	83	P	-	Default: VSS
VDD	84	P	-	Default: VDD
PD14	85	I/O	5VT	Default: PD14 Alternate: TIMER3_CH2, EXMC_D0, TIMER7_CH1, EVENTOUT
PD15	86	I/O	5VT	Default: PD15 Alternate: TIMER3_CH3, EXMC_D1, CTC_SYNC, USART2_RX, EVENTOUT
PG2	87	I/O	5VT	Default: PG2 Alternate: EXMC_A12, EVENTOUT
PG3	88	I/O	5VT	Default: PG3

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Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Alternate: EXMC_A13, EVENTOUT
PG4	89	I/O	5VT	Default: PG4 Alternate: EXMC_A14, SPI5_NSS, EVENTOUT
PG5	90	I/O	5VT	Default: PG5 Alternate: EXMC_A15, EVENTOUT
PG6	91	I/O	5VT	Default: PG6 Alternate: EXMC_INT1, DCI_D12, TLI_R7, I2C4_SMBA, EVENTOUT
PG7	92	I/O	5VT	Default: PG7 Alternate: USART5_CK, EXMC_INT2, DCI_D13, TLI_PIXCLK, I2C4_SCL, EVENTOUT
PG8	93	I/O	5VT	Default: PG8 Alternate: SPI5_NSS, USART5_RTS, ETH_PPS_OUT, EXMC_SDCLK, I2C4_SDA, EVENTOUT
VSS	94	P	-	Default: VSS
VDD	95	P	-	Default: VDD
PC6	96	I/O	5VT	Default: PC6 Alternate: TIMER2_CH0, TIMER7_CH0, I2S1_MCK, USART5_TX, SDIO_D6, DCI_D0, TLI_HSYNC, TIMER7_CH0_ON, EVENTOUT
PC7	97	I/O	5VT	Default: PC7 Alternate: TIMER2_CH1, TIMER7_CH1, SPI1_SCK, I2S1_CK, I2S2_MCK, USART5_RX, SDIO_D7, DCI_D1, TLI_G6, EVENTOUT
PC8	98	I/O	5VT	Default: PC8 Alternate: TIMER2_CH2, TIMER7_CH2, USART5_CK, SDIO_D0, DCI_D2, EVENTOUT
PC9	99	I/O	5VT	Default: PC9 Alternate: CK_OUT1, TIMER2_CH3, TIMER7_CH3, I2C2_SDA, I2S_CKIN, SDIO_D1, DCI_D3, TIMER0_CH1_ON, EVENTOUT
PA8	100	I/O	5VT	Default: PA8 Alternate: CK_OUT0, TIMER0_CH0, I2C2_SCL, USART0_CK, USBFS_SOF, SDIO_D1, TLI_R6, CTC_SYNC, EVENTOUT
PA9	101	I/O	5VT	Default: PA9 Alternate: TIMER0_CH1, I2C2_SMBA, SPI1_SCK, I2S1_CK, SAI0_SD_1, USART0_TX, SDIO_D2, DCI_D0, EVENTOUT Additional: USBFS_VBUS
PA10	102	I/O	5VT	Default: PA10 Alternate: TIMER0_CH2, SPI4_MOSI, USART0_RX, USBFS_ID, DCI_D1, I2C2_TXFRAME, EVENTOUT
PA11	103	I/O	5VT	Default: PA11 Alternate: TIMER0_CH3, SPI3_MISO, USART0_CTS,

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Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				USART5_TX, CAN0_RX, USBFS_DM, TLI_R4, EVENTOUT
PA12	104	I/O	5VT	Default: PA12 Alternate: TIMER0_ETI, SPI4_MISO, USART0_RTS, USART5_RX, CAN0_TX, USBFS_DP, TLI_R5, EVENTOUT
PA13	105	I/O	5VT	Default: JTMS, SWDIO, PA13 Alternate: EVENTOUT
NC	106	-	-	-
VSS	107	P	-	Default: VSS
VDD	108	P	-	Default: VDD
PA14	109	I/O	5VT	Default: JTCK, SWCLK, PA14 Alternate: EVENTOUT
PA15	110	I/O	5VT	Default: JTDI/PA15 Alternate: TIMER1_CH0, TIMER1_ETI, SPI0_NSS, SPI2_NSS, I2S2_WS, USART0_TX, EVENTOUT
PC10	111	I/O	5VT	Default: PC10 Alternate: SPI2_SCK, I2S2_CK, USART2_TX, UART3_TX, SDIO_D2, DCI_D8, TLI_R2, EVENTOUT
PC11	112	I/O	5VT	Default: PC11 Alternate: I2S2_ADD_SD, SPI2_MISO, USART2_RX, UART3_RX, SDIO_D3, DCI_D4, EVENTOUT
PC12	113	I/O	5VT	Default: PC12 Alternate: I2C1_SDA, SPI2_MOSI, I2S2_SD, USART2_CK, UART4_TX, SDIO_CK, DCI_D9, EVENTOUT
PD0	114	I/O	5VT	Default: PD0 Alternate: SPI3_MISO, SPI2_MOSI, I2S2_SD, CAN0_RX, EXMC_D2, EVENTOUT
PD1	115	I/O	5VT	Default: PD1 Alternate: SPI1_NSS, I2S1_WS, CAN0_TX, EXMC_D3, TIMER7_CH3_ON, EVENTOUT
PD2	116	I/O	5VT	Default: PD2 Alternate: TIMER2_ETI, UART4_RX, SDIO_CMD, DCI_D11, EVENTOUT
PD3	117	I/O	5VT	Default: PD3 Alternate: SPI1_SCK, I2S1_CK, USART1_CTS, EXMC_CLK, DCI_D5, TLI_G7, EVENTOUT
PD4	118	I/O	5VT	Default: PD4 Alternate: USART1_RTS, EXMC_NOE, EVENTOUT, I2C3_SCL
PD5	119	I/O	5VT	Default: PD5 Alternate: USART1_TX, EXMC_NWE, EVENTOUT
VSS	120	P	-	Default: VSS
VDD	121	P	-	Default: VDD
PD6	122	I/O	5VT	Default: PD6

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Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Alternate: SPI2_MOSI, I2S2_SD, SAI0_SD_0, USART1_RX, EXMC_NWAIT, DCI_D10, TLI_B2, TIMER0_CH2_ON, EVENTOUT
PD7	123	I/O	5VT	Default: PD7 Alternate: USART1_CK, EXMC_NE0, EXMC_NCE1, EVENTOUT
PG9	124	I/O	5VT	Default: PG9 Alternate: USART5_RX, EXMC_NE1, EXMC_NCE2, DCI_VSYNC, EVENTOUT
PG10	125	I/O	5VT	Default: PG10 Alternate: SPI5_IO2, TLI_G3, EXMC_NCE3_0, EXMC_NE2, DCI_D2, TLI_B2, EVENTOUT
PG11	126	I/O	5VT	Default: PG11 Alternate: SPI5_IO3, SPI3_SCK, ETH_MII_TX_EN, ETH_RMII_TX_EN, EXMC_NCE3_1, DCI_D3, TLI_B3, EVENTOUT
PG12	127	I/O	5VT	Default: PG12 Alternate: SPI5_MISO, SPI3_MISO, USART5_RTS, TLI_B4, EXMC_NE3, TLI_B1, EVENTOUT
PG13	128	I/O	5VT	Default: PG13 Alternate: SPI5_SCK, SPI3_MOSI, USART5_CTS, ETH_MII_TXD0, ETH_RMII_TXD0, EXMC_A24, EVENTOUT
PG14	129	I/O	5VT	Default: PG14 Alternate: SPI5_MOSI, SPI3_NSS, USART5_TX, ETH_MII_TXD1, ETH_RMII_TXD1, EXMC_A25, I2C4_SCL, EVENTOUT
VSS	130	P	-	Default: VSS
VDD	131	P	-	Default: VDD
PG15	132	I/O	5VT	Default: PG15 Alternate: USART5_CTS, EXMC_SDNCAS, DCI_D13, I2C5_SMBA, EVENTOUT
PB3	133	I/O	5VT	Default: JTDO, PB3 Alternate: TRACESWO, TIMER1_CH1, SPI0_SCK, SPI2_SCK, I2S2_CK, USART0_RX, I2C1_SDA, EVENTOUT
PB4	134	I/O	5VT	Default: NJTRST Alternate: TIMER2_CH0, SPI0_MISO, SPI2_MISO, I2S2_ADD_SD, I2C2_SDA, SDIO_D0, I2C0_TXFRAME, TIMER7_CH0, EVENTOUT
PB5	135	I/O	5VT	Default: PB5 Alternate: TIMER2_CH1, I2C0_SMBA, SPI0_MOSI, SPI2_MOSI, I2S2_SD, CAN1_RX, USBHS_ULPI_D7, ETH_PPS_OUT, EXMC_SDCKE1, DCI_D10, SPI0_NSS, EVENTOUT

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Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PB6	136	I/O	5VT	Default: PB6 Alternate: TIMER3_CH0, I2C0_SCL, SPI5_MOSI, USART0_TX, CAN1_TX, EXMC_SDNE1, DCI_D5, EVENTOUT
PB7	137	I/O	5VT	Default: PB7 Alternate: TIMER3_CH1, I2C0_SDA, USART0_RX, EXMC_NL, EXMC_NADV, DCI_VSYNC, EVENTOUT
BOOT0	138	I/O	5VT	Default: BOOT0
PB8	139	I/O	5VT	Default: PB8 Alternate: TIMER1_CH0, TIMER1_ETI, TIMER3_CH2, TIMER9_CH0, I2C0_SCL, SPI5_NSS, SPI4_MOSI, CAN0_RX, ETH_MII_TXD3, SDIO_D4, DCI_D6, TLI_B6, EVENTOUT
PB9	140	I/O	5VT	Default: PB9 Alternate: TIMER1_CH1, TIMER3_CH3, TIMER10_CH0, I2C0_SDA, SPI1_NSS, I2S1_WS, SAI0_FS_1, CAN0_TX, SDIO_D5, DCI_D7, TLI_B7, EVENTOUT
PE0	141	I/O	5VT	Default: PE0 Alternate: TIMER3_ETI, SPI0_MOSI, UART7_RX, EXMC_NBL0, DCI_D2, EVENTOUT
PE1	142	I/O	5VT	Default: PE1 Alternate: TIMER0_CH1_ON, UART7_TX, EXMC_NBL1, DCI_D3, TIMER7_CH3, EVENTOUT
PDR_ON	143	P	-	Default: PDR_ON(3)
VDD	144	P	-	Default: VDD

Notes:

(1) Type: I = input, O = output, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

(3) PDR_ON pin should be pulled up to VDD, refer to ***Figure 4-2. Recommended PDR_ON pin circuit***.

2.6.4. GD32F527Vx LQFP100 pin definitions

Table 2-7. GD32F527Vx LQFP100 pin definitions

GD32F527Vx LQFP100				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PE2	1	I/O	5VT	Default: PE2 Alternate: SPI3_SCK, SAI0_MCLK_0, ETH_MII_TXD3, EXMC_A23, EVENTOUT
PE3	2	I/O	5VT	Default: PE3 Alternate: SAI0_SD_1, EXMC_A19, EVENTOUT
PE4	3	I/O	5VT	Default: PE4

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GD32F527Vx LQFP100				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Alternate: SPI3_NSS, SAI0_FS_0, EXMC_A20, DCI_D4, TLI_B0, EVENTOUT
PE5	4	I/O	5VT	Default: PE5 Alternate: TIMER8_CH0, SPI3_MISO, SAI0_SCK_0, SPI0_MISO, EXMC_A21, DCI_D6, TLI_G0, EVENTOUT
PE6	5	I/O	5VT	Default: PE6 Alternate: TIMER8_CH1, SPI3_MOSI, SAI0_SD_0, EXMC_A22, DCI_D7, TLI_G1, EVENTOUT
VBAT	6	P	-	Default: VBAT
PC13-TAMPER-RTC	7	I/O	5VT	Default: PC13 Alternate: SPI0_SCK, EVENTOUT Additional: RTC_TAMP0, RTC_OUT, RTC_TS
PC14-OSC32IN	8	I/O	5VT	Default: PC14 Alternate: EVENTOUT Additional: OSC32IN
PC15-OSC32OUT	9	I/O	5VT	Default: PC15 Alternate: EVENTOUT Additional: OSC32OUT
VSS	10	P	-	Default: VSS
VDD	11	P	-	Default: VDD
PH0/OSCIN	12	I/O	5VT	Default: PH0, OSCIN Alternate: EVENTOUT Additional: OSCIN
PH1/OSCOUT	13	I/O	5VT	Default: PH1, OSCOUT Alternate: EVENTOUT Additional: OSCOUT
NRST	14	-	-	Default: NRST
PC0	15	I/O	5VT	Default: PC0 Alternate: SAI0_MCLK_1, USBHS_ULPI_STP, TIMER7_CH2_ON, EVENTOUT Additional: ADC012_IN10
PC1	16	I/O	5VT	Default: PC1 Alternate: SPI2_MOSI, I2S2_SD, SAI0_SD_0, SPI1_MOSI, I2S1_SD, ETH_MDC, EVENTOUT Additional: ADC012_IN11
PC2	17	I/O	5VT	Default: PC2 Alternate: SPI1_MISO, I2S1_ADD_SD, USBHS_ULPI_DIR, ETH_MII_TXD2, EVENTOUT Additional: ADC012_IN12
PC3	18	I/O	5VT	Default: PC3 Alternate: SPI1_MOSI, I2S1_SD, USBHS_ULPI_NXT, ETH_MII_TX_CLK, EVENTOUT

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Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Additional: ADC012_IN13
VDD	19	P	-	Default: VDD
VSSA	20	P	-	Default: VSSA
VREFP	21	P	-	Default: VREFP
VDDA	22	P	-	Default: VDDA
PA0-WKUP	23	I/O	5VT	Default: PA0 Alternate: TIMER1_CH0, TIMER1_ETI, TIMER4_CH0, TIMER7_ETI, USART1_CTS, UART3_TX, ETH_MII_CRS, EVENTOUT Additional: ADC012_IN0, WKUP
PA1	24	I/O	5VT	Default: PA1 Alternate: TIMER1_CH1, TIMER4_CH1, SPI3_MOSI, USART1_RTS, UART3_RX, ETH_MII_RX_CLK, ETH_RMII_REF_CLK, EVENTOUT Additional: ADC012_IN1
PA2	25	I/O	5VT	Default: PA2 Alternate: TIMER1_CH2, TIMER4_CH2, TIMER8_CH0, I2S_CKIN, USART1_TX, ETH_MDIO, EVENTOUT Additional: ADC012_IN2
PA3	26	I/O	5VT	Default: PA3 Alternate: TIMER1_CH3, TIMER4_CH3, TIMER8_CH1, I2S1_MCK, SAI0_FS_0, USART1_RX, USBHS_ULPI_D0, ETH_MII_COL, TLI_B5, EVENTOUT Additional: ADC012_IN3
VSS	27	P	-	Default: VSS
VDD	28	P	-	Default: VDD
PA4	29	I/O		Default: PA4 Alternate: SPI0_NSS, SPI2_NSS, I2S2_WS, USART1_CK, USBHS_SOF, DCI_HSYNC, TLI_VSYNC, TIMER7_CH1_ON, EVENTOUT Additional: ADC01_IN4, DAC0_OUT0
PA5	30	I/O		Default: PA5 Alternate: TIMER1_CH0, TIMER1_ETI, TIMER7_CH0_ON, SPI0_SCK, USBHS_ULPI_CK, EVENTOUT Additional: ADC01_IN5, DAC0_OUT1
PA6	31	I/O	5VT	Default: PA6 Alternate: TIMER0_BRKIN, TIMER2_CH0, TIMER7_BRKIN, SPI0_MISO, I2S1_MCK, TIMER12_CH0, SDIO_CMD, DCI_PIXCLK, TLI_G2, SPI4_NSS, EVENTOUT Additional: ADC01_IN6
PA7	32	I/O	5VT	Default: PA7 Alternate: TIMER0_CH0_ON, TIMER2_CH1, TIMER7_CH0_ON, SPI0_MOSI, TIMER13_CH0,

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Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				ETH_MII_RX_DV, ETH_RMII_CRS_DV, EVENTOUT Additional: ADC01_IN7
PC4	33	I/O	5VT	Default: PC4 Alternate: ETH_MII_RXD0, ETH_RMII_RXD0, EVENTOUT Additional: ADC01_IN14
PC5	34	I/O	5VT	Default: PC5 Alternate: USART2_RX, ETH_MII_RXD1, ETH_RMII_RXD1, EVENTOUT Additional: ADC01_IN15
PB0	35	I/O	5VT	Default: PB0 Alternate: TIMER0_CH1_ON, TIMER2_CH2, TIMER7_CH1_ON, SPI4_SCK, SPI2_MOSI, I2S2_SD, TLI_R3, USBHS_ULPI_D1, ETH_MII_RXD2, SDIO_D1, EVENTOUT Additional: ADC01_IN8, IREF
PB1	36	I/O	5VT	Default: PB1 Alternate: TIMER0_CH2_ON, TIMER2_CH3, TIMER7_CH2_ON, SPI4_NSS, TLI_R6, USBHS_ULPI_D2, ETH_MII_RXD3, SDIO_D2, EVENTOUT, TIMER0_CH2 Additional: ADC01_IN9
PB2	37	I/O	5VT	Default: BOOT1 Alternate: TIMER1_CH3, SAI0_SD_0, SPI2_MOSI, I2S2_SD, USBHS_ULPI_D4, SDIO_CK, EVENTOUT
PE7	38	I/O	5VT	Default: PE7 Alternate: TIMER0_ETI, UART6_RX, EXMC_D4, TIMER0_CH1, EVENTOUT
PE8	39	I/O	5VT	Default: PE8 Alternate: TIMER0_CH0_ON, UART6_TX, EXMC_D5, USART2_TX, EVENTOUT
PE9	40	I/O	5VT	Default: PE9 Alternate: TIMER0_CH0, EXMC_D6, EVENTOUT
PE10	41	I/O	5VT	Default: PE10 Alternate: TIMER0_CH1_ON, EXMC_D7, EVENTOUT
PE11	42	I/O	5VT	Default: PE11 Alternate: TIMER0_CH1, SPI3_NSS, SPI4_NSS, EXMC_D8, TLI_G3, EVENTOUT
PE12	43	I/O	5VT	Default: PE12 Alternate: TIMER0_CH2_ON, SPI3_SCK, SPI4_SCK, EXMC_D9, TLI_B4, EVENTOUT
PE13	44	I/O	5VT	Default: PE13 Alternate: TIMER0_CH2, SPI3_MISO, SPI4_MISO, EXMC_D10, TLI_DE, EVENTOUT
PE14	45	I/O	5VT	Default: PE14

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Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Alternate: TIMER0_CH3, SPI3_MOSI, SPI4_MOSI, EXMC_D11, TLI_PIXCLK, EVENTOUT
PE15	46	I/O	5VT	Default: PE15 Alternate: TIMER0_BRKIN, EXMC_D12, TLI_R7, EVENTOUT
PB10	47	I/O	5VT	Default: PB10 Alternate: TIMER1_CH2, I2C1_SCL, SPI1_SCK, I2S1_CK, I2S2_MCK, USART2_TX, USBHS_ULPI_D3, ETH_MII_RX_ER, SDIO_D7, TLI_G4, EVENTOUT
PB11	48	I/O	5VT	Default: PB11 Alternate: TIMER1_CH3, I2C1_SDA, I2S_CKIN, USART2_RX, USBHS_ULPI_D4, ETH_MII_TX_EN, ETH_RMII_TX_EN, TLI_G5, EVENTOUT
NC	49	-	-	-
VDD	50	P	-	Default: VDD
PB12	51	I/O	5VT	Default: PB12 Alternate: TIMER0_BRKIN, I2C1_SMBA, SPI1_NSS, I2S1_WS, SPI3_NSS, USART2_CK, CAN1_RX, USBHS_ULPI_D5, ETH_MII_TXD0, ETH_RMII_TXD0, USBHS_ID, EVENTOUT
PB13	52	I/O	5VT	Default: PB13 Alternate: TIMER0_CH0_ON, SPI1_SCK, I2S1_CK, SPI3_SCK, USART2_CTS, CAN1_TX, USBHS_ULPI_D6, ETH_MII_TXD1, ETH_RMII_TXD1, I2C1_TXFRAME, EVENTOUT Additional: USBHS_VBUS
PB14	53	I/O	5VT	Default: PB14 Alternate: TIMER0_CH1_ON, TIMER7_CH1_ON, SPI1_MISO, I2S1_ADD_SD, USART2_RTS, TIMER11_CH0, USBHS_DM, EVENTOUT
PB15	54	I/O	5VT	Default: PB15 Alternate: RTC_REFIN, TIMER0_CH2_ON, TIMER7_CH2_ON, SPI1_MOSI, I2S1_SD, TIMER11_CH1, USBHS_DP, EVENTOUT
PD8	55	I/O	5VT	Default: PD8 Alternate: USART2_TX, EXMC_D13, EVENTOUT
PD9	56	I/O	5VT	Default: PD9 Alternate: USART2_RX, EXMC_D14, SPI2_NSS, EVENTOUT
PD10	57	I/O	5VT	Default: PD10 Alternate: USART2_CK, EXMC_D15, TLI_B3, EVENTOUT
PD11	58	I/O	5VT	Default: PD11

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GD32F527Vx LQFP100				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Alternate: USART2_CTS, EXMC_A16, EXMC_CLE, EVENTOUT
PD12	59	I/O	5VT	Default: PD12 Alternate: TIMER3_CH0, USART2_RTS, EXMC_A17, EXMC_ALE, TIMER0_CH1, EVENTOUT
PD13	60	I/O	5VT	Default: PD13 Alternate: TIMER3_CH1, EXMC_A18, EVENTOUT
PD14	61	I/O	5VT	Default: PD14 Alternate: TIMER3_CH2, EXMC_D0, TIMER7_CH1, EVENTOUT
PD15	62	I/O	5VT	Default: PD15 Alternate: TIMER3_CH3, EXMC_D1, CTC_SYNC, USART2_RX, EVENTOUT
PC6	63	I/O	5VT	Default: PC6 Alternate: TIMER2_CH0, TIMER7_CH0, I2S1_MCK, USART5_TX, SDIO_D6, DCI_D0, TLI_HSYNC, TIMER7_CH0_ON, EVENTOUT
PC7	64	I/O	5VT	Default: PC7 Alternate: TIMER2_CH1, TIMER7_CH1, SPI1_SCK, I2S1_CK, I2S2_MCK, USART5_RX, SDIO_D7, DCI_D1, TLI_G6, EVENTOUT
PC8	65	I/O	5VT	Default: PC8 Alternate: TIMER2_CH2, TIMER7_CH2, USART5_CK, SDIO_D0, DCI_D2, EVENTOUT
PC9	66	I/O	5VT	Default: PC9 Alternate: CK_OUT1, TIMER2_CH3, TIMER7_CH3, I2C2_SDA, I2S_CKIN, SDIO_D1, DCI_D3, TIMER0_CH1_ON, EVENTOUT
PA8	67	I/O	5VT	Default: PA8 Alternate: CK_OUT0, TIMER0_CH0, I2C2_SCL, USART0_CK, USBFS_SOF, SDIO_D1, TLI_R6, CTC_SYNC, EVENTOUT
PA9	68	I/O	5VT	Default: PA9 Alternate: TIMER0_CH1, I2C2_SMBA, SPI1_SCK, I2S1_CK, SAI0_SD_1, USART0_TX, SDIO_D2, DCI_D0, EVENTOUT Additional: USBFS_VBUS
PA10	69	I/O	5VT	Default: PA10 Alternate: TIMER0_CH2, SPI4_MOSI, USART0_RX, USBFS_ID, DCI_D1, I2C2_TXFRAME, EVENTOUT
PA11	70	I/O	5VT	Default: PA11 Alternate: TIMER0_CH3, SPI3_MISO, USART0_CTS,

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GD32F527Vx LQFP100				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				USART5_TX, CAN0_RX, USBFS_DM, TLI_R4, EVENTOUT
PA12	71	I/O	5VT	Default: PA12 Alternate: TIMER0_ETI, SPI4_MISO, USART0_RTS, USART5_RX, CAN0_TX, USBFS_DP, TLI_R5, EVENTOUT
PA13	72	I/O	5VT	Default: JTMS, SWDIO, PA13 Alternate: EVENTOUT
NC	73	-	-	-
VSS	74	P	-	Default: VSS
VDD	75	P	-	Default: VDD
PA14	76	I/O	5VT	Default: JTCK, SWCLK, PA14 Alternate: EVENTOUT
PA15	77	I/O	5VT	Default: JTDI/PA15 Alternate: TIMER1_CH0, TIMER1_ETI, SPI0_NSS, SPI2_NSS, I2S2_WS, USART0_TX, EVENTOUT
PC10	78	I/O	5VT	Default: PC10 Alternate: SPI2_SCK, I2S2_CK, USART2_TX, UART3_TX, SDIO_D2, DCI_D8, TLI_R2, EVENTOUT
PC11	79	I/O	5VT	Default: PC11 Alternate: I2S2_ADD_SD, SPI2_MISO, USART2_RX, UART3_RX, SDIO_D3, DCI_D4, EVENTOUT
PC12	80	I/O	5VT	Default: PC12 Alternate: I2C1_SDA, SPI2_MOSI, I2S2_SD, USART2_CK, UART4_TX, SDIO_CK, DCI_D9, EVENTOUT
PD0	81	I/O	5VT	Default: PD0 Alternate: SPI3_MISO, SPI2_MOSI, I2S2_SD, CAN0_RX, EXMC_D2, EVENTOUT
PD1	82	I/O	5VT	Default: PD1 Alternate: SPI1_NSS, I2S1_WS, CAN0_TX, EXMC_D3, TIMER7_CH3_ON, EVENTOUT
PD2	83	I/O	5VT	Default: PD2 Alternate: TIMER2_ETI, UART4_RX, SDIO_CMD, DCI_D11, EVENTOUT
PD3	84	I/O	5VT	Default: PD3 Alternate: SPI1_SCK, I2S1_CK, USART1_CTS, EXMC_CLK, DCI_D5, TLI_G7, EVENTOUT
PD4	85	I/O	5VT	Default: PD4 Alternate: USART1_RTS, EXMC_NOE, EVENTOUT
PD5	86	I/O	5VT	Default: PD5 Alternate: USART1_TX, EXMC_NWE, EVENTOUT
PD6	87	I/O	5VT	Default: PD6 Alternate: SPI2_MOSI, I2S2_SD, SAI0_SD_0,

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Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				USART1_RX, EXMC_NWAIT, DCI_D10, TLI_B2, TIMER0_CH2_ON, EVENTOUT
PD7	88	I/O	5VT	Default: PD7 Alternate: USART1_CK, EXMC_NE0, EXMC_NCE1, EVENTOUT
PB3	89	I/O	5VT	Default: JTDO, PB3 Alternate: TRACESWO, TIMER1_CH1, SPI0_SCK, SPI2_SCK, I2S2_CK, USART0_RX, I2C1_SDA, EVENTOUT
PB4	90	I/O	5VT	Default: NJTRST Alternate: TIMER2_CH0, SPI0_MISO, SPI2_MISO, I2S2_ADD_SD, I2C2_SDA, SDIO_D0, I2C0_TXFRAME, TIMER7_CH0, EVENTOUT
PB5	91	I/O	5VT	Default: PB5 Alternate: TIMER2_CH1, I2C0_SMBA, SPI0_MOSI, SPI2_MOSI, I2S2_SD, CAN1_RX, USBHS_ULPI_D7, ETH_PPS_OUT, DCI_D10, SPI0_NSS, EVENTOUT
PB6	92	I/O	5VT	Default: PB6 Alternate: TIMER3_CH0, I2C0_SCL, USART0_TX, CAN1_TX, DCI_D5, EVENTOUT
PB7	93	I/O	5VT	Default: PB7 Alternate: TIMER3_CH1, I2C0_SDA, USART0_RX, EXMC_NL, EXMC_NADV, DCI_VSYNC, EVENTOUT
BOOT0	94	I/O	5VT	Default: BOOT0
PB8	95	I/O	5VT	Default: PB8 Alternate: TIMER1_CH0, TIMER1_ETI, TIMER3_CH2, TIMER9_CH0, I2C0_SCL, SPI4_MOSI, CAN0_RX, ETH_MII_TXD3, SDIO_D4, DCI_D6, TLI_B6, EVENTOUT
PB9	96	I/O	5VT	Default: PB9 Alternate: TIMER1_CH1, TIMER3_CH3, TIMER10_CH0, I2C0_SDA, SPI1_NSS, I2S1_WS, SAI0_FS_1, CAN0_TX, SDIO_D5, DCI_D7, TLI_B7, EVENTOUT
PE0	97	I/O	5VT	Default: PE0 Alternate: TIMER3_ETI, SPI0_MOSI, UART7_RX, EXMC_NBL0, DCI_D2, EVENTOUT
PE1	98	I/O	5VT	Default: PE1 Alternate: TIMER0_CH1_ON, UART7_TX, EXMC_NBL1, DCI_D3, TIMER7_CH3, EVENTOUT
VSS	99	P	-	Default: VSS
VDD	100	P	-	Default: VDD

Notes:

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(1) Type: I = input, O = output, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

2.6.5. GD32F527Rx LQFP64 pin definitions

Table 2-8. GD32F527Rx LQFP64 pin definitions

GD32F527Rx LQFP64				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
VBAT	1	P	-	Default: VBAT
PC13-TAMPER-RTC	2	I/O	5VT	Default: PC13 Alternate: SPI0_SCK, EVENTOUT Additional: RTC_TAMP0, RTC_OUT, RTC_TS
PC14-OSC32IN	3	I/O	5VT	Default: PC14 Alternate: EVENTOUT Additional: OSC32IN
PC15-OSC32OUT	4	I/O	5VT	Default: PC15 Alternate: EVENTOUT Additional: OSC32OUT
PH0/OSCIN	5	I/O	5VT	Default: PH0, OSCIN Alternate: EVENTOUT Additional: OSCIN
PH1/OSCOUT	6	I/O	5VT	Default: PH1, OSCOUT Alternate: EVENTOUT Additional: OSCOUT
NRST	7	-	-	Default: NRST
PC0	8	I/O	5VT	Default: PC0 Alternate: USBHS_ULPI_STP, TIMER7_CH2_ON, EVENTOUT Additional: ADC012_IN10
PC1	9	I/O	5VT	Default: PC1 Alternate: SPI2_MOSI, I2S2_SD, SPI1_MOSI, I2S1_SD, ETH_MDC, EVENTOUT Additional: ADC012_IN11
PC2	10	I/O	5VT	Default: PC2 Alternate: SPI1_MISO, I2S1_ADD_SD, USBHS_ULPI_DIR, ETH_MII_TXD2, EVENTOUT Additional: ADC012_IN12
PC3	11	I/O	5VT	Default: PC3 Alternate: SPI1_MOSI, I2S1_SD, USBHS_ULPI_NXT, ETH_MII_TX_CLK, EVENTOUT Additional: ADC012_IN13
VSSA	12	P	-	Default: VSSA
VDDA	13	P	-	Default: VDDA
PA0-	14	I/O	5VT	Default: PA0

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Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
WKUP				Alternate: TIMER1_CH0, TIMER1_ETI, TIMER4_CH0, TIMER7_ETI, USART1_CTS, UART3_TX, ETH_MII_CRS, EVENTOUT Additional: ADC012_IN0, WKUP
PA1	15	I/O	5VT	Default: PA1 Alternate: TIMER1_CH1, TIMER4_CH1, USART1_RTS, UART3_RX, ETH_MII_RX_CLK, ETH_RMII_REF_CLK, EVENTOUT Additional: ADC012_IN1
PA2	16	I/O	5VT	Default: PA2 Alternate: TIMER1_CH2, TIMER4_CH2, TIMER8_CH0, I2S_CKIN, USART1_TX, ETH_MDIO, EVENTOUT Additional: ADC012_IN2
PA3	17	I/O	5VT	Default: PA3 Alternate: TIMER1_CH3, TIMER4_CH3, TIMER8_CH1, I2S1_MCK, USART1_RX, USBHS_ULPI_D0, ETH_MII_COL, EVENTOUT Additional: ADC012_IN3
VSS	18	P	-	Default: VSS
VDD	19	P	-	Default: VDD
PA4	20	I/O		Default: PA4 Alternate: SPI0_NSS, SPI2_NSS, I2S2_WS, USART1_CK, USBHS_SOF, DCI_HSYNC, TIMER7_CH1_ON, EVENTOUT Additional: ADC01_IN4, DAC0_OUT0
PA5	21	I/O		Default: PA5 Alternate: TIMER1_CH0, TIMER1_ETI, TIMER7_CH0_ON, SPI0_SCK, USBHS_ULPI_CK, EVENTOUT Additional: ADC01_IN5, DAC0_OUT1
PA6	22	I/O	5VT	Default: PA6 Alternate: TIMER0_BRKIN, TIMER2_CH0, TIMER7_BRKIN, SPI0_MISO, I2S1_MCK, TIMER12_CH0, SDIO_CMD, DCI_PIXCLK, EVENTOUT Additional: ADC01_IN6
PA7	23	I/O	5VT	Default: PA7 Alternate: TIMER0_CH0_ON, TIMER2_CH1, TIMER7_CH0_ON, SPI0_MOSI, TIMER13_CH0, ETH_MII_RX_DV, ETH_RMII_CRS_DV, EVENTOUT Additional: ADC01_IN7
PC4	24	I/O	5VT	Default: PC4 Alternate: ETH_MII_RXD0, ETH_RMII_RXD0, EVENTOUT Additional: ADC01_IN14
PC5	25	I/O	5VT	Default: PC5 Alternate: USART2_RX, ETH_MII_RXD1, ETH_RMII_RXD1, EVENTOUT

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GD32F527Rx LQFP64				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Additional: ADC01_IN15
PB0	26	I/O	5VT	Default: PB0 Alternate: TIMER0_CH1_ON, TIMER2_CH2, TIMER7_CH1_ON, SPI2_MOSI, I2S2_SD, USBHS_ULPI_D1, ETH_MII_RXD2, SDIO_D1, EVENTOUT Additional: ADC01_IN8, IREF
PB1	27	I/O	5VT	Default: PB1 Alternate: TIMER0_CH2_ON, TIMER2_CH3, TIMER7_CH2_ON, USBHS_ULPI_D2, ETH_MII_RXD3, SDIO_D2, EVENTOUT, TIMER0_CH2 Additional: ADC01_IN9
PB2	28	I/O	5VT	Default: BOOT1 Alternate: TIMER1_CH3, SPI2_MOSI, I2S2_SD, USBHS_ULPI_D4, SDIO_CK, EVENTOUT
PB10	29	I/O	5VT	Default: PB10 Alternate: TIMER1_CH2, I2C1_SCL, SPI1_SCK, I2S1_CK, I2S2_MCK, USART2_TX, USBHS_ULPI_D3, ETH_MII_RX_ER, SDIO_D7, EVENTOUT
PB11	30	I/O	5VT	Default: PB11 Alternate: TIMER1_CH3, I2C1_SDA, I2S_CKIN, USART2_RX, USBHS_ULPI_D4, ETH_MII_TX_EN, ETH_RMII_TX_EN, EVENTOUT
NC	31	-	-	-
VDD	32	P	-	Default: VDD
PB12	33	I/O	5VT	Default: PB12 Alternate: TIMER0_BRKIN, I2C1_SMBA, SPI1_NSS, I2S1_WS, USART2_CK, CAN1_RX, USBHS_ULPI_D5, ETH_MII_TXD0, ETH_RMII_TXD0, USBHS_ID, EVENTOUT
PB13	34	I/O	5VT	Default: PB13 Alternate: TIMER0_CH0_ON, SPI1_SCK, I2S1_CK, USART2_CTS, CAN1_TX, USBHS_ULPI_D6, ETH_MII_TXD1, ETH_RMII_TXD1, I2C1_TXFRAME, EVENTOUT Additional: USBHS_VBUS
PB14	35	I/O	5VT	Default: PB14 Alternate: TIMER0_CH1_ON, TIMER7_CH1_ON, SPI1_MISO, I2S1_ADD_SD, USART2_RTS, TIMER11_CH0, USBHS_DM, EVENTOUT
PB15	36	I/O	5VT	Default: PB15 Alternate: RTC_REFIN, TIMER0_CH2_ON, TIMER7_CH2_ON, SPI1_MOSI, I2S1_SD, TIMER11_CH1, USBHS_DP, EVENTOUT
PC6	37	I/O	5VT	Default: PC6

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GD32F527Rx LQFP64				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Alternate: TIMER2_CH0, TIMER7_CH0, I2S1_MCK, USART5_TX, SDIO_D6, DCI_D0, TIMER7_CH0_ON, EVENTOUT
PC7	38	I/O	5VT	Default: PC7 Alternate: TIMER2_CH1, TIMER7_CH1, SPI1_SCK, I2S1_CK, I2S2_MCK, USART5_RX, SDIO_D7, DCI_D1, EVENTOUT
PC8	39	I/O	5VT	Default: PC8 Alternate: TIMER2_CH2, TIMER7_CH2, USART5_CK, SDIO_D0, DCI_D2, EVENTOUT
PC9	40	I/O	5VT	Default: PC9 Alternate: CK_OUT1, TIMER2_CH3, TIMER7_CH3, I2C2_SDA, I2S_CKIN, SDIO_D1, DCI_D3, TIMER0_CH1_ON, EVENTOUT
PA8	41	I/O	5VT	Default: PA8 Alternate: CK_OUT0, TIMER0_CH0, I2C2_SCL, USART0_CK, USBFS_SOF, SDIO_D1, CTC_SYNC, EVENTOUT
PA9	42	I/O	5VT	Default: PA9 Alternate: TIMER0_CH1, I2C2_SMBA, SPI1_SCK, I2S1_CK, USART0_TX, SDIO_D2, DCI_D0, EVENTOUT Additional: USBFS_VBUS
PA10	43	I/O	5VT	Default: PA10 Alternate: TIMER0_CH2, USART0_RX, USBFS_ID, DCI_D1, I2C2_TXFRAME, EVENTOUT
PA11	44	I/O	5VT	Default: PA11 Alternate: TIMER0_CH3, USART0_CTS, USART5_TX, CAN0_RX, USBFS_DM, EVENTOUT
PA12	45	I/O	5VT	Default: PA12 Alternate: TIMER0_ETI, USART0_RTS, USART5_RX, CAN0_TX, USBFS_DP, EVENTOUT
PA13	46	I/O	5VT	Default: JTMS, SWDIO, PA13 Alternate: EVENTOUT
NC	47	-	-	
VDD	48	P	-	
PA14	49	I/O	5VT	Default: JTCK, SWCLK, PA14 Alternate: EVENTOUT
PA15	50	I/O	5VT	Default: JTDI/PA15 Alternate: TIMER1_CH0, TIMER1_ETI, SPI0_NSS, SPI2_NSS, I2S2_WS, USART0_TX, EVENTOUT
PC10	51	I/O	5VT	Default: PC10 Alternate: SPI2_SCK, I2S2_CK, USART2_TX, UART3_TX,

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Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				SDIO_D2, DCI_D8, EVENTOUT
PC11	52	I/O	5VT	Default: PC11 Alternate: I2S2_ADD_SD, SPI2_MISO, USART2_RX, UART3_RX, SDIO_D3, DCI_D4, EVENTOUT
PC12	53	I/O	5VT	Default: PC12 Alternate: I2C1_SDA, SPI2_MOSI, I2S2_SD, USART2_CK, UART4_TX, SDIO_CK, DCI_D9, EVENTOUT
PD2	54	I/O	5VT	Default: PD2 Alternate: TIMER2_ETI, UART4_RX, SDIO_CMD, DCI_D11, EVENTOUT
PB3	55	I/O	5VT	Default: JTDO, PB3 Alternate: TRACESWO, TIMER1_CH1, SPI0_SCK, SPI2_SCK, I2S2_CK, USART0_RX, I2C1_SDA, EVENTOUT
PB4	56	I/O	5VT	Default: NJTRST Alternate: TIMER2_CH0, SPI0_MISO, SPI2_MISO, I2S2_ADD_SD, I2C2_SDA, SDIO_D0, I2C0_TXFRAME, TIMER7_CH0, EVENTOUT
PB5	57	I/O	5VT	Default: PB5 Alternate: TIMER2_CH1, I2C0_SMBA, SPI0_MOSI, SPI2_MOSI, I2S2_SD, CAN1_RX, USBHS_ULPI_D7, ETH_PPS_OUT, DCI_D10, SPI0_NSS, EVENTOUT
PB6	58	I/O	5VT	Default: PB6 Alternate: TIMER3_CH0, I2C0_SCL, USART0_TX, CAN1_TX, DCI_D5, EVENTOUT
PB7	59	I/O	5VT	Default: PB7 Alternate: TIMER3_CH1, I2C0_SDA, USART0_RX, DCI_VSYNC, EVENTOUT
BOOT0	60	I/O	5VT	Default: BOOT0
PB8	61	I/O	5VT	Default: PB8 Alternate: TIMER1_CH0, TIMER1_ETI, TIMER3_CH2, TIMER9_CH0, I2C0_SCL, CAN0_RX, ETH_MII_TXD3, SDIO_D4, DCI_D6, EVENTOUT
PB9	62	I/O	5VT	Default: PB9 Alternate: TIMER1_CH1, TIMER3_CH3, TIMER10_CH0, I2C0_SDA, SPI1_NSS, I2S1_WS, CAN0_TX, SDIO_D5, DCI_D7, EVENTOUT
VSS	63	P	-	Default: VSS
VDD	64	P	-	Default: VDD

Notes:

(1) Type: I = input, O = output, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

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2.6.6. GD32F527xx pin alternate functions

Table 2-9. Port A alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PA0		TIMER1_CH0 /TIMER1_ETI	TIMER4_ CH0	TIMER7_E TI				USART1_ CTS	UART3_T X			ETH_MII_C RS				EVENTOUT
PA1		TIMER1_CH1	TIMER4_ CH1			SPI3_MO SI		USART1_ RTS	UART3_R X			ETH_MII_R X_CLK/ETH _RMII_REF _CLK				EVENTOUT
PA2		TIMER1_CH2	TIMER4_ CH2	TIMER8_C H0		I2S_CKIN		USART1_ TX				ETH_MDIO				EVENTOUT
PA3		TIMER1_CH3	TIMER4_ CH3	TIMER8_C H1	I2C3_SDA	I2S1_MCK	SAI0_FS_ 0	USART1_ RX			USBHS_U LPI_D0	ETH_MII_C OL			TLI_B5	EVENTOUT
PA4				TIMER7_C H1_ON		SPI0_NSS	SPI2_NSS/ I2S2_WS	USART1_ CK					USBHS_ SOF	DCI_HSY NC	TLI_VS YNC	EVENTOUT
PA5		TIMER1_CH0 /TIMER1_ETI		TIMER7_C H0_ON		SPI0_SCK					USBHS_U LPI_CK					EVENTOUT
PA6		TIMER0_BR KIN	TIMER2_ CH0	TIMER7_B RKIN	SPI4_NS S	SPI0_MIS O	I2S1_MCK			TIMER12_ CH0			SDIO_C MD	DCI_PIXC LK	TLI_G2	EVENTOUT
PA7		TIMER0_CH0 _ON	TIMER2_ CH1	TIMER7_C H0_ON		SPI0_MO SI				TIMER13_ CH0		ETH_MII_R X_DV/ETH_ RMII_CRS_ DV	EXMC_S DNWE			EVENTOUT
PA8	CK_OUT 0	TIMER0_CH0			I2C2_SCL			USART0_ CK		CTC_SYN C	USBFS_S OF		SDIO_D 1		TLI_R6	EVENTOUT
PA9		TIMER0_CH1			I2C2_SM BA	SPI1_SCK /I2S1_CK	SAI0_SD_ 1	USART0_ TX					SDIO_D 2	DCI_D0		EVENTOUT
PA10		TIMER0_CH2			I2C2_TXF RAME		SPI4_MOS I	USART0_ RX			USBFS_ID			DCI_D1		EVENTOUT
PA11		TIMER0_CH3					SPI3_MIS O	USART0_ CTS	USART5_ TX	CAN0_RX	USBFS_D M				TLI_R4	EVENTOUT
PA12		TIMER0_ETI					SPI4_MIS O	USART0_ RTS	USART5_ RX	CAN0_TX	USBFS_D P				TLI_R5	EVENTOUT
PA13	JTMS/S WDIO															EVENTOUT
PA14	JTCK/S WCLK															EVENTOUT
PA15	JTDI	TIMER1_CH0 /TIMER1_ETI				SPI0_NSS	SPI2_NSS/ I2S2_WS	USART0_ TX								EVENTOUT

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Table 2-10. Port B alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PB0		TIMER0_CH1_ON	TIMER2_CH2	TIMER7_CH1_ON			SPI4_SCK	SPI2_MOSI/I2S2_SD		TLI_R3	USBHS_ULPI_D1	ETH_MII_RXD2	SDIO_D1			EVENTOUT
PB1		TIMER0_CH2_ON	TIMER2_CH3	TIMER7_CH2_ON	TIMER0_CH2		SPI4_NSS			TLI_R6	USBHS_ULPI_D2	ETH_MII_RXD3	SDIO_D2			EVENTOUT
PB2		TIMER1_CH3					SAI0_SD_0	SPI2_MOSI/I2S2_SD			USBHS_ULPI_D4		SDIO_CK			EVENTOUT
PB3	JTDO/TRACESWO	TIMER1_CH1				SPI0_SCK	SPI2_SCK/I2S2_CK	USART0_RX		I2C1_SDA						EVENTOUT
PB4	NJTRST		TIMER2_CH0	TIMER7_CH0	I2C0_TXFRAME	SPI0_MISO	SPI2_MISO	I2S2_ADD_SD		I2C2_SDA			SDIO_D0			EVENTOUT
PB5			TIMER2_CH1		I2C0_SMBA	SPI0_MOSI	SPI2_MOSI/I2S2_SD	SPI0_NSS		CAN1_RX	USBHS_ULPI_D7	ETH_PPS_OUT	EXMC_SDCKE1	DCI_D10		EVENTOUT
PB6			TIMER3_CH0		I2C0_SCL		SPI5_MOSI	USART0_TX		CAN1_TX			EXMC_SDNE1	DCI_D5		EVENTOUT
PB7			TIMER3_CH1		I2C0_SDA			USART0_RX					EXMC_NL	DCI_VSYNC		EVENTOUT
PB8		TIMER1_CH0/TIMER1_ETI	TIMER3_CH2	TIMER9_CH0	I2C0_SCL	SPI5_NSS	SPI4_MOSI			CAN0_RX		ETH_MII_TXD3	SDIO_D4	DCI_D6	TLI_B6	EVENTOUT
PB9		TIMER1_CH1	TIMER3_CH3	TIMER10_CH0	I2C0_SDA	SPI1_NSS/I2S1_WS	SAI0_FS_1			CAN0_TX			SDIO_D5	DCI_D7	TLI_B7	EVENTOUT
PB10		TIMER1_CH2			I2C1_SCL	SPI1_SCK/I2S1_CK	I2S2_MCK	USART2_TX			USBHS_ULPI_D3	ETH_MII_RX_ER	SDIO_D7		TLI_G4	EVENTOUT
PB11		TIMER1_CH3			I2C1_SDA	I2S_CKIN		USART2_RX			USBHS_ULPI_D4	ETH_MII_TX_EN/ETH_RMII_TX_EN			TLI_G5	EVENTOUT
PB12		TIMER0_BRKIN			I2C1_SMBA	SPI1_NSS/I2S1_WS	SPI3_NSS	USART2_CK		CAN1_RX	USBHS_ULPI_D5	ETH_MII_TXD0/ETH_RMII_TXD0	USBHS_ID	SPI5_MISO		EVENTOUT
PB13		TIMER0_CH0_ON			I2C1_TXFRAME	SPI1_SCK/I2S1_CK	SPI3_SCK	USART2_CTS		CAN1_TX	USBHS_ULPI_D6	ETH_MII_TXD1/ETH_RMII_TXD1				EVENTOUT
PB14		TIMER0_CH1_ON		TIMER7_CH1_ON		SPI1_MISO	I2S1_ADD_SD	USART2_RTS		TIMER11_CH0			USBHS_DM			EVENTOUT
PB15	RTC_REFIN	TIMER0_CH2_ON		TIMER7_CH2_ON		SPI1_MOSI/I2S1_SD				TIMER11_CH1			USBHS_DP			EVENTOUT

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Table 2-11. Port C alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PC0				TIMER7_CH2_ON			SAI0_MCLK_1				USBHS_ULPI_STP		EXMC_SDNWE			EVENTOUT
PC1						SPI2_MOSI/I2S2_SD	SAI0_SD_0	SPI1_MOSI/I2S1_SD				ETH_MDC				EVENTOUT
PC2						SPI1_MISO	I2S1_ADD_SD				USBHS_ULPI_DIR	ETH_MII_TXD2	EXMC_SDNE0			EVENTOUT
PC3						SPI1_MOSI/I2S1_SD					USBHS_ULPI_NXT	ETH_MII_TX_CLK	EXMC_SDCKE0			EVENTOUT
PC4												ETH_MII_RXD0/ETH_RMII_RXD0	EXMC_SDNE0			EVENTOUT
PC5								USART2_RX				ETH_MII_RXD1/ETH_RMII_RXD1	EXMC_SDCKE0			EVENTOUT
PC6		TIMER7_CH0_ON	TIMER2_CH0	TIMER7_CH0		I2S1_MCK			USART5_TX				SDIO_D6	DCI_D0	TLI_HSYNC	EVENTOUT
PC7			TIMER2_CH1	TIMER7_CH1		SPI1_SCK/I2S1_CK	I2S2_MCK		USART5_RX				SDIO_D7	DCI_D1	TLI_G6	EVENTOUT
PC8			TIMER2_CH2	TIMER7_CH2					USART5_CK				SDIO_D0	DCI_D2		EVENTOUT
PC9	CK_OUT1	TIMER0_CH1_ON	TIMER2_CH3	TIMER7_CH3	I2C2_SDA	I2S_CKIN							SDIO_D1	DCI_D3		EVENTOUT
PC10							SPI2_SCK/I2S2_CK	USART2_TX	UART3_TX				SDIO_D2	DCI_D8	TLI_R2	EVENTOUT
PC11						I2S2_ADD_SD	SPI2_MISO	USART2_RX	UART3_RX				SDIO_D3	DCI_D4		EVENTOUT
PC12					I2C1_SDA		SPI2_MOSI/I2S2_SD	USART2_CK	UART4_TX				SDIO_CK	DCI_D9		EVENTOUT
PC13						SPI0_SCK										EVENTOUT
PC14																EVENTOUT
PC15																EVENTOUT

Table 2-12. Port D alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PD0						SPI3_MISO	SPI2_MOSI/I2S2_SD			CAN0_RX			EXMC_D2			EVENTOUT

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Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PD1				TIMER7_CH3_ON				SPI1_NSS/I2S1_WS		CAN0_TX			EXMC_D3			EVENTOUT
PD2			TIMER2_ETI						UART4_RX				SDIO_CMD	DCI_D11		EVENTOUT
PD3						SPI1_SCK/I2S1_CK		USART1_CTS					EXMC_CLK	DCI_D5	TLI_G7	EVENTOUT
PD4						I2C3_SCL		USART1_RTS					EXMC_NOE			EVENTOUT
PD5								USART1_TX					EXMC_NWE			EVENTOUT
PD6		TIMER0_CH2_ON				SPI2_MOSI/I2S2_SD	SAI0_SD_0	USART1_RX					EXMC_NWAIT	DCI_D10	TLI_B2	EVENTOUT
PD7								USART1_CK					EXMC_NE0/EXMC_NCE1			EVENTOUT
PD8								USART2_TX					EXMC_D13			EVENTOUT
PD9						SPI2_NSS		USART2_RX					EXMC_D14			EVENTOUT
PD10								USART2_CK					EXMC_D15	SPI5_SCK	TLI_B3	EVENTOUT
PD11								USART2_CTS					EXMC_A16/EXMC_CLE			EVENTOUT
PD12		TIMER0_CH1	TIMER3_CH0					USART2_RTS					EXMC_A17/EXMC_ALE			EVENTOUT
PD13			TIMER3_CH1										EXMC_A18			EVENTOUT
PD14			TIMER3_CH2	TIMER7_CH1									EXMC_D0			EVENTOUT
PD15	CTC_SYNC		TIMER3_CH3					USART2_RX					EXMC_D1			EVENTOUT

Table 2-13. Port E alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PE0			TIMER3_ETI			SPI0_MOSI			UART7_RX				EXMC_NBL0	DCI_D2		EVENTOUT
PE1		TIMER0_CH1_ON		TIMER7_CH3					UART7_TX				EXMC_NBL1	DCI_D3		EVENTOUT
PE2						SPI3_SCK	SAI0_MCLK_0					ETH_MII_TXD3	EXMC_A23			EVENTOUT

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Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PE3							SAI0_SD_1						EXMC_A19			EVENTOUT
PE4						SPI3_NSS	SAI0_FS_0						EXMC_A20	DCI_D4	TLI_B0	EVENTOUT
PE5				TIMER8_CH0		SPI3_MISO	SAI0_SCK_0	SPI0_MISO					EXMC_A21	DCI_D6	TLI_G0	EVENTOUT
PE6				TIMER8_CH1		SPI3_MOSI	SAI0_SD_0						EXMC_A22	DCI_D7	TLI_G1	EVENTOUT
PE7		TIMER0_ETI	TIMER0_CH1						UART6_RX				EXMC_D4			EVENTOUT
PE8		TIMER0_CH0_ON						USART2_TX	UART6_TX				EXMC_D5	SPI5_IO2		EVENTOUT
PE9		TIMER0_CH0											EXMC_D6			EVENTOUT
PE10		TIMER0_CH1_ON											EXMC_D7			EVENTOUT
PE11		TIMER0_CH1				SPI3_NSS	SPI4_NSS						EXMC_D8		TLI_G3	EVENTOUT
PE12		TIMER0_CH2_ON				SPI3_SCK	SPI4_SCK						EXMC_D9		TLI_B4	EVENTOUT
PE13		TIMER0_CH2				SPI3_MISO	SPI4_MISO						EXMC_D10		TLI_DE	EVENTOUT
PE14		TIMER0_CH3				SPI3_MOSI	SPI4_MOSI						EXMC_D11		TLI_PIXCLK	EVENTOUT
PE15		TIMER0_BRKIN											EXMC_D12		TLI_R7	EVENTOUT

Table 2-14. Port F alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PF0	CTC_SYNC				I2C1_SDA		I2C4_SDA						EXMC_A0			EVENTOUT
PF1					I2C1_SCL		I2C4_SCL						EXMC_A1			EVENTOUT
PF2					I2C1_SMBA		I2C4_SMBA						EXMC_A2			EVENTOUT
PF3					I2C1_TXFRAME	SPI2_NSS							EXMC_A3			EVENTOUT
PF4													EXMC_A4			EVENTOUT

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Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PF5													EXMC_A5			EVENTOUT
PF6				TIMER9_CH0		SPI4_NSS	SAI0_SD_1		UART6_RX				EXMC_NIORD			EVENTOUT
PF7				TIMER10_CH0		SPI4_SCK	SAI0_MCLK_1		UART6_TX				EXMC_NREG			EVENTOUT
PF8						SPI4_MISO	SAI0_SCK_1			TIMER12_CH0			EXMC_NIOWR			EVENTOUT
PF9						SPI4_MOSI	SAI0_FS_1			TIMER13_CH0			EXMC_CD			EVENTOUT
PF10					I2C5_SMBA								EXMC_INTR	DCI_D11	TLI_DE	EVENTOUT
PF11					I2C5_SCL	SPI4_MOSI							EXMC_SDNRAS	DCI_D12		EVENTOUT
PF12					I2C5_SDA								EXMC_A6			EVENTOUT
PF13					I2C3_SMBA								EXMC_A7			EVENTOUT
PF14					I2C3_SCL	SPI1_MOSI							EXMC_A8			EVENTOUT
PF15		TIMER0_CH3			I2C3_SDA								EXMC_A9			EVENTOUT

Table 2-15. Port G alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PG0		TIMER0_CH3_ON			I2C3_SDA								EXMC_A10			EVENTOUT
PG1				TIMER7_CH2	I2C3_SCL								EXMC_A11			EVENTOUT
PG2													EXMC_A12			EVENTOUT
PG3													EXMC_A13			EVENTOUT
PG4													EXMC_A14	SPI5_NSS		EVENTOUT
PG5													EXMC_A15			EVENTOUT
PG6							I2C4_SMBA						EXMC_INT1	DCI_D12	TLI_R7	EVENTOUT

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Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PG7							I2C4_SCL		USART5_CK				EXMC_INT2	DCI_D13	TLI_PIXCLK	EVENTOUT
PG8						SPI5_NSS	I2C4_SDA		USART5_RTS			ETH_PPS_OUT	EXMC_SDCLK			EVENTOUT
PG9									USART5_RX				EXMC_NE1/EXMC_NCE2	DCI_VSYNC		EVENTOUT
PG10						SPI5_IO2				TLI_G3			EXMC_NCE3_0/EXMC_NE2	DCI_D2	TLI_B2	EVENTOUT
PG11						SPI5_IO3	SPI3_SCK					ETH_MII_TX_EN/ETH_RMII_TX_EN	EXMC_NCE3_1	DCI_D3	TLI_B3	EVENTOUT
PG12						SPI5_MISO	SPI3_MISO		USART5_RTS	TLI_B4			EXMC_NE3		TLI_B1	EVENTOUT
PG13						SPI5_SCK	SPI3_MOSI		USART5_CTS			ETH_MII_TXD0/ETH_RMII_TXD0	EXMC_A24			EVENTOUT
PG14					I2C4_SCL	SPI5_MOSI	SPI3_NSS		USART5_TX			ETH_MII_TXD1/ETH_RMII_TXD1	EXMC_A25			EVENTOUT
PG15					I2C5_SMBA				USART5_CTS				EXMC_SDNCAS	DCI_D13		EVENTOUT

Table 2-16. Port H alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PH0																EVENTOUT
PH1																EVENTOUT
PH2												ETH_MII_CRS	EXMC_SDCKE0		TLI_R0	EVENTOUT
PH3					I2C1_TXFRAME							ETH_MII_COL	EXMC_SDNE0		TLI_R1	EVENTOUT
PH4					I2C1_SCL	SPI5_SCK					USBHS_ULPI_NXT			SPI5_IO3		EVENTOUT
PH5					I2C1_SDA	SPI4_NSS							EXMC_SDNWE			EVENTOUT

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Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PH6					I2C1_SMBA	SPI4_SCK				TIMER11_CH0		ETH_MII_RXD2	EXMC_SDNE1	DCI_D8		EVENTOUT
PH7					I2C2_SCL	SPI4_MISO						ETH_MII_RXD3	EXMC_SDCKE1	DCI_D9		EVENTOUT
PH8					I2C2_SDA	I2C3_SMBA							EXMC_D16	DCI_HSYNC	TLI_R2	EVENTOUT
PH9					I2C2_SMBA					TIMER11_CH1			EXMC_D17	DCI_D0	TLI_R3	EVENTOUT
PH10			TIMER4_CH0		I2C2_TXFRAME								EXMC_D18	DCI_D1	TLI_R4	EVENTOUT
PH11			TIMER4_CH1			I2C3_SCL							EXMC_D19	DCI_D2	TLI_R5	EVENTOUT
PH12			TIMER4_CH2			I2C3_SDA							EXMC_D20	DCI_D3	TLI_R6	EVENTOUT
PH13				TIMER7_CH0_ON						CAN0_TX			EXMC_D21		TLI_G2	EVENTOUT
PH14				TIMER7_CH1_ON	I2C5_SCL								EXMC_D22	DCI_D4	TLI_G3	EVENTOUT
PH15				TIMER7_CH2_ON	I2C5_SDA								EXMC_D23	DCI_D11	TLI_G4	EVENTOUT

Table 2-17. Port I alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PI0			TIMER4_CH3			SPI1_NSS/I2S1_WS							EXMC_D24	DCI_D13	TLI_G5	EVENTOUT
PI1						SPI1_SCK/I2S1_CK	SPI1_NSS/I2S1_WS						EXMC_D25	DCI_D8	TLI_G6	EVENTOUT
PI2				TIMER7_CH3		SPI1_MISO	I2S1_ADD_SD						EXMC_D26	DCI_D9	TLI_G7	EVENTOUT
PI3		TIMER0_CH0		TIMER7_ETI		SPI1_MOSI/I2S1_SD							EXMC_D27	DCI_D10		EVENTOUT
PI4				TIMER7_BRKIN		SPI4_MOSI							EXMC_NBL2	DCI_D5	TLI_B4	EVENTOUT
PI5				TIMER7_CH0	I2C5_SCL	SPI2_MOSI							EXMC_NBL3	DCI_VSYNC	TLI_B5	EVENTOUT
PI6				TIMER7_CH1									EXMC_D28	DCI_D6	TLI_B6	EVENTOUT
PI7				TIMER7_CH2	I2C5_SDA								EXMC_D29	DCI_D7	TLI_B7	EVENTOUT

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Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PI8																EVENTOUT
PI9										CAN0_RX			EXMC_D30		TLI_VSYNC	EVENTOUT
PI10												ETH_MII_RX_ER	EXMC_D31		TLI_HSYNC	EVENTOUT
PI11											USBHS_ULPI_DIR					EVENTOUT

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3. Functional description

3.1. Arm® Cortex®-M33 core

The Cortex®-M33 processor is a 32-bit processor that possesses low interrupt latency and low-cost debug. The characteristics of integrated and advanced make the Cortex®-M33 processor suitable for market products that require microcontrollers with high performance and low power consumption. The Cortex®-M33 processor is based on the Armv8 architecture and supports a powerful and scalable instruction set including general data processing I/O control tasks, advanced data processing bit field manipulations and DSP. Some system peripherals listed below are also provided by Cortex®-M33:

- Internal Bus Matrix connected with Code bus, System bus, and Private Peripheral Bus (PPB) and debug accesses
- Nested Vectored Interrupt Controller (NVIC)
- Breakpoint Unit (BPU)
- Data Watchpoint and Trace (DWT)
- Instrumentation Trace Macrocell (ITM)
- Serial Wire JTAG Debug Port (SWJ-DP)
- Trace Port Interface Unit (TPIU)
- Memory Protection Unit (MPU)
- Floating Point Unit (FPU)
- DSP Extension (DSP)

3.2. System Security

The GD32F527xx is designed with a comprehensive set of system security features. System security features cover several aspects, including firmware intellectual property protection, device private data protection, and service execution assurance. The key system security features are as follows.

- Memory protections:
  - System FLASH protection.
  - User FLASH protection.
  - SRAM protection.
  - Trusted code protection.
  - Password protection.
  - External SDRAM, Nand-Flash and Nor-Flash protection.
- Boot protection:
  - Unique boot entry.
  - Secure boot.
- Debugging security.
  - Limit debugging.

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- Disable the debugging function.

- Encryption and random numbers.
  - Public key cryptographic acceleration unit (PKCAU).
  - Hash acceleration unit (HAU).
  - Cryptographic acceleration unit (CAU).

3.3. On-chip memory

- Up to 7680KB of main flash memory with ECC for instruction and data
- The region of the MCU executing instructions without waiting time is up to 2048K bytes (in case that Flash size equal to 2048K, all memory is no waiting time). A long delay when CPU fetches the instructions out of the range.
- For flash memory structure with only Bank0 and Bank1_EX, the memory mapping swap is not supported.
- 64B OTP0 (One-time program) block used for user data storage. Additional 128K bytes OTP1 and 128B OTP2.
- 2B One-time programmable nonvolatile EFUSE storage cells.
- Up to 512 KB SRAM for SRAM0, SRAM1 and SRAM2 with ECC.
- Up to 512KB ADDSRAM with ECC.
- Up to 64KB TCMSRAM with ECC.
- Support RAM ECC monitor for each Region.

For GD32F527xx with flash no more than 7680KB, with 16K bytes of 8 sectors, 64K bytes of 2 sectors, 128K bytes of 30 sectors, 256K bytes of 14 sectors. Each sector can be erased individually. The flash memory structure is divided into 4MB dual bank, 2MB dual bank, 1MB single bank, and 512KB single bank, each of which has bank1 extended flash (Bank1_Ex). The Bank1_Ex starts at 0x08400000 and operates in the same way as Bank1.

The GD32F527xx series contain up to 512KB of on-chip SRAM (SRAM0, SRAM1, SRAM2), 512KB of ADDSRAM and up to 64KB TCMSRAM. All of AHB SRAM support byte, half-word (16 bits), and word (32 bits) accesses. TCMSRAM is the tightly-coupled memory SRAM. SRAM0, SRAM1 and SRAM2 are on-chip static random access memories. ADDSRAM is the additional SRAM, which is available only in some particular GD32F527xx devices. The additional 4KB of backup SRAM (BKP SRAM) is implemented in the backup domain, which can keep its content even when the VDD power supply is down.***Table 2-3. GD32F527xx memory map*** shows the memory map of the GD32F527xx series of devices, including Flash, SRAM, peripheral, and other pre-defined regions.

3.4. Clock, reset and supply management

- Internal 16 MHz factory-trimmed RC and external 4 to 32 MHz crystal oscillator
- Internal 48 MHz RC oscillator
- Internal 32 KHz RC calibrated oscillator and external 32.768 KHz crystal oscillator
- Integrated system clock PLL

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- 1.71 to 3.6V application supply and I/Os
- Supply Supervisor: POR (Power On Reset), PDR (Power Down Reset), and low voltage detector (LVD)

The Clock Control Unit (CCU) provides a range of oscillator and clock functions. These include internal RC oscillator and external crystal oscillator, high speed and low speed two types. Several prescalers allow the frequency configuration of the AHB and two APB domains. The maximum frequency of the two AHB domains are 200 MHz. The maximum frequency of the two APB domains including APB1 is 50 MHz and APB2 is 100 MHz. See ***Figure 2-7. GD32F527xx clock tree*** for details on the clock tree.

The Reset Control Unit (RCU) controls three kinds of reset: system reset resets the processor core and peripheral IP components except for the SW-DP controller and the Backup domain. Power-on reset (POR) and power-down reset (PDR) are always active, and ensures proper operation starting from 1.68V and down to 1.64V. The device remains in reset mode when V_{DD} is below a specified threshold. The embedded low voltage detector (LVD) monitors the power supply, compares it to the voltage threshold and generates an interrupt as a warning message for leading the MCU into security.

Power supply schemes:

- V_{DD} range: 1.71V to 3.6V, external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins
- V_{SSA}, V_{DDA} range: 1.71V to 3.6V, external analog power supplies for ADC, reset blocks, RCs and PLL. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively
- V_{BAT} range: 1.71V to 3.6V, power supply for RTC, external clock 32 KHz oscillator and backup registers (through power switch) when V_{DD} is not present

3.5. Boot modes

At startup, boot pins are used to select one of four boot options:

- Boot from main Flash memory (default)
- Boot from system memory
- Boot from on-chip SRAM
- Boot from OTP1

GD32F527xx devices provide three kinds of boot sources which can be selected by the BOOT0 and BOOT1 pins. The details are shown in the following table. The value on the two pins is latched on the 4th rising edge of CK_SYS after a reset. It is up to the user to set the BOOT0 and BOOT1 pins after a power-on reset or a system reset to select the required boot source. Once the two pins have been sampled, they are free and can be used for other purposes.

Table 3-1. Boot modes

Security Protection	EFUSE		Boot pad		BOOT_MODE[2:0]	Boot Select
	NBTSB	BTFOSEL	BOOT0	BOOT1		

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no protection/ Protection level low	0	x	1	1	011	SRAM
no protection/ Protection level low	0	x	1	0	001	BootLoader
no protection/ Protection level low	0	0	0	x	000	Main Flash
no protection/ Protection level low	0	1	0	x	101	OTP1
x	1	0	x	x	000	Main Flash
x	1	1	x	x	101	OTP1
Protection level high	x	0	x	x	000	Main Flash
Protection level high	x	1	x	x	101	OTP1

The boot loader is located in non-user System memory. It is used to reprogram the Flash memory by using USART0 (PA9 and PA10), USART2 (PB10 and PB11, PC10 and PC11, PE8 and PD15), USBFS (PA11 PA12) in device mode. It also can be used to transfer and update the Flash memory code, the data and the vector table sections.

3.6. Power saving modes

The MCU supports three kinds of power saving modes to achieve even lower power consumption. They are sleep mode, deep-sleep mode, and standby mode. These operating modes reduce the power consumption and allow the application to achieve the best balance between the CPU operating time, speed and power consumption.

- **Sleep mode**
  In sleep mode, only the clock of CPU core is off. All peripherals continue to operate and any interrupt / event can wake up the system.
- **Deep-sleep mode**
  In deep-sleep mode, all clocks in the V_{CORE} domain are off, and all of the high speed crystal oscillator (IRC16M, IRC48M, HXTAL) and PLL are disabled. Only the contents of SRAM and registers are retained. Any interrupt or wakeup event from EXTI lines can wake up the system from the deep-sleep mode including the 16 external lines, the RTC alarm, RTC Tamper and TimeStamp event, the LVD output, ENET wakeup, RTC wakeup, I2C wakeup and USB wakeup. When exiting the deep-sleep mode, the IRC16M is selected as the system clock.
- **Standby mode**
  In standby mode, the whole V_{CORE} domain is power off, the LDO is shut down, and all of

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IRC16M, HXTAL and PLL are disabled. The contents of SRAM and registers (except backup registers) are lost. There are four wakeup sources for the standby mode, including the external reset from NRST pin, the RTC, the FWDGT reset, and the rising edge on WKUP pin.

3.7. General-purpose and alternate-function I/Os (GPIO and AFIO)

- Up to 140 fast GPIOs, all mappable on 16 external interrupt lines, each pin weak pull-up/pull-down function
- Output push-pull/open drain enable control
- Analog input/output configuration
- Alternate function input/output configuration

GD32F527xx is up to 140 general purpose I / O pins (GPIO), named PA0 ~ PA15, PB0 ~ PB15, PC0 ~ PC15, PD0 ~ PD15, PE0 ~ PE15, PF0 ~ PF15, PG0 ~ PG15, PH0 ~ PH15 and PI0 ~ PI11 for the device to implement logic input / output functions. Each GPIO port has related control and configuration registers to satisfy the requirements of specific applications. The external interrupts on the GPIO pins of the device have related control and configuration registers in the Interrupt / Event Controller Unit (EXTI).

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), input, peripheral alternate function or analog mode. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current capable except for analog mode.

3.8. CRC calculation unit (CRC)

- 32-bit data input and 32-bit data output register. Calculation period is 4 AHB clock cycles for 32-bit input data size from data entered to the calculation result available.
- Free 8-bit register is unrelated to calculation and can be used for any other goals by any other peripheral devices.
- Fixed polynomial: 0x4C11DB7:
  $X^{32}+X^{26}+X^{23}+X^{22}+X^{16}+X^{12}+X^{11}+X^{10}+X^{8}+X^{7}+X^{5}+X^{4}+X^{2}+X+1$

A cyclic redundancy check (CRC) is an error-detecting code commonly used in digital networks and storage devices to detect accidental changes to raw data. The CRC calculation unit can be used to calculate 32 bit CRC code with fixed polynomial.

3.9. True random number generator (TRNG)

- About 40 periods of TRNG_CLK are needed between two consecutive random numbers
- 32-bit random value seed is generated from analog noise, so the random number is a true random number.

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The true random number generator (TRNG) module can generate a 32-bit random value by using continuous analog noise.

3.10. Public Key Cryptographic Acceleration Unit (PKCAU)

- Support RSA / DH algorithms with up to 3136 bits of operands.
- Support ECC algorithm with up to 640 bits of operands.
- RSA modular exponentiation, RSA CRT exponentiation.
- ECC scalar multiplication, check point on elliptic curve.
- ECDSA (Elliptic Curve Digital Signature Algorithm) signature and verification.
- Support Montgomery multiplication, accelerate RSA, DH and ECC operations.
- Embedded RAM of 3584 bytes.
- Conversion between the Montgomery domain and the natural domain.
- PKCAU is a 32-bit peripheral, only 32-bit access is supported.

Public key encryption is also called asymmetric encryption, asymmetric encryption algorithms use different keys for encryption and decryption. The Public Key Cryptographic Acceleration Unit (PKCAU) can accelerate RSA (Rivest, Shamir and Adleman), Diffie-Hellmann (DH key exchange) and ECC (elliptic curve cryptography) in GF(p) (Galois domain). These operations are performed in the Montgomery domain to improve computational efficiency.

3.11. Hash Acceleration Unit (HAU)

- 32-bit AHB slave peripheral.
- High performance of computation of hash algorithms.
- Little-endian data representation.
- Multiple data types are supported, including no swapping, half-word swapping, byte swapping, and bit swapping with 32-bit data words.
- Automatic data padding to fill the 512-bit message block for digest computation.
- DMA transfer is supported.
- Hash / HMAC process suspended mode.

The hash acceleration unit is used for information security. The secure hash algorithm (SHA-1, SHA-224, SHA-256), the message-digest algorithm (MD5) and the keyed-hash message authentication code (HMAC) algorithm are supported for various applications. The digest will be computed and the length is 160 / 224 / 256 / 128 bits for a message up to $(2^{64} - 1)$ bits computed by SHA-1, SHA-224, SHA-256 and MD5 algorithms respectively. In HMAC algorithm, SHA-1, SHA-224, SHA-256 or MD5 will be called twice as hash functions and authenticating messages can be produced.

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3.12. Cryptographic Acceleration Unit (CAU)

- DES, TDES and AES encryption / decryption algorithms are supported.
- Multiple modes are supported respectively in DES, TDES and AES, including Electronic codebook (ECB), Cipher block chaining (CBC), Counter mode (CTR), Galois / counter mode (GCM), Galois message authentication code mode (GMAC), Counter with CBC-MAC (CCM), Cipher Feedback mode (CFB) and Output Feedback mode(OFB).
- DMA transfer for incoming and outgoing data is supported.

The cryptographic acceleration unit (CAU) is used to encipher and decipher data with DES, Triple-DES or AES (128, 192, or 256) algorithms. DES / TDES / AES algorithms with different key sizes are supported to perform data encryption and decryption in the CAU in multiple modes. The CAU is a 32-bit peripheral, DMA transfer is supported and data can be accessed in the input and output FIFO.

3.13. Direct memory access controller (DMA)

- Two AHB master interface for transferring data, and one AHB slave interface for programming DMA
- 16 channels (8 for DMA0 and 8 for DMA1) and each channel are configurable
- Support independent single, 4, 8, 16-beat incrementing burst memory and peripheral transfer
- Support independent 8, 16, 32-bit memory and peripheral transfer
- Peripherals supported: Timers, ADC, SPI, I2C, USART, UART, DAC, I2S, SDIO, SAI, CAU, HAU and DCI.

The direct memory access (DMA) controller provides a hardware method of transferring data between peripherals and/or memory without intervention from the MCU, thereby increasing system performance by off-loading the MCU from copying large amounts of data and avoiding frequent interrupts to serve peripherals needing more data or having available data.

Two AHB master interfaces and eight four-word depth 32-bit width FIFOs are presented in each DMA controller, which achieves a high DMA transmission performance. There are 16 independent channels in the DMA controller (8 for DMA0 and 8 for DMA1). Each channel is assigned a specific or multiple target peripheral devices for memory access request management. Two arbiters respectively for memory and peripheral are implemented inside to handle the priority among DMA requests.

3.14. Analog to digital converter (ADC)

- 12-bit ADC conversion rate is up to 2.6 MSPS.
- 12-bit, 10-bit, 8-bit or 6-bit configurable resolution for ADC.
- In ADC0 and ADC1, Oversampling ratio arbitrarily adjustable from 2x to 1024X.

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- Oversampling ratio arbitrarily adjustable from 2x to 256X.
- ADC supply requirements: 2.6V to 3.6V, and typical power supply voltage is 3.3V.
- ADC input voltage range: $V_{REFN} \leq V_{IN} \leq V_{REFP}$
- Temperature sensor

A 12-bit successive approximation analog-to-digital converter module(ADC) is integrated on the MCU chip, which can sample analog signals from 16 external channels and 2 internal channels and the battery voltage (VBAT) channel. The 19 ADC sampling channels all support a variety of operation modes. After sampling and conversion, the conversion results can be stored in the corresponding data registers according to the least significant bit(LSB) alignment or the most significant(MSB) bit alignment. An on-chip hardware oversample scheme improves performances and reduces the computational burden of MCU. For motors, power supplies and other applications that have a higher demand for ADC, you can contact our sales staff for more ADC details.

3.15. Digital to analog converter (DAC)

- The Digital-to-analog8-bit or 12-bit resolution. Right or left data alignment.
- DMA support.
- Conversion update synchronously.
- Conversion trigged by external triggers.
- Configurable internal buffer.
- extern voltage reference, V_{REFP}
- Noise wave (LFSR noise mode and Triangle noise mode).
- Two DAC channels in concurrent mode.

The Digital-to-analog converter converts 12-bit digital data to a voltage on the external pins. The digital data can be configured in 8-bit or 12-bit mode, left-aligned or right-aligned mode. DMA can be used to update the digital data on external triggers. The output voltage can be optionally buffered for higher drive capability. The two DAC channels can work independently or concurrently.

3.16. Real time clock (RTC) and backup registers

- Daylight saving compensation supported by software
- External high-accurate low frequency (50Hz or 60Hz) clock used to achieve higher calendar accuracy performed by reference clock detection option function
- Atomic clock adjust (max adjust accuracy is 0.95PPM) for calendar calibration performed by digital calibration function
- Sub-second adjustment by shift function
- Time-stamp function for saving event time
- Two Tamper sources can be chosen and tamper type is configurable
- Programmable calendar and two field maskable alarms
- Maskable interrupt source:

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- Alarm 0 and Alarm 1
- Time-stamp detection
- Tamper detection
- Auto wakeup event

- Twenty 32-bit (80 bytes total) universal backup registers which can keep data under power saving mode. Backup register will be reset if tamper event detected

The RTC provides a time which includes hour/minute/second/sub-second and a calendar includes year/month/day/week day. The time and calendar are expressed in BCD code except sub-second. Sub-second is expressed in binary code. Hour adjust for daylight saving time. Working in power saving mode and smart wakeup is software configurable. Support improving the calendar accuracy using extern accurate low frequency clock.

3.17. Timers and PWM generation

- Two 16-bit Advanced timer (TIMER0 & TIMER7), two 16-bit General-L0 timers (TIMER2 & TIMER3), two 32-bit General-L0 timers (TIMER1 & TIMER4), two 16-bit General-L1 timers (TIMER8 & TIMER11), four 16-bit General-L2 timers (TIMER9, TIMER10, TIMER12, TIMER13) and two 16-bit Basic timer (TIMER5 & TIMER6)
- Up to4 independent channels of PWM, output compare or input capture for each general timer and external trigger input
- 16-bit, motor control PWM advanced timer with programmable dead-time generation for output match
- Encoder interface controller with two inputs using quadrature decoder
- 24-bit SysTick timer down counter
- 2 watchdog timers (free watchdog timer and window watchdog timer)

The advanced timer (TIMER0 & TIMER7) can be used as a three-phase PWM multiplexed on 6 channels. It has complementary PWM outputs with programmable dead-time generation. It can also be used as a complete general timer. The 4 independent channels can be used for input capture, output compare, PWM generation (edge-aligned or center-aligned counting modes) and single pulse mode output. If configured as a general 16-bit timer, it has the same functions as the TIMERx timer. It can be synchronized with external signals or to interconnect with other general timers together which have the same architecture and features.

The general timer, can be used for a variety of purposes including general timer, input signal pulse width measurement or output waveform generation such as a single pulse generation or PWM output, up to 4 independent channels for input capture/output compare. TIMER1 & TIMER4 is based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler. TIMER2 & TIMER3 is based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. TIMER8 ~ TIMER13 is based on a 16-bit auto-reload upcounter and a 16-bit prescaler. The general timer (TIMER1~4) also supports an encoder interface with two inputs using quadrature decoder.

The basic timer, known as TIMER5 & TIMER6, are mainly used for DAC trigger generation. They can also be used as a simple 16-bit time base.

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The GD32F527xx have two watchdog peripherals, free watchdog timer and window watchdog timer. They offer a combination of high safety level, flexibility of use and timing accuracy.

The free watchdog timer includes a 12-bit down-counting counter and an 8-bit prescaler. It is clocked from an independent 32 KHz internal RC and as it operates independently of the main clock, it can operate in deep-sleep and standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management.

The window watchdog timer is based on a 7-bit down counter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early wakeup interrupt capability and the counter can be frozen in debug mode.

The SysTick timer is dedicated for OS, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Auto reload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

3.18. Universal synchronous/asynchronous receiver transmitter (USART/UART)

- Maximum speed up to 12.5 MBits/s for USART0 and USART5 PLCK2 is 100MHz and oversampling is by 8.
- Maximum speed up to 6.25 MBits/s for USART1/2 and UART3/4/6/7 when PLCK1 is 50MHz and oversampling is by 8.
- Supports both asynchronous and clocked synchronous serial communication modes
- IrDA SIR encoder and decoder support
- LIN break generation and detection
- ISO 7816-3 compliant smart card interface

The USART (USART0, USART1, USART2, USART5) and UART (UART3, UART4, UART6, UART7) are used to transfer data between parallel and serial interfaces, provides a flexible full duplex data exchange using synchronous or asynchronous transfer. It is also commonly used for RS-232 standard communication. The USART/UART includes a programmable baud rate generator which is capable of dividing the system clock to produce a dedicated clock for the USART/UART transmitter and receiver.

3.19. Inter-integrated circuit (I2C)

The GD32F527xx device supports six I2C interfaces, which are different in design from the I2C0/1/2 and I2C3/4/5.

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The I2C (inter-integrated circuit) module provides an I2C interface which is an industry standard two-line serial interface for MCU to communicate with external I2C interface. I2C bus uses two serial lines: a serial data line, SDA, and a serial clock line, SCL. The I2C interface implements standard I2C protocol with standard mode (up to 100KHz), fast mode (up to 400KHz) and fast mode plus (up to 1MHz, only for I2C3/4/5) as well as CRC calculation and checking, SMBus (system management bus), and PMBus (power management bus).

I2C0~2:

- Supports standard-mode (up to 100 kHz) and fast-mode (up to 400 kHz).
- Provide arbitration function, optional PEC (packet error checking) generation and checking
- Supports 7-bit and 10-bit addressing mode and general call addressing mode
- SMBus 2.0 and PMBus compatible
- Supports SAM_V mode.
- Supports DMA mode.

I2C3~5:

- Supports 7-bit and 10-bit addressing and general call addressing.
- Multiple 7-bit slave addresses (2 address, 1 with configurable mask).
- Programmable setup time and hold time.
- Supports standard mode (up to 100 kHz) and fast mode (up to 400 kHz) and fast mode plus (up to 1MHz, I2CxFMP (x = 3,4,5) must be enabled in SYSCFG_CFG1).
- Supports DMA mode.
- SMBus 3.0 and PMBus 1.3 compatible.
- Programmable analog and digital noise filters.
- Wakeup from sleep mode and Deep-sleep mode on I2C address match.
- Independent clock from PCLK.

3.20. Serial peripheral interface (SPI)

- Master or slave operation with full-duplex or simplex mode
- Separate transmit and receive buffer, 16-bits wide
- Data frame size can be 8 or 16 bits
- Bit order can be LSB first or MSB first
- Software and hardware NSS management
- Hardware CRC calculation, transmission and checking
- Transmission and reception using DMA
- SPI TI mode supported
- Quad-SPI configuration available in master mode (only in SPI5)

The SPI interface uses 4 pins, among which are the serial data input and output lines (MISO & MOSI), the clock line (SCK) and the slave select line (NSS). Both SPIs can be served by the DMA controller. The SPI interface may be used for a variety of purposes, including simplex synchronous transfers on two lines with a possible bidirectional data line or reliable communication using CRC checking. Quad-SPI master mode is also supported in SPI5.

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3.21. Inter-IC sound (I2S)

- Master or slave operation with transmission or reception mode
- Master or slave operation with full-duplex mode (only in SPI1 and SPI2)
- Four I2S standards supported: Phillips, MSB justified, LSB justified and PCM standard
- Data length can be 16 bits, 24 bits or 32 bits
- Channel length can be 16 bits or 32 bits
- Transmission and reception using a 16 bits wide buffer
- Audio sample frequency can be 8 kHz to 192 kHz using I2S clock divider
- Programmable idle state clock polarity
- Master clock (MCK) can be output
- Transmission and reception using DMA

The inter-IC sound (I2S) supports four audio standards: I2S Phillips standard, MSB justified standard, LSB justified standard, and PCM standard. I2S works at either master or slave mode for transmission and reception. (By using two extra I2S modules called I2S1_ADD and I2S2_ADD, I2S full duplex mode is also supported in SPI1 and SPI2.). The audio sampling frequencies from 8 KHz to 192 KHz is supported.

3.22. Digital camera interface (DCI)

- Support for CCIR656 video interface as well as traditional sensor interface
- Digital video/picture capture
- 8/10/12/14 data width supported
- High transfer efficiency with DMA interface
- Video/picture crop supported
- Various pixel digital encoding formats supported including YCbCr422 / RGB565
- JPEG compression format supported
- Hard/embedded synchronous signals supported

DCI is an 8-bit to 14-bit parallel interface that able to capture video or picture from a camera via Digital Camera Interface. It supports 8/10/12/14-bits data width through DMA operation.

DCI supports various color space such as YUV/RGB, as well as compression format such as JPEG. Support CCIR656 video decoder formats and perform additional processing of the image.

3.23. TFT LCD interface (TLI)

- Supports up to 24-bits data output per pixel
- Supports up to 2048 x 2048 resolution
- Support various pixel formats: ARGB8888, RGB888, RGB565, etc
- Support CLUT (Color Look-Up-Table) and Color-Keying format

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The TFT LCD interface provides a parallel digital RGB (Red, Green and Blue) and signals for horizontal, vertical synchronization, pixel clock and data enable as output to interface directly to a variety of LCD (Liquid Crystal Display) and TFT (Thin Film Transistor) panels. A built-in DMA engine continuously move data from system memory to TLI and then, output to an external LCD display. Two separate layers are supported in TLI, as well as layer window and blending function.

3.24. Serial Audio Interface (SAI)

- Two independent audio sub-blocks
- Each audio sub-block can be configured as any of the master/slave and transmitter/receiver combination with 8-word FIFO
- Local clock divider logic to satisfy the various audio sampling rates
- Flexible audio protocol configuration such as I2S, PCM/DSP, AC'97, LSB or MSB-justified and TDM
- PDM interface, supporting up to 3 microphone pairs
- Mono/Stereo audio capability with mute option
- Frame Synchronization configuration (active level, active length and offset)
- Each audio frame contains up to 16 configurable slots
- Slot length is flexible, and can be configured as active or inactive
- Each slot can hold a data of size 8-, 10-, 16-, 20-, 24-, and 32-bits with configurable first bit offset, and configurable LSB or MSB data transfer
- Two independent DMA interface for each audio sub-block. Support slave mode with a frequency up to 4MHz

The Serial Audio Interface (SAI) is designed to target a wide range of commonly used audio protocols, both in mono and stereo modes, such as I2S, PCM/DSP, AC'97, LSB or MSB-justified and TDM. SPDIF output is offered when the audio block is configured as a transmitter. The SAI can be configured to any of the master/slave and transmitter/receiver combination, full/half-duplex operating mode depends on synchronous/asynchronous configuration of the audio sub-blocks.

3.25. Image processing accelerator (IPA)

- Copy one source image to the destination image
- Convert one source image to the destination image with specific pixel format
- Convert and blend two source images to the destination image with specific pixel format
- Fill up the destination image with a specific color

The IPA provides a configurable and flexible image format conversion from one or two source image to the destination image. Sixteen pixel formats for foreground from 4-bit up to 32-bit per pixel, eleven pixel formats for background from 4-bit up to 32-bit per pixel, and five pixel formats from 16-bit up to 32-bit per pixel for the destination image are supported. Two 256*32 bits LUTs (Look-Up Table) separately for the two source images are implemented for the

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indirect pixel formats.

3.26. Secure digital input and output card interface (SDIO)

- **MMC:** Full support for Multimedia Card System Specification Version 4.2(and previous versions) Card and three different data bus modes: 1-bit (default), 4-bit and 8-bit
- **SD Card:** Full support for *SD Memory Card Specifications Version 2.0*
- **SD I/O:** Full support for *SD I/O Card Specification Version 2.0* card and two different data bus modes: 1-bit (default) and 4-bit
- **CE-ATA:** Full compliance with *CE-ATA digital protocol Version 1.1*
- 48MHz data transfer frequency and 8-bit data transfer mode.
- Interrupt and DMA request to processor.

The secure digital input/output interface (SDIO) defines the SD/SD I/O /MMC CE-ATA card host interface, which provides command/data transfer between the APB2 system bus and SD memory cards, SD I/O cards, Multimedia Card (MMC), and CE-ATA devices.

3.27. External memory controller (EXMC)

- Supported external memory: SRAM, PSRAM/SQPI-PSRAM, ROM, NOR-Flash, 16-bit PC Card, Flash and, 8-bit or 16-bit NAND Flash and Synchronous DRAM(SDRAM)
- Embedded ECC hardware for NAND Flash access
- Two SDRAM banks with independent configuration, up to 13-bits Row Address, 11-bits Column Address, 2-bits internal banks address
- SDRAM Memory size: 4x16Mx32bit (256 MB), 4x16Mx16bit (128 MB), 4x16Mx8bit (64 MB)

The external memory controller EXMC, is used to access a variety of external memories. By configuring the related registers, it can automatically convert AMBA memory access protocol into a specific memory access protocol, such as SRAM, PSRAM, ROM and NOR Flash. Users can also adjust the timing parameters in the configuration registers to improve memory access efficiency. EXMC access space is divided into multiple banks; each bank is assigned to access a specific memory type with flexible parameter configuration as defined in the controlling register.

3.28. Controller area network (CAN)

- Supports CAN protocols version 2.0A, B.
- Supports CAN FD Frame with up to 64 data bytes (ISO11898-1 and Bosch CAN FD specification V1.0).
- Baud rates up to 1 Mbit/s when classical frames and 6 Mbit/s when FD frames.
- Supports transmitter delay compensation.
- Supports the time-triggered communication.

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- Interrupt enable and clear.

CAN bus (Controller Area Network) is a bus standard designed to allow microcontrollers and devices to communicate with each other without a host computer.

As CAN network interface, basic extended CAN supports the CAN protocols version 2.0A, 2.0B, ISO11898-1:2015 and BOSCH CAN FD specification. The CAN interface automatically handles the transmission and the reception of CAN frames. The CAN provides 28 scalable/configurable identifier filter banks. The filters are used for selecting the input message as software requirement and otherwise discarding the message. Three transmit mailboxes are provided to the software for transfer messages. The transmission scheduler decides which mailbox will be transmitted firstly. Three complete messages can be stored in every FIFO. The FIFOs are managed completely by hardware. Two receiving FIFOs are used by hardware to store the incoming messages. In addition, the CAN controller provides all hardware functions, which supports the time-triggered communication option, in safety-critical applications.

3.29. Ethernet (ENET)

- IEEE 802.3 compliant media access controller (MAC) for Ethernet LAN
- 10/100 Mbit/s rates with dedicated DMA controller and SRAM
- Support hardware precision time protocol (PTP) with conformity to IEEE 1588

The Ethernet media access controller (MAC) conforms to IEEE 802.3 specifications and fully supports IEEE 1588 standards. The embedded MAC provides the interface to the required external network physical interface (PHY) for LAN bus connection via an internal media independent interface (MII) or a reduced media independent interface (RMII). The number of MII signals provided up to 16 with 25 MHz output and RMII up to 7 with 50 MHz output. The function of 32-bit CRC checking is also available.

3.30. Universal serial bus full-speed interface (USBFS)

- Supports USB 2.0 host mode at Full-Speed(12Mb/s) or Low-Speed(1.5Mb/s)
- Supports USB 2.0 device mode at Full-Speed(12Mb/s)
- Supports OTG protocol with HNP (Host Negotiation Protocol) and SRP (Session Request Protocol)

USB Full-Speed (USBFS) controller provides a USB-connection solution for portable devices. USBFS supports host and device modes, as well as OTG mode with HNP (Host Negotiation Protocol) and SRP (Session Request Protocol). USBFS contains a full-speed internal USB PHY and external PHY chip is not contained. USBFS supports all the four types of transfer (control, bulk, Interrupt and isochronous) which defined in USB 2.0 protocol.

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3.31. Universal serial bus high-speed interface (USBHS)

- Supports USB 2.0 Host mode at High-Speed(480Mb/s), Full-Speed(12Mb/s) or Low-Speed(1.5Mb/s)
- Supports USB 2.0 device mode at High-Speed(480Mb/s) or Full-Speed(12Mb/s)
- Supports OTG protocol with HNP (Host Negotiation Protocol) and SRP (Session Request Protocol)

USB High-Speed (USBHS) controller provides a USB-connection solution for portable devices. USBHS supports both host and device modes, as well as OTG mode with HNP (Host Negotiation Protocol) and SRP (Session Request Protocol). USBHS provides ULPI interface for external USB PHY integration and it also contains a full-speed USB PHY internal. So for full-speed or low-speed operation, no more external PHY chip is needed. USBHS supports all the four types of transfer (control, bulk, Interrupt and isochronous) defined in USB 2.0 protocol. HUB connection is supported when USBHS operates at high-speed in host mode. There is also a DMA engine operating as an AHB bus master in USBHS to speed up the data transfer between USBHS and system.

3.32. Debug mode

- Serial wire JTAG debug port (SWJ-DP)

The Arm® SWJ-DP Interface is embedded and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

3.33. Package and operation temperature

- BGA176 (GD32F527IxT), LQFP176 (GDF527IxK), LQFP144 (GD32F527Zx), LQFP100 (GD32F527Vx) and LQFP64 (GD32F527Rx)
- Operation temperature range: -40°C to +105°C (industrial level)

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4. Electrical characteristics

To better understand this chapter, read the following before moving on to the rest of this chapter.

- A + or no sign before the current value indicates that the current is output from the MCU.
- A - before the current value indicates that the current is input to the MCU.
- T_A (Ambient temperature) tested condition.
- T_J (Junction temperature) tested condition.
- Value guaranteed by design, not 100% tested in production indicates that the value is derived from simulation of IC designers.
- Value guaranteed by characterization, not 100% tested in production indicates that the value is derived from random test.
- Unless otherwise specified, all values given for V_{DD} = V_{DDA} = 3.3 V, T_A = 25 °C.
- The devices will be damaged or work abnormally if the electrical parameters beyond the range of maximum and minimum values.

See the following table for some abbreviation terms and their descriptions in this chapter.

Table 4-1. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
CAN	Controller Area Network
DAC	Digital-to-Analog Converter
DMA	Direct Memory Access
GPIO	General Purpose Input/Output
JTAG	Joint Test Action Group
PLL	Phase-Locked Loop
PWM	Pulse Width Modulator
USB	Universal Serial Bus
SPI	Serial Peripheral Interface
RMII	Reduced Media Independent Interface

4.1. Absolute maximum ratings

The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 4-2. Absolute maximum ratings(1)(2)(3)(4)

Symbol	Parameter	Min	Max	Unit
V_{DD}	External voltage range(2)	V_{SS} - 0.3	4.0	V

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Symbol	Parameter	Min	Max	Unit
V_{DDA}	External analog supply voltage	V_{SSA} - 0.3	4.0	V
V_{BAT}	External battery supply voltage	V_{SS} - 0.3	4.0	V
V_{IN}	Input voltage on 5VT I/O(3)	V_{SS} - 0.3	VDD + 4.0	V
	Input voltage on other I/O	V_{SS} - 0.3	4.0	
$\|\Delta V_{DDX}\|$	Variations between different V_{DD} power pins	—	50	mV
$\|V_{SSX} - V_{SS}\|$	Variations between different ground pins	—	50	mV
I_{IO}	Maximum current for GPIO pins	—	±25	mA
$\sum I_{IO}$	Maximum current sunk/sourced by all GPIO pin	—	150	
I_{DD}	Maximum current into each V_{DD} pin	—	100	
I_{SS}	Maximum current into each V_{SS} pin	—	100	
$\sum I_{DD}$	Total current into all V_{DD} pins	—	250	
$\sum I_{SS}$	Total current into all V_{SS} pins	—	250	
T_A	Operating temperature range for grade 7 device	-40	+105	°C
P_D(5)	Power dissipation at T_A = 105°C of LQFP176	—	399	mW
	Power dissipation at T_A = 105°C of BGA176	—	444	
	Power dissipation at T_A = 105°C of LQFP144	—	410	
	Power dissipation at T_A = 105°C of LQFP100	—	407	
	Power dissipation at T_A = 105°C of LQFP64	—	367	
T_{STG}	Storage temperature range	-65	+150	°C
T_J	Maximum junction temperature	—	125	°C

(1) Value guaranteed by design, not 100% tested in production.

(2) All main power and ground pins should be connected to an external power source within the allowable range.

(3) V_{IN} maximum value cannot exceed 5.5 V.

(4) It is recommended that V_{DD} and V_{DDA} are powered by the same source. The maximum difference between V_{DD} and V_{DDA} does not exceed 300 mV during power-up and operation.

(5) Value guaranteed by characterization, not 100% tested in production.

4.2. Operating conditions characteristics

Table 4-3. DC operating conditions(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	Supply voltage	—	1.71	3.3	3.6	V
V_{DDA}	Analog supply voltage	Same as V_{DD}	1.71	3.3	3.6	V
V_{BAT}(2)(3)	Battery supply voltage	—	1.71	3.3	3.6	V
V_{CORE}	Core logic supply voltage powered by internal voltage regulator	LDOVS[1:0] = 01	—	1.1	—	V
		LDOVS[1:0] = 1x	—	1.2	—	

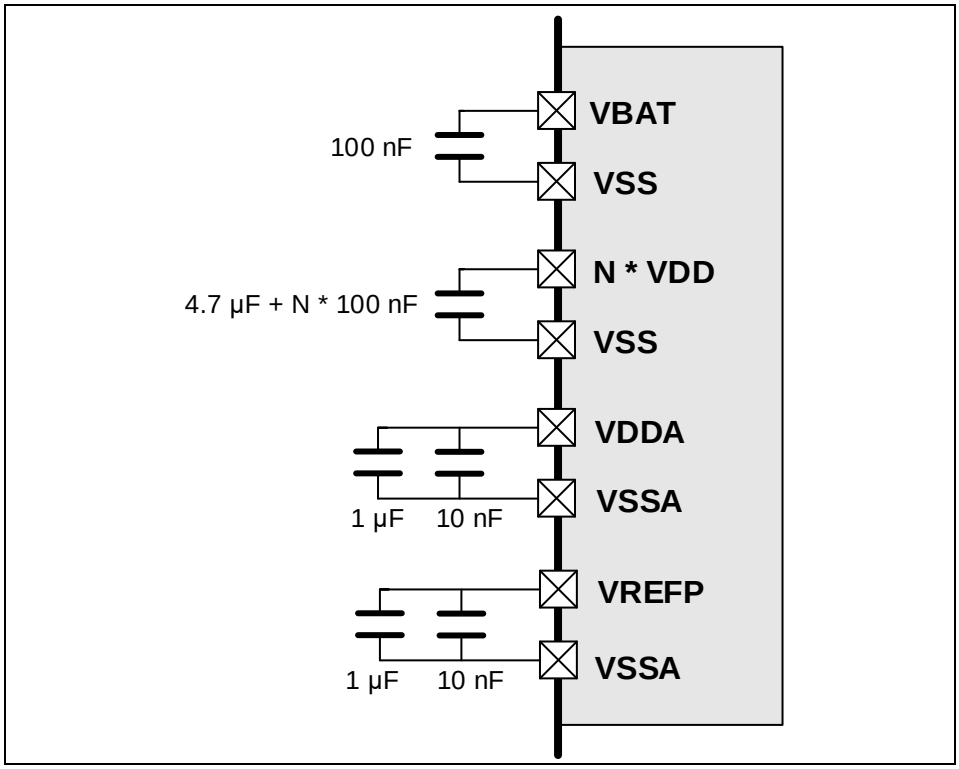
(1) Value guaranteed by design, not 100% tested in production.

(2) In the application which V_{BAT} supply the backup domains, if the V_{BAT} voltage drops below the minimum value, when V_{DD} is powered on again, it is necessary to refresh the registers of backup domains and enable LXTAL again.

(3) When both V_{DD} and V_{BAT} are powered simultaneously, it is required that $V_{BAT} \leq V_{DD}$ + 0.3 V.

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Figure 4-1. Recommended power supply decoupling capacitors(1)



(1) All decoupling capacitors need to be as close as possible to the pins on the PCB board.

Table 4-4. Clock frequency(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{CPU}	Core clock frequency	—	—	200	MHz
f_{AHB}	AHB clock frequency	—	—	200	
f_{APB1}	APB1 clock frequency	—	—	50	
f_{APB2}	APB2 clock frequency	—	—	100	

(1) Value guaranteed by design, not 100% tested in production.

Table 4-5. Operating conditions at Power up / Power down(1)

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	—	0	∞	µs/V
	V_{DD} fall time rate		50	∞	
t_{VDDA}	V_{DDA} rise time rate	—	0	∞	
	V_{DDA} fall time rate		50	∞	

(1) Value guaranteed by design, not 100% tested in production.

Table 4-6. Start-up timings of Operating conditions(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{start-up}$	Start-up time	Code area in FLASH = 1536 KB	65	77	80	ms
		Code area in FLASH = 2048 KB	85	99	105	

(1) Guaranteed by design, not tested in production.

(2) After power-up, the start-up time is the time between the rising edge of NRST high and the first I/O instruction conversion in SystemInit function.

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Table 4-7. Power saving mode wakeup timings characteristics(1)

Symbol	Parameter			Min	Typ	Max	Unit
t_{Sleep}(2)	Wakeup from Sleep mode				0.71	—	μs
$t_{Deep-sleep}$(2)	Wakeup from Deep-sleep mode	LDO On	LOWDRIVER_ENABLE	—	1.72	—	
			LOWDRIVER_DISABLE	—	1.72	—	
		LDO in low power mode	LOWDRIVER_ENABLE	—	1.72	—	
			LOWDRIVER_DISABLE	—	1.72	—	
$t_{Standby}$(3)	Wakeup from Standby mode		Code area in FLASH = 1536 KB	65	77	80	ms
			Code area in FLASH = 2048 KB	85	99	105	

(1) The wakeup time is measured from the wakeup event to the point at which the application code reads the first instruction under the below conditions: V_{DD} = V_{DDA} = 3.3 V, IRC16M = System clock = 16MHz.

(2) Value guaranteed by characterization, not tested in production.

(3) Value guaranteed by design, not 100% tested in production.

4.3. Power consumption

The power measurements specified in the tables represent that code with data executing from on-chip Flash with the following specifications.

Table 4-8. Power consumption characteristics(2)(3)(4)(5)

Symbol	Parameter	Conditions	T_A = -40 °C		T_A = 25 °C		T_A = 105 °C		Unit
			Typ(1)	Max	Typ(1)	Max	Typ(1)	Max	
I_{DD}+I_{DDA}	Supply current (Run mode)	VDD = VDDA = 3.3 V, HXTAL = 25 MHz, System clock = 200 MHz, All peripherals enabled	88.83	—	92.47	—	142.07	—	mA
		VDD = VDDA = 3.3 V, HXTAL = 25 MHz, System clock = 200 MHz, All peripherals disabled	39.73	—	45.90	—	86.27	—	mA
		VDD = VDDA = 3.3 V, HXTAL = 25 MHz, System clock = 180 MHz, All peripherals enabled	80.23	—	83.73	—	132.63	—	mA
		VDD = VDDA = 3.3 V, HXTAL = 25 MHz, System clock = 180 MHz, All peripherals disabled	36.00	—	41.77	—	82.03	—	mA
		VDD = VDDA = 3.3 V, HXTAL = 25 MHz, System clock = 168 MHz, All peripherals enabled	75.03	—	78.40	—	126.90	—	mA
		VDD = VDDA = 3.3 V, HXTAL = 25 MHz, System clock = 168 MHz, All peripherals disabled	33.73	—	39.30	—	79.47	—	mA

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Symbol	Parameter	Conditions	T_A = -40 °C		T_A = 25 °C		T_A = 105 °C		Unit
			Typ(1)	Max	Typ(1)	Max	Typ(1)	Max	
		VDD = VDDA = 3.3 V, HXTAL = 25 MHz, System clock = 120 MHz, All peripherals enabled	54.20	—	57.40	—	103.43	—	mA
		VDD = VDDA = 3.3 V, HXTAL = 25 MHz, System clock = 120 MHz, All peripherals disabled	24.67	—	29.43	—	69.33	—	mA
		VDD = VDDA = 3.3 V, HXTAL = 25 MHz, System clock = 108 MHz, All peripherals enabled	49.00	—	52.10	—	97.57	—	mA
		VDD = VDDA = 3.3 V, HXTAL = 25 MHz, System clock = 108 MHz, All peripherals disabled	22.47	—	26.97	—	66.83	—	mA
		VDD = VDDA = 3.3 V, HXTAL = 25 MHz, System clock = 90 MHz, All peripherals enabled	41.20	—	44.23	—	88.70	—	mA
		VDD = VDDA = 3.3 V, HXTAL = 25 MHz, System clock = 90 MHz, All peripherals disabled	19.07	—	23.23	—	63.00	—	mA
		VDD = VDDA = 3.3 V, HXTAL = 25 MHz, System clock = 60 MHz, All peripherals enabled	28.20	—	31.07	—	74.00	—	mA
		VDD = VDDA = 3.3 V, HXTAL = 25 MHz, System clock = 60 MHz, All peripherals disabled	13.40	—	17.07	—	56.73	—	mA
		VDD = VDDA = 3.3 V, HXTAL = 25 MHz, System clock = 30 MHz, All peripherals enabled	16.13	—	18.90	—	60.40	—	mA
		VDD = VDDA = 3.3 V, HXTAL = 25 MHz, System clock = 30 MHz, All peripherals disabled	8.40	—	11.57	—	51.20	—	mA
		VDD = VDDA = 3.3 V, HXTAL = 25 MHz, System clock = 25 MHz, All peripherals enabled	13.77	—	16.50	—	57.67	—	mA
		VDD = VDDA = 3.3 V, HXTAL = 25 MHz, System clock = 25 MHz, All peripherals disabled	7.40	—	10.43	—	50.03	—	mA
		VDD = VDDA = 3.3 V, HXTAL = 25 MHz, System clock = 16 MHz, All peripherals enabled	9.60	—	12.30	—	52.90	—	mA
		VDD = VDDA = 3.3 V, HXTAL = 25 MHz, System clock = 16 MHz, All peripherals disabled	5.50	—	8.40	—	48.00	—	mA

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Symbol	Parameter	Conditions	T_A = -40 °C		T_A = 25 °C		T_A = 105 °C		Unit
			Typ(1)	Max	Typ(1)	Max	Typ(1)	Max	
		VDD = VDDA = 3.3 V, HXTAL = 25 MHz, System clock = 8 MHz, All peripherals enabled	5.87	—	8.47	—	48.67	—	mA
		VDD = VDDA = 3.3 V, HXTAL = 25 MHz, System clock = 8 MHz, All peripherals disabled	3.80	—	6.57	—	46.20	—	mA
	Supply current (Sleep mode)	VDD = VDDA = 3.3 V, HXTAL = 25 MHz, System clock = 200 MHz,CPU clock off, All peripherals enabled	65.57	—	69.80	—	115.57	—	mA
		VDD = VDDA = 3.3 V, HXTAL = 25 MHz, System clock = 200 MHz, CPU clock off, All peripherals disabled	18.43	—	21.37	—	62.00	—	mA
		VDD = VDDA = 3.3 V, HXTAL = 25 MHz, System clock = 180 MHz, CPU clock off, All peripherals enabled	59.27	—	63.30	—	108.43	—	mA
		VDD = VDDA = 3.3 V, HXTAL = 25 MHz, System clock = 180 MHz, CPU clock off, All peripherals disabled	16.83	—	19.70	—	60.20	—	mA
		VDD = VDDA = 3.3 V, HXTAL = 25 MHz, System clock = 168 MHz, CPU clock off, All peripherals enabled	55.47	—	59.40	—	104.17	—	mA
		VDD = VDDA = 3.3 V, HXTAL = 25 MHz, System clock = 168 MHz, CPU clock off, All peripherals disabled	15.83	—	18.67	—	59.03	—	mA
		VDD = VDDA = 3.3 V, HXTAL = 25 MHz, System clock = 120 MHz, CPU clock off, All peripherals enabled	40.23	—	43.77	—	87.07	—	mA
		VDD = VDDA = 3.3 V, HXTAL = 25 MHz, System clock = 120 MHz, CPU clock off, All peripherals disabled	11.90	—	14.67	—	54.63	—	mA
		VDD = VDDA = 3.3 V, HXTAL = 25 MHz, System clock = 108 MHz, CPU clock off, All peripherals enabled	36.40	—	39.87	—	82.70	—	mA

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Symbol	Parameter	Conditions	T_A = -40 °C		T_A = 25 °C		T_A = 105 °C		Unit
			Typ(1)	Max	Typ(1)	Max	Typ(1)	Max	
		VDD = VDDA = 3.3 V, HXTAL = 25 MHz, System clock = 108 MHz, CPU clock off, All peripherals disabled	10.93	—	13.67	—	53.53	—	mA
		VDD = VDDA = 3.3 V, HXTAL = 25 MHz, System clock = 90 MHz, CPU clock off, All peripherals enabled	30.70	—	34.00	—	76.23	—	mA
		VDD = VDDA = 3.3 V, HXTAL = 25 MHz, System clock = 90 MHz, CPU clock off, All peripherals disabled	9.47	—	12.17	—	51.90	—	mA
		VDD = VDDA = 3.3 V, HXTAL = 25 MHz, System clock = 60 MHz, CPU clock off, All peripherals enabled	21.17	—	24.23	—	65.60	—	mA
		VDD = VDDA = 3.3 V, HXTAL = 25 MHz, System clock = 60 MHz, CPU clock off, All peripherals disabled	7.00	—	9.67	—	49.20	—	mA
		VDD = VDDA = 3.3 V, HXTAL = 25 MHz, System clock = 30 MHz, CPU clock off, All peripherals enabled	12.63	—	15.43	—	55.90	—	mA
		VDD = VDDA = 3.3 V, HXTAL = 25 MHz, System clock = 30 MHz, CPU clock off, All peripherals disabled	5.20	—	7.83	—	47.20	—	mA
		VDD = VDDA = 3.3 V, HXTAL = 25 MHz, System clock = 25 MHz, CPU clock off, All peripherals enabled	10.87	—	13.63	—	53.87	—	mA
		VDD = VDDA = 3.3 V, HXTAL = 25 MHz, System clock = 25 MHz, CPU clock off, All peripherals disabled	4.70	—	7.30	—	46.63	—	mA
		VDD = VDDA = 3.3 V, HXTAL = 25 MHz, System clock = 16 MHz, CPU clock off, All peripherals enabled	7.73	—	10.40	—	50.30	—	mA
		VDD = VDDA = 3.3 V, HXTAL = 25 MHz, System clock = 16	3.80	—	6.33	—	45.67	—	mA

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Symbol	Parameter	Conditions	T_A = -40 °C		T_A = 25 °C		T_A = 105 °C		Unit
			Typ(1)	Max	Typ(1)	Max	Typ(1)	Max	
		MHz, CPU clock off, All peripherals disabled							
		VDD = VDDA = 3.3 V, HXTAL = 25 MHz, System clock = 8 MHz, CPU clock off, All peripherals enabled	4.93	—	7.57	—	47.10	—	mA
		VDD = VDDA = 3.3 V, HXTAL = 25 MHz, System clock = 8 MHz, CPU clock off, All peripherals disabled	2.97	—	5.53	—	44.80	—	mA
	Supply current (Deep-sleep mode)	VDD = VDDA = 3.3 V, LDO in run mode and normal driver mode, IRC32K off, RTC off, All GPIOs analog mode	0.56	—	2.88	—	37.00	—	mA
		VDD = VDDA = 3.3 V, LDO in low power mode and normal driver mode, IRC32K off, RTC off, All GPIOs analog mode	0.49	—	2.82	—	36.77	—	mA
		VDD = VDDA = 3.3 V, LDO in run mode and low driver mode, IRC32K off, RTC off, All GPIOs analog mode	0.52	10.50	2.85	11.00	36.83	80.00	mA
		VDD = VDDA = 3.3 V, LDO in low power mode and low driver mode, IRC32K off, RTC off, All GPIOs analog mode	0.46	—	2.78	—	36.50	—	mA
	Supply current (Standby mode)	VDD = VDDA = 3.3 V, LXTAL off, IRC32K on, RTC on, backup SRAM LDO ON	8.19	—	13.68	—	96.73	—	µA
		VDD = VDDA = 3.3 V, LXTAL off, IRC32K on, RTC off, backup SRAM LDO ON	7.94	—	13.44	—	96.13	—	µA
		VDD = VDDA = 3.3 V, LXTAL off, IRC32K off, RTC off, backup SRAM LDO ON	7.38	—	12.91	—	95.37	—	µA
		VDD = VDDA = 3.3 V, LXTAL off, IRC32K off, RTC off, backup SRAM LDO OFF	1.82	5.50	2.31	6.00	14.10	30.00	µA
I_{BAT}	Battery supply current	VDD off, VDDA off, Vbat=3.6V, LXTAL on with external crystal, RTC on, LXTAL High driving, backup SRAM LDO ON	7.18	—	12.00	—	77.20	—	µA

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Symbol	Parameter	Conditions	T_A = -40 °C		T_A = 25 °C		T_A = 105 °C		Unit
			Typ(1)	Max	Typ(1)	Max	Typ(1)	Max	
	(Backup mode)	VDD off, VDDA off, Vbat=3.3V, LXTAL on with external crystal, RTC on, LXTAL High driving, backup SRAM LDO ON	7.05	—	11.82	—	76.57	—	µA
		VDD off, VDDA off, Vbat=2.6V, LXTAL on with external crystal, RTC on, LXTAL High driving, backup SRAM LDO ON	6.90	—	11.61	—	75.83	—	µA
		VDD off, VDDA off, Vbat=1.8V, LXTAL on with external crystal, RTC on, LXTAL High driving, backup SRAM LDO ON	6.78	—	11.48	—	75.47	—	µA
		VDD off, VDDA off, Vbat=3.6V, LXTAL on with external crystal, RTC on, LXTAL High driving, backup SRAM LDO OFF	1.62	—	1.88	—	2.96	—	µA
		VDD off, VDDA off, Vbat=3.3V, LXTAL on with external crystal, RTC on, LXTAL High driving, backup SRAM LDO OFF	1.54	—	1.77	—	2.71	—	µA
		VDD off, VDDA off, Vbat=2.6V, LXTAL on with external crystal, RTC on, LXTAL High driving, backup SRAM LDO OFF	1.42	—	1.64	—	2.40	—	µA
		VDD off, VDDA off, Vbat=1.8V, LXTAL on with external crystal, RTC on, LXTAL High driving, backup SRAM LDO OFF	1.33	—	1.54	—	2.23	—	µA
		VDD off, VDDA off, Vbat=3.6V, LXTAL on with external crystal, RTC on, LXTAL Low driving, backup SRAM LDO ON	6.53	—	11.27	—	76.27	—	µA
		VDD off, VDDA off, Vbat=3.3V, LXTAL on with external crystal, RTC on, LXTAL Low driving, backup SRAM LDO ON	6.41	—	11.08	—	75.60	—	µA
		VDD off, VDDA off, Vbat=2.6V, LXTAL on with external crystal, RTC on, LXTAL Low driving, backup SRAM LDO ON	6.25	—	10.88	—	74.93	—	µA
		VDD off, VDDA off, Vbat=1.8V, LXTAL on with external crystal,	6.14	—	10.75	—	74.53	—	µA

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Symbol	Parameter	Conditions	T_A = -40 °C		T_A = 25 °C		T_A = 105 °C		Unit
			Typ(1)	Max	Typ(1)	Max	Typ(1)	Max	
		RTC on, LXTAL Low driving, backup SRAM LDO ON							
		VDD off, VDDA off, Vbat=3.6V, LXTAL on with external crystal, RTC on, LXTAL Low driving, backup SRAM LDO OFF	0.96	—	1.12	—	1.98	—	µA
		VDD off, VDDA off, Vbat=3.3V, LXTAL on with external crystal, RTC on, LXTAL Low driving, backup SRAM LDO OFF	0.89	—	1.02	—	1.74	—	µA
		VDD off, VDDA off, Vbat=2.6V, LXTAL on with external crystal, RTC on, LXTAL Low driving, backup SRAM LDO OFF	0.78	—	0.90	—	1.46	—	µA
		VDD off, VDDA off, Vbat=1.8V, LXTAL on with external crystal, RTC on, LXTAL Low driving, backup SRAM LDO OFF	0.69	—	0.80	—	1.30	—	µA

(1) Value guaranteed by characterization, not 100% tested in production.
(2) When analog peripheral blocks such as ADCs, DACs, HXTAL, LXTAL, IRC16M, or IRC32K are ON, an additional power consumption should be considered.
(3) When System Clock is greater than 8 MHz, a crystal 8 MHz is used, and the HXTAL bypass function is closed, using PLL.
(4) During power consumption test, GPIO needs to be configure as Analog Input mode except standby mode.
(5) All GPIOs are configured as analog mode except standby mode.

4.4. EMC characteristics

System level ESD (Electrostatic discharge, according to IEC 61000-4-2) and EFT (Electrical Fast Transient/burst, according to IEC 61000-4-4) testing result is given in the ***Table 4-9. System level ESD and EFT characteristics***(1). System level ESD is for end-customer operation, it includes ESD field events on system level occur in an unprotected area (outside EPA). System level ESD protection necessary to satisfy higher ESD levels.

Table 4-9. System level ESD and EFT characteristics(1)

Symbol	Description	Conditions	Package	Unit	Level
V_{ESD}	Contact / Air mode high voltage stressed on few special I/O pins	V_{DD} = 3.3 V, T_J = 25 °C, f_{HCLK} = 200 MHz IEC 61000-4-2	LQFP176	CD 8kV AD 15kV	4A
V_{EFT}	Fast transient high voltage burst stressed on Power and GND	V_{DD} = 3.3 V, T_J = 25 °C, f_{HCLK} = 200 MHz IEC 61000-4-4	LQFP176	4kV	4A

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(1) Value guaranteed by characterization, not 100% tested in production.

EMI (Electromagnetic Interference) emission test result is given in the ***Table 4-10. EMI characteristics***(1), The electromagnetic field emitted by the device are monitored while an application, executing EEMBC code, is running. The test is compliant with SAE J1752-3:2017 standard which specifies the test board and the pin loading.

Table 4-10. EMI characteristics(1)

Symbol	Parameter	Conditions	Package	Max vs. [f_{HXTAL}/f_{HCLK}] 25MHz / 200 MHz			Unit
				0.1-30MHz	30-130MHz	130MHz-1GHz	
S_{EMI}	Peak level	V_{DD} = 3.6 V, T_J = +25 °C, f_{HCLK} = 200 MHz, conforms to SAE J1752-3:2017	LQFP176	4.70	14.58	13.48	dBμV

(1) Value guaranteed by characterization, not 100% tested in production.

Component level ESD include HBM (Human body model, according to ANSI/ESDA/JEDEC JS-001) and CDM (ANSI/ESDA/JEDEC JS-002), that ESD field events during manufacturing in an ESD protected area, such as PCB assembly/repair, IC assembly/test and Fab environment. The ESD protected area (EPA) has many measures, for instance ESD protective packaging, grounding person wrist strap to ground (or flooring/footwear), grounded work surface and ionizer.

Static latch-up (LU, according to JEDEC78) test is based on the two measurement methods, I/O current injection value (I-test) and power supply over-voltage value.

Table 4-11. Component level ESD and latch-up characteristics(1)

Symbol	Description	Conditions	Package	Max	Unit	Level
V_{HBM}	Human body model electrostatic discharge voltage (Any pin combination)	T_J = 25 °C; JS-001-2017	LQFP176	2000	V	2
V_{CDM}	Charge device model electrostatic discharge voltage (All pins)	T_J = 25 °C; JS-002-2018	LQFP176	500	V	C2a
LU	I-test	T_A = 125 °C, JESD78F	LQFP176	200	mA	Class II Level A
	V_{supply} over voltage			5.4	V	

(1) Value guaranteed by characterization, not 100% tested in production.

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4.5. Power supply supervisor characteristics

Table 4-12. Power supply supervisor characteristics(1)

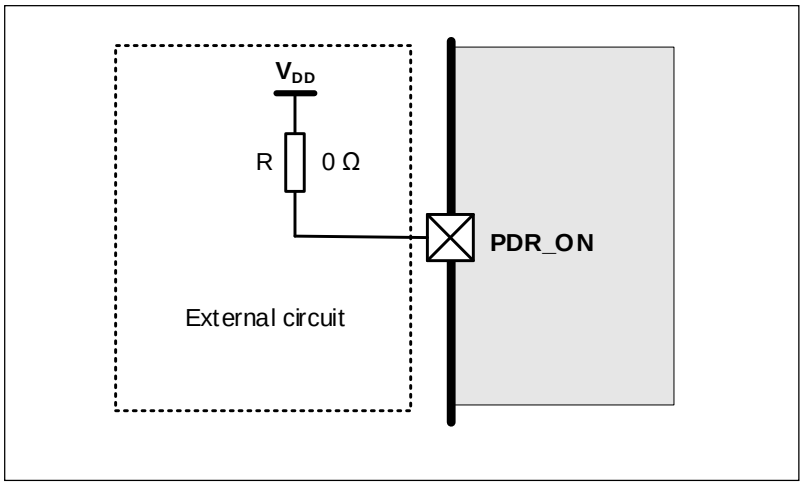
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{LVD}	Low voltage Detector level selection	LVDT<2:0> = 000(rising edge)	1.96	2.14	2.28	V
		LVDT<2:0> = 000(falling edge)	1.87	2.04	2.18	
		LVDT<2:0> = 001(rising edge)	2.09	2.28	2.43	
		LVDT<2:0> = 001(falling edge)	2.00	2.18	2.32	
		LVDT<2:0> = 010(rising edge)	2.22	2.42	2.58	
		LVDT<2:0> = 010(falling edge)	2.13	2.32	2.47	
		LVDT<2:0> = 011(rising edge)	2.35	2.56	2.72	
		LVDT<2:0> = 011(falling edge)	2.26	2.46	2.62	
		LVDT<2:0> = 100(rising edge)	2.49	2.7	2.87	
		LVDT<2:0> = 100(falling edge)	2.39	2.6	2.77	
		LVDT<2:0> = 101(rising edge)	2.62	2.84	3.02	
		LVDT<2:0> = 101(falling edge)	2.52	2.74	2.91	
		LVDT<2:0> = 110(rising edge)	2.75	2.98	3.16	
		LVDT<2:0> = 110(falling edge)	2.65	2.88	3.06	
		LVDT<2:0> = 111(rising edge)	2.88	3.12	3.31	
		LVDT<2:0> = 111(falling edge)	2.78	3.02	3.21	
$V_{LVD\ (HYST)}$	LVD hystersis	—	—	100	—	mV
V_{POR}	Power on reset threshold	—	1.63	1.68	1.73	V
V_{PDR}	Power down reset threshold	—	1.59	1.64	1.69	
$V_{PDR\ (HYST)}$	PDR hysteresis	—	—	40	—	mV
V_{BOR1}	Brown-out reset threshold 1	rising edge	2.12	2.3	2.45	V
		falling edge	2.02	2.2	2.34	
V_{BOR2}	Brown-out reset threshold 2	rising edge	2.40	2.6	2.76	V
		falling edge	2.30	2.5	2.66	
V_{BOR3}	Brown-out reset threshold 3	rising edge	2.68	2.9	3.08	V
		falling edge	2.58	2.8	2.97	
$V_{BOR(HYST)}$	BOR hysteresis	—	—	100	—	mV

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{RST(TEMPO)}$	Reset temporization	—	1.5	2.0	2.6	ms

(1) Value guaranteed by design, not 100% tested in production.

Figure 4-2. Recommended PDR_ON pin circuit



(1) The PDR supervisor can be enabled/disabled through PDR_ON pin.

(2) When PDR_ON pin is connected to VSS (Internal Reset OFF), the VBAT functionality is no more available and VBAT pin should be connected to VDD.

(3) The PDR_ON pin must be kept at high level. The user can flexibly adjust the value of the pull-up resistor R according to the specific scenario for a better performance.

4.6. External clock characteristics

Table 4-13. High speed external clock (HXTAL) generated from a crystal/ceramic characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HXTAL}	Crystal or ceramic frequency	V_{DD} = 3.3 V	4	8	32	MHz
R_F	Feedback resistor	V_{DD} = 3.3 V	—	400	—	kΩ
C_{HXTAL}(2)	Recommended matching capacitance on OSCIN and OSCOUT	—	—	20	30	pF
$Duty_{HXTAL}$	Crystal or ceramic duty cycle	—	30	50	70	%
g_m(3)	Oscillator transconductance	Startup	—	30	—	mA/V
$I_{DD(HXTAL)}$	Crystal or ceramic operating current	V_{DD} = 3.3 V HXTAL = 8 MHz	—	1.1	—	mA
$t_{START(HXTAL)}$	Crystal or ceramic startup time	V_{DD} = 3.3 V HXTAL = 8 MHz	—	1.8	—	ms

(1) Value guaranteed by design, not 100% tested in production.

(2) $C_{HXTAL1} = C_{HXTAL2} = 2*(C_{LOAD} - C_S)$, For C_{HXTAL1} and C_{HXTAL2}, it is recommended matching capacitance on OSCIN and OSCOUT. For C_{LOAD}, it is crystal/ceramic load capacitance, provided by the crystal or ceramic manufacturer. For C_S, it is PCB and MCU pin stray capacitance.

(3) More details about g_m could be found in ***AN052 GD32 MCU Resonator-Based Clock Circuits.***

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Table 4-14. High speed external clock characteristics (HXTAL in bypass mode)(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{HXTAL(EXT)}$	External clock source or oscillator frequency	1.71 V ≤ V_{DD} ≤ 3.6 V	1	—	50	MHz
V_{HXTALH}	OSCIN input pin high level voltage	V_{DD} = 3.3 V	0.7 V_{DD}	—	V_{DD}	V
V_{HXTALL}	OSCIN input pin low level voltage		V_{SS}	—	0.3 V_{DD}	V
$t_{H/L(HXTAL)}$	OSCIN high or low time	—	5	—	—	ns
$t_{R/F(HXTAL)}$	OSCIN rise or fall time	—	—	—	10	ns
C_{IN}	OSCIN input capacitance	—	—	5	—	pF
$Duty_{HXTAL}$	Duty cycle	—	40	—	60	%

(1) Value guaranteed by design, not 100% tested in production.

Table 4-15. Low speed external clock (LXTAL) generated from a crystal/ceramic characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LXTAL}	Crystal or ceramic frequency	—	—	32.768	—	kHz
C_{LXTAL}(2)	Recommended matching capacitance on OSC32IN and OSC32OUT	—	—	15	—	pF
$Duty_{LXTAL}$	Crystal or ceramic duty cycle	—	30	—	70	%
g_m(3)	Oscillator transconductance	LXTALDRI[1:0] = 00	—	4.6	—	μA/V
		LXTALDRI[1:0] = 01	—	7	—	
		LXTALDRI[1:0] = 10	—	13.9		
		LXTALDRI[1:0] = 11	—	20.8		
$I_{DD(LXTAL)}$	Crystal or ceramic operating current	LXTALDRI[1:0] = 00	—	0.6		
		LXTALDRI[1:0] = 01	—	0.8		
		LXTALDRI[1:0] = 10		1.1	—	μA
		LXTALDRI[1:0] = 11		1.6	—	
$t_{START(LXTAL)}$	Crystal or ceramic startup time	—	—	1.8	—	s

(1) Value guaranteed by design, not 100% tested in production.

(2) $C_{LXTAL1} = C_{LXTAL2} = 2*(C_{LOAD} - C_S)$, For C_{LXTAL1} and C_{LXTAL2}, it is recommended matching capacitance on OSC32IN and OSC32OUT. For C_{LOAD}, it is crystal/ceramic load capacitance, provided by the crystal or ceramic manufacturer. For C_S, it is PCB and MCU pin stray capacitance.

(3) More details about g_m could be found in ***AN052 GD32 MCU Resonator-Based Clock Circuits.***

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Table 4-16. Low speed external user clock characteristics (LXTAL in bypass mode)(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{LXTAL(EXT)}$	External clock source or oscillator frequency	V_{DD} = 3.3 V	—	32.768	1000	kHz
V_{LXTALH}	OSC32IN input pin high level voltage	—	0.7 V_{DD}	—	V_{DD}	V
V_{LXTALL}	OSC32IN input pin low level voltage	—	V_{SS}	—	0.3 V_{DD}	
$t_{H/L(LXTAL)}$	OSC32IN high or low time	—	450	—	—	ns
$t_{R/F(LXTAL)}$	OSC32IN rise or fall time	—	—	—	50	
C_{IN}	OSC32IN input capacitance	—	—	5	—	pF
$Duty_{LXTAL}$	Duty cycle	—	30	50	70	%

(1) Value guaranteed by design, not 100% tested in production.

Figure 4-3. Recommended external OSCIN and OSCOUT pins circuit for crystal

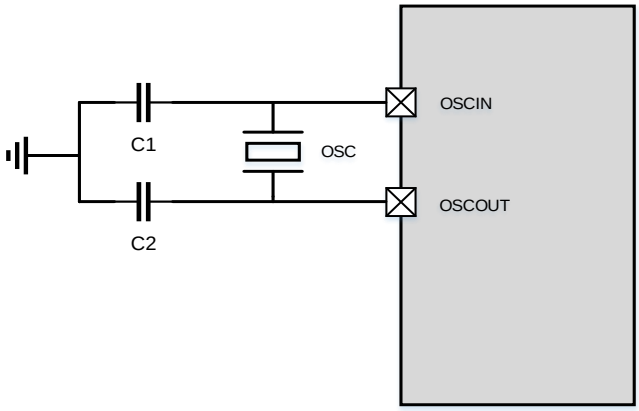
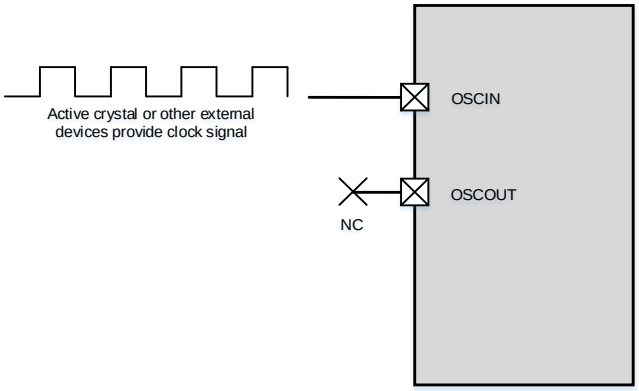


Figure 4-4. Recommended external OSCIN and OSCOUT pins circuit for oscillator



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4.7. Internal clock characteristics

Table 4-17. High speed internal clock (IRC16M) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{IRC16M}(1)	High Speed Internal Oscillator (IRC16M) frequency	V_{DD} = 3.3 V	—	16	—	MHz
$Drift_{IRC16M}$(2)	IRC16M oscillator Frequency Drift, Factory-trimmed	V_{DD} = V_{DDA} = 3.3 V, T_A = -40 °C ~ +105 °C	-4.0	—	4.0	%
		V_{DD} = V_{DDA} = 3.3 V, T_A = 25 °C	-1.0	—	1.0	%
	IRC16M oscillator Frequency accuracy, User trimming step	—	—	0.5	—	%
$Duty_{IRC16M}$(1)	IRC16M oscillator duty cycle	V_{DD} = V_{DDA} = 3.3 V	45	50	55	%
$I_{DDA(IRC16M)}$(1)	IRC16M oscillator operating current	—	—	76	—	μA
$t_{START(IRC16M)}$(2)	IRC16M oscillator startup time	—	—	1.2	—	μs

(1) Value guaranteed by design, not 100% tested in production.
(2) Value guaranteed by characterization, not 100% tested in production.

Table 4-18. High speed internal clock (IRC48M) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{IRC48M}(1)	High Speed Internal Oscillator (IRC48M) frequency	V_{DD} = 3.3 V	—	48	—	MHz
$Drift_{IRC48M}$(2)	IRC48M oscillator Frequency drift, Factory-trimmed	V_{DD} = V_{DDA} = 3.3 V, T_A = -40 °C ~ +105 °C	-4.0	—	4.0	%
		V_{DD} = V_{DDA} = 3.3 V, T_J = 25 °C	-2.0	—	2.0	%
	IRC48M oscillator Frequency accuracy, User trimming step	—	—	0.13	—	%
$Duty_{IRC48M}$(1)	IRC48M oscillator duty cycle	V_{DD} = V_{DDA} = 3.3 V	45	50	55	%
$I_{DDA(IRC48M)}$(2)	IRC48M oscillator operating current	—	—	444	—	μA
$t_{START(IRC48M)}$(2)	IRC48M oscillator startup time	—	—	1.1	—	μs

(1) Value guaranteed by design, not 100% tested in production.
(2) Value guaranteed by characterization, not 100% tested in production.

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Table 4-19. Low speed internal clock (IRC32K) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{IRC32K}	Low Speed Internal oscillator (IRC32K) frequency	V_{DD} = V_{DDA} = 3.3 V, T_A = -40 °C ~ +105 °C	20	32	45	kHz
$I_{DDA(IRC32K)}$(1)	IRC32K oscillator operating current	V_{DD} = V_{DDA} = 3.3 V	—	550	—	nA
$t_{SUIRC32K}$(1)	IRC32K oscillator startup time	—	—	20	—	μs

(1) Value guaranteed by characterization, not 100% tested in production.

4.8. PLL characteristics

Table 4-20. PLL characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLLIN}	PLL input clock frequency	After pre div	1	—	2	MHz
f_{VCO}	PLL VCO output clock frequency	—	100	—	500	MHz
t_{LOCK}	PLL lock time	—	—	—	400	μs
I_{DDA}	Current consumption on V_{DDA}	VCO freq = 500 MHz	—	600	—	μA
$Jitter_{PLL}$(2)	Cycle Jitter(rms)	VCO freq = 480 MHz	—	25	—	ps
	Cycle Jitter（peak to peak）		—	200	—	
	Cycle to cycle Jitter(rms)		—	40	—	
	Cycle to cycle Jitter（peak to peak）		—	400	—	

(1) Value guaranteed by design, not 100% tested in production.

(2) Value given with main PLL running.

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Table 4-21. PLLI2S characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLLIN}	PLLI2S input clock frequency	After pre div	1	—	2	MHz
f_{VCO}	PLLI2S VCO output clock frequency	—	100	—	500	MHz
t_{LOCK}	PLLI2S lock time	—	—	—	400	μs
I_{DDA}	Current consumption on V_{DDA}	VCO freq = 400 MHz	—	600	—	μA
$Jitter_{PLL}$(2)	Cycle Jitter(rms)	VCO freq = 480 MHz	—	25	—	ps
	Cycle Jitter（peak to peak）		—	200	—	
	Cycle to cycle Jitter(rms)		—	40	—	
	Cycle to cycle Jitter（peak to peak）		—	400	—	

(1) Value guaranteed by design, not 100% tested in production.
(2) Value given with main PLL running.

Table 4-22. PLLSAI characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLLIN}	PLLSAI input clock frequency	After pre div	1	—	2	MHz
f_{VCO}	PLLSAI VCO output clock frequency	—	100	—	500	MHz
t_{LOCK}	PLLSAI lock time	—	—	—	400	μs
I_{DDA}	Current consumption on V_{DDA}	VCO freq = 400 MHz	—	600	—	μA
$Jitter_{PLL}$(2)	Cycle Jitter(rms)	VCO freq = 480 MHz	—	25	—	ps
	Cycle Jitter（peak to peak）		—	200	—	
	Cycle to cycle Jitter(rms)		—	40	—	
	Cycle to cycle Jitter（peak to peak）		—	400	—	

(1) Value guaranteed by design, not 100% tested in production.
(2) Value given with main PLL running.

Table 4-23. PLL spread spectrum clock generation (SSCG) characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{MOD}	Modulation frequency	—	—	—	10	KHz
Mdamp	Peak modulation amplitude	—	—	—	2	%
MODCNT* MODSTEP	—	—	—	—	2^{15}-1	—

(1) Value guaranteed by design, not 100% tested in production.

Equation 1: SSCG configuration equation:

$$\mathrm{MODCNT} = \mathrm{round}(f_{PLLIN}/4/f_{mod})$$

$$\mathrm{MODSTEP} = \mathrm{round}(\mathrm{mdamp} * \mathrm{PLLN} * 2^{14}/(\mathrm{MODCNT} * 100))$$

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The formula above (*Value guaranteed* by design, not 100% tested in production.
Equation 1) is SSCG configuration equation.

4.9. Memory characteristics

Table 4-24. Flash memory characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PE_{CYC}	Number of guaranteed program /erase cycles before failure (Endurance)	T_A = -40 °C ~ +105 °C	100	—	—	kcycles
t_{RET}	Data retention time	T_A = 70 °C after up to 0 kcycle	—	20	—	years
t_{PROG}	Word programming time	T_A = -40°C ~ +105 °C	—	110	412	µs
t_{PROG_D}	Double word programming time	T_A = -40°C ~ +105 °C	—	115	532	µs
$t_{ERASE4kB}$	Page(4kB) erase time	T_A = -40°C ~ +105 °C	—	70+10	800	ms
$t_{ERASE16kB}$	Sector(16kB) erase time		—	320	3200	
$t_{ERASE64kB}$	Sector(64kB) erase time		—	300 + 100	6000	
$t_{ERASE128kB}$	Sector(128kB) erase time		—	800	12000	
$t_{ERASE256kB}$	Sector(256kB) erase time		—	1600	24000	
$t_{MERASE(7.5MB)}$	Mass erase time	T_A = -40°C ~ +105 °C	—	48	720	s

(1) Value guaranteed by design, not 100% tested in production.

4.10. NRST pin characteristics

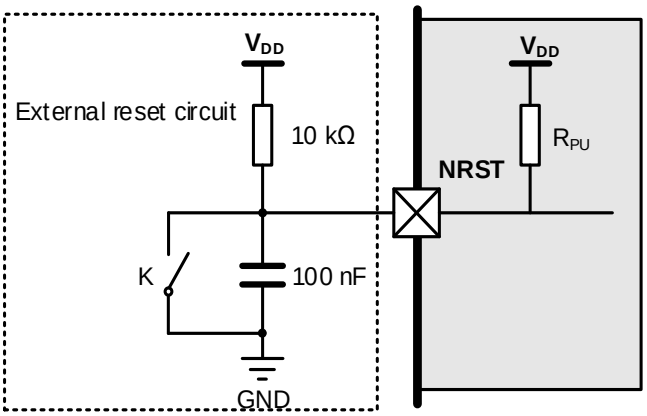
Table 4-25. NRST pin characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST Input low level voltage	V_{DD} = V_{DDA} = 1.71 V	-0.3	—	0.3 V_{DD}	V
$V_{IH(NRST)}$	NRST Input high level voltage		0.7 V_{DD}	—	V_{DD} + 0.3	
V_{hyst}	Schmidt trigger Voltage hysteresis		—	350	—	mV
$V_{IL(NRST)}$	NRST Input low level voltage	V_{DD} = V_{DDA} = 3.3 V	-0.3	—	0.3 V_{DD}	V
$V_{IH(NRST)}$	NRST Input high level voltage		0.7 V_{DD}	—	V_{DD} + 0.3	
V_{hyst}	Schmidt trigger Voltage hysteresis		—	429	—	mV
$V_{IL(NRST)}$	NRST Input low level voltage	V_{DD} = V_{DDA} = 3.6 V	-0.3	—	0.3 V_{DD}	V
$V_{IH(NRST)}$	NRST Input high level voltage		0.7 V_{DD}	—	V_{DD} + 0.3	
V_{hyst}	Schmidt trigger Voltage hysteresis		—	448	—	mV
R_{pu}	Pull-up equivalent resistor	—	—	40	—	kΩ

(1) Value guaranteed by design, not 100% tested in production.

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Figure 4-5. Recommended external NRST pin circuit



4.11. GPIO characteristics

Table 4-26. I/O port static characteristics(1)

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
V_{IL}	Standard IO Low level input voltage		1.71 V ≤ VDD = VDDA ≤ 3.6 V	-0.3	—	0.3 VDD	V
	5V-tolerant IO Low level input voltage		1.71 V ≤ VDD = VDDA ≤ 3.6 V	-0.3	—	0.3 VDD	V
V_{IH}	Standard IO High level input voltage		1.71 V ≤ VDD = VDDA ≤ 3.6 V	0.7 VDD	—	VDD + 0.3	V
	5V-tolerant IO High level input voltage		1.71 V ≤ VDD = VDDA ≤ 3.6 V	0.7 VDD	—	VDD + 3.6	V
V_{HYS}	input hysteresis		V_{DD} =3.3 V	—	490	—	mV
I_{LEAK}	Input leakage current		$V_{SS} \le V_{IN} \le V_{DD}$	-41.9	—	69.9	nA
R_{PU}	Internal pull-up resistor	All pins	—	—	40	—	kΩ
		PA10	—	—	10	—	
R_{PD}	Internal pull-down resistor	All pins	—	—	40	—	kΩ
		PA10	—	—	10	—	

(1) Value guaranteed by design, not 100% tested in production

Table 4-27. Output voltage characteristics for all I/Os except PC13, PC14, PC15(1)(2)

Speed	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
00	V_{OL}	Low level output voltage for an IO Pin (I_{IO} = +1 mA)	V_{DD} = 1.71 V	—	0.217	—	V
			V_{DD} = 3.3 V	—	0.123	—	
			V_{DD} = 3.6 V	—	0.122	—	
		Low level output voltage for an IO Pin (I_{IO} = +4 mA)	V_{DD} = 1.71 V	—	/	—	
			V_{DD} = 3.3 V	—	0.523	—	
			V_{DD} = 3.6 V	—	0.504	—	
	V_{OH}	High level output voltage for an IO Pin	V_{DD} = 1.71V	—	1.425	—	
			V_{DD} = 3.3 V	—	3.161	—	

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Speed	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		(I_{IO} = +1 mA)	V_{DD} = 3.6 V	—	3.481	—	
		High level output voltage for an IO Pin (I_{IO} = +4 mA)	V_{DD} = 1.71V	—	/	—	
			V_{DD} = 3.3 V	—	2.666	—	
			V_{DD} = 3.6 V	—	3.015	—	
01	V_{OL}	Low level output voltage for an IO Pin (I_{IO} = +8 mA)	V_{DD} = 1.71 V	—	0.395	—	V
			V_{DD} = 3.3 V	—	0.212	—	
			V_{DD} = 3.6 V	—	0.207	—	
		Low level output voltage for an IO Pin (I_{IO} = +20 mA)	V_{DD} = 1.71 V	—	/	—	
			V_{DD} = 3.3 V	—	0.557	—	
			V_{DD} = 3.6 V	—	0.541	—	
	V_{OH}	High level output voltage for an IO Pin (I_{IO} = +8 mA)	V_{DD} = 1.71 V	—	1.175	—	
			V_{DD} = 3.3 V	—	3.054	—	
			V_{DD} = 3.6 V	—	3.382	—	
		High level output voltage for an IO Pin (I_{IO} = +20 mA)	V_{DD} = 1.71 V	—	/	—	
			V_{DD} = 3.3 V	—	2.618	—	
			V_{DD} = 3.6 V	—	2.975	—	
10	V_{OL}	Low level output voltage for an IO Pin (I_{IO} = +8 mA)	V_{DD} = 1.71 V	—	0.262	—	V
			V_{DD} = 3.3 V	—	0.156	—	
			V_{DD} = 3.6 V	—	0.152	—	
		Low level output voltage for an IO Pin (I_{IO} = +20 mA)	V_{DD} = 1.71 V	—	/	—	
			V_{DD} = 3.3 V	—	0.403	—	
			V_{DD} = 3.6 V	—	0.392	—	
	V_{OH}	High level output voltage for an IO Pin (I_{IO} = +8 mA)	V_{DD} = 1.71 V	—	1.363	—	
			V_{DD} = 3.3 V	—	3.125	—	
			V_{DD} = 3.6 V	—	3.449	—	
		High level output voltage for an IO Pin (I_{IO} = +20 mA)	V_{DD} = 1.71 V	—	/	—	
			V_{DD} = 3.3 V	—	2.820	—	
			V_{DD} = 3.6 V	—	3.163	—	
11	V_{OL}	Low level output voltage for an IO Pin (I_{IO} = +8 mA)	V_{DD} = 1.71 V	—	0.166	—	V
			V_{DD} = 3.3 V	—	0.105	—	
			V_{DD} = 3.6 V	—	0.104	—	
		Low level output voltage for an IO Pin (I_{IO} = +15 mA)	V_{DD} = 1.71 V	—	0.339	—	
		Low level output voltage for an IO Pin (I_{IO} = +20 mA)	V_{DD} = 3.3 V	—	0.269	—	
			V_{DD} = 3.6 V	—	0.263	—	
	V_{OH}	High level output voltage for an IO Pin (I_{IO} = +8 mA)	V_{DD} = 1.71 V	—	1.495	—	V
			V_{DD} = 3.3 V	—	3.186	—	
			V_{DD} = 3.6 V	—	3.506	—	
		High level output voltage for an IO Pin	V_{DD} = 1.71 V	—	1.262	—	

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Speed	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		(I_{IO} = +15 mA)					
		High level output voltage for an IO Pin (I_{IO} = +20 mA)	V_{DD} = 3.3 V	—	2.987	—	
			V_{DD} = 3.6 V	—	3.315	—	

(1) Value guaranteed by characterization, not 100% tested in production.

(2) All pins except PC13 / PC14 / PC15. Since PC13 to PC15 are supplied through the Power Switch, which can only be obtained by a small current(typical source capability:3 mA shared between these IOs, but sink capability is same as other IO), the speed of GPIOs PC13 to PC15 should not exceed 2 MHz when they are in output mode(maximum load: 30 pF).

Table 4-28. I/O port AC characteristics(1)(2)(3)(4)

Speed	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
00	tr/tf	Output high to low level fall time and output low to high level rise time	1.71 V≤ VDD≤3.6 V, C_L = 10 pF	—	44.8	—	ns
			1.71 V≤ VDD≤3.6 V, C_L = 30 pF	—	60.8	—	
			1.71 V≤ VDD≤3.6 V, C_L = 50 pF	—	78.2	—	
01	tr/tf	Output high to low level fall time and output low to high level rise time	1.71 V≤ VDD≤3.6 V, C_L = 10 pF	—	4.6	—	ns
			1.71 V≤ VDD≤3.6 V, C_L = 30 pF	—	11	—	
			1.71 V≤ VDD≤3.6 V, C_L = 50 pF	—	14	—	
10	tr/tf	Output high to low level fall time and output low to high level rise time	1.71 V≤ VDD≤3.6 V, C_L = 10 pF	—	3.4	—	ns
			1.71 V≤ VDD≤3.6 V, C_L = 30 pF	—	4.6	—	
			1.71 V≤ VDD≤3.6 V, C_L = 50 pF	—	6.4	—	
11(5)	tr/tf	Output high to low level fall time and output low to high level rise time	1.71 V≤ VDD≤3.6 V, C_L = 10 pF	—	2.4	—	ns
			1.71 V≤ VDD≤3.6 V, C_L = 30 pF	—	3.4	—	
			1.71 V≤ VDD≤3.6 V, C_L = 50 pF	—	4.3	—	

(1) The maximum frequency is defined with the following conditions: (tr+tf) ≤ 2/3 T Skew ≤ 1/20 T 45%<Duty cycle<55%

(2) The fall and rise times are defined between 90% and 10% and between 10% and 90% of the output waveform, respectively.

(3) Value guaranteed by characterization, not 100% tested in production.

(4) The data is for reference only, and the specific values are related to PCB Layout.

(5) I/O port compensation active.

4.12. ADC characteristics

Table 4-29. ADC characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Operating voltage	—	1.8	3.3	3.6	V
V_{IN}	ADC input voltage range	—	0	—	V_{REFP}	V
V_{REFP}(2)	Positive Reference Voltage	V_{DDA}≥V_{REFP}	1.8	3.3	V_{DDA}	V
f_{ADC}	ADC clock	2.6 V≤V_{DDA}≤3.6 V	—	—	40	MHz

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		1.8 V≤V_{REFP}≤V_{DDA}				
		1.8 V≤V_{DDA}≤2.6 V 1.8 V≤V_{REFP}≤V_{DDA}	—	—	36	
f_S	Sampling rate	12-bit	0.15	—	2.67	MSPS
		10-bit	0.16	—	3.07	
		8-bit	0.161	—	3.63	
		6-bit	0.162	—	4.44	
V_{AIN}	Conversion voltage range	24 external; 3 internal	0	—	V_{REFP}	V
R_{AIN}	External input impedance	See ***Equation 2***	—	—	49.17	kΩ
R_{ADC}	Internal resistance	V_{DDA} ≥ 2.6V	—	—	0.55	kΩ
C_{ADC}	Input sampling capacitance	No pin/pad capacitance included	—	—	3.68	pF
t_{START}	ADC Start-up time	—	—	—	1	μs
t_{CAL}	calibration time	f_{ADC} = 40 MHz	—	14.05	56.3	1/f_{ADC}
t_s	Sampling time	f_{ADC} = 40 MHz	0.075	—	12	1/f_{ADC}
t_{CONV}	Total conversion time (including sampling time)	12-bit	—	15	—	1/ f_{ADC}
		10-bit	—	13	—	
		8-bit	—	11	—	
		6-bit	—	9	—	

(1) Value guaranteed by design, not 100% tested in production.

(2) V_{REFP} should always be equal to or less than V_{DDA}, especially during power up.

Equation 2: R_{AIN} max formula $R_{AIN} < \frac{T_s}{f_{ADC} * C_{ADC} * \ln(2^{N+2})} - R_{ADC}$

The formula above (***Equation 2***) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

Table 4-30. Internal reference voltage calibration values(1)(2)

Symbol	Test conditions	Memory address
V_{REFINT}	V_{DD} = V_{DDA} = V_{REFP} = 3.3 V (± 10mV, Temperature = 25 °C (± 5 °C)	0x1FFF 77FC - 0x1FFF 77FD

(1) V_{REFINT} is internally connected to the ADC_IN17 input channel.

(2) Value guaranteed by characterization, not 100% tested in production.

Table 4-31. ADC R_{AIN} max for f_{ADC} = 40 MHz(1)(2)

T_s (cycles)	t_s (us)	$R_{AIN\ max}$ (kΩ)
3	0.075	0.55
15	0.375	4.65
28	0.7	9.15
55	1.375	18.43

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T_s (cycles)	t_s (us)	$R_{AIN\ max}$ (kΩ)
84	2.1	28.46
112	2.8	38.1
144	3.6	49.17
480	12	N/A

(1) Value guaranteed by design, not 100% tested in production.

(2) Extra internal capacitors (such as pin capacitors, etc.) need to be considered when calculating the actual RAIN. Here we take 3.8pF for the extra internal capacitance.

Table 4-32. ADC dynamic accuracy at f_{ADC} = 36 MHz(1)(2)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ENOB	Effective number of bits	f_{ADC} = 36 MHz V_{DDA} = V_{REF+} = 1.8 V Input Frequency = 50 kHz Temperature = 25 ℃	10.4	10.65	—	bits
△ENOB(3)	Impact of Adjacent Pin Level Switching on ENOB		—	-0.1	—	
SNDR	Signal-to-noise and distortion ratio		64.5	65.8	—	dB
SNR	Signal-to-noise ratio		64.8	67	—	
THD	Total harmonic distortion		-74	-76	—	

(1) Value guaranteed by characterization, not 100% tested in production.

(2) The other pins adjacent to the pin that under test do not exhibit IO toggling during testing.

(3) PA0, PA5, and PF5 are each individually configured as ADC pins, with their corresponding adjacent level-switching pins being PA1, PA6, and PF6 respectively.

Table 4-33. ADC dynamic accuracy at f_{ADC} = 40 MHz(1)(2)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ENOB	Effective number of bits	f_{ADC} = 40 MHz V_{DDA} = V_{REF+} = 3.3 V Input Frequency = 50 kHz Temperature = 25 ℃	10.8	11	—	bits
△ENOB(3)	Impact of Adjacent Pin Level Switching on ENOB		—	-0.1	—	
SNDR	Signal-to-noise and distortion ratio		66.8	68	—	dB
SNR	Signal-to-noise ratio		66.7	68.5	—	
THD	Total harmonic distortion		-75	-78	—	

(1) Value guaranteed by characterization, not 100% tested in production.

(2) The other pins adjacent to the pin that under test do not exhibit IO toggling during testing.

(3) PA0, PA5, and PF5 are each individually configured as ADC pins, with their corresponding adjacent level-switching pins being PA1, PA6, and PF6 respectively.

Table 4-34. ADC static accuracy at f_{ADC} = 36 MHz(1)(2)

Symbol	Parameter	Test conditions	Typ	Max	Unit
Offset	Offset error	f_{ADC} = 36 MHz V_{DDA} = V_{REF+} = 1.8 V	±1.5	-	LSB
DNL	Differential linearity error		±0.9	-	
INL	Integral linearity error		±2	-	

(1) Value guaranteed by characterization, not 100% tested in production.

(2) The other pins adjacent to the pin that under test do not exhibit IO toggling during testing.

Table 4-35. ADC static accuracy at f_{ADC} = 40 MHz(1)(2)

Symbol	Parameter	Test conditions	Typ	Max	Unit
Offset	Offset error	f_{ADC} = 40 MHz V_{DDA} = V_{REF+} = 3.3 V	±1.5	—	LSB
DNL	Differential linearity error		±0.9	—	

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INL	Integral linearity error		±1.5	—	

(1) Value guaranteed by characterization, not 100% tested in production.
(2) The other pins adjacent to the pin that under test do not exhibit IO toggling during testing.

4.13. Temperature sensor characteristics

Table 4-36. Temperature sensor characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
T_L	V_{SENSE} linearity with temperature	—	±1.5	—	°C
Avg_Slope	Average slope	—	3.9	—	mV/°C
V_{25}	Voltage at 25 °C	—	1.225	—	V
t_{start}	Start time	—	10	15	µs
t_{S_temp}(2)	ADC sampling time when reading the temperature	—	17.1	—	µs

(1) Value guaranteed by characterization, not 100% tested in production.
(2) Shortest sampling time can be determined in the application by multiple iterations.

Table 4-37. Temperature sensor calibration values

Symbol	Test conditions	Memory address
TSV25	V_{DD} = V_{DDA} = V_{REFP} = 3.3 V (± 10mV, Temperature = 25 °C (± 5 °C)	0x1FFF 77F8 - 0x1FFF 77F9

4.14. DAC characteristics

Table 4-38. DAC characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Operating voltage	—		1.71	3.3	3.6	V
V_{REFP}	Positive Reference Voltage	—		1.71	—	V_{DDA}	V
V_{REFN}	Negative Reference Voltage	—		—	V_{SSA}	—	V
R_{LOAD}	Resistive load	Resistive load with buffer ON	connected to V_{SSA}	5	—	—	kΩ
			connected to V_{DDA}	5	—	—	
Ro	Impedance output	Impedance output with buffer OFF		—	—	15	kΩ
C_{LOAD}	Capacitive load	DAC output buffer ON		—	—	50	pF
V_{DAC_OUT}	Voltage on DAC_OUT output	DAC output buffer ON		0.2	—	V_{DDA}-0.2	V
		DAC output buffer OFF		0.5	—	V_{DDA}-1LSB	mV
$t_{SETTLING}$	Settling time (full scale: for a 12-bit code transition between the lowest and the highest input codes when	Normal mode, DAC output buffer ON, CL ≤ 50 pF, RL ≥ 5 kΩ	±1 LSB	—	0.6	—	µs
			±2 LSB	—	0.52	—	
			±4 LSB	—	0.51	—	
			±8 LSB	—	0.5	—	

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Symbol	Parameter	Conditions		Min	Typ	Max	Unit
	DAC_OUT reaches the final value of ±1LSB, ±2LSB, ±4LSB, ±8LSB)	Normal mode, DAC output buffer OFF, ±1LSB CL=10 pF		—	1.9	—	
t_{WAKEUP}	Wakeup time from off state (setting the ENx bit in the DAC Control register) until the final value of ±1LSB is reached	Normal mode, DAC output buffer ON, CL ≤ 50 pF, RL = 5 kΩ		—	5	10	µs
		Normal mode, DAC output buffer OFF, CL ≤ 10 pF		—	3	6	
I_{DDA}	DAC current consumption in quiescent mode	DAC output buffer ON	No load, middle code (0x800)	—	450	—	µA
			No load, worst code (0xF1C)	—	500	—	
		DAC output buffer OFF	No load, middle (0x800)	—	1.3	—	
$I_{DDVREFP}$	DAC current consumption in quiescent mode	DAC output buffer ON	No load, middle code (0x800)	—	82	—	µA
			No load, worst code (0xF1C)	—	286	—	
		DAC output buffer OFF	No load, middle code (0x800)	—	82	—	
PSRR	Power supply rejection ratio(to V_{DDA})	No R_{Load}, C_{LOAD}=50 pF		—	-90	-75	dB

(1) Value guaranteed by design, not 100% tested in production.

Table 4-39. DAC accuracy(1)

Symbol	Parameter	Test conditions		Min	Typ	Max	Unit
DNL	Differential non linearity	DAC output buffer ON	V_{REFP} = 3.6 V	—	0.93	—	LSB
			V_{REFP} = 1.71 V	—	0.83	—	
		DAC output buffer OFF	V_{REFP} = 3.6 V	—	0.91	—	
			V_{REFP} = 1.71 V	—	0.88	—	
INL	Integral non linearity	DAC output buffer ON	V_{REFP} = 3.6 V	—	2.65	—	LSB
			V_{REFP} = 1.71 V	—	2.47	—	
		DAC output buffer OFF	V_{REFP} = 3.6 V	—	1.43	—	
			V_{REFP} = 1.71 V	—	1.64	—	
Offset	Offset error	DAC output buffer ON	V_{REFP} = 3.6 V	—	0.4	—	LSB
			V_{REFP} = 1.71 V	—	-0.92	—	
		DAC output buffer	V_{REFP} = 3.6 V	—	1.25	—	

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Symbol	Parameter	Test conditions		Min	Typ	Max	Unit
		OFF	V_{REFP} = 1.71 V	—	1.24	—	
GE	Gain error	DAC output buffer ON	V_{REFP} = 3.6 V	—	-0.03	—	%
			V_{REFP} = 1.71 V	—	-0.05	—	
		DAC output buffer OFF	V_{REFP} = 3.6 V	—	-0.02	—	
			V_{REFP} = 1.71 V	—	0.004	—	

(1) Value guaranteed by characterization, not 100% tested in production.

4.15. I2C characteristics

Table 4-40. I2C characteristics(1)(2)

Symbol	Parameter	Conditions	Standard mode		Fast mode		Fast mode plus		Unit
			Min	Max	Min	Max	Min	Max	
$t_{SCL(H)}$	SCL clock high time	—	4.0	—	0.6	—	0.2	—	μs
$t_{SCL(L)}$	SCL clock low time	—	4.7	—	1.3	—	0.5	—	μs
$t_{SU(SDA)}$	SDA setup time	—	250	—	100	—	50	—	ns
$t_{H(SDA)}$	SDA data hold time	—	0(3)	3450	0	900	0	450	ns
$t_{R(SDA/SCL)}$	SDA and SCL rise time	—	—	1000	—	300	—	120	ns
$t_{F(SDA/SCL)}$	SDA and SCL fall time	—	—	300	—	300	—	120	ns
$t_{H(STA)}$	Start condition hold time	—	4.0	—	0.6	—	0.26	—	μs
$t_{SU(STA)}$	Repeated Start condition setup time	—	4.7	—	0.6	—	0.26	—	μs
$t_{SU(STO)}$	Stop condition setup time	—	4.0	—	0.6	—	0.26	—	μs
t_{BUFF}	Stop to Start condition time (bus free)	—	4.7	—	1.3	—	0.5	—	μs

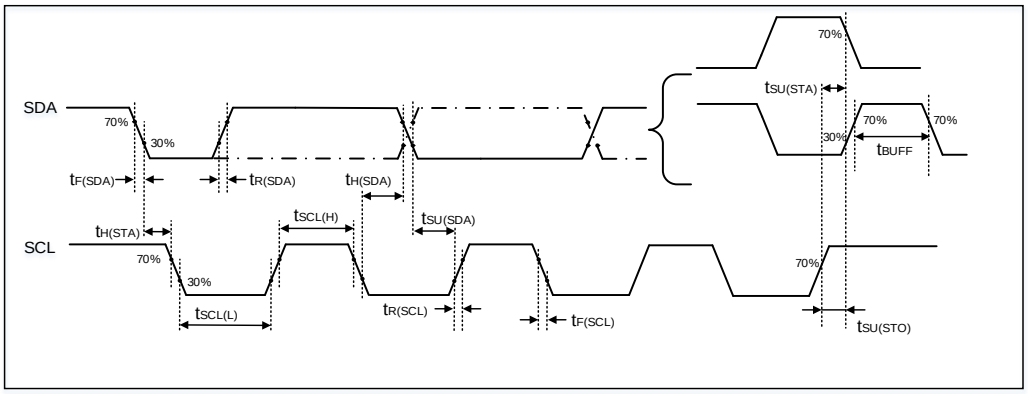
(1) Value guaranteed by design, not 100% tested in production.

(2) To ensure the standard mode I2C frequency, f_{PCLK1} must be at least 2 MHz. To ensure the fast mode I2C frequency, f_{PCLK1} must be at least 4 MHz. To ensure the fast mode plus I2C frequency, f_{PCLK1} must be at least a multiple of 10 MHz.

(3) The device should provide a data hold time of 300 ns at least in order to bridge the undefined region of the falling edge of SCL.

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Figure 4-6. I2C bus timing diagram



4.16. SPI characteristics

Table 4-41. Standard SPI characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK}(1)	SCK clock frequency	—	—	—	25	MHz
$t_{SCK(H)}$(2)	SCK clock high time	Master mode, f_{PCLKx} = 100 MHz, presc = 4	16.5	18	19	ns
$t_{SCK(L)}$(2)	SCK clock low time	Master mode, f_{PCLKx} = 100 MHz, presc = 4	16.5	18	19	ns
SPI master mode						
$t_{V(MO)}$(2)	Data output valid time	—	—	—	8	ns
$t_{SU(MI)}$(1)	Data input setup time	—	6	—	—	ns
$t_{H(MI)}$(1)	Data input hold time	—	0	—	—	ns
SPI slave mode						
$t_{SU(NSS)}$(1)	NSS enable setup time	—	0	—	—	ns
$t_{H(NSS)}$(1)	NSS enable hold time	—	3.3	—	—	ns
$t_{A(SO)}$(2)	Data output access time	—	—	5.5	—	ns
$t_{DIS(SO)}$(2)	Data output disable time	—	—	8	—	ns
$t_{V(SO)}$(2)	Data output valid time	—	—	9	—	ns
$t_{SU(SI)}$(1)	Data input setup time	—	0	—	—	ns
$t_{H(SI)}$(1)	Data input hold time	—	2.2	—	—	ns

(1) Value guaranteed by design, not 100% tested in production.

(2) Value guaranteed by characterization, not 100% tested in production.

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Figure 4-7. SPI timing diagram - master mode

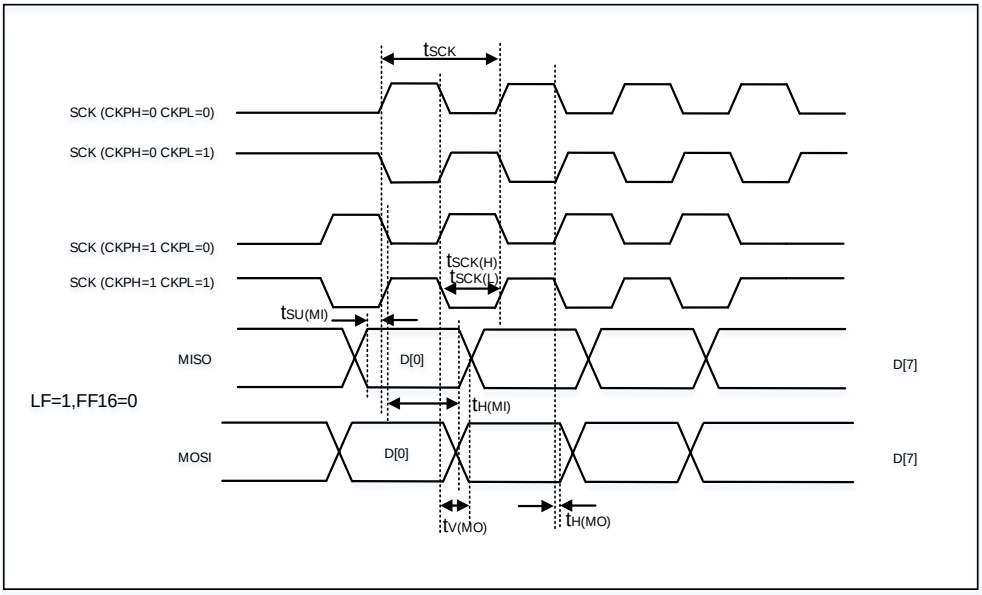
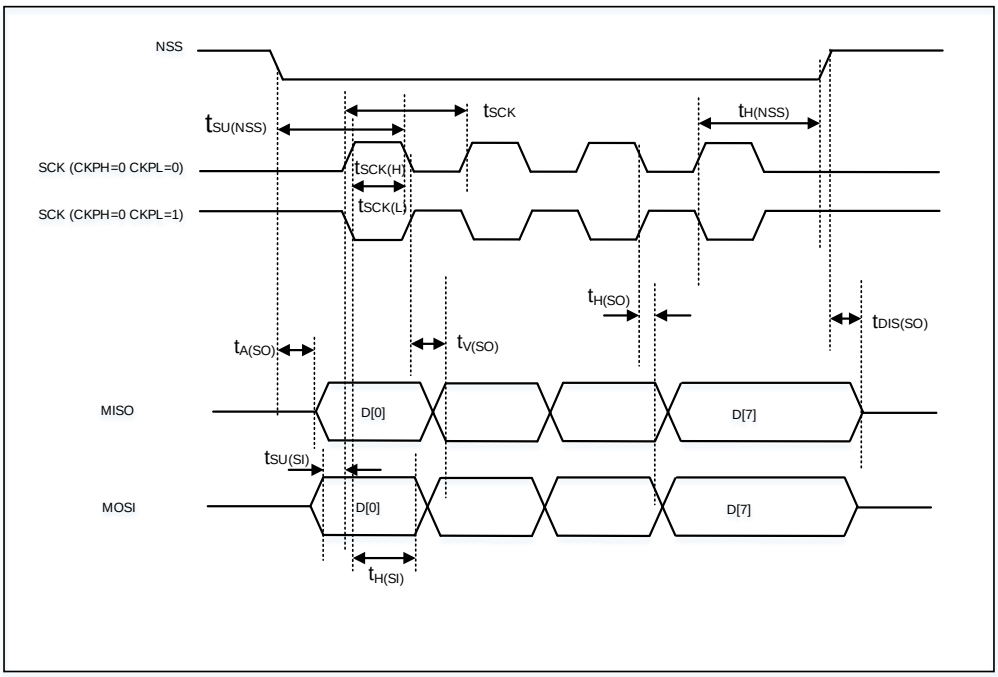


Figure 4-8. SPI timing diagram - slave mode



4.17. SAI characteristics

Table 4-42. SAI characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{MCK}	SAI Main clock output	—	—	—	50	MHz
f_{CK}	SAI clock frequency	Master transmitter, 2.7 V ≤ V_{DD} ≤ 3.6 V	—	—	45	

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		Master transmitter, 1.71 V ≤ V_{DD} ≤ 3.6 V	—	—	32	
		Master receiver, 1.71 V ≤ V_{DD} ≤ 3.6 V	—	—	32	
		Slave transmitter, 2.7 V ≤ V_{DD} ≤ 3.6 V	—	—	47.5	
		Slave transmitter, 1.71 V ≤ V_{DD} ≤ 3.6 V	—	—	41.5	
		Slave receiver, 1.71 V ≤ V_{DD} ≤ 3.6 V	—	—	50	

(1) Value guaranteed by design, not 100% tested in production.

4.18. I2S characteristics

Table 4-43. I2S characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CK} (1)	Clock frequency	Master mode (data: 32 bits, Audio frequency = 96 kHz)	—	6.25	—	MHz
		Slave mode	—	—	12.5	
t_H (2)	Clock high time	—	—	81.6	—	ns
t_L (2)	Clock low time		—	79.8	—	ns
$t_{V(WS)}$ (2)	WS valid time	Master mode	—	4.8	—	ns
$t_{H(WS)}$ (2)	WS hold time	Master mode	—	4.6	—	ns
$t_{SU(WS)}$ (1)	WS setup time	Slave mode	0	—	—	ns
$t_{H(WS)}$ (1)	WS hold time	Slave mode	3	—	—	ns
$Ducy_{(SCK)}$ (1)	I2S slave input clock duty cycle	Slave mode	—	50	—	%
$t_{SU(SD_MR)}$ (1)	Data input setup time	Master mode	0	—	—	ns
$t_{su(SD_SR)}$ (1)	Data input setup time	Slave mode	0	—	—	ns
$t_{H(SD_MR)}$ (1)	Data input hold time	Master receiver	1	—	—	ns
$t_{H(SD_SR)}$ (1)		Slave receiver	3	—	—	ns
$t_{v(SD_ST)}$ (2)	Data output valid time	Slave transmitter (after enable edge)	—	—	9.6	ns
$t_{h(SD_ST)}$ (2)	Data output hold time	Slave transmitter (after enable edge)	3.1	—	—	ns
$t_{v(SD_MT)}$ (2)	Data output valid time	Master transmitter (after enable edge)	—	—	7.4	ns
$t_{h(SD_MT)}$ (2)	Data output hold time	Master transmitter (after enable edge)	2.2	—	—	ns

(1) Value guaranteed by design, not 100% tested in production.

(2) Value guaranteed by characterization, not 100% tested in production.

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Figure 4-9. I2S timing diagram - master mode

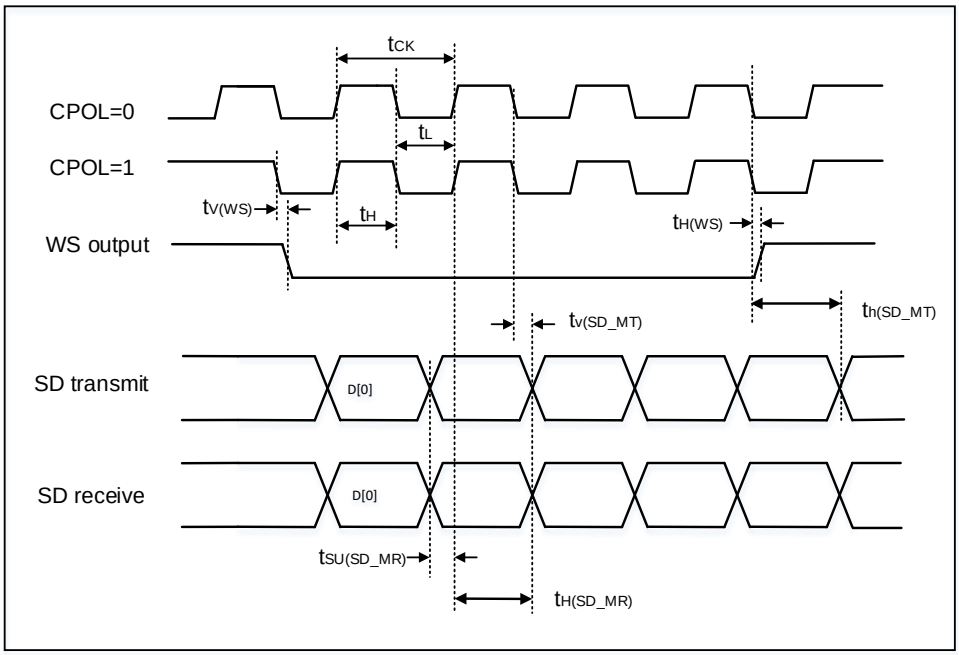
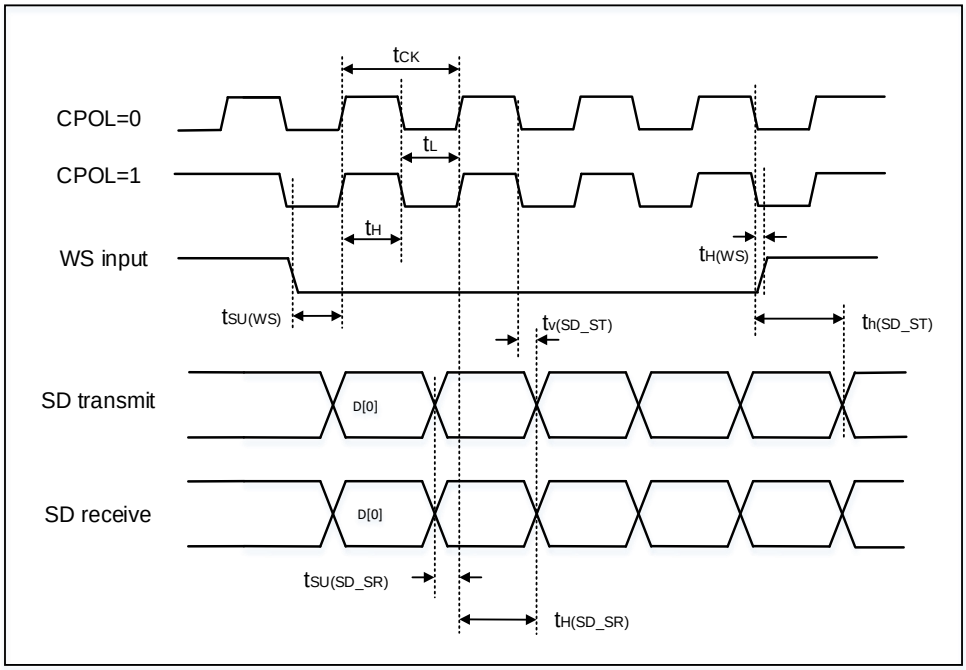


Figure 4-10. I2S timing diagram - slave mode



4.19. USART characteristics

Table 4-44. USART/UART characteristics in Synchronous mode(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency	Fplckx = 100 MHz	—	—	12.5	MHz

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{SCK(H)}$	SCK clock high time	Fplckx = 100 MHz	4.75	5.00	—	ns
$t_{SCK(L)}$	SCK clock low time	Fplckx = 100 MHz	4.75	5.00	—	ns

(1) Value guaranteed by design, not 100% tested in production.

Table 4-45. USART/UART characteristics in Smartcard mode(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency	Fplckx = 100 MHz	—	—	50	MHz
$t_{SCK(H)}$	SCK clock high time	Fplckx = 100 MHz	4.75	5.00	—	ns
$t_{SCK(L)}$	SCK clock low time	Fplckx = 100 MHz	4.75	5.00	—	ns

(1) Value guaranteed by design, not 100% tested in production.

4.20. SDIO characteristics

Table 4-46. SDIO characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP}(3)	Clock frequency in data transfer mode	—	0	—	48	MHz
$t_{W(CKL)}$ (3)	Clock low time	f_{pp} = 48 MHz	10.5	11	—	ns
$t_{W(CKH)}$ (3)	Clock high time	f_{pp} = 48 MHz	9.5	10	—	ns
CMD, D inputs (referenced to CK) in MMC and SD HS mode						
t_{ISU}(4)	Input setup time HS	f_{pp} = 48 MHz	4	—	—	ns
t_{IH}(4)	Input hold time HS	f_{pp} = 48 MHz	3	—	—	ns
CMD, D outputs (referenced to CK) in MMC and SD HS mode						
t_{OV}(3)	Output valid time HS	f_{pp} = 48 MHz	—	—	13.8	ns
t_{OH}(3)	Output hold time HS	f_{pp} = 48 MHz	12	—	—	ns
CMD, D inputs (referenced to CK) in SD default mode						
t_{ISUD}(4)	Input setup time SD	f_{pp} = 24 MHz	3	—	—	ns
t_{IHD}(4)	Input hold time SD	f_{pp} = 24 MHz	3	—	—	ns
CMD, D outputs (referenced to CK) in SD default mode						
t_{OVD}(3)	Output valid default time SD	f_{pp} = 24 MHz	—	2.4	2.8	ns
t_{OHD}(3)	Output hold default time SD	f_{pp} = 24 MHz	0.8	—	—	ns

(1) CLK timing is measured at 50% of V_{DD}.
(2) Capacitive load C_L = 30 pF.
(3) Value guaranteed by characterization, not 100% tested in production.
(4) Value guaranteed by design, not 100% tested in production.

4.21. CAN characteristics

Refer to ***Table 4-27. Output voltage characteristics for all I/Os except PC13, PC14, PC15(1)(2)*** for more details on the input/output alternate function characteristics (CANTX and CANRX).

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4.22. USBFS characteristics

Table 4-47. USBFS start up time(1)

Symbol	Parameter	Max	Unit
$t_{STARTUP}$	USBFS startup time	1	μs

(1) Value guaranteed by design, not 100% tested in production.

Table 4-48. USBFS DC electrical characteristics(1)

Symbol		Parameter	Conditions	Min	Typ	Max	Unit
Input levels	V_{DD}	USBFS operating voltage	—	3	—	3.6	V
	V_{DI}	Differential input sensitivity	—	0.2	—	—	
	V_{CM}	Differential common mode range	Includes V_{DI} range	0.8	—	2.5	
	V_{SE}	Single ended receiver threshold	—	1.3	—	2.0	
Output levels	V_{OL}	Static output level low	R_L of 1.0 kΩ to 3.6 V	—	0.06	0.3	V
	V_{OH}	Static output level high	R_L of 15 kΩ to V_{SS}	2.8	3.3	3.6	
R_{PD}		PA11, PA12(USBFS_DM/DP) PB14, PB15(USBHS_ DM/DP)	$V_{IN} = V_{DD}$	17.839	21.097	24.241	kΩ
		PA9(USBFS_VBUS) PB13(USBHS_VBUS)		0.787	0.918	1.052	
R_{PU}		PA11, PA12(USBFS_DM/DP) PB14, PB15(USBHS_ DM/DP)	$V_{IN} = V_{SS}$	1.37	1.598	1.819	
		PA9(USBFS_VBUS) PB13(USBHS_VBUS)		0.298	0.353	0.416	

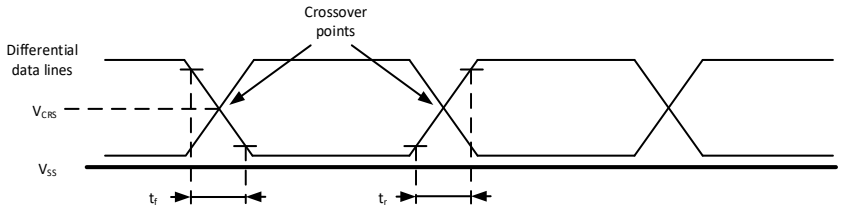
(1) Value guaranteed by design, not 100% tested in production.

Table 4-49. USBFS full speed-electrical characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_R	Rise time	C_L = 50 pF	4	—	20	ns
t_F	Fall time	C_L = 50 pF	4	—	20	ns
t_{RFM}	Rise/ fall time matching	t_R / t_F	90	—	110	%
V_{CRS}	Output signal crossover voltage	—	1.3	—	2.0	V

(1) Value guaranteed by design, not 100% tested in production.

Figure 4-11. USBFS timings: definition of data signal rise and fall time



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4.23. USBHS characteristics

Table 4-50. USBHS clock timing parameters(1)

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	USBHS operating voltage	3.0	—	3.63	V
f_{HCLK}	f_{HCLK} value to guarantee proper operation of USBHS interface	30	—	—	MHz
F_{START_8BIT}	Frequency (first transition) 8-bit ± 10%	54	60	66	MHz
F_{STEADY}	Frequency (steady state) ±500 ppm	59.97	60	60.63	MHz
D_{START_8BIT}	Duty cycle (first transition) 8-bit ± 10%	40	50	60	%
D_{STEADY}	Duty cycle (steady state) ±500 ppm	49.975	50	50.025	%

(1) Value guaranteed by design, not 100% tested in production.

Table 4-51. USB-ULPI Dynamic characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
t_{SC}	Control in (ULPI_DIR, ULPI_NXT) setup time	—	—	2	ns
t_{HC}	Control in (ULPI_DIR, ULPI_NXT) hold time	0.5	—	—	ns
t_{SD}	Data in setup time	—	—	2	ns
t_{HD}	Data in hold time	0	—	—	ns

(1) Value guaranteed by design, not 100% tested in production.

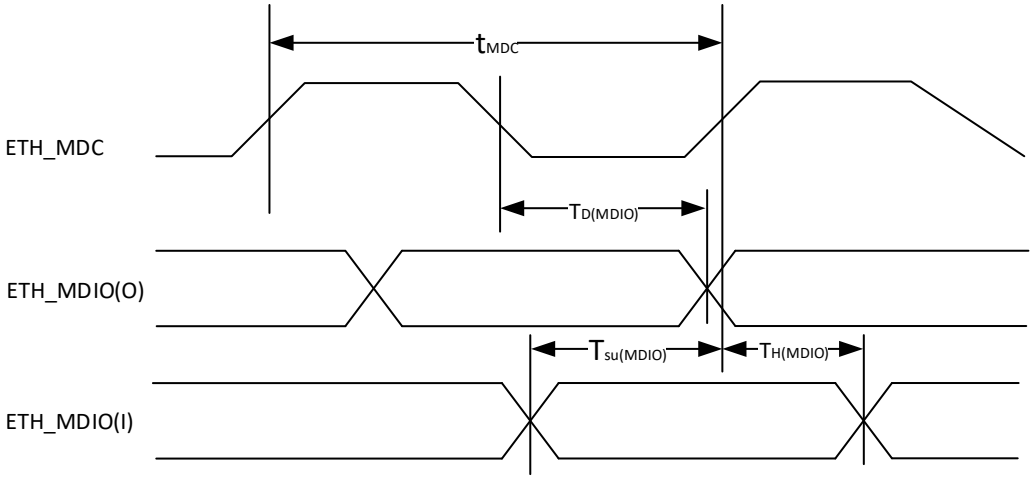
4.24. Ethernet (ENET) characteristics

Table 4-52. Dynamics characteristics: Ethernet MAC signals for SMI(1)

Symbol	Parameter	Min	Typ	Max	Unit
t_{MDC}	MDC cycle time(2.38 MHz)	411	420	425	ns
$T_{D(MDIO)}$	Write data valid delay time	1/4 tmdc	1/4 tmdc	1/4 tmdc	
$t_{SU(MDIO)}$	Read data setup time	12	—	—	
$t_{H(MDIO)}$	Read data hold time	0	—	—	

(1) Value guaranteed by design, not 100% tested in production.

Figure 4-12. Ethernet SMI timing diagram



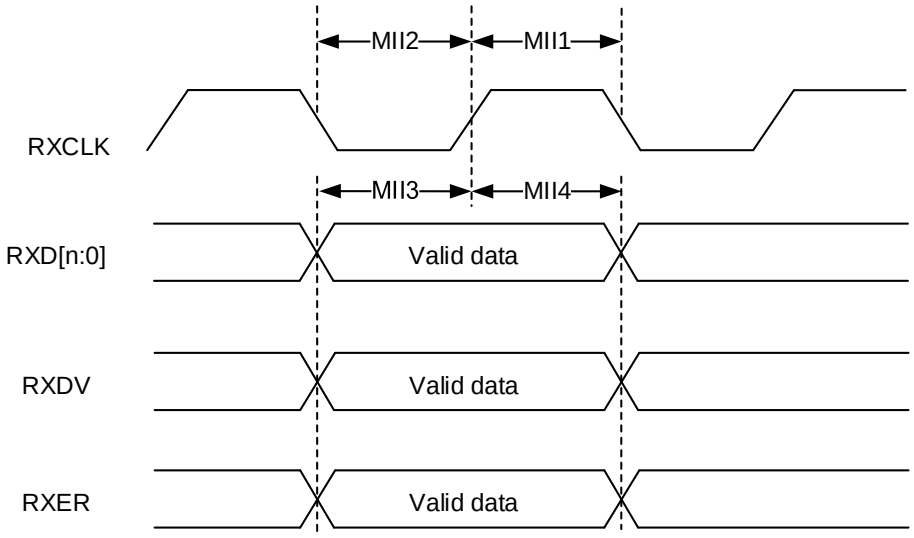
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Table 4-53. Ethernet timing for MII(1)

Symbol	Description	Min	Typ	Max	Unit
—	RXCLK frequency	—	25	—	MHz
MII1	RXCLK pulse width high	35	—	65	%RXCLK period
MII2	RXCLK pulse width low	35	—	65	%RXCLK period
MII3	RXD[3:0], RXDV, RXER to RXCLK setup	10	—	—	ns
MII4	RXCLK to RXD[3:0], RXDV, RXER hold	10	—	—	ns
t_{CYC_TX}	TXCLK frequency	—	25	—	MHz
MII5	TXCLK pulse width high	35	—	65	%TXCLK period
MII6	TXCLK pulse width low	35	—	65	%TXCLK period
MII7	TXCLK to TXD[3:0],TXEN, TXER invalid	0	—	—	ns
MII8	TXCLK to TXD[3:0], TXEN, TXER valid	—	—	25	ns

(1) Guaranteed by design, not 100% tested in production

Figure 4-13. Ethernet MII receive diagram



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Figure 4-14. Ethernet MII transmit diagram

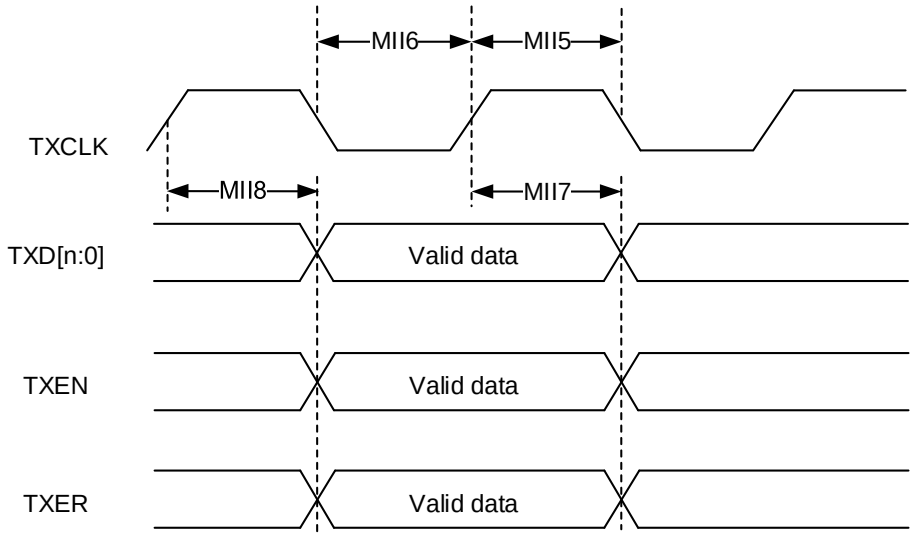
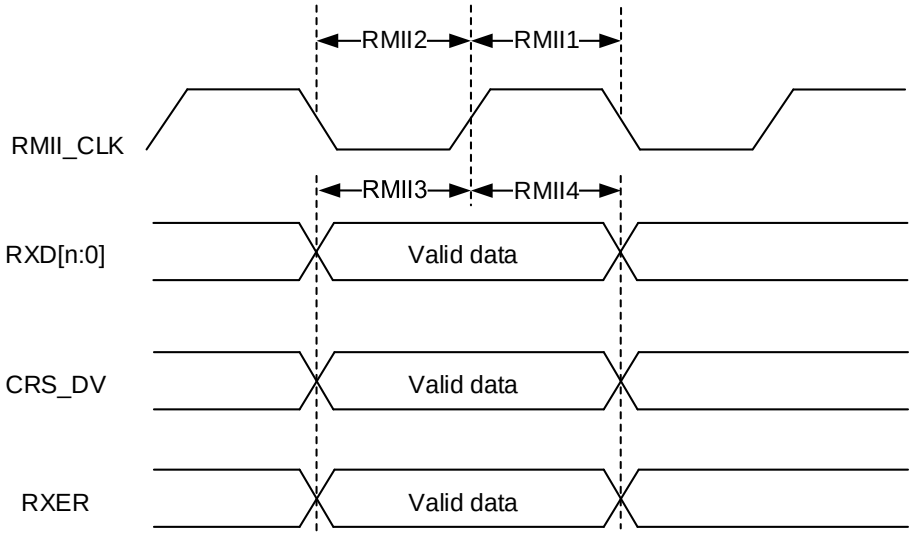


Table 4-54. Ethernet MAC timing for RMII(1)

Symbol	Description	Min	Typ	Max	Unit
—	RMII input clock frequency (RMII_CLK)	—	—	50	MHz
RMII1, RMII5	RMII_CLK pulse width high	35	—	65	%RMII_CLK period
RMII2, RMII6	RMII_CLK pulse width low	35	—	65	%RMII_CLK period
RMII3	RXD[1:0], CRS_DV, RXER to RMII_CLK setup	4	—	—	ns
RMII4	RMII_CLK to RXD[1:0], CRS_DV, RXER hold	2	—	—	ns
RMII8	RMII_CLK to TXD[1:0], TXEN data valid	—	—	14	ns
RMII7	RMII_CLK to TXD[1:0], TXEN data invalid	0	—	—	ns

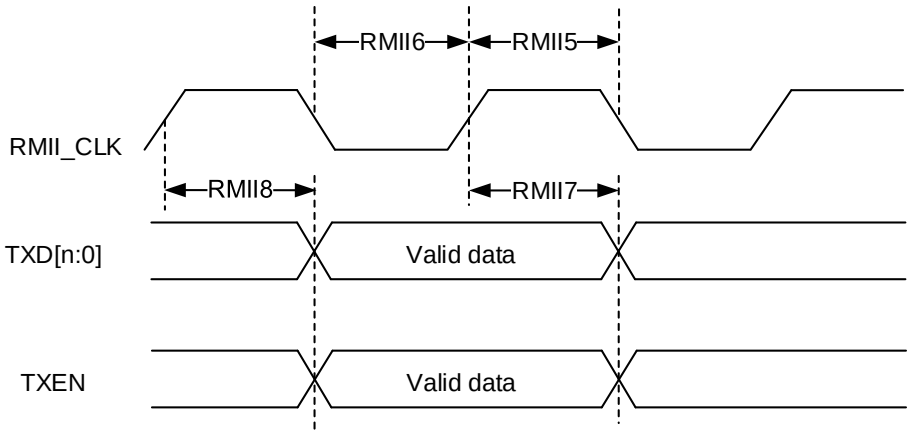
(1) Guaranteed by design, not 100% tested in production

Figure 4-15. Ethernet RMII receive diagram



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Figure 4-16. Ethernet RMII transmit diagram



4.25. EXMC characteristics

Table 4-55. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings(1)(2)(3)(4)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	EXMC_NE low time	34.7	36.7	ns
$t_{V(NOE_NE)}$	EXMC_NEx low to EXMC_NOE low	0	—	ns
$t_{w(NOE)}$	EXMC_NOE low time	34.7	36.7	ns
$t_{h(NE_NOE)}$	EXMC_NOE high to EXMC_NE high hold time	0	—	ns
$t_{v(A_NE)}$	EXMC_NEx low to EXMC_A valid	0	—	ns
$t_{v(BL_NE)}$	EXMC_NEx low to EXMC_BL valid	0	—	ns
$t_{su(DATA_NE)}$	Data to EXMC_NEx high setup time	34.7	—	ns
$t_{su(DATA_NOE)}$	Data to EXMC_NOEx high setup time	34.7	—	ns
$t_{h(DATA_NOE)}$	Data hold time after EXMC_NOE high	0	—	ns
$t_{h(DATA_NE)}$	Data hold time after EXMC_NEx high	0	—	ns
$t_{v(NADV_NE)}$	EXMC_NEx low to EXMC_NADV low	0	—	ns
$t_{w(NADV)}$	EXMC_NADV low time	5.0	7.0	ns

(1) C_L = 30 pF.

(2) Value guaranteed by design, not 100% tested in production.

(3) Based on configure: f_{HCLK} = 200 MHz, AddressSetupTime = 2, AddressHoldTime = 3, DataSetupTime = 4.

(4) In NOR non-multiplexed mode B, when AHB asynchronous split read and write memory (32-bit to 16-bit, 32-bit to 8-bit, 16-bit to 8-bit), the maximum rate is only supported up to 30 MHz.

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Table 4-56. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings(1)(2)(3)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	EXMC_NE low time	40.7	42.7	ns
$t_{V(NWE_NE)}$	EXMC_NEx low to EXMC_NWE low	5.0	—	ns
$t_{w(NWE)}$	EXMC_NWE low time	5.0	7.0	ns
$t_{h(NE_NWE)}$	EXMC_NWE high to EXMC_NE high hold time	5.0	7.0	ns
$t_{v(A_NE)}$	EXMC_NEx low to EXMC_A valid	0	—	ns
$t_{V(NADV_NE)}$	EXMC_NEx low to EXMC_NADV low	0	—	ns
$t_{w(NADV)}$	EXMC_NADV low time	5.0	7.0	ns
$t_{h(AD_NADV)}$	EXMC_AD(address) valid hold time after EXMC_NADV high	34.7	—	ns
$t_{h(A_NWE)}$	Address hold time after EXMC_NWE high	5.0	—	ns
$t_{h(BL_NWE)}$	EXMC_BL hold time after EXMC_NWE high	5.0	—	ns
$t_{v(BL_NE)}$	EXMC_NEx low to EXMC_BL valid	0	—	ns
$t_{v(DATA_NADV)}$	EXMC_NADV high to DATA valid	0	—	ns
$t_{h(DATA_NWE)}$	Data hold time after EXMC_NWE high	5.0	—	ns

(1) C_L = 30 pF.
(2) Value guaranteed by design, not 100% tested in production.
(3) Based on configure: f_{HCLK} = 200 MHz, AddressSetupTime = 2, AddressHoldTime = 3, DataSetupTime = 4.

Table 4-57. Asynchronous multiplexed PSRAM/NOR read timings(1)(2)(3)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	EXMC_NE low time	44.2	45.8	ns
$t_{V(NOE_NE)}$	EXMC_NEx low to EXMC_NOE low	25.0	—	ns
$t_{w(NOE)}$	EXMC_NOE low time	19.2	20.0	ns
$t_{h(NE_NOE)}$	EXMC_NOE high to EXMC_NE high hold time	0	—	ns
$t_{v(A_NE)}$	EXMC_NEx low to EXMC_A valid	0	—	ns
$t_{v(A_NOE)}$	Address hold time after EXMC_NOE high	0	—	ns
$t_{v(BL_NE)}$	EXMC_NEx low to EXMC_BL valid	0	—	ns
$t_{h(BL_NOE)}$	EXMC_BL hold time after EXMC_NOE high	0	—	ns
$t_{su(DATA_NE)}$	Data to EXMC_NEx high setup time	19.2	—	ns
$t_{su(DATA_NOE)}$	Data to EXMC_NOEx high setup time	19.2	—	ns
$t_{h(DATA_NOE)}$	Data hold time after EXMC_NOE high	0	—	ns
$t_{h(DATA_NE)}$	Data hold time after EXMC_NEx high	0	—	ns
$t_{v(NADV_NE)}$	EXMC_NEx low to EXMC_NADV low	0	—	ns
$t_{w(NADV)}$	EXMC_NADV low time	4.2	5.8	ns
$T_{h(AD_NADV)}$	EXMC_AD(adress) valid hold time after EXMC_NADV high	4.2	5.8	ns

(1) C_L = 30 pF.
(2) Value guaranteed by design, not 100% tested in production.
(3) Based on configure: f_{HCLK} = 200 MHz, AddressSetupTime = 2, AddressHoldTime = 3, DataSetupTime = 4.

Table 4-58. Asynchronous multiplexed PSRAM/NOR write timings(1)(2)(3)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	EXMC_NE low time	49.2	50.0	ns

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$t_{V(NWE_NE)}$	EXMC_NEx low to EXMC_NWE low	9.2	—	ns
$t_{w(NWE)}$	EXMC_NWE low time	34.2	—	ns
$t_{h(NE_NWE)}$	EXMC_NWE high to EXMC_NE high hold time	4.2	—	ns
$t_{v(A_NE)}$	EXMC_NEx low to EXMC_A valid	0	—	ns
$t_{V(NADV_NE)}$	EXMC_NEx low to EXMC_NADV low	0	—	ns
$t_{w(NADV)}$	EXMC_NADV low time	9.2	—	ns
$t_{h(AD_NADV)}$	EXMC_AD(address) valid hold time after EXMC_NADV high	14.2	—	ns
$t_{h(A_NWE)}$	Address hold time after EXMC_NWE high	9.2	—	ns
$t_{h(BL_NWE)}$	EXMC_BL hold time after EXMC_NWE high	9.2	—	ns
$t_{v(BL_NE)}$	EXMC_NEx low to EXMC_BL valid	0	—	ns
$t_{v(DATA_NADV)}$	EXMC_NADV high to DATA valid	0	—	ns
$t_{h(DATA_NWE)}$	Data hold time after EXMC_NWE high	4.2	—	ns

(1) C_L = 30 pF.
(2) Value guaranteed by design, not 100% tested in production.
(3) Based on configure: f_{HCLK} = 200 MHz, AddressSetupTime = 2, AddressHoldTime = 3, DataSetupTime = 4.

Table 4-59. Synchronous multiplexed PSRAM/NOR read timings(1)(2)(3)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	EXMC_CLK period	20.0	—	ns
$t_{d(CLKL-NExL)}$	EXMC_CLK low to EXMC_NEx low	0	—	ns
$t_{d(CLKH-NExH)}$	EXMC_CLK high to EXMC_NEx high	9.2	—	ns
$t_{d(CLKL-NADVL)}$	EXMC_CLK low to EXMC_NADV low	0	—	ns
$t_{d(CLKL-NADVH)}$	EXMC_CLK low to EXMC_NADV high	0	—	ns
$t_{d(CLKL-AV)}$	EXMC_CLK low to EXMC_Ax valid	0	—	ns
$t_{d(CLKH-AIV)}$	EXMC_CLK high to EXMC_Ax invalid	9.2	—	ns
$t_{d(CLKL-NOEL)}$	EXMC_CLK low to EXMC_NOE low	0	—	ns
$t_{d(CLKH-NOEH)}$	EXMC_CLK high to EXMC_NOE high	9.2	—	ns
$t_{d(CLKL-ADV)}$	EXMC_CLK low to EXMC_AD valid	0	—	ns
$t_{d(CLKL-ADIV)}$	EXMC_CLK low to EXMC_AD invalid	0	—	ns

(1) C_L = 30 pF.
(2) Value guaranteed by design, not 100% tested in production.
(3) Based on configure: f_{HCLK} = 200 MHz, BurstAccessMode = Enable; Memory Type = PSRAM; WriteBurst = Enable; CLKDivision = 3 (EXMC_CLK is 4 divided by HCLK); Data Latency = 1.

Table 4-60. Synchronous multiplexed PSRAM write timings(1)(2)(3)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	EXMC_CLK period	20.0	—	ns
$t_{d(CLKL-NExL)}$	EXMC_CLK low to EXMC_NEx low	0	—	ns
$t_{d(CLKH-NExH)}$	EXMC_CLK high to EXMC_NEx high	9.2	—	ns
$t_{d(CLKL-NADVL)}$	EXMC_CLK low to EXMC_NADV low	0	—	ns
$t_{d(CLKL-NADVH)}$	EXMC_CLK low to EXMC_NADV high	0	—	ns
$t_{d(CLKL-AV)}$	EXMC_CLK low to EXMC_Ax valid	0	—	ns
$t_{d(CLKH-AIV)}$	EXMC_CLK high to EXMC_Ax invalid	9.2	—	ns
$t_{d(CLKL-NWEL)}$	EXMC_CLK low to EXMC_NWE low	0	—	ns
$t_{d(CLKH-NWEH)}$	EXMC_CLK high to EXMC_NWE high	9.2	—	ns

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Symbol	Parameter	Min	Max	Unit
$t_{d(CLKL-ADIV)}$	EXMC_CLK low to EXMC_AD invalid	0	—	ns
$t_{d(CLKL-DATA)}$	EXMC_A/D valid data after EXMC_CLK low	0	—	ns
$t_{h(CLKL-NBLH)}$	EXMC_CLK low to EXMC_NBL high	0	—	ns

(1) C_L = 30 pF.
(2) Value guaranteed by design, not 100% tested in production.
(3) Based on configure: f_{HCLK} = 200 MHz, BurstAccessMode = Enable; Memory Type = PSRAM; WriteBurst = Enable; CLKDivision = 3 (EXMC_CLK is 4 divided by HCLK); Data Latency = 1.

Table 4-61. Synchronous non-multiplexed PSRAM/NOR read timings(1)(2)(3)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	EXMC_CLK period	20.0	—	ns
$t_{d(CLKL-NExL)}$	EXMC_CLK low to EXMC_NEx low	0	—	ns
$t_{d(CLKH-NExH)}$	EXMC_CLK high to EXMC_NEx high	9.2	—	ns
$t_{d(CLKL-NADVL)}$	EXMC_CLK low to EXMC_NADV low	0	—	ns
$t_{d(CLKL-NADVH)}$	EXMC_CLK low to EXMC_NADV high	0	—	ns
$t_{d(CLKL-AV)}$	EXMC_CLK low to EXMC_Ax valid	0	—	ns
$t_{d(CLKH-AIV)}$	EXMC_CLK high to EXMC_Ax invalid	9.2	—	ns
$t_{d(CLKL-NOEL)}$	EXMC_CLK low to EXMC_NOE low	0	—	ns
$t_{d(CLKH-NOEH)}$	EXMC_CLK high to EXMC_NOE high	9.2	—	ns

(1) C_L = 30 pF.
(2) Value guaranteed by design, not 100% tested in production.
(3) Based on configure: f_{HCLK} = 200 MHz, BurstAccessMode = Enable; Memory Type = PSRAM; WriteBurst = Enable; CLKDivision = 3 (EXMC_CLK is 4 divided by HCLK); Data Latency = 1.

Table 4-62. Synchronous non-multiplexed PSRAM write timings(1)(2)(3)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	EXMC_CLK period	20.0	—	ns
$t_{d(CLKL-NExL)}$	EXMC_CLK low to EXMC_NEx low	0	—	ns
$t_{d(CLKH-NExH)}$	EXMC_CLK high to EXMC_NEx high	9.2	—	ns
$t_{d(CLKL-NADVL)}$	EXMC_CLK low to EXMC_NADV low	0	—	ns
$t_{d(CLKL-NADVH)}$	EXMC_CLK low to EXMC_NADV high	0	—	ns
$t_{d(CLKL-AV)}$	EXMC_CLK low to EXMC_Ax valid	0	—	ns
$t_{d(CLKH-AIV)}$	EXMC_CLK high to EXMC_Ax invalid	9.2	—	ns
$t_{d(CLKL-NWEL)}$	EXMC_CLK low to EXMC_NWE low	0	—	ns
$t_{d(CLKH-NWEH)}$	EXMC_CLK high to EXMC_NWE high	9.2	—	ns
$t_{d(CLKL-DATA)}$	EXMC_A/D valid data after EXMC_CLK low	0	—	ns
$t_{h(CLKL-NBLH)}$	EXMC_CLK low to EXMC_NBL high	0	—	ns

(1) C_L = 30 pF.
(2) Value guaranteed by design, not 100% tested in production.
(3) Based on configure:f_{HCLK} = 200 MHz.

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Table 4-63. SDRAM read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(SDCLK)}$	EXMC_SDCLK period	9.6	10.4	ns
$t_{su(SDCLKH_Data)}$	Data input setup time	2.9	—	
$t_{h(SDCLKH_Data)}$	Data input hold time	0	—	
$t_{d(SDCLKL_Add)}$	Address valid time	—	2.1	
$t_{d(SDCLKL-SDNE)}$	Chip select valid time	—	2.1	
$t_{h(SDCLKL_SDNE)}$	Chip select hold time	0	—	
$t_{d(SDCLKL_NRAS)}$	NRAS valid time	—	1.7	
$t_{h(SDCLKL_NRAS)}$	NRAS hold time	0	—	
$t_{d(SDCLKL_NCAS)}$	NCAS valid time	—	1.7	
$t_{h(SDCLKL_NCAS)}$	NCAS hold time	0	—	

(1) Based on configure:f_{HCLK} = 200 MHz.

(2) Value guaranteed by design, not 100% tested in production.

4.26. TIMER characteristics

Table 4-64. TIMER characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
t_{RES}	Timer resolution time	—	1	—	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 200 MHz	5	—	ns
f_{EXT}	Timer external clock frequency	—	0	100	MHz
		$f_{TIMERxCLK}$ = 200 MHz	0	100	MHz
RES	Timer resolution	TIMERx（except TIMER1 & TIMER4）	—	16	bit
		TIMER1 & TIMER4	—	32	
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected	—	1	65536	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 200 MHz	0.005	327.68	μs
t_{MAX_COUNT}	Maximum possible count	—	—	65536 × 65536	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 200 MHz	—	21.4	s

(1) Value guaranteed by design, not 100% tested in production.

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4.27. DCI characteristics

Table 4-65. DCI characteristics(1)

Symbol	Parameter	Min	Max	Unit
Frequency ratio	DCI_PIXCLK /f_{HCLK}	—	0.4	%
DCI_PIXCLK	Pixel clock input	—	80	MHz
DPixel	Pixel clock input duty cycle	30	70	%
$t_{su(DATA)}$	Data input setup time	2.5	—	ns
$t_{h(DATA)}$	Data input hold time	1	—	ns
$t_{su(HSYNC)}$	DCI_HS input setup time	2	—	ns
$t_{su(VSYNC)}$	DCI_VS input setup time	2	—	ns
$t_{h(HSYNC)}$	DCI_HS input hold time	0.5	—	ns
$t_{h(VSYNC)}$	DCI_VS input hold time	0.5	—	ns

(1) Value guaranteed by design, not 100% tested in production.

4.28. WDGT characteristics

Table 4-66. FWDGT min/max timeout period at 32 kHz (IRC32K)(1)

Prescaler divider	PSC[3:0] bits	Min timeout RLD[11:0] = 0x000	Max timeout RLD[11:0] = 0xFFF	Unit
1/4	0000	0.125	511.9	ms
1/8	0001	0.25	1023.8	
1/16	0010	0.5	2047.5	
1/32	0011	1.0	4095.0	
1/64	0100	2.0	8190.0	
1/128	0101	4.0	16380.0	
1/256	0110	8.0	32760.0	
1/512	0111	16	65520.0	
1/1024	1000	32	131040.0	
1/2048	1001	64	262080.0	
1/4096	1010	128	524160.0	
1/8192	1011	256	1048320.0	
1/16384	1100	512	2096640.0	
1/32768	>=1101	1024	4193280.0	

(1) Value guaranteed by design, not 100% tested in production.

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Table 4-67. WWDGT min-max timeout value at 50 MHz (f_{PCLK1})(1)

Prescaler divider	PSC[4:0]	Min timeout value CNT[6:0] = 0x40	Unit	Max timeout value CNT[6:0] = 0x7F	Unit
1/1	00000	0.082	ms	5.243	ms
1/2	00001	0.164		10.486	
1/4	00010	0.328		20.972	
1/8	00011	0.655		41.943	
1/16	00100	1.311		83.886	
1/32	00101	2.621		167.772	
1/64	00110	5.243		335.544	
1/128	00111	10.486		671.089	
1/256	01000	20.972		1342.177	
1/512	01001	41.943		2684.355	
1/1024	01010	83.886		5368.709	
1/2048	01011	167.772		10737.418	
1/4096	01100	335.544		21474.836	
1/8192	01101	671.089		42949.673	
1/16384	01110	1342.177		85899.346	
1/32768	01111	2684.355		171798.692	
1/65536	10000	5368.709		343597.384	
1/131072	10001	10737.418		687194.767	
1/262144	10010	21474.836		1374389.535	

(1) Value guaranteed by design, not 100% tested in production.

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5. Package information

5.1. LQFP176 package outline dimensions

Figure 5-1. LQFP176 package outline

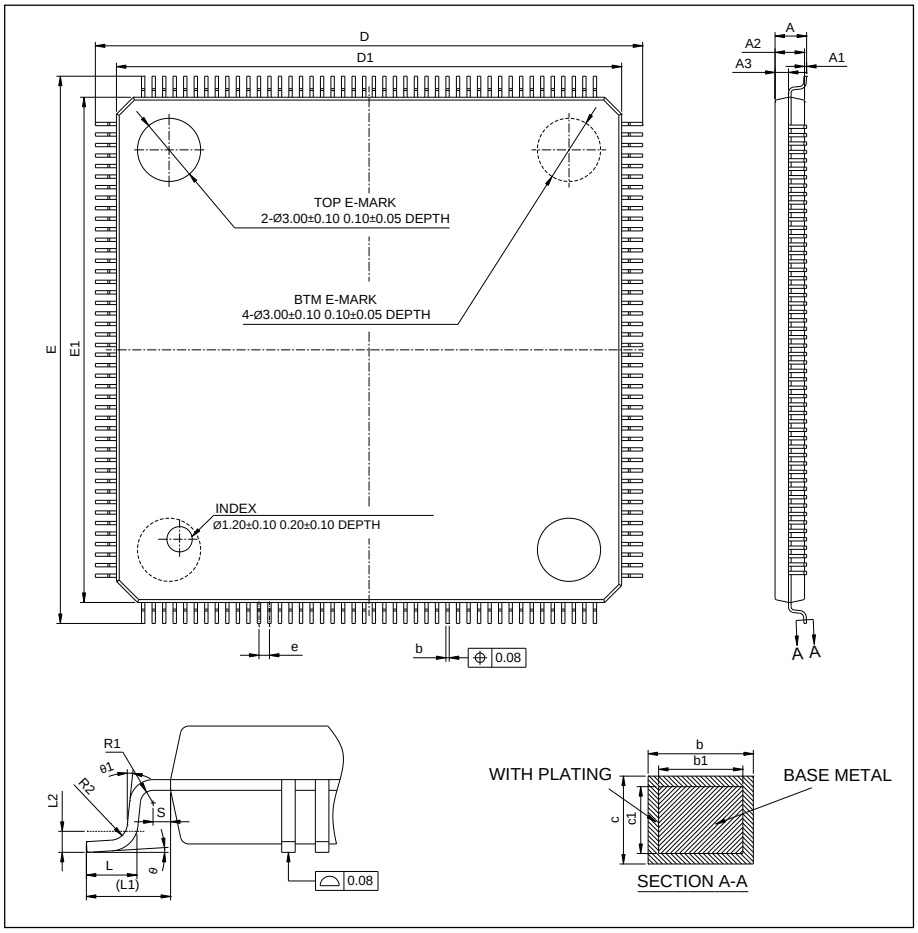


Table 5-1. LQFP176 package dimensions

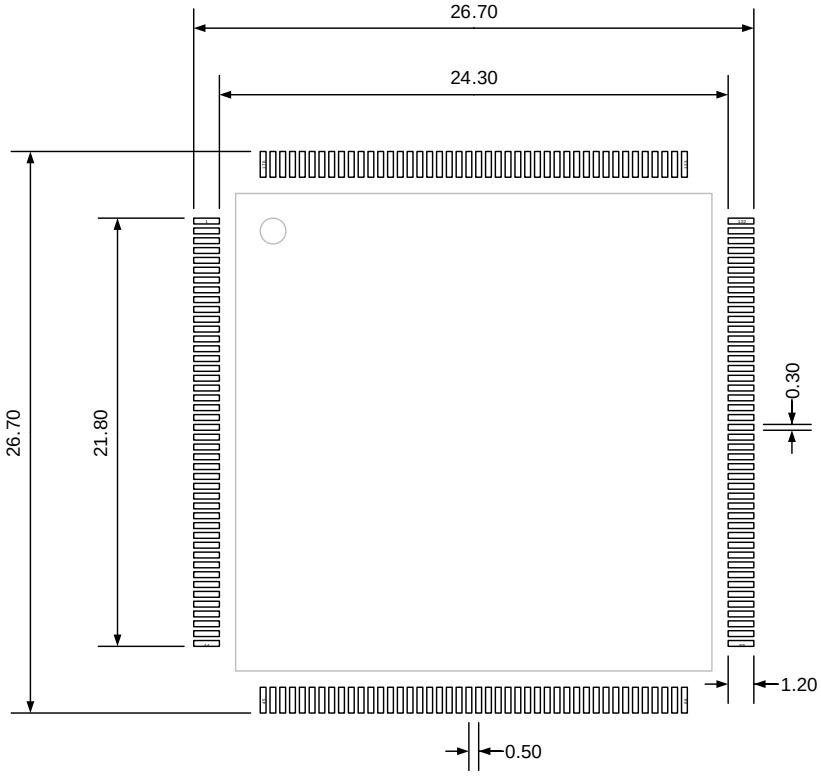
Symbol	Min	Typ	Max
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.17	—	0.27
b1	0.17	—	0.23
c	0.127	—	0.18
c1	0.119	0.127	0.135
D	25.90	26.00	26.10
D1	23.90	24.00	24.10
E	25.90	26.00	26.10
E1	23.90	24.00	24.10

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Symbol	Min	Typ	Max
e	0.45	0.50	0.55
L	0.45	0.60	0.75
L1	—	1.00	—
L2	—	0.25	—
R1	0.08	—	—
R2	0.08	—	0.20
S	0.20	—	—
θ	0°	3.5°	7°
θ1	0°	—	—

(Original dimensions are in millimeters)

Figure 5-2. LQFP176 recommended footprint



(Original dimensions are in millimeters)

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5.2. BGA176 package outline dimensions

Figure 5-3. BGA176 package outline

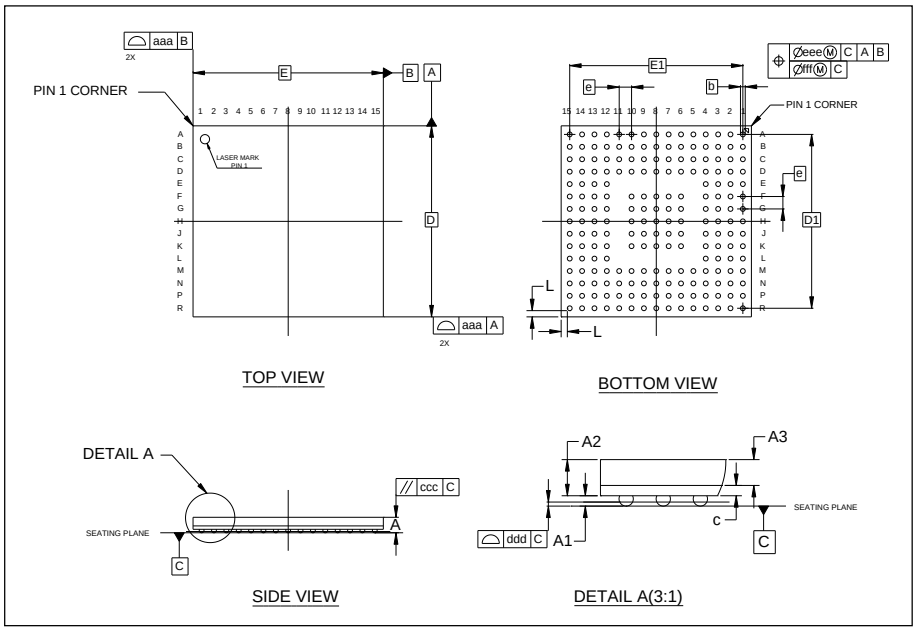


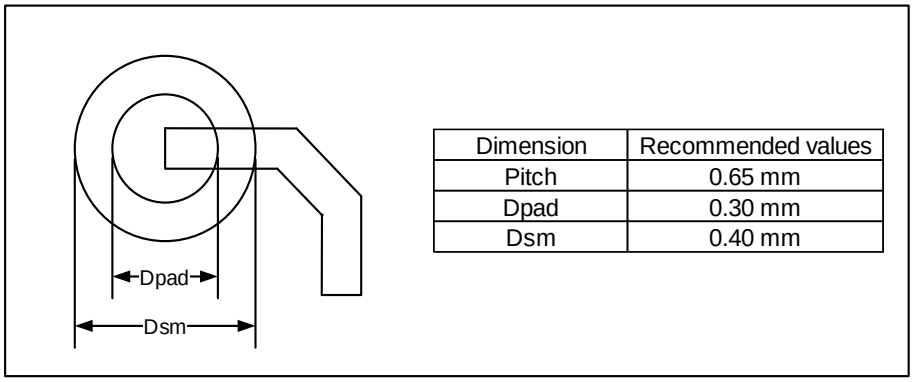
Table 5-2. BGA176 package dimensions

Symbol	Min	Typ	Max
A	—	—	0.89
A1	0.13	0.18	0.23
A2	0.58	0.63	0.68
A3	—	0.45	—
b	0.20	0.25	0.30
c	0.15	0.18	0.21
D	9.90	10.00	10.10
D1	—	9.10	—
E	9.90	10.00	10.10
E1	—	9.10	—
e	—	0.65	—
L	—	0.325	—
aaa	—	0.10	—
ccc	—	0.20	—
ddd	—	0.08	—
eee	—	0.15	—
fff	—	0.08	—

(Original dimensions are in millimeters)

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Figure 5-4. BGA176 recommended footprint



Dimension	Recommended values
Pitch	0.65 mm
Dpad	0.30 mm
Dsm	0.40 mm

(Original dimensions are in millimeters)

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5.3. LQFP144 package outline dimensions

Figure 5-5. LQFP144 package outline

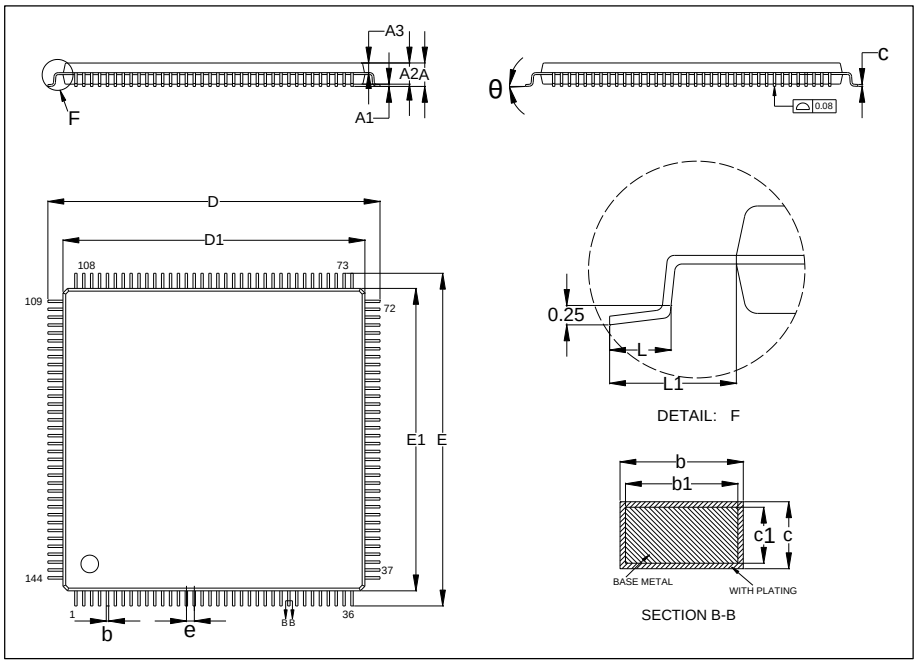


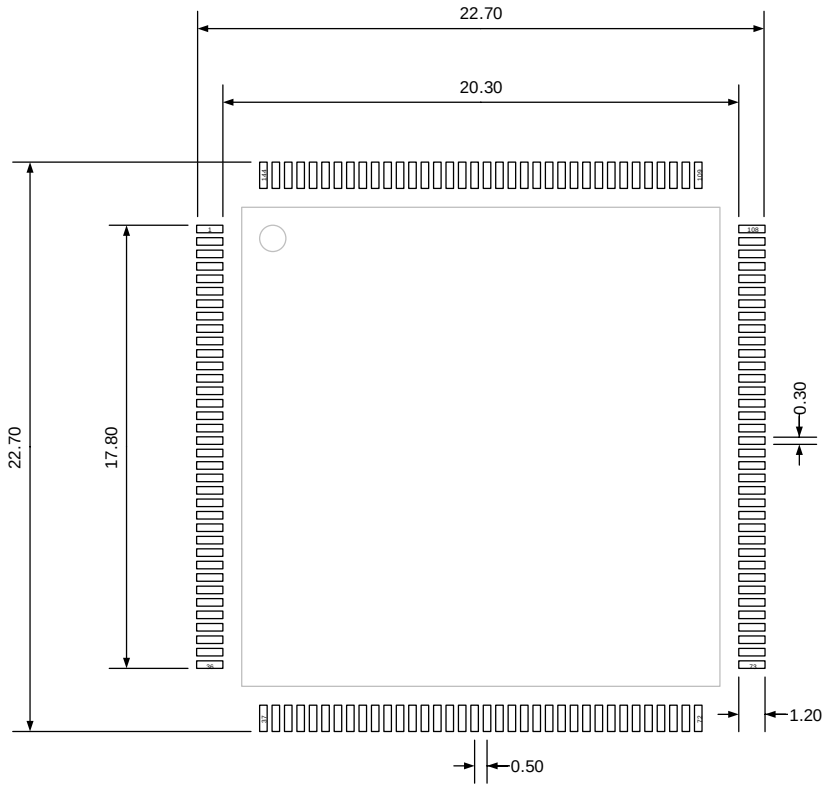
Table 5-3. LQFP144 package dimensions

Symbol	Min	Typ	Max
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	—	0.26
b1	0.17	0.20	0.23
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	21.80	22.00	22.20
D1	19.90	20.00	20.10
E	21.80	22.00	22.20
E1	19.90	20.00	20.10
e	—	0.50	—
L	0.45	—	0.75
L1	—	1.00	—
θ	0°	—	7°

(Original dimensions are in millimeters)

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Figure 5-6. LQFP144 recommended footprint



(Original dimensions are in millimeters)

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5.4. LQFP100 package outline dimensions

Figure 5-7. LQFP100 package outline

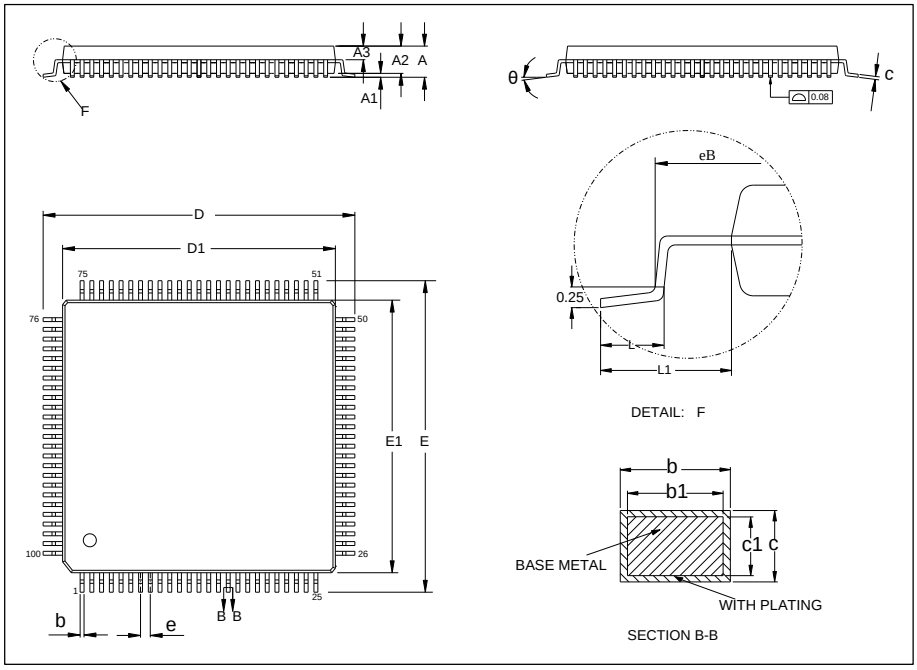


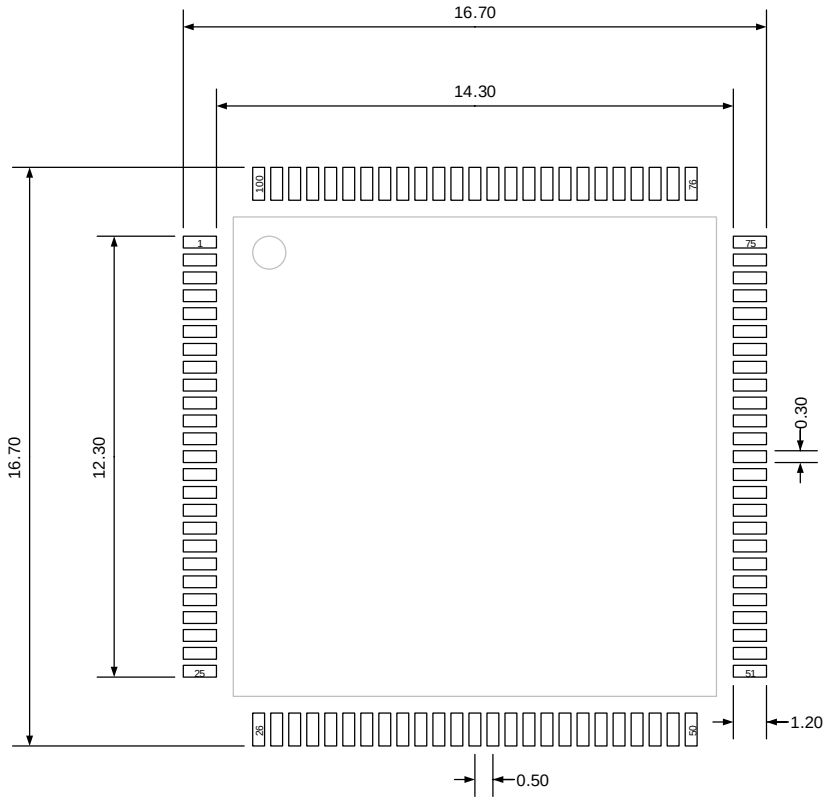
Table 5-4. LQFP100 package dimensions

Symbol	Min	Typ	Max
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	—	0.26
b1	0.17	0.20	0.23
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	15.80	16.00	16.20
D1	13.90	14.00	14.10
E	15.80	16.00	16.20
E1	13.90	14.00	14.10
e	—	0.50	—
eB	15.05	—	15.35
L	0.45	—	0.75
L1	—	1.00	—
θ	0°	—	7°

(Original dimensions are in millimeters)

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Figure 5-8. LQFP100 recommended footprint



(Original dimensions are in millimeters)

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5.5. LQFP64 package outline dimensions

Figure 5-9. LQFP64 package outline

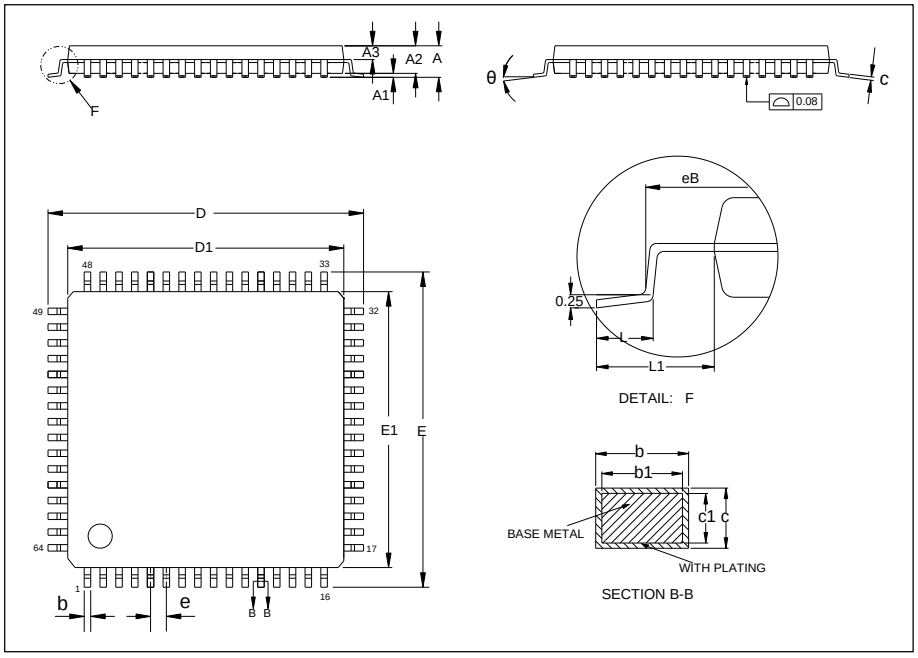


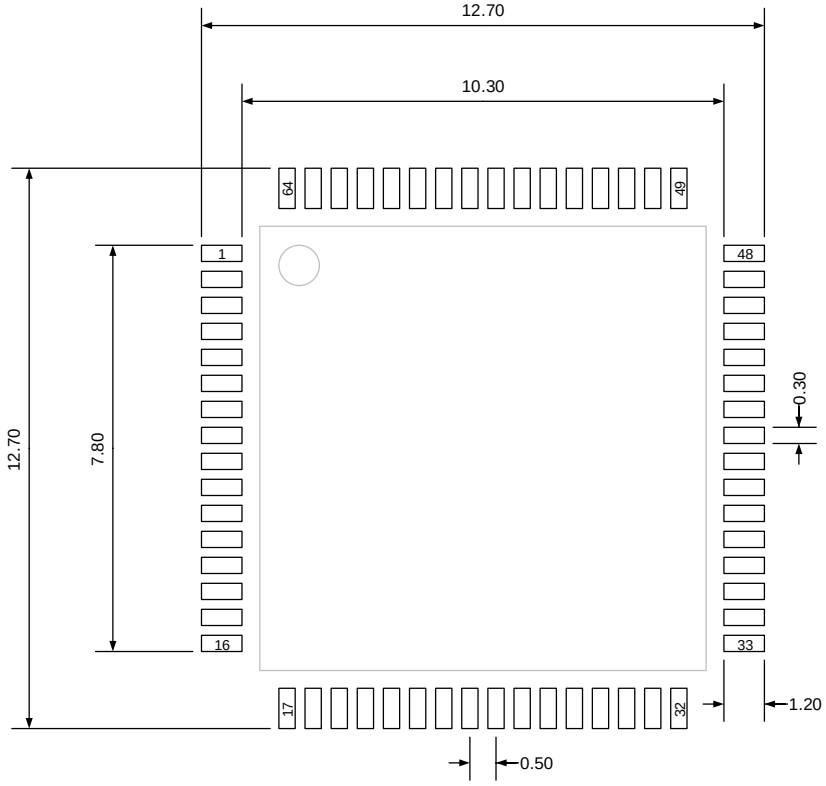
Table 5-5. LQFP64 package dimensions

Symbol	Min	Typ	Max
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	—	0.26
b1	0.17	0.20	0.23
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
E	11.80	12.00	12.20
E1	9.90	10.00	10.10
e	—	0.50	—
eB	11.25	—	11.45
L	0.45	—	0.75
L1	—	1.00	—
θ	0°	—	7°

(Original dimensions are in millimeters)

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Figure 5-10. LQFP64 recommended footprint



(Original dimensions are in millimeters)

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5.6. Thermal characteristics

Thermal resistance is used to characterize the thermal performance of the package device, which is represented by the Greek letter "θ". For semiconductor devices, thermal resistance represents the steady-state temperature rise of the chip junction due to the heat dissipated on the chip surface.

θ_{JA}: Thermal resistance, junction-to-ambient.

θ_{JB}: Thermal resistance, junction-to-board.

θ_{JC}: Thermal resistance, junction-to-case.

Ψ_{JB}: Thermal characterization parameter, junction-to-board.

Ψ_{JT}: Thermal characterization parameter, junction-to-top center.

$$\theta_{JA}=(T_J-T_A)/P_D \quad (5\text{-}1)$$

$$\theta_{JB}=(T_J-T_B)/P_D \quad (5\text{-}2)$$

$$\theta_{JC}=(T_J-T_C)/P_D \quad (5\text{-}3)$$

Where, T_J = Junction temperature.

T_A = Ambient temperature

T_B = Board temperature

T_C = Case temperature which is monitoring on package surface

P_D = Total power dissipation

θ_{JA} represents the resistance of the heat flows from the heating junction to ambient air. It is an indicator of package heat dissipation capability. Lower θ_{JA} can be considerate as better overall thermal performance. θ_{JA} is generally used to estimate junction temperature.

θ_{JB} is used to measure the heat flow resistance between the chip surface and the PCB board.

θ_{JC} represents the thermal resistance between the chip surface and the package top case. θ_{JC} is mainly used to estimate the heat dissipation of the system (using heat sink or other heat dissipation methods outside the device package).

Table 5-6. Package thermal characteristics(1)

Symbol	Condition	Package	Value	Unit
θ_{JA}	Natural convection, 2S2P PCB	LQFP176	50.13	°C/W
		BGA176	45.02	
		LQFP144	48.76	
		LQFP100	49.18	
		LQFP64	54.57	
θ_{JB}	Cold plate, 2S2P PCB	LQFP176	38.50	°C/W

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Symbol	Condition	Package	Value	Unit
		BGA176	26.55	
		LQFP144	35.00	
		LQFP100	22.70	
		LQFP64	35.08	
θ_{JC}	Cold plate, 2S2P PCB	LQFP176	7.57	°C/W
		BGA176	9.93	
		LQFP144	12.03	
		LQFP100	12.52	
		LQFP64	18.11	
Ψ_{JB}	Natural convection, 2S2P PCB	LQFP176	39.67	°C/W
		BGA176	28.31	
		LQFP144	35.32	
		LQFP100	32.85	
		LQFP64	35.41	
Ψ_{JT}	Natural convection, 2S2P PCB	LQFP176	0.64	°C/W
		BGA176	0.69	
		LQFP144	1.86	
		LQFP100	0.53	
		LQFP64	1.10	

(1): Thermal characteristics are based on simulation, and meet JEDEC specification.

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6. Ordering information

Table 6-1. Part ordering code for GD32F527xx devices

Ordering code	Flash (KB)	Package	Package type	Temperature operating range
GD32F527IST7	7680	LQFP176	Green	Industrial -40°C to +105°C
GD32F527IMT7	4096	LQFP176	Green	Industrial -40°C to +105°C
GD32F527ISK7	7680	BGA176	Green	Industrial -40°C to +105°C
GD32F527IMK7	4096	BGA176	Green	Industrial -40°C to +105°C
GD32F527ZST7	7680	LQFP144	Green	Industrial -40°C to +105°C
GD32F527ZMT7	4096	LQFP144	Green	Industrial -40°C to +105°C
GD32F527VST7	7680	LQFP100	Green	Industrial -40°C to +105°C
GD32F527VMT7	4096	LQFP100	Green	Industrial -40°C to +105°C
GD32F527RST7	7680	LQFP64	Green	Industrial -40°C to +105°C
GD32F527RMT7	4096	LQFP64	Green	Industrial -40°C to +105°C

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7. Revision history

Table 7-1. Revision history

Revision No.	Description	Date
1.0	Initial Release	Mar.1, 2024
1.1	1. Fixed a clerical error in PA4 and PA5 pin functions. 2. Add ***Table 4-36. Temperature sensor calibration values***. 3. Update the maximum and minimum values of IRC48M, IRC16M, and IRC32K clocks when TA = -40 °C ~ +105 °C.	Jul.15, 2024
1.2	1. Update the Flash schema information for GD32F527xM series in ***Table 2-1. GD32F527xx devices features and peripheral list*** and ***Table 2-2. GD32F527xx devices features and peripheral list (Cont.)***. 2. Update the ***Figure 4-2. Recommended PDR_ON pin circuit***. 3. Add typical values for high and low temperature power consumption in ***Table 4-7. Power consumption characteristics***.	Aug.3, 2024
1.3	1. Update the ***Table 6-1. Part ordering code for GD32F527xx devices***.	Oct.12, 2024
1.4	1. Update the ***Table 4-3. DC operating conditions***. 2. Update the ***Table 4-6. Power saving mode wakeup timings characteristics***. 3. Update the ***Table 4-9. EMI characteristics***. 4. Update the ***Table 4-10. Component level ESD and latch-up characteristics***. 5. Modify ***Figure 4-2. Recommended PDR_ON pin circuit*** and add note (3) to it. 6. Update the ***Table 4-18. Low speed internal clock (IRC32K) characteristics***. 7. Update the ***Table 4-19. PLL characteristics***. 8. Update the ***Table 4-20. PLLI2S characteristics***. 9. Update the ***Table 4-21. PLLSAI characteristics***. 10. Add startup time and delete Note 3 in ***Table 4-35. Temperature sensor characteristics***. 11. Update the ***Table 4-25. I/O port static characteristics***. 12. Update the ***Table 4-27. I/O port AC characteristics***. 13. Modify the maximum values of VDD, VDDA, VBAT, and VIN in ***Table 4-2. Absolute maximum ratings***. 14. Add the Max and Min values in ***Table 4-11. Power supply supervisor characteristics***. 15. Update the ***Table 4-28. ADC characteristics*** and ***Table 4-30. ADC RAIN max for fADC = 40 MHz***.	Feb.7, 2025

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Revision No.	Description	Date
	16. Updated the description of the maximum speed supported by USART/UART in ***Universal synchronous/asynchronous receiver transmitter (USART/UART)***.	
1.5	1. Updated the description of USBFS in ***Universal serial bus full-speed interface (USBFS)***. 2. Updated the description of USBHS in ***Universal serial bus high-speed interface (USBHS)***.	Feb.10, 2025
1.6	1. Update the pins PF3, PF4 and PF5 in ***Table 2-5. GD32F527Ix BGA176 pin definitions***. 2. Add the ***Table 4-5. Start-up timings of Operating conditions***. 3. Update the ***Table 4-6. Power saving mode wakeup timings characteristics***. And add the Min item.	Apr.27, 2025
1.7	1. Update the ***Table 4-2. Absolute maximum ratings***. 2. Add the ***Figure 4-13. Ethernet MII receive diagram***. 3. Delete the ***Figure 4-12. USBFS timings: definition of data signal rise and fall time***. 4. Update the ***Table 4-32*** to ***Table 4-34,*** and add notes. 5. Update the ***Table 4-41. Standard SPI characteristics***. 6. Update the ***Table 4-44. USART/UART characteristics in Synchronous mode***. 7. Update the ***Ethernet (ENET) characteristics***.	Aug.29, 2025
1.8	1. Change 1.1V domain to Vcore domain in the ***Power saving modes***. 2. Add the V_{CORE} voltage parameter in ***Table 4-3. DC operating conditions***. 3. Update the minimum and maximum values of LVD and BOR in ***Table 4-12. Power supply supervisor characteristics***, and a note 3 for the VBAT item. 4. Modify the typical and maximum values of t_{PROG} in ***Table 4-24. Flash memory characteristics***, and add a new parameter t_{PROG_D}. 5. Delete the I2S1_CK function on the PC13 pin. 6. Update the ***Table 4-38. DAC characteristics***. 7. Add a description of the actual number of pins for the BGA176 package in ***Figure 2-2. GD32F527Ix BGA176 pinouts*** and ***Table 2-5. GD32F527Ix BGA176 pin definitions***. 8. Correct the errors in pins PG6 and PG7 regarding the EXMC_INTx function. 9. Correct the errors in pins PD7 and PG9 regarding the EXMC_NCEx function. 10. Modify the conditions of the t_{RET} parameter in ***Table 4-24.***	Feb.11, 2026

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Revision No.	Description	Date
	Flash memory characteristics. 10. Delete the non-existent functions TRACECLK, TRACED0, TRACED1, TRACED2, and TRACED3 in ***Pin definitions***.	

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