GigaDevice Semiconductor Inc.

GD32F460xx
Arm® Cortex®-M4 32-bit MCU

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Datasheet

Revision 1.2

(Apr. 2025)

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1. General description

The GD32F460xx device belongs to the stretch performance line of GD32 MCU family. It is a new 32-bit general-purpose microcontroller based on the Arm® Cortex®-M4 RISC core with best cost-performance ratio in terms of enhanced processing capacity, reduced power consumption and peripheral set. The Cortex®-M4 core features a Floating Point Unit (FPU) that accelerates single precision floating point math operations and supports all Arm® single precision instructions and data types. It implements a full set of DSP instructions to address digital signal control markets that demand an efficient, easy-to-use blend of control and signal processing capabilities. It also provides a Memory Protection Unit (MPU) and powerful trace technology for enhanced application security and advanced debug support.

The GD32F460xx device incorporates the Arm® Cortex®-M4 32-bit processor core operating at 240 MHz frequency with Flash accesses zero wait states to obtain maximum efficiency. It provides up to 2048 KB on-chip Flash memory and 768 KB SRAM memory. An extensive range of enhanced I/Os and peripherals connected to two APB buses. The devices offer up to three 12-bit 2.6 MSPS ADCs, two 12-bit DACs, up to eight general 16-bit timers, two 16-bit PWM advanced timers, two 32-bit general timers, and two 16-bit basic timers, as well as standard and advanced communication interfaces: up to five SPIs, three I2Cs, four USARTs and four UARTs, two I2Ss, two CANs, a SDIO, USBFS and USBHS, and an ENET. Additional peripherals as Digital camera interface (DCI), EXMC, TFT-LCD Interface (TLI) and Image Processing Accelerator (IPA) are included.

The device operates from a 2.6 to 3.6V power supply and available in -40 to 105 °C temperature range for grade 7 devices. Three power saving modes provide the flexibility for maximum optimization of power consumption, an especially important consideration in low power applications.

The above features make GD32F460xx devices suitable for a wide range of interconnection and advanced applications, especially in areas such as industrial control, consumer and handheld equipment, embedded modules, human machine interface, security and alarm systems, graphic display, automotive navigation, drone, IoT and so on.

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2. Device overview

2.1. Device information

Table 2-1. GD32F460xx devices features and peripheral list

Part Number		GD32F460VGT7	GD32F460VIT7	GD32F460RGT7
Flash	Code area (KB)	768	512	768
	Data area (KB)	256	1536	256
	Total (KB)	1024	2048	1024
SRAM (KB)		512	768	512
Timers	General timer(16-bit)	8 (2-3,8-13)	8 (2-3,8-13)	8 (2-3,8-13)
	General timer(32-bit)	2 (1,4)	2 (1,4)	2 (1,4)
	Advanced timer(16-bit)	2 (0,7)	2 (0,7)	2 (0,7)
	Basic timer(16-bit)	2 (5,6)	2 (5,6)	2 (5,6)
	SysTick	1	1	1
	Watchdog	2	2	2
	RTC	1	1	1
Connectivity	USART	4 (0,1,2,5)	4 (0,1,2,5)	4 (0,1,2,5)
	UART	4 (3,4,6,7)	4 (3,4,6,7)	2 (3,4)
	I2C	3	3	3
	SPI/I2S	5/2 (0-4)/(1-2)	5/2 (0-4)/(1-2)	3/2 (0-2)/(1-2)
	SDIO	1	1	1
	CAN	2	2	2
	USB	FS+HS	FS+HS	FS+HS
	ENET	1	1	1

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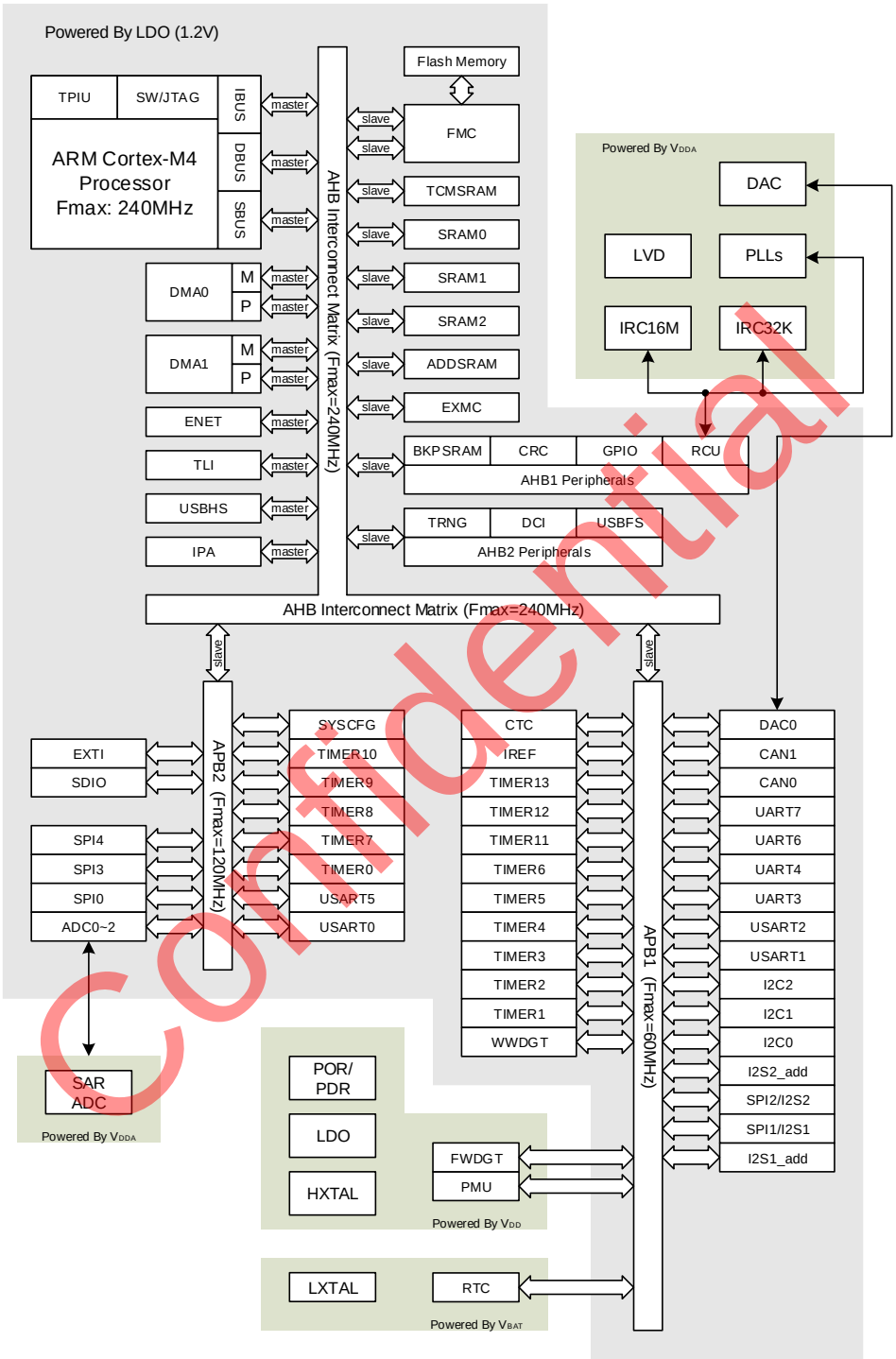
Part Number		GD32F460VGT7	GD32F460VIT7	GD32F460RGT7
	TLI	1	1	0
	DCI	1	1	1
GPIO		82	82	51
EXMC/SDRAM		1/0	1/0	0/0
ADC(CHs)		3(16)	3(16)	3(16)
DAC	Units	1	1	1
	Channels	2	2	2
Package		LQFP100	LQFP100	LQFP64

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2.2. Block diagram

Figure 2-1. GD32F460xx block diagram

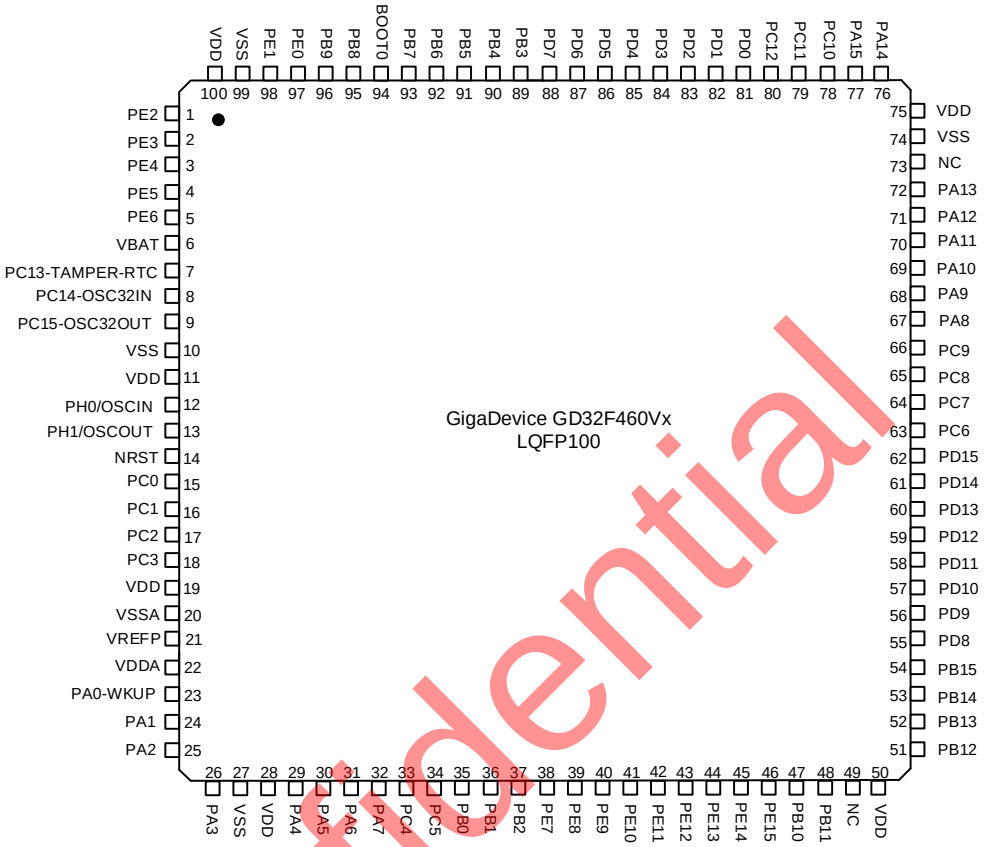


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2.3. Pinouts and pin assignment

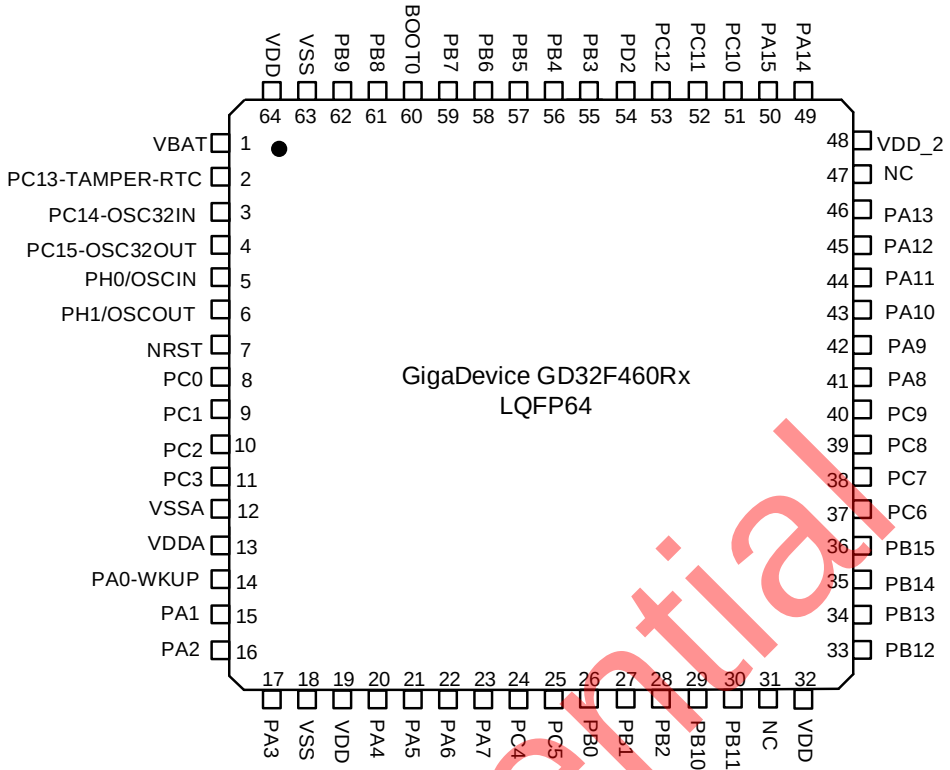
Figure 2-2. GD32F460Vx LQFP100 pinouts



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Figure 2-3. GD32F460Rx LQFP64 pinouts



2.4. Memory map

Table 2-2. GD32F460xx memory map

Pre-defined Regions	Bus	Address	Peripherals
External Device	AHB	0xA000 1000 - 0xBFFF FFFF	Reserved
		0xA000 0000 - 0xA000 0FFF	EXMC - SWREG
External RAM		0x9000 0000 - 0x9FFF FFFF	EXMC - PC CARD
		0x7000 0000 - 0x8FFF FFFF	EXMC - NAND
		0x6000 0000 - 0x6FFF FFFF	EXMC - NOR/PSRAM/SRAM
Peripheral	AHB2	0x5006 0C00 - 0x5FFF FFFF	Reserved
		0x5006 0800 - 0x5006 0BFF	TRNG
		0x5005 0400 - 0x5006 07FF	Reserved
		0x5005 0000 - 0x5005 03FF	DCI
		0x5004 0000 - 0x5004 FFFF	Reserved
		0x5000 0000 - 0x5003 FFFF	USBFS
	AHB1	0x4008 0000 - 0x4FFF FFFF	Reserved
		0x4004 0000 - 0x4007 FFFF	USBHS
		0x4002 BC00 - 0x4003 FFFF	Reserved
		0x4002 B000 - 0x4002 BBFF	IPA
		0x4002 A000 - 0x4002 AFFF	Reserved

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Pre-defined Regions	Bus	Address	Peripherals
		0x4002 8000 - 0x4002 9FFF	ENET
		0x4002 6800 - 0x4002 7FFF	Reserved
		0x4002 6400 - 0x4002 67FF	DMA1
		0x4002 6000 - 0x4002 63FF	DMA0
		0x4002 5000 - 0x4002 5FFF	Reserved
		0x4002 4000 - 0x4002 4FFF	BKP SRAM
		0x4002 3C00 - 0x4002 3FFF	FMC
		0x4002 3800 - 0x4002 3BFF	RCU
		0x4002 3400 - 0x4002 37FF	Reserved
		0x4002 3000 - 0x4002 33FF	CRC
		0x4002 2400 - 0x4002 2FFF	Reserved
		0x4002 2000 - 0x4002 23FF	GPIOI
		0x4002 1C00 - 0x4002 1FFF	GPIOH
		0x4002 1800 - 0x4002 1BFF	GPIOG
		0x4002 1400 - 0x4002 17FF	GPIOF
		0x4002 1000 - 0x4002 13FF	GPIOE
		0x4002 0C00 - 0x4002 0FFF	GPIOD
		0x4002 0800 - 0x4002 0BFF	GPIOC
		0x4002 0400 - 0x4002 07FF	GPIOB
		0x4002 0000 - 0x4002 03FF	GPIOA
	APB2	0x4001 6C00 - 0x4001 FFFF	Reserved
		0x4001 6800 - 0x4001 6BFF	TLI
		0x4001 5800 - 0x4001 67FF	Reserved
		0x4001 5400 - 0x4001 57FF	SPI5
		0x4001 5000 - 0x4001 53FF	SPI4
		0x4001 4C00 - 0x4001 4FFF	Reserved
		0x4001 4800 - 0x4001 4BFF	TIMER10
		0x4001 4400 - 0x4001 47FF	TIMER9
		0x4001 4000 - 0x4001 43FF	TIMER8
		0x4001 3C00 - 0x4001 3FFF	EXTI
		0x4001 3800 - 0x4001 3BFF	SYSCFG
		0x4001 3400 - 0x4001 37FF	SPI3
		0x4001 3000 - 0x4001 33FF	SPI0
		0x4001 2C00 - 0x4001 2FFF	SDIO
		0x4001 2400 - 0x4001 2BFF	Reserved
		0x4001 2300 - 0x4001 23FF	ADC0(1)
		0x4001 2200 - 0x4001 22FF	ADC2
		0x4001 2100 - 0x4001 21FF	ADC1
		0x4001 2000 - 0x4001 20FF	ADC0
		0x4001 1800 - 0x4001 1FFF	Reserved
		0x4001 1400 - 0x4001 17FF	USART5

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Pre-defined Regions	Bus	Address	Peripherals
		0x4001 1000 - 0x4001 13FF	USART0
		0x4001 0800 - 0x4001 0FFF	Reserved
		0x4001 0400 - 0x4001 07FF	TIMER7
		0x4001 0000 - 0x4001 03FF	TIMER0
	APB1	0x4000 C800 - 0x4000 FFFF	Reserved
		0x4000 C400 - 0x4000 C7FF	IREF
		0x4000 8000 - 0x4000 C3FF	Reserved
		0x4000 7C00 - 0x4000 7FFF	UART7
		0x4000 7800 - 0x4000 7BFF	UART6
		0x4000 7400 - 0x4000 77FF	DAC0
		0x4000 7000 - 0x4000 73FF	PMU
		0x4000 6C00 - 0x4000 6FFF	CTC
		0x4000 6800 - 0x4000 6BFF	CAN1
		0x4000 6400 - 0x4000 67FF	CAN0
		0x4000 6000 - 0x4000 63FF	Reserved
		0x4000 5C00 - 0x4000 5FFF	I2C2
		0x4000 5800 - 0x4000 5BFF	I2C1
		0x4000 5400 - 0x4000 57FF	I2C0
		0x4000 5000 - 0x4000 53FF	UART4
		0x4000 4C00 - 0x4000 4FFF	UART3
		0x4000 4800 - 0x4000 4BFF	USART2
		0x4000 4400 - 0x4000 47FF	USART1
		0x4000 4000 - 0x4000 43FF	I2S2_add
		0x4000 3C00 - 0x4000 3FFF	SPI2/I2S2
		0x4000 3800 - 0x4000 3BFF	SPI1/I2S1
		0x4000 3400 - 0x4000 37FF	I2S1_add
		0x4000 3000 - 0x4000 33FF	FWDGT
		0x4000 2C00 - 0x4000 2FFF	WWDGT
		0x4000 2800 - 0x4000 2BFF	RTC
		0x4000 2400 - 0x4000 27FF	Reserved
		0x4000 2000 - 0x4000 23FF	TIMER13
		0x4000 1C00 - 0x4000 1FFF	TIMER12
		0x4000 1800 - 0x4000 1BFF	TIMER11
		0x4000 1400 - 0x4000 17FF	TIMER6
		0x4000 1000 - 0x4000 13FF	TIMER5
		0x4000 0C00 - 0x4000 0FFF	TIMER4
		0x4000 0800 - 0x4000 0BFF	TIMER3
		0x4000 0400 - 0x4000 07FF	TIMER2
		0x4000 0000 - 0x4000 03FF	TIMER1
SRAM	AHB	0x200B 0000 - 0x3FFF FFFF	Reserved
		0x2003 0000 - 0x200A FFFF	ADDSRAM(512KB)

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Pre-defined Regions	Bus	Address	Peripherals
		0x2002 0000 - 0x2002 FFFF	SRAM2(64KB)
		0x2001 C000 - 0x2001 FFFF	SRAM1(16KB)
		0x2000 0000 - 0x2001 BFFF	SRAM0(112KB)
Code	AHB	0x1FFF C010 - 0x1FFF FFFF	Reserved
		0x1FFF C000 - 0x1FFF C00F	Option bytes(Bank 0)
		0x1FFF 7A10 - 0x1FFF BFFF	Reserved
		0x1FFF 7800 - 0x1FFF 7A0F	OTP(512B)
		0x1FFF 0000 - 0x1FFF 77FF	Boot loader(30KB)
		0x1FFE C010 - 0x1FFE FFFF	Reserved
		0x1FFE C000 - 0x1FFE C00F	Option bytes(Bank 1)
		0x1001 0000 - 0x1FFE BFFF	Reserved
		0x1000 0000 - 0x1000 FFFF	TCMSRAM(64KB)
		0x0820 0000 - 0x0FFF FFFF	Reserved
		0x0800 0000 - 0x081F FFFF	Main Flash(2048KB)
		0x0000 0000 - 0x07FF FFFF	Aliased to the boot device

Note:

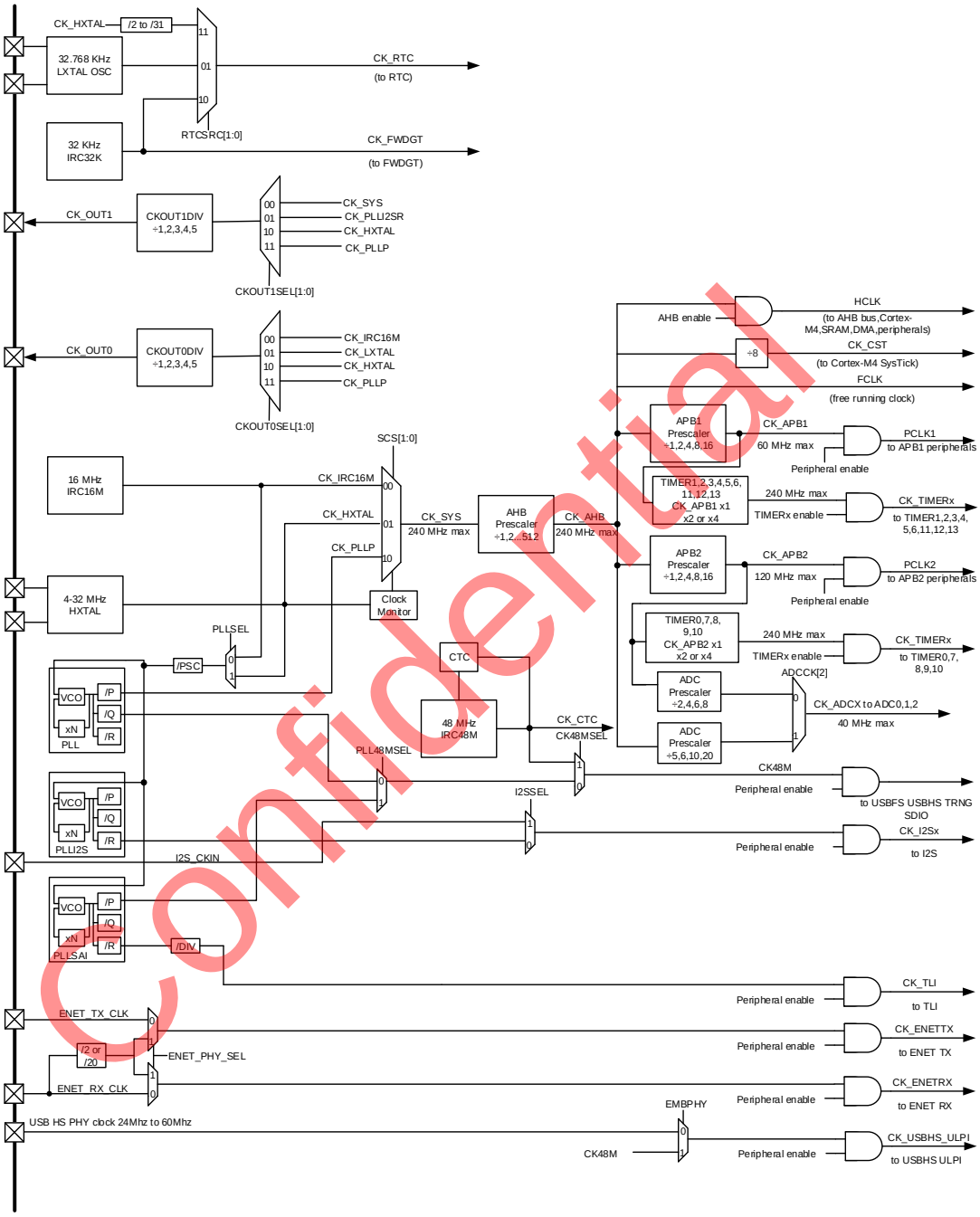
(1) ADC_SSTAT, ADC_SYNCCTL, ADC_SYNCDATA based on base address of ADC0.

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2.5. Clock tree

Figure 2-4. GD32F460xx clock tree



Legend:

HXTAL: High speed crystal oscillator

LXTAL: Low speed crystal oscillator

IRC16M: Internal 16M RC oscillators

IRC32K: Internal 32K RC oscillator

IRC48M: Internal 48M RC oscillators

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2.6. Pin definitions

2.6.1. GD32F460Vx LQFP100 pin definitions

Table 2-3. GD32F460Vx LQFP100 pin definitions

GD32F460Vx LQFP64				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PE2	1	I/O	5VT	Default: PE2 Alternate: SPI3_SCK, ENET_MII_TXD3, EXMC_A23, EVENTOUT
PE3	2	I/O	5VT	Default: PE3 Alternate: EXMC_A19, EVENTOUT
PE4	3	I/O	5VT	Default: PE4 Alternate: SPI3_NSS, EXMC_A20, DCI_D4, TLI_B0, EVENTOUT
PE5	4	I/O	5VT	Default: PE5 Alternate: TIMER8_CH0, SPI3_MISO, EXMC_A21, DCI_D6, TLI_G0, EVENTOUT
PE6	5	I/O	5VT	Default: PE6 Alternate: TIMER8_CH1, SPI3_MOSI, EXMC_A22, DCI_D7, TLI_G1, EVENTOUT
VBAT	6	P	-	Default: VBAT
PC13-TAMPER-RTC	7	I/O	5VT	Default: PC13 Alternate: EVENTOUT Additional: RTC_TAMP0, RTC_OUT, RTC_TS
PC14-OSC32IN	8	I/O	5VT	Default: PC14 Alternate: EVENTOUT Additional: OSC32IN
PC15-OSC32OUT	9	I/O	5VT	Default: PC15 Alternate: EVENTOUT Additional: OSC32OUT
VSS	10	P	-	Default: VSS
VDD	11	P	-	Default: VDD
PH0/OSCIN	12	I/O	5VT	Default: PH0, OSCIN Alternate: EVENTOUT Additional: OSCIN
PH1/OSCOUT	13	I/O	5VT	Default: PH1, OSCOUT Alternate: EVENTOUT Additional: OSCOUT
NRST	14	-	-	Default: NRST
PC0	15	I/O	5VT	Default: PC0 Alternate: USBHS_ULPI_STP, EVENTOUT Additional: ADC012_IN10
PC1	16	I/O	5VT	Default: PC1 Alternate: SPI2_MOSI, I2S2_SD, SPI1_MOSI, I2S1_SD,

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Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				ENET_MDC, EVENTOUT Additional: ADC012_IN11
PC2	17	I/O	5VT	Default: PC2 Alternate: SPI1_MISO, I2S1_ADD_SD, USBHS_ULPI_DIR, ENET_MII_TXD2, EVENTOUT Additional: ADC012_IN12
PC3	18	I/O	5VT	Default: PC3 Alternate: SPI1_MOSI, I2S1_SD, USBHS_ULPI_NXT, ENET_MII_TX_CLK, EVENTOUT Additional: ADC012_IN13
VDD	19	P	-	Default: VDD
VSSA	20	P	-	Default: VSSA
V_{REFP}	21	P	-	Default: VREFP
VDDA	22	P	-	Default: VDDA
PA0-WKUP	23	I/O	5VT	Default: PA0 Alternate: TIMER1_CH0, TIMER1_ETI, TIMER4_CH0, TIMER7_ETI, USART1_CTS, UART3_TX, ENET_MII_CRS, EVENTOUT Additional: ADC012_IN0, WKUP
PA1	24	I/O	5VT	Default: PA1 Alternate: TIMER1_CH1, TIMER4_CH1, SPI3_MOSI, USART1_RTS, UART3_RX, ENET_MII_RX_CLK, ENET_RMII_REF_CLK, EVENTOUT Additional: ADC012_IN1
PA2	25	I/O	5VT	Default: PA2 Alternate: TIMER1_CH2, TIMER4_CH2, TIMER8_CH0, I2S_CKIN, USART1_TX, ENET_MDIO, EVENTOUT Additional: ADC012_IN2
PA3	26	I/O	5VT	Default: PA3 Alternate: TIMER1_CH3, TIMER4_CH3, TIMER8_CH1, I2S1_MCK, USART1_RX, USBHS_ULPI_D0, ENET_MII_COL, TLI_B5, EVENTOUT Additional: ADC012_IN3
VSS	27	P	-	Default: VSS
VDD	28	P	-	Default: VDD
PA4	29	I/O		Default: PA4 Alternate: SPI0_NSS, SPI2_NSS, I2S2_WS, USART1_CK, USBHS_SOF, DCI_HSYNC, TLI_VSYNC, EVENTOUT Additional: ADC01_IN4, DAC0_OUT0
PA5	30	I/O		Default: PA5 Alternate: TIMER1_CH0, TIMER1_ETI, TIMER7_CH0_ON, SPI0_SCK, USBHS_ULPI_CK, EVENTOUT Additional: ADC01_IN5, DAC0_OUT1
PA6	31	I/O	5VT	Default: PA6 Alternate: TIMER0_BRKIN, TIMER2_CH0,

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GD32F460Vx LQFP64				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				TIMER7_BRKIN, SPI0_MISO, I2S1_MCK, TIMER12_CH0, SDIO_CMD, DCI_PIXCLK, TLI_G2, EVENTOUT Additional: ADC01_IN6
PA7	32	I/O	5VT	Default: PA7 Alternate: TIMER0_CH0_ON, TIMER2_CH1, TIMER7_CH0_ON, SPI0_MOSI, TIMER13_CH0, ENET_MII_RX_DV, ENET_RMII_CRS_DV, EVENTOUT Additional: ADC01_IN7
PC4	33	I/O	5VT	Default: PC4 Alternate: ENET_MII_RXD0, ENET_RMII_RXD0, EVENTOUT Additional: ADC01_IN14
PC5	34	I/O	5VT	Default: PC5 Alternate: USART2_RX, ENET_MII_RXD1, ENET_RMII_RXD1, EVENTOUT Additional: ADC01_IN15
PB0	35	I/O	5VT	Default: PB0 Alternate: TIMER0_CH1_ON, TIMER2_CH2, TIMER7_CH1_ON, SPI4_SCK, SPI2_MOSI, I2S2_SD, TLI_R3, USBHS_ULPI_D1, ENET_MII_RXD2, SDIO_D1, EVENTOUT Additional: ADC01_IN8, IREF
PB1	36	I/O	5VT	Default: PB1 Alternate: TIMER0_CH2_ON, TIMER2_CH3, TIMER7_CH2_ON, SPI4_NSS, TLI_R6, USBHS_ULPI_D2, ENET_MII_RXD3, SDIO_D2, EVENTOUT Additional: ADC01_IN9
PB2	37	I/O	5VT	Default: PB2, BOOT1 Alternate: TIMER1_CH3, SPI2_MOSI, I2S2_SD, USBHS_ULPI_D4, SDIO_CK, EVENTOUT
PE7	38	I/O	5VT	Default: PE7 Alternate: TIMER0_ETI, UART6_RX, EXMC_D4, EVENTOUT
PE8	39	I/O	5VT	Default: PE8 Alternate: TIMER0_CH0_ON, UART6_TX, EXMC_D5, EVENTOUT
PE9	40	I/O	5VT	Default: PE9 Alternate: TIMER0_CH0, EXMC_D6, EVENTOUT
PE10	41	I/O	5VT	Default: PE10 Alternate: TIMER0_CH1_ON, EXMC_D7, EVENTOUT
PE11	42	I/O	5VT	Default: PE11 Alternate: TIMER0_CH1, SPI3_NSS, SPI4_NSS, EXMC_D8, TLI_G3, EVENTOUT
PE12	43	I/O	5VT	Default: PE12 Alternate: TIMER0_CH2_ON, SPI3_SCK, SPI4_SCK,

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Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				EXMC_D9, TLI_B4, EVENTOUT
PE13	44	I/O	5VT	Default: PE13 Alternate: TIMER0_CH2, SPI3_MISO, SPI4_MISO, EXMC_D10, TLI_DE, EVENTOUT
PE14	45	I/O	5VT	Default: PE14 Alternate: TIMER0_CH3, SPI3_MOSI, SPI4_MOSI, EXMC_D11, TLI_PIXCLK, EVENTOUT
PE15	46	I/O	5VT	Default: PE15 Alternate: TIMER0_BRKIN, EXMC_D12, TLI_R7, EVENTOUT
PB10	47	I/O	5VT	Default: PB10 Alternate: TIMER1_CH2, I2C1_SCL, SPI1_SCK, I2S1_CK, I2S2_MCK, USART2_TX, USBHS_ULPI_D3, ENET_MII_RX_ER, SDIO_D7, TLI_G4, EVENTOUT
PB11	48	I/O	5VT	Default: PB11 Alternate: TIMER1_CH3, I2C1_SDA, I2S_CKIN, USART2_RX, USBHS_ULPI_D4, ENET_MII_TX_EN, ENET_RMII_TX_EN, TLI_G5, EVENTOUT
NC	49	-	-	-
VDD	50	P	-	Default: VDD
PB12	51	I/O	5VT	Default: PB12 Alternate: TIMER0_BRKIN, I2C1_SMBA, SPI1_NSS, I2S1_WS, SPI3_NSS, USART2_CK, CAN1_RX, USBHS_ULPI_D5, ENET_MII_TXD0, ENET_RMII_TXD0, USBHS_ID, EVENTOUT
PB13	52	I/O	5VT	Default: PB13 Alternate: TIMER0_CH0_ON, SPI1_SCK, I2S1_CK, SPI3_SCK, USART2_CTS, CAN1_TX, USBHS_ULPI_D6, ENET_MII_TXD1, ENET_RMII_TXD1, EVENTOUT, I2C1_TXFRAME Additional: USBHS_VBUS
PB14	53	I/O	5VT	Default: PB14 Alternate: TIMER0_CH1_ON, TIMER7_CH1_ON, SPI1_MISO, I2S1_ADD_SD, USART2_RTS, TIMER11_CH0, USBHS_DM, EVENTOUT
PB15	54	I/O	5VT	Default: PB15 Alternate: RTC_REFIN, TIMER0_CH2_ON, TIMER7_CH2_ON, SPI1_MOSI, I2S1_SD, TIMER11_CH1, USBHS_DP, EVENTOUT
PD8	55	I/O	5VT	Default: PD8 Alternate: USART2_TX, EXMC_D13, EVENTOUT
PD9	56	I/O	5VT	Default: PD9 Alternate: USART2_RX, EXMC_D14, EVENTOUT
PD10	57	I/O	5VT	Default: PD10 Alternate: USART2_CK, EXMC_D15, TLI_B3, EVENTOUT

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Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PD11	58	I/O	5VT	Default: PD11 Alternate: USART2_CTS, EXMC_A16/EXMC_CLE, EVENTOUT
PD12	59	I/O	5VT	Default: PD12 Alternate: TIMER3_CH0, USART2_RTS, EXMC_A17/EXMC_ALE, EVENTOUT
PD13	60	I/O	5VT	Default: PD13 Alternate: TIMER3_CH1, EXMC_A18, EVENTOUT
PD14	61	I/O	5VT	Default: PD14 Alternate: TIMER3_CH2, EXMC_D0, EVENTOUT
PD15	62	I/O	5VT	Default: PD15 Alternate: TIMER3_CH3, EXMC_D1, EVENTOUT, CTC_SYNC
PC6	63	I/O	5VT	Default: PC6 Alternate: TIMER2_CH0, TIMER7_CH0, I2S1_MCK, USART5_TX, SDIO_D6, DCI_D0, TLI_HSYNC, EVENTOUT
PC7	64	I/O	5VT	Default: PC7 Alternate: TIMER2_CH1, TIMER7_CH1, SPI1_SCK, I2S1_CK, I2S2_MCK, USART5_RX, SDIO_D7, DCI_D1, TLI_G6, EVENTOUT
PC8	65	I/O	5VT	Default: PC8 Alternate: TIMER2_CH2, TIMER7_CH2, USART5_CK, SDIO_D0, DCI_D2, EVENTOUT
PC9	66	I/O	5VT	Default: PC9 Alternate: CK_OUT1, TIMER2_CH3, TIMER7_CH3, I2C2_SDA, I2S_CKIN, SDIO_D1, DCI_D3, EVENTOUT
PA8	67	I/O	5VT	Default: PA8 Alternate: CK_OUT0, TIMER0_CH0, I2C2_SCL, USART0_CK, USBFS_SOF, SDIO_D1, TLI_R6, EVENTOUT, CTC_SYNC
PA9	68	I/O	5VT	Default: PA9 Alternate: TIMER0_CH1, I2C2_SMBA, SPI1_SCK, I2S1_CK, USART0_TX, SDIO_D2, DCI_D0, EVENTOUT Additional: USBFS_VBUS
PA10	69	I/O	5VT	Default: PA10 Alternate: TIMER0_CH2, SPI4_MOSI, USART0_RX, USBFS_ID, DCI_D1, EVENTOUT, I2C2_TXFRAME
PA11	70	I/O	5VT	Default: PA11 Alternate: TIMER0_CH3, SPI3_MISO, USART0_CTS, USART5_TX, CAN0_RX, USBFS_DM, TLI_R4, EVENTOUT
PA12	71	I/O	5VT	Default: PA12 Alternate: TIMER0_ETI, SPI4_MISO, USART0_RTS, USART5_RX, CAN0_TX, USBFS_DP, TLI_R5,

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GD32F460Vx LQFP64				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				EVENTOUT
PA13	72	I/O	5VT	Default: JTMS, SWDIO, PA13 Alternate: EVENTOUT
NC	73	-	-	-
VSS	74	P	-	Default: VSS
VDD	75	P	-	Default: VDD
PA14	76	I/O	5VT	Default: JTCK, SWCLK, PA14 Alternate: EVENTOUT
PA15	77	I/O	5VT	Default: JTDI, PA15 Alternate: TIMER1_CH0, TIMER1_ETI, SPI0_NSS, SPI2_NSS, I2S2_WS, USART0_TX, EVENTOUT
PC10	78	I/O	5VT	Default: PC10 Alternate: SPI2_SCK, I2S2_CK, USART2_TX, UART3_TX, SDIO_D2, DCI_D8, TLI_R2, EVENTOUT
PC11	79	I/O	5VT	Default: PC11 Alternate: I2S2_ADD_SD, SPI2_MISO, USART2_RX, UART3_RX, SDIO_D3, DCI_D4, EVENTOUT
PC12	80	I/O	5VT	Default: PC12 Alternate: I2C1_SDA, SPI2_MOSI, I2S2_SD, USART2_CK, UART4_TX, SDIO_CK, DCI_D9, EVENTOUT
PD0	81	I/O	5VT	Default: PD0 Alternate: SPI3_MISO, SPI2_MOSI, I2S2_SD, CAN0_RX, EXMC_D2, EVENTOUT
PD1	82	I/O	5VT	Default: PD1 Alternate: SPI1_NSS, I2S1_WS, CAN0_TX, EXMC_D3, EVENTOUT
PD2	83	I/O	5VT	Default: PD2 Alternate: TIMER2_ETI, UART4_RX, SDIO_CMD, DCI_D11, EVENTOUT
PD3	84	I/O	5VT	Default: PD3 Alternate: SPI1_SCK, I2S1_CK, USART1_CTS, EXMC_CLK, DCI_D5, TLI_G7, EVENTOUT
PD4	85	I/O	5VT	Default: PD4 Alternate: USART1_RTS, EXMC_NOE, EVENTOUT
PD5	86	I/O	5VT	Default: PD5 Alternate: USART1_TX, EXMC_NWE, EVENTOUT
PD6	87	I/O	5VT	Default: PD6 Alternate: SPI2_MOSI, I2S2_SD, USART1_RX, EXMC_NWAIT, DCI_D10, TLI_B2, EVENTOUT
PD7	88	I/O	5VT	Default: PD7 Alternate: USART1_CK, EXMC_NE0, EXMC_NCE1, EVENTOUT
PB3	89	I/O	5VT	Default: JTDO, PB3 Alternate: TRACESWO, TIMER1_CH1, SPI0_SCK, SPI2_SCK, I2S2_CK, USART0_RX, I2C1_SDA,

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Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				EVENTOUT
PB4	90	I/O	5VT	Default: JNTRST, PB4 Alternate: TIMER2_CH0, SPI0_MISO, SPI2_MISO, I2S2_ADD_SD, I2C2_SDA, SDIO_D0, EVENTOUT, I2C0_TXFRAME
PB5	91	I/O	5VT	Default: PB5 Alternate: TIMER2_CH1, I2C0_SMBA, SPI0_MOSI, SPI2_MOSI, I2S2_SD, CAN1_RX, USBHS_ULPI_D7, ENET_PPS_OUT, DCI_D10, EVENTOUT
PB6	92	I/O	5VT	Default: PB6 Alternate: TIMER3_CH0, I2C0_SCL, USART0_TX, CAN1_TX, DCI_D5, EVENTOUT
PB7	93	I/O	5VT	Default: PB7 Alternate: TIMER3_CH1, I2C0_SDA, USART0_RX, EXMC_NL/EXMC_NADV, DCI_VSYNC, EVENTOUT
BOOT0	94	I/O	5VT	Default: BOOT0
PB8	95	I/O	5VT	Default: PB8 Alternate: TIMER1_CH0, TIMER1_ETI, TIMER3_CH2, TIMER9_CH0, I2C0_SCL, SPI4_MOSI, CAN0_RX, ENET_MII_TXD3, SDIO_D4, DCI_D6, TLI_B6, EVENTOUT
PB9	96	I/O	5VT	Default: PB9 Alternate: TIMER1_CH1, TIMER3_CH3, TIMER10_CH0, I2C0_SDA, SPI1_NSS, I2S1_WS, CAN0_TX, SDIO_D5, DCI_D7, TLI_B7, EVENTOUT
PE0	97	I/O	5VT	Default: PE0 Alternate: TIMER3_ETI, UART7_RX, EXMC_NBL0, DCI_D2, EVENTOUT
PE1	98	I/O	5VT	Default: PE1 Alternate: TIMER0_CH1_ON, UART7_TX, EXMC_NBL1, DCI_D3, EVENTOUT
VSS	99	P	-	Default: VSS
VDD	100	P	-	Default: VDD

Notes:

(1) Type: I = input, O = output, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

2.6.2. GD32F460Rx LQFP64 pin definitions

Table 2-4. GD32F460Rx LQFP64 pin definitions

GD32F427Rx LQFP64				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
VBAT	1	P	-	Default: VBAT

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GD32F427Rx LQFP64				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PC13-TAMPER-RTC	2	I/O	5VT	Default: PC13 Alternate: EVENTOUT Additional: RTC_TAMP0, RTC_OUT, RTC_TS
PC14-OSC32IN	3	I/O	5VT	Default: PC14 Alternate: EVENTOUT Additional: OSC32IN
PC15-OSC32OUT	4	I/O	5VT	Default: PC15 Alternate: EVENTOUT Additional: OSC32OUT
PH0/OSCIN	5	I/O	5VT	Default: PH0, OSCIN Alternate: EVENTOUT Additional: OSCIN
PH1/OSCOUT	6	I/O	5VT	Default: PH1, OSCOUT Alternate: EVENTOUT Additional: OSCOUT
NRST	7	-	-	Default: NRST
PC0	8	I/O	5VT	Default: PC0 Alternate: USBHS_ULPI_STP, EVENTOUT Additional: ADC012_IN10
PC1	9	I/O	5VT	Default: PC1 Alternate: SPI2_MOSI, I2S2_SD, SPI1_MOSI, I2S1_SD, ENET_MDC, EVENTOUT Additional: ADC012_IN11
PC2	10	I/O	5VT	Default: PC2 Alternate: SPI1_MISO, I2S1_ADD_SD, USBHS_ULPI_DIR, ENET_MII_TXD2, EVENTOUT Additional: ADC012_IN12
PC3	11	I/O	5VT	Default: PC3 Alternate: SPI1_MOSI, I2S1_SD, USBHS_ULPI_NXT, ENET_MII_TX_CLK, EVENTOUT Additional: ADC012_IN13
VSSA	12	P	-	Default: VSSA
VDDA	13	P	-	Default: VDDA
PA0-WKUP	14	I/O	5VT	Default: PA0 Alternate: TIMER1_CH0, TIMER1_ETI, TIMER4_CH0, TIMER7_ETI, USART1_CTS, UART3_TX, ENET_MII_CRS, EVENTOUT Additional: ADC012_IN0, WKUP
PA1	15	I/O	5VT	Default: PA1 Alternate: TIMER1_CH1, TIMER4_CH1, USART1_RTS, UART3_RX, ENET_MII_RX_CLK, ENET_RMII_REF_CLK,

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GD32F427Rx LQFP64				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				EVENTOUT Additional: ADC012_IN1
PA2	16	I/O	5VT	Default: PA2 Alternate: TIMER1_CH2, TIMER4_CH2, TIMER8_CH0, I2S_CKIN, USART1_TX, ENET_MDIO, EVENTOUT Additional: ADC012_IN2
PA3	17	I/O	5VT	Default: PA3 Alternate: TIMER1_CH3, TIMER4_CH3, TIMER8_CH1, I2S1_MCK, USART1_RX, USBHS_ULPI_D0, ENET_MII_COL, EVENTOUT Additional: ADC012_IN3
VSS	18	P	-	Default: VSS
VDD	19	P	-	Default: VDD
PA4	20	I/O		Default: PA4 Alternate: SPI0_NSS, SPI2_NSS, I2S2_WS, USART1_CK, USBHS_SOF, DCI_HSYNC, EVENTOUT Additional: ADC01_IN4, DAC0_OUT0
PA5	21	I/O		Default: PA5 Alternate: TIMER1_CH0, TIMER1_ETI, TIMER7_CH0_ON, SPI0_SCK, USBHS_ULPI_CK, EVENTOUT Additional: ADC01_IN5, DAC0_OUT1
PA6	22	I/O	5VT	Default: PA6 Alternate: TIMER0_BRKIN, TIMER2_CH0, TIMER7_BRKIN, SPI0_MISO, I2S1_MCK, TIMER12_CH0, SDIO_CMD, DCI_PIXCLK, EVENTOUT Additional: ADC01_IN6
PA7	23	I/O	5VT	Default: PA7 Alternate: TIMER0_CH0_ON, TIMER2_CH1, TIMER7_CH0_ON, SPI0_MOSI, TIMER13_CH0, ENET_MII_RX_DV, ENET_RMII_CRS_DV, EVENTOUT Additional: ADC01_IN7
PC4	24	I/O	5VT	Default: PC4 Alternate: ENET_MII_RXD0, ENET_RMII_RXD0, EVENTOUT Additional: ADC01_IN14
PC5	25	I/O	5VT	Default: PC5 Alternate: USART2_RX, ENET_MII_RXD1, ENET_RMII_RXD1, EVENTOUT Additional: ADC01_IN15
PB0	26	I/O	5VT	Default: PB0 Alternate: TIMER0_CH1_ON, TIMER2_CH2,

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GD32F427Rx LQFP64				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				TIMER7_CH1_ON, SPI2_MOSI, I2S2_SD, USBHS_ULPI_D1, ENET_MII_RXD2, SDIO_D1, EVENTOUT Additional: ADC01_IN8, IREF
PB1	27	I/O	5VT	Default: PB1 Alternate: TIMER0_CH2_ON, TIMER2_CH3, TIMER7_CH2_ON, USBHS_ULPI_D2, ENET_MII_RXD3, SDIO_D2, EVENTOUT Additional: ADC01_IN9
PB2	28	I/O	5VT	Default: PB2, BOOT1 Alternate: TIMER1_CH3, SPI2_MOSI, I2S2_SD, USBHS_ULPI_D4, SDIO_CK, EVENTOUT
PB10	29	I/O	5VT	Default: PB10 Alternate: TIMER1_CH2, I2C1_SCL, SPI1_SCK, I2S1_CK, I2S2_MCK, USART2_TX,USBHS_ULPI_D3, ENET_MII_RX_ER, SDIO_D7, EVENTOUT
PB11	30	I/O	5VT	Default: PB11 Alternate: TIMER1_CH3, I2C1_SDA, I2S_CKIN, USART2_RX, USBHS_ULPI_D4, ENET_MII_TX_EN, ENET_RMII_TX_EN, EVENTOUT
NC	31	-	-	-
VDD	32	P	-	Default: VDD
PB12	33	I/O	5VT	Default: PB12 Alternate: TIMER0_BRKIN, I2C1_SMBA, SPI1_NSS, I2S1_WS, USART2_CK, CAN1_RX, USBHS_ULPI_D5, ENET_MII_TXD0, ENET_RMII_TXD0, USBHS_ID, EVENTOUT
PB13	34	I/O	5VT	Default: PB13 Alternate: TIMER0_CH0_ON, SPI1_SCK, I2S1_CK, USART2_CTS, CAN1_TX, USBHS_ULPI_D6, ENET_MII_TXD1, ENET_RMII_TXD1, EVENTOUT, I2C1_TXFRAME Additional: USBHS_VBUS
PB14	35	I/O	5VT	Default: PB14 Alternate: TIMER0_CH1_ON, TIMER7_CH1_ON, SPI1_MISO, I2S1_ADD_SD, USART2_RTS, TIMER11_CH0, USBHS_DM, EVENTOUT
PB15	36	I/O	5VT	Default: PB15 Alternate: RTC_REFIN, TIMER0_CH2_ON, TIMER7_CH2_ON, SPI1_MOSI, I2S1_SD, TIMER11_CH1, USBHS_DP, EVENTOUT

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Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PC6	37	I/O	5VT	Default: PC6 Alternate: TIMER2_CH0, TIMER7_CH0, I2S1_MCK, USART5_TX, SDIO_D6, DCI_D0, EVENTOUT
PC7	38	I/O	5VT	Default: PC7 Alternate: TIMER2_CH1, TIMER7_CH1, SPI1_SCK, I2S1_CK, I2S2_MCK, USART5_RX, SDIO_D7, DCI_D1, EVENTOUT
PC8	39	I/O	5VT	Default: PC8 Alternate: TIMER2_CH2, TIMER7_CH2, USART5_CK, SDIO_D0, DCI_D2, EVENTOUT
PC9	40	I/O	5VT	Default: PC9 Alternate: CK_OUT1, TIMER2_CH3, TIMER7_CH3, I2C2_SDA, I2S_CKIN, SDIO_D1, DCI_D3, EVENTOUT
PA8	41	I/O	5VT	Default: PA8 Alternate: CK_OUT0, TIMER0_CH0, I2C2_SCL, USART0_CK, USBFS_SOF, SDIO_D1, EVENTOUT, CTC_SYNC
PA9	42	I/O	5VT	Default: PA9 Alternate: TIMER0_CH1, I2C2_SMBA, SPI1_SCK, I2S1_CK, USART0_TX, SDIO_D2, DCI_D0, EVENTOUT Additional: USBFS_VBUS
PA10	43	I/O	5VT	Default: PA10 Alternate: TIMER0_CH2, USART0_RX, USBFS_ID, DCI_D1, EVENTOUT, I2C2_TXFRAME
PA11	44	I/O	5VT	Default: PA11 Alternate: TIMER0_CH3, USART0_CTS, USART5_TX, CAN0_RX, USBFS_DM, EVENTOUT
PA12	45	I/O	5VT	Default: PA12 Alternate: TIMER0_ETI, USART0_RTS, USART5_RX, CAN0_TX, USBFS_DP, EVENTOUT
PA13	46	I/O	5VT	Default: JTMS, SWDIO, PA13 Alternate: EVENTOUT
VDD	48	P	-	Default: VDD
PA14	49	I/O	5VT	Default: JTCK, SWCLK, PA14 Alternate: EVENTOUT
PA15	50	I/O	5VT	Default: JTDI, PA15 Alternate: TIMER1_CH0, TIMER1_ETI, SPI0_NSS, SPI2_NSS, I2S2_WS, USART0_TX, EVENTOUT
PC10	51	I/O	5VT	Default: PC10 Alternate: SPI2_SCK, I2S2_CK, USART2_TX, UART3_TX, SDIO_D2, DCI_D8, EVENTOUT

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GD32F427Rx LQFP64				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PC11	52	I/O	5VT	Default: PC11 Alternate: I2S2_ADD_SD, SPI2_MISO, USART2_RX, UART3_RX, SDIO_D3, DCI_D4, EVENTOUT
PC12	53	I/O	5VT	Default: PC12 Alternate: I2C1_SDA, SPI2_MOSI, I2S2_SD, USART2_CK, UART4_TX, SDIO_CK, DCI_D9, EVENTOUT
PD2	54	I/O	5VT	Default: PD2 Alternate: TIMER2_ETI, UART4_RX, SDIO_CMD, DCI_D11, EVENTOUT
PB3	55	I/O	5VT	Default: JTDO, PB3 Alternate: TRACESWO, TIMER1_CH1, SPI0_SCK, SPI2_SCK, I2S2_CK, USART0_RX, I2C1_SDA, EVENTOUT
PB4	56	I/O	5VT	Default: NJTRST, PB4 Alternate: TIMER2_CH0, SPI0_MISO, SPI2_MISO, I2S2_ADD_SD, I2C2_SDA, SDIO_D0, EVENTOUT, I2C0_TXFRAME
PB5	57	I/O	5VT	Default: PB5 Alternate: TIMER2_CH1, I2C0_SMBA, SPI0_MOSI, SPI2_MOSI, I2S2_SD, CAN1_RX, USBHS_ULPI_D7, ENET_PPS_OUT, DCI_D10, EVENTOUT
PB6	58	I/O	5VT	Default: PB6 Alternate: TIMER3_CH0, I2C0_SCL, USART0_TX, CAN1_TX, DCI_D5, EVENTOUT
PB7	59	I/O	5VT	Default: PB7 Alternate: TIMER3_CH1, I2C0_SDA, USART0_RX, DCI_VSYNC, EVENTOUT
BOOT0	60	I/O	5VT	Default: BOOT0
PB8	61	I/O	5VT	Default: PB8 Alternate: TIMER1_CH0, TIMER1_ETI, TIMER3_CH2, TIMER9_CH0, I2C0_SCL, CAN0_RX, ENET_MII_TXD3, SDIO_D4, DCI_D6, EVENTOUT
PB9	62	I/O	5VT	Default: PB9 Alternate: TIMER1_CH1, TIMER3_CH3, TIMER10_CH0, I2C0_SDA, SPI1_NSS, I2S1_WS, CAN0_TX, SDIO_D5, DCI_D7, EVENTOUT
VSS	63	P	-	Default: VSS
VDD	64	P	-	Default: VDD

Notes:

(1) Type: I = input, O = output, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

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2.6.3. GD32F460xx pin alternate functions

Table 2-5. Port A alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PA0		TIMER1_CH0/TIMER1_ETI	TIMER4_CH0	TIMER7_ETI				USART1_CTS	UART3_TX			ENET_MII_CRS				EVENTOUT
PA1		TIMER1_CH1	TIMER4_CH1			SPI3_MOSI		USART1_RTS	UART3_RX			ENET_MII_RX_CLK/ENET_RMII_REF_CLK				EVENTOUT
PA2		TIMER1_CH2	TIMER4_CH2	TIMER8_CH0		I2S_CKIN		USART1_TX				ENET_MDIO				EVENTOUT
PA3		TIMER1_CH3	TIMER4_CH3	TIMER8_CH1		I2S1_MCK		USART1_RX			USBHS_ULPI_D0	ENET_MII_COL			TLI_B5	EVENTOUT
PA4						SPI0_NSS	SPI2_NSS/I2S2_WS	USART1_CK					USBHS_SOF	DCI_HSYNC	TLI_VSYNC	EVENTOUT
PA5		TIMER1_CH0/TIMER1_ETI		TIMER7_CH0_ON		SPI0_SCK					USBHS_ULPI_CK					EVENTOUT
PA6		TIMER0_BRKIN	TIMER2_CH0	TIMER7_BRKIN		SPI0_MISO	I2S1_MCK			TIMER12_CH0			SDIO_CMD	DCI_PIXCLK	TLI_G2	EVENTOUT
PA7		TIMER0_CH0_ON	TIMER2_CH1	TIMER7_CH0_ON		SPI0_MOSI				TIMER13_CH0		ENET_MII_RX_DV/ENET_RMII_CRS_DV				EVENTOUT
PA8	CK_OUT0	TIMER0_CH0			I2C2_SCL			USART0_CK		CTC_SYNC	USBFS_SOF		SDIO_D1		TLI_R6	EVENTOUT
PA9		TIMER0_CH1			I2C2_SMBA	SPI1_SCK/I2S1_CK		USART0_TX					SDIO_D2	DCI_D0		EVENTOUT
PA10		TIMER0_CH2			I2C2_TXFRAME		SPI4_MOSI	USART0_RX			USBFS_ID			DCI_D1		EVENTOUT
PA11		TIMER0_CH3					SPI3_MISO	USART0_CTS	USART5_TX	CAN0_RX	USBFS_DM				TLI_R4	EVENTOUT
PA12		TIMER0_ETI					SPI4_MISO	USART0_RTS	USART5_RX	CAN0_TX	USBFS_DP				TLI_R5	EVENTOUT
PA13	JTMS/SWDIO															EVENTOUT
PA14	JTCK/SWCLK															EVENTOUT

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Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PA15	JTDI	TIMER1_CH0/TIMER1_ETI				SPI0_NSS	SPI2_NSS/I2S2_WS	USART0_TX								EVENTOUT

Table 2-6. Port B alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PB0		TIMER0_CH1_ON	TIMER2_CH2	TIMER7_CH1_ON			SPI4_SCK	SPI2_MOSI/I2S2_SD		TLI_R3	USBHS_ULPI_D1	ENET_MII_RXD2	SDIO_D1			EVENTOUT
PB1		TIMER0_CH2_ON	TIMER2_CH3	TIMER7_CH2_ON			SPI4_NSS			TLI_R6	USBHS_ULPI_D2	ENET_MII_RXD3	SDIO_D2			EVENTOUT
PB2		TIMER1_CH3						SPI2_MOSI/I2S2_SD			USBHS_ULPI_D4		SDIO_CK			EVENTOUT
PB3	JTDO/TRACESWO	TIMER1_CH1				SPI0_SCK	SPI2_SCK/I2S2_CK	USART0_RX		I2C1_SDA						EVENTOUT
PB4	NJTRST		TIMER2_CH0		I2C0_TXFRAME	SPI0_MISO	SPI2_MISO	I2S2_ADD_SD		I2C2_SDA			SDIO_D0			EVENTOUT
PB5			TIMER2_CH1		I2C0_SMBA	SPI0_MOSI	SPI2_MOSI/I2S2_SD			CAN1_RX	USBHS_ULPI_D7	ENET_PPS_OUT		DCI_D10		EVENTOUT
PB6			TIMER3_CH0		I2C0_SCL			USART0_TX		CAN1_TX				DCI_D5		EVENTOUT
PB7			TIMER3_CH1		I2C0_SDA			USART0_RX					EXMC_NL/EXMC_NADV	DCI_VSYNC		EVENTOUT
PB8		TIMER1_CH0/TIMER1_ETI	TIMER3_CH2	TIMER9_CH0	I2C0_SCL		SPI4_MOSI			CAN0_RX		ENET_MII_TXD3	SDIO_D4	DCI_D6	TLI_B6	EVENTOUT
PB9		TIMER1_CH1	TIMER3_CH3	TIMER10_CH0	I2C0_SDA	SPI1_NSS/I2S1_WS				CAN0_TX			SDIO_D5	DCI_D7	TLI_B7	EVENTOUT
PB10		TIMER1_CH2			I2C1_SCL	SPI1_SCK/I2S1_CK	I2S2_MCK	USART2_TX			USBHS_ULPI_D3	ENET_MII_RX_ER	SDIO_D7		TLI_G4	EVENTOUT
PB11		TIMER1_CH3			I2C1_SDA	I2S_CKIN		USART2_RX			USBHS_ULPI_D4	ENET_MII_TX_EN/ENET_RMII_TX_EN			TLI_G5	EVENTOUT
PB12		TIMER0_BRKIN			I2C1_SMBA	SPI1_NSS/I2S1_WS	SPI3_NSS	USART2_CK		CAN1_RX	USBHS_ULPI_D5	ENET_MII_TXD0/ENET_RMII_TXD0	USBHS_ID			EVENTOUT
PB13		TIMER0_CH0_ON			I2C1_TXFRAME	SPI1_SCK/I2S1_CK	SPI3_SCK	USART2_CTS		CAN1_TX	USBHS_ULPI_D6	ENET_MII_TXD1/ENET_RMII_TXD1				EVENTOUT

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Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PB14		TIMER0_CH1_ON		TIMER7_CH1_ON		SPI1_MISO	I2S1_ADD_SD	USART2_RTS		TIMER11_CH0			USBHS_DM			EVENTOUT
PB15	RTC_REFIN	TIMER0_CH2_ON		TIMER7_CH2_ON		SPI1_MOSI/I2S1_SD				TIMER11_CH1			USBHS_DP			EVENTOUT

Table 2-7. Port C alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PC0											USBHS_ULPI_STP					EVENTOUT
PC1						SPI2_MOSI/I2S2_SD		SPI1_MOSI/I2S1_SD				ENET_MDC				EVENTOUT
PC2						SPI1_MISO	I2S1_ADD_SD				USBHS_ULPI_DIR	ENET_MII_TXD2				EVENTOUT
PC3						SPI1_MOSI/I2S1_SD					USBHS_ULPI_NXT	ENET_MII_TX_CLK				EVENTOUT
PC4												ENET_MII_RXD0/ENET_RMII_RXD0				EVENTOUT
PC5								USART2_RX				ENET_MII_RXD1/ENET_RMII_RXD1				EVENTOUT
PC6			TIMER2_CH0	TIMER7_CH0		I2S1_MCK			USART5_TX				SDIO_D6	DCI_D0	TLI_HSYNC	EVENTOUT
PC7			TIMER2_CH1	TIMER7_CH1		SPI1_SCK/I2S1_CK	I2S2_MCK		USART5_RX				SDIO_D7	DCI_D1	TLI_G6	EVENTOUT
PC8			TIMER2_CH2	TIMER7_CH2					USART5_CK				SDIO_D0	DCI_D2		EVENTOUT
PC9	CK_OUT1		TIMER2_CH3	TIMER7_CH3	I2C2_SDA	I2S_CKIN							SDIO_D1	DCI_D3		EVENTOUT
PC10							SPI2_SCK/I2S2_CK	USART2_TX	UART3_TX				SDIO_D2	DCI_D8	TLI_R2	EVENTOUT
PC11						I2S2_ADD_SD	SPI2_MISO	USART2_RX	UART3_RX				SDIO_D3	DCI_D4		EVENTOUT
PC12					I2C1_SDA		SPI2_MOSI/I2S2_SD	USART2_CK	UART4_TX				SDIO_CK	DCI_D9		EVENTOUT
PC13																EVENTOUT
PC14																EVENTOUT

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Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PC15																EVENTOUT

Table 2-8. Port D alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PD0						SPI3_MISO	SPI2_MOSI/I2S2_SD			CAN0_RX			EXMC_D2			EVENTOUT
PD1								SPI1_NSS/I2S1_WS		CAN0_TX			EXMC_D3			EVENTOUT
PD2			TIMER2_ETI						UART4_RX				SDIO_CMD	DCI_D11		EVENTOUT
PD3						SPI1_SCK/I2S1_CK		USART1_CTS					EXMC_CLK	DCI_D5	TLI_G7	EVENTOUT
PD4								USART1_RTS					EXMC_NOE			EVENTOUT
PD5								USART1_TX					EXMC_NWE			EVENTOUT
PD6						SPI2_MOSI/I2S2_SD		USART1_RX					EXMC_NWAIT	DCI_D10	TLI_B2	EVENTOUT
PD7								USART1_CK					EXMC_NE0/EXMC_NCE1			EVENTOUT
PD8								USART2_TX					EXMC_D13			EVENTOUT
PD9								USART2_RX					EXMC_D14			EVENTOUT
PD10								USART2_CK					EXMC_D15		TLI_B3	EVENTOUT
PD11								USART2_CTS					EXMC_A16/EXMC_CLE			EVENTOUT
PD12			TIMER3_CH0					USART2_RTS					EXMC_A17/EXMC_ALE			EVENTOUT
PD13			TIMER3_CH1										EXMC_A18			EVENTOUT
PD14			TIMER3_CH2										EXMC_D0			EVENTOUT

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Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PD15	CTC_SYNC		TIMER3_CH3										EXMC_D1			EVENTOUT

Table 2-9. Port E alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PE0			TIMER3_ETI						UART7_RX				EXMC_NBL0	DCI_D2		EVENTOUT
PE1		TIMER0_CH1_ON							UART7_TX				EXMC_NBL1	DCI_D3		EVENTOUT
PE2						SPI3_SCK						ENET_MII_TXD3	EXMC_A23			EVENTOUT
PE3													EXMC_A19			EVENTOUT
PE4						SPI3_NSS							EXMC_A20	DCI_D4	TLI_B0	EVENTOUT
PE5				TIMER8_CH0		SPI3_MISO							EXMC_A21	DCI_D6	TLI_G0	EVENTOUT
PE6				TIMER8_CH1		SPI3_MOSI							EXMC_A22	DCI_D7	TLI_G1	EVENTOUT
PE7		TIMER0_ETI							UART6_RX				EXMC_D4			EVENTOUT
PE8		TIMER0_CH0_ON							UART6_TX				EXMC_D5			EVENTOUT
PE9		TIMER0_CH0											EXMC_D6			EVENTOUT
PE10		TIMER0_CH1_ON											EXMC_D7			EVENTOUT
PE11		TIMER0_CH1				SPI3_NSS	SPI4_NSS						EXMC_D8		TLI_G3	EVENTOUT
PE12		TIMER0_CH2_ON				SPI3_SCK	SPI4_SCK						EXMC_D9		TLI_B4	EVENTOUT
PE13		TIMER0_CH2				SPI3_MISO	SPI4_MISO						EXMC_D10		TLI_DE	EVENTOUT
PE14		TIMER0_CH3				SPI3_MOSI	SPI4_MOSI						EXMC_D11		TLI_PIXCLK	EVENTOUT
PE15		TIMER0_BRKIN											EXMC_D12		TLI_R7	EVENTOUT

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Table 2-10. Port H alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PH0																EVENTOUT
PH1																EVENTOUT

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3. Functional description

3.1. Arm® Cortex®-M4 core

The Arm® Cortex®-M4 processor is a high performance embedded processor with DSP instructions which allow efficient signal processing and complex algorithm execution. It brings an efficient, easy-to-use blend of control and signal processing capabilities to meet the digital signal control markets demand. The processor is highly configurable enabling a wide range of implementations from those requiring floating point operations, memory protection and powerful trace technology to cost sensitive devices requiring minimal area, while delivering outstanding computational performance and an advanced system response to interrupts.

32-bit Arm® Cortex®-M4 processor core

- Up to 240 MHz operation frequency
- Single-cycle multiplication and hardware divider
- Floating Point Unit (FPU)
- Integrated DSP instructions
- Integrated Nested Vectored Interrupt Controller (NVIC)
- 24-bit SysTick timer

The Cortex®-M4 processor is based on the Armv7-M architecture and supports both Thumb and Thumb-2 instruction sets. Some system peripherals listed below are also provided by Cortex®-M4:

- Internal Bus Matrix connected with ICode bus, DCode bus, system bus, Private Peripheral Bus (PPB) and debug accesses (AHB-AP)
- Nested Vectored Interrupt Controller (NVIC)
- Flash Patch and Breakpoint (FPB)
- Data Watchpoint and Trace (DWT)
- Instrument Trace Macrocell (ITM)
- Memory Protection Unit (MPU)
- Serial Wire JTAG Debug Port (SWJ-DP)
- Trace Port Interface Unit (TPIU)

3.2. On-chip memory

- Up to 2048 Kbytes of Flash memory, including code Flash and data Flash.
- The region of the MCU executing instructions without waiting time is up to 768K bytes. A long delay when CPU fetches the instructions out of the range.
- 768 KB of SRAM.

The Arm® Cortex®-M4 processor is structured in Harvard architecture which can use separate buses to fetch instructions and load/store data. Up to 2048 Kbytes of inner Flash, which includes code Flash and data Flash is available for storing programs and data, and there is

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no waiting time within code Flash area when CPU executes instructions. Up to 768 Kbytes of inner SRAM is composed of SRAM0 (112KB), SRAM1 (16KB), and SRAM2 (64KB) and ADDSRAM (512KB) that can be accessed at same time, and including 64 KB of TCM (tightly-coupled memory) data RAM that can be accessed only by the data bus of the Cortex®-M4 core. The additional 4KB of backup SRAM (BKP SRAM) is implemented in the backup domain, which can keep its content even when the V_{DD} power supply is down. ***Table 2-2. GD32F460xx memory map*** shows the memory map of the GD32F460xx series of devices, including Flash, SRAM, peripheral, and other pre-defined regions.

3.3. Clock, reset and supply management

- Internal 16 MHz factory-trimmed RC and external 4 to 32 MHz crystal oscillator
- Internal 48 MHz RC oscillator
- Internal 32 KHz RC calibrated oscillator and external 32.768 KHz crystal oscillator
- Integrated system clock PLL
- 2.6 to 3.6 V application supply and I/Os
- Supply Supervisor: POR (Power On Reset), PDR (Power Down Reset), and low voltage detector (LVD)

The Clock Control Unit (CCU) provides a range of oscillator and clock functions. These include internal RC oscillator and external crystal oscillator, high speed and low speed two types. Several prescalers allow the frequency configuration of the AHB and two APB domains. The maximum frequency of the two AHB domains are 240 MHz. The maximum frequency of the two APB domains including APB1 is 60 MHz and APB2 is 120 MHz. See ***Figure 2-4. GD32F460xx clock tree*** for details on the clock tree.

The Reset Control Unit (RCU) controls three kinds of reset: system reset resets the processor core and peripheral IP components. Power-on reset (POR) and power-down reset (PDR) are always active, and ensures proper operation starting from 2.4 V and down to 1.8V. The device remains in reset mode when V_{DD} is below a specified threshold. The embedded low voltage detector (LVD) monitors the power supply, compares it to the voltage threshold and generates an interrupt as a warning message for leading the MCU into security.

Power supply schemes:

- V_{DD} range: 2.6 to 3.6 V, external power supply for I/Os and the internal regulator. Provided externally through VDD pins.
- V_{SSA}, V_{DDA} range: 2.6 to 3.6 V, external analog power supplies for ADC, reset blocks, RCs and PLL. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.
- V_{BAT} range: 1.8 to 3.6 V, power supply for RTC, external clock 32 KHz oscillator and backup registers (through power switch) when V_{DD} is not present.

3.4. Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from main Flash memory (default)

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- Boot from system memory
- Boot from on-chip SRAM

The boot loader is located in the internal 30KB of information blocks for the boot ROM memory (system memory). It is used to reprogram the Flash memory by using USART0 (PA9 and PA10), USART2 (PB10 and PB11, or PC10 and PC11), and USBFS (PA9, PA10, PA11 and PA12) in device mode. It also can be used to transfer and update the Flash memory code, the data and the vector table sections. In default condition, boot from bank 0 of Flash memory is selected. It also supports to boot from bank 1 of Flash memory by setting a bit in option bytes.

3.5. Power saving modes

The MCU supports three kinds of power saving modes to achieve even lower power consumption. They are sleep mode, deep-sleep mode, and standby mode. These operating modes reduce the power consumption and allow the application to achieve the best balance between the CPU operating time, speed and power consumption.

- **Sleep** mode
  In sleep mode, only the clock of CPU core is off. All peripherals continue to operate and any interrupt/event can wake up the system.
- **Deep-sleep** mode
  In deep-sleep mode, all clocks in the 1.2V domain are off, and all of the high speed crystal oscillator (IRC16M, HXTAL) and PLL are disabled. Only the contents of SRAM and registers are retained. Any interrupt or wakeup event from EXTI lines can wake up the system from the deep-sleep mode including the 16 external lines, the RTC alarm, RTC Tamper and TimeStamp event, the LVD output, ENET wakeup, RTC wakeup and USB wakeup. When exiting the deep-sleep mode, the IRC16M is selected as the system clock.
- **Standby** mode
  In standby mode, the whole 1.2V domain is power off, the LDO is shut down, and all of IRC16M, HXTAL and PLL are disabled. The contents of SRAM and registers (except backup registers) are lost. There are four wakeup sources for the standby mode, including the external reset from NRST pin, the RTC, the FWDGT reset, and the rising edge on WKUP pin.

3.6. Analog to digital converter (ADC)

- 12-bit SAR ADC's conversion rate is up to 2.6 MSPS
- 12-bit, 10-bit, 8-bit or 6-bit configurable resolution
- Hardware oversampling ratio adjustable from 2 to 256x improves resolution to 16-bit
- Input voltage range: V_{SSA} to V_{DDA} (2.6 V ≤ V_{DDA} ≤ 3.6 V)
- Temperature sensor

Up to three 12-bit 2.6 MSPS multi-channel ADCs are integrated in the device. It has a total of

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19 multiplexed channels: 16 external channels, 1 channel for internal temperature sensor (V_{SENSE}), 1 channel for internal reference voltage (V_{REFINT}) and 1 channel for external battery power supply (V_{BAT}). The input voltage range is between 2.6 V and 3.6 V. An on-chip hardware oversampling scheme improves performance while off-loading the related computational burden from the CPU. An analog watchdog block can be used to detect the channels, which are required to remain within a specific threshold window. A configurable channel management block can be used to perform conversions in single, continuous, scan or discontinuous mode to support more advanced use.

The ADC can be triggered from the events generated by the general level 0 timers (TIMERx) and the advanced timers (TIMER0 and TIMER7) with internal connection. The temperature sensor can be used to generate a voltage that varies linearly with temperature. It is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage in a digital value.

3.7. Digital to analog converter (DAC)

- Two 12-bit DAC converter of independent output channel
- 8-bit or 12-bit mode in conjunction with the DMA controller

The 12-bit buffered DAC channel is used to generate variable analog outputs. The DACs are designed with integrated resistor strings structure. The DAC channels can be triggered by the timer update outputs or EXTI with DMA support. The maximum output value of the DAC is V_{REFP}.

3.8. DMA

- 16 channels DMA controller and each channel are configurable (8 for DMA0 and 8 for DMA1)
- Support independent 8, 16, 32-bit memory and peripheral transfer
- Peripherals supported: Timers, ADC, SPIs, I2Cs, USARTs, UARTs, DAC, I2S, SDIO and DCI

The flexible general-purpose DMA controllers provide a hardware method of transferring data between peripherals and/or memory without intervention from the CPU, thereby freeing up bandwidth for other system functions. Three types of access method are supported: peripheral to memory, memory to peripheral, memory to memory.

Each channel is connected to fixed hardware DMA requests. The priorities of DMA channel requests are determined by software configuration and hardware channel number. Transfer size of source and destination are independent and configurable.

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3.9. General-purpose inputs/outputs (GPIOs)

- Up to 82 fast GPIOs, all mappable on 16 external interrupt lines
- Analog input/output configurable
- Alternate function input/output configurable

There are up to 82 general purpose I/O pins (GPIO) in GD32F460xx, named PA0 ~ PA15, PB0 ~ PB15, PC0 ~ PC15, PD0 ~ PD15, PE0 ~ PE15 and PH0 ~ PH1 to implement logic input/output functions. Each of the GPIO ports has related control and configuration registers to satisfy the requirements of specific applications. The external interrupts on the GPIO pins of the device have related control and configuration registers in the Interrupt/event controller (EXTI). The GPIO ports are pin-shared with other alternative functions (AFs) to obtain maximum flexibility on the package pins. Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current capable except for analog inputs.

3.10. Timers and PWM generation

- Two 16-bit advanced timer (TIMER0 & TIMER7), eight 16-bit general timers (TIMER2, TIMER3, TIMER8 ~ TIMER13), two 32-bit general timers (TIMER1 & TIMER4) and two 16-bit basic timer (TIMER5 & TIMER6)
- Up to 4 independent channels of PWM, output compare or input capture for each general timer and external trigger input
- 16-bit, motor control PWM advanced timer with programmable dead-time generation for output match
- Encoder interface controller with two inputs using quadrature decoder
- 24-bit SysTick timer down counter
- 2 watchdog timers (free watchdog timer and window watchdog timer)

The advanced timer (TIMER0 & TIMER7) can be used as a three-phase PWM multiplexed on 6 channels. It has complementary PWM outputs with programmable dead-time generation. It can also be used as a complete general timer. The 4 independent channels can be used for input capture, output compare, PWM generation (edge-aligned or center-aligned counting modes) and single pulse mode output. If configured as a general 16-bit timer, it has the same functions as the TIMERx timer. It can be synchronized with external signals or to interconnect with other general timers together which have the same architecture and features.

The general timer, can be used for a variety of purposes including general timer, input signal pulse width measurement or output waveform generation such as a single pulse generation or PWM output, up to 4 independent channels for input capture/output compare. TIMER1 & TIMER4 is based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler. TIMER2 & TIMER3 is based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. TIMER8 ~ TIMER13 is based on a 16-bit auto-reload upcounter and a 16-bit prescaler. The general timer

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also supports an encoder interface with two inputs using quadrature decoder.

The basic timer, known as TIMER5 & TIMER6, are mainly used for DAC trigger generation. They can also be used as a simple 16-bit time base.

The GD32F460xx have two watchdog peripherals, free watchdog timer and window watchdog timer. They offer a combination of high safety level, flexibility of use and timing accuracy.

The free watchdog timer includes a 12-bit down-counting counter and an 8-bit prescaler. It is clocked from an independent 32 KHz internal RC and as it operates independently of the main clock, it can operate in deep-sleep and standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management.

The window watchdog timer is based on a 7-bit down counter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early wakeup interrupt capability and the counter can be frozen in debug mode.

The SysTick timer is dedicated for OS, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Auto reload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

3.11. Real time clock (RTC) and backup registers

- Independent binary-coded decimal (BCD) format timer/counter with twenty 32-bit backup registers.
- Calendar with sub-second, seconds, minutes, hours, week day, date, year and month automatically correction
- Alarm function with wake up from deep-sleep and standby mode capability
- On-the-fly correction for synchronization with master clock. Digital calibration with 1 ppm resolution for compensation of quartz crystal inaccuracy.

The real time clock is an independent timer which provides a set of continuously running counters in backup registers to provide a real calendar function, and provides an alarm interrupt or an expected interrupt. It is not reset by a system or power reset, or when the device wakes up from standby mode. A prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 KHz from external crystal oscillator.

3.12. Inter-integrated circuit (I2C)

- Up to three I2C bus interfaces can support both master and slave mode with a frequency

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up to 400 KHz (Fast mode)

- Provide arbitration function, optional PEC (packet error checking) generation and checking
- Supports 7-bit and 10-bit addressing mode and general call addressing mode

The I2C interface is an internal circuit allowing communication with an external I2C interface which is an industry standard two line serial interface used for connection to external hardware. These two serial lines are known as a serial data line (SDA) and a serial clock line (SCL). The I2C module provides transfer rate of up to 100 KHz in standard mode and up to 400 KHz in fast mode. The I2C module also has an arbitration detect function to prevent the situation where more than one master attempts to transmit data to the I2C bus at the same time. A CRC-8 calculator is also provided in I2C interface to perform packet error checking for I2C data.

3.13. Serial peripheral interface (SPI)

- Master or slave operation with full-duplex or simplex mode
- Support both master and slave mode
- Hardware CRC calculation and transmit automatic CRC error checking

The SPI interface uses 4 pins, among which are the serial data input and output lines (MISO & MOSI), the clock line (SCK) and the slave select line (NSS). Both SPIs can be served by the DMA controller. The SPI interface may be used for a variety of purposes, including simplex synchronous transfers on two lines with a possible bidirectional data line or reliable communication using CRC checking.

3.14. Universal synchronous/asynchronous receiver transmitter (USART/UART)

- Maximum speed up to 15MBit/s for USART0 and USART5
- Maximum speed up to 7.5MBit/s for USART1, USART2, UART3, UART4, UART6 and UART7
- Supports both asynchronous and clocked synchronous serial communication modes
- IrDA SIR encoder and decoder support
- LIN break generation and detection
- ISO 7816-3 compliant smart card interface

The USART (USART0, USART1, USART2, USART5) and UART (UART3, UART4, UART6, UART7) are used to transfer data between serial interfaces, provides a flexible full duplex data exchange using synchronous or asynchronous transfer. It is also commonly used for RS-232 standard communication. The USART/UART includes a programmable baud rate generator which is capable of dividing the system clock to produce a dedicated clock for the USART/UART transmitter and receiver. The USART/UART also supports DMA function for high speed data communication.

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3.15. Inter-IC sound (I2S)

- Two I2S bus Interfaces with sampling frequency from 8 KHz to 192 KHz, multiplexed with SPI1 and SPI2
- Support either master or slave mode Audio
- Sampling frequencies from 8 KHz up to 192 KHz are supported

The Inter-IC sound (I2S) bus provides a standard communication interface for digital audio applications by 4-wire serial lines. GD32F460xx contain an I2S-bus interface that can be operated with 16/32 bit resolution in master or slave mode, pin multiplexed with SPI1 and SPI2. The audio sampling frequencies from 8 KHz to 192 KHz is supported.

3.16. Universal serial bus full-speed interface (USBFS)

- One USB device/host/OTG full-speed Interface with frequency up to 12 Mbit/s
- Internal 48 MHz oscillator support crystal-less operation
- Internal main PLL for USB CLK compliantly
- Internal USBFS PHY support

The Universal Serial Bus (USB) is a 4-wire bus with 4 bidirectional endpoints. The device controller enables 12 Mbit/s data exchange with integrated transceivers. Transaction formatting is performed by the hardware, including CRC generation and checking. It supports both host and device modes, as well as OTG mode with Host Negotiation Protocol (HNP) and Session Request Protocol (SRP). The controller contains a full-speed USB PHY internal. For full-speed or low-speed operation, no more external PHY chip is needed. It supports all the four types of transfer (control, bulk, Interrupt and isochronous) defined in USB 2.0 protocol. The required precise 48 MHz clock which can be generated from the internal main PLL (the clock source must use an HXTAL crystal oscillator) or by the internal 48 MHz oscillator in automatic trimming mode that allows crystal-less operation.

3.17. Universal serial bus high-speed interface (USBHS)

- One USB device/host/OTG high-speed Interface with frequency up to 480 Mbit/s
- An external PHY device connected to the ULPI is required when using in HS mode

USBHS supports both host and device modes, as well as OTG mode with Host Negotiation Protocol (HNP) and Session Request Protocol (SRP). The controller provides ULPI interface for external USB PHY integration and it also contains a full-speed USB PHY internal. For full-speed or low-speed operation, no more external PHY chip is needed. It supports all the four types of transfer (control, bulk, Interrupt and isochronous) defined in USB 2.0 protocol. HUB connection is supported when USBHS operates at high-speed in host mode. There is also a DMA engine operating as an AHB bus master in USBHS to speed up the data transfer between USBHS and system.

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3.18. Controller area network (CAN)

- Two CAN2.0B interface with communication frequency up to 1 Mbit/s
- Internal main PLL for CAN CLK compliantly

Controller area network (CAN) is a method for enabling serial communication in field bus. The CAN protocol has been used extensively in industrial automation and automotive applications. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. Each CAN has three mailboxes for transmission and two FIFOs of three message deep for reception. It also provides 28 scalable/configurable identifier filter banks for selecting the incoming messages needed and discarding the others.

3.19. Ethernet (ENET)

- IEEE 802.3 compliant media access controller (MAC) for Ethernet LAN
- 10/100 Mbit/s rates with dedicated DMA controller and SRAM
- Support hardware precision time protocol (PTP) with conformity to IEEE 1588

The Ethernet media access controller (MAC) conforms to IEEE 802.3 specifications and fully supports IEEE 1588 standards. The embedded MAC provides the interface to the required external network physical interface (PHY) for LAN bus connection via an internal media independent interface (MII) or a reduced media independent interface (RMII). The number of MII signals provided up to 16 with 25 MHz output and RMII up to 7 with 50 MHz output. The function of 32-bit CRC checking is also available.

3.20. External memory controller (EXMC)

- Supported external memory: SRAM, PSRAM, ROM and NOR-Flash, NAND Flash and CF card with up to 32-bit data bus
- Provide ECC calculating hardware module for NAND Flash memory block

External memory controller (EXMC) is an abbreviation of external memory controller. It is divided in to several sub-banks for external device support, each sub-bank has its own chip selection signal but at one time, only one bank can be accessed. The EXMC supports code execution from external memory except NAND Flash and CF card. The EXMC also can be configured to interface with the most common LCD module of Motorola 6800 and Intel 8080 series and reduce the system cost and complexity.

3.21. Secure digital input and output card interface (SDIO)

- Support SD2.0/SDIO2.0/MMC4.2 host interface

The Secure Digital Input and Output Card Interface (SDIO) provides access to external SD memory cards specifications version 2.0, SDIO card specification version 2.0 and multi-media

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card system specification version 4.2 with DMA supported. In addition, this interface is also compliant with CE-ATA digital protocol rev1.1.

3.22. TFT LCD interface (TLI)

- 24-bit RGB Parallel Pixel Output; 8 bits-per-pixel (RGB888)
- Supports up to XVGA (1024x768) resolution
- 2 display layers with dedicated FIFO (64x32-bit)

The TFT LCD interface provides a parallel digital RGB (Red, Green and Blue) and signals for horizontal, vertical synchronization, Pixel Clock and Data Enable as output to interface directly to a variety of LCD (Liquid Crystal Display) and TFT (Thin Film Transistor) panels. A built-in DMA engine continuously move data from system memory to TLI and then, output to an external LCD display. Two separate layers are supported in TLI, as well as layer window and blending function.

3.23. Image processing accelerator (IPA)

- Copy one source image to the destination image
- Convert one source image to the destination image with specific pixel format
- Convert and blend two source images to the destination image with specific pixel format
- Fill up the destination image with a specific color

The Image processing accelerator (IPA) provides a configurable and flexible image format conversion from one or two source image to the destination image. Eleven pixel formats from 4-bit up to 32-bit per pixel independently for the two source images and five pixel formats from 16-bit up to 32-bit per pixel for the destination image are supported. Two 256*32 bits Look-Up Tables (LUT) separately for the two source images are implemented for the indirect pixel formats.

3.24. Digital camera interface (DCI)

- Digital video/picture capture
- 8/10/12/14 data width supported
- High transfer efficiency with DMA interface
- Video/picture crop supported
- Various pixel formats supported including JPEG/YCrCb/RGB
- Hard/embedded synchronous signals supported

DCI is an 8-bit to 14-bit parallel interface that able to capture video or picture from a camera via Digital Camera Interface. It supports 8/10/12/14 bits data width through DMA operation.

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3.25. Debug mode

- Serial wire JTAG debug port (SWJ-DP)

The Arm® SWJ-DP Interface is embedded and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

3.26. Package and operation temperature

- LQFP100(GD32F460Vx), LQFP64(GD32F460Rx)
- Operation temperature range: -40°C to +105°C

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4. Electrical characteristics

4.1. Absolute maximum ratings

The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 4-1. Absolute maximum ratings(1)(4)

Symbol	Parameter	Min	Max	Unit
V_{DD}	External voltage range(2)	V_{SS} - 0.3	V_{SS} + 3.6	V
V_{DDA}	External analog supply voltage	V_{SSA} - 0.3	V_{SSA} + 3.6	V
V_{BAT}	External battery supply voltage	V_{SS} - 0.3	V_{SS} + 3.6	V
V_{IN}	Input voltage on 5V tolerant pin(3)	V_{SS} - 0.3	V_{DD} + 3.6	V
	Input voltage on other I/O	V_{SS} - 0.3	3.6	V
$\|\Delta V_{DDX}\|$	Variations between different VDD power pins	—	50	mV
$\|V_{SSX} - V_{SS}\|$	Variations between different ground pins	—	50	mV
I_{IO}	Maximum current for GPIO pins	—	±25	mA
T_A	Operating temperature range for grade 7 device	-40	+105	°C
P_D	Power dissipation at T_A = 105°C of LQFP100	—	348	mW
	Power dissipation at T_A = 105°C of LQFP64	—	386	
T_{STG}	Storage temperature range	-65	+150	°C
T_J	Maximum junction temperature	—	125	°C

(1) Guaranteed by design, not tested in production.

(2) All main power and ground pins should be connected to an external power source within the allowable range.

(3) V_{IN} maximum value cannot exceed 5.5 V.

(4) It is recommended that V_{DD} and V_{DDA} are powered by the same source. The maximum difference between V_{DD} and V_{DDA} does not exceed 300 mV during power-up and operation.

4.2. Recommended DC characteristics

Table 4-2. DC operating conditions

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
V_{DD}	Supply voltage	—	2.6	3.3	3.6	V
V_{DDA}	Analog supply voltage	Same as V_{DD}	2.6	3.3	3.6	V
V_{BAT}	Battery supply voltage	—	1.8(2)	—	3.6	V

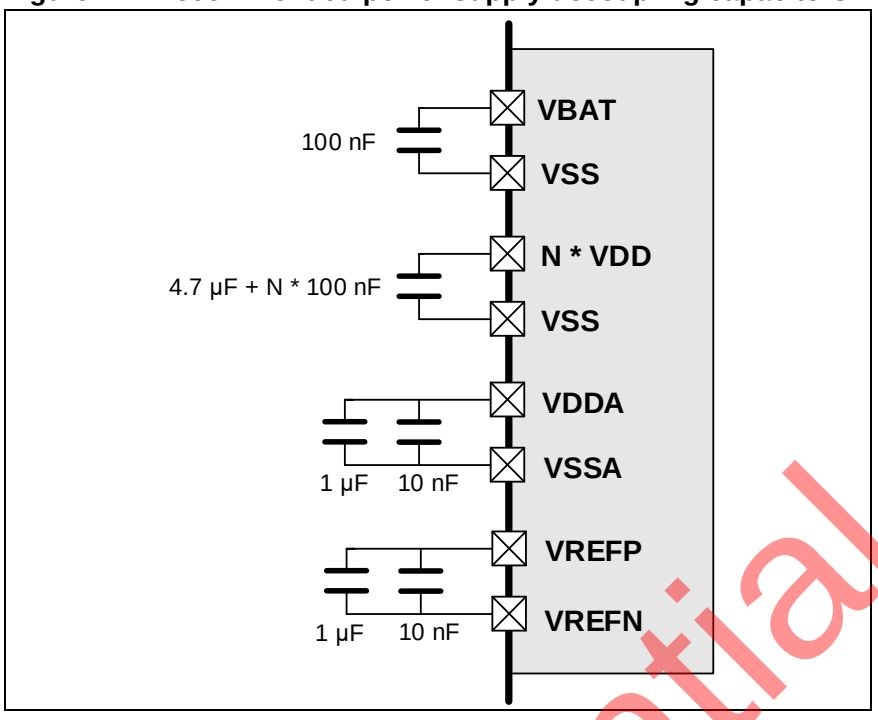
(1) Based on characterization, not tested in production.

(2) In the application which VBAT supply the backup domains, if the VBAT voltage drops below the minimum value, when V_{DD} is powered on again, it is necessary to refresh the registers of backup domains and enable LXTAL again.

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Figure 4-1. Recommended power supply decoupling capacitors(1)(2)



(1) The VREFP and VREFN pins are only available on no less than 100-pin packages, or else the VREFP and VREFN pins are not available and internally connected to VDDA and VSSA pins.

(2) All decoupling capacitors need to be as close as possible to the pins on the PCB board.

Table 4-3. Clock frequency(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	AHB clock frequency	—	—	240	MHz
f_{APB1}	APB1 clock frequency	—	—	60	MHz
f_{APB2}	APB2 clock frequency	—	—	120	MHz

(1) Guaranteed by design, not tested in production.

Table 4-4. Operating conditions at Power up / Power down(1)

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	—	0	∞	µs/V
	V_{DD} fall time rate		20	∞	

(1) Guaranteed by design, not tested in production.

Table 4-5. Start-up timings of Operating conditions(1)(2)(3)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{start-up}$	Start-up time	Code area in FLASH = 512 kB	130	140	150	ms
		Code area in FLASH = 768 kB	190	203	215	

(1) Guaranteed by design, not tested in production.

(2) After power-up, the start-up time is the time between the rising edge of NRST high and the first I/O instruction conversion in SystemInit function.

(3) PLL is off.

Table 4-6. Power saving mode wakeup timings characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
t_{Sleep}(2)	Wakeup from Sleep mode	—	0.623	—	µs
$t_{Deep-sleep}$(2)	Wakeup from Deep-sleep mode（LDO On）	—	1.57	—	

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Symbol	Parameter		Min	Typ	Max	Unit
	Wakeup from Deep-sleep mode （LDO in low power mode）		—	1.57	—	
$t_{Standby}$(3)	Wakeup from Standby mode	Code area in FLASH = 512 kB	130	140	150	ms
		Code area in FLASH = 768 kB	190	203	215	

(1) The wakeup time is measured from the wakeup event to the point at which the application code reads the first instruction under the below conditions: V_{DD} = V_{DDA} = 3.3 V, IRC16M = System clock = 16 MHz.

(2) Based on characterization, not tested in production.

(3) Guaranteed by design, not tested in production.

4.3. Power consumption

The power measurements specified in the tables represent that code with data executing from on-chip Flash with the following specifications.

Table 4-7. Power consumption characteristics(2)(3)(4)(5)(6)

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Unit
I_{DD}+I_{DDA}	Supply current (Run mode)	V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 240 MHz, All peripherals enabled	—	73.5	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 240 MHz, All peripherals disabled	—	44.1	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 200 MHz, All peripherals enabled	—	61.5	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 200 MHz, All peripherals disabled	—	37.1	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 180 MHz, All peripherals enabled	—	55.9	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 180 MHz, All peripherals disabled	—	33.9	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 168 MHz, All peripherals enabled	—	52.6	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 168 MHz, All peripherals disabled	—	32.0	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 120 MHz, All peripherals enabled	—	38.6	—	mA

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Symbol	Parameter	Conditions	Min	Typ(1)	Max	Unit
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 120 MHz, All peripherals disabled	—	23.9	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 108 MHz, All peripherals enabled	—	35.2	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 108 MHz, All peripherals disabled	—	22.0	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 90 MHz, All peripherals enabled	—	29.9	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 90 MHz, All peripherals disabled	—	19.0	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 60 MHz, All peripherals enabled	—	21.2	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 60 MHz, All peripherals disabled	—	13.9	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 30 MHz, All peripherals enabled	—	13.3	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 30 MHz, All peripherals disabled	—	9.5	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 25 MHz, All peripherals enabled	—	11.7	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 25 MHz, All peripherals disabled	—	8.5	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 16 MHz, All peripherals enabled	—	8.9	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 16 MHz, All peripherals disabled	—	6.9	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 8 MHz, All peripherals enabled	—	6.4	—	mA

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Symbol	Parameter	Conditions	Min	Typ(1)	Max	Unit
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 8 MHz, All peripherals disabled	—	5.3	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 4 MHz, All peripherals enabled	—	5.0	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 4 MHz, All peripherals disabled	—	4.5	—	mA
	Supply current (Sleep mode)	V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 240 MHz,CPU clock off, All peripherals enabled	—	50.0	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 240 MHz, CPU clock off, All peripherals disabled	—	21.7	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 200 MHz,CPU clock off, All peripherals enabled	—	42.2	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 200 MHz, CPU clock off, All peripherals disabled	—	18.7	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 180 MHz, CPU clock off, All peripherals enabled	—	38.5	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 180 MHz, CPU clock off, All peripherals disabled	—	17.2	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 168 MHz, CPU clock off, All peripherals enabled	—	36.2	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 168 MHz, CPU clock off, All peripherals disabled	—	16.4	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 120 MHz, CPU clock off, All peripherals enabled	—	27.0	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 120 MHz, CPU clock off, All peripherals disabled	—	12.8	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 108 MHz, CPU clock off, All peripherals enabled	—	24.7	—	mA

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Symbol	Parameter	Conditions	Min	Typ(1)	Max	Unit
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 108 MHz, CPU clock off, All peripherals disabled	—	11.9	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 90 MHz, CPU clock off, All peripherals enabled	—	21.2	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 90 MHz, CPU clock off, All peripherals disabled	—	10.5	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 60 MHz, CPU clock off, All peripherals enabled	—	15.5	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 60 MHz, CPU clock off, All peripherals disabled	—	8.4	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 30 MHz, CPU clock off, All peripherals enabled	—	10.5	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 30 MHz, CPU clock off, All peripherals disabled	—	6.7	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 25 MHz, CPU clock off, All peripherals enabled	—	9.4	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 25 MHz, CPU clock off, All peripherals disabled	—	6.2	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 16 MHz, CPU clock off, All peripherals enabled	—	7.4	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 16 MHz, CPU clock off, All peripherals disabled	—	5.4	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 8 MHz, CPU clock off, All peripherals enabled	—	5.7	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 8 MHz, CPU clock off, All peripherals disabled	—	4.7	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 4 MHz, CPU clock off, All peripherals enabled	—	4.8	—	mA

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Symbol	Parameter	Conditions	Min	Typ(1)	Max	Unit
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 4 MHz, CPU clock off, All peripherals disabled	—	4.3	—	mA
	Supply current (Deep-Sleep mode)	V_{DD} = V_{DDA} = 3.3 V, LDO in run mode and normal driver mode, IRC32K off, RTC off	—	1.39	—	mA
		V_{DD} = V_{DDA} = 3.3 V, LDO in low power mode and normal driver mode, IRC32K off	—	1.36	11	mA
		V_{DD} = V_{DDA} = 3.3 V, LDO in run mode and low driver mode, IRC32K off, RTC off	—	1.33	—	mA
		V_{DD} = V_{DDA} = 3.3 V, LDO in low power mode and low driver mode, IRC32K off	—	1.30	—	mA
	Supply current (Standby mode)	V_{DD} = V_{DDA} = 3.3 V, LXTAL off, IRC32K on, RTC on, backup SRAM LDO ON	—	9.90	17.5	μA
		V_{DD} = V_{DDA} = 3.3 V, LXTAL off, IRC32K on, RTC off, backup SRAM LDO ON	—	9.67	17.3	μA
		V_{DD} = V_{DDA} = 3.3 V, LXTAL off, IRC32K off, RTC off, backup SRAM LDO ON	—	9.19	16.8	μA
		V_{DD} = V_{DDA} = 3.3 V, LXTAL off, IRC32K off, RTC off, backup SRAM LDO OFF	—	3.379	11	μA
I_{BAT}	Battery supply current (Backup mode)	V_{DD} off, V_{DDA} off, V_{BAT}=3.6V, LXTAL on with external crystal, RTC on, LXTAL High driving, backup SRAM LDO ON	—	9.09	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} =3.3V, LXTAL on with external crystal, RTC on, LXTAL High driving, backup SRAM LDO ON	—	8.93	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} =2.6V, LXTAL on with external crystal, RTC on, LXTAL High driving, backup SRAM LDO ON	—	8.74	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} =1.8V, LXTAL on with external crystal, RTC on, LXTAL High driving, backup SRAM LDO ON	—	7.47	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} =3.6V, LXTAL on with external crystal, RTC on, LXTAL High driving, backup SRAM LDO OFF	—	2.23	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} =3.3V, LXTAL on with external crystal, RTC on, LXTAL High driving, backup SRAM LDO OFF	—	2.13	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} =2.6V, LXTAL on with external crystal, RTC on, LXTAL High driving, backup SRAM LDO OFF	—	2	—	μA

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Symbol	Parameter	Conditions	Min	Typ(1)	Max	Unit
		V_{DD} off, V_{DDA} off, V_{BAT} =1.8V, LXTAL on with external crystal, RTC on, LXTAL High driving, backup SRAM LDO OFF	—	1.89	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} =3.6V, LXTAL on with external crystal, RTC on, LXTAL Low driving, backup SRAM LDO ON	—	8.16	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} =3.3V, LXTAL on with external crystal, RTC on, LXTAL Low driving, backup SRAM LDO ON	—	8	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} =2.6V, LXTAL on with external crystal, RTC on, LXTAL Low driving, backup SRAM LDO ON	—	7.8	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} =1.8V, LXTAL on with external crystal, RTC on, LXTAL Low driving, backup SRAM LDO ON	—	6.7	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} =3.6V, LXTAL on with external crystal, RTC on, LXTAL Low driving, backup SRAM LDO OFF	—	1.27	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} =3.3V, LXTAL on with external crystal, RTC on, LXTAL Low driving, backup SRAM LDO OFF	—	1.18	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} =2.6V, LXTAL on with external crystal, RTC on, LXTAL Low driving, backup SRAM LDO OFF	—	1.06	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} =1.8V, LXTAL on with external crystal, RTC on, LXTAL Low driving, backup SRAM LDO OFF	—	0.96	—	μA

(1) Based on characterization, not tested in production.

(2) Unless otherwise specified, all values given for T_A = 25 ℃ and test result is mean value.

(3) When System Clock is less than 4 MHz, an external source is used, and the HXTAL bypass function is needed, no PLL.

(4) When System Clock is greater than 8 MHz, a crystal 8 MHz is used, and the HXTAL bypass function is closed, using PLL.

(5) When analog peripheral blocks such as ADCs, DACs, HXTAL, LXTAL, IRC16M, or IRC32K are ON, an additional power consumption should be considered.

(6) All GPIOs are configured as analog mode except standby mode.

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Figure 4-2. Typical supply current consumption in Run mode

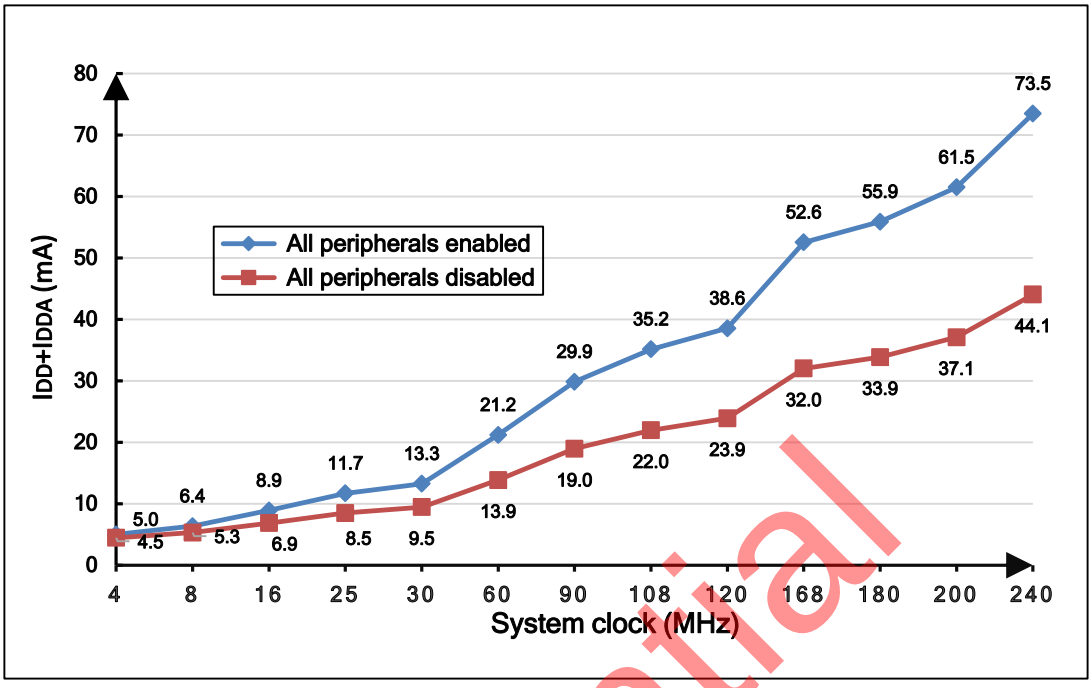
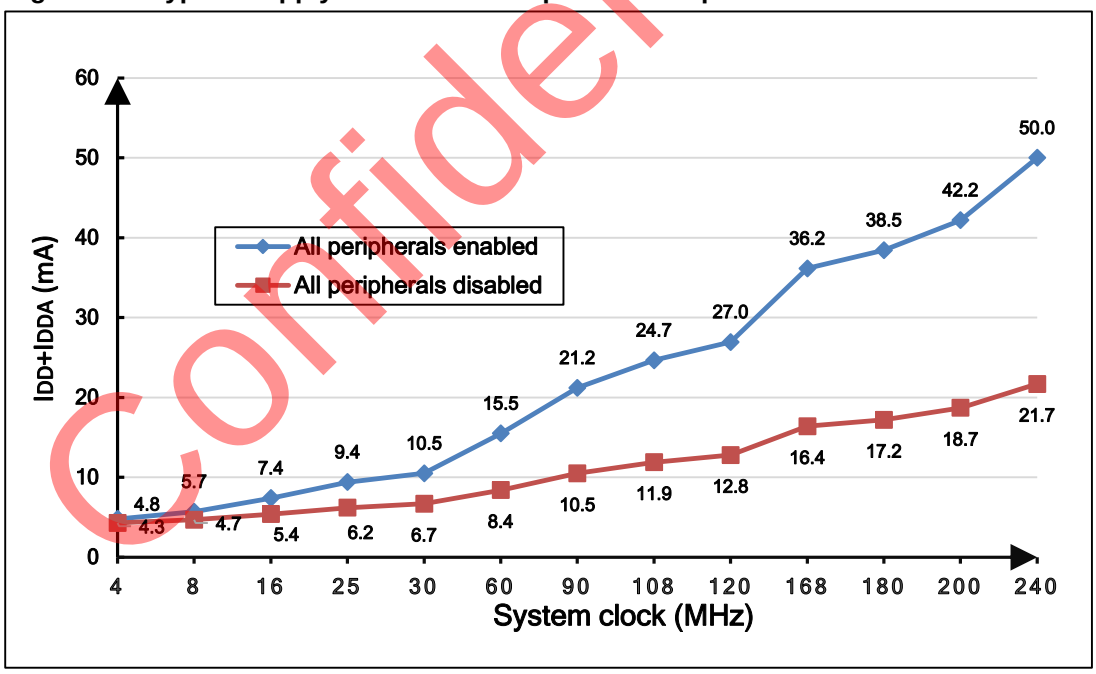


Figure 4-3. Typical supply current consumption in Sleep mode



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4.4. EMC characteristics

System level ESD (Electrostatic discharge, according to IEC 61000-4-2) and EFT (Electrical Fast Transient/burst, according to IEC 61000-4-4) testing result is given in the ***Table 4-8. EMS characteristics***[1]. System level ESD is for end-customer operation, it includes ESD field events on system level occur in an unprotected area (outside EPA). System level ESD protection necessary to satisfy higher ESD levels.

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Table 4-8. EMS characteristics(1)

Symbol	Parameter	Conditions	Package	Class	Level
V_{ESD}	Contact / Air mode high voltage stressed on few special I/O pins	V_{DD} = 3.3 V, T_A = 25 °C f_{HCLK} = 240 MHz conforms to IEC 61000-4-2	LQFP100	CD 8kV AD 15kV	4A
V_{EFT}	Fast transient high voltage burst stressed on Power and GND	V_{DD} = 3.3 V, T_A = 25 °C f_{HCLK} = 240 MHz conforms to IEC 61000-4-4	LQFP100	4kV	4A

(1) Based on characterization, not tested in production.

EMI (Electromagnetic Interference) emission test result is given in the ***Table 4-9. EMI characteristics***(1), The electromagnetic field emitted by the device are monitored while an application, executing EEMBC code, is running. The test is compliant with SAE J1752-3:2017 standard which specifies the test board and the pin loading.

Table 4-9. EMI characteristics(1)

Symbol	Parameter	Conditions	Tested frequency band	Max vs. [f_{HXTAL}/f_{HCLK}] 25/240 MHz	Unit
S_{EMI}	Peak level	V_{DD} = 3.6 V, T_A = +25 °C, LQFP100, f_{HCLK} = 240 MHz, conforms to SAE J1752-3:2017	0.15 MHz to 30 MHz	-0.43	dBµV
			30 MHz to 130 MHz	6.56	
			130 MHz to 1 GHz	9.87	

(1) Based on characterization, not tested in production.

Component level ESD include HBM (Human body model, according to ANSI/ESDA/JEDEC JS-001) and CDM (ANSI/ESDA/JEDEC JS-002), that ESD field events during manufacturing in an ESD protected area, such as PCB assembly/repair, IC assembly/test and Fab environment. The ESD protected area (EPA) has many measures, for instance ESD protective packaging, grounding person wrist strap to ground (or flooring/footwear), grounded work surface and ionizer.

Static latch-up (LU, according to JEDEC78) test is based on the two measurement methods, I/O current injection value (I-test) and power supply over-voltage value.

Table 4-10. Component level ESD and latch-up characteristics(1)

Symbol	Description	Conditions	Package	Max	Unit	Level
V_{HBM}	Human body model electrostatic discharge voltage (Any pin combination)	T_A = 25 °C; JS-001-2017	LQFP100	5000	V	3A
V_{CDM}	Charge device model electrostatic discharge voltage (All pins)	T_A = 25 °C; JS-002-2018	LQFP100	1000	V	C3
LU	I-test	T_A = 125 °C, JESD78F	LQFP100	200	mA	Class II Level A
	V_{supply} over voltage			5.4	V	

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(1) Based on characterization, not tested in production.

4.5. Power supply supervisor characteristics

Table 4-11. Power supply supervisor characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{LVD}(1)	Low voltage Detector level selection	LVDT<2:0> = 000(rising edge)	—	2.1	—	V
		LVDT<2:0> = 000(falling edge)	—	1.98	—	
		LVDT<2:0> = 001(rising edge)	—	2.23	—	
		LVDT<2:0> = 001(falling edge)	—	2.12	—	
		LVDT<2:0> = 010(rising edge)	—	2.36	—	
		LVDT<2:0> = 010(falling edge)	—	2.25	—	
		LVDT<2:0> = 011(rising edge)	—	2.50	—	
		LVDT<2:0> = 011(falling edge)	—	2.38	—	
		LVDT<2:0> = 100(rising edge)	—	2.62	—	
		LVDT<2:0> = 100(falling edge)	—	2.52	—	
		LVDT<2:0> = 101(rising edge)	—	2.74	—	
		LVDT<2:0> = 101(falling edge)	—	2.66	—	
		LVDT<2:0> = 110(rising edge)	—	2.90	—	
		LVDT<2:0> = 110(falling edge)	—	2.80	—	
		LVDT<2:0> = 111(rising edge)	—	3.03	—	
		LVDT<2:0> = 111(falling edge)	—	2.93	—	
$V_{LVDhyst}$(2)	LVD hystersis	—	—	100	—	mV
V_{POR}(1)	Power on reset threshold	—	—	2.45	—	V
V_{PDR}(1)	Power down reset threshold	—	—	1.82	—	V
$V_{PDRhyst}$(2)	PDR hysteresis	—	—	600	—	mV
V_{BOR3}(1)	Brownout level 3 threshold	Falling edge	—	2.80	—	V
		Rising edge	—	2.89	—	V
V_{BOR2}(1)	Brownout level 2 threshold	Falling edge	—	2.51	—	V
		Rising edge	—	2.59	—	V
V_{BOR1}(1)	Brownout level 1 threshold	Falling edge	—	2.20	—	V
		Rising edge	—	2.30	—	V

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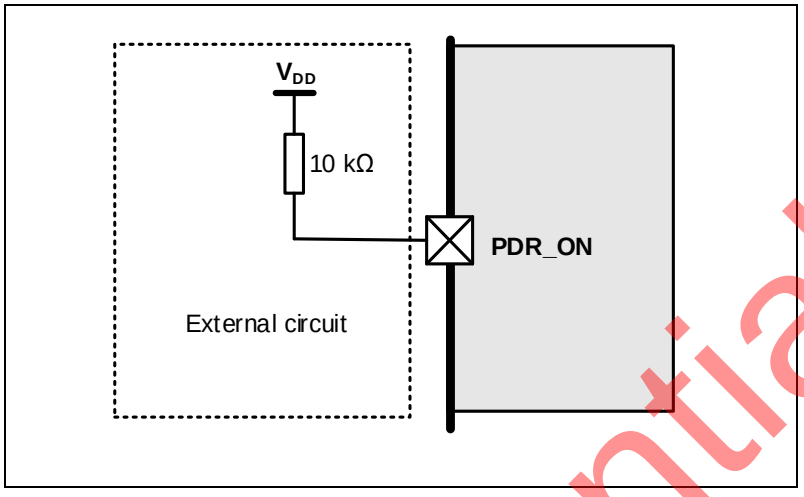
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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{BORhyst}$(2)	BOR hysteresis	—	—	100	—	mV
$t_{RSTTEMPO}$(2)	Reset temporization	—	—	2	—	ms

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

Figure 4-4. Recommended PDR_ON pin circuit



(1) The PDR supervisor can be enabled/disabled through PDR_ON pin.

(2) When PDR_ON pin is connected to VSS (Internal Reset OFF), the VBAT functionality is no more available and VBAT pin should be connected to VDD.

4.6. External clock characteristics

Table 4-12. High speed external clock (HXTAL) generated from a crystal/ceramic characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HXTAL}(1)	Crystal or ceramic frequency	2.6 V ≤V_{DD} ≤ 3.6 V	4	25	32	MHz
R_F(2)	Feedback resistor	V_{DD} = 3.3 V	—	400	—	kΩ
C_{HXTAL}(2) (3)	Recommended matching capacitance on OSCIN and OSCOUT	—	—	20	30	pF
$Ducy_{(HXTAL)}$(2)	Crystal or ceramic duty cycle	—	30	50	70	%
g_m(2)	Oscillator transconductance	Startup	—	25	—	mA/V
$I_{DDHXTAL}$(1)	Crystal or ceramic operating current	V_{DD} = 3.3 V	—	1.2	—	mA
$t_{SUHXTAL}$(1)	Crystal or ceramic startup time	V_{DD} = 3.3 V	—	0.42	—	ms

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

(3) $C_{HXTAL1} = C_{HXTAL2} = 2*(C_{LOAD} - C_S)$, For C_{HXTAL1} and C_{HXTAL2}, it is recommended matching capacitance on OSCIN and OSCOUT. For C_{LOAD}, it is crystal/ceramic load capacitance, provided by the crystal or ceramic manufacturer. For C_S, it is PCB and MCU pin stray capacitance.

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Table 4-13. High speed external clock characteristics (HXTAL in bypass mode)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HXTAL_ext}(1)	External clock source or oscillator frequency	2.6 V ≤V_{DD} ≤ 3.6 V	1	—	50	MHz
V_{HXTALH}(2)	OSCIN input pin high level voltage	V_{DD} = 3.3 V	0.7 V_{DD}	—	V_{DD}	V
V_{HXTALL}(2)	OSCIN input pin low level voltage		V_{SS}	—	0.3 V_{DD}	V
$t_{H/L(HXTAL)}$ (2)	OSCIN high or low time	—	5	—	—	ns
$t_{R/F(HXTAL)}$ (2)	OSCIN rise or fall time	—	—	—	10	ns
C_{IN}(2)	OSCIN input capacitance	—	—	5	—	pF
$Ducy_{(HXTAL)}$ (2)	Duty cycle	—	40	—	60	%

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

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Table 4-14. Low speed external clock (LXTAL) generated from a crystal/ceramic characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LXTAL}(1)	Crystal or ceramic frequency	V_{DD} = 3.3 V	—	32.768	—	kHz
C_{LXTAL}(2) (3)	Recommended matching capacitance on OSC32IN and OSC32OUT	—	—	15	—	pF
$Ducy_{(LXTAL)}$(2)	Crystal or ceramic duty cycle	—	30	—	70	%
g_m(2)	Oscillator transconductance	Medium low driving capability	—	6	—	μA/V
		Higher driving capability	—	18	—	
$I_{DDLXTAL}$ (1)	Crystal or ceramic operating current	LXTALDRI= 0	—	0.8	—	μA
		LXTALDRI= 1	—	1.6	—	
$t_{SULXTAL}$(1) (4)	Crystal or ceramic startup time	LXTALDRI= 0	—	369	—	ms
		LXTALDRI= 1	—	175	—	ms

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

(3) $C_{LXTAL1} = C_{LXTAL2} = 2*(C_{LOAD} - C_S)$, For C_{LXTAL1} and C_{LXTAL2}, it is recommended matching capacitance on OSC32IN and OSC32OUT. For C_{LOAD}, it is crystal/ceramic load capacitance, provided by the crystal or ceramic manufacturer. For C_S, it is PCB and MCU pin stray capacitance.

(4) $t_{SULXTAL}$ is the startup time measured from the moment it is enabled (by software) to the 32.768 kHz oscillator stabilization flags is SET. This value varies significantly with the crystal manufacturer.

Table 4-15. Low speed external user clock characteristics (LXTAL in bypass mode)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LXTAL_ext}(1)	External clock source or oscillator frequency	V_{DD} = 3.3 V	—	32.768	1000	kHz
V_{LXTALH}(2)	OSC32IN input pin high level voltage	—	0.7 V_{DD}	—	V_{DD}	V
V_{LXTALL}(2)	OSC32IN input pin low level voltage	—	V_{SS}	—	0.3 V_{DD}	
$t_{H/L(LXTAL)}$ (2)	OSC32IN high or low time	—	450	—	—	ns
$t_{R/F(LXTAL)}$ (2)	OSC32IN rise or fall time	—	—	—	50	
C_{IN}(2)	OSC32IN input capacitance	—	—	5	—	pF
$Ducy_{(LXTAL)}$ (2)	Duty cycle	—	30	50	70	%

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

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4.7. Internal clock characteristics

Table 4-16. High speed internal clock (IRC16M) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{IRC16M}	High Speed Internal Oscillator (IRC16M) frequency	V_{DD} = V_{DDA} = 3.3 V	—	16	—	MHz
ACC_{IRC16M}	IRC16M oscillator Frequency accuracy, Factory-trimmed	V_{DD} = V_{DDA} = 3.3 V, T_A = -40 °C ~ +105 °C	—	-1.8 to 1.1 (1)	—	%
		V_{DD} = V_{DDA} = 3.3 V, T_A = 25 °C	-1.0	—	+1.0	
	IRC16M oscillator Frequency accuracy, User trimming step(1)	—	—	0.5	—	%
$Ducy_{IRC16M}$(2)	IRC16M oscillator duty cycle	V_{DD} = V_{DDA} = 3.3 V	45	50	55	%
$I_{DDIRC16M+}$ $I_{DDAIRC16M}$(1)	IRC16M oscillator operating current	V_{DD} = V_{DDA} = 3.3 V, f_{HCLK} =f_{HXTAL} = 25 MHz	—	47	—	μA
$t_{SUIRC16M}$(1)	IRC16M oscillator startup time	V_{DD} = V_{DDA} = 3.3 V, f_{HCLK} =f_{HXTAL_PLL} = 200 MHz	—	1.18	—	μs

(1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.

Table 4-17. High speed internal clock (IRC48M) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{IRC48M}	High Speed Internal Oscillator (IRC48M) frequency	VDD = 3.3 V	—	48	—	MHz
ACC_{IRC48M}	IRC48M oscillator Frequency accuracy, Factory-trimmed	V_{DD} = V_{DDA} = 3.3 V, T_A = -40 °C ~ +105 °C	—	-1.48 to 0.39 (1)	—	%
		V_{DD} = V_{DDA} = 3.3 V, T_A = 25 °C	-2.0	—	+2.0	
	IRC48M oscillator Frequency accuracy, User trimming step(1)	—	—	0.12	—	%
D_{IRC48M}(2)	IRC48M oscillator duty cycle	V_{DD} = V_{DDA} = 3.3 V	45	50	55	%
$I_{DDIRC48M+}$ $I_{DDAIRC48M}$(1)	IRC48M oscillator operating current	V_{DD} = V_{DDA} = 3.3 V, f_{HCLK} = f_{IRC16M} = 16 MHz	—	358	—	μA
$t_{SUIRC48M}$(1)	IRC48M oscillator startup time	V_{DD} = V_{DDA} = 3.3 V, f_{HCLK} = f_{HXTAL_PLL} = 200 MHz	—	1.23	—	μs

(1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.

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Table 4-18. Low speed internal clock (IRC32K) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{IRC32K}(1)	Low Speed Internal oscillator (IRC32K) frequency	V_{DD} = V_{DDA} = 3.3 V	—	32	—	kHz
$I_{DDAIRC32K}$(2)	IRC32K oscillator operating current	V_{DD} = V_{DDA} = 3.3 V, f_{HCLK} = f_{IRC16M} = 16 MHz	—	0.43	—	μA
$t_{SUIRC32K}$(2)	IRC32K oscillator startup time	V_{DD} = V_{DDA} = 3.3 V, f_{HCLK} = f_{HXTAL_PLL} = 200 MHz	—	22.1	—	μs

(1) Guaranteed by design, not tested in production.
(2) Based on characterization, not tested in production.

4.8. PLL characteristics

Table 4-19. PLL characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLLIN}(1)	PLL input clock frequency	—	1	—	4	MHz
f_{PLLOUT}(2)	PLL output clock frequency	—	32	—	250	MHz
f_{VCO}(2)	PLL VCO output clock frequency	—	64	—	500	MHz
t_{LOCK}(2)	PLL lock time	—	—	—	400	μs
I_{DDA}(1)(3)	Current consumption on V_{DDA}	VCO freq = 400 MHz	—	797	—	μA
$Jitter_{PLL}$	Cycle to cycle Jitter(rms)	System clock	—	40	—	ps
	Cycle to cycle Jitter（peak to peak）		—	400	—	

(1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.
(3) System clock = HXTAL = 25 MHz, PLL clock source = HXTAL/25 = 1 MHz, f_{PLLOUT} = 100 MHz.
(4) Value given with main PLL running.

Table 4-20. PLLI2S characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLLIN}(1)	PLLI2S input clock frequency	—	1	—	4	MHz
f_{PLLOUT}(2)	PLLI2S output clock frequency	—	32	—	250	MHz
f_{VCO}(2)	PLLI2S VCO output clock frequency	—	64	—	500	MHz
t_{LOCK}(2)	PLLI2S lock time	—	—	—	400	μs
I_{DDA}(1)(3)	Current consumption on V_{DDA}	VCO freq = 400 MHz	—	814	—	μA
$Jitter_{PLL}$	Cycle to cycle Jitter(rms)	System clock	—	40	—	ps
	Cycle to cycle Jitter（peak to peak）		—	400	—	

(1) Based on characterization, not tested in production.

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(2) Guaranteed by design, not tested in production.
(3) System clock = HXTAL = 25 MHz, PLL clock source = HXTAL/25 = 1 MHz, f_{PLLOUT} = 100 MHz.
(4) Value given with main PLLI2S running.

Table 4-21. PLLSAI characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLLIN}(1)	PLLSAI input clock frequency	—	1	—	4	MHz
f_{PLLOUT}(2)	PLLSAI output clock frequency	—	32	—	250	MHz
f_{VCO}(2)	PLLSAI VCO output clock frequency	—	64	—	500	MHz
t_{LOCK}(2)	PLLSAI lock time	—	—	—	400	μs
I_{DDA}(1)(3)	Current consumption on V_{DDA}	VCO freq = 400 MHz	—	796	—	μA
$Jitter_{PLL}$	Cycle to cycle Jitter(rms)	System clock	—	40	—	ps
	Cycle to cycle Jitter （peak to peak）		—	400	—	

(1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.
(3) System clock = HXTAL = 25 MHz, PLL clock source = HXTAL/25 = 1 MHz, f_{PLLOUT} = 100 MHz.
(4) Value given with main PLLSAI running.

Table 4-22. PLL spread spectrum clock generation (SSCG) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{MOD}	Modulation frequency	—	—	—	10	KHz
Mdamp	Peak modulation amplitude	—	—	—	2	%
MODCNT* MODSTEP	—	—	—	—	2^{15}-1	—

(1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.

Equation 1: SSCG configuration equation:

$$MODCNT = round(f_{PLLIN}/4/f_{mod})$$

$$MODSTEP = round(mdamp * PLLN * 2^{14}/(MODCNT * 100))$$

The formula above (Equation 1) is SSCG configuration equation.

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4.9. Memory characteristics

Table 4-23. Flash memory characteristics(1)

Symbol	Parameter	Conditions	Min(1)	Typ(1)	Max(1)	Unit
PE_{CYC}	Number of guaranteed program /erase cycles before failure (Endurance)	—	100	—	—	kcycles
t_{READ}	Read time at code flash area	—	—	1	—	hclks
	Read time at data flash area		56	—	4176	
t_{RET}	Data retention time	—	—	20	—	years
t_{PROG}	Word programming time	T_A range(2)	—	37.5	180	µs
$t_{ERASE16kB}$	Sector(16kB) erase time		—	200	2000	ms
$t_{ERASE64kB}$	Sector(64kB) erase time		—	300	4000	
$t_{ERASE128kB}$	Sector(128kB) erase time		—	600	8000	
$t_{MERASE(512K)}$	Mass erase time		—	2.4	32	s
$t_{MERASE(1MB)}$	Mass erase time		—	4.8	64	s

(1) Guaranteed by design and/or characterization, not 100% tested in production.

(2) For grade 6 devices, T_A range= -40°C ~ +85°C. For grade 7 devices, TA range= -40°C ~ +105°C.

4.10. NRST pin characteristics

Table 4-24. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST Input low level voltage	V_{DD} = V_{DDA} = 2.6 V	-0.3	—	0.3 V_{DD}	V
$V_{IH(NRST)}$(1)	NRST Input high level voltage		0.7 V_{DD}	—	V_{DD} + 0.3	
V_{hyst}(1)	Schmidt trigger Voltage hysteresis		—	440	—	mV
$V_{IL(NRST)}$(1)	NRST Input low level voltage	V_{DD} = V_{DDA} = 3.3 V	-0.3	—	0.3 V_{DD}	V
$V_{IH(NRST)}$(1)	NRST Input high level voltage		0.7 V_{DD}	—	V_{DD} + 0.3	
V_{hyst}(1)	Schmidt trigger Voltage hysteresis		—	490	—	mV
$V_{IL(NRST)}$(1)	NRST Input low level voltage	V_{DD} = V_{DDA} = 3.6 V	-0.3	—	0.3 V_{DD}	V
$V_{IH(NRST)}$(1)	NRST Input high level voltage		0.7 V_{DD}	—	V_{DD} + 0.3	
V_{hyst}(1)	Schmidt trigger Voltage hysteresis		—	510	—	mV
R_{pu}(2)	Pull-up equivalent resistor	—	—	40	—	kΩ

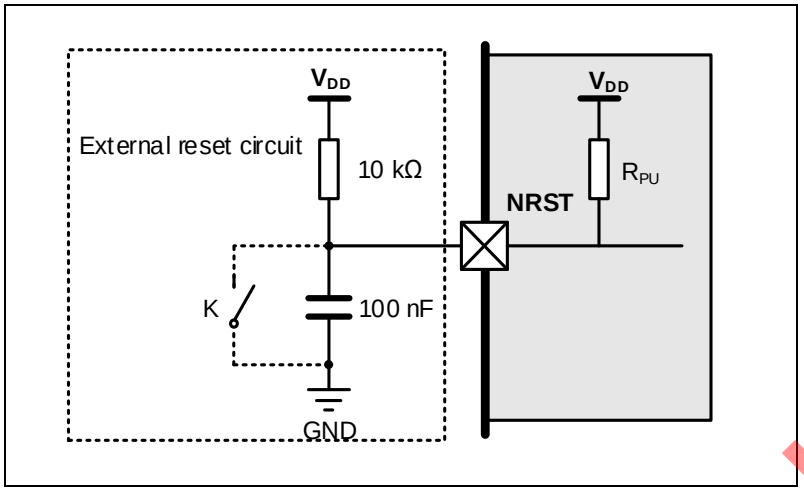
(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

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Figure 4-5. Recommended external NRST pin circuit(1)



(1) Unless the voltage on NRST pin go below $V_{IL(NRST)}$ level, the device would not generate a reliable reset.

4.11. GPIO characteristics

Table 4-25. I/O port DC characteristics(1)(3)

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
V_{IL}	Standard IO Low level input voltage		2.6 V ≤V_{DD} = V_{DDA} ≤ 3.6 V	—	—	0.3 V_{DD}	V
	5V-tolerant IO Low level input voltage		2.6 V ≤V_{DD} = V_{DDA} ≤ 3.6 V	—	—	0.3 V_{DD}	V
V_{IH}	Standard IO High level input voltage		2.6 V ≤V_{DD} = V_{DDA} ≤ 3.6 V	0.7 V_{DD}	—	—	V
	5V-tolerant IO High level input voltage		2.6 V ≤V_{DD} = V_{DDA} ≤ 3.6 V	0.7 V_{DD}	—	—	V
R_{PU}(2)	Internal pull-up resistor	All pins	V_{IN} = V_{SS}	—	40	—	kΩ
		PA10	—	—	10	—	
R_{PD}(2)	Internal pull-down resistor	All pins	V_{IN} = V_{DD}	—	40	—	kΩ
		PA10	—	—	10	—	
IO_Speed:level 3							
V_{OL}	Low level output voltage for an IO Pin (I_{IO} = +8 mA)		V_{DD} = 2.6 V	—	—	0.2	V
			V_{DD} = 3.3 V	—	—	0.2	
			V_{DD} = 3.6 V	—	—	0.2	
	Low level output voltage for an IO Pin (I_{IO} = +20 mA)		V_{DD} = 2.6 V	—	—	0.29	
			V_{DD} = 3.3 V	—	—	0.27	
			V_{DD} = 3.6 V	—	—	0.26	
V_{OH}	High level output voltage for an IO Pin (I_{IO} = +8 mA)		V_{DD} = 2.6 V	2.38	—	—	
			V_{DD} = 3.3 V	3.1	—	—	
			V_{DD} = 3.6 V	3.4	—	—	
	High level output voltage for an IO Pin		V_{DD} = 2.6 V	2.22	—	—	
			V_{DD} = 3.3 V	2.98	—	—	

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	(I_{IO} = +20 mA)	V_{DD} = 3.6 V	3.29	—	—	
IO_Speed:level 2						
V_{OL}	Low level output voltage for an IO Pin (I_{IO} = +8 mA)	V_{DD} = 2.6 V	—	—	0.25	V
		V_{DD} = 3.3 V	—	—	0.24	
		V_{DD} = 3.6 V	—	—	0.24	
	Low level output voltage for an IO Pin (I_{IO} = +20 mA)	V_{DD} = 2.6 V	—	—	0.43	
		V_{DD} = 3.3 V	—	—	0.37	
		V_{DD} = 3.6 V	—	—	0.36	
V_{OH}	High level output voltage for an IO Pin (I_{IO} = +8 mA)	V_{DD} = 2.6 V	2.32	—	—	
		V_{DD} = 3.3 V	3.04	—	—	
		V_{DD} = 3.6 V	3.36	—	—	
	High level output voltage for an IO Pin (I_{IO} = +20 mA)	V_{DD} = 2.6 V	2.05	—	—	
		V_{DD} = 3.3 V	2.84	—	—	
		V_{DD} = 3.6 V	3.17	—	—	
IO_Speed:level 1						
V_{OL}	Low level output voltage for an IO Pin (I_{IO} = +8 mA)	V_{DD} = 2.6 V	—	—	0.37	V
		V_{DD} = 3.3 V	—	—	0.38	
		V_{DD} = 3.6 V	—	—	0.34	
	(I_{IO} = +15 mA)	V_{DD} = 2.6 V	—	—	0.57	
	Low level output voltage for an IO Pin (I_{IO} = +20 mA)	V_{DD} = 3.3 V	—	—	0.66	
		V_{DD} = 3.6 V	—	—	0.64	
V_{OH}	High level output voltage for an IO Pin (I_{IO} = +8 mA)	V_{DD} = 2.6 V	2.15	—	—	
		V_{DD} = 3.3 V	2.92	—	—	
		V_{DD} = 3.6 V	3.23	—	—	
	(I_{IO} = +15 mA)	V_{DD} = 2.6 V	1.83	—	—	
	High level output voltage for an IO Pin (I_{IO} = +20 mA)	V_{DD} = 3.3 V	2.45	—	—	
		V_{DD} = 3.6 V	2.81	—	—	
IO_Speed:level 0						
V_{OL}	Low level output voltage for an IO Pin (I_{IO} = +1 mA)	V_{DD} = 2.6 V	—	—	0.17	V
		V_{DD} = 3.3 V	—	—	0.15	
		V_{DD} = 3.6 V	—	—	0.15	
	Low level output voltage for an IO Pin (I_{IO} = +4 mA)	V_{DD} = 2.6 V	—	—	0.80	
		V_{DD} = 3.3 V	—	—	0.63	
		V_{DD} = 3.6 V	—	—	0.60	
V_{OH}	High level output voltage for an IO Pin (I_{IO} = +1 mA)	V_{DD} = 2.6 V	2.38	—	—	
		V_{DD} = 3.3 V	3.12	—	—	
		V_{DD} = 3.6 V	3.42	—	—	
	High level output voltage for an IO Pin (I_{IO} = +4 mA)	V_{DD} = 2.6 V	1.45	—	—	
		V_{DD} = 3.3 V	2.48	—	—	
		V_{DD} = 3.6 V	2.83	—	—	

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(1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.
(3) All pins except PC13 / PC14 / PC15 / PI8. Since PC13 to PC15 and PI8 are supplied through the Power Switch, which can only be obtained by a small current, the speed of GPIOs PC13 to PC15 and PI8 should not exceed 2 MHz when they are in output mode (maximum load: 30 pF).

Table 4-26. I/O port AC characteristics(1)(2)(4)

GPIOx_OSPD[1:0] bit value(3)	Parameter	Conditions	Max	Unit
GPIOx_OSPD0->OSPDy[1:0] = 00 (IO_Speed:level 0)	T_{Rise}/T_{Fall}	2.6 ≤ V_{DD} ≤ 3.6 V, C_L = 10 pF	51	ns
		2.6 ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF	63.2	
		2.6 ≤ V_{DD} ≤ 3.6 V, C_L = 50 pF	74.2	
GPIOx_OSPD0->OSPDy[1:0] = 01 (IO_Speed:level 1)	T_{Rise}/T_{Fall}	2.6 ≤ V_{DD} ≤ 3.6 V, C_L = 10 pF	3.6	ns
		2.6 ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF	9.6	
		2.6 ≤ V_{DD} ≤ 3.6 V, C_L = 50 pF	12.2	
GPIOx_OSPD0->OSPDy[1:0] = 10 (IO_Speed: level 2)	T_{Rise}/T_{Fall}	2.6 ≤ V_{DD} ≤ 3.6 V, C_L = 10 pF	2.2	ns
		2.6 ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF	3	
		2.6 ≤ V_{DD} ≤ 3.6 V, C_L = 50 pF	3.8	
GPIOx_OSPD0->OSPDy[1:0] = 11 (IO_Speed:level 3)	T_{Rise}/T_{Fall}	2.6 ≤ V_{DD} ≤ 3.6 V, C_L = 10 pF	2	ns
		2.6 ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF	2.8	
		2.6 ≤ V_{DD} ≤ 3.6 V, C_L = 50 pF	3.4	

(1) Based on characterization, not tested in production.
(2) Unless otherwise specified, all test results given for T_A = 25 °C.
(3) The I/O speed is configured using the GPIOx_OSPD -> OSPDy[1:0]bits.
(4) Only for reference, Depending on user's design.
(5) Max frequency is defined when the sum of rise time plus the fall time is less than 2/3 cycle.

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4.12. ADC characteristics

Table 4-27. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA} (1)	Operating voltage	—	2.6	3.3	3.6	V
V_{IN}(1)	ADC input voltage range	—	0	—	V_{REFP}	V
V_{REFP}(2)(3)	Positive Reference Voltage	—	2.6	—	V_{DDA}	V
V_{REFN}(2)	Negative Reference Voltage	—	—	V_{SSA}	—	V
f_{ADC}(1)	ADC clock	—	0.1	—	40	MHz
f_S(1)	Sampling rate	12-bit	0.007	—	2.6	MSPS
		10-bit	0.008	—	3.1	
		8-bit	0.01	—	3.6	
		6-bit	0.011	—	4.4	
V_{AIN}(1)	Analog input voltage	16 external; 3 internal	0	—	V_{REFP}	V
R_{AIN}(2)	External input impedance	See *Equation 2*	—	—	308.6	kΩ
R_{ADC}(2)	Input sampling switch resistance	—	—	—	0.55	kΩ
C_{ADC}(2)	Input sampling capacitance	No pin/pad capacitance included	—	—	4.0	pF
t_{CAL}(2)	Calibration time	f_{ADC} = 40 MHz	—	3.275	—	µs
t_s(2)	Sampling time	f_{ADC} = 40 MHz	0.075	—	12	µs
t_{CONV}(2)	Total conversion time (including sampling time)	12-bit	—	15	—	1/ f_{ADC}
		10-bit	—	13	—	
		8-bit	—	11	—	
		6-bit	—	9	—	
t_{SU}(2)	Startup time	—	—	—	1	µs

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

(3) V_{REFP} should always be equal to or less than V_{DDA}, especially during power up.

Equation 2: R_{AIN} max formula $$R_{AIN} < \frac{T_s}{f_{ADC} * C_{ADC} * \ln(2^{N+2})} - R_{ADC}$$

The formula above (Equation 2) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

Table 4-28. ADC RAIN max for f_{ADC} = 40 MHz(2)

T_s (cycles)	t_s (us)	$R_{AIN\ max}$ (KΩ)
3	0.075	1.3
15	0.375	9.1
28	0.7	17.4
55	1.375	34.8
84	2.1	53.5
112	2.8	71.5
144	3.6	92.4
480	12	308.6

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(1) Based on characterization, not tested in production.
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Table 4-29. ADC dynamic accuracy at f_{ADC} = 40 MHz(1)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ENOB	Effective number of bits	f_{ADC} = 40 MHz V_{DDA} = V_{REFP} = 3.3 V Input Frequency = 110 kHz Temperature = 25 ℃	—	10.9	—	bits
SNDR	Signal-to-noise and distortion ratio		—	67.3	—	dB
SNR	Signal-to-noise ratio		—	67.7	—	
THD	Total harmonic distortion		—	-75	—	

(1) Based on characterization, not tested in production.

Table 4-30. ADC static accuracy at f_{ADC} = 40 MHz(1)

Symbol	Parameter	Test conditions	Typ	Max	Unit
Offset	Offset error	f_{ADC} = 40 MHz V_{DDA} = V_{REFP} = 3.3 V	±1	—	LSB
DNL	Differential linearity error		±1	—	
INL	Integral linearity error		±1.5	—	

(1) Based on characterization, not tested in production.

4.13. Temperature sensor characteristics

Table 4-31. Temperature sensor characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
T_L	V_{SENSE} linearity with temperature	—	±1.5	—	℃
Avg_Slope	Average slope	—	4.4	—	mV/℃
V_{25}	Voltage at 25 °C	—	1.4	—	V
t_{S_temp} (2)	ADC sampling time when reading the temperature	—	17.1	—	μs

(1) Based on characterization, not tested in production.
(2) Shortest sampling time can be determined in the application by multiple iterations.

4.14. DAC characteristics

Table 4-32. DAC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA} (1)	Operating voltage	—	2.6	3.3	3.6	V
V_{REFP} (2)	Positive Reference Voltage	—	2.6	—	V_{DDA}	V
V_{REFN} (2)	Negative Reference Voltage	—	—	V_{SSA}	—	V
R_{LOAD}(2)	Resistive load	Resistive load with buffer ON	5	—	—	kΩ
Ro(2)	Impedance output	Impedance output with buffer OFF	—	—	15	kΩ
C_{LOAD}(2)	Capacitive load	Capacitive load with buffer ON	—	—	50	pF
DAC_OUT min(2)	Lower DAC_OUT voltage	Lower DAC_OUT voltage with buffer ON	0.2	—	—	V
		Lower DAC_OUT voltage with	0.5	—	—	mV

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		buffer OFF				
DAC_OUT max (2)	Higher DAC_OUT voltage	Higher DAC_OUT voltage with buffer ON	—	—	V_{DDA} - 0.2	V
		Higher DAC_OUT voltage with buffer OFF	—	—	V_{DDA} - 1LSB	V
I_{DDA}(1)	DAC current consumption in quiescent mode	With no load, middle code(0x800) on the input, V_{REFP} = 3.6 V	—	350	—	μA
		With no load, worst code(0xF1C) on the input, V_{REFP} = 3.6 V	—	430	—	
$I_{DDVREFP}$(1)	DAC current consumption in quiescent mode	With no load, middle code(0x800) on the input, V_{REFP} = 3.6 V	—	115	—	μA
		With no load, worst code(0xF1C) on the input, V_{REFP} = 3.6 V	—	298	—	
DNL(1)	Differential non linearity	10-bit configuration	—	—	±0.75	LSB
		12-bit configuration	—	—	±3	
INL(1)	Integral non linearity	10-bit configuration	—	—	±1.25	LSB
		12-bit configuration	—	—	±5	
Offset(1)	Offset error	DAC in 12-bit mode	—	—	±24	LSB
GE(1)	Gain error	DAC in 12-bit mode	—	—	±1.5	%
$T_{setting}$(1)	Settling time	$C_{LOAD} \leqslant$ 50 pF, $R_{LOAD} \geqslant$ 5 kΩ	—	0.5	1	μs
T_{wakeup}(2)	Wakeup from off state	—	—	5	10	μs
Update rate(2)	Max frequency for a correct DAC_OUT change from code i to i±1LSB	$C_{LOAD} \leqslant$ 50 pF, $R_{LOAD} \geqslant$ 5 kΩ	—	—	4	MS/s
PSRR(2)	Power supply rejection ratio(to V_{DDA})	No R_{Load}, C_{LOAD}=50 pF	—	-90	—	dB

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

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4.15. I2C characteristics

Table 4-33. I2C characteristics(1)(2)

Symbol	Parameter	Conditions	Standard mode		Fast mode		Unit
			Min	Max	Min	Max	
$t_{SCL(H)}$	SCL clock high time	—	4.0	—	0.6	—	μs
$t_{SCL(L)}$	SCL clock low time	—	4.7	—	1.3	—	μs
$t_{SU(SDA)}$	SDA setup time	—	250	—	100	—	ns
$t_{h(SDA)}$	SDA data hold time	—	0(3)	3450	0	900	ns

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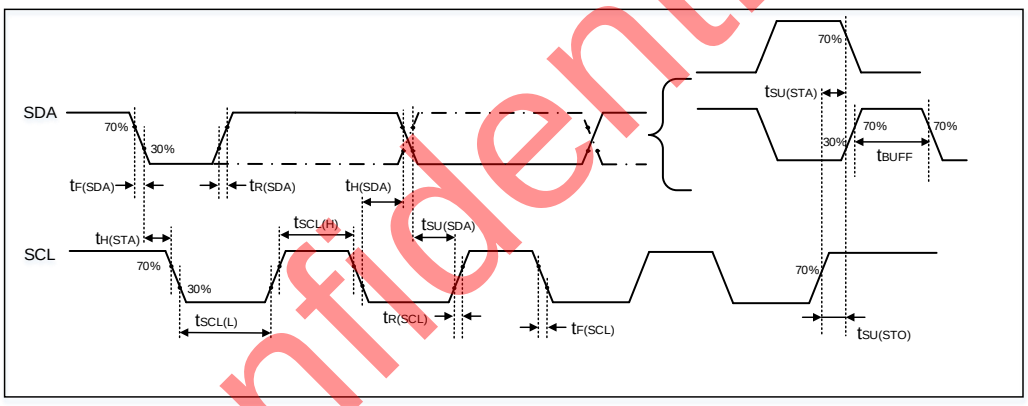
Symbol	Parameter	Conditions	Standard mode		Fast mode		Unit
			Min	Max	Min	Max	
$t_{r(SDA/SCL)}$	SDA and SCL rise time	—	—	1000	—	300	ns
$t_{f(SDA/SCL)}$	SDA and SCL fall time	—	—	300	—	300	ns
$t_{h(STA)}$	Start condition hold time	—	4.0	—	0.6	—	μs
$t_{SU(STA)}$	Repeated Start condition setup time	—	4.7	—	0.6	—	μs
$t_{SU(STO)}$	Stop condition setup time	—	4.0	—	0.6	—	μs
t_{buff}	Stop to Start condition time (bus free)	—	4.7	—	1.3	—	μs

(1) Guaranteed by design, not tested in production.

(2) To ensure the standard mode I2C frequency, f_{PCLK1} must be at least 2 MHz. To ensure the fast mode I2C frequency, f_{PCLK1} must be at least 4 MHz.

(3) The device should provide a data hold time of 300 ns at least in order to bridge the undefined region of the falling edge of SCL.

Figure 4-6. I2C bus timing diagram



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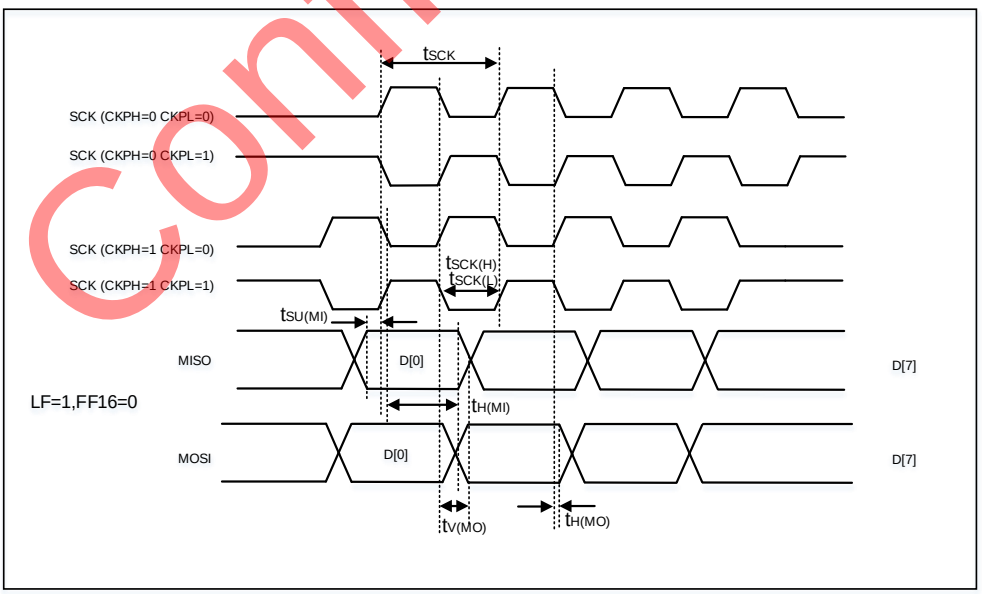
4.16. SPI characteristics

Table 4-34. Standard SPI characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency	—	—	—	30	MHz
$t_{SCK(H)}$	SCK clock high time	Master mode, f_{PCLKx} = 120 MHz, presc = 4	14.67	16.67	18.67	ns
$t_{SCK(L)}$	SCK clock low time	Master mode, f_{PCLKx} = 120 MHz, presc = 4	14.67	16.67	18.67	ns
SPI master mode						
$t_{V(MO)}$	Data output valid time	—	—	—	8	ns
$t_{SU(MI)}$	Data input setup time	—	6	—	—	ns
$t_{H(MI)}$	Data input hold time	—	0	—	—	ns
SPI slave mode						
$t_{SU(NSS)}$	NSS enable setup time	—	0	—	—	ns
$t_{H(NSS)}$	NSS enable hold time	—	3.3	—	—	ns
$t_{A(SO)}$	Data output access time	—	—	9	—	ns
$t_{DIS(SO)}$	Data output disable time	—	—	10	—	ns
$t_{V(SO)}$	Data output valid time	—	—	11	—	ns
$t_{SU(SI)}$	Data input setup time	—	0	—	—	ns
$t_{H(SI)}$	Data input hold time	—	2.2	—	—	ns

(1) Based on characterization, not tested in production.

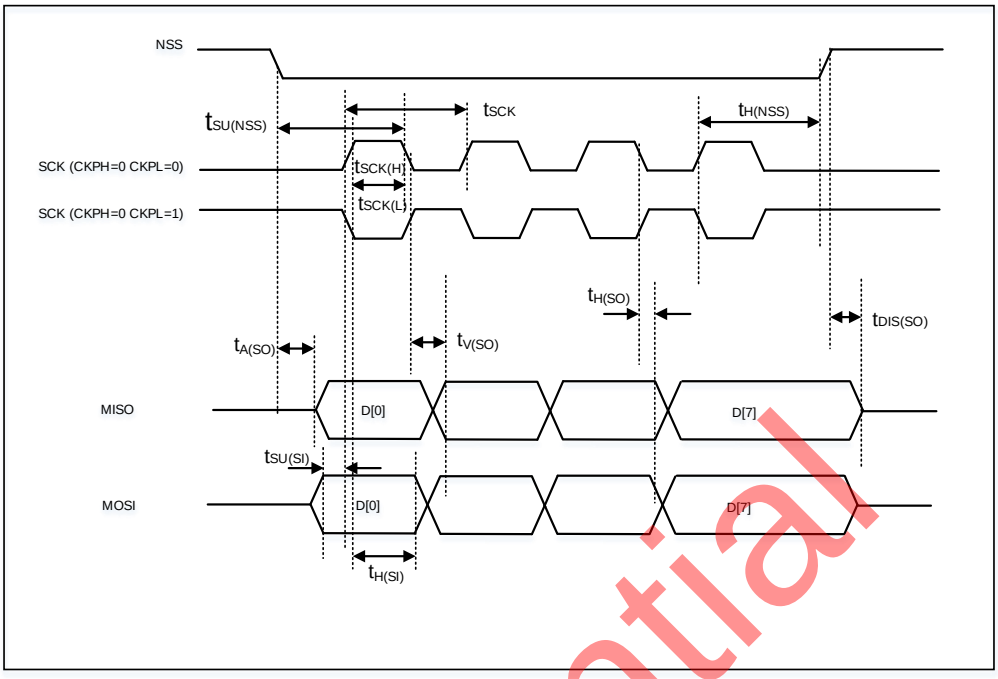
Figure 4-7. SPI timing diagram - master mode



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Figure 4-8. SPI timing diagram - slave mode



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4.17. I2S characteristics

Table 4-35. I2S characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CK}	Clock frequency	Master mode (data: 32 bits, Audio frequency = 96 kHz)	—	6.25	—	MHz
		Slave mode	—	—	12.5	
t_H	Clock high time	—	—	80	—	ns
t_L	Clock low time		—	80	—	ns
$t_{V(WS)}$	WS valid time	Master mode	—	3	—	ns
$t_{H(WS)}$	WS hold time	Master mode	—	3	—	ns
$t_{SU(WS)}$	WS setup time	Slave mode	0	—	—	ns
$t_{H(WS)}$	WS hold time	Slave mode	3	—	—	ns
$Ducy_{(SCK)}$	I2S slave input clock duty cycle	Slave mode	—	50	—	%
$t_{SU(SD_MR)}$	Data input setup time	Master mode	0	—	—	ns
$t_{su(SD_SR)}$	Data input setup time	Slave mode	0	—	—	ns
$t_{H(SD_MR)}$	Data input hold time	Master receiver	1	—	—	ns
$t_{H(SD_SR)}$		Slave receiver	3	—	—	ns
$t_{V(SD_ST)}$	Data output valid time	Slave transmitter (after enable edge)	—	—	9	ns
$t_{H(SD_ST)}$	Data output hold time	Slave transmitter (after enable edge)	6	—	—	ns
$t_{V(SD_MT)}$	Data output valid time	Master transmitter (after enable edge)	—	—	6	ns
$t_{H(SD_MT)}$	Data output hold time	Master transmitter (after enable edge)	0	—	—	ns

(1) Guaranteed by design, not tested in production.

(2) Based on characterization, not tested in production.

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Figure 4-9. I2S timing diagram - master mode

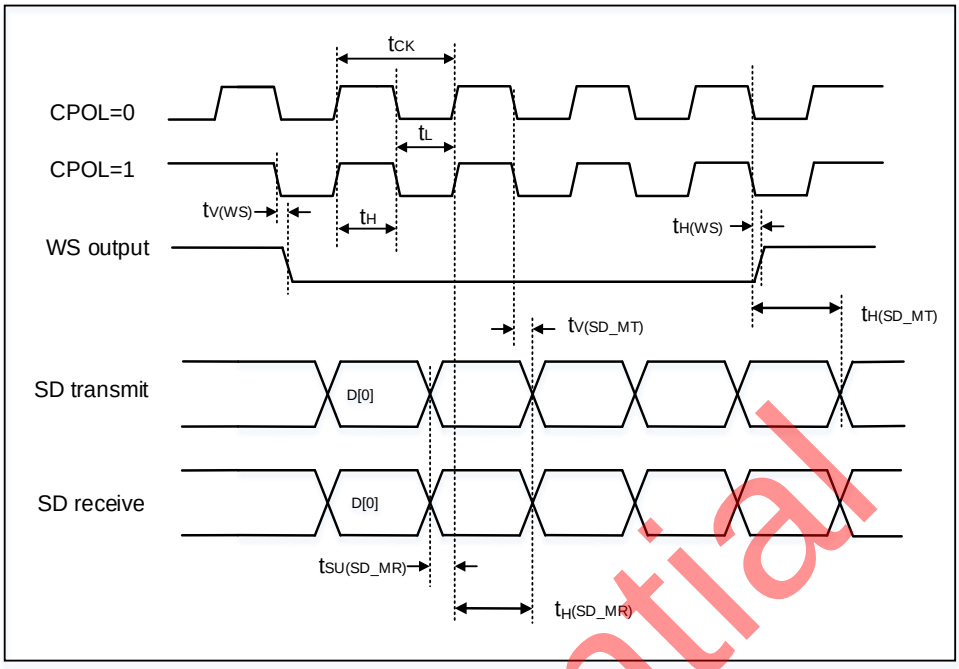
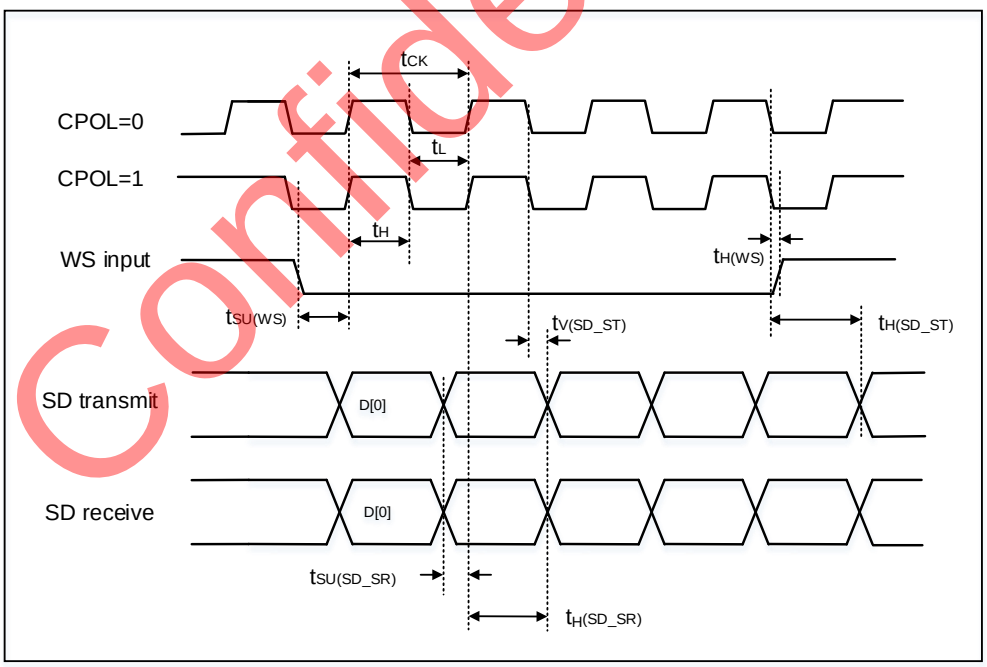


Figure 4-10. I2S timing diagram - slave mode



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4.18. USART characteristics

Table 4-36. USART characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency	f_{PCLKx} = 120 MHz	—	—	60	MHz
$t_{SCK(H)}$	SCK clock high time	f_{PCLKx} = 120 MHz	8.33	—	—	ns
$t_{SCK(L)}$	SCK clock low time	f_{PCLKx} = 120 MHz	8.33	—	—	ns

(1) Guaranteed by design, not tested in production.

4.19. SDIO characteristics

Table 4-37. SDIO characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP}(3)	Clock frequency in data transfer mode	—	0	—	48	MHz
$t_{W(CKL)}$ (3)	Clock low time	f_{pp} = 48 MHz	9.5	10.5	—	ns
$t_{W(CKH)}$ (3)	Clock high time	f_{pp} = 48 MHz	9.3	10.3	—	ns
CMD, D inputs (referenced to CK) in MMC and SD HS mode						
t_{ISU}(4)	Input setup time HS	f_{pp} = 48 MHz	4	—	—	ns
t_{IH}(4)	Input hold time HS	f_{pp} = 48 MHz	3	—	—	ns
CMD, D outputs (referenced to CK) in MMC and SD HS mode						
t_{OV}(3)	Output valid time HS	f_{pp} = 48 MHz	—	—	13.8	ns
t_{OH}(3)	Output hold time HS	f_{pp} = 48 MHz	12	—	—	ns
CMD, D inputs (referenced to CK) in SD default mode						
t_{ISUD}(4)	Input setup time SD	f_{pp} = 24 MHz	3	—	—	ns
t_{IHD}(4)	Input hold time SD	f_{pp} = 24 MHz	3	—	—	ns
CMD, D outputs (referenced to CK) in SD default mode						
t_{OVD}(3)	Output valid default time SD	f_{pp} = 24 MHz	—	2.4	2.8	ns
t_{OHD}(3)	Output hold default time SD	f_{pp} = 24 MHz	2	—	—	ns

(1) CLK timing is measured at 50% of V_{DD}.
(2) Capacitive load C_L = 30 pF.
(3) Based on characterization, not tested in production.
(4) Guaranteed by design, not tested in production.

4.20. CAN characteristics

Refer to ***Table 4-25. I/O port DC characteristics(1)*** for more details on the input/output alternate function characteristics (CANTX and CANRX).

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4.21. USBFS characteristics

Table 4-38. USBFS start up time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	USBFS startup time	1	μs

(1) Guaranteed by design, not tested in production.

Table 4-39. USBFS DC electrical characteristics

Symbol		Parameter	Conditions	Min	Typ	Max	Unit
Input levels(1)	V_{DD}	USBFS operating voltage	—	3	—	3.6	V
	V_{DI}	Differential input sensitivity	—	0.2	—	—	
	V_{CM}	Differential common mode range	Includes V_{DI} range	0.8	—	2.5	
	V_{SE}	Single ended receiver threshold	—	1.3	—	2.0	
Output levels (2)	V_{OL}	Static output level low	R_L of 1.0 kΩ to 3.6 V	—	0.06	0.3	V
	V_{OH}	Static output level high	R_L of 15 kΩ to V_{SS}	2.8	3.3	3.6	
R_{PD}(2)		PA11, PA12(USBFS_DM/DP) PB14, PB15(USBHS_ DM/DP)	V_{IN} = V_{DD}	17	21	25	kΩ
		PA9(USBFS_VBUS) PB13(USBHS_VBUS)		0.72	0.9	1.1	
R_{PU}(2)		PA11, PA12(USBFS_DM/DP) PB14, PB15(USBHS_ DM/DP)	V_{IN} = V_{SS}	1.2	1.5	1.8	
		PA9(USBFS_VBUS) PB13(USBHS_VBUS)		0.24	0.3	0.33	

(1) Guaranteed by design, not tested in production.

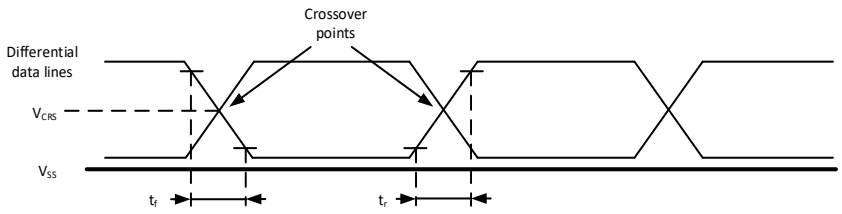
(2) Based on characterization, not tested in production.

Table 4-40. USBFS full speed-electrical characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_R	Rise time	C_L = 50 pF	4	—	20	ns
t_F	Fall time	C_L = 50 pF	4	—	20	ns
t_{RFM}	Rise/ fall time matching	t_R / t_F	90	—	110	%
V_{CRS}	Output signal crossover voltage	—	1.3	—	2.0	V

(1) Guaranteed by design, not tested in production.

Figure 4-11. USBFS timings: definition of data signal rise and fall time



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4.22. USBHS characteristics

Table 4-41. USBHS clock timing parameters(1)

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	USBHS operating voltage	3.0	—	3.6	V
f_{HCLK}	f_{HCLK} value to guarantee proper operation of USBHS interface	30	—	—	MHz
F_{START_8BIT}	Frequency (first transition) 8-bit ± 10%	54	60	66	MHz
F_{STEADY}	Frequency (steady state) ±500 ppm	59.97	60	60.63	MHz
D_{START_8BIT}	Duty cycle (first transition) 8-bit ± 10%	40	50	60	%
D_{STEADY}	Duty cycle (steady state) ±500 ppm	49.975	50	50.025	%

(1) Guaranteed by design, not tested in production.

Table 4-42. USB-ULPI Dynammic characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t_{SC}	Control in (ULPI_DIR, ULPI_NXT) setup time	—	—	2	ns
t_{HC}	Control in (ULPI_DIR, ULPI_NXT) hold time	0.5	—	—	ns
t_{SD}	Data in setup time	—	—	2	ns
t_{HD}	Data in hold time	0	—	—	ns

(1) Guaranteed by design, not tested in production.

4.23. EXMC characteristics

Table 4-43. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings(1)(2)(3)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	EXMC_NE low time	19.85	21.85	ns
$t_{V(NOE_NE)}$	EXMC_NEx low to EXMC_NOE low	0	—	ns
$t_{w(NOE)}$	EXMC_NOE low time	19.85	21.85	ns
$t_{h(NE_NOE)}$	EXMC_NOE high to EXMC_NE high hold time	0	—	ns
$t_{v(A_NE)}$	EXMC_NEx low to EXMC_A valid	0	—	ns
$t_{v(BL_NE)}$	EXMC_NEx low to EXMC_BL valid	0	—	ns
$t_{su(DATA_NE)}$	Data to EXMC_NEx high setup time	15.68	—	ns
$t_{su(DATA_NOE)}$	Data to EXMC_NOEx high setup time	15.68	—	ns
$t_{h(DATA_NOE)}$	Data hold time after EXMC_NOE high	0	—	ns
$t_{h(DATA_NE)}$	Data hold time after EXMC_NEx high	0	—	ns
$t_{v(NADV_NE)}$	EXMC_NEx low to EXMC_NADV low	0	—	ns
$t_{w(NADV)}$	EXMC_NADV low time	3.17	5.17	ns

(1) C_L = 30 pF.
(2) Guaranteed by design, not tested in production.
(3) Based on configure: f_{HCLK} = 240 MHz, AddressSetupTime = 0, AddressHoldTime = 1, DataSetupTime = 1.

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Table 4-44. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings(1)(2)(3)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	EXMC_NE low time	11.51	13.51	ns
$t_{V(NWE_NE)}$	EXMC_NEx low to EXMC_NWE low	3.17	—	ns
$t_{w(NWE)}$	EXMC_NWE low time	3.17	5.17	ns
$t_{h(NE_NWE)}$	EXMC_NWE high to EXMC_NE high hold time	3.17	5.17	ns
$t_{v(A_NE)}$	EXMC_NEx low to EXMC_A valid	0	—	ns
$t_{V(NADV_NE)}$	EXMC_NEx low to EXMC_NADV low	0	—	ns
$t_{w(NADV)}$	EXMC_NADV low time	3.17	5.17	ns
$t_{h(AD_NADV)}$	EXMC_AD(address) valid hold time after EXMC_NADV high	7.34	—	ns
$t_{h(A_NWE)}$	Address hold time after EXMC_NWE high	3.17	—	ns
$t_{h(BL_NWE)}$	EXMC_BL hold time after EXMC_NWE high	3.17	—	ns
$t_{v(BL_NE)}$	EXMC_NEx low to EXMC_BL valid	0	—	ns
$t_{v(DATA_NADV)}$	EXMC_NADV high to DATA valid	0	—	ns
$t_{h(DATA_NWE)}$	Data hold time after EXMC_NWE high	3.17	—	ns

(1) C_L = 30 pF.
(2) Guaranteed by design, not tested in production.
(3) Based on configure: f_{HCLK} = 240 MHz, AddressSetupTime = 0, AddressHoldTime = 1, DataSetupTime = 1.

Table 4-45. Asynchronous multiplexed PSRAM/NOR read timings(1)(2)(3)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	EXMC_NE low time	28.19	30.19	ns
$t_{V(NOE_NE)}$	EXMC_NEx low to EXMC_NOE low	11.51	—	ns
$t_{w(NOE)}$	EXMC_NOE low time	15.68	17.68	ns
$t_{h(NE_NOE)}$	EXMC_NOE high to EXMC_NE high hold time	0	—	ns
$t_{v(A_NE)}$	EXMC_NEx low to EXMC_A valid	0	—	ns
$t_{v(A_NOE)}$	Address hold time after EXMC_NOE high	0	—	ns
$t_{v(BL_NE)}$	EXMC_NEx low to EXMC_BL valid	0	—	ns
$t_{h(BL_NOE)}$	EXMC_BL hold time after EXMC_NOE high	0	—	ns
$t_{su(DATA_NE)}$	Data to EXMC_NEx high setup time	15.68	—	ns
$t_{su(DATA_NOE)}$	Data to EXMC_NOEx high setup time	15.68	—	ns
$t_{h(DATA_NOE)}$	Data hold time after EXMC_NOE high	0	—	ns
$t_{h(DATA_NE)}$	Data hold time after EXMC_NEx high	0	—	ns
$t_{v(NADV_NE)}$	EXMC_NEx low to EXMC_NADV low	0	—	ns
$t_{w(NADV)}$	EXMC_NADV low time	3.17	5.17	ns
$T_{h(AD_NADV)}$	EXMC_AD(adress) valid hold time after EXMC_NADV high	3.17	5.17	ns

(1) C_L = 30 pF.
(2) Guaranteed by design, not tested in production.
(3) Based on configure: f_{HCLK}= 240 MHz, AddressSetupTime = 0, AddressHoldTime = 1, DataSetupTime = 1.

Table 4-46. Asynchronous multiplexed PSRAM/NOR write timings(1)(2)(3)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	EXMC_NE low time	19.85	21.85	ns

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Symbol	Parameter	Min	Max	Unit
$t_{V(NWE_NE)}$	EXMC_NEx low to EXMC_NWE low	3.17	—	ns
$t_{w(NWE)}$	EXMC_NWE low time	11.51	13.51	ns
$t_{h(NE_NWE)}$	EXMC_NWE high to EXMC_NE high hold time	3.17	—	ns
$t_{v(A_NE)}$	EXMC_NEx low to EXMC_A valid	0	—	ns
$t_{V(NADV_NE)}$	EXMC_NEx low to EXMC_NADV low	0	—	ns
$t_{w(NADV)}$	EXMC_NADV low time	3.17	5.17	ns
$t_{h(AD_NADV)}$	EXMC_AD(address) valid hold time after EXMC_NADV high	3.17	—	ns
$t_{h(A_NWE)}$	Address hold time after EXMC_NWE high	3.17	—	ns
$t_{h(BL_NWE)}$	EXMC_BL hold time after EXMC_NWE high	3.17	—	ns
$t_{v(BL_NE)}$	EXMC_NEx low to EXMC_BL valid	0	—	ns
$t_{v(DATA_NADV)}$	EXMC_NADV high to DATA valid	3.17	—	ns
$t_{h(DATA_NWE)}$	Data hold time after EXMC_NWE high	3.17	—	ns

(1) C_L = 30 pF.
(2) Guaranteed by design, not tested in production.
(3) Based on configure: f_{HCLK} = 240 MHz, AddressSetupTime = 0, AddressHoldTime = 1, DataSetupTime = 1.

Table 4-47. Synchronous multiplexed PSRAM/NOR read timings(1)(2)(3)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	EXMC_CLK period	16.67	—	ns
$t_{d(CLKL-NExL)}$	EXMC_CLK low to EXMC_NEx low	0	—	ns
$t_{d(CLKH-NExH)}$	EXMC_CLK high to EXMC_NEx high	7.34	—	ns
$t_{d(CLKL-NADVL)}$	EXMC_CLK low to EXMC_NADV low	0	—	ns
$t_{d(CLKL-NADVH)}$	EXMC_CLK low to EXMC_NADV high	0	—	ns
$t_{d(CLKL-AV)}$	EXMC_CLK low to EXMC_Ax valid	0	—	ns
$t_{d(CLKH-AIV)}$	EXMC_CLK high to EXMC_Ax invalid	7.34	—	ns
$t_{d(CLKL-NOEL)}$	EXMC_CLK low to EXMC_NOE low	0	—	ns
$t_{d(CLKH-NOEH)}$	EXMC_CLK high to EXMC_NOE high	7.34	—	ns
$t_{d(CLKL-ADV)}$	EXMC_CLK low to EXMC_AD valid	0	—	ns
$t_{d(CLKL-ADIV)}$	EXMC_CLK low to EXMC_AD invalid	0	—	ns

(1) C_L = 30 pF.
(2) Guaranteed by design, not tested in production.
(3) (Based on configure: f_{HCLK} = 240 MHz, BurstAccessMode = Enable; Memory Type = PSRAM; WriteBurst = Enable; CLKDivision = 3 (EXMC_CLK is 4 divided by HCLK); Data Latency = 1.

Table 4-48. Synchronous multiplexed PSRAM write timings(1)(2)(3)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	EXMC_CLK period	16.67	—	ns
$t_{d(CLKL-NExL)}$	EXMC_CLK low to EXMC_NEx low	0	—	ns
$t_{d(CLKH-NExH)}$	EXMC_CLK high to EXMC_NEx high	7.34	—	ns
$t_{d(CLKL-NADVL)}$	EXMC_CLK low to EXMC_NADV low	0	—	ns
$t_{d(CLKL-NADVH)}$	EXMC_CLK low to EXMC_NADV high	0	—	ns
$t_{d(CLKL-AV)}$	EXMC_CLK low to EXMC_Ax valid	0	—	ns
$t_{d(CLKH-AIV)}$	EXMC_CLK high to EXMC_Ax invalid	7.34	—	ns
$t_{d(CLKL-NWEL)}$	EXMC_CLK low to EXMC_NWE low	0	—	ns

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Symbol	Parameter	Min	Max	Unit
$t_{d(CLKH-NWEH)}$	EXMC_CLK high to EXMC_NWE high	7.34	—	ns
$t_{d(CLKL-ADIV)}$	EXMC_CLK low to EXMC_AD invalid	0	—	ns
$t_{d(CLKL-DATA)}$	EXMC_A/D valid data after EXMC_CLK low	0	—	ns
$t_{h(CLKL-NBLH)}$	EXMC_CLK low to EXMC_NBL high	0	—	ns

(1) C_L = 30 pF.
(2) Guaranteed by design, not tested in production.
(3) Based on configure: f_{HCLK} = 240 MHz, BurstAccessMode = Enable; MemoryType = PSRAM; WriteBurst = Enable; CLKDivision = 3 (EXMC_CLK is 4 divided by HCLK); DataLatency = 1.

Table 4-49. Synchronous non-multiplexed PSRAM/NOR read timings(1)(2)(3)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	EXMC_CLK period	16.67	—	ns
$t_{d(CLKL-NExL)}$	EXMC_CLK low to EXMC_NEx low	0	—	ns
$t_{d(CLKH-NExH)}$	EXMC_CLK high to EXMC_NEx high	7.34	—	ns
$t_{d(CLKL-NADVL)}$	EXMC_CLK low to EXMC_NADV low	0	—	ns
$t_{d(CLKL-NADVH)}$	EXMC_CLK low to EXMC_NADV high	0	—	ns
$t_{d(CLKL-AV)}$	EXMC_CLK low to EXMC_Ax valid	0	—	ns
$t_{d(CLKH-AIV)}$	EXMC_CLK high to EXMC_Ax invalid	7.34	—	ns
$t_{d(CLKL-NOEL)}$	EXMC_CLK low to EXMC_NOE low	0	—	ns
$t_{d(CLKH-NOEH)}$	EXMC_CLK high to EXMC_NOE high	7.34	—	ns

(1) C_L = 30 pF.
(2) Guaranteed by design, not tested in production.
(3) Based on configure: f_{HCLK} = 240 MHz, BurstAccessMode = Enable; MemoryType = PSRAM; WriteBurst = Enable; CLKDivision = 3 (EXMC_CLK is 4 divided by HCLK); DataLatency = 1.

Table 4-50. Synchronous non-multiplexed PSRAM write timings(1)(2)(3)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	EXMC_CLK period	16.67	—	ns
$t_{d(CLKL-NExL)}$	EXMC_CLK low to EXMC_NEx low	0	—	ns
$t_{d(CLKH-NExH)}$	EXMC_CLK high to EXMC_NEx high	7.34	—	ns
$t_{d(CLKL-NADVL)}$	EXMC_CLK low to EXMC_NADV low	0	—	ns
$t_{d(CLKL-NADVH)}$	EXMC_CLK low to EXMC_NADV high	0	—	ns
$t_{d(CLKL-AV)}$	EXMC_CLK low to EXMC_Ax valid	0	—	ns
$t_{d(CLKH-AIV)}$	EXMC_CLK high to EXMC_Ax invalid	7.34	—	ns
$t_{d(CLKL-NWEL)}$	EXMC_CLK low to EXMC_NWE low	0	—	ns
$t_{d(CLKH-NWEH)}$	EXMC_CLK high to EXMC_NWE high	7.34	—	ns
$t_{d(CLKL-DATA)}$	EXMC_A/D valid data after EXMC_CLK low	0	—	ns
$t_{h(CLKL-NBLH)}$	EXMC_CLK low to EXMC_NBL high	0	—	ns

(1) C_L = 30 pF.
(2) Guaranteed by design, not tested in production.
(3) Based on configure: f_{HCLK} = 240 MHz, BurstAccessMode = Enable; MemoryType = PSRAM; WriteBurst = Enable; CLKDivision = 3 (EXMC_CLK is 4 divided by HCLK); DataLatency = 1.

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4.24. TIMER characteristics

Table 4-51. TIMER characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
t_{res}	Timer resolution time	—	1	—	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 240 MHz	4.17	—	ns
f_{EXT}	Timer external clock frequency	—	0	$f_{TIMERxCLK}/2$	MHz
		$f_{TIMERxCLK}$ = 240 MHz	0	120	MHz
RES	Timer resolution	TIMERx (except TIMER1 & TIMER4)	—	16	bit
		TIMER1 & TIMER4	—	32	bit
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected	—	1	65536	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 240 MHz	0.004	273.07	μs
t_{MAX_COUNT}	Maximum possible count	—	—	65536x65536	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 240 MHz	—	17.90	s

(1) Guaranteed by design, not tested in production.

4.25. DCI characteristics

Table 4-52. DCI characteristics(1)

Symbol	Parameter	Min	Max	Unit
Frequency ratio	DCI_PIXCLK /fHCLK	—	0.4	
DCI_PIXCLK	Pixel clock input	—	96	MHz
D_{Pixel}	Pixel clock input duty cycle	30	70	%
$t_{su(DATA)}$	Data input setup time	2.5	—	ns
$t_{h(DATA)}$	Data input hold time	1	—	ns
$t_{su(HSYNC)}$	DCI_HS input setup time	2	—	ns
$t_{su(VSYNC)}$	DCI_VS input setup time	2	—	ns
$t_{h(HSYNC)}$	DCI_HS input hold time	0.5	—	ns
$t_{h(VSYNC)}$	DCI_VS input hold time	0.5	—	ns

(1) Guaranteed by design, not tested in production.

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4.26. WDGT characteristics

Table 4-53. FWDGT min/max timeout period at 32 kHz (IRC32K)(1)

Prescaler divider	PSC[2:0] bits	Min timeout RLD[11:0] = 0x000	Max timeout RLD[11:0] = 0xFFF	Unit
1/4	000	0.03125	511.90625	ms
1/8	001	0.03125	1023.7812	
1/16	010	0.03125	2047.53125	
1/32	011	0.03125	4095.03125	
1/64	100	0.03125	8190.03125	
1/128	101	0.03125	16380.03125	
1/256	110 or 111	0.03125	32760.03125	

(1) Guaranteed by design, not tested in production.

Table 4-54. WWDGT min-max timeout value at 60 MHz (f_{PCLK1})(1)

Prescaler divider	PSC[1:0]	Min timeout value CNT[6:0] = 0x40	Unit	Max timeout value CNT[6:0] = 0x7F	Unit
1/1	00	68.27	μs	4.37	ms
1/2	01	136.53		8.74	
1/4	10	273.07		17.48	
1/8	11	546.13		34.95	

(1) Guaranteed by design, not tested in production.

4.27. Parameter conditions

Unless otherwise specified, all values given for V_{DD} = V_{DDA} = 3.3 V, T_A = 25°C.

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5. Package information

5.1. LQFP100 package outline dimensions

Figure 5-1. LQFP100 package outline

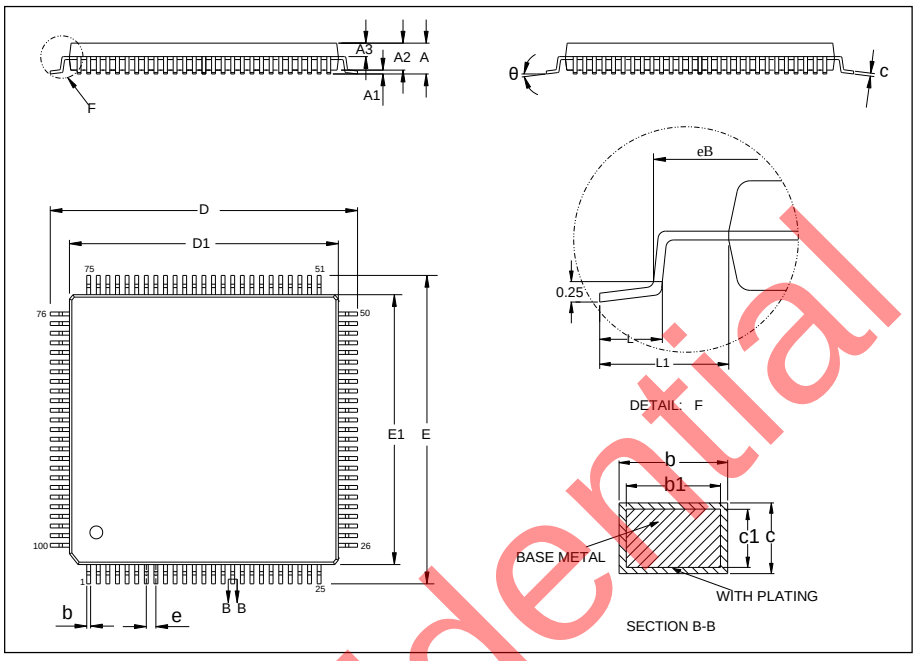


Table 5-1. LQFP100 package dimensions

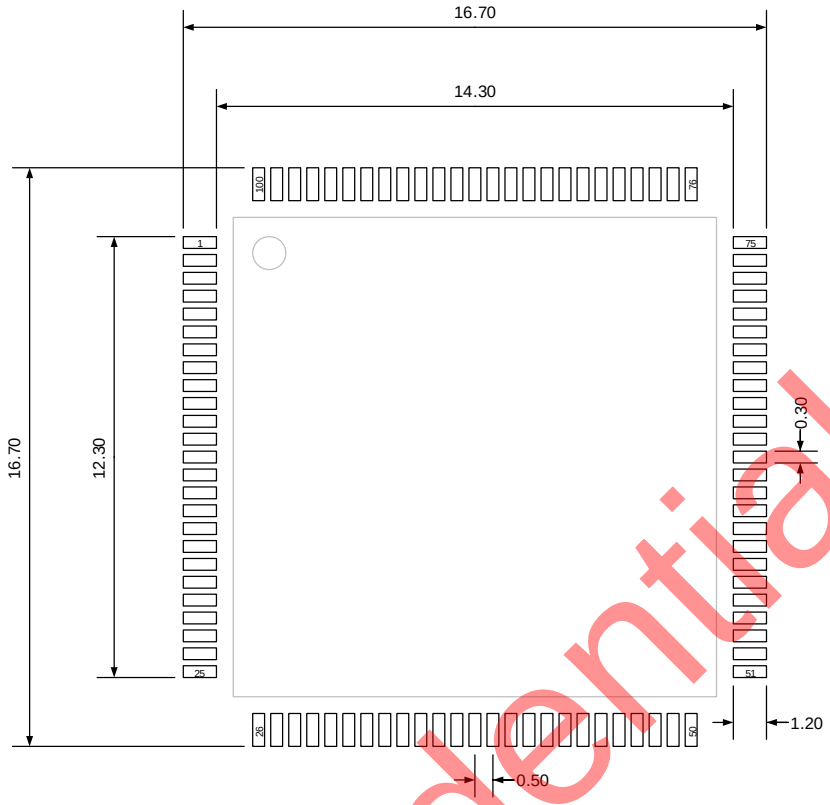
Symbol	Min	Typ	Max
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	—	0.26
b1	0.17	0.20	0.23
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	15.80	16.00	16.20
D1	13.90	14.00	14.10
E	15.80	16.00	16.20
E1	13.90	14.00	14.10
e	—	0.50	—
eB	15.05	—	15.35
L	0.45	—	0.75
L1	—	1.00	—
θ	0°	—	7°

(Original dimensions are in millimeters)

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Figure 5-2. LQFP100 recommended footprint



(Original dimensions are in millimeters)

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5.2. LQFP64 package outline dimensions

Figure 5-3. LQFP64 package outline

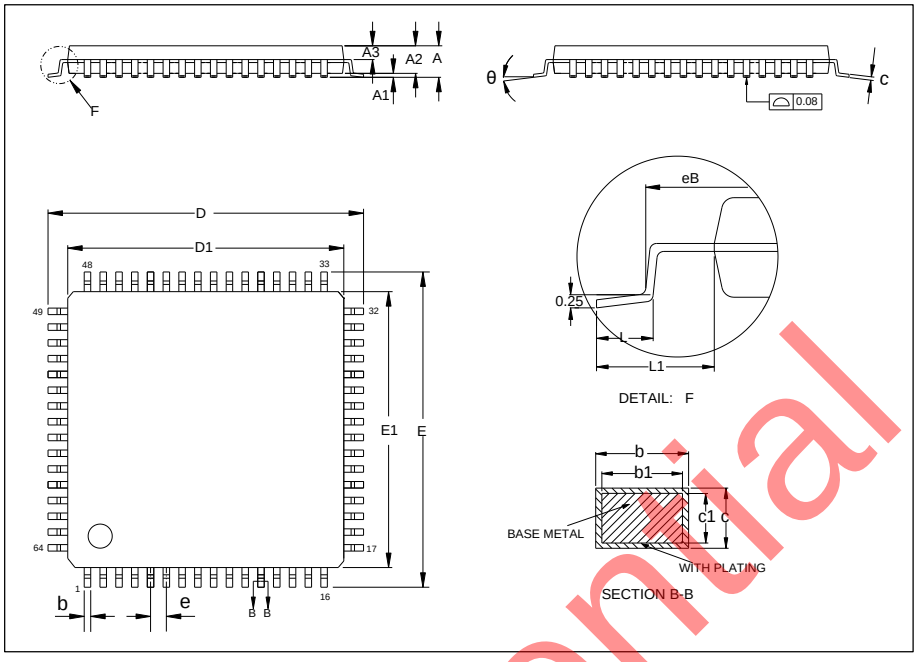


Table 5-2. LQFP64 package dimensions

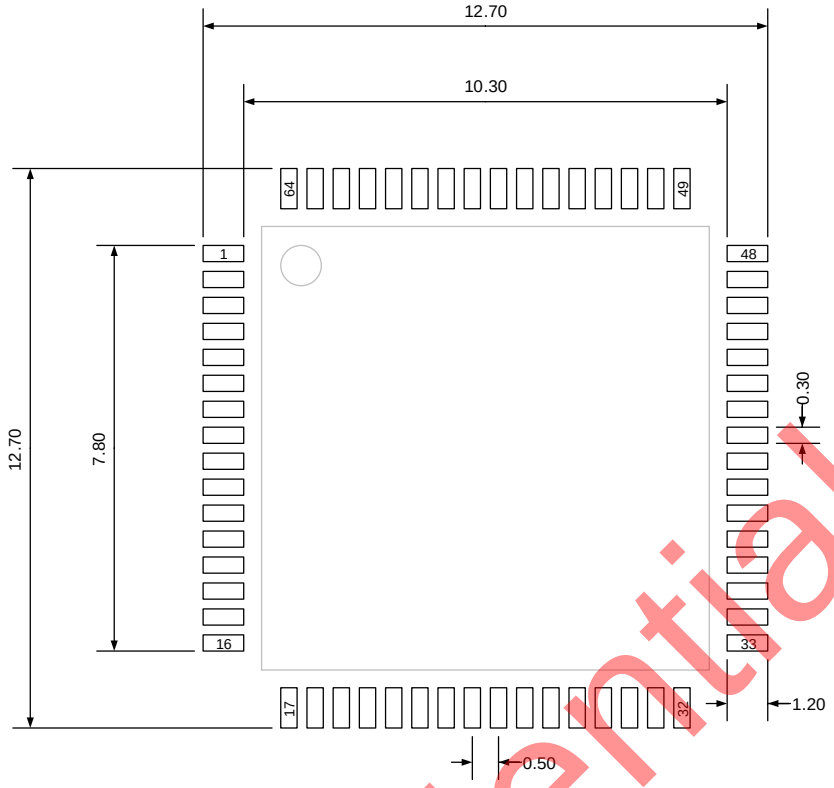
Symbol	Min	Typ	Max
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	—	0.26
b1	0.17	0.20	0.23
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
E	11.80	12.00	12.20
E1	9.90	10.00	10.10
e	—	0.50	—
eB	11.25	—	11.45
L	0.45	—	0.75
L1	—	1.00	—
θ	0°	—	7°

(Original dimensions are in millimeters)

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Figure 5-4. LQFP64 recommended footprint



(Original dimensions are in millimeters)

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5.3. Thermal characteristics

Thermal resistance is used to characterize the thermal performance of the package device, which is represented by the Greek letter "θ". For semiconductor devices, thermal resistance represents the steady-state temperature rise of the chip junction due to the heat dissipated on the chip surface.

θ_{JA}: Thermal resistance, junction-to-ambient.

θ_{JB}: Thermal resistance, junction-to-board.

θ_{JC}: Thermal resistance, junction-to-case.

Ψ_{JB}: Thermal characterization parameter, junction-to-board.

Ψ_{JT}: Thermal characterization parameter, junction-to-top center.

$$\theta_{JA}=(T_J-T_A)/P_D \quad (5\text{-}1)$$

$$\theta_{JB}=(T_J-T_B)/P_D \quad (5\text{-}2)$$

$$\theta_{JC}=(T_J-T_C)/P_D \quad (5\text{-}3)$$

Where, T_J = Junction temperature.

T_A = Ambient temperature

T_B = Board temperature

T_C = Case temperature which is monitoring on package surface

P_D = Total power dissipation

θ_{JA} represents the resistance of the heat flows from the heating junction to ambient air. It is an indicator of package heat dissipation capability. Lower θ_{JA} can be considerate as better overall thermal performance. θ_{JA} is generally used to estimate junction temperature.

θ_{JB} is used to measure the heat flow resistance between the chip surface and the PCB board.

θ_{JC} represents the thermal resistance between the chip surface and the package top case. θ_{JC} is mainly used to estimate the heat dissipation of the system (using heat sink or other heat dissipation methods outside the device package).

Table 5-3. Package thermal characteristics(1)

Symbol	Condition	Package	Value	Unit
θ_{JA}	Natural convection, 2S2P PCB	LQFP100	57.42	°C/W
		LQFP64	51.81	
θ_{JB}	Cold plate, 2S2P PCB	LQFP100	31.68	°C/W
		LQFP64	33.36	
θ_{JC}	Cold plate, 2S2P PCB	LQFP100	13.85	°C/W

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Symbol	Condition	Package	Value	Unit
		LQFP64	11.25	
Ψ_{JB}	Natural convection, 2S2P PCB	LQFP100	41.28	°C/W
		LQFP64	33.53	
Ψ_{JT}	Natural convection, 2S2P PCB	LQFP100	0.75	°C/W
		LQFP64	0.49	

(1) Thermal characteristics are based on simulation, and meet JEDEC specification.

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6. Ordering information

Table 6-1. Part ordering code for GD32F460xx devices

Ordering code	Flash (KB)	Package	Package type	Temperature operating range
GD32F460VGT7	1024	LQFP100	Green	Industrial -40°C to +105°C
GD32F460VIT7	2048	LQFP100	Green	Industrial -40°C to +105°C
GD32F460RGT7	1024	LQFP64	Green	Industrial -40°C to +105°C

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7. Revision history

Table 7-1. Revision history

Revision No.	Description	Date
1.0	Initial Release	Jan.31, 2024
1.1	1. Delete EXMC SDRAM function in pin definition. 2. Update the note on VREFP power up timing in ***Table 4-27. ADCcharacteristic***. 3. Modify DAC to DAC0 in chapter ***2. Device-overview***. 4. Update the parameters f_{PLLOUT} and f_{VCO} in ***Table 4-19. PLL characteristic***, ***Table 4-20. PLLI2S characteristic*** and ***Table 4-21. PLLSAI characteristic***. 5. Update ***Table 4-8. EMS characteristics(1)*** and ***Table 4-9. EMI characteristics(1)***. 6. Update description in chapter ***3.13. Serial peripheral interface*** and ***3.14 Universal synchronous/asynchronous receiver transmitter (USART/UART)***.	Dec.12, 2024
1.2	1. Add GD32460RGT7. 2. Update the description of t_h(DATA) in ***Table 4-52. DCI characteristics(1)***. 3. Update the ***Table 4-5. Start-up timings of Operating conditions(1)(2)(3)*** and ***Table 4-6. Power saving mode wakeup timings characteristics(1)***.	Apr.25, 2025

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