# GigaDevice Semiconductor Inc.

# GD32F450VGH6
# ARM® Cortex®-M4 32-bit MCU

Datasheet



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# 1. General description

The GD32F450VGH6 device belongs to the stretch performance line of GD32 MCU family. It is a new 32-bit general-purpose microcontroller based on the ARM® Cortex®-M4 RISC core with best cost-performance ratio in terms of enhanced processing capacity, reduced power consumption and peripheral set. The Cortex®-M4 core features a Floating Point Unit (FPU) that accelerates single precision floating point math operations and supports all ARM® single precision instructions and data types. It implements a full set of DSP instructions to address digital signal control markets that demand an efficient, easy-to-use blend of control and signal processing capabilities. It also provides a Memory Protection Unit (MPU) and powerful trace technology for enhanced application security and advanced debug support.

The GD32F450VGH6 device incorporates the ARM® Cortex®-M4 32-bit processor core operating at 200 MHz frequency with Flash accesses zero wait states to obtain maximum efficiency. It provides up to 1024 KB on-chip Flash memory and 256 KB SRAM memory. An extensive range of enhanced I/Os and peripherals connected to two APB buses. The devices offer up to three 12-bit 2.6M SPS ADCs, two 12-bit DACs, up to eight general-purpose 16-bit timers, two 16-bit PWM advanced-control timers , two 32-bit general-purpose timers, and two 16-bit basic timers, as well as standard and advanced communication interfaces: up to five SPIs, three I2Cs, four USARTs and four UARTs, two I2Ss, two CANs, a SDIO, USB device/host/OTG FS and HS, and an Ethernet MAC. Additional peripherals as Digital camera interface (DCI), EXMC interface with SDRAM extension support, TFT-LCD Interface (TLI) and Image Processing Accelerator (IPA) are included

The device operates from a 2.6 to 3.6V power supply and available in –40 to +85 °C temperature range. Three power saving modes provide the flexibility for maximum optimization of power consumption, an especially important consideration in low power applications.

The above features make GD32F450VGH6 devices suitable for a wide range of interconnection and advanced applications, especially in areas such as industrial control, consumer and handheld equipment, embedded modules, human machine interface, security and alarm systems, graphic display, automotive navigation, drone, IoT and so on.






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# 2. Device overview

## 2.1. Device information

**Table 2-1. GD32F450VGH6 devices features and peripheral list**

| GD32F450VGH6 | | |
|---|---|---|
| Flash | Code Area (KB) | 512 |
| | Data Area (KB) | 512 |
| | Total (KB) | 1024 |
| SRAM (KB) | | 256 |
| Timers | GPTM(16 bit) | 8 (2-3,8-13) |
| | GPTM(32 bit) | 2 (1,4) |
| | Advanced TM(16 bit) | 2 (0,7) |
| | Basic TM(16 bit) | 2 (5,6) |
| | SysTick | 1 |
| | Watchdog | 2 |
| | RTC | 1 |
| Connectivity | USART | 4 |
| | UART | 4 |
| | I2C | 3 |
| | SPI/I2S | 5/2 (0-4)/(1-2) |
| | SDIO | 1 |
| | CAN 2.0B | 2 |
| | USB | FS+HS |
| | Ethernet MAC | 1 |
| | TFT-LCD | 1 |
| | Digital Camera | 1 |
| GPIO | | 82 |
| EXMC/SDRAM | | 1/0 |

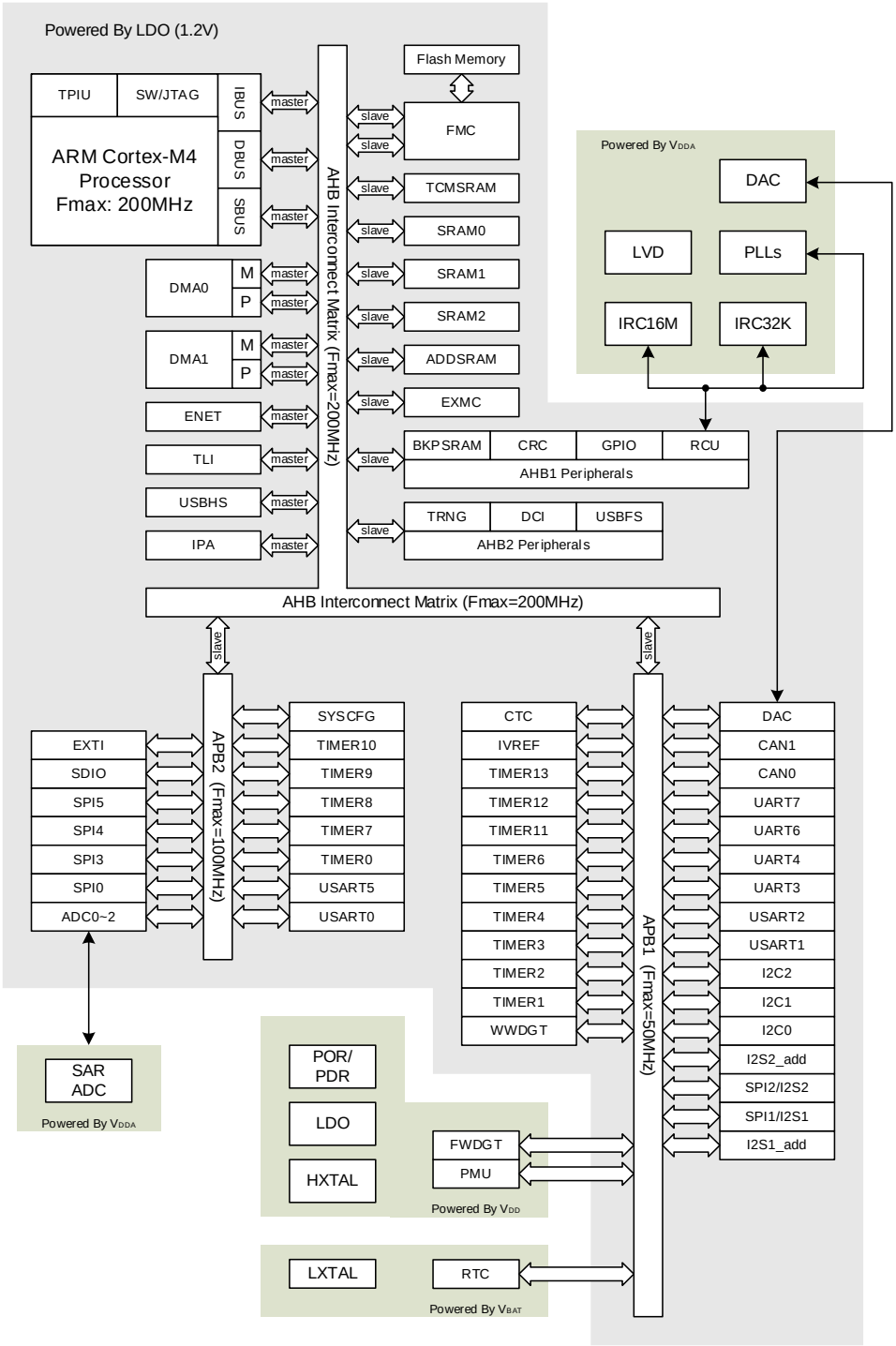


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| | |
|---|---|
| **ADC Unit (CHs)** | 3(16) |
| **DAC** | 2 |
| **Package** | **BGA100** |

## 2.2. Block diagram

**Figure 2-1. GD32F450VGH6 block diagram**

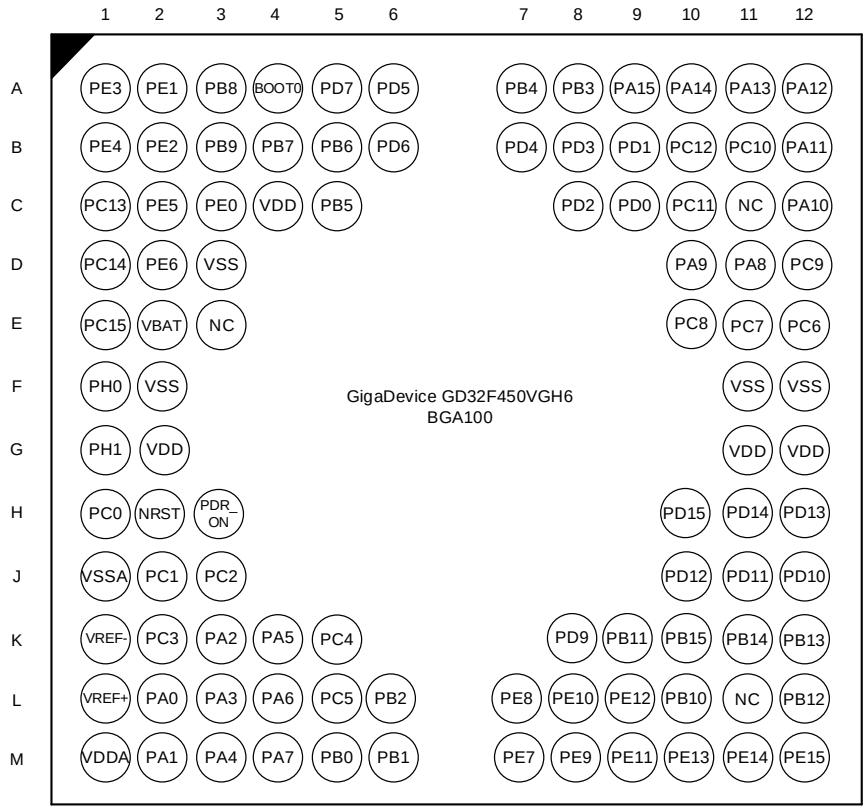





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## 2.3. Pinouts and pin assignment

**Figure 2-2. GD32F450VGH6 BGA100 pinouts**






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## 2.4. Memory map

**Table 2-2. GD32F450VGH6 memory map**

| Pre-defined Regions | Bus | Address | Peripherals |
|---|---|---|---|
| External Device | AHB matrix | 0xC000 0000 - 0xDFFF FFFF | EXMC - SDRAM |
| | | 0xA000 1000 - 0xBFFF FFFF | Reserved |
| | | 0xA000 0000 - 0xA000 0FFF | EXMC - SWREG |
| External RAM | | 0x9000 0000 - 0x9FFF FFFF | EXMC - PC CARD |
| | | 0x7000 0000 - 0x8FFF FFFF | EXMC - NAND |
| | | 0x6000 0000 - 0x6FFF FFFF | EXMC - NOR/PSRAM/SRAM |
| Peripheral | AHB2 | 0x5006 0C00 - 0x5FFF FFFF | Reserved |
| | | 0x5006 0800 - 0x5006 0BFF | TRNG |
| | | 0x5005 0400 - 0x5006 07FF | Reserved |
| | | 0x5005 0000 - 0x5005 03FF | DCI |
| | | 0x5004 0000 - 0x5004 FFFF | Reserved |
| | | 0x5000 0000 - 0x5003 FFFF | USBFS |
| | AHB1 | 0x4008 0000 - 0x4FFF FFFF | Reserved |
| | | 0x4004 0000 - 0x4007 FFFF | USBHS |
| | | 0x4002 BC00 - 0x4003 FFFF | Reserved |
| | | 0x4002 B000 - 0x4002 BBFF | IPA |
| | | 0x4002 A000 - 0x4002 AFFF | Reserved |
| | | 0x4002 8000 - 0x4002 9FFF | ENET |
| | | 0x4002 6800 - 0x4002 7FFF | Reserved |
| | | 0x4002 6400 - 0x4002 67FF | DMA1 |
| | | 0x4002 6000 - 0x4002 63FF | DMA0 |
| | | 0x4002 5000 - 0x4002 5FFF | Reserved |
| | | 0x4002 4000 - 0x4002 4FFF | BKPSRAM |
| | | 0x4002 3C00 - 0x4002 3FFF | FMC |
| | | 0x4002 3800 - 0x4002 3BFF | RCU |
| | | 0x4002 3400 - 0x4002 37FF | Reserved |
| | | 0x4002 3000 - 0x4002 33FF | CRC |
| | | 0x4002 2400 - 0x4002 2FFF | Reserved |
| | | 0x4002 2000 - 0x4002 23FF | GPIOI |
| | | 0x4002 1C00 - 0x4002 1FFF | GPIOH |
| | | 0x4002 1800 - 0x4002 1BFF | GPIOG |
| | | 0x4002 1400 - 0x4002 17FF | GPIOF |
| | | 0x4002 1000 - 0x4002 13FF | GPIOE |
| | | 0x4002 0C00 - 0x4002 0FFF | GPIOD |
| | | 0x4002 0800 - 0x4002 0BFF | GPIOC |
| | | 0x4002 0400 - 0x4002 07FF | GPIOB |



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| Pre-defined Regions | Bus | Address | Peripherals |
|---|---|---|---|
| | | 0x4002 0000 - 0x4002 03FF | GPIOA |
| | APB2 | 0x4001 6C00 - 0x4001 FFFF | Reserved |
| | | 0x4001 6800 - 0x4001 6BFF | TLI |
| | | 0x4001 5800 - 0x4001 67FF | Reserved |
| | | 0x4001 5400 - 0x4001 57FF | SPI5 |
| | | 0x4001 5000 - 0x4001 53FF | SPI4 |
| | | 0x4001 4C00 - 0x4001 4FFF | Reserved |
| | | 0x4001 4800 - 0x4001 4BFF | TIMER10 |
| | | 0x4001 4400 - 0x4001 47FF | TIMER9 |
| | | 0x4001 4000 - 0x4001 43FF | TIMER8 |
| | | 0x4001 3C00 - 0x4001 3FFF | EXTI |
| | | 0x4001 3800 - 0x4001 3BFF | SYSCFG |
| | | 0x4001 3400 - 0x4001 37FF | SPI3 |
| | | 0x4001 3000 - 0x4001 33FF | SPI0 |
| | | 0x4001 2C00 - 0x4001 2FFF | SDIO |
| | | 0x4001 2400 - 0x4001 2BFF | Reserved |
| | | 0x4001 2000 - 0x4001 23FF | ADC |
| | | 0x4001 1800 - 0x4001 1FFF | Reserved |
| | | 0x4001 1400 - 0x4001 17FF | USART5 |
| | | 0x4001 1000 - 0x4001 13FF | USART0 |
| | | 0x4001 0800 - 0x4001 0FFF | Reserved |
| | | 0x4001 0400 - 0x4001 07FF | TIMER7 |
| | | 0x4001 0000 - 0x4001 03FF | TIMER0 |
| | APB1 | 0x4000 C800 - 0x4000 FFFF | Reserved |
| | | 0x4000 C400 - 0x4000 C7FF | IVREF |
| | | 0x4000 8000 - 0x4000 C3FF | Reserved |
| | | 0x4000 7C00 - 0x4000 7FFF | UART7 |
| | | 0x4000 7800 - 0x4000 7BFF | UART6 |
| | | 0x4000 7400 - 0x4000 77FF | DAC |
| | | 0x4000 7000 - 0x4000 73FF | PMU |
| | | 0x4000 6C00 - 0x4000 6FFF | CTC |
| | | 0x4000 6800 - 0x4000 6BFF | CAN1 |
| | | 0x4000 6400 - 0x4000 67FF | CAN0 |
| | | 0x4000 6000 - 0x4000 63FF | Reserved |
| | | 0x4000 5C00 - 0x4000 5FFF | I2C2 |
| | | 0x4000 5800 - 0x4000 5BFF | I2C1 |
| | | 0x4000 5400 - 0x4000 57FF | I2C0 |
| | | 0x4000 5000 - 0x4000 53FF | UART4 |
| | | 0x4000 4C00 - 0x4000 4FFF | UART3 |
| | | 0x4000 4800 - 0x4000 4BFF | USART2 |



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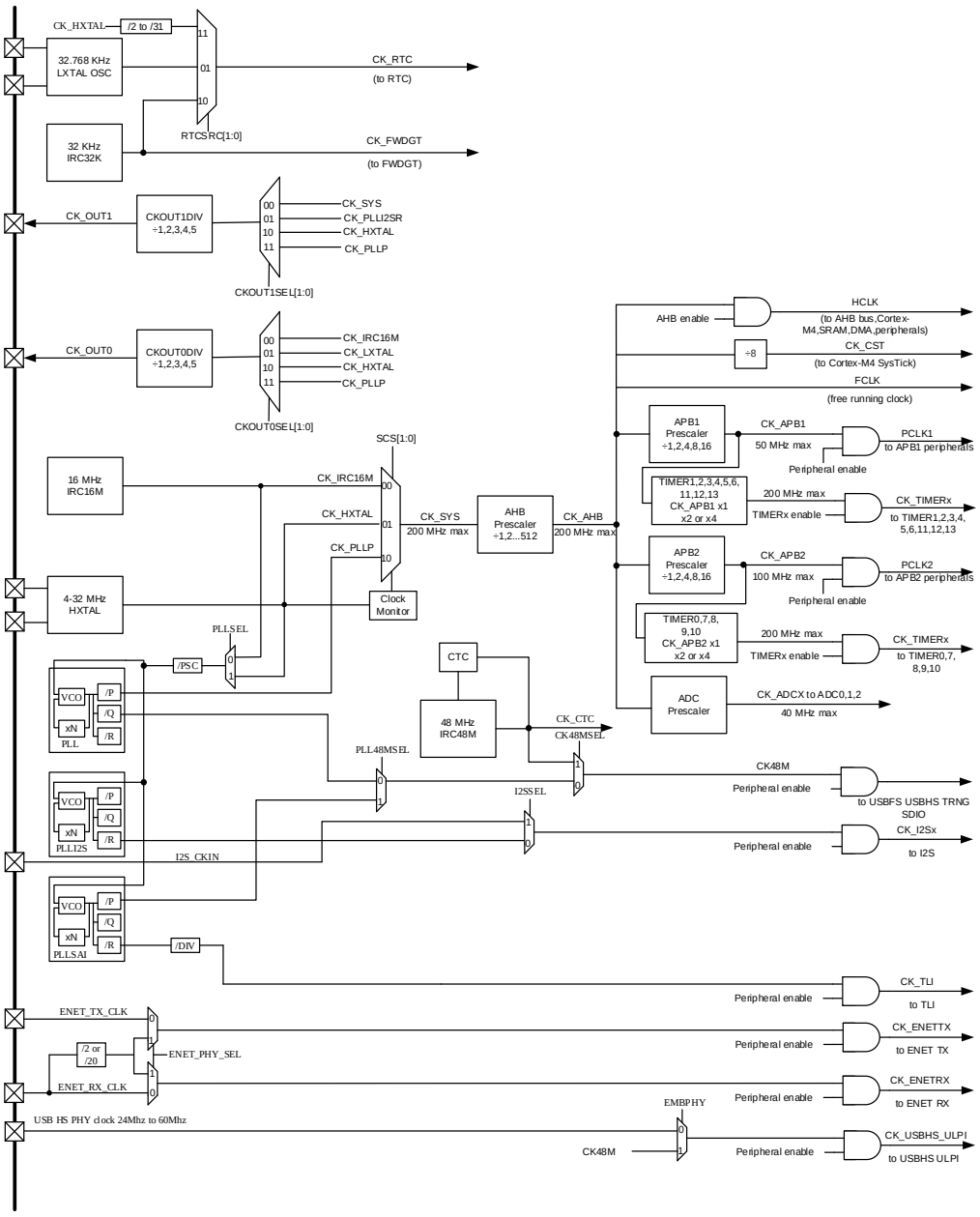
| Pre-defined Regions | Bus | Address | Peripherals |
|---|---|---|---|
| | | 0x4000 4400 - 0x4000 47FF | USART1 |
| | | 0x4000 4000 - 0x4000 43FF | I2S2_add |
| | | 0x4000 3C00 - 0x4000 3FFF | SPI2/I2S2 |
| | | 0x4000 3800 - 0x4000 3BFF | SPI1/I2S1 |
| | | 0x4000 3400 - 0x4000 37FF | I2S1_add |
| | | 0x4000 3000 - 0x4000 33FF | FWDGT |
| | | 0x4000 2C00 - 0x4000 2FFF | WWDGT |
| | | 0x4000 2800 - 0x4000 2BFF | RTC |
| | | 0x4000 2400 - 0x4000 27FF | Reserved |
| | | 0x4000 2000 - 0x4000 23FF | TIMER13 |
| | | 0x4000 1C00 - 0x4000 1FFF | TIMER12 |
| | | 0x4000 1800 - 0x4000 1BFF | TIMER11 |
| | | 0x4000 1400 - 0x4000 17FF | TIMER6 |
| | | 0x4000 1000 - 0x4000 13FF | TIMER5 |
| | | 0x4000 0C00 - 0x4000 0FFF | TIMER4 |
| | | 0x4000 0800 - 0x4000 0BFF | TIMER3 |
| | | 0x4000 0400 - 0x4000 07FF | TIMER2 |
| | | 0x4000 0000 - 0x4000 03FF | TIMER1 |
| SRAM | AHB matrix | 0x2007 0000 - 0x3FFF FFFF | Reserved |
| | | 0x2003 0000 - 0x2006 FFFF | SRAM3(256KB) |
| | | 0x2002 0000 - 0x2002 FFFF | SRAM2(64KB) |
| | | 0x2001 C000 - 0x2001 FFFF | SRAM1(16KB) |
| | | 0x2000 0000 - 0x2001 BFFF | SRAM0(112KB) |
| Code | AHB matrix | 0x1FFF C010 - 0x1FFF FFFF | Reserved |
| | | 0x1FFF C000 - 0x1FFF C00F | Option bytes(Bank 0) |
| | | 0x1FFF 7A10 - 0x1FFF BFFF | Reserved |
| | | 0x1FFF 7800 - 0x1FFF 7A0F | Reserved |
| | | 0x1FFF 0000 - 0x1FFF 77FF | Boot loader(30KB) |
| | | 0x1FFE C010 - 0x1FFE FFFF | Reserved |
| | | 0x1FFE C000 - 0x1FFE C00F | Option bytes(Bank 1) |
| | | 0x1001 0000 - 0x1FFE BFFF | Reserved |
| | | 0x1000 0000 - 0x1000 FFFF | TCMSRAM(64KB) |
| | | 0x0830 0000 - 0x0FFF FFFF | Reserved |
| | | 0x0800 0000 - 0x082F FFFF | Flash |
| | | 0x0000 0000 - 0x07FF FFFF | Aliased to the boot device |



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## 2.5. Clock tree

**Figure 2-3. GD32F450VGH6 clock tree**




**Legend:**

HXTAL: High speed crystal oscillator

LXTAL: Low speed crystal oscillator

IRC16M: Internal 16M RC oscillators

IRC32K: Internal 32K RC oscillator

IRC48M: Internal 48M RC oscillators



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## 2.6. Pin definitions

### 2.6.1. GD32F450VGH6 BGA100 pin definitions

**Table 2-3. GD32F450VGH6 BGA100 pin definitions**

| Pin Name | Pins | Pin Type(1) | I/O Level(2) | Functions description |
|---|---|---|---|---|
| PE2 | B2 | I/O | 5VT | Default: PE2<br>Alternate: TRACECLK, SPI3_SCK, ETH_MII_TXD3, EXMC_A23, EVENTOUT |
| PE3 | A1 | I/O | 5VT | Default: PE3<br>Alternate:TRACED0, EXMC_A19, EVENTOUT |
| PE4 | B1 | I/O | 5VT | Default: PE4<br>Alternate:TRACED1, SPI3_NSS, EXMC_A20, DCI_D4, TLI_B0, EVENTOUT |
| PE5 | C2 | I/O | 5VT | Default: PE5<br>Alternate:TRACED2, TIMER8_CH0, SPI3_MISO, EXMC_A21, DCI_D6, TLI_G0, EVENTOUT |
| PE6 | D2 | I/O | 5VT | Default: PE6<br>Alternate:TRACED3, TIMER8_CH1, SPI3_MOSI, EXMC_A22, DCI_D7, TLI_G1, EVENTOUT |
| $V_{BAT}$ | E2 | P | - | Default: $V_{BAT}$ |
| PC13-TAMPER-RTC | C1 | I/O | 5VT | Default: PC13<br>Alternate: EVENTOUT<br>Additional: RTC_TAMP0, RTC_OUT, RTC_TS |
| PC14-OSC32IN | D1 | I/O | 5VT | Default: PC14<br>Alternate: EVENTOUT<br>Additional: OSC32IN |
| PC15-OSC32OUT | E1 | I/O | 5VT | Default: PC15<br>Alternate: EVENTOUT<br>Additional: OSC32OUT |
| $V_{SS}$ | F2 | P | - | Default: $V_{SS}$ |
| $V_{DD}$ | G2 | P | - | Default: $V_{DD}$ |
| PH0 | F1 | I/O | 5VT | Default: PH0, OSCIN<br>Alternate: EVENTOUT<br>Additional: OSCIN |
| PH1 | G1 | I/O | 5VT | Default: PH1, OSCOUT<br>Alternate: EVENTOUT<br>Additional: OSCOUT |
| NRST | H2 | - | - | Default: NRST |
| PC0 | H1 | I/O | 5VT | Default: PC0<br>Alternate: USBHS_ULPI_STP, EXMC_SDNWE, EVENTOUT<br>Additional: ADC012_IN10 |
| PC1 | J2 | I/O | 5VT | Default: PC1<br>Alternate:SPI2_MOSI, I2S2_SD, SPI1_MOSI, I2S1_SD, |



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| Pin Name | Pins | Pin Type(1) | I/O Level(2) | Functions description |
|---|---|---|---|---|
| | | | | ETH_MDC, EVENTOUT<br>Additional: ADC012_IN11 |
| PC2 | J3 | I/O | 5VT | Default: PC2<br>Alternate:SPI1_MISO, I2S1_ADD_SD, USBHS_ULPI_DIR, ETH_MII_TXD2, EXMC_SDNE0, EVENTOUT<br>Additional: ADC012_IN12 |
| PC3 | K2 | I/O | 5VT | Default: PC3<br>Alternate:SPI1_MOSI, I2S1_SD, USBHS_ULPI_NXT, ETH_MII_TX_CLK, EXMC_SDCKE0, EVENTOUT<br>Additional: ADC012_IN13 |
| $V_{SSA}$ | J1 | P | - | Default: $V_{SSA}$ |
| $V_{REFN}$ | K1 | P | - | Default: $V_{REF-}$ |
| $V_{REFP}$ | L1 | P | - | Default: $V_{REF+}$ |
| $V_{DDA}$ | M1 | P | - | Default: $V_{DDA}$ |
| PA0-WKUP | L2 | I/O | 5VT | Default: PA0<br>Alternate:TIMER1_CH0, TIMER1_ETI, TIMER4_CH0, TIMER7_ETI, USART1_CTS, UART3_TX, ETH_MII_CRS, EVENTOUT<br>Additional: ADC012_IN0, WKUP |
| PA1 | M2 | I/O | 5VT | Default: PA1<br>Alternate:TIMER1_CH1, TIMER4_CH1, SPI3_MOSI, USART1_RTS, UART3_RX, ETH_MII_RX_CLK, ETH_RMII_REF_CLK, EVENTOUT<br>Additional: ADC012_IN1 |
| PA2 | K3 | I/O | 5VT | Default: PA2<br>Alternate:TIMER1_CH2, TIMER4_CH2, TIMER8_CH0, I2S_CKIN, USART1_TX, ETH_MDIO, EVENTOUT<br>Additional: ADC012_IN2 |
| PA3 | L3 | I/O | 5VT | Default: PA3<br>Alternate:TIMER1_CH3, TIMER4_CH3, TIMER8_CH1, I2S1_MCK, USART1_RX, USBHS_ULPI_D0, ETH_MII_COL, TLI_B5, EVENTOUT<br>Additional: ADC012_IN3 |
| NC | E3 | - | - | - |
| PA4 | M3 | I/O | TTa | Default: PA4<br>Alternate:SPI0_NSS, SPI2_NSS, I2S2_WS, USART1_CK, USBHS_SOF, DCI_HSYNC, TLI_VSYNC, EVENTOUT<br>Additional: ADC01_IN4, DAC_OUT0 |
| PA5 | K4 | I/O | TTa | Default: PA5<br>Alternate:TIMER1_CH0, TIMER1_ETI, TIMER7_CH0_ON, SPI0_SCK, USBHS_ULPI_CK, EVENTOUT<br>Additional: ADC01_IN5, DAC_OUT1 |
| PA6 | L4 | I/O | 5VT | Default: PA6<br>Alternate:TIMER0_BRKIN, TIMER2_CH0, TIMER7_BRKIN, SPI0_MISO, I2S1_MCK, TIMER12_CH0, SDIO_CMD, |



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| Pin Name | Pins | Pin Type(1) | I/O Level(2) | Functions description |
|---|---|---|---|---|
| | | | | DCI_PIXCLK, TLI_G2, EVENTOUT<br>Additional: ADC01_IN6 |
| PA7 | M4 | I/O | 5VT | Default: PA7<br>Alternate:TIMER0_CH0_ON, TIMER2_CH1, TIMER7_CH0_ON, SPI0_MOSI, TIMER13_CH0, ETH_MII_RX_DV, ETH_RMII_CRS_DV, EXMC_SDNWE, EVENTOUT<br>Additional: ADC01_IN7 |
| PC4 | K5 | I/O | 5VT | Default: PC4<br>Alternate: ETH_MII_RXD0, ETH_RMII_RXD0, EXMC_SDNE0, EVENTOUT<br>Additional: ADC01_IN14 |
| PC5 | L5 | I/O | 5VT | Default: PC5<br>Alternate:USART2_RX, ETH_MII_RXD1, ETH_RMII_RXD1, EXMC_SDCKE0, EVENTOUT<br>Additional: ADC01_IN15 |
| PB0 | M5 | I/O | 5VT | Default: PB0<br>Alternate:TIMER0_CH1_ON, TIMER2_CH2, TIMER7_CH1_ON, SPI4_SCK, SPI2_MOSI, I2S2_SD, TLI_R3, USBHS_ULPI_D1, ETH_MII_RXD2, SDIO_D1, EVENTOUT<br>Additional: ADC01_IN8, IREF |
| PB1 | M6 | I/O | 5VT | Default: PB1<br>Alternate:TIMER0_CH2_ON, TIMER2_CH3, TIMER7_CH2_ON, SPI4_NSS, TLI_R6, USBHS_ULPI_D2, ETH_MII_RXD3, SDIO_D2, EVENTOUT<br>Additional: ADC01_IN9 |
| PB2 | L6 | I/O | 5VT | Default: PB2, BOOT1<br>Alternate:TIMER1_CH3, SPI2_MOSI, I2S2_SD, USBHS_ULPI_D4, SDIO_CK, EVENTOUT |
| PE7 | M7 | I/O | 5VT | Default: PE7<br>Alternate: TIMER0_ETI, UART6_RX, EXMC_D4, EVENTOUT |
| PE8 | L7 | I/O | 5VT | Default: PE8<br>Alternate: TIMER0_CH0_ON, UART6_TX, EXMC_D5, EVENTOUT |
| PE9 | M8 | I/O | 5VT | Default: PE9<br>Alternate: TIMER0_CH0, EXMC_D6, EVENTOUT |
| PE10 | L8 | I/O | 5VT | Default: PE10<br>Alternate: TIMER0_CH1_ON, EXMC_D7, EVENTOUT |
| PE11 | M9 | I/O | 5VT | Default: PE11<br>Alternate:TIMER0_CH1, SPI3_NSS, SPI4_NSS, EXMC_D8, TLI_G3, EVENTOUT |
| PE12 | L9 | I/O | 5VT | Default: PE12<br>Alternate:TIMER0_CH2_ON, SPI3_SCK, SPI4_SCK, EXMC_D9, TLI_B4, EVENTOUT |



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| Pin Name | Pins | Pin Type(1) | I/O Level(2) | Functions description |
|---|---|---|---|---|
| PE13 | M10 | I/O | 5VT | Default: PE13<br>Alternate:TIMER0_CH2, SPI3_MISO, SPI4_MISO, EXMC_D10, TLI_DE, EVENTOUT |
| PE14 | M11 | I/O | 5VT | Default: PE14<br>Alternate:TIMER0_CH3, SPI3_MOSI, SPI4_MOSI, EXMC_D11, TLI_PIXCLK, EVENTOUT |
| PE15 | M12 | I/O | 5VT | Default: PE15<br>Alternate: TIMER0_BRKIN, EXMC_D12, TLI_R7, EVENTOUT |
| PB10 | L10 | I/O | 5VT | Default: PB10<br>Alternate:TIMER1_CH2, I2C1_SCL, SPI1_SCK, I2S1_CK, I2S2_MCK, USART2_TX, USBHS_ULPI_D3, ETH_MII_RX_ER, SDIO_D7, TLI_G4, EVENTOUT |
| PB11 | K9 | I/O | 5VT | Default: PB11<br>Alternate:TIMER1_CH3, I2C1_SDA, I2S_CKIN, USART2_RX, USBHS_ULPI_D4, ETH_MII_TX_EN, ETH_RMII_TX_EN, TLI_G5, EVENTOUT |
| NC | L11 | P | - | Default: $V_{CORE}$ |
| $V_{SS}$ | F12 | P | - | Default: $V_{SS}$ |
| $V_{DD}$ | G12 | P | - | Default: $V_{DD}$ |
| PB12 | L12 | I/O | 5VT | Default: PB12<br>Alternate:TIMER0_BRKIN, I2C1_SMBA, SPI1_NSS, I2S1_WS, SPI3_NSS, USART2_CK, CAN1_RX, USBHS_ULPI_D5, ETH_MII_TXD0, ETH_RMII_TXD0, USBHS_ID, EVENTOUT |
| PB13 | K12 | I/O | 5VT | Default: PB13<br>Alternate:TIMER0_CH0_ON, SPI1_SCK, I2S1_CK, SPI3_SCK, USART2_CTS, CAN1_TX, USBHS_ULPI_D6, ETH_MII_TXD1, ETH_RMII_TXD1, EVENTOUT, I2C1_TXFRAME<br>Additional: USBHS_VBUS |
| PB14 | K11 | I/O | 5VT | Default: PB14<br>Alternate:TIMER0_CH1_ON, TIMER7_CH1_ON, SPI1_MISO, I2S1_ADD_SD, USART2_RTS, TIMER11_CH0, USBHS_DM, EVENTOUT |
| PB15 | K10 | I/O | 5VT | Default: PB15<br>Alternate: RTC_REFIN, TIMER0_CH2_ON, TIMER7_CH2_ON, SPI1_MOSI, I2S1_SD, TIMER11_CH1, USBHS_DP, EVENTOUT |
| PD9 | K8 | I/O | 5VT | Default: PD9<br>Alternate: USART2_RX, EXMC_D14, EVENTOUT |
| PD10 | J12 | I/O | 5VT | Default: PD10<br>Alternate: USART2_CK, EXMC_D15, TLI_B3, EVENTOUT |
| PD11 | J11 | I/O | 5VT | Default: PD11<br>Alternate: USART2_CTS, EXMC_A16, EVENTOUT |



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| Pin Name | Pins | Pin Type(1) | I/O Level(2) | Functions description |
|---|---|---|---|---|
| PD12 | J10 | I/O | 5VT | Default: PD12<br>Alternate: TIMER3_CH0, USART2_RTS, EXMC_A17, EVENTOUT |
| PD13 | H12 | I/O | 5VT | Default: PD13<br>Alternate: TIMER3_CH1, EXMC_A18, EVENTOUT |
| PD14 | H11 | I/O | 5VT | Default: PD14<br>Alternate: TIMER3_CH2, EXMC_D0, EVENTOUT |
| PD15 | H10 | I/O | 5VT | Default: PD15<br>Alternate: TIMER3_CH3, EXMC_D1, EVENTOUT, CTC_SYNC |
| PC6 | E12 | I/O | 5VT | Default: PC6<br>Alternate:TIMER2_CH0, TIMER7_CH0, I2S1_MCK, USART5_TX, SDIO_D6, DCI_D0, TLI_HSYNC, EVENTOUT |
| PC7 | E11 | I/O | 5VT | Default: PC7<br>Alternate:TIMER2_CH1, TIMER7_CH1, SPI1_SCK, I2S1_CK, I2S2_MCK, USART5_RX, SDIO_D7, DCI_D1, TLI_G6, EVENTOUT |
| PC8 | E10 | I/O | 5VT | Default: PC8<br>Alternate:TRACED0, TIMER2_CH2, TIMER7_CH2, USART5_CK, SDIO_D0, DCI_D2, EVENTOUT |
| PC9 | D12 | I/O | 5VT | Default: PC9<br>Alternate:CK_OUT1, TIMER2_CH3, TIMER7_CH3, I2C2_SDA, I2S_CKIN, SDIO_D1, DCI_D3, EVENTOUT |
| PA8 | D11 | I/O | 5VT | Default: PA8<br>Alternate: CK_OUT0, TIMER0_CH0, I2C2_SCL, USART0_CK, USBFS_SOF, SDIO_D1, TLI_R6, EVENTOUT, CTC_SYNC |
| PA9 | D10 | I/O | 5VT | Default: PA9<br>Alternate:TIMER0_CH1, I2C2_SMBA, SPI1_SCK, I2S1_CK, USART0_TX, SDIO_D2, DCI_D0, EVENTOUT<br>Additional: USBFS_VBUS |
| PA10 | C12 | I/O | 5VT | Default: PA10<br>Alternate:TIMER0_CH2, SPI4_MOSI, USART0_RX, USBFS_ID, DCI_D1, EVENTOUT, I2C2_TXFRAME |
| PA11 | B12 | I/O | 5VT | Default: PA11<br>Alternate:TIMER0_CH3, SPI3_MISO, USART0_CTS, USART5_TX, CAN0_RX, USBFS_DM, TLI_R4, EVENTOUT |
| PA12 | A12 | I/O | 5VT | Default: PA12<br>Alternate:TIMER0_ETI, SPI4_MISO, USART0_RTS, USART5_RX, CAN0_TX, USBFS_DP, TLI_R5, EVENTOUT |
| PA13 | A11 | I/O | 5VT | Default: JTMS, SWDIO, PA13<br>Alternate: EVENTOUT |
| NC | C11 | - | - | - |
| $V_{SS}$ | F11 | P | - | Default: $V_{SS}$ |
| $V_{DD}$ | G11 | P | - | Default: $V_{DD}$ |



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| Pin Name | Pins | Pin Type(1) | I/O Level(2) | Functions description |
|---|---|---|---|---|
| PA14 | A10 | I/O | 5VT | Default: JTCK, SWCLK, PA14<br>Alternate: EVENTOUT |
| PA15 | A9 | I/O | 5VT | Default: JTDI, PA15<br>Alternate:TIMER1_CH0, TIMER1_ETI, SPI0_NSS, SPI2_NSS, I2S2_WS, USART0_TX, EVENTOUT |
| PC10 | B11 | I/O | 5VT | Default: PC10<br>Alternate:SPI2_SCK, I2S2_CK, USART2_TX, UART3_TX, SDIO_D2, DCI_D8, TLI_R2, EVENTOUT |
| PC11 | C10 | I/O | 5VT | Default: PC11<br>Alternate:I2S2_ADD_SD, SPI2_MISO, USART2_RX, UART3_RX, SDIO_D3, DCI_D4, EVENTOUT |
| PC12 | B10 | I/O | 5VT | Default: PC12<br>Alternate:I2C1_SDA, SPI2_MOSI, I2S2_SD, USART2_CK, UART4_TX, SDIO_CK, DCI_D9, EVENTOUT |
| PD0 | C9 | I/O | 5VT | Default: PD0<br>Alternate:SPI3_MISO, SPI2_MOSI, I2S2_SD, CAN0_RX, EXMC_D2, EVENTOUT |
| PD1 | B9 | I/O | 5VT | Default: PD1<br>Alternate: SPI1_NSS, I2S1_WS, CAN0_TX, EXMC_D3, EVENTOUT |
| PD2 | C8 | I/O | 5VT | Default: PD2<br>Alternate: TIMER2_ETI, UART4_RX, SDIO_CMD, DCI_D11, EVENTOUT |
| PD3 | B8 | I/O | 5VT | Default: PD3<br>Alternate:TRACED1, SPI1_SCK, I2S1_CK, USART1_CTS, EXMC_CLK, DCI_D5, TLI_G7, EVENTOUT |
| PD4 | B7 | I/O | 5VT | Default: PD4<br>Alternate: USART1_RTS, EXMC_NOE, EVENTOUT |
| PD5 | A6 | I/O | 5VT | Default: PD5<br>Alternate: USART1_TX, EXMC_NWE, EVENTOUT |
| PD6 | B6 | I/O | 5VT | Default: PD6<br>Alternate:SPI2_MOSI, I2S2_SD, USART1_RX, EXMC_NWAIT, DCI_D10, TLI_B2, EVENTOUT |
| PD7 | A5 | I/O | 5VT | Default: PD7<br>Alternate: USART1_CK, EXMC_NE0, EXMC_NCE1, EVENTOUT |
| PB3 | A8 | I/O | 5VT | Default: JTDO, PB3<br>Alternate: TRACESWO, TIMER1_CH1, SPI0_SCK, SPI2_SCK, I2S2_CK, USART0_RX, I2C1_SDA, EVENTOUT |
| PB4 | A7 | I/O | 5VT | Default: JNTRST, PB4<br>Alternate:TIMER2_CH0, SPI0_MISO, SPI2_MISO, I2S2_ADD_SD, I2C2_SDA, SDIO_D0, EVENTOUT, I2C0_TXFRAME |
| PB5 | C5 | I/O | 5VT | Default: PB5<br>Alternate:TIMER2_CH1, I2C0_SMBA, SPI0_MOSI, SPI2_MOSI, I2S2_SD, CAN1_RX, USBHS_ULPI_D7, |



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| Pin Name | Pins | Pin Type(1) | I/O Level(2) | Functions description |
|---|---|---|---|---|
| | | | | ETH_PPS_OUT, EXMC_SDCKE1, DCI_D10, EVENTOUT |
| PB6 | B5 | I/O | 5VT | Default: PB6<br>Alternate:TIMER3_CH0, I2C0_SCL, USART0_TX, CAN1_TX, EXMC_SDNE1, DCI_D5, EVENTOUT |
| PB7 | B4 | I/O | 5VT | Default: PB7<br>Alternate:TIMER3_CH1, I2C0_SDA, USART0_RX, EXMC_NL, DCI_VSYNC, EVENTOUT |
| BOOT0 | A4 | I/O | 5VT | Default: BOOT0 |
| PB8 | A3 | I/O | 5VT | Default: PB8<br>Alternate:TIMER1_CH0, TIMER1_ETI, TIMER3_CH2, TIMER9_CH0, I2C0_SCL, SPI4_MOSI, CAN0_RX, ETH_MII_TXD3, SDIO_D4, DCI_D6, TLI_B6, EVENTOUT |
| PB9 | B3 | I/O | 5VT | Default: PB9<br>Alternate:TIMER1_CH1, TIMER3_CH3, TIMER10_CH0, I2C0_SDA, SPI1_NSS, I2S1_WS, CAN0_TX, SDIO_D5, DCI_D7, TLI_B7, EVENTOUT |
| PE0 | C3 | I/O | 5VT | Default: PE0<br>Alternate: TIMER3_ETI, UART7_RX, EXMC_NBL0, DCI_D2, EVENTOUT |
| PE1 | A2 | I/O | 5VT | Default: PE1<br>Alternate: TIMER0_CH1_ON, UART7_TX, EXMC_NBL1, DCI_D3, EVENTOUT |
| $V_{SS}$ | D3 | P | - | Default: $V_{SS}$ |
| PDR_ON | H3 | P | - | Default: PDR_ON |
| $V_{DD}$ | C4 | P | - | Default: $V_{DD}$ |

**Notes:**

(1) Type: I = input, O = output, P = power.

(2) I/O Level: 5VT = 5 V tolerant.



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### 2.6.2. GD32F450VGH6 pin alternate functions

**Table 2-4. Port A alternate functions summary**

| Pin Name | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **PA0** | | TIMER1_CH0/TIMER1_ETI | TIMER4_CH0 | TIMER7_ETI | | | | USART1_CTS | UART3_TX | | | ETH_MII_CRS | | | | EVENTOUT |
| **PA1** | | TIMER1_CH1 | TIMER4_CH1 | | | SPI3_MOSI | | USART1_RTS | UART3_RX | | | ETH_MII_RX_CLK/ETH_RMII_REF_CLK | | | | EVENTOUT |
| **PA2** | | TIMER1_CH2 | TIMER4_CH2 | TIMER8_CH0 | | I2S_CKIN | | USART1_TX | | | | ETH_MDIO | | | | EVENTOUT |
| **PA3** | | TIMER1_CH3 | TIMER4_CH3 | TIMER8_CH1 | | I2S1_MCK | | USART1_RX | | | USBHS_ULPI_D0 | ETH_MII_COL | | | TLI_B5 | EVENTOUT |
| **PA4** | | | | | | SPI0_NSS | SPI2_NSS/I2S2_WS | USART1_CK | | | | | USBHS_SOF | DCI_HSYNC | TLI_VSYNC | EVENTOUT |
| **PA5** | | TIMER1_CH0/TIMER1_ETI | | TIMER7_CH0_ON | | SPI0_SCK | | | | | USBHS_ULPI_CK | | | | | EVENTOUT |
| **PA6** | | TIMER0_BRKIN | TIMER2_CH0 | TIMER7_BRKIN | | SPI0_MISO | I2S1_MCK | | | TIMER12_CH0 | | | SDIO_CMD | DCI_PIXCLK | TLI_G2 | EVENTOUT |
| **PA7** | | TIMER0_CH0_ON | TIMER2_CH1 | TIMER7_CH0_ON | | SPI0_MOSI | | | | TIMER13_CH0 | | ETH_MII_RX_DV/ETH_RMII_CRS_DV | EXMC_SDNWE | | | EVENTOUT |
| **PA8** | CK_OUT0 | TIMER0_CH0 | | | I2C2_SCL | | | USART0_CK | | CTC_SYNC | USBFS_SOF | | SDIO_D1 | | TLI_R6 | EVENTOUT |
| **PA9** | | TIMER0_CH1 | | | I2C2_SMBA | SPI1_SCK/I2S1_CK | | USART0_TX | | | | | SDIO_D2 | DCI_D0 | | EVENTOUT |
| **PA10** | | TIMER0_CH2 | | | I2C2_TXFRAME | | SPI4_MOSI | USART0_RX | | | USBFS_ID | | | DCI_D1 | | EVENTOUT |
| **PA11** | | TIMER0_CH3 | | | | | SPI3_MISO | USART0_CTS | USART5_TX | CAN0_RX | USBFS_DM | | | | TLI_R4 | EVENTOUT |
| **PA12** | | TIMER0_ETI | | | | | SPI4_MISO | USART0_RTS | USART5_RX | CAN0_TX | USBFS_DP | | | | TLI_R5 | EVENTOUT |
| **PA13** | JTMS/SWDIO | | | | | | | | | | | | | | | EVENTOUT |
| **PA14** | JTCK/SWCLK | | | | | | | | | | | | | | | EVENTOUT |



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| Pin Name | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **PA15** | JTDI | TIMER1_CH0 /TIMER1_ETI | | | | SPI0_NSS | SPI2_NSS/I2S2_WS | USART0_TX | | | | | | | | EVENTOUT |

**Table 2-5. Port B alternate functions summary**

| Pin Name | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **PB0** | | TIMER0_CH1_ON | TIMER2_CH2 | TIMER7_CH1_ON | | | SPI4_SCK | SPI2_MOSI /I2S2_SD | | TLI_R3 | USBHS_ULPI_D1 | ETH_MII_RXD2 | SDIO_D1 | | | EVENTOUT |
| **PB1** | | TIMER0_CH2_ON | TIMER2_CH3 | TIMER7_CH2_ON | | | SPI4_NSS | | | TLI_R6 | USBHS_ULPI_D2 | ETH_MII_RXD3 | SDIO_D2 | | | EVENTOUT |
| **PB2** | | TIMER1_CH3 | | | | | | SPI2_MOSI /I2S2_SD | | | USBHS_ULPI_D4 | | SDIO_CK | | | EVENTOUT |
| **PB3** | JTDO/TRACESWO | TIMER1_CH1 | | | | SPI0_SCK | SPI2_SCK /I2S2_CK | USART0_RX | | I2C1_SDA | | | | | | EVENTOUT |
| **PB4** | JNTRST | | TIMER2_CH0 | | I2C0_TXFRAME | SPI0_MISO | SPI2_MISO | I2S2_ADD_SD | | I2C2_SDA | | | SDIO_D0 | | | EVENTOUT |
| **PB5** | | | TIMER2_CH1 | | I2C0_SMBA | SPI0_MOSI | SPI2_MOSI/I2S2_SD | | | CAN1_RX | USBHS_ULPI_D7 | ETH_PPS_OUT | EXMC_SDCKE1 | DCI_D10 | | EVENTOUT |
| **PB6** | | | TIMER3_CH0 | | I2C0_SCL | | | USART0_TX | | CAN1_TX | | | EXMC_SDNE1 | DCI_D5 | | EVENTOUT |
| **PB7** | | | TIMER3_CH1 | | I2C0_SDA | | | USART0_RX | | | | | EXMC_NL | DCI_VSYNC | | EVENTOUT |
| **PB8** | | TIMER1_CH0/TIMER1_ETI | TIMER3_CH2 | TIMER9_CH0 | I2C0_SCL | | SPI4_MOSI | | | CAN0_RX | | ETH_MII_TXD3 | SDIO_D4 | DCI_D6 | TLI_B6 | EVENTOUT |
| **PB9** | | TIMER1_CH1 | TIMER3_CH3 | TIMER10_CH0 | I2C0_SDA | SPI1_NSS /I2S1_WS | | | | CAN0_TX | | | SDIO_D5 | DCI_D7 | TLI_B7 | EVENTOUT |
| **PB10** | | TIMER1_CH2 | | | I2C1_SCL | SPI1_SCK /I2S1_CK | I2S2_MCK | USART2_TX | | | USBHS_ULPI_D3 | ETH_MII_RX_ER | SDIO_D7 | | TLI_G4 | EVENTOUT |
| **PB11** | | TIMER1_CH3 | | | I2C1_SDA | I2S_CKIN | | USART2_RX | | | USBHS_ULPI_D4 | ETH_MII_TX_EN/ETH_RMII_TX_EN | | | TLI_G5 | EVENTOUT |
| **PB12** | | TIMER0_BRKIN | | | I2C1_SMBA | SPI1_NSS /I2S1_WS | SPI3_NSS | USART2_CK | | CAN1_RX | USBHS_ULPI_D5 | ETH_MII_TXD0/ETH_RMII_TXD0 | USBHS_ID | | | EVENTOUT |
| **PB13** | | TIMER0_CH0_ON | | | I2C1_TXFRAME | SPI1_SCK /I2S1_CK | SPI3_SCK | USART2_CTS | | CAN1_TX | USBHS_ULPI_D6 | ETH_MII_TXD1/ETH_RMII_TXD1 | | | | EVENTOUT |



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| Pin Name | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **PB14** | | TIMER0_CH1_ON | | TIMER7_CH1_ON | | SPI1_MISO | I2S1_ADD_SD | USART2_RTS | | TIMER11_CH0 | | | USBHS_DM | | | EVENTOUT |
| **PB15** | RTC_REFIN | TIMER0_CH2_ON | | TIMER7_CH2_ON | | SPI1_MOSI/I2S1_SD | | | | TIMER11_CH1 | | | USBHS_DP | | | EVENTOUT |

**Table 2-6. Port C alternate functions summary**

| Pin Name | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **PC0** | | | | | | | | | | | USBHS_ULPI_STP | | EXMC_SDNWE | | | EVENTOUT |
| **PC1** | | | | | | SPI2_MOSI/I2S2_SD | | SPI1_MOSI/I2S1_SD | | | | ETH_MDC | | | | EVENTOUT |
| **PC2** | | | | | | SPI1_MISO | I2S1_ADD_SD | | | | USBHS_ULPI_DIR | ETH_MII_TXD2 | EXMC_SDNE0 | | | EVENTOUT |
| **PC3** | | | | | | SPI1_MOSI/I2S1_SD | | | | | USBHS_ULPI_NXT | ETH_MII_TX_CLK | EXMC_SDCKE0 | | | EVENTOUT |
| **PC4** | | | | | | | | | | | | ETH_MII_RXD0/ETH_RMII_RXD0 | EXMC_SDNE0 | | | EVENTOUT |
| **PC5** | | | | | | | | USART2_RX | | | | ETH_MII_RXD1/ETH_RMII_RXD1 | EXMC_SDCKE0 | | | EVENTOUT |
| **PC6** | | | TIMER2_CH0 | TIMER7_CH0 | | I2S1_MCK | | | USART5_TX | | | | SDIO_D6 | DCI_D0 | TLI_HSYNC | EVENTOUT |
| **PC7** | | | TIMER2_CH1 | TIMER7_CH1 | | SPI1_SCK/I2S1_CK | I2S2_MCK | | USART5_RX | | | | SDIO_D7 | DCI_D1 | TLI_G6 | EVENTOUT |
| **PC8** | TRACED0 | | TIMER2_CH2 | TIMER7_CH2 | | | | | USART5_CK | | | | SDIO_D0 | DCI_D2 | | EVENTOUT |
| **PC9** | CK_OUT1 | | TIMER2_CH3 | TIMER7_CH3 | I2C2_SDA | I2S_CKIN | | | | | | | SDIO_D1 | DCI_D3 | | EVENTOUT |
| **PC10** | | | | | | | SPI2_SCK/I2S2_CK | USART2_TX | UART3_TX | | | | SDIO_D2 | DCI_D8 | TLI_R2 | EVENTOUT |
| **PC11** | | | | | | I2S2_ADD_SD | SPI2_MISO | USART2_RX | UART3_RX | | | | SDIO_D3 | DCI_D4 | | EVENTOUT |



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|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PC12 | | | | | I2C1_SDA | | SPI2_MOSI/I2S2_SD | USART2_CK | UART4_TX | | | | SDIO_CK | DCI_D9 | | EVENTOUT |
| PC13 | | | | | | | | | | | | | | | | EVENTOUT |
| PC14 | | | | | | | | | | | | | | | | EVENTOUT |
| PC15 | | | | | | | | | | | | | | | | EVENTOUT |

**Table 2-7. Port D alternate functions summary**

| Pin Name | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PD0 | | | | | | SPI3_MISO | SPI2_MOSI/I2S2_SD | | | CAN0_RX | | | EXMC_D2 | | | EVENTOUT |
| PD1 | | | | | | | | SPI1_NSS/I2S1_WS | | CAN0_TX | | | EXMC_D3 | | | EVENTOUT |
| PD2 | | | TIMER2_ETI | | | | | | UART4_RX | | | | SDIO_CMD | DCI_D11 | | EVENTOUT |
| PD3 | TRACED1 | | | | | SPI1_SCK/I2S1_CK | | USART1_CTS | | | | | EXMC_CLK | DCI_D5 | TLI_G7 | EVENTOUT |
| PD4 | | | | | | | | USART1_RTS | | | | | EXMC_NOE | | | EVENTOUT |
| PD5 | | | | | | | | USART1_TX | | | | | EXMC_NWE | | | EVENTOUT |
| PD6 | | | | | | SPI2_MOSI/I2S2_SD | | USART1_RX | | | | | EXMC_NWAIT | DCI_D10 | TLI_B2 | EVENTOUT |
| PD7 | | | | | | | | USART1_CK | | | | | EXMC_NE0/EXMC_NCE1 | | | EVENTOUT |
| PD8 | | | | | | | | USART2_TX | | | | | EXMC_D13 | | | EVENTOUT |
| PD9 | | | | | | | | USART2_RX | | | | | EXMC_D14 | | | EVENTOUT |
| PD10 | | | | | | | | USART2_CK | | | | | EXMC_D15 | | TLI_B3 | EVENTOUT |
| PD11 | | | | | | | | USART2_CTS | | | | | EXMC_A16 | | | EVENTOUT |



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|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **PD12** | | | TIMER3_CH0 | | | | | USART2_RTS | | | | | EXMC_A17 | | | EVENTOUT |
| **PD13** | | | TIMER3_CH1 | | | | | | | | | | EXMC_A18 | | | EVENTOUT |
| **PD14** | | | TIMER3_CH2 | | | | | | | | | | EXMC_D0 | | | EVENTOUT |
| **PD15** | CTC_SYNC | | TIMER3_CH3 | | | | | | | | | | EXMC_D1 | | | EVENTOUT |

**Table 2-8. Port E alternate functions summary**

| Pin Name | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **PE0** | | | TIMER3_ETI | | | | | | UART7_RX | | | | EXMC_NBL0 | DCI_D2 | | EVENTOUT |
| **PE1** | | TIMER0_CH1_ON | | | | | | | UART7_TX | | | | EXMC_NBL1 | DCI_D3 | | EVENTOUT |
| **PE2** | TRACECLK | | | | | SPI3_SCK | | | | | | ETH_MII_TXD3 | EXMC_A23 | | | EVENTOUT |
| **PE3** | TRACED0 | | | | | | | | | | | | EXMC_A19 | | | EVENTOUT |
| **PE4** | TRACED1 | | | | | SPI3_NSS | | | | | | | EXMC_A20 | DCI_D4 | TLI_B0 | EVENTOUT |
| **PE5** | TRACED2 | | | TIMER8_CH0 | | SPI3_MISO | | | | | | | EXMC_A21 | DCI_D6 | TLI_G0 | EVENTOUT |
| **PE6** | TRACED3 | | | TIMER8_CH1 | | SPI3_MOSI | | | | | | | EXMC_A22 | DCI_D7 | TLI_G1 | EVENTOUT |
| **PE7** | | TIMER0_ETI | | | | | | | UART6_RX | | | | EXMC_D4 | | | EVENTOUT |
| **PE8** | | TIMER0_CH0_ON | | | | | | | UART6_TX | | | | EXMC_D5 | | | EVENTOUT |
| **PE9** | | TIMER0_CH0 | | | | | | | | | | | EXMC_D6 | | | EVENTOUT |
| **PE10** | | TIMER0_CH1_ON | | | | | | | | | | | EXMC_D7 | | | EVENTOUT |
| **PE11** | | TIMER0_CH1 | | | | SPI3_NSS | SPI4_NSS | | | | | | EXMC_D8 | | TLI_G3 | EVENTOUT |



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|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **PE12** | | TIMER0_CH2_ON | | | | SPI3_SCK | SPI4_SCK | | | | | | EXMC_D9 | | TLI_B4 | EVENTOUT |
| **PE13** | | TIMER0_CH2 | | | | SPI3_MISO | SPI4_MISO | | | | | | EXMC_D10 | | TLI_DE | EVENTOUT |
| **PE14** | | TIMER0_CH3 | | | | SPI3_MOSI | SPI4_MOSI | | | | | | EXMC_D11 | | TLI_PIXCLK | EVENTOUT |
| **PE15** | | TIMER0_BRKIN | | | | | | | | | | | EXMC_D12 | | TLI_R7 | EVENTOUT |

**Table 2-9. Port F alternate functions summary**

| Pin Name | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **PF0** | CTC_SYNC | | | | I2C1_SDA | | | | | | | | EXMC_A0 | | | EVENTOUT |
| **PF1** | | | | | I2C1_SCL | | | | | | | | EXMC_A1 | | | EVENTOUT |
| **PF2** | | | | | I2C1_SMBA | | | | | | | | EXMC_A2 | | | EVENTOUT |
| **PF3** | | | | | I2C1_TXFRAME | | | | | | | | EXMC_A3 | | | EVENTOUT |
| **PF4** | | | | | | | | | | | | | EXMC_A4 | | | EVENTOUT |
| **PF5** | | | | | | | | | | | | | EXMC_A5 | | | EVENTOUT |
| **PF6** | | | | TIMER9_CH0 | | SPI4_NSS | | | UART6_RX | | | | EXMC_NIORD | | | EVENTOUT |
| **PF7** | | | | TIMER10_CH0 | | SPI4_SCK | | | UART6_TX | | | | EXMC_NREG | | | EVENTOUT |
| **PF8** | | | | | | SPI4_MISO | | | | TIMER12_CH0 | | | EXMC_NIOWR | | | EVENTOUT |
| **PF9** | | | | | | SPI4_MOSI | | | | TIMER13_CH0 | | | EXMC_CD | | | EVENTOUT |
| **PF10** | | | | | | | | | | | | | EXMC_INTR | DCI_D11 | TLI_DE | EVENTOUT |
| **PF11** | | | | | | SPI4_MOSI | | | | | | | EXMC_SDNRAS | DCI_D12 | | EVENTOUT |



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|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PF12 | | | | | | | | | | | | | EXMC_A6 | | | EVENTOUT |
| PF13 | | | | | | | | | | | | | EXMC_A7 | | | EVENTOUT |
| PF14 | | | | | | | | | | | | | EXMC_A8 | | | EVENTOUT |
| PF15 | | | | | | | | | | | | | EXMC_A9 | | | EVENTOUT |

**Table 2-10. Port G alternate functions summary**

| Pin Name | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PG0 | | | | | | | | | | | | | EXMC_A10 | | | EVENTOUT |
| PG1 | | | | | | | | | | | | | EXMC_A11 | | | EVENTOUT |
| PG2 | | | | | | | | | | | | | EXMC_A12 | | | EVENTOUT |
| PG3 | | | | | | | | | | | | | EXMC_A13 | | | EVENTOUT |
| PG4 | | | | | | | | | | | | | EXMC_A14 | | | EVENTOUT |
| PG5 | | | | | | | | | | | | | EXMC_A15 | | | EVENTOUT |
| PG6 | | | | | | | | | | | | | EXMC_INT1 | DCI_D12 | TLI_R7 | EVENTOUT |
| PG7 | | | | | | | | | USART5_CK | | | | EXMC_INT2 | DCI_D13 | TLI_PIXCLK | EVENTOUT |
| PG8 | | | | | | SPI5_NSS | | | USART5_RTS | | | ETH_PPS_OUT | EXMC_SDCLK | | | EVENTOUT |
| PG9 | | | | | | | | | USART5_RX | | | | EXMC_NE1/EXMC_NCE2 | DCI_VSYNC | | EVENTOUT |
| PG10 | | | | | | SPI5_IO2 | | | | TLI_G3 | | | EXMC_NCE3_0/EXMC_NE2 | DCI_D2 | TLI_B2 | EVENTOUT |
| PG11 | | | | | | SPI5_IO3 | SPI3_SCK | | | | | ETH_MII_TX_EN/ET | EXMC_NCE3_1 | DCI_D3 | TLI_B3 | EVENTOUT |



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|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | | | H_RMII_TX_EN | | | | |
| **PG12** | | | | | | SPI5_MISO | SPI3_MISO | | USART5_RTS | TLI_B4 | | | EXMC_NE3 | | TLI_B1 | EVENTOUT |
| **PG13** | TRACED2 | | | | | SPI5_SCK | SPI3_MOSI | | USART5_CTS | | | ETH_MII_TXD0/ETH_RMII_TXD0 | EXMC_A24 | | | EVENTOUT |
| **PG14** | TRACED3 | | | | | SPI5_MOSI | SPI3_NSS | | USART5_TX | | | ETH_MII_TXD1/ETH_RMII_TXD1 | EXMC_A25 | | | EVENTOUT |
| **PG15** | | | | | | | | | USART5_CTS | | | | EXMC_SDNCAS | DCI_D13 | | EVENTOUT |

**Table 2-11. Port H alternate functions summary**

| Pin Name | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **PH0** | | | | | | | | | | | | | | | | EVENTOUT |
| **PH1** | | | | | | | | | | | | | | | | EVENTOUT |
| **PH2** | | | | | | | | | | | | ETH_MII_CRS | EXMC_SDCKE0 | | TLI_R0 | EVENTOUT |
| **PH3** | | | | | I2C1_TXFRAME | | | | | | | ETH_MII_COL | EXMC_SDNE0 | | TLI_R1 | EVENTOUT |
| **PH4** | | | | | I2C1_SCL | | | | | | USBHS_ULPI_NXT | | | | | EVENTOUT |
| **PH5** | | | | | I2C1_SDA | SPI4_NSS | | | | | | | EXMC_SDNWE | | | EVENTOUT |
| **PH6** | | | | | I2C1_SMBA | SPI4_SCK | | | | TIMER11_CH0 | | ETH_MII_RXD2 | EXMC_SDNE1 | DCI_D8 | | EVENTOUT |
| **PH7** | | | | | I2C2_SCL | SPI4_MISO | | | | | | ETH_MII_RXD3 | EXMC_SDCKE1 | DCI_D9 | | EVENTOUT |
| **PH8** | | | | | I2C2_SDA | | | | | | | | EXMC_D16 | DCI_HSYNC | TLI_R2 | EVENTOUT |



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| Pin Name | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **PH9** | | | | | I2C2_SMBA | | | | | TIMER11_CH1 | | | EXMC_D17 | DCI_D0 | TLI_R3 | EVENTOUT |
| **PH10** | | | TIMER4_CH0 | | I2C2_TXFRAME | | | | | | | | EXMC_D18 | DCI_D1 | TLI_R4 | EVENTOUT |
| **PH11** | | | TIMER4_CH1 | | | | | | | | | | EXMC_D19 | DCI_D2 | TLI_R5 | EVENTOUT |
| **PH12** | | | TIMER4_CH2 | | | | | | | | | | EXMC_D20 | DCI_D3 | TLI_R6 | EVENTOUT |
| **PH13** | | | | TIMER7_CH0_ON | | | | | | CAN0_TX | | | EXMC_D21 | | TLI_G2 | EVENTOUT |
| **PH14** | | | | TIMER7_CH1_ON | | | | | | | | | EXMC_D22 | DCI_D4 | TLI_G3 | EVENTOUT |
| **PH15** | | | | TIMER7_CH2_ON | | | | | | | | | EXMC_D23 | DCI_D11 | TLI_G4 | EVENTOUT |

**Table 2-12. Port I alternate functions summary**

| Pin Name | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **PI0** | | | TIMER4_CH3 | | | SPI1_NSS/I2S1_WS | | | | | | | EXMC_D24 | DCI_D13 | TLI_G5 | EVENTOUT |
| **PI1** | | | | | | SPI1_SCK/I2S1_CK | | | | | | | EXMC_D25 | DCI_D8 | TLI_G6 | EVENTOUT |
| **PI2** | | | | TIMER7_CH3 | | SPI1_MISO | I2S1_ADD_SD | | | | | | EXMC_D26 | DCI_D9 | TLI_G7 | EVENTOUT |
| **PI3** | | | | TIMER7_ETI | | SPI1_MOSI/I2S1_SD | | | | | | | EXMC_D27 | DCI_D10 | | EVENTOUT |
| **PI4** | | | | TIMER7_BRKIN | | | | | | | | | EXMC_NBL2 | DCI_D5 | TLI_B4 | EVENTOUT |
| **PI5** | | | | TIMER7_CH0 | | | | | | | | | EXMC_NBL3 | DCI_VSYNC | TLI_B5 | EVENTOUT |
| **PI6** | | | | TIMER7_CH1 | | | | | | | | | EXMC_D28 | DCI_D6 | TLI_B6 | EVENTOUT |
| **PI7** | | | | TIMER7_CH2 | | | | | | | | | EXMC_D29 | DCI_D7 | TLI_B7 | EVENTOUT |



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|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **PI8** | | | | | | | | | | | | | | | | EVENTOUT |
| **PI9** | | | | | | | | | | CAN0_RX | | | EXMC_D30 | | TLI_VSYNC | EVENTOUT |
| **PI10** | | | | | | | | | | | | ETH_MII_RX_ER | EXMC_D31 | | TLI_HSYNC | EVENTOUT |
| **PI11** | | | | | | | | | | | USBHS_ULPI_DIR | | | | | EVENTOUT |



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# 3. Functional description

## 3.1. ARM® Cortex®-M4 core

The ARM® Cortex®-M4 processor is a high performance embedded processor with DSP instructions which allow efficient signal processing and complex algorithm execution. It brings an efficient, easy-to-use blend of control and signal processing capabilities to meet the digital signal control markets demand. The processor is highly configurable enabling a wide range of implementations from those requiring floating point operations, memory protection and powerful trace technology to cost sensitive devices requiring minimal area, while delivering outstanding computational performance and an advanced system response to interrupts.

32-bit ARM® Cortex®-M4 processor core

- Up to 200 MHz operation frequency
- Single-cycle multiplication and hardware divider
- Floating Point Unit (FPU)
- Integrated DSP instructions
- Integrated Nested Vectored Interrupt Controller (NVIC)
- 24-bit SysTick timer

The Cortex®-M4 processor is based on the ARMv7-M architecture and supports both Thumb and Thumb-2 instruction sets. Some system peripherals listed below are also provided by Cortex®-M4:

- Internal Bus Matrix connected with ICode bus, DCode bus, system bus, Private Peripheral Bus (PPB) and debug accesses (AHB-AP)
- Nested Vectored Interrupt Controller (NVIC)
- Flash Patch and Breakpoint (FPB)
- Data Watchpoint and Trace (DWT)
- Instrument Trace Macrocell (ITM)
- Memory Protection Unit (MPU)
- Serial Wire JTAG Debug Port (SWJ-DP)
- Trace Port Interface Unit (TPIU)

## 3.2. On-chip memory

- Up to 1024 Kbytes of Flash memory, including code Flash and data Flash
- 256 KB of SRAM

The ARM® Cortex®-M4 processor is structured in Harvard architecture which can use separate buses to fetch instructions and load/store data. 1024 Kbytes of inner Flash at most, which includes code Flash and data Flash is available for storing programs and data, and accessed (R/W) at CPU clock speed with zero wait states. Up to 256 Kbytes of inner SRAM



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that can be accessed at same time, and including 64 KB of TCM (tightly-coupled memory) data RAM that can be accessed only by the data bus of the Cortex®-M4 core. The additional 4KB of backup SRAM (BKP SRAM) is implemented in the backup domain, which can keep its content even when the $V_{DD}$ power supply is down. ***Table 2-2. GD32F450VGH6 memory map*** shows the memory map of the GD32F450VGH6 series of devices, including Flash, SRAM, peripheral, and other pre-defined regions.

## 3.3. Clock, reset and supply management

- Internal 16 MHz factory-trimmed RC and external 4 to 32 MHz crystal oscillator
- Internal 48 MHz RC oscillator
- Internal 32 KHz RC calibrated oscillator and external 32.768 KHz crystal oscillator
- Integrated system clock PLL
- 2.6 to 3.6 V application supply and I/Os
- Supply Supervisor: POR (Power On Reset), PDR (Power Down Reset), and low voltage detector (LVD)

The Clock Control Unit (CCU) provides a range of oscillator and clock functions. These include internal RC oscillator and external crystal oscillator, high speed and low speed two types. Several prescalers allow the frequency configuration of the AHB and two APB domains. The maximum frequency of the two AHB domains are 200 MHz. The maximum frequency of the two APB domains including APB1 is 50 MHz and APB2 is 100 MHz. See ***Figure 2-5. GD32F450VGH6 clock tree*** for details on the clock tree.

The Reset Control Unit (RCU) controls three kinds of reset: system reset resets the processor core and peripheral IP components. Power-on reset (POR) and power-down reset (PDR) are always active, and ensures proper operation starting from 2.4 V and down to 1.8V. The device remains in reset mode when $V_{DD}$ is below a specified threshold. The embedded low voltage detector (LVD) monitors the power supply, compares it to the voltage threshold and generates an interrupt as a warning message for leading the MCU into security.

Power supply schemes:

- $V_{DD}$ range: 2.6 to 3.6 V, external power supply for I/Os and the internal regulator. Provided externally through $V_{DD}$ pins.
- $V_{SSA}$, $V_{DDA}$ range: 2.6 to 3.6 V, external analog power supplies for ADC, reset blocks, RCs and PLL. $V_{DDA}$ and $V_{SSA}$ must be connected to $V_{DD}$ and $V_{SS}$, respectively.
- $V_{BAT}$ range: 1.8 to 3.6 V, power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when $V_{DD}$ is not present.

## 3.4. Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from main Flash memory (default)
- Boot from system memory



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- Boot from on-chip SRAM

The boot loader is located in the internal 30KB of information blocks for the boot ROM memory (system memory). It is used to reprogram the Flash memory by using USART0 (PA9 and PA10), USART2 (PB10 and PB11, or PC10 and PC11), and USBFS (PA9, PA10, PA11 and PA12) in device mode. It also can be used to transfer and update the Flash memory code, the data and the vector table sections. In default condition, boot from bank 0 of Flash memory is selected. It also supports to boot from bank 1 of Flash memory by setting a bit in option bytes.

## 3.5. Power saving modes

The MCU supports three kinds of power saving modes to achieve even lower power consumption. They are sleep mode, deep-sleep mode, and standby mode. These operating modes reduce the power consumption and allow the application to achieve the best balance between the CPU operating time, speed and power consumption.

- **Sleep** mode
  In sleep mode, only the clock of CPU core is off. All peripherals continue to operate and any interrupt/event can wake up the system.
- **Deep-sleep** mode
  In deep-sleep mode, all clocks in the 1.2V domain are off, and all of the high speed crystal oscillator (IRC16M, HXTAL) and PLL are disabled. Only the contents of SRAM and registers are retained. Any interrupt or wakeup event from EXTI lines can wake up the system from the deep-sleep mode including the 23 external lines, the RTC alarm, the LVD output, and USB wakeup. When exiting the deep-sleep mode, the IRC16M is selected as the system clock.
- **Standby** mode
  In standby mode, the whole 1.2V domain is power off, the LDO is shut down, and all of IRC16M, HXTAL and PLL are disabled. The contents of SRAM and registers (except backup registers) are lost. There are four wakeup sources for the standby mode, including the external reset from NRST pin, the RTC, the FWDGT reset, and the rising edge on WKUP pin.

## 3.6. Analog to digital converter (ADC)

- 12-bit SAR ADC's conversion rate is up to 2.6MSPS
- 12-bit, 10-bit, 8-bit or 6-bit configurable resolution
- Hardware oversampling ratio adjustable from 2 to 256x improves resolution to 16-bit
- Input voltage range: $V_{SSA}$ to $V_{DDA}$ (2.6 to 3.6 V)
- Temperature sensor

Up to three 12-bit 2.6MSPS multi-channel ADCs are integrated in the device. It has a total of 19 multiplexed channels: 16 external channels, 1 channel for internal temperature sensor



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($V_{SENSE}$), 1 channel for internal reference voltage ($V_{REFINT}$) and 1 channel for external battery power supply ($V_{BAT}$). The input voltage range is between 2.6 V and 3.6 V. An on-chip hardware oversampling scheme improves performance while off-loading the related computational burden from the CPU. An analog watchdog block can be used to detect the channels, which are required to remain within a specific threshold window. A configurable channel management block can be used to perform conversions in single, continuous, scan or discontinuous mode to support more advanced use.

The ADC can be triggered from the events generated by the general-purpose level 0 timers (TIMERx) and the advanced-control timers (TIMER0 and TIMER7) with internal connection. The temperature sensor can be used to generate a voltage that varies linearly with temperature. It is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage in a digital value.

## 3.7. Digital to analog converter (DAC)

- Two 12-bit DAC converter of independent output channel
- 8-bit or 12-bit mode in conjunction with the DMA controller

The 12-bit buffered DAC channel is used to generate variable analog outputs. The DACs are designed with integrated resistor strings structure. The DAC channels can be triggered by the timer update outputs or EXTI with DMA support. The maximum output value of the DAC is $V_{REF+}$.

## 3.8. DMA

- 16 channels DMA controller and each channel are configurable (8 for DMA0 and 8 for DMA1)
- Support independent 8, 16, 32-bit memory and peripheral transfer
- Peripherals supported: Timers, ADC, SPIs, I2Cs, USARTs, UARTs, DAC, I2S, SDIO and DCI

The flexible general-purpose DMA controllers provide a hardware method of transferring data between peripherals and/or memory without intervention from the CPU, thereby freeing up bandwidth for other system functions. Three types of access method are supported: peripheral to memory, memory to peripheral, memory to memory

Each channel is connected to fixed hardware DMA requests. The priorities of DMA channel requests are determined by software configuration and hardware channel number. Transfer size of source and destination are independent and configurable.

## 3.9. General-purpose inputs/outputs (GPIOs)

- Up to 140 fast GPIOs, all mappable on 16 external interrupt vectors (EXTI)



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- Analog input/output configurable
- Alternate function input/output configurable

There are up to 140 general purpose I/O pins (GPIO) in GD32F450VGH6, named PA0 ~ PA15, PB0 ~ PB15, PC0 ~ PC15, PD0 ~ PD15, PE0 ~ PE15, PF0 ~ PF15, PG0 ~ PG15, PH0 ~ PH15 and PI0 ~ PI11 to implement logic input/output functions. Each of the GPIO ports has related control and configuration registers to satisfy the requirements of specific applications. The external interrupts on the GPIO pins of the device have related control and configuration registers in the External Interrupt Control Unit (EXTI). The GPIO ports are pin-shared with other alternative functions (AFs) to obtain maximum flexibility on the package pins. Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current capable except for analog inputs.

## 3.10. Timers and PWM generation

- Two 16-bit advanced-control timer (TIMER0 & TIMER7), eight 16-bit general-purpose timers (TIMER2, TIMER3, TIMER8 ~ TIMER13), two 32-bit general-purpose timers (TIMER1 & TIMER4) and two 16-bit basic timer (TIMER5 & TIMER6)
- Up to 4 independent channels of PWM, output compare or input capture for each general-purpose timer (GPTM) and external trigger input
- 16-bit, motor control PWM advanced-control timer with programmable dead-time generation for output match
- Encoder interface controller with two inputs using quadrature decoder
- 24-bit SysTick timer down counter
- 2 watchdog timers (free watchdog timer and window watchdog timer)

The advanced-control timer (TIMER0 & TIMER7) can be used as a three-phase PWM multiplexed on 6 channels. It has complementary PWM outputs with programmable dead-time generation. It can also be used as a complete general-purpose timer. The 4 independent channels can be used for input capture, output compare, PWM generation (edge- or center-aligned counting modes) and single pulse mode output. If configured as a general-purpose 16-bit timer, it has the same functions as the TIMERx timer. It can be synchronized with external signals or to interconnect with other GPTMs together which have the same architecture and features.

The general-purpose timer (GPTM), can be used for a variety of purposes including general time, input signal pulse width measurement or output waveform generation such as a single pulse generation or PWM output, up to 4 independent channels for input capture/output compare. TIMER1 & TIMER4 is based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler. TIMER2 & TIMER3 is based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. TIMER8 ~ TIMER13 is based on a 16-bit auto-reload upcounter and a 16-bit prescaler. The GPTM also supports an encoder interface with two inputs using quadrature



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decoder.

The basic timer, known as TIMER5 & TIMER6, are mainly used for DAC trigger generation. They can also be used as a simple 16-bit time base.

The GD32F450VGH6 have two watchdog peripherals, free watchdog timer and window watchdog timer. They offer a combination of high safety level, flexibility of use and timing accuracy.

The free watchdog timer includes a 12-bit down-counting counter and an 8-bit prescaler, It is clocked from an independent 32 kHz internal RC and as it operates independently of the main clock, it can operate in deep-sleep and standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management.

The window watchdog timer is based on a 7-bit down counter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

The SysTick timer is dedicated for OS, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Auto reload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

## 3.11. Real time clock (RTC) and backup registers

- Independent binary-coded decimal (BCD) format timer/counter with twenty 32-bit backup registers.
- Calendar with sub-second, seconds, minutes, hours, week day, date, year and month automatically correction
- Alarm function with wake up from deep-sleep and standby mode capability
- On-the-fly correction for synchronization with master clock. Digital calibration with 1 ppm resolution for compensation of quartz crystal inaccuracy.

The real time clock is an independent timer which provides a set of continuously running counters in backup registers to provide a real calendar function, and provides an alarm interrupt or an expected interrupt. It is not reset by a system or power reset, or when the device wakes up from standby mode. A prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 kHz from external crystal oscillator.



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## 3.12. Inter-integrated circuit (I2C)

- Up to three I2C bus interfaces can support both master and slave mode with a frequency up to 400 kHz (Fast mode)
- Provide arbitration function, optional PEC (packet error checking) generation and checking
- Supports 7-bit and 10-bit addressing mode and general call addressing mode

The I2C interface is an internal circuit allowing communication with an external I2C interface which is an industry standard two line serial interface used for connection to external hardware. These two serial lines are known as a serial data line (SDA) and a serial clock line (SCL). The I2C module provides transfer rate of up to 100 KHz in standard mode and up to 400 KHz in fast mode. The I2C module also has an arbitration detect function to prevent the situation where more than one master attempts to transmit data to the I2C bus at the same time. A CRC-8 calculator is also provided in I2C interface to perform packet error checking for I2C data.

## 3.13. Serial peripheral interface (SPI)

- Up to five SPI interfaces with a frequency of up to 30 MHz
- Support both master and slave mode
- Hardware CRC calculation and transmit automatic CRC error checking
- Quad wire configuration available in master mode (only in SPI5)

The SPI interface uses 4 pins, among which are the serial data input and output lines (MISO & MOSI), the clock line (SCK) and the slave select line (NSS). Both SPIs can be served by the DMA controller. The SPI interface may be used for a variety of purposes, including simplex synchronous transfers on two lines with a possible bidirectional data line or reliable communication using CRC checking. Quad-SPI master mode is also supported in SPI5 (SPI5 is not available in GD32F450Vx series).

## 3.14. Universal synchronous/asynchronous receiver transmitter (USART/UART)

- Up to four USARTs and four UARTs with operating frequency up to 12.5 MHz
- Supports both asynchronous and clocked synchronous serial communication modes
- IrDA SIR encoder and decoder support
- LIN break generation and detection
- ISO 7816-3 compliant smart card interface

The USART (USART0, USART1, USART2, USART5) and UART (UART3, UART4, UART6, UART7) are used to transfer data between parallel and serial interfaces, provides a flexible



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full duplex data exchange using synchronous or asynchronous transfer. It is also commonly used for RS-232 standard communication. The USART/UART includes a programmable baud rate generator which is capable of dividing the system clock to produce a dedicated clock for the USART/UART transmitter and receiver. The USART/UART also supports DMA function for high speed data communication.

## 3.15. Inter-IC sound (I2S)

- Two I2S bus Interfaces with sampling frequency from 8 kHz to 192 kHz, multiplexed with SPI1 and SPI2
- Support either master or slave mode Audio
- Sampling frequencies from 8 kHz up to 192 kHz are supported.

The Inter-IC sound (I2S) bus provides a standard communication interface for digital audio applications by 4-wire serial lines. GD32F450VGH6 contain an I2S-bus interface that can be operated with 16/32 bit resolution in master or slave mode, pin multiplexed with SPI1 and SPI2. The audio sampling frequencies from 8 kHz to 192 kHz is supported.

## 3.16. Universal serial bus full-speed interface (USBFS)

- One USB device/host/OTG full-speed Interface with frequency up to 12 Mbit/s
- Internal 48 MHz oscillator support crystal-less operation
- Internal main PLL for USB CLK compliantly
- Internal USBFS PHY support

The Universal Serial Bus (USB) is a 4-wire bus with 4 bidirectional endpoints. The device controller enables 12 Mbit/s data exchange with integusrated transceivers. Transaction formatting is performed by the hardware, including CRC generation and checking. It supports both host and device modes, as well as OTG mode with Host Negotiation Protocol (HNP) and Session Request Protocol (SRP). The controller contains a full-speed USB PHY internal. For full-speed or low-speed operation, no more external PHY chip is needed. It supports all the four types of transfer (control, bulk, Interrupt and isochronous) defined in USB 2.0 protocol. The required precise 48 MHz clock which can be generated from the internal main PLL (the clock source must use an HXTAL crystal oscillator) or by the internal 48 MHz oscillator in automatic trimming mode that allows crystal-less operation.

## 3.17. Universal serial bus high-speed interface (USBHS)

- One USB device/host/OTG high-speed Interface with frequency up to 480 Mbit/s
- An external PHY device connected to the ULPI is required when using in HS mode

USBHS supports both host and device modes, as well as OTG mode with Host Negotiation Protocol (HNP) and Session Request Protocol (SRP). The controller provides ULPI interface



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for external USB PHY integration and it also contains a full-speed USB PHY internal. For full-speed or low-speed operation, no more external PHY chip is needed. It supports all the four types of transfer (control, bulk, Interrupt and isochronous) defined in USB 2.0 protocol. HUB connection is supported when USB HS operates at high-speed in host mode. There is also a DMA engine operating as an AHB bus master in USBHS to speed up the data transfer between USBHS and system.

## 3.18. Controller area network (CAN)

- Two CAN2.0B interface with communication frequency up to 1 Mbit/s
- Internal main PLL for CAN CLK compliantly

Controller area network (CAN) is a method for enabling serial communication in field bus. The CAN protocol has been used extensively in industrial automation and automotive applications. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. Each CAN has three mailboxes for transmission and two FIFOs of three message deep for reception. It also provides 28 scalable/configurable identifier filter banks for selecting the incoming messages needed and discarding the others.

## 3.19. Ethernet MAC interface

- IEEE 802.3 compliant media access controller (MAC) for Ethernet LAN
- 10/100 Mbit/s rates with dedicated DMA controller and SRAM
- Support hardware precision time protocol (PTP) with conformity to IEEE 1588

The Ethernet media access controller (MAC) conforms to IEEE 802.3 specifications and fully supports IEEE 1588 standards. The embedded MAC provides the interface to the required external network physical interface (PHY) for LAN bus connection via an internal media independent interface (MII) or a reduced media independent interface (RMII). The number of MII signals provided up to 16 with 25 MHz output and RMII up to 7 with 50 MHz output. The function of 32-bit CRC checking is also available.

## 3.20. External memory controller (EXMC)

- Supported external memory: SRAM, PSRAM, ROM and NOR-Flash, NAND Flash and CF card, SDRAM with up to 32-bit data bus
- Provide ECC calculating hardware module for NAND Flash memory block
- Two SDRAM banks with independent configuration, up to 13-bits Row Address, 11-bits Column Address, 2-bits internal banks address
- SDRAM Memory size: 4x16Mx32bit (256 MB), 4x16Mx16bit (128 MB), 4x16Mx8bit (64 MB)

External memory controller (EXMC) is an abbreviation of external memory controller. It is



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divided in to several sub-banks for external device support, each sub-bank has its own chip selection signal but at one time, only one bank can be accessed. The EXMC supports code execution from external memory except NAND Flash and CF card. The EXMC also can be configured to interface with the most common LCD module of Motorola 6800 and Intel 8080 series and reduce the system cost and complexity.

The EXMC of GD32F450VGH6 in LQFP144 & BGA176 package also supports synchronous dynamic random access memory (SDRAM). It translates AHB transactions into the appropriate SDRAM protocol, and meanwhile, makes sure the access time requirements of the external SDRAM devices are satisfied.

## 3.21. Secure digital input and output card interface (SDIO)

- Support SD2.0/SDIO2.0/MMC4.2 host interface

The Secure Digital Input and Output Card Interface (SDIO) provides access to external SD memory cards specifications version 2.0, SDIO card specification version 2.0 and multi-media card system specification version 4.2 with DMA supported. In addition, this interface is also compliant with CE-ATA digital protocol rev1.1.

## 3.22. TFT LCD interface (TLI)

- 24-bit RGB Parallel Pixel Output; 8 bits-per-pixel (RGB888)
- Supports up to XVGA (1024x768) resolution
- 2 display layers with dedicated FIFO (64x32-bit)

The TFT LCD interface provides a parallel digital RGB (Red, Green and Blue) and signals for horizontal, vertical synchronization, Pixel Clock and Data Enable as output to interface directly to a variety of LCD (Liquid Crystal Display) and TFT (Thin Film Transistor) panels. A built-in DMA engine continuously move data from system memory to TLI and then, output to an external LCD display. Two separate layers are supported in TLI, as well as layer window and blending function.

## 3.23. Image processing accelerator (IPA)

- Copy one source image to the destination image
- Convert one source image to the destination image with specific pixel format
- Convert and blend two source images to the destination image with specific pixel format
- Fill up the destination image with a specific color

The Image processing accelerator (IPA) provides a configurable and flexible image format conversion from one or two source image to the destination image. Eleven pixel formats from 4-bit up to 32-bit per pixel independently for the two source images and five pixel formats from 16-bit up to 32-bit per pixel for the destination image are supported. Two 256*32 bits Look-



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Up Tables (LUT) separately for the two source images are implemented for the indirect pixel formats.

## 3.24. Digital camera interface (DCI)

- Digital video/picture capture
- 8/10/12/14 data width supported
- High transfer efficiency with DMA interface
- Video/picture crop supported
- Various pixel formats supported including JPEG/YCrCb/RGB
- Hard/embedded synchronous signals supported

DCI is an 8-bit to 14-bit parallel interface that able to capture video or picture from a camera via Digital Camera Interface. It supports 8/10/12/14 bits data width through DMA operation.

## 3.25. Debug mode

- Serial wire JTAG debug port (SWJ-DP)

The ARM® SWJ-DP Interface is embedded and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

## 3.26. Package and operation temperature

- BGA100 (GD32F450VGH6)
- Operation temperature range: -40°C to +85°C (industrial level)



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# 4. Electrical characteristics

## 4.1. Absolute maximum ratings

The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

**Table 4-1. Absolute maximum ratings**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{DD}$ | External voltage range | $V_{SS}$ - 0.3 | $V_{SS}$ + 3.6 | V |
| $V_{DDA}$ | External analog supply voltage | $V_{SSA}$ - 0.3 | $V_{SSA}$ + 3.6 | V |
| $V_{BAT}$ | External battery supply voltage | $V_{SS}$ - 0.3 | $V_{SS}$ + 3.6 | V |
| $V_{IN}$ | Input voltage on 5V tolerant pin | $V_{SS}$ - 0.3 | $V_{DD}$ + 4.0 | V |
| | Input voltage on other I/O | $V_{SS}$ - 0.3 | 4.0 | V |
| $I_{IO}$ | Maximum current for GPIO pins | — | 25 | mA |
| $T_A$ | Operating temperature range | -40 | +85 | °C |
| $T_{STG}$ | Storage temperature range | -55 | +150 | °C |
| $T_J$ | Maximum junction temperature | — | 125 | °C |

## 4.2. Recommended DC characteristics

**Table 4-2. DC operating conditions**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | — | 2.6 | 3.3 | 3.6 | V |
| $V_{DDA}$ | Analog supply voltage | Same as $V_{DD}$ | 2.6 | 3.3 | 3.6 | V |
| $V_{BAT}$ | Battery supply voltage | — | 1.8 | — | 3.6 | V |

## 4.3. Power consumption

The power measurements specified in the tables represent that code with data executing from on-chip Flash with the following specifications.

**Table 4-3. Power consumption characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{DD}$ | Supply current (Run mode) | $V_{DD}$=$V_{DDA}$=3.3V, HXTAL=25MHz, System clock=200MHz, All peripherals enabled | — | 99.2 | — | mA |
| | | $V_{DD}$=$V_{DDA}$=3.3V, HXTAL =25MHz, System clock =200MHz, All peripherals disabled | — | 60.1 | — | mA |
| | | $V_{DD}$=$V_{DDA}$=3.3V, HXTAL =25MHz, System | -— | 56.3 | — | mA |



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| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | | clock =108MHz, All peripherals enabled | | | | |
| | | $V_{DD}$=$V_{DDA}$=3.3V, HXTAL =25MHz, System Clock =108MHz, All peripherals disabled | — | 35.2 | — | mA |
| | Supply current (Sleep mode) | $V_{DD}$=$V_{DDA}$=3.3V, HXTAL =25MHz, CPU clock off, System clock=200MHz, All peripherals enabled | — | 67.9 | — | mA |
| | | $V_{DD}$=$V_{DDA}$=3.3V, HXTAL =25MHz, CPU clock off, System clock=200MHz, All peripherals disabled | — | 30 | — | mA |
| | Supply current (Deep-Sleep mode) | $V_{DD}$=$V_{DDA}$=3.3V, Regulator in run mode, IRC32K on, RTC on, All GPIOs analog mode | — | 1.57 | — | mA |
| | | $V_{DD}$=$V_{DDA}$=3.3V, Regulator in low power mode, IRC32K on, RTC on, All GPIOs analog mode | — | 1.55 | — | mA |
| | Supply current (Standby mode) | $V_{DD}$=$V_{DDA}$=3.3V, LXTAL off, IRC32K on, RTC on | — | 5.36 | — | µA |
| | | $V_{DD}$=$V_{DDA}$=3.3V, LXTAL off, IRC32K on, RTC off | — | 5.03 | — | µA |
| | | $V_{DD}$=$V_{DDA}$=3.3V, LXTAL off, IRC32K off, RTC off | — | 4.45 | — | µA |
| $I_{BAT}$ | Battery supply current | $V_{DD}$ not available, $V_{BAT}$=3.6 V, LXTAL on with external crystal, RTC on, Higher driving | — | 2.03 | — | µA |
| | | $V_{DD}$ not available, $V_{BAT}$=3.3 V, LXTAL on with external crystal, RTC on, Higher driving | — | 1.73 | — | µA |
| | | $V_{DD}$ not available, $V_{BAT}$=2.6 V, LXTAL on with external crystal, RTC on, Higher driving | — | 1.43 | — | µA |
| | | $V_{DD}$ not available, $V_{BAT}$=3.6 V, LXTAL on with external crystal, RTC on, Lower driving | — | 1.43 | — | µA |
| | | $V_{DD}$ not available, $V_{BAT}$=3.3 V, LXTAL on with external crystal, RTC on, Lower driving | — | 1.15 | — | µA |
| | | $V_{DD}$ not available, $V_{BAT}$=2.6 V, LXTAL on with external crystal, RTC on, Lower driving | — | 0.83 | — | µA |



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## 4.4. EMC characteristics

EMS (electromagnetic susceptibility) includes ESD (Electrostatic discharge, positive and negative) and FTB (Burst of Fast Transient voltage, positive and negative) testing result is given in ***Table 4-4. EMS characteristics***, based on the EMS levels and classes compliant with IEC 61000 series standard.

**Table 4-4. EMS characteristics**

| Symbol | Parameter | Conditions | Level/Class |
|---|---|---|---|
| $V_{ESD}$ | Voltage applied to all device pins to induce a functional disturbance | $V_{DD}$ = 3.3 V, $T_A$ = +25 °C conforms to IEC 61000-4-2 | 3B |
| $V_{FTB}$ | Fast transient voltage burst applied to induce a functional disturbance through 100 pF on $V_{DD}$ and $V_{SS}$ pins | $V_{DD}$ = 3.3 V, $T_A$ = +25 °C conforms to IEC 61000-4-4 | 4A |

EMI (Electromagnetic Interference) emission testing result is given in ***Table 4-5. EMI characteristics***, compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

**Table 4-5. EMI characteristics**

| Symbol | Parameter | Conditions | Tested frequency band | Conditions | | Unit |
|---|---|---|---|---|---|---|
| | | | | 24M | 48M | |
| $S_{EMI}$ | Peak level | $V_{DD}$ = 3.3 V, $T_A$ = +25 °C, compliant with IEC 61967-2 | 0.1 to 2 MHz | <0 | <0 | dBµV |
| | | | 2 to 30 MHz | -3.9 | -2.8 | |
| | | | 30 to 130 MHz | -7.2 | -8 | |
| | | | 130 MHz to 1GHz | -7 | -7 | |

## 4.5. Power supply supervisor characteristics

**Table 4-6. Power supply supervisor characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{POR}$ | Power on reset threshold | — | 2.30 | 2.40 | 2.48 | V |
| $V_{PDR}$ | Power down reset threshold | | 1.72 | 1.80 | 1.88 | V |
| $V_{HYST}$ | PDR hysteresis | | — | 0.6 | — | V |
| $T_{RSTTEMP}$ | Reset temporization | | — | 2 | — | ms |

## 4.6. Electrical sensitivity

The device is strained in order to determine its performance in terms of electrical sensitivity.



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Electrostatic discharges (ESD) are applied directly to the pins of the sample. Static latch-up (LU) test is based on the two measurement methods.

**Table 4-7. ESD characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{ESD(HBM)}$ | Electrostatic discharge voltage (human body model) | $T_A$=25 °C; JESD22-A114 | — | — | 7000 | V |
| $V_{ESD(CDM)}$ | Electrostatic discharge voltage (charge device model) | $T_A$=25 °C; JESD22-C101 | — | — | 800 | V |

**Table 4-8. Static latch-up characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| LU | I-test | $T_A$=25 °C; JESD78 | — | — | ±200 | mA |
| | $V_{supply}$ over voltage | | — | — | 5.4 | V |

## 4.7. External clock characteristics

**Table 4-9. High speed external clock (HXTAL) generated from a crystal/ceramic characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{HXTAL}$ | High Speed External oscillator (HXTAL) frequency | $V_{DD}$=5.0V | 4 | 8 | 32 | MHz |
| $C_{HXTAL}$ | Recommended load capacitance on OSCIN and OSCOUT | — | — | 20 | 30 | pF |
| $R_{FHXTAL}$ | Recommended external feedback resistor between OSCIN and OSCOUT | — | — | 400 | — | KΩ |
| $D_{HXTAL}$ | HXTAL oscillator duty cycle | — | 30 | 50 | 70 | % |
| $I_{DDHXTAL}$ | HXTAL oscillator operating current | $V_{DD}$=3.3V, $T_A$=25°C | — | 1 | — | mA |
| $t_{SUHXTAL}$ | HXTAL oscillator startup time | $V_{DD}$=3.3V, $T_A$=25°C | — | 2 | — | ms |

**Table 4-10. Low speed external clock (LXTAL) generated from a crystal/ceramic characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{LXTAL}$ | Low Speed External oscillator (LXTAL) frequency | $V_{DD}$=$V_{BAT}$=3.3V | — | 32.768 | — | KHz |
| $C_{LXTAL}$ | Recommended load capacitance on OSC32IN and OSC32OUT | — | — | — | 15 | pF |
| $D_{LXTAL}$ | LXTAL oscillator duty cycle | — | 30 | 50 | 70 | % |
| $I_{DDLXTAL}$ | LXTAL oscillator operating | Low Drive | — | 0.7 | — | µA |



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| | | | | | | |
|---|---|---|---|---|---|---|
| | current | High Drive | — | 1.3 | — | |
| $t_{SULXTAL}$ | LXTAL oscillator startup time | $V_{DD}$=$V_{BAT}$=3.3V | — | 2 | — | s |

## 4.8. Internal clock characteristics

**Table 4-11. High speed internal clock (IRC16M) characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{IRC16M}$ | High Speed Internal Oscillator (IRC16M) frequency | $V_{DD}$=3.3V | — | 16 | — | MHz |
| $ACC_{IRC16M}$ | IRC16M oscillator Frequency accuracy, Factory-trimmed | $V_{DD}$=3.3V, $T_A$=-40°C ~+105°C | -4.0 | — | +5.0 | % |
| | | $V_{DD}$=3.3V, $T_A$=0°C ~ +85°C | -2.0 | — | +2.0 | % |
| | | $V_{DD}$=3.3V, $T_A$=25°C | -1.0 | — | +1.0 | % |
| | IRC16M oscillator Frequency accuracy, User trimming step | — | — | 0.5 | — | % |
| $D_{IRC16M}$ | IRC16M oscillator duty cycle | $V_{DD}$=3.3V, $f_{IRC16M}$=16MHz | 45 | 50 | 55 | % |
| $I_{DDIRC16M}$ | IRC16M oscillator operating current | $V_{DD}$=3.3V, $f_{IRC16M}$=16MHz | — | 66 | 80 | μA |
| $t_{SUIRC16M}$ | IRC16M oscillator startup time | $V_{DD}$=3.3V, $f_{IRC16M}$=16MHz | — | 2.5 | 4 | us |

**Table 4-12. High speed internal clock (IRC48M) characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{IRC48M}$ | High Speed Internal Oscillator (IRC48M) frequency | $V_{DD}$=3.3V | — | 48 | — | MHz |
| $ACC_{IRC48M}$ | IRC48M oscillator Frequency accuracy, Factory-trimmed | $V_{DD}$=3.3V, $T_A$=-40°C ~+105°C | -4.0 | — | +5.0 | % |
| | | $V_{DD}$=3.3V, $T_A$=0°C ~ +85°C | -3.0 | — | +3.0 | % |
| | | $V_{DD}$=3.3V, $T_A$=25°C | -2.0 | — | +2.0 | % |
| | IRC48M oscillator Frequency accuracy, User trimming step | — | — | 0.12 | — | % |
| $D_{IRC48M}$ | IRC48M oscillator duty cycle | $V_{DD}$=3.3V, $f_{IRC48M}$=16MHz | 45 | 50 | 55 | % |
| $I_{DDIRC48M}$ | IRC48M oscillator operating current | $V_{DD}$=3.3V, $f_{IRC48M}$=16MHz | — | 240 | 300 | μA |
| $t_{SUIRC48M}$ | IRC48M oscillator startup time | $V_{DD}$=3.3V, $f_{IRC48M}$=16MHz | — | 2.5 | 4 | us |



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**Table 4-13. Low speed internal clock (IRC32K) characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{IRC32K}$ | Low Speed Internal oscillator (IRC32K) frequency | $V_{DD}$=$V_{BAT}$=3.3V, $T_A$=-40°C ~ +85°C | 20 | 32 | 45 | KHz |
| $I_{DDIRC32K}$ | IRC32K oscillator operating current | $V_{DD}$=$V_{BAT}$=3.3V, $T_A$=25°C | — | 0.4 | 0.6 | μA |
| $t_{SUIRC32K}$ | IRC32K oscillator startup time | $V_{DD}$=$V_{BAT}$=3.3V, $T_A$=25°C | — | 110 | 130 | μs |

## 4.9. PLL characteristics

**Table 4-14. PLL characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{PLLIN}$ | PLL input clock frequency | — | 1 | — | 4 | MHz |
| $f_{PLL}$ | PLL output clock frequency | — | 100 | — | 500 | MHz |
| $t_{LOCK}$ | PLL lock time | VCO freq=100MHz | — | 80 | 200 | μs |
| | | VCO freq=500MHz | — | 100 | 300 | |
| $I_{DD}$ | Current consumption on VDD | VCO freq=500MHz | — | 750 | — | μA |
| $I_{DDA}$ | Current consumption on VDDA | VCO freq=500MHz | — | 1100 | — | μA |
| $Jitter_{PLL}$ | Cycle to cycle Jitter | System clock 120MHz | — | 30 | — | ps |

**Table 4-15. PLL spread spectrum clock generation (SSCG) characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $F_{MOD}$ | Modulation frequency | — | — | — | 10 | KHz |
| Mdamp | Peak modulation amplitude | — | — | — | 2 | % |
| MODCNT* MODSTEP | — | — | — | — | $2^{15}$-1 | — |

***Equation 1***: SSCG configuration equation:

$$MODCNT = round(f_{PLLIN} / 4 / f_{mod})$$

$$MODSTEP = round\left(mdamp * PLLN * 2^{14} / \left(MODCNT * 100\right)\right)$$

The formula above (Equation 1) is SSCG configuration equation.

## 4.10. Memory characteristics

**Table 4-16. Flash memory characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $PE_{CYC}$ | Number of guaranteed program /erase cycles before failure (Endurance) | $T_A$=-40°C ~ +85°C | 100 | — | — | kcycles |



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| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{RET}$ | Data retention time | $T_A$=125°C | 20 | — | — | years |
| $t_{PROG}$ | Word programming time | $T_A$=-40°C ~ +85°C | 200 | — | 400 | us |
| $t_{ERASE}$ | Page erase time | $T_A$=-40°C ~ +85°C | 60 | 100 | 450 | ms |
| $t_{MERASE}$ | Mass erase time | $T_A$=-40°C ~ +85°C | 3.2 | — | 9.6 | s |

## 4.11. GPIO characteristics

**Table 4-17. I/O port characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Standard IO Low level input voltage | $V_{DD}$=2.6V | — | — | 1.27 | V |
| | | $V_{DD}$=3.3V | — | — | 1.58 | |
| | | $V_{DD}$=3.6V | — | — | 1.71 | |
| | High Voltage tolerant IO Low level input voltage | $V_{DD}$=2.6V | — | — | 1.27 | V |
| | | $V_{DD}$=3.3V | — | — | 1.58 | |
| | | $V_{DD}$=3.6V | — | — | 1.71 | |
| $V_{IH}$ | Standard IO High level input voltage | $V_{DD}$=2.6V | 1.40 | — | — | V |
| | | $V_{DD}$=3.3V | 1.71 | — | — | |
| | | $V_{DD}$=3.6V | 1.84 | — | — | |
| | High Voltage tolerant IO High level input voltage | $V_{DD}$=2.6V | 1.40 | — | — | V |
| | | $V_{DD}$=3.3V | 1.71 | — | — | |
| | | $V_{DD}$=3.6V | 1.84 | — | — | |
| $V_{OL}$ | Low level output voltage | $V_{DD}$=2.6V, $I_{IO}$=8mA | — | — | 0.17 | V |
| | | $V_{DD}$=3.3V, $I_{IO}$=8mA | — | — | 0.16 | |
| | | $V_{DD}$=3.6V, $I_{IO}$=8mA | — | — | 0.16 | |
| | | $V_{DD}$=2.6V, $I_{IO}$=20mA | — | — | 0.46 | |
| | | $V_{DD}$=3.3V, $I_{IO}$=20mA | — | — | 0.40 | |
| | | $V_{DD}$=3.6V, $I_{IO}$=20mA | — | — | 0.40 | |
| $V_{OH}$ | High level output voltage | $V_{DD}$=2.6V, $I_{IO}$=8mA | 2.39 | — | — | V |
| | | $V_{DD}$=3.3V, $I_{IO}$=8mA | 3.12 | — | — | |
| | | $V_{DD}$=3.6V, $I_{IO}$=8mA | 3.41 | — | — | |
| | | $V_{DD}$=2.6V, $I_{IO}$=20mA | 2.05 | — | — | |
| | | $V_{DD}$=3.3V, $I_{IO}$=20mA | 2.84 | — | — | |
| | | $V_{DD}$=3.6V, $I_{IO}$=20mA | 3.12 | — | — | |
| $R_{PU}$ | Internal pull-up resistor | $V_{IN}$=$V_{SS}$ | 30 | 40 | 50 | kΩ |
| $R_{PD}$ | Internal pull-down resistor | $V_{IN}$=$V_{DD}$ | 30 | 40 | 50 | kΩ |



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## 4.12. ADC characteristics

**Table 4-18. ADC characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DDA}$ | Operating voltage | — | 2.6 | 3.3 | 3.6 | V |
| $V_{IN}$ | ADC input voltage range | — | 0 | — | $V_{REF+}$ | V |
| $f_{ADC}$ | ADC clock | — | 0.1 | — | 40 | MHz |
| $f_S$ | Sampling rate | 12-bit | 0.007 | — | 2.6 | MSPS |
| | | 10-bit | 0.008 | — | 3.1 | |
| | | 8-bit | 0.01 | — | 3.6 | |
| | | 6-bit | 0.011 | — | 4.4 | |
| $V_{IN}$ | Analog input voltage | 16 external;3 internal | 0 | — | $V_{DDA}$ | V |
| $V_{REF+}$ | Positive Reference Voltage | — | — | $V_{DDA}$ | — | V |
| $V_{REF-}$ | Negative Reference Voltage | — | — | 0 | — | V |
| $R_{AIN}$ | External input impedance | See ***Equation 2*** | — | — | 52.1 | kΩ |
| $R_{ADC}$ | Input sampling switch resistance | — | — | — | 0.55 | kΩ |
| $C_{ADC}$ | Input sampling capacitance | No pin/pad capacitance included | — | — | 5.5 | pF |
| $t_{CAL}$ | Calibration time | $f_{ADC}$=40MHz | — | 3.275 | — | μs |
| $t_s$ | Sampling time | $f_{ADC}$=40MHz | 0.075 | — | 12 | μs |
| $t_{CONV}$ | Total conversion time (including sampling time) | 12-bit | — | 15 | — | 1/ $f_{ADC}$ |
| | | 10-bit | — | 13 | — | |
| | | 8-bit | — | 11 | — | |
| | | 6-bit | — | 9 | — | |
| $t_{SU}$ | Startup time | — | — | — | 1 | μs |

***Equation 2***: $R_{AIN}$ max formula $R_{AIN} < \frac{T_s}{f_{ADC} * C_{ADC} * \ln(2^{N+2})} - R_{ADC}$

The formula above (Equation 2) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N=12 (from 12-bit resolution).

**Table 4-19. ADC $R_{AIN}$ max for $f_{ADC}$=40MHz**

| $T_s$ (cycles) | $t_s$ (us) | $R_{AIN\ max}$ (KΩ) |
|---|---|---|
| 3 | 0.075 | 0.85 |
| 15 | 0.375 | 6.5 |
| 28 | 0.7 | 12.6 |
| 55 | 1.375 | 25.7 |
| 84 | 2.1 | 38.8 |
| 112 | 2.8 | 51.9 |
| 144 | 3.6 | N/A |
| 480 | 12 | N/A |

**Note:** Guaranteed by design, not tested in production.



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**Table 4-20. ADC dynamic accuracy at $f_{ADC}$ = 30 MHz**

| Symbol | Parameter | Test conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| ENOB | Effective number of bits | $f_{ADC}$=30MHz | 10.5 | 10.6 | — | bits |
| SNDR | Signal-to-noise and distortion ratio | $V_{DDA}$=$V_{REFP}$=2.6V | 65 | 65.6 | — | dB |
| SNR | Signal-to-noise ratio | Input | 65.5 | 66 | — | |
| THD | Total harmonic distortion | Frequency=110KHz Temperature=25℃ | -74 | -76 | — | |

**Table 4-21. ADC dynamic accuracy at $f_{ADC}$ = 30 MHz**

| Symbol | Parameter | Test conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| ENOB | Effective number of bits | $f_{ADC}$=30MHz | 10.7 | 10.8 | — | bits |
| SNDR | Signal-to-noise and distortion ratio | $V_{DDA}$=$V_{REFP}$=3.3V | 66.2 | 65.8 | — | dB |
| SNR | Signal-to-noise ratio | Input Frequency=110KHz | 66.8 | 67.4 | — | |
| THD | Total harmonic distortion | Temperature=25℃ | -71 | -75 | — | |

**Table 4-22. ADC dynamic accuracy at $f_{ADC}$ = 36 MHz**

| Symbol | Parameter | Test conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| ENOB | Effective number of bits | $f_{ADC}$=36MHz | 10.3 | 10.4 | — | bits |
| SNDR | Signal-to-noise and distortion ratio | $V_{DDA}$=$V_{REFP}$=3.3V | 63.8 | 64.4 | — | dB |
| SNR | Signal-to-noise ratio | Input Frequency=110KHz | 64.2 | 65 | — | |
| THD | Total harmonic distortion | Temperature=25℃ | -70 | -72 | — | |

**Table 4-23. ADC dynamic accuracy at $f_{ADC}$ = 40 MHz**

| Symbol | Parameter | Test conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| ENOB | Effective number of bits | $f_{ADC}$=40MHz | 9.9 | 10.0 | — | bits |
| SNDR | Signal-to-noise and distortion ratio | $V_{DDA}$=$V_{REFP}$=3.3V | 61.4 | 62 | — | dB |
| SNR | Signal-to-noise ratio | Input Frequency=110KHz | 62 | 62.4 | — | |
| THD | Total harmonic distortion | Temperature=25℃ | -68 | -70 | — | |

**Table 4-24. ADC static accuracy at $f_{ADC}$ = 15 MHz**

| Symbol | Parameter | Test conditions | Typ | Max | Unit |
|---|---|---|---|---|---|
| Offset | Offset error | $f_{ADC}$=15MHz $V_{DDA}$=$V_{REFP}$=3.3V | ±2 | ±3 | LSB |
| DNL | Differential linearity error | | ±0.9 | ±1.2 | |
| INL | Integral linearity error | | ±1.1 | ±1.5 | |

## 4.13. DAC characteristics

**Table 4-25. DAC characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DDA}$ | Operating voltage | — | 2.6 | 3.3 | 3.6 | V |
| $R_{LOAD}$ | Resistive load | Resistive load with buffer ON | 5 | — | — | kΩ |



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| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $R_O$ | Impedance output | Impedance output with buffer OFF | — | — | 15 | kΩ |
| $C_{LOAD}$ | Capacitive load | Capacitive load with buffer ON | — | — | 50 | pF |
| $DAC_OUT_{min}$ | Lower DAC_OUT voltage | Lower DAC_OUT voltage with buffer ON | 0.2 | — | — | V |
| | | Lower DAC_OUT voltage with buffer OFF | 0.5 | — | — | mV |
| $DAC_OUT_{max}$ | Higher DAC_OUT voltage | Higher DAC_OUT voltage with buffer ON | — | — | $V_{DDA}$-0.2 | V |
| | | Higher DAC_OUT voltage with buffer OFF | — | — | $V_{DDA}$-1LSB | V |
| $I_{DDA}$ | DC current consumption in quiescent mode with no load | Middle code on the input | — | — | 500 | μA |
| | | Worst code on the input | — | — | 560 | |
| DNL | Differential non linearity | 10-bit configuration | — | — | ±0.5 | LSB |
| | | 12-bit configuration | — | — | ±2 | |
| INL | Integral non linearity | 10-bit configuration | — | — | ±1 | LSB |
| | | 12-bit configuration | — | — | ±4 | |
| Gain error | Gain error | — | — | ±0.5 | — | % |
| $T_{SETTLING}$ | Settling time | $C_{LOAD}$≤50pF, $R_{LOAD}$≥5kΩ | — | 0.5 | 1 | μs |
| Update rate | Max frequency for a correct DAC_OUT change from code i to i±1LSB | $C_{LOAD}$≤50pF, $R_{LOAD}$≥5kΩ | — | — | 4 | MS/s |
| $T_{WAKEUP}$ | Wakeup time from off state | $C_{LOAD}$≤50pF, $R_{LOAD}$≥5kΩ | — | 1 | 2 | μs |
| PSRR | Power supply rejection ratio | No $R_{Load}$, $C_{LOAD}$=50pF | — | -90 | -75 | dB |

## 4.14. SPI characteristics

**Table 4-26. SPI characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{SCK}$ | SCK clock frequency | — | — | — | 30 | MHz |
| $TSI_{K(H)}$ | SCK clock high time | — | 19 | — | — | ns |
| $TSI_{K(L)}$ | SCK clock low time | — | 19 | — | — | ns |
| **SPI master mode** | | | | | | |
| $t_{V(MO)}$ | Data output valid time | — | — | — | 25 | ns |
| $t_{H(MO)}$ | Data output hold time | — | 2 | — | — | ns |
| $t_{SU(MI)}$ | Data input setup time | — | 5 | — | — | ns |
| $t_{H(MI)}$ | Data input hold time | — | 5 | — | — | ns |



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| SPI slave mode | | | | | | |
|---|---|---|---|---|---|---|
| $t_{SU(NSS)}$ | NSS enable setup time | $f_{PCLK}$=54MHz | 74 | — | — | ns |
| $t_{H(NSS)}$ | NSS enable hold time | $f_{PCLK}$=54MHz | 37 | — | — | ns |
| $t_{A(SO)}$ | Data output access time | $f_{PCLK}$=54MHz | 0 | — | 55 | ns |
| $t_{DIS(SO)}$ | Data output disable time | — | 3 | — | 10 | ns |
| $t_{V(SO)}$ | Data output valid time | — | — | — | 25 | ns |
| $t_{H(SO)}$ | Data output hold time | — | 15 | — | — | ns |
| $t_{SU(SI)}$ | Data input setup time | — | 5 | — | — | ns |
| $t_{H(SI)}$ | Data input hold time | — | 4 | — | — | ns |

## 4.15. I2C characteristics

**Table 4-27. I2C characteristics**

| Symbol | Parameter | Conditions | Standard mode | | Fast mode | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| $f_{SCL}$ | SCL clock frequency | — | 0 | 100 | 0 | 400 | KHz |
| $TSI_{L(H)}$ | SCL clock high time | — | 4.0 | — | 0.6 | — | ns |
| $TSI_{L(L)}$ | SCL clock low time | — | 4.7 | — | 1.3 | — | ns |

## 4.16. USART characteristics

**Table 4-28. USART characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{SCK}$ | SCK clock frequency | — | — | — | 36 | MHz |
| $TSI_{K(H)}$ | SCK clock high time | — | 13 | — | — | ns |
| $TSI_{K(L)}$ | SCK clock low time | — | 13 | — | — | ns |



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# 5. Package information

## 5.1. BGA package outline dimensions

**Figure 5-1. BGA package outline**

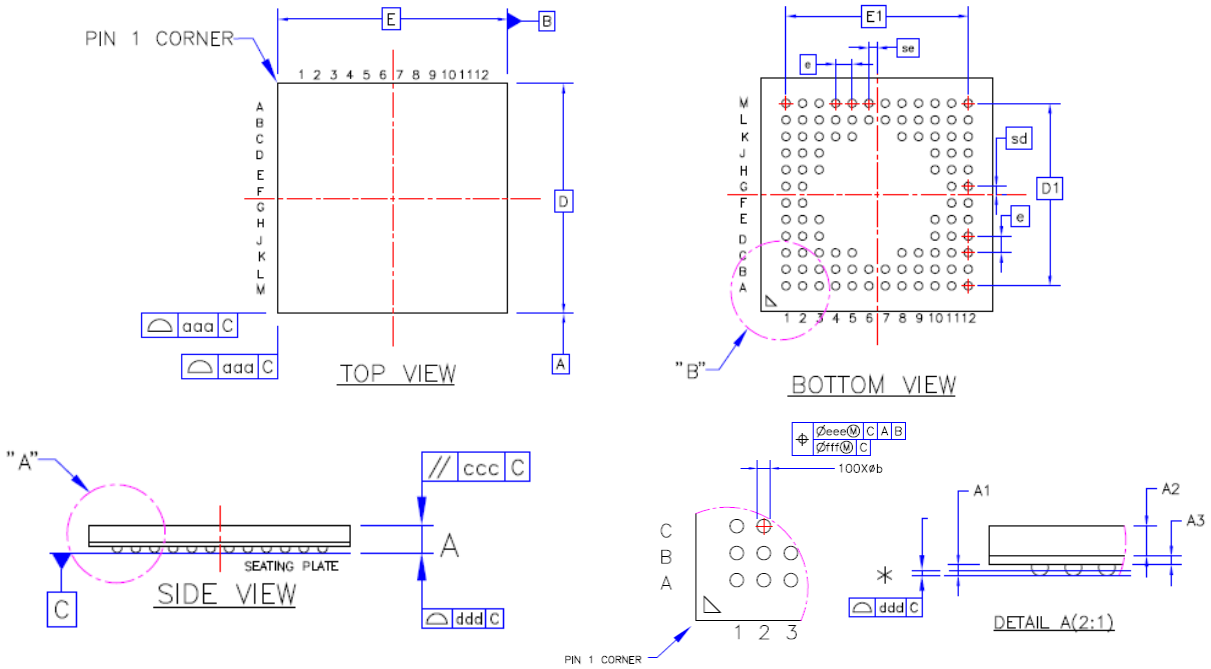



**Table 5-1. BGA package dimensions**

| Symbol | BGA100 | | |
|---|---|---|---|
| | Min | Typ | Max |
| A | - | 0.74 | 0.84 |
| A1 | 0.11 | 0.16 | 0.21 |
| A2 | - | 0.45 | - |
| A3 | 0.10 | 0.13 | 0.16 |
| D | 6.90 | 7.00 | 7.10 |
| E | 6.90 | 7.00 | 7.10 |
| e | - | 0.50 | - |
| b | 0.20 | 0.25 | 0.30 |
| D1 | - | 5.50 | - |
| E1 | - | 5.50 | - |
| aaa | 0.10 | | |
| bbb | - | | |
| ccc | 0.10 | | |
| ddd | 0.08 | | |
| eee | 0.15 | | |
| fff | 0.05 | | |



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(Original dimensions are in millimeters)



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# 6. Ordering information

**Table 6-1. Part ordering code for GD32F450VGH6 devices**

| Ordering code | Flash (KB) | Package | Package type | Temperature operating range |
|---|---|---|---|---|
| GD32F450VGH6 | 1024 | BGA100 | Green | Industrial<br>-40°C to +85°C |



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# 7. Revision history

**Table 7-1. Revision history**

| Revision No. | Description | Date |
|---|---|---|
| 1.0 | Initial Release | Oct. 25, 2016 |
| 1.1 | Pin alternate functions summary updated | Oct. 29, 2016 |
| 1.20 | Repair history accumulation error | Aug.20, 2019 |



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