# GigaDevice Semiconductor Inc.

# GD32F425xx
# Arm® Cortex®-M4 32-bit MCU

Datasheet

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# 1. General description

The GD32F425xx device belongs to the connectivity line of GD32 MCU family. It is a new 32-bit general-purpose microcontroller based on the Arm® Cortex®-M4 RISC core with best cost-performance ratio in terms of enhanced processing capacity, reduced power consumption and peripheral set. The Cortex®-M4 core features a Floating Point Unit (FPU) that accelerates single precision floating point math operations and supports all Arm® single precision instructions and data types. It implements a full set of DSP instructions to address digital signal control markets that demand an efficient, easy-to-use blend of control and signal processing capabilities. It also provides a Memory Protection Unit (MPU) and powerful trace technology for enhanced application security and advanced debug support.

The GD32F425xx device incorporates the Arm® Cortex®-M4 32-bit processor core operating at 200 MHz frequency with Flash accesses zero wait states to obtain maximum efficiency. It provides up to 3072 KB on-chip Flash memory and 256 KB SRAM memory. An extensive range of enhanced I/Os and peripherals connected to two APB buses. The devices offer up to three 12-bit 2.6 MSPS ADCs, two 12-bit DACs, up to eight general 16-bit timers, two 16-bit PWM advanced-control timers, two 32-bit general timers, and two 16-bit basic timers, as well as standard and advanced communication interfaces: up to three SPIs, three I2Cs, four USARTs and two UARTs, two I2Ss, two CANs, a SDIO, USBFS and USBHS. Additional peripherals as Digital camera interface (DCI) is included.

The device operates from a 2.6 to 3.6V power supply and available in –40 to +85 °C temperature range. Three power saving modes provide the flexibility for maximum optimization of power consumption, an especially important consideration in low power applications.

The above features make GD32F425xx devices suitable for a wide range of interconnection and advanced applications, especially in areas such as industrial control, consumer and handheld equipment, embedded modules, human machine interface, security and alarm systems, graphic display, automotive navigation, drone, IoT and so on.






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# 2. Device overview

## 2.1. Device information

**Table 2-1. GD32F425xx devices features and peripheral list**

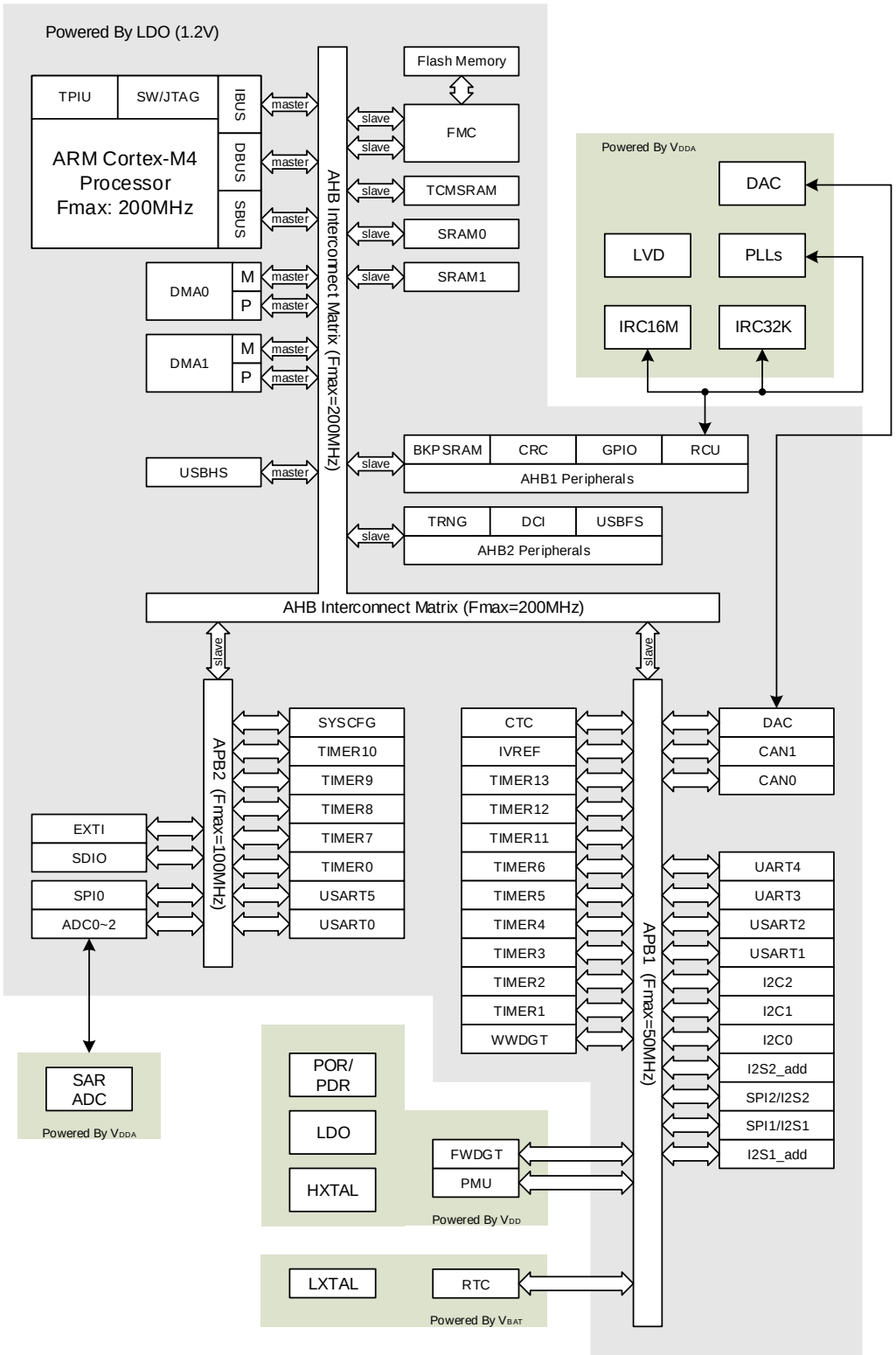
| Part Number | | GD32F425xx | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | RE | RG | RK | VG | VK | VG | VK | ZG | ZK |
| Flash | Code area (KB) | 512 | 512 | 512 | 512 | 512 | 512 | 512 | 512 | 512 |
| | Data area (KB) | 0 | 512 | 2560 | 512 | 2560 | 512 | 2560 | 512 | 2560 |
| | Total (KB) | 512 | 1024 | 3072 | 1024 | 3072 | 1024 | 3072 | 1024 | 3072 |
| SRAM (KB) | | 256 | 256 | 256 | 256 | 256 | 256 | 256 | 256 | 256 |
| Timers | General timer(16-bit) | 8 (2-3,8-13) | 8 (2-3,8-13) | 8 (2-3,8-13) | 8 (2-3,8-13) | 8 (2-3,8-13) | 8 (2-3,8-13) | 8 (2-3,8-13) | 8 (2-3,8-13) | 8 (2-3,8-13) |
| | General timer (32-bit) | 2 (1,4) | 2 (1,4) | 2 (1,4) | 2 (1,4) | 2 (1,4) | 2 (1,4) | 2 (1,4) | 2 (1,4) | 2 (1,4) |
| | Advanced timer(16-bit) | 2 (0,7) | 2 (0,7) | 2 (0,7) | 2 (0,7) | 2 (0,7) | 2 (0,7) | 2 (0,7) | 2 (0,7) | 2 (0,7) |
| | Basic timer(16-bit) | 2 (5,6) | 2 (5,6) | 2 (5,6) | 2 (5,6) | 2 (5,6) | 2 (5,6) | 2 (5,6) | 2 (5,6) | 2 (5,6) |
| | SysTick | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | Watchdog | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| | RTC | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Connectivity | USART | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 |
| | UART | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| | I2C | 3 | 3 | 3 | 3 | 3 | 3 | 3 | 3 | 3 |
| | SPI/I2S | 3/2 (0-2)/(1-2) | 3/2 (0-2)/(1-2) | 3/2 (0-2)/(1-2) | 3/2 (0-2)/(1-2) | 3/2 (0-2)/(1-2) | 3/2 (0-2)/(1-2) | 3/2 (0-2)/(1-2) | 3/2 (0-2)/(1-2) | 3/2 (0-2)/(1-2) |
| | SDIO | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | CAN | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| | USB | FS+HS | FS+HS | FS+HS | FS+HS | FS+HS | FS+HS | FS+HS | FS+HS | FS+HS |
| | DCI | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| GPIO | | 51 | 51 | 51 | 82 | 82 | 82 | 82 | 114 | 114 |
| ADC(CHs) | | 3(16) | 3(16) | 3(16) | 3(16) | 3(16) | 3(16) | 3(16) | 3(24) | 3(24) |
| DAC | | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| Package | | LQFP64 | | | LQFP100 | | BGA100 | | LQFP144 | |



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## 2.2. Block diagram

**Figure 2-1. GD32F425xx block diagram**

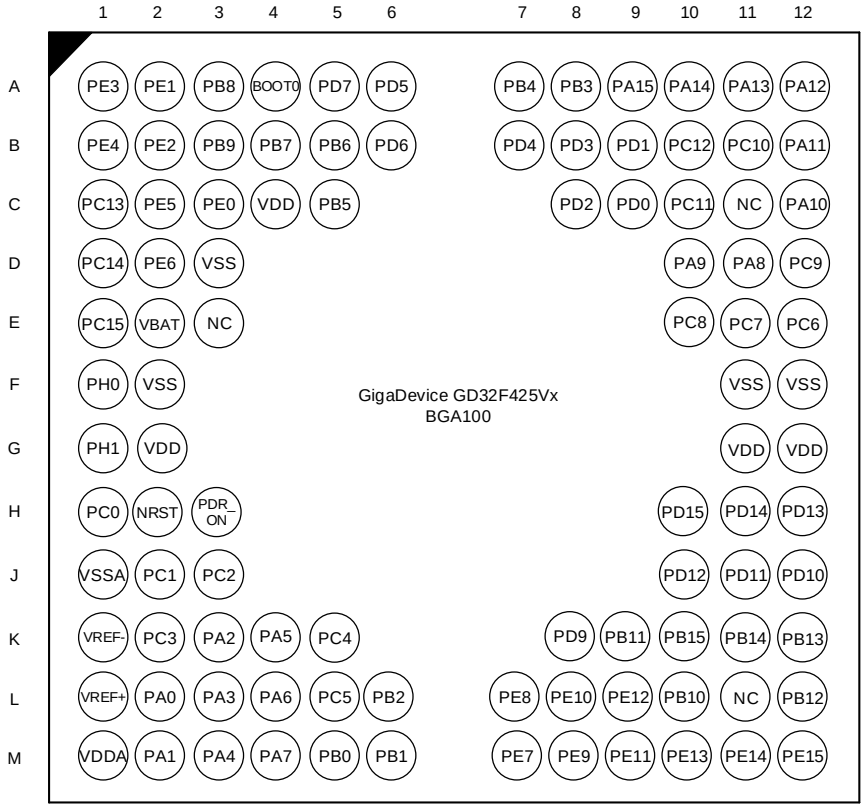





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## 2.3. Pinouts and pin assignment

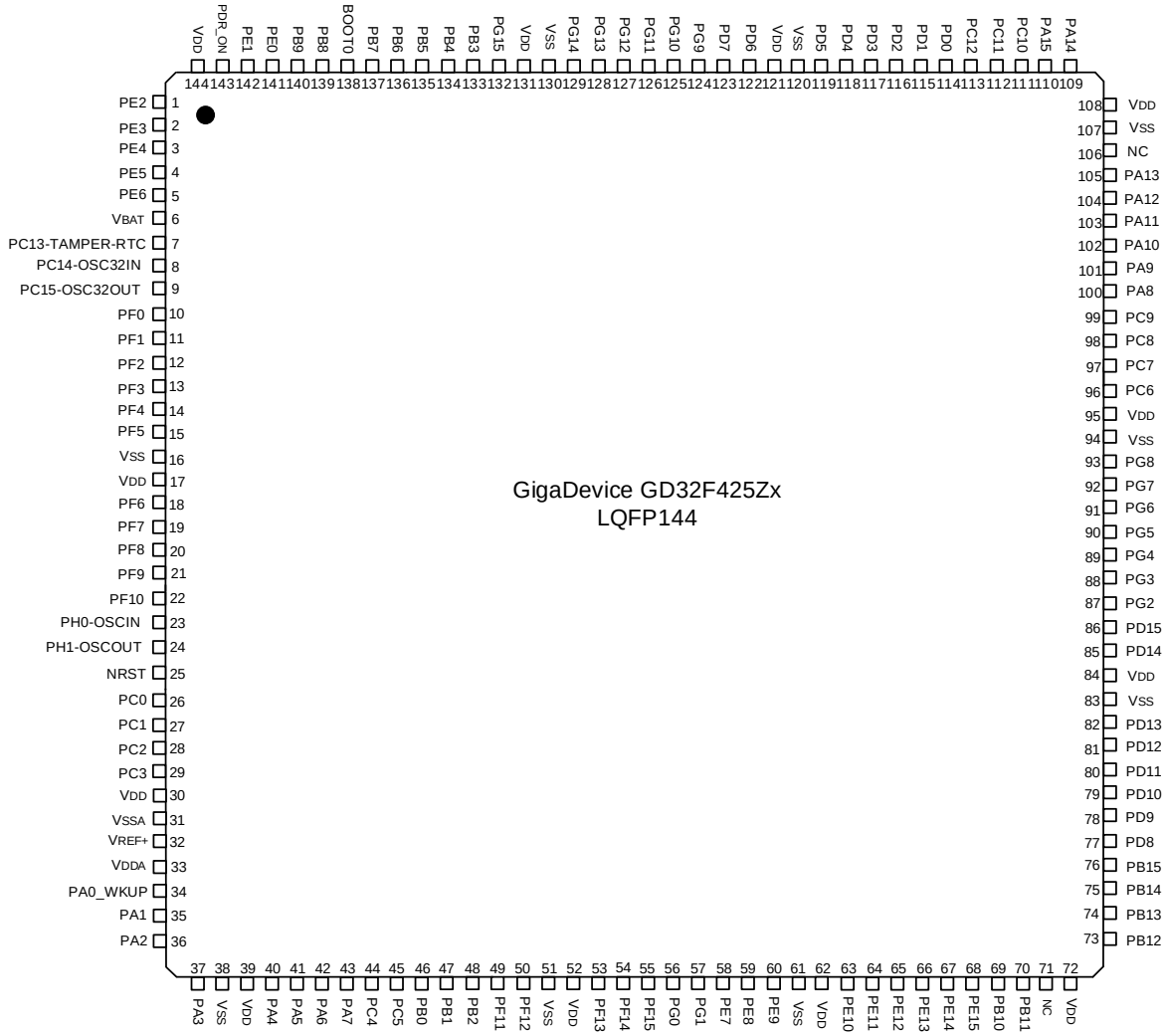
**Figure 2-2. GD32F425Vx BGA100 pinouts**






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**Figure 2-3. GD32F425Zx LQFP144 pinouts**






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**Figure 2-4. GD32F425Vx LQFP100 pinouts**

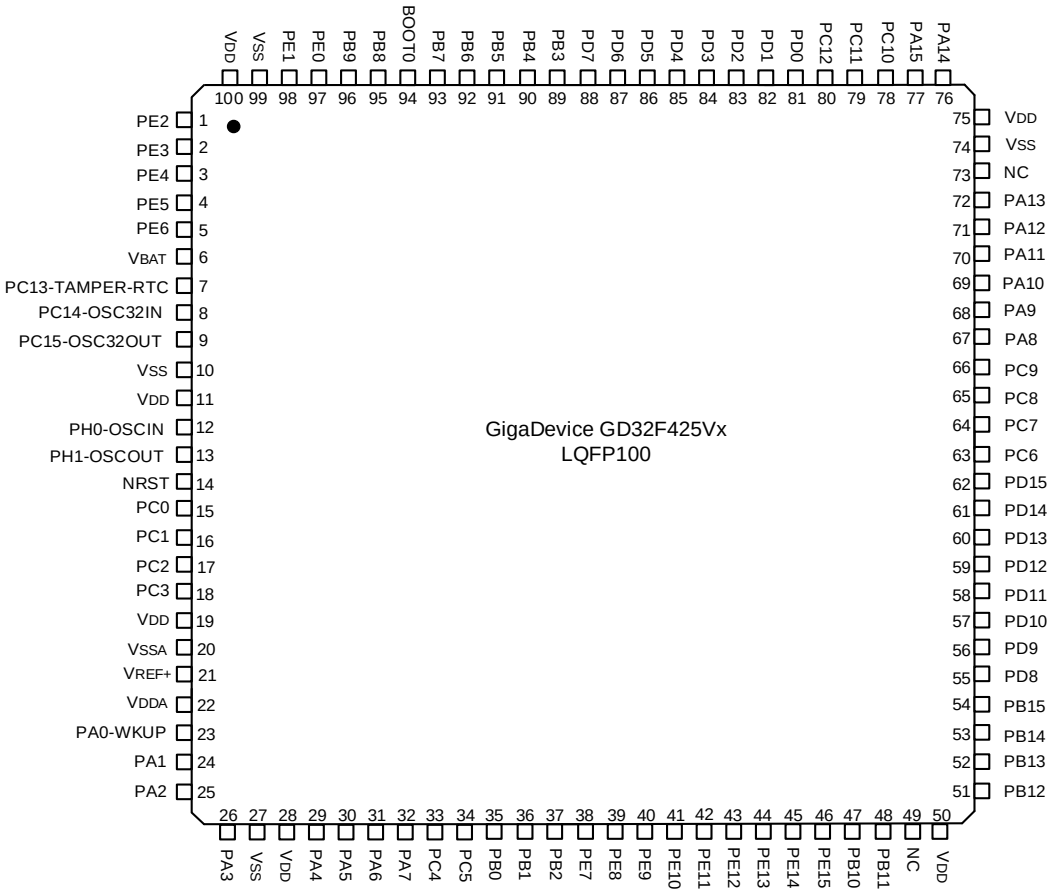
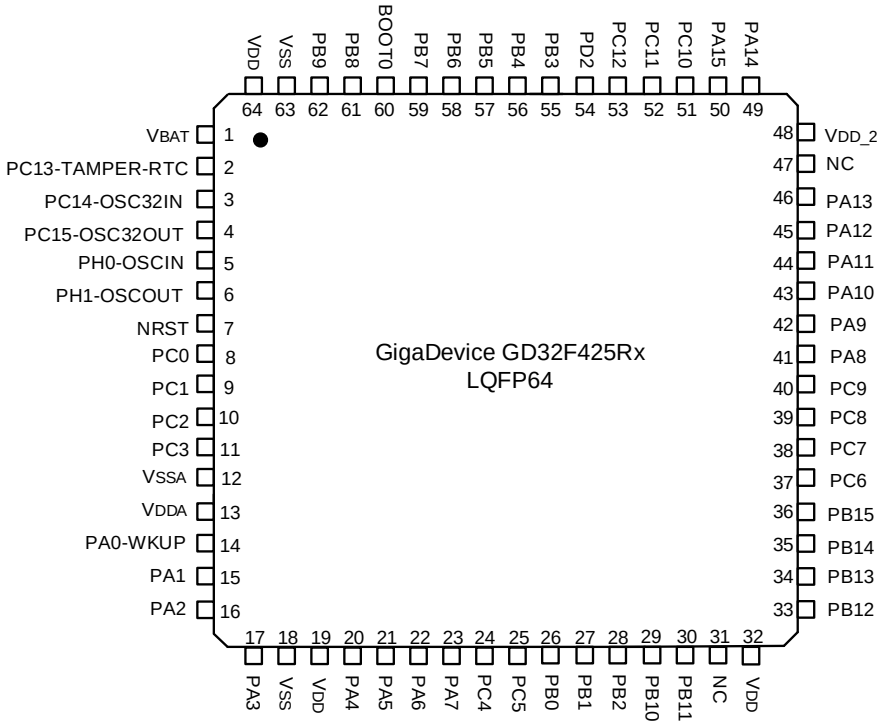



**Figure 2-5. GD32F425Rx LQFP64 pinouts**






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## 2.4. Memory map

**Table 2-2. GD32F425xx memory map**

| Pre-defined Regions | Bus | Address | Peripherals |
|---|---|---|---|
| External Device | AHB | 0xC000 0000 - 0xDFFF FFFF | Reserved |
| | | 0xA000 1000 - 0xBFFF FFFF | Reserved |
| | | 0xA000 0000 - 0xA000 0FFF | Reserved |
| External RAM | | 0x9000 0000 - 0x9FFF FFFF | Reserved |
| | | 0x7000 0000 - 0x8FFF FFFF | Reserved |
| | | 0x6000 0000 - 0x6FFF FFFF | Reserved |
| Peripheral | AHB2 | 0x5006 0C00 - 0x5FFF FFFF | Reserved |
| | | 0x5006 0800 - 0x5006 0BFF | TRNG |
| | | 0x5005 0400 - 0x5006 07FF | Reserved |
| | | 0x5005 0000 - 0x5005 03FF | DCI |
| | | 0x5004 0000 - 0x5004 FFFF | Reserved |
| | | 0x5000 0000 - 0x5003 FFFF | USBFS |
| | AHB1 | 0x4008 0000 - 0x4FFF FFFF | Reserved |
| | | 0x4004 0000 - 0x4007 FFFF | USBHS |
| | | 0x4002 BC00 - 0x4003 FFFF | Reserved |
| | | 0x4002 B000 - 0x4002 BBFF | Reserved |
| | | 0x4002 A000 - 0x4002 AFFF | Reserved |
| | | 0x4002 8000 - 0x4002 9FFF | Reserved |
| | | 0x4002 6800 - 0x4002 7FFF | Reserved |
| | | 0x4002 6400 - 0x4002 67FF | DMA1 |
| | | 0x4002 6000 - 0x4002 63FF | DMA0 |
| | | 0x4002 5000 - 0x4002 5FFF | Reserved |
| | | 0x4002 4000 - 0x4002 4FFF | BKP SRAM |
| | | 0x4002 3C00 - 0x4002 3FFF | FMC |
| | | 0x4002 3800 - 0x4002 3BFF | RCU |
| | | 0x4002 3400 - 0x4002 37FF | Reserved |
| | | 0x4002 3000 - 0x4002 33FF | CRC |
| | | 0x4002 2400 - 0x4002 2FFF | Reserved |
| | | 0x4002 2000 - 0x4002 23FF | GPIOI |
| | | 0x4002 1C00 - 0x4002 1FFF | GPIOH |
| | | 0x4002 1800 - 0x4002 1BFF | GPIOG |
| | | 0x4002 1400 - 0x4002 17FF | GPIOF |
| | | 0x4002 1000 - 0x4002 13FF | GPIOE |
| | | 0x4002 0C00 - 0x4002 0FFF | GPIOD |
| | | 0x4002 0800 - 0x4002 0BFF | GPIOC |
| | | 0x4002 0400 - 0x4002 07FF | GPIOB |
| | | 0x4002 0000 - 0x4002 03FF | GPIOA |



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| Pre-defined Regions | Bus | Address | Peripherals |
|---|---|---|---|
| | APB2 | 0x4001 6C00 - 0x4001 FFFF | Reserved |
| | | 0x4001 6800 - 0x4001 6BFF | Reserved |
| | | 0x4001 5800 - 0x4001 67FF | Reserved |
| | | 0x4001 5400 - 0x4001 57FF | Reserved |
| | | 0x4001 5000 - 0x4001 53FF | Reserved |
| | | 0x4001 4C00 - 0x4001 4FFF | Reserved |
| | | 0x4001 4800 - 0x4001 4BFF | TIMER10 |
| | | 0x4001 4400 - 0x4001 47FF | TIMER9 |
| | | 0x4001 4000 - 0x4001 43FF | TIMER8 |
| | | 0x4001 3C00 - 0x4001 3FFF | EXTI |
| | | 0x4001 3800 - 0x4001 3BFF | SYSCFG |
| | | 0x4001 3400 - 0x4001 37FF | Reserved |
| | | 0x4001 3000 - 0x4001 33FF | SPI0 |
| | | 0x4001 2C00 - 0x4001 2FFF | SDIO |
| | | 0x4001 2400 - 0x4001 2BFF | Reserved |
| | | 0x4001 2300 - 0x4001 23FF | ADC0(1) |
| | | 0x4001 2200 - 0x4001 22FF | ADC2 |
| | | 0x4001 2100 - 0x4001 21FF | ADC1 |
| | | 0x4001 2000 - 0x4001 20FF | ADC0 |
| | | 0x4001 1800 - 0x4001 1FFF | Reserved |
| | | 0x4001 1400 - 0x4001 17FF | USART5 |
| | | 0x4001 1000 - 0x4001 13FF | USART0 |
| | | 0x4001 0800 - 0x4001 0FFF | Reserved |
| | | 0x4001 0400 - 0x4001 07FF | TIMER7 |
| | | 0x4001 0000 - 0x4001 03FF | TIMER0 |
| | APB1 | 0x4000 C800 - 0x4000 FFFF | Reserved |
| | | 0x4000 C400 - 0x4000 C7FF | IREF |
| | | 0x4000 8000 - 0x4000 C3FF | Reserved |
| | | 0x4000 7C00 - 0x4000 7FFF | Reserved |
| | | 0x4000 7800 - 0x4000 7BFF | Reserved |
| | | 0x4000 7400 - 0x4000 77FF | DAC |
| | | 0x4000 7000 - 0x4000 73FF | PMU |
| | | 0x4000 6C00 - 0x4000 6FFF | CTC |
| | | 0x4000 6800 - 0x4000 6BFF | CAN1 |
| | | 0x4000 6400 - 0x4000 67FF | CAN0 |
| | | 0x4000 6000 - 0x4000 63FF | Reserved |
| | | 0x4000 5C00 - 0x4000 5FFF | I2C2 |
| | | 0x4000 5800 - 0x4000 5BFF | I2C1 |
| | | 0x4000 5400 - 0x4000 57FF | I2C0 |
| | | 0x4000 5000 - 0x4000 53FF | UART4 |
| | | 0x4000 4C00 - 0x4000 4FFF | UART3 |



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| Pre-defined Regions | Bus | Address | Peripherals |
|---|---|---|---|
| | | 0x4000 4800 - 0x4000 4BFF | USART2 |
| | | 0x4000 4400 - 0x4000 47FF | USART1 |
| | | 0x4000 4000 - 0x4000 43FF | I2S2_add |
| | | 0x4000 3C00 - 0x4000 3FFF | SPI2/I2S2 |
| | | 0x4000 3800 - 0x4000 3BFF | SPI1/I2S1 |
| | | 0x4000 3400 - 0x4000 37FF | I2S1_add |
| | | 0x4000 3000 - 0x4000 33FF | FWDGT |
| | | 0x4000 2C00 - 0x4000 2FFF | WWDGT |
| | | 0x4000 2800 - 0x4000 2BFF | RTC |
| | | 0x4000 2400 - 0x4000 27FF | Reserved |
| | | 0x4000 2000 - 0x4000 23FF | TIMER13 |
| | | 0x4000 1C00 - 0x4000 1FFF | TIMER12 |
| | | 0x4000 1800 - 0x4000 1BFF | TIMER11 |
| | | 0x4000 1400 - 0x4000 17FF | TIMER6 |
| | | 0x4000 1000 - 0x4000 13FF | TIMER5 |
| | | 0x4000 0C00 - 0x4000 0FFF | TIMER4 |
| | | 0x4000 0800 - 0x4000 0BFF | TIMER3 |
| | | 0x4000 0400 - 0x4000 07FF | TIMER2 |
| | | 0x4000 0000 - 0x4000 03FF | TIMER1 |
| SRAM | AHB | 0x2007 0000 - 0x3FFF FFFF | Reserved |
| | | 0x2003 0000 - 0x2006 FFFF | Reserved |
| | | 0x2002 0000 - 0x2002 FFFF | SRAM2(64KB) |
| | | 0x2001 C000 - 0x2001 FFFF | SRAM1(16KB) |
| | | 0x2000 0000 - 0x2001 BFFF | SRAM0(112KB) |
| Code | AHB | 0x1FFF C010 - 0x1FFF FFFF | Reserved |
| | | 0x1FFF C000 - 0x1FFF C00F | Option bytes(Bank 0) |
| | | 0x1FFF 7A10 - 0x1FFF BFFF | Reserved |
| | | 0x1FFF 7800 - 0x1FFF 7A0F | OTP(512B) |
| | | 0x1FFF 0000 - 0x1FFF 77FF | Boot loader(30KB) |
| | | 0x1FFE C010 - 0x1FFE FFFF | Reserved |
| | | 0x1FFE C000 - 0x1FFE C00F | Option bytes(Bank 1) |
| | | 0x1001 0000 - 0x1FFE BFFF | Reserved |
| | | 0x1000 0000 - 0x1000 FFFF | TCMSRAM(64KB) |
| | | 0x0830 0000 - 0x0FFF FFFF | Reserved |
| | | 0x0800 0000 - 0x082F FFFF | Main Flash(3072KB) |
| | | 0x0000 0000 - 0x07FF FFFF | Aliased to the boot device |

**Note:**

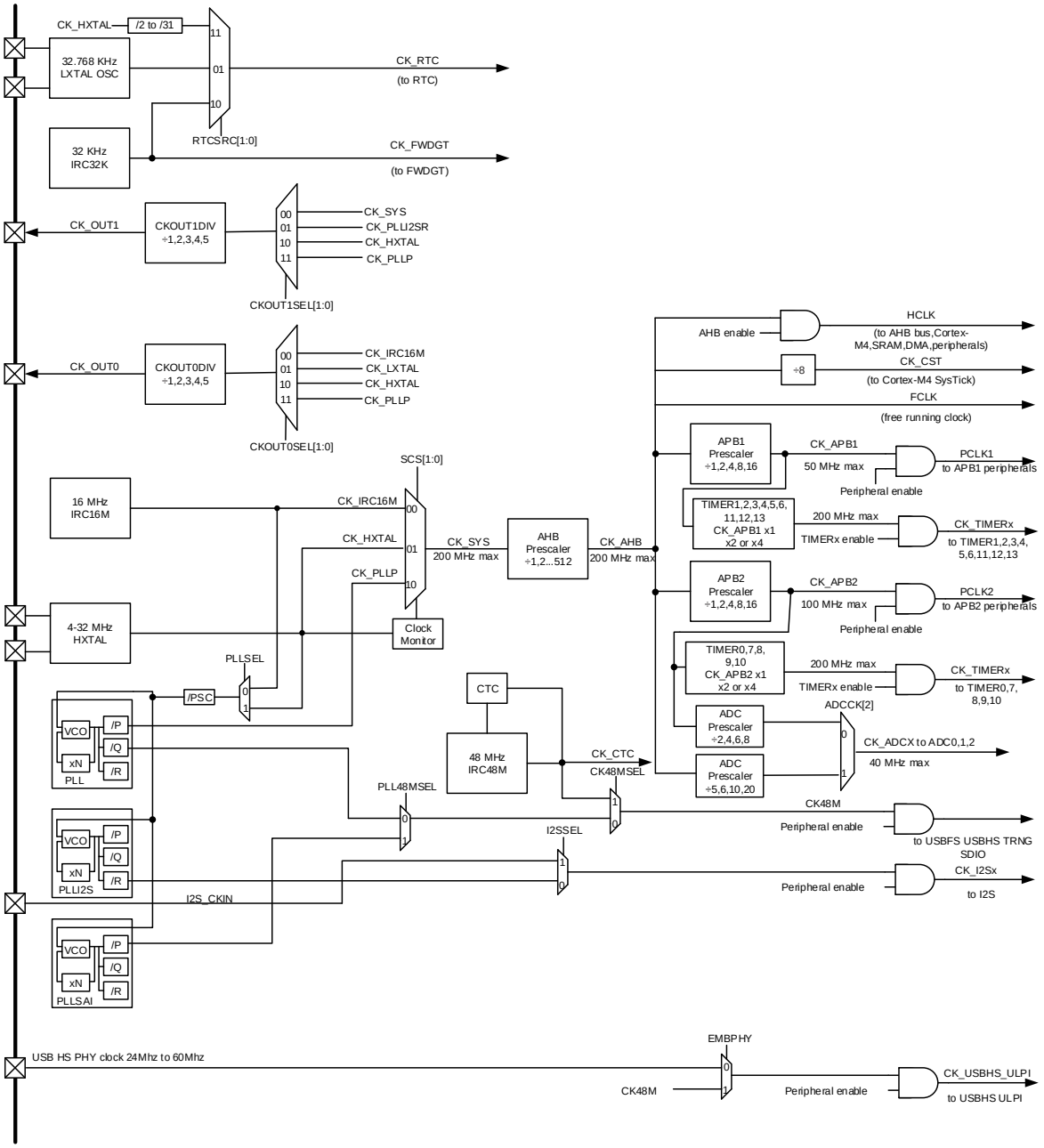
(1) ADC_SSTAT, ADC_SYNCCTL, ADC_SYNCDATA based on base address of ADC0.



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## 2.5. Clock tree

**Figure 2-6. GD32F425xx clock tree**




**Legend:**

HXTAL: High speed crystal oscillator

LXTAL: Low speed crystal oscillator

IRC16M: Internal 16M RC oscillators

IRC32K: Internal 32K RC oscillator

IRC48M: Internal 48M RC oscillators



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## 2.6. Pin definitions

### 2.6.1. GD32F425Zx LQFP144 pin definitions

**Table 2-3. GD32F425Zx LQFP144 pin definitions**

| Pin Name | Pins | Pin Type(1) | I/O Level(2) | Functions description |
|---|---|---|---|---|
| PE2 | 1 | I/O | 5VT | Default: PE2<br>Alternate: TRACECK, EVENTOUT |
| PE3 | 2 | I/O | 5VT | Default: PE3<br>Alternate:TRACED0, EVENTOUT |
| PE4 | 3 | I/O | 5VT | Default: PE4<br>Alternate:TRACED1, DCI_D4, EVENTOUT |
| PE5 | 4 | I/O | 5VT | Default: PE5<br>Alternate:TRACED2,TIMER8_CH0, DCI_D6, EVENTOUT |
| PE6 | 5 | I/O | 5VT | Default: PE6<br>Alternate:TRACED3,TIMER8_CH1, DCI_D7, EVENTOUT |
| $V_{BAT}$ | 6 | P | - | Default: $V_{BAT}$ |
| PC13-TAMPER-RTC | 7 | I/O | 5VT | Default: PC13<br>Alternate: EVENTOUT<br>Additional: RTC_TAMP0, RTC_OUT, RTC_TS |
| PC14-OSC32IN | 8 | I/O | 5VT | Default: PC14<br>Alternate: EVENTOUT<br>Additional: OSC32IN |
| PC15-OSC32OUT | 9 | I/O | 5VT | Default: PC15<br>Alternate: EVENTOUT<br>Additional: OSC32OUT |
| PF0 | 10 | I/O | 5VT | Default: PF0<br>Alternate:I2C1_SDA, EVENTOUT, CTC_SYNC |
| PF1 | 11 | I/O | 5VT | Default: PF1<br>Alternate: I2C1_SCL, EVENTOUT |
| PF2 | 12 | I/O | 5VT | Default: PF2<br>Alternate: I2C1_SMBA, EVENTOUT |
| PF3 | 13 | I/O | 5VT | Default: PF3<br>Alternate: EVENTOUT, I2C1_TXFRAME<br>Additional: ADC2_IN9 |
| PF4 | 14 | I/O | 5VT | Default: PF4<br>Alternate: EVENTOUT<br>Additional: ADC2_IN14 |
| PF5 | 15 | I/O | 5VT | Default: PF5<br>Alternate: EVENTOUT<br>Additional: ADC2_IN15 |
| $V_{SS}$ | 16 | P | - | Default: $V_{SS}$ |



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| Pin Name | Pins | Pin Type(1) | I/O Level(2) | Functions description |
|---|---|---|---|---|
| $V_{DD}$ | 17 | P | - | Default: $V_{DD}$ |
| PF6 | 18 | I/O | 5VT | Default: PF6<br>Alternate: TIMER9_CH0, EVENTOUT<br>Additional: ADC2_IN4 |
| PF7 | 19 | I/O | 5VT | Default: PF7<br>Alternate: TIMER10_CH0, EVENTOUT<br>Additional: ADC2_IN5 |
| PF8 | 20 | I/O | 5VT | Default: PF8<br>Alternate: TIMER12_CH0, EVENTOUT<br>Additional: ADC2_IN6 |
| PF9 | 21 | I/O | 5VT | Default: PF9<br>Alternate: TIMER13_CH0, EVENTOUT<br>Additional: ADC2_IN7 |
| PF10 | 22 | I/O | 5VT | Default: PF10<br>Alternate: DCI_D11, EVENTOUT<br>Additional: ADC2_IN8 |
| PH0 | 23 | I/O | 5VT | Default: PH0, OSCIN<br>Alternate: EVENTOUT<br>Additional: OSCIN |
| PH1 | 24 | I/O | 5VT | Default: PH1, OSCOUT<br>Alternate: EVENTOUT<br>Additional: OSCOUT |
| NRST | 25 | - | - | Default: NRST |
| PC0 | 26 | I/O | 5VT | Default: PC0<br>Alternate: USBHS_ULPI_STP, EVENTOUT<br>Additional: ADC012_IN10 |
| PC1 | 27 | I/O | 5VT | Default: PC1<br>Alternate: SPI2_MOSI, I2S2_SD, SPI1_MOSI, I2S1_SD, EVENTOUT<br>Additional: ADC012_IN11 |
| PC2 | 28 | I/O | 5VT | Default: PC2<br>Alternate: SPI1_MISO,I2S1_ADD_SD,USBHS_ULPI_DIR, EVENTOUT<br>Additional: ADC012_IN12 |
| PC3 | 29 | I/O | 5VT | Default: PC3<br>Alternate: SPI1_MOSI,I2S1_SD,USBHS_ULPI_NXT, EVENTOUT<br>Additional: ADC012_IN13 |
| $V_{DD}$ | 30 | P | - | Default: $V_{DD}$ |
| $V_{SSA}$ | 31 | P | - | Default: $V_{SSA}$ |
| $V_{REFP}$ | 32 | P | - | Default: $V_{REF+}$ |
| $V_{DDA}$ | 33 | P | - | Default: $V_{DDA}$ |



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| Pin Name | Pins | Pin Type(1) | I/O Level(2) | Functions description |
|---|---|---|---|---|
| PA0-WKUP | 34 | I/O | 5VT | Default: PA0<br>Alternate: TIMER1_CH0,TIMER1_ETI,TIMER4_CH0, TIMER7_ETI,USART1_CTS, UART3_TX, EVENTOUT<br>Additional: ADC012_IN0, WKUP |
| PA1 | 35 | I/O | 5VT | Default: PA1<br>Alternate: TIMER1_CH1, TIMER4_CH1, USART1_RTS, UART3_RX, EVENTOUT<br>Additional: ADC012_IN1 |
| PA2 | 36 | I/O | 5VT | Default: PA2<br>Alternate: TIMER1_CH2,TIMER4_CH2,TIMER8_CH0, I2S_CKIN, USART1_TX, EVENTOUT<br>Additional: ADC012_IN2 |
| PA3 | 37 | I/O | 5VT | Default: PA3<br>Alternate: TIMER1_CH3,TIMER4_CH3,TIMER8_CH1, I2S1_MCK,USART1_RX,USBHS_ULPI_D0, EVENTOUT<br>Additional: ADC012_IN3 |
| $V_{SS}$ | 38 | P | - | Default: $V_{SS}$ |
| $V_{DD}$ | 39 | P | - | Default: $V_{DD}$ |
| PA4 | 40 | I/O | | Default: PA4<br>Alternate: SPI0_NSS,SPI2_NSS, I2S2_WS, USART1_CK, USBHS_SOF, DCI_HSYNC, EVENTOUT<br>Additional: ADC01_IN4, DAC_OUT0 |
| PA5 | 41 | I/O | | Default: PA5<br>Alternate: TIMER1_CH0,TIMER1_ETI, TIMER7_CH0_ON, SPI0_SCK, USBHS_ULPI_CK, EVENTOUT<br>Additional: ADC01_IN5, DAC_OUT1 |
| PA6 | 42 | I/O | 5VT | Default: PA6<br>Alternate: TIMER0_BRKIN, TIMER2_CH0, TIMER7_BRKIN, SPI0_MISO, I2S1_MCK, TIMER12_CH0, SDIO_CMD, DCI_PIXCLK, EVENTOUT<br>Additional: ADC01_IN6 |
| PA7 | 43 | I/O | 5VT | Default: PA7<br>Alternate: TIMER0_CH0_ON, TIMER2_CH1, TIMER7_CH0_ON, SPI0_MOSI, TIMER13_CH0, EVENTOUT<br>Additional: ADC01_IN7 |
| PC4 | 44 | I/O | 5VT | Default: PC4<br>Alternate: EVENTOUT<br>Additional: ADC01_IN14 |
| PC5 | 45 | I/O | 5VT | Default: PC5<br>Alternate: USART2_RX, EVENTOUT<br>Additional: ADC01_IN15 |
| PB0 | 46 | I/O | 5VT | Default: PB0 |



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| Pin Name | Pins | Pin Type(1) | I/O Level(2) | Functions description |
|---|---|---|---|---|
| | | | | Alternate: TIMER0_CH1_ON, TIMER2_CH2, TIMER7_CH1_ON, SPI2_MOSI, I2S2_SD, USBHS_ULPI_D1, SDIO_D1, EVENTOUT<br>Additional: ADC01_IN8, IREF |
| PB1 | 47 | I/O | 5VT | Default: PB1<br>Alternate: TIMER0_CH2_ON, TIMER2_CH3, TIMER7_CH2_ON, USBHS_ULPI_D2, SDIO_D2, EVENTOUT<br>Additional: ADC01_IN9 |
| PB2 | 48 | I/O | 5VT | Default: PB2, BOOT1<br>Alternate: TIMER1_CH3, SPI2_MOSI, I2S2_SD, USBHS_ULPI_D4, SDIO_CK, EVENTOUT |
| PF11 | 49 | I/O | 5VT | Default: PF11<br>Alternate: DCI_D12, EVENTOUT |
| PF12 | 50 | I/O | 5VT | Default: PF12<br>Alternate: EVENTOUT |
| $V_{SS}$ | 51 | P | - | Default: $V_{SS}$ |
| $V_{DD}$ | 52 | P | - | Default: $V_{DD}$ |
| PF13 | 53 | I/O | 5VT | Default: PF13<br>Alternate: EVENTOUT |
| PF14 | 54 | I/O | 5VT | Default: PF14<br>Alternate: EVENTOUT |
| PF15 | 55 | I/O | 5VT | Default: PF15<br>Alternate: EVENTOUT |
| PG0 | 56 | I/O | 5VT | Default: PG0<br>Alternate: EVENTOUT |
| PG1 | 57 | I/O | 5VT | Default: PG1<br>Alternate: EVENTOUT |
| PE7 | 58 | I/O | 5VT | Default: PE7<br>Alternate: TIMER0_ETI, EVENTOUT |
| PE8 | 59 | I/O | 5VT | Default: PE8<br>Alternate: TIMER0_CH0_ON, EVENTOUT |
| PE9 | 60 | I/O | 5VT | Default: PE9<br>Alternate: TIMER0_CH0, EVENTOUT |
| $V_{SS}$ | 61 | P | - | Default: $V_{SS}$ |
| $V_{DD}$ | 62 | P | - | Default: $V_{DD}$ |
| PE10 | 63 | I/O | 5VT | Default: PE10<br>Alternate: TIMER0_CH1_ON, EVENTOUT |
| PE11 | 64 | I/O | 5VT | Default: PE11<br>Alternate:TIMER0_CH1, EVENTOUT |
| PE12 | 65 | I/O | 5VT | Default: PE12<br>Alternate:TIMER0_CH2_ON, EVENTOUT |
| PE13 | 66 | I/O | 5VT | Default: PE13 |



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| Pin Name | Pins | Pin Type(1) | I/O Level(2) | Functions description |
|---|---|---|---|---|
| | | | | Alternate:TIMER0_CH2, EVENTOUT |
| PE14 | 67 | I/O | 5VT | Default: PE14<br>Alternate:TIMER0_CH3, EVENTOUT |
| PE15 | 68 | I/O | 5VT | Default: PE15<br>Alternate: TIMER0_BRKIN, EVENTOUT |
| PB10 | 69 | I/O | 5VT | Default: PB10<br>Alternate: TIMER1_CH2,I2C1_SCL, SPI1_SCK, I2S1_CK, I2S2_MCK, USART2_TX, USBHS_ULPI_D3, SDIO_D7, EVENTOUT |
| PB11 | 70 | I/O | 5VT | Default: PB11<br>Alternate: TIMER1_CH3, I2C1_SDA, I2S_CKIN, USART2_RX, USBHS_ULPI_D4, EVENTOUT |
| NC | 71 | - | - | - |
| $V_{DD}$ | 72 | P | - | Default: $V_{DD}$ |
| PB12 | 73 | I/O | 5VT | Default: PB12<br>Alternate: TIMER0_BRKIN, I2C1_SMBA, SPI1_NSS, I2S1_WS, USART2_CK, CAN1_RX, USBHS_ULPI_D5, USBHS_ID, EVENTOUT |
| PB13 | 74 | I/O | 5VT | Default: PB13<br>Alternate: TIMER0_CH0_ON, SPI1_SCK, I2S1_CK, USART2_CTS, CAN1_TX, USBHS_ULPI_D6, EVENTOUT, I2C1_TXFRAME<br>Additional: USBHS_VBUS |
| PB14 | 75 | I/O | 5VT | Default: PB14<br>Alternate: TIMER0_CH1_ON, TIMER7_CH1_ON, SPI1_MISO, I2S1_ADD_SD, USART2_RTS, TIMER11_CH0, USBHS_DM, EVENTOUT |
| PB15 | 76 | I/O | 5VT | Default: PB15<br>Alternate: RTC_REFIN, TIMER0_CH2_ON, TIMER7_CH2_ON, SPI1_MOSI, I2S1_SD, TIMER11_CH1, USBHS_DP, EVENTOUT |
| PD8 | 77 | I/O | 5VT | Default: PD8<br>Alternate: USART2_TX, EVENTOUT |
| PD9 | 78 | I/O | 5VT | Default: PD9<br>Alternate: USART2_RX, EVENTOUT |
| PD10 | 79 | I/O | 5VT | Default: PD10<br>Alternate: USART2_CK, EVENTOUT |
| PD11 | 80 | I/O | 5VT | Default: PD11<br>Alternate: USART2_CTS, EVENTOUT |
| PD12 | 81 | I/O | 5VT | Default: PD12<br>Alternate: TIMER3_CH0,USART2_RTS , EVENTOUT |
| PD13 | 82 | I/O | 5VT | Default: PD13 |



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| Pin Name | Pins | Pin Type(1) | I/O Level(2) | Functions description |
|---|---|---|---|---|
| | | | | Alternate: TIMER3_CH1, EVENTOUT |
| $V_{SS}$ | 83 | P | - | Default: $V_{SS}$ |
| $V_{DD}$ | 84 | P | - | Default: $V_{DD}$ |
| PD14 | 85 | I/O | 5VT | Default: PD14<br>Alternate: TIMER3_CH2, EVENTOUT |
| PD15 | 86 | I/O | 5VT | Default: PD15<br>Alternate: TIMER3_CH3, EVENTOUT, CTC_SYNC |
| PG2 | 87 | I/O | 5VT | Default: PG2<br>Alternate: EVENTOUT |
| PG3 | 88 | I/O | 5VT | Default: PG3<br>Alternate: EVENTOUT |
| PG4 | 89 | I/O | 5VT | Default: PG4<br>Alternate: EVENTOUT |
| PG5 | 90 | I/O | 5VT | Default: PG5<br>Alternate: EVENTOUT |
| PG6 | 91 | I/O | 5VT | Default: PG6<br>Alternate: DCI_D12, EVENTOUT |
| PG7 | 92 | I/O | 5VT | Default: PG7<br>Alternate: USART5_CK, DCI_D13, EVENTOUT |
| PG8 | 93 | I/O | 5VT | Default: PG8<br>Alternate: USART5_RTS, EVENTOUT |
| $V_{SS}$ | 94 | P | - | Default: $V_{SS}$ |
| $V_{DD}$ | 95 | P | - | Default: $V_{DD}$ |
| PC6 | 96 | I/O | 5VT | Default: PC6<br>Alternate: TIMER2_CH0, TIMER7_CH0, I2S1_MCK, USART5_TX, SDIO_D6, DCI_D0, EVENTOUT |
| PC7 | 97 | I/O | 5VT | Default: PC7<br>Alternate: TIMER2_CH1, TIMER7_CH1, SPI1_SCK, I2S1_CK, I2S2_MCK, USART5_RX, SDIO_D7, DCI_D1, EVENTOUT |
| PC8 | 98 | I/O | 5VT | Default: PC8<br>Alternate: TRACED0, TIMER2_CH2, TIMER7_CH2, USART5_CK, SDIO_D0, DCI_D2, EVENTOUT |
| PC9 | 99 | I/O | 5VT | Default: PC9<br>Alternate: CK_OUT1, TIMER2_CH3, TIMER7_CH3, I2C2_SDA, I2S_CKIN, SDIO_D1, DCI_D3, EVENTOUT |
| PA8 | 100 | I/O | 5VT | Default: PA8<br>Alternate: CK_OUT0, TIMER0_CH0, I2C2_SCL, USART0_CK, USBFS_SOF, SDIO_D1, EVENTOUT, CTC_SYNC |
| PA9 | 101 | I/O | 5VT | Default: PA9<br>Alternate: TIMER0_CH1, I2C2_SMBA, SPI1_SCK, I2S1_CK, USART0_TX, SDIO_D2, DCI_D0, EVENTOUT<br>Additional: USBFS_VBUS |



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| Pin Name | Pins | Pin Type(1) | I/O Level(2) | Functions description |
|---|---|---|---|---|
| PA10 | 102 | I/O | 5VT | Default: PA10<br>Alternate: TIMER0_CH2, I2C2_TXFRAME, USART0_RX, USBFS_ID, DCI_D1, EVENTOUT |
| PA11 | 103 | I/O | 5VT | Default: PA11<br>Alternate: TIMER0_CH3, USART0_CTS, USART5_TX, CAN0_RX, USBFS_DM, EVENTOUT |
| PA12 | 104 | I/O | 5VT | Default: PA12<br>Alternate: TIMER0_ETI, USART0_RTS, USART5_RX, CAN0_TX, USBFS_DP, EVENTOUT |
| PA13 | 105 | I/O | 5VT | Default: JTMS, SWDIO, PA13<br>Alternate: EVENTOUT |
| NC | 106 | - | - | - |
| $V_{SS}$ | 107 | P | - | Default: $V_{SS}$ |
| $V_{DD}$ | 108 | P | - | Default: $V_{DD}$ |
| PA14 | 109 | I/O | 5VT | Default: JTCK, SWCLK, PA14<br>Alternate: EVENTOUT |
| PA15 | 110 | I/O | 5VT | Default: JTDI, PA15<br>Alternate: TIMER1_CH0, TIMER1_ETI, SPI0_NSS, SPI2_NSS, I2S2_WS, USART0_TX, EVENTOUT |
| PC10 | 111 | I/O | 5VT | Default: PC10<br>Alternate: SPI2_SCK, I2S2_CK, USART2_TX, UART3_TX, SDIO_D2, DCI_D8, EVENTOUT |
| PC11 | 112 | I/O | 5VT | Default: PC11<br>Alternate: I2S2_ADD_SD, SPI2_MISO, USART2_RX, UART3_RX, SDIO_D3, DCI_D4, EVENTOUT |
| PC12 | 113 | I/O | 5VT | Default: PC12<br>Alternate: I2C1_SDA, SPI2_MOSI, I2S2_SD, USART2_CK, UART4_TX, SDIO_CK, DCI_D9, EVENTOUT |
| PD0 | 114 | I/O | 5VT | Default: PD0<br>Alternate: SPI2_MOSI, I2S2_SD, CAN0_RX, EVENTOUT |
| PD1 | 115 | I/O | 5VT | Default: PD1<br>Alternate: SPI1_NSS, I2S1_WS, CAN0_TX, EVENTOUT |
| PD2 | 116 | I/O | 5VT | Default: PD2<br>Alternate: TIMER2_ETI, UART4_RX, SDIO_CMD, DCI_D11, EVENTOUT |
| PD3 | 117 | I/O | 5VT | Default: PD3<br>Alternate: TRACED1, SPI1_SCK, I2S1_CK, USART1_CTS, DCI_D5, EVENTOUT |
| PD4 | 118 | I/O | 5VT | Default: PD4<br>Alternate: USART1_RTS, EVENTOUT |
| PD5 | 119 | I/O | 5VT | Default: PD5<br>Alternate: USART1_TX, EVENTOUT |



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| Pin Name | Pins | Pin Type(1) | I/O Level(2) | Functions description |
|---|---|---|---|---|
| $V_{SS}$ | 120 | P | - | Default: $V_{SS}$ |
| $V_{DD}$ | 121 | P | - | Default: $V_{DD}$ |
| PD6 | 122 | I/O | 5VT | Default: PD6<br>Alternate: SPI2_MOSI, I2S2_SD, USART1_RX, DCI_D10, EVENTOUT |
| PD7 | 123 | I/O | 5VT | Default: PD7<br>Alternate: USART1_CK, EVENTOUT |
| PG9 | 124 | I/O | 5VT | Default: PG9<br>Alternate: USART5_RX, DCI_VSYNC, EVENTOUT |
| PG10 | 125 | I/O | 5VT | Default: PG10<br>Alternate: DCI_D2, EVENTOUT |
| PG11 | 126 | I/O | 5VT | Default: PG11<br>Alternate: DCI_D3, EVENTOUT |
| PG12 | 127 | I/O | 5VT | Default: PG12<br>Alternate: USART5_RTS, EVENTOUT |
| PG13 | 128 | I/O | 5VT | Default: PG13<br>Alternate: TRACED2, USART5_CTS, EVENTOUT |
| PG14 | 129 | I/O | 5VT | Default: PG14<br>Alternate:TRACED3, USART5_TX, EVENTOUT |
| $V_{SS}$ | 130 | P | - | Default: $V_{SS}$ |
| $V_{DD}$ | 131 | P | - | Default: $V_{DD}$ |
| PG15 | 132 | I/O | 5VT | Default: PG15<br>Alternate: USART5_CTS, DCI_D13, EVENTOUT |
| PB3 | 133 | I/O | 5VT | Default: JTDO, PB3<br>Alternate: TRACESWO, TIMER1_CH1, SPI0_SCK, SPI2_SCK, I2S2_CK, USART0_RX, I2C1_SDA, EVENTOUT |
| PB4 | 134 | I/O | 5VT | Default: NJTRST, PB4<br>Alternate: TIMER2_CH0, I2C0_TXFRAME, SPI0_MISO, SPI2_MISO, I2S2_ADD_SD, I2C2_SDA, SDIO_D0, EVENTOUT |
| PB5 | 135 | I/O | 5VT | Default: PB5<br>Alternate: TIMER2_CH1, I2C0_SMBA, SPI0_MOSI, SPI2_MOSI, I2S2_SD, CAN1_RX, USBHS_ULPI_D7, DCI_D10, EVENTOUT |
| PB6 | 136 | I/O | 5VT | Default: PB6<br>Alternate: TIMER3_CH0, I2C0_SCL, USART0_TX, CAN1_TX, DCI_D5, EVENTOUT |
| PB7 | 137 | I/O | 5VT | Default: PB7<br>Alternate: TIMER3_CH1, I2C0_SDA, USART0_RX, DCI_VSYNC, EVENTOUT |
| BOOT0 | 138 | I/O | 5VT | Default: BOOT0 |
| PB8 | 139 | I/O | 5VT | Default: PB8 |



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| Pin Name | Pins | Pin Type(1) | I/O Level(2) | Functions description |
|---|---|---|---|---|
| | | | | Alternate: TIMER1_CH0, TIMER1_ETI, TIMER3_CH2, TIMER9_CH0, I2C0_SCL, CAN0_RX, SDIO_D4, DCI_D6, EVENTOUT |
| PB9 | 140 | I/O | 5VT | Default: PB9<br>Alternate: TIMER1_CH1, TIMER3_CH3, TIMER10_CH0, I2C0_SDA, SPI1_NSS, I2S1_WS, CAN0_TX, SDIO_D5, DCI_D7, EVENTOUT |
| PE0 | 141 | I/O | 5VT | Default: PE0<br>Alternate: TIMER3_ETI, DCI_D2, EVENTOUT |
| PE1 | 142 | I/O | 5VT | Default: PE1<br>Alternate: TIMER0_CH1_ON, DCI_D3, EVENTOUT |
| PDR_ON | 143 | P | - | Default: PDR_ON |
| $V_{DD}$ | 144 | P | - | Default: $V_{DD}$ |

**Notes:**

(1) Type: I = input, O = output, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

### 2.6.2. GD32F425Vx LQFP100 pin definitions

**Table 2-4. GD32F425Vx LQFP100 pin definitions**

| Pin Name | Pins | Pin Type(1) | I/O Level(2) | Functions description |
|---|---|---|---|---|
| PE2 | 1 | I/O | 5VT | Default: PE2<br>Alternate: TRACECK, EVENTOUT |
| PE3 | 2 | I/O | 5VT | Default: PE3<br>Alternate: TRACED0, EVENTOUT |
| PE4 | 3 | I/O | 5VT | Default: PE4<br>Alternate: TRACED1, DCI_D4, EVENTOUT |
| PE5 | 4 | I/O | 5VT | Default: PE5<br>Alternate: TRACED2, TIMER8_CH0, DCI_D6, EVENTOUT |
| PE6 | 5 | I/O | 5VT | Default: PE6<br>Alternate: TRACED3, TIMER8_CH1, DCI_D7, EVENTOUT |
| $V_{BAT}$ | 6 | P | - | Default: $V_{BAT}$ |
| PC13-TAMPER-RTC | 7 | I/O | 5VT | Default: PC13<br>Alternate: EVENTOUT<br>Additional: RTC_TAMP0, RTC_OUT, RTC_TS |
| PC14-OSC32IN | 8 | I/O | 5VT | Default: PC14<br>Alternate: EVENTOUT<br>Additional: OSC32IN |
| PC15-OSC32O | 9 | I/O | 5VT | Default: PC15<br>Alternate: EVENTOUT |



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| Pin Name | Pins | Pin Type(1) | I/O Level(2) | Functions description |
|---|---|---|---|---|
| UT | | | | Additional: OSC32OUT |
| $V_{SS}$ | 10 | P | - | Default: $V_{SS}$ |
| $V_{DD}$ | 11 | P | - | Default: $V_{DD}$ |
| PH0 | 12 | I/O | 5VT | Default: PH0, OSCIN<br>Alternate: EVENTOUT<br>Additional: OSCIN |
| PH1 | 13 | I/O | 5VT | Default: PH1, OSCOUT<br>Alternate: EVENTOUT<br>Additional: OSCOUT |
| NRST | 14 | - | - | Default: NRST |
| PC0 | 15 | I/O | 5VT | Default: PC0<br>Alternate: USBHS_ULPI_STP, EVENTOUT<br>Additional: ADC012_IN10 |
| PC1 | 16 | I/O | 5VT | Default: PC1<br>Alternate: SPI2_MOSI, I2S2_SD, SPI1_MOSI, I2S1_SD, EVENTOUT<br>Additional: ADC012_IN11 |
| PC2 | 17 | I/O | 5VT | Default: PC2<br>Alternate: SPI1_MISO, I2S1_ADD_SD, USBHS_ULPI_DIR, EVENTOUT<br>Additional: ADC012_IN12 |
| PC3 | 18 | I/O | 5VT | Default: PC3<br>Alternate: SPI1_MOSI, I2S1_SD, USBHS_ULPI_NXT, EVENTOUT<br>Additional: ADC012_IN13 |
| $V_{DD}$ | 19 | P | - | Default: $V_{DD}$ |
| $V_{SSA}$ | 20 | P | - | Default: $V_{SSA}$ |
| $V_{REF+}$ | 21 | P | - | Default: $V_{REF+}$ |
| $V_{DDA}$ | 22 | P | - | Default: $V_{DDA}$ |
| PA0-WKUP | 23 | I/O | 5VT | Default: PA0<br>Alternate: TIMER1_CH0, TIMER1_ETI, TIMER4_CH0, TIMER7_ETI, USART1_CTS, UART3_TX, EVENTOUT<br>Additional: ADC012_IN0, WKUP |
| PA1 | 24 | I/O | 5VT | Default: PA1<br>Alternate: TIMER1_CH1, TIMER4_CH1, USART1_RTS, UART3_RX, EVENTOUT<br>Additional: ADC012_IN1 |
| PA2 | 25 | I/O | 5VT | Default: PA2<br>Alternate: TIMER1_CH2, TIMER4_CH2, TIMER8_CH0, I2S_CKIN, USART1_TX, EVENTOUT<br>Additional: ADC012_IN2 |
| PA3 | 26 | I/O | 5VT | Default: PA3 |



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|---|---|---|---|---|
| | | | | Alternate: TIMER1_CH3, TIMER4_CH3, TIMER8_CH1, I2S1_MCK, USART1_RX, USBHS_ULPI_D0, EVENTOUT<br>Additional: ADC012_IN3 |
| $V_{SS}$ | 27 | P | - | Default: $V_{SS}$ |
| $V_{DD}$ | 28 | P | - | Default: $V_{DD}$ |
| PA4 | 29 | I/O | | Default: PA4<br>Alternate: SPI0_NSS, SPI2_NSS, I2S2_WS, USART1_CK, USBHS_SOF, DCI_HSYNC, EVENTOUT<br>Additional: ADC01_IN4, DAC_OUT0 |
| PA5 | 30 | I/O | | Default: PA5<br>Alternate: TIMER1_CH0, TIMER1_ETI, TIMER7_CH0_ON, SPI0_SCK, USBHS_ULPI_CK, EVENTOUT<br>Additional: ADC01_IN5, DAC_OUT1 |
| PA6 | 31 | I/O | 5VT | Default: PA6<br>Alternate: TIMER0_BRKIN, TIMER2_CH0, TIMER7_BRKIN, SPI0_MISO, I2S1_MCK, TIMER12_CH0, SDIO_CMD, DCI_PIXCLK, EVENTOUT<br>Additional: ADC01_IN6 |
| PA7 | 32 | I/O | 5VT | Default: PA7<br>Alternate: TIMER0_CH0_ON, TIMER2_CH1, TIMER7_CH0_ON, SPI0_MOSI, TIMER13_CH0, EVENTOUT<br>Additional: ADC01_IN7 |
| PC4 | 33 | I/O | 5VT | Default: PC4<br>Alternate: EVENTOUT<br>Additional: ADC01_IN14 |
| PC5 | 34 | I/O | 5VT | Default: PC5<br>Alternate: USART2_RX, EVENTOUT<br>Additional: ADC01_IN15 |
| PB0 | 35 | I/O | 5VT | Default: PB0<br>Alternate: TIMER0_CH1_ON, TIMER2_CH2, TIMER7_CH1_ON, SPI2_MOSI, I2S2_SD, USBHS_ULPI_D1, SDIO_D1, EVENTOUT<br>Additional: ADC01_IN8, IREF |
| PB1 | 36 | I/O | 5VT | Default: PB1<br>Alternate: TIMER0_CH2_ON, TIMER2_CH3, TIMER7_CH2_ON, USBHS_ULPI_D2, SDIO_D2, EVENTOUT<br>Additional: ADC01_IN9 |
| PB2 | 37 | I/O | 5VT | Default: PB2, BOOT1<br>Alternate: TIMER1_CH3, SPI2_MOSI, I2S2_SD, USBHS_ULPI_D4, SDIO_CK, EVENTOUT |
| PE7 | 38 | I/O | 5VT | Default: PE7<br>Alternate: TIMER0_ETI, EVENTOUT |



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|---|---|---|---|---|
| PE8 | 39 | I/O | 5VT | Default: PE8<br>Alternate: TIMER0_CH0_ON, EVENTOUT |
| PE9 | 40 | I/O | 5VT | Default: PE9<br>Alternate: TIMER0_CH0, EVENTOUT |
| PE10 | 41 | I/O | 5VT | Default: PE10<br>Alternate: TIMER0_CH1_ON, EVENTOUT |
| PE11 | 42 | I/O | 5VT | Default: PE11<br>Alternate: TIMER0_CH1, EVENTOUT |
| PE12 | 43 | I/O | 5VT | Default: PE12<br>Alternate:TIMER0_CH2_ON, EVENTOUT |
| PE13 | 44 | I/O | 5VT | Default: PE13<br>Alternate: TIMER0_CH2, EVENTOUT |
| PE14 | 45 | I/O | 5VT | Default: PE14<br>Alternate: TIMER0_CH3, EVENTOUT |
| PE15 | 46 | I/O | 5VT | Default: PE15<br>Alternate: TIMER0_BRKIN, EVENTOUT |
| PB10 | 47 | I/O | 5VT | Default: PB10<br>Alternate: TIMER1_CH2, I2C1_SCL, SPI1_SCK, I2S1_CK, I2S2_MCK, USART2_TX, USBHS_ULPI_D3, SDIO_D7, EVENTOUT |
| PB11 | 48 | I/O | 5VT | Default: PB11<br>Alternate: TIMER1_CH3, I2C1_SDA, I2S_CKIN, USART2_RX, USBHS_ULPI_D4, EVENTOUT |
| NC | 49 | - | - | - |
| $V_{DD}$ | 50 | P | - | Default: $V_{DD}$ |
| PB12 | 51 | I/O | 5VT | Default: PB12<br>Alternate: TIMER0_BRKIN, I2C1_SMBA, SPI1_NSS, I2S1_WS, USART2_CK, CAN1_RX, USBHS_ULPI_D5, USBHS_ID, EVENTOUT |
| PB13 | 52 | I/O | 5VT | Default: PB13<br>Alternate: TIMER0_CH0_ON, SPI1_SCK, I2S1_CK, USART2_CTS, CAN1_TX, USBHS_ULPI_D6, EVENTOUT, I2C1_TXFRAME<br>Additional: USBHS_VBUS |
| PB14 | 53 | I/O | 5VT | Default: PB14<br>Alternate: TIMER0_CH1_ON, TIMER7_CH1_ON, SPI1_MISO, I2S1_ADD_SD, USART2_RTS, TIMER11_CH0, USBHS_DM, EVENTOUT |
| PB15 | 54 | I/O | 5VT | Default: PB15<br>Alternate: RTC_REFIN, TIMER0_CH2_ON, TIMER7_CH2_ON, SPI1_MOSI, I2S1_SD, TIMER11_CH1, USBHS_DP, EVENTOUT |



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|---|---|---|---|---|
| PD8 | 55 | I/O | 5VT | Default: PD8<br>Alternate: USART2_TX, EVENTOUT |
| PD9 | 56 | I/O | 5VT | Default: PD9<br>Alternate: USART2_RX, EVENTOUT |
| PD10 | 57 | I/O | 5VT | Default: PD10<br>Alternate: USART2_CK, EVENTOUT |
| PD11 | 58 | I/O | 5VT | Default: PD11<br>Alternate: USART2_CTS, EVENTOUT |
| PD12 | 59 | I/O | 5VT | Default: PD12<br>Alternate: TIMER3_CH0, USART2_RTS, EVENTOUT |
| PD13 | 60 | I/O | 5VT | Default: PD13<br>Alternate: TIMER3_CH1, EVENTOUT |
| PD14 | 61 | I/O | 5VT | Default: PD14<br>Alternate: TIMER3_CH2, EVENTOUT |
| PD15 | 62 | I/O | 5VT | Default: PD15<br>Alternate:TIMER3_CH3, EVENTOUT, CTC_SYNC |
| PC6 | 63 | I/O | 5VT | Default: PC6<br>Alternate: TIMER2_CH0, TIMER7_CH0, I2S1_MCK, USART5_TX, SDIO_D6, DCI_D0, EVENTOUT |
| PC7 | 64 | I/O | 5VT | Default: PC7<br>Alternate: TIMER2_CH1, TIMER7_CH1, SPI1_SCK, I2S1_CK, I2S2_MCK, USART5_RX, SDIO_D7, DCI_D1, EVENTOUT |
| PC8 | 65 | I/O | 5VT | Default: PC8<br>Alternate: TRACED0, TIMER2_CH2, TIMER7_CH2, USART5_CK, SDIO_D0, DCI_D2, EVENTOUT |
| PC9 | 66 | I/O | 5VT | Default: PC9<br>Alternate: CK_OUT1, TIMER2_CH3, TIMER7_CH3, I2C2_SDA, I2S_CKIN, SDIO_D1, DCI_D3, EVENTOUT |
| PA8 | 67 | I/O | 5VT | Default: PA8<br>Alternate: CK_OUT0, TIMER0_CH0, I2C2_SCL, USART0_CK, USBFS_SOF, SDIO_D1, EVENTOUT, CTC_SYNC |
| PA9 | 68 | I/O | 5VT | Default: PA9<br>Alternate: TIMER0_CH1, I2C2_SMBA, SPI1_SCK, I2S1_CK, USART0_TX, SDIO_D2, DCI_D0, EVENTOUT<br>Additional: USBFS_VBUS |
| PA10 | 69 | I/O | 5VT | Default: PA10<br>Alternate: TIMER0_CH2, USART0_RX, USBFS_ID, DCI_D1, EVENTOUT, I2C2_TXFRAME |
| PA11 | 70 | I/O | 5VT | Default: PA11<br>Alternate: TIMER0_CH3, USART0_CTS, USART5_TX, CAN0_RX, USBFS_DM, EVENTOUT |
| PA12 | 71 | I/O | 5VT | Default: PA12 |



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|---|---|---|---|---|
| | | | | Alternate: TIMER0_ETI, USART0_RTS, USART5_RX, CAN0_TX, USBFS_DP, EVENTOUT |
| PA13 | 72 | I/O | 5VT | Default: JTMS, SWDIO, PA13<br>Alternate: EVENTOUT |
| NC | 73 | - | - | - |
| $V_{SS}$ | 74 | P | - | Default: $V_{SS}$ |
| $V_{DD}$ | 75 | P | - | Default: $V_{DD}$ |
| PA14 | 76 | I/O | 5VT | Default: JTCK, SWCLK, PA14<br>Alternate: EVENTOUT |
| PA15 | 77 | I/O | 5VT | Default: JTDI, PA15<br>Alternate: TIMER1_CH0, TIMER1_ETI, SPI0_NSS, SPI2_NSS, I2S2_WS, USART0_TX, EVENTOUT |
| PC10 | 78 | I/O | 5VT | Default: PC10<br>Alternate: SPI2_SCK, I2S2_CK, USART2_TX, UART3_TX, SDIO_D2, DCI_D8, EVENTOUT |
| PC11 | 79 | I/O | 5VT | Default: PC11<br>Alternate: I2S2_ADD_SD, SPI2_MISO, USART2_RX, UART3_RX, SDIO_D3, DCI_D4, EVENTOUT |
| PC12 | 80 | I/O | 5VT | Default: PC12<br>Alternate: I2C1_SDA, SPI2_MOSI, I2S2_SD, USART2_CK, UART4_TX, SDIO_CK, DCI_D9, EVENTOUT |
| PD0 | 81 | I/O | 5VT | Default: PD0<br>Alternate: SPI2_MOSI, I2S2_SD, CAN0_RX, EVENTOUT |
| PD1 | 82 | I/O | 5VT | Default: PD1<br>Alternate: SPI1_NSS, I2S1_WS, CAN0_TX, EVENTOUT |
| PD2 | 83 | I/O | 5VT | Default: PD2<br>Alternate: TIMER2_ETI, UART4_RX, SDIO_CMD, DCI_D11, EVENTOUT |
| PD3 | 84 | I/O | 5VT | Default: PD3<br>Alternate: TRACED1, SPI1_SCK, I2S1_CK, USART1_CTS, DCI_D5, EVENTOUT |
| PD4 | 85 | I/O | 5VT | Default: PD4<br>Alternate: USART1_RTS, EVENTOUT |
| PD5 | 86 | I/O | 5VT | Default: PD5<br>Alternate: USART1_TX, EVENTOUT |
| PD6 | 87 | I/O | 5VT | Default: PD6<br>Alternate: SPI2_MOSI, I2S2_SD, USART1_RX, DCI_D10, EVENTOUT |
| PD7 | 88 | I/O | 5VT | Default: PD7<br>Alternate: USART1_CK, EVENTOUT |
| PB3 | 89 | I/O | 5VT | Default: JTDO, PB3<br>Alternate: TRACESWO, TIMER1_CH1, SPI0_SCK, SPI2_SCK, |



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|---|---|---|---|---|
| | | | | I2S2_CK, USART0_RX, I2C1_SDA, EVENTOUT |
| PB4 | 90 | I/O | 5VT | Default: NJTRST, PB4<br>Alternate: TIMER2_CH0, SPI0_MISO, SPI2_MISO, I2S2_ADD_SD, I2C2_SDA, SDIO_D0, EVENTOUT, I2C0_TXFRAME |
| PB5 | 91 | I/O | 5VT | Default: PB5<br>Alternate: TIMER2_CH1, I2C0_SMBA, SPI0_MOSI, SPI2_MOSI, I2S2_SD, CAN1_RX, USBHS_ULPI_D7, DCI_D10, EVENTOUT |
| PB6 | 92 | I/O | 5VT | Default: PB6<br>Alternate: TIMER3_CH0, I2C0_SCL, USART0_TX, CAN1_TX, DCI_D5, EVENTOUT |
| PB7 | 93 | I/O | 5VT | Default: PB7<br>Alternate: TIMER3_CH1, I2C0_SDA, USART0_RX, DCI_VSYNC, EVENTOUT |
| BOOT0 | 94 | I/O | 5VT | Default: BOOT0 |
| PB8 | 95 | I/O | 5VT | Default: PB8<br>Alternate: TIMER1_CH0, TIMER1_ETI, TIMER3_CH2, TIMER9_CH0, I2C0_SCL, CAN0_RX, SDIO_D4, DCI_D6, EVENTOUT |
| PB9 | 96 | I/O | 5VT | Default: PB9<br>Alternate: TIMER1_CH1, TIMER3_CH3, TIMER10_CH0, I2C0_SDA, SPI1_NSS, I2S1_WS, CAN0_TX, SDIO_D5, DCI_D7, EVENTOUT |
| PE0 | 97 | I/O | 5VT | Default: PE0<br>Alternate: TIMER3_ETI, DCI_D2, EVENTOUT |
| PE1 | 98 | I/O | 5VT | Default: PE1<br>Alternate: TIMER0_CH1_ON, DCI_D3, EVENTOUT |
| $V_{SS}$ | 99 | P | - | Default: $V_{SS}$ |
| $V_{DD}$ | 100 | P | - | Default: $V_{DD}$ |

**Notes:**

(1) Type: I = input, O = output, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

### 2.6.3. GD32F425Vx BGA100 pin definitions

**Table 2-5. GD32F425Vx BGA100 pin definitions**

| Pin Name | Pins | Pin Type(1) | I/O Level(2) | Functions description |
|---|---|---|---|---|
| PE2 | B2 | I/O | 5VT | Default: PE2<br>Alternate: TRACECK, EVENTOUT |
| PE3 | A1 | I/O | 5VT | Default: PE3 |



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|---|---|---|---|---|
| | | | | Alternate:TRACED0, EVENTOUT |
| PE4 | B1 | I/O | 5VT | Default: PE4<br>Alternate: TRACED1, DCI_D4, EVENTOUT |
| PE5 | C2 | I/O | 5VT | Default: PE5<br>Alternate: TRACED2, TIMER8_CH0, DCI_D6, EVENTOUT |
| PE6 | D2 | I/O | 5VT | Default: PE6<br>Alternate: TRACED3, TIMER8_CH1, DCI_D7, EVENTOUT |
| $V_{BAT}$ | E2 | P | - | Default: $V_{BAT}$ |
| PC13-TAMPER-RTC | C1 | I/O | 5VT | Default: PC13<br>Alternate: EVENTOUT<br>Additional: RTC_TAMP0, RTC_OUT, RTC_TS |
| PC14-OSC32IN | D1 | I/O | 5VT | Default: PC14<br>Alternate: EVENTOUT<br>Additional: OSC32IN |
| PC15-OSC32OUT | E1 | I/O | 5VT | Default: PC15<br>Alternate: EVENTOUT<br>Additional: OSC32OUT |
| $V_{SS}$ | F2 | P | - | Default: $V_{SS}$ |
| $V_{DD}$ | G2 | P | - | Default: $V_{DD}$ |
| PH0 | F1 | I/O | 5VT | Default: PH0, OSCIN<br>Alternate: EVENTOUT<br>Additional: OSCIN |
| PH1 | G1 | I/O | 5VT | Default: PH1, OSCOUT<br>Alternate: EVENTOUT<br>Additional: OSCOUT |
| NRST | H2 | - | - | Default: NRST |
| PC0 | H1 | I/O | 5VT | Default: PC0<br>Alternate: USBHS_ULPI_STP, EVENTOUT<br>Additional: ADC012_IN10 |
| PC1 | J2 | I/O | 5VT | Default: PC1<br>Alternate: SPI2_MOSI, I2S2_SD, SPI1_MOSI, I2S1_SD, EVENTOUT<br>Additional: ADC012_IN11 |
| PC2 | J3 | I/O | 5VT | Default: PC2<br>Alternate: SPI1_MISO, I2S1_ADD_SD, USBHS_ULPI_DIR, EVENTOUT<br>Additional: ADC012_IN12 |
| PC3 | K2 | I/O | 5VT | Default: PC3<br>Alternate: SPI1_MOSI, I2S1_SD, USBHS_ULPI_NXT, EVENTOUT<br>Additional: ADC012_IN13 |
| $V_{SSA}$ | J1 | P | - | Default: $V_{SSA}$ |



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|---|---|---|---|---|
| $V_{REFN}$ | K1 | P | - | Default: $V_{REF-}$ |
| $V_{REFP}$ | L1 | P | - | Default: $V_{REF+}$ |
| $V_{DDA}$ | M1 | P | - | Default: $V_{DDA}$ |
| PA0-WKUP | L2 | I/O | 5VT | Default: PA0<br>Alternate: TIMER1_CH0, TIMER1_ETI, TIMER4_CH0, TIMER7_ETI, USART1_CTS, UART3_TX, EVENTOUT<br>Additional: ADC012_IN0, WKUP |
| PA1 | M2 | I/O | 5VT | Default: PA1<br>Alternate: TIMER1_CH1, TIMER4_CH1, USART1_RTS, UART3_RX, EVENTOUT<br>Additional: ADC012_IN1 |
| PA2 | K3 | I/O | 5VT | Default: PA2<br>Alternate: TIMER1_CH2, TIMER4_CH2, TIMER8_CH0, I2S_CKIN, USART1_TX, EVENTOUT<br>Additional: ADC012_IN2 |
| PA3 | L3 | I/O | 5VT | Default: PA3<br>Alternate: TIMER1_CH3, TIMER4_CH3, TIMER8_CH1, I2S1_MCK, USART1_RX, USBHS_ULPI_D0, EVENTOUT<br>Additional: ADC012_IN3 |
| NC | E3 | - | - | - |
| PA4 | M3 | I/O | | Default: PA4<br>Alternate: SPI0_NSS, SPI2_NSS, I2S2_WS, USART1_CK, USBHS_SOF, DCI_HSYNC, EVENTOUT<br>Additional: ADC01_IN4, DAC_OUT0 |
| PA5 | K4 | I/O | | Default: PA5<br>Alternate: TIMER1_CH0, TIMER1_ETI, TIMER7_CH0_ON, SPI0_SCK, USBHS_ULPI_CK, EVENTOUT<br>Additional: ADC01_IN5, DAC_OUT1 |
| PA6 | L4 | I/O | 5VT | Default: PA6<br>Alternate: TIMER0_BRKIN, TIMER2_CH0, TIMER7_BRKIN, SPI0_MISO, I2S1_MCK, TIMER12_CH0, SDIO_CMD, DCI_PIXCLK, EVENTOUT<br>Additional: ADC01_IN6 |
| PA7 | M4 | I/O | 5VT | Default: PA7<br>Alternate: TIMER0_CH0_ON, TIMER2_CH1, TIMER7_CH0_ON, SPI0_MOSI, TIMER13_CH0, EVENTOUT<br>Additional: ADC01_IN7 |
| PC4 | K5 | I/O | 5VT | Default: PC4<br>Alternate: EVENTOUT<br>Additional: ADC01_IN14 |
| PC5 | L5 | I/O | 5VT | Default: PC5<br>Alternate: USART2_RX, EVENTOUT |



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|---|---|---|---|---|
| | | | | Additional: ADC01_IN15 |
| PB0 | M5 | I/O | 5VT | Default: PB0<br>Alternate: TIMER0_CH1_ON, TIMER2_CH2, TIMER7_CH1_ON, SPI2_MOSI, I2S2_SD, USBHS_ULPI_D1, SDIO_D1, EVENTOUT<br>Additional: ADC01_IN8, IREF |
| PB1 | M6 | I/O | 5VT | Default: PB1<br>Alternate: TIMER0_CH2_ON, TIMER2_CH3, TIMER7_CH2_ON, USBHS_ULPI_D2, SDIO_D2, EVENTOUT<br>Additional: ADC01_IN9 |
| PB2 | L6 | I/O | 5VT | Default: PB2, BOOT1<br>Alternate: TIMER1_CH3, SPI2_MOSI, I2S2_SD, USBHS_ULPI_D4, SDIO_CK, EVENTOUT |
| PE7 | M7 | I/O | 5VT | Default: PE7<br>Alternate: TIMER0_ETI, EVENTOUT |
| PE8 | L7 | I/O | 5VT | Default: PE8<br>Alternate: TIMER0_CH0_ON, EVENTOUT |
| PE9 | M8 | I/O | 5VT | Default: PE9<br>Alternate: TIMER0_CH0, EVENTOUT |
| PE10 | L8 | I/O | 5VT | Default: PE10<br>Alternate: TIMER0_CH1_ON, EVENTOUT |
| PE11 | M9 | I/O | 5VT | Default: PE11<br>Alternate: TIMER0_CH1, EVENTOUT |
| PE12 | L9 | I/O | 5VT | Default: PE12<br>Alternate: TIMER0_CH2_ON, EVENTOUT |
| PE13 | M10 | I/O | 5VT | Default: PE13<br>Alternate: TIMER0_CH2, EVENTOUT |
| PE14 | M11 | I/O | 5VT | Default: PE14<br>Alternate: TIMER0_CH3, EVENTOUT |
| PE15 | M12 | I/O | 5VT | Default: PE15<br>Alternate: TIMER0_BRKIN, EVENTOUT |
| PB10 | L10 | I/O | 5VT | Default: PB10<br>Alternate: TIMER1_CH2, I2C1_SCL, SPI1_SCK, I2S1_CK, I2S2_MCK, USART2_TX, USBHS_ULPI_D3, SDIO_D7, EVENTOUT |
| PB11 | K9 | I/O | 5VT | Default: PB11<br>Alternate: TIMER1_CH3, I2C1_SDA, I2S_CKIN, USART2_RX, USBHS_ULPI_D4, EVENTOUT |
| NC | L11 | - | - | - |
| $V_{SS}$ | F12 | P | - | Default: $V_{SS}$ |
| $V_{DD}$ | G12 | P | - | Default: $V_{DD}$ |
| PB12 | L12 | I/O | 5VT | Default: PB12 |



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| Pin Name | Pins | Pin Type(1) | I/O Level(2) | Functions description |
|---|---|---|---|---|
| | | | | Alternate: TIMER0_BRKIN, I2C1_SMBA, SPI1_NSS, I2S1_WS, USART2_CK, CAN1_RX, USBHS_ULPI_D5, USBHS_ID, EVENTOUT |
| PB13 | K12 | I/O | 5VT | Default: PB13<br>Alternate: TIMER0_CH0_ON, SPI1_SCK, I2S1_CK, USART2_CTS, CAN1_TX, USBHS_ULPI_D6, EVENTOUT, I2C1_TXFRAME<br>Additional: USBHS_VBUS |
| PB14 | K11 | I/O | 5VT | Default: PB14<br>Alternate: TIMER0_CH1_ON, TIMER7_CH1_ON, SPI1_MISO, I2S1_ADD_SD, USART2_RTS, TIMER11_CH0, USBHS_DM, EVENTOUT |
| PB15 | K10 | I/O | 5VT | Default: PB15<br>Alternate: RTC_REFIN, TIMER0_CH2_ON, TIMER7_CH2_ON, SPI1_MOSI, I2S1_SD, TIMER11_CH1, USBHS_DP, EVENTOUT |
| PD9 | K8 | I/O | 5VT | Default: PD9<br>Alternate: USART2_RX, EVENTOUT |
| PD10 | J12 | I/O | 5VT | Default: PD10<br>Alternate: USART2_CK, EVENTOUT |
| PD11 | J11 | I/O | 5VT | Default: PD11<br>Alternate: USART2_CTS, EVENTOUT |
| PD12 | J10 | I/O | 5VT | Default: PD12<br>Alternate: TIMER3_CH0, USART2_RTS, EVENTOUT |
| PD13 | H12 | I/O | 5VT | Default: PD13<br>Alternate: TIMER3_CH1, EVENTOUT |
| PD14 | H11 | I/O | 5VT | Default: PD14<br>Alternate: TIMER3_CH2, EVENTOUT |
| PD15 | H10 | I/O | 5VT | Default: PD15<br>Alternate: TIMER3_CH3, EVENTOUT, CTC_SYNC |
| PC6 | E12 | I/O | 5VT | Default: PC6<br>Alternate: TIMER2_CH0, TIMER7_CH0, I2S1_MCK, USART5_TX, SDIO_D6, DCI_D0, EVENTOUT |
| PC7 | E11 | I/O | 5VT | Default: PC7<br>Alternate: TIMER2_CH1, TIMER7_CH1, SPI1_SCK, I2S1_CK, I2S2_MCK, USART5_RX, SDIO_D7, DCI_D1, EVENTOUT |
| PC8 | E10 | I/O | 5VT | Default: PC8<br>Alternate: TRACED0, TIMER2_CH2, TIMER7_CH2, USART5_CK, SDIO_D0, DCI_D2, EVENTOUT |
| PC9 | D12 | I/O | 5VT | Default: PC9<br>Alternate: CK_OUT1, TIMER2_CH3, TIMER7_CH3, I2C2_SDA, I2S_CKIN, SDIO_D1, DCI_D3, EVENTOUT |



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| Pin Name | Pins | Pin Type(1) | I/O Level(2) | Functions description |
|---|---|---|---|---|
| PA8 | D11 | I/O | 5VT | Default: PA8<br>Alternate: CK_OUT0, TIMER0_CH0, I2C2_SCL, USART0_CK, USBFS_SOF, SDIO_D1, EVENTOUT, CTC_SYNC |
| PA9 | D10 | I/O | 5VT | Default: PA9<br>Alternate: TIMER0_CH1, I2C2_SMBA, SPI1_SCK, I2S1_CK, USART0_TX, SDIO_D2, DCI_D0, EVENTOUT<br>Additional: USBFS_VBUS |
| PA10 | C12 | I/O | 5VT | Default: PA10<br>Alternate: TIMER0_CH2, USART0_RX, USBFS_ID, DCI_D1, EVENTOUT, I2C2_TXFRAME |
| PA11 | B12 | I/O | 5VT | Default: PA11<br>Alternate: TIMER0_CH3, USART0_CTS, USART5_TX, CAN0_RX, USBFS_DM, EVENTOUT |
| PA12 | A12 | I/O | 5VT | Default: PA12<br>Alternate: TIMER0_ETI, USART0_RTS, USART5_RX, CAN0_TX, USBFS_DP, EVENTOUT |
| PA13 | A11 | I/O | 5VT | Default: JTMS, SWDIO, PA13<br>Alternate: EVENTOUT |
| NC | C11 | - | - | - |
| $V_{SS}$ | F11 | P | - | Default: $V_{SS}$ |
| $V_{DD}$ | G11 | P | - | Default: $V_{DD}$ |
| PA14 | A10 | I/O | 5VT | Default: JTCK, SWCLK, PA14<br>Alternate: EVENTOUT |
| PA15 | A9 | I/O | 5VT | Default: JTDI, PA15<br>Alternate: TIMER1_CH0, TIMER1_ETI, SPI0_NSS, SPI2_NSS, I2S2_WS, USART0_TX, EVENTOUT |
| PC10 | B11 | I/O | 5VT | Default: PC10<br>Alternate: SPI2_SCK, I2S2_CK, USART2_TX, UART3_TX, SDIO_D2, DCI_D8, EVENTOUT |
| PC11 | C10 | I/O | 5VT | Default: PC11<br>Alternate: I2S2_ADD_SD, SPI2_MISO, USART2_RX, UART3_RX, SDIO_D3, DCI_D4, EVENTOUT |
| PC12 | B10 | I/O | 5VT | Default: PC12<br>Alternate: I2C1_SDA, SPI2_MOSI, I2S2_SD, USART2_CK, UART4_TX, SDIO_CK, DCI_D9, EVENTOUT |
| PD0 | C9 | I/O | 5VT | Default: PD0<br>Alternate: SPI2_MOSI, I2S2_SD, CAN0_RX, EVENTOUT |
| PD1 | B9 | I/O | 5VT | Default: PD1<br>Alternate: SPI1_NSS, I2S1_WS, CAN0_TX, EVENTOUT |
| PD2 | C8 | I/O | 5VT | Default: PD2<br>Alternate: TIMER2_ETI, UART4_RX, SDIO_CMD, DCI_D11, EVENTOUT |



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| Pin Name | Pins | Pin Type(1) | I/O Level(2) | Functions description |
|---|---|---|---|---|
| PD3 | B8 | I/O | 5VT | Default: PD3<br>Alternate: TRACED1, SPI1_SCK, I2S1_CK, USART1_CTS, DCI_D5, EVENTOUT |
| PD4 | B7 | I/O | 5VT | Default: PD4<br>Alternate: USART1_RTS, EVENTOUT |
| PD5 | A6 | I/O | 5VT | Default: PD5<br>Alternate: USART1_TX, EVENTOUT |
| PD6 | B6 | I/O | 5VT | Default: PD6<br>Alternate: SPI2_MOSI, I2S2_SD, USART1_RX, DCI_D10, EVENTOUT |
| PD7 | A5 | I/O | 5VT | Default: PD7<br>Alternate: USART1_CK, EVENTOUT |
| PB3 | A8 | I/O | 5VT | Default: JTDO, PB3<br>Alternate: TRACESWO, TIMER1_CH1, SPI0_SCK, SPI2_SCK, I2S2_CK, USART0_RX, I2C1_SDA, EVENTOUT |
| PB4 | A7 | I/O | 5VT | Default: NJTRST, PB4<br>Alternate: TIMER2_CH0, SPI0_MISO, SPI2_MISO, I2S2_ADD_SD, I2C2_SDA, SDIO_D0, EVENTOUT, I2C0_TXFRAME |
| PB5 | C5 | I/O | 5VT | Default: PB5<br>Alternate: TIMER2_CH1, I2C0_SMBA, SPI0_MOSI, SPI2_MOSI, I2S2_SD, CAN1_RX, USBHS_ULPI_D7, DCI_D10, EVENTOUT |
| PB6 | B5 | I/O | 5VT | Default: PB6<br>Alternate: TIMER3_CH0, I2C0_SCL, USART0_TX, CAN1_TX, DCI_D5, EVENTOUT |
| PB7 | B4 | I/O | 5VT | Default: PB7<br>Alternate: TIMER3_CH1, I2C0_SDA, USART0_RX, DCI_VSYNC, EVENTOUT |
| BOOT0 | A4 | I/O | 5VT | Default: BOOT0 |
| PB8 | A3 | I/O | 5VT | Default: PB8<br>Alternate: TIMER1_CH0, TIMER1_ETI, TIMER3_CH2, TIMER9_CH0, I2C0_SCL, CAN0_RX, SDIO_D4, DCI_D6, EVENTOUT |
| PB9 | B3 | I/O | 5VT | Default: PB9<br>Alternate: TIMER1_CH1, TIMER3_CH3, TIMER10_CH0, I2C0_SDA, SPI1_NSS, I2S1_WS, CAN0_TX, SDIO_D5, DCI_D7, EVENTOUT |
| PE0 | C3 | I/O | 5VT | Default: PE0<br>Alternate: TIMER3_ETI, DCI_D2, EVENTOUT |
| PE1 | A2 | I/O | 5VT | Default: PE1<br>Alternate: TIMER0_CH1_ON, DCI_D3, EVENTOUT |



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| Pin Name | Pins | Pin Type(1) | I/O Level(2) | Functions description |
|---|---|---|---|---|
| $V_{SS}$ | D3 | P | - | Default: $V_{SS}$ |
| PDR_ON | H3 | P | - | Default: PDR_ON |
| $V_{DD}$ | C4 | P | - | Default: $V_{DD}$ |

**Notes:**

(1) Type: I = input, O = output, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

### 2.6.4. GD32F425Rx LQFP64 pin definitions

**Table 2-6. GD32F425Rx LQFP64 pin definitions**

| Pin Name | Pins | Pin Type(1) | I/O Level(2) | Functions description |
|---|---|---|---|---|
| $V_{BAT}$ | 1 | P | - | Default: $V_{BAT}$ |
| PC13-TAMPER-RTC | 2 | I/O | 5VT | Default: PC13<br>Alternate: EVENTOUT<br>Additional: RTC_TAMP0, RTC_OUT, RTC_TS |
| PC14-OSC32IN | 3 | I/O | 5VT | Default: PC14<br>Alternate: EVENTOUT<br>Additional: OSC32IN |
| PC15-OSC32OUT | 4 | I/O | 5VT | Default: PC15<br>Alternate: EVENTOUT<br>Additional: OSC32OUT |
| PH0 | 5 | I/O | 5VT | Default: PH0, OSCIN<br>Alternate: EVENTOUT<br>Additional: OSCIN |
| PH1 | 6 | I/O | 5VT | Default: PH1, OSCOUT<br>Alternate: EVENTOUT<br>Additional: OSCOUT |
| NRST | 7 | - | - | Default: NRST |
| PC0 | 8 | I/O | 5VT | Default: PC0<br>Alternate: USBHS_ULPI_STP, EVENTOUT<br>Additional: ADC012_IN10 |
| PC1 | 9 | I/O | 5VT | Default: PC1<br>Alternate: SPI2_MOSI, I2S2_SD, SPI1_MOSI, I2S1_SD, EVENTOUT<br>Additional: ADC012_IN11 |
| PC2 | 10 | I/O | 5VT | Default: PC2<br>Alternate: SPI1_MISO, I2S1_ADD_SD, USBHS_ULPI_DIR, EVENTOUT<br>Additional: ADC012_IN12 |
| PC3 | 11 | I/O | 5VT | Default: PC3 |



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| Pin Name | Pins | Pin Type(1) | I/O Level(2) | Functions description |
|---|---|---|---|---|
| | | | | Alternate: SPI1_MOSI, I2S1_SD, USBHS_ULPI_NXT, EVENTOUT<br>Additional: ADC012_IN13 |
| $V_{SSA}$ | 12 | P | - | Default: $V_{SSA}$ |
| $V_{DDA}$ | 13 | P | - | Default: $V_{DDA}$ |
| PA0-WKUP | 14 | I/O | 5VT | Default: PA0<br>Alternate: TIMER1_CH0, TIMER1_ETI, TIMER4_CH0, TIMER7_ETI, USART1_CTS, UART3_TX, EVENTOUT<br>Additional: ADC012_IN0, WKUP |
| PA1 | 15 | I/O | 5VT | Default: PA1<br>Alternate: TIMER1_CH1, TIMER4_CH1, USART1_RTS, UART3_RX, EVENTOUT<br>Additional: ADC012_IN1 |
| PA2 | 16 | I/O | 5VT | Default: PA2<br>Alternate: TIMER1_CH2, TIMER4_CH2, TIMER8_CH0, I2S_CKIN, USART1_TX, EVENTOUT<br>Additional: ADC012_IN2 |
| PA3 | 17 | I/O | 5VT | Default: PA3<br>Alternate: TIMER1_CH3, TIMER4_CH3, TIMER8_CH1, I2S1_MCK, USART1_RX, USBHS_ULPI_D0, EVENTOUT<br>Additional: ADC012_IN3 |
| $V_{SS}$ | 18 | P | - | Default: $V_{SS}$ |
| $V_{DD}$ | 19 | P | - | Default: $V_{DD}$ |
| PA4 | 20 | I/O | | Default: PA4<br>Alternate: SPI0_NSS, SPI2_NSS, I2S2_WS, USART1_CK, USBHS_SOF, DCI_HSYNC, EVENTOUT<br>Additional: ADC01_IN4, DAC_OUT0 |
| PA5 | 21 | I/O | | Default: PA5<br>Alternate: TIMER1_CH0, TIMER1_ETI, TIMER7_CH0_ON, SPI0_SCK, USBHS_ULPI_CK, EVENTOUT<br>Additional: ADC01_IN5, DAC_OUT1 |
| PA6 | 22 | I/O | 5VT | Default: PA6<br>Alternate: TIMER0_BRKIN, TIMER2_CH0, TIMER7_BRKIN, SPI0_MISO, I2S1_MCK, TIMER12_CH0, SDIO_CMD, DCI_PIXCLK, EVENTOUT<br>Additional: ADC01_IN6 |
| PA7 | 23 | I/O | 5VT | Default: PA7<br>Alternate: TIMER0_CH0_ON, TIMER2_CH1, TIMER7_CH0_ON, SPI0_MOSI, TIMER13_CH0, EVENTOUT<br>Additional: ADC01_IN7 |
| PC4 | 24 | I/O | 5VT | Default: PC4<br>Alternate: EVENTOUT |



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| Pin Name | Pins | Pin Type(1) | I/O Level(2) | Functions description |
|---|---|---|---|---|
| | | | | Additional: ADC01_IN14 |
| PC5 | 25 | I/O | 5VT | Default: PC5<br>Alternate: USART2_RX, EVENTOUT<br>Additional: ADC01_IN15 |
| PB0 | 26 | I/O | 5VT | Default: PB0<br>Alternate: TIMER0_CH1_ON, TIMER2_CH2, TIMER7_CH1_ON, SPI2_MOSI, I2S2_SD, USBHS_ULPI_D1, SDIO_D1, EVENTOUT<br>Additional: ADC01_IN8, IREF |
| PB1 | 27 | I/O | 5VT | Default: PB1<br>Alternate: TIMER0_CH2_ON, TIMER2_CH3, TIMER7_CH2_ON, USBHS_ULPI_D2, SDIO_D2, EVENTOUT<br>Additional: ADC01_IN9 |
| PB2 | 28 | I/O | 5VT | Default: PB2, BOOT1<br>Alternate: TIMER1_CH3, SPI2_MOSI, I2S2_SD, USBHS_ULPI_D4, SDIO_CK, EVENTOUT |
| PB10 | 29 | I/O | 5VT | Default: PB10<br>Alternate: TIMER1_CH2, I2C1_SCL, SPI1_SCK, I2S1_CK, I2S2_MCK, USART2_TX, USBHS_ULPI_D3, SDIO_D7, EVENTOUT |
| PB11 | 30 | I/O | 5VT | Default: PB11<br>Alternate: TIMER1_CH3, I2C1_SDA, I2S_CKIN, USART2_RX, USBHS_ULPI_D4, EVENTOUT |
| NC | 31 | - | - | - |
| $V_{DD}$ | 32 | P | - | Default: $V_{DD}$ |
| PB12 | 33 | I/O | 5VT | Default: PB12<br>Alternate: TIMER0_BRKIN, I2C1_SMBA, SPI1_NSS, I2S1_WS, USART2_CK, CAN1_RX, USBHS_ULPI_D5, USBHS_ID, EVENTOUT |
| PB13 | 34 | I/O | 5VT | Default: PB13<br>Alternate: TIMER0_CH0_ON, SPI1_SCK, I2S1_CK, USART2_CTS, CAN1_TX, USBHS_ULPI_D6, EVENTOUT, I2C1_TXFRAME<br>Additional: USBHS_VBUS |
| PB14 | 35 | I/O | 5VT | Default: PB14<br>Alternate: TIMER0_CH1_ON, TIMER7_CH1_ON, SPI1_MISO, I2S1_ADD_SD, USART2_RTS, TIMER11_CH0, USBHS_DM, EVENTOUT |
| PB15 | 36 | I/O | 5VT | Default: PB15<br>Alternate: RTC_REFIN, TIMER0_CH2_ON, TIMER7_CH2_ON, SPI1_MOSI, I2S1_SD, TIMER11_CH1, USBHS_DP, EVENTOUT |
| PC6 | 37 | I/O | 5VT | Default: PC6 |



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| Pin Name | Pins | Pin Type(1) | I/O Level(2) | Functions description |
|---|---|---|---|---|
| | | | | Alternate: TIMER2_CH0, TIMER7_CH0, I2S1_MCK, USART5_TX, SDIO_D6, DCI_D0, EVENTOUT |
| PC7 | 38 | I/O | 5VT | Default: PC7<br>Alternate: TIMER2_CH1, TIMER7_CH1, SPI1_SCK, I2S1_CK, I2S2_MCK, USART5_RX, SDIO_D7, DCI_D1, EVENTOUT |
| PC8 | 39 | I/O | 5VT | Default: PC8<br>Alternate: TRACED0, TIMER2_CH2, TIMER7_CH2, USART5_CK, SDIO_D0, DCI_D2, EVENTOUT |
| PC9 | 40 | I/O | 5VT | Default: PC9<br>Alternate: CK_OUT1, TIMER2_CH3, TIMER7_CH3, I2C2_SDA, I2S_CKIN, SDIO_D1, DCI_D3, EVENTOUT |
| PA8 | 41 | I/O | 5VT | Default: PA8<br>Alternate: CK_OUT0, TIMER0_CH0, I2C2_SCL, USART0_CK, USBFS_SOF, SDIO_D1, EVENTOUT, CTC_SYNC |
| PA9 | 42 | I/O | 5VT | Default: PA9<br>Alternate: TIMER0_CH1, I2C2_SMBA, SPI1_SCK, I2S1_CK, USART0_TX, SDIO_D2, DCI_D0, EVENTOUT<br>Additional: USBFS_VBUS |
| PA10 | 43 | I/O | 5VT | Default: PA10<br>Alternate: TIMER0_CH2, USART0_RX, USBFS_ID, DCI_D1, EVENTOUT, I2C2_TXFRAME |
| PA11 | 44 | I/O | 5VT | Default: PA11<br>Alternate: TIMER0_CH3, USART0_CTS, USART5_TX, CAN0_RX, USBFS_DM, EVENTOUT |
| PA12 | 45 | I/O | 5VT | Default: PA12<br>Alternate: TIMER0_ETI, USART0_RTS, USART5_RX, CAN0_TX, USBFS_DP, EVENTOUT |
| PA13 | 46 | I/O | 5VT | Default: JTMS, SWDIO, PA13<br>Alternate: EVENTOUT |
| NC | 47 | - | - | - |
| $V_{SS}$ | - | P | - | Default: $V_{SS}$ |
| $V_{DD}$ | 48 | P | - | Default: $V_{DD}$ |
| PA14 | 49 | I/O | 5VT | Default: JTCK, SWCLK, PA14<br>Alternate: EVENTOUT |
| PA15 | 50 | I/O | 5VT | Default: JTDI, PA15<br>Alternate: TIMER1_CH0, TIMER1_ETI, SPI0_NSS, SPI2_NSS, I2S2_WS, USART0_TX, EVENTOUT |
| PC10 | 51 | I/O | 5VT | Default: PC10<br>Alternate: SPI2_SCK, I2S2_CK, USART2_TX, UART3_TX, SDIO_D2, DCI_D8, EVENTOUT |
| PC11 | 52 | I/O | 5VT | Default: PC11<br>Alternate: I2S2_ADD_SD, SPI2_MISO, USART2_RX, |



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| Pin Name | Pins | Pin Type(1) | I/O Level(2) | Functions description |
|---|---|---|---|---|
| | | | | UART3_RX, SDIO_D3, DCI_D4, EVENTOUT |
| PC12 | 53 | I/O | 5VT | Default: PC12<br>Alternate: I2C1_SDA, SPI2_MOSI, I2S2_SD, USART2_CK, UART4_TX, SDIO_CK, DCI_D9, EVENTOUT |
| PD2 | 54 | I/O | 5VT | Default: PD2<br>Alternate: TIMER2_ETI, UART4_RX, SDIO_CMD, DCI_D11, EVENTOUT |
| PB3 | 55 | I/O | 5VT | Default: JTDO, PB3<br>Alternate: TRACESWO, TIMER1_CH1, SPI0_SCK, SPI2_SCK, I2S2_CK, USART0_RX, I2C1_SDA, EVENTOUT |
| PB4 | 56 | I/O | 5VT | Default: NJTRST, PB4<br>Alternate: TIMER2_CH0, SPI0_MISO, SPI2_MISO, I2S2_ADD_SD, I2C2_SDA, SDIO_D0, EVENTOUT, I2C0_TXFRAME |
| PB5 | 57 | I/O | 5VT | Default: PB5<br>Alternate: TIMER2_CH1, I2C0_SMBA, SPI0_MOSI, SPI2_MOSI, I2S2_SD, CAN1_RX, USBHS_ULPI_D7, DCI_D10, EVENTOUT |
| PB6 | 58 | I/O | 5VT | Default: PB6<br>Alternate: TIMER3_CH0, I2C0_SCL, USART0_TX, CAN1_TX, DCI_D5, EVENTOUT |
| PB7 | 59 | I/O | 5VT | Default: PB7<br>Alternate: TIMER3_CH1, I2C0_SDA, USART0_RX, DCI_VSYNC, EVENTOUT |
| BOOT0 | 60 | I/O | 5VT | Default: BOOT0 |
| PB8 | 61 | I/O | 5VT | Default: PB8<br>Alternate: TIMER1_CH0, TIMER1_ETI, TIMER3_CH2, TIMER9_CH0, I2C0_SCL, CAN0_RX, SDIO_D4, DCI_D6, EVENTOUT |
| PB9 | 62 | I/O | 5VT | Default: PB9<br>Alternate: TIMER1_CH1, TIMER3_CH3, TIMER10_CH0, I2C0_SDA, SPI1_NSS, I2S1_WS, CAN0_TX, SDIO_D5, DCI_D7, EVENTOUT |
| $V_{SS}$ | 63 | P | - | Default: $V_{SS}$ |
| $V_{DD}$ | 64 | P | - | Default: $V_{DD}$ |

**Notes:**

(1) Type: I = input, O = output, P = power.

(2) I/O Level: 5VT = 5 V tolerant.



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## 2.6.5. GD32F425xx pin alternate functions

**Table 2-7. Port A alternate functions summary**

| Pin Name | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **PA0** | | TIMER1_CH0/TIMER1_ETI | TIMER4_CH0 | TIMER7_ETI | | | | USART1_CTS | UART3_TX | | | | | | | EVENTOUT |
| **PA1** | | TIMER1_CH1 | TIMER4_CH1 | | | | | USART1_RTS | UART3_RX | | | | | | | EVENTOUT |
| **PA2** | | TIMER1_CH2 | TIMER4_CH2 | TIMER8_CH0 | | I2S_CKIN | | USART1_TX | | | | | | | | EVENTOUT |
| **PA3** | | TIMER1_CH3 | TIMER4_CH3 | TIMER8_CH1 | | I2S1_MCK | | USART1_RX | | | USBHS_ULPI_D0 | | | | | EVENTOUT |
| **PA4** | | | | | | SPI0_NSS | SPI2_NSS/I2S2_WS | USART1_CK | | | | | USBHS_SOF | DCI_HSYNC | | EVENTOUT |
| **PA5** | | TIMER1_CH0/TIMER1_ETI | | TIMER7_CH0_ON | | SPI0_SCK | | | | | USBHS_ULPI_CK | | | | | EVENTOUT |
| **PA6** | | TIMER0_BRKIN | TIMER2_CH0 | TIMER7_BRKIN | | SPI0_MISO | I2S1_MCK | | | TIMER12_CH0 | | | SDIO_CMD | DCI_PIXCLK | | EVENTOUT |
| **PA7** | | TIMER0_CH0_ON | TIMER2_CH1 | TIMER7_CH0_ON | | SPI0_MOSI | | | | TIMER13_CH0 | | | | | | EVENTOUT |
| **PA8** | CK_OUT0 | TIMER0_CH0 | | | I2C2_SCL | | | USART0_CK | | CTC_SYNC | USBFS_SOF | | SDIO_D1 | | | EVENTOUT |
| **PA9** | | TIMER0_CH1 | | | I2C2_SMBA | SPI1_SCK/I2S1_CK | | USART0_TX | | | | | SDIO_D2 | DCI_D0 | | EVENTOUT |
| **PA10** | | TIMER0_CH2 | | | I2C2_TXFRAME | | | USART0_RX | | | USBFS_ID | | | DCI_D1 | | EVENTOUT |
| **PA11** | | TIMER0_CH3 | | | | | | USART0_CTS | USART5_TX | CAN0_RX | USBFS_DM | | | | | EVENTOUT |
| **PA12** | | TIMER0_ETI | | | | | | USART0_RTS | USART5_RX | CAN0_TX | USBFS_DP | | | | | EVENTOUT |
| **PA13** | JTMS/SWDIO | | | | | | | | | | | | | | | EVENTOUT |
| **PA14** | JTCK/SWCLK | | | | | | | | | | | | | | | EVENTOUT |
| **PA15** | JTDI | TIMER1_CH0/TIMER1_ETI | | | | SPI0_NSS | SPI2_NSS/I2S2_WS | USART0_TX | | | | | | | | EVENTOUT |

**Table 2-8. Port B alternate functions summary**

| Pin Name | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **PB0** | | TIMER0_CH1_ON | TIMER2_CH2 | TIMER7_CH1_ON | | | | SPI2_MOSI/I2S2_SD | | | USBHS_ULPI_D1 | | SDIO_D1 | | | EVENTOUT |
| **PB1** | | TIMER0_CH2_ON | TIMER2_CH3 | TIMER7_CH2_ON | | | | | | | USBHS_ULPI_D2 | | SDIO_D2 | | | EVENTOUT |
| **PB2** | | TIMER1_CH3 | | | | | | SPI2_MOSI/I2S2_SD | | | USBHS_ULPI_D4 | | SDIO_CK | | | EVENTOUT |
| **PB3** | JTDO/TRACESWO | TIMER1_CH1 | | | | SPI0_SCK | SPI2_SCK/I2S2_CK | USART0_RX | | I2C1_SDA | | | | | | EVENTOUT |
| **PB4** | NJTRST | | TIMER2_CH0 | | I2C0_TXFRAME | SPI0_MISO | SPI2_MISO | I2S2_ADD_SD | | I2C2_SDA | | | SDIO_D0 | | | EVENTOUT |
| **PB5** | | | TIMER2_CH1 | | I2C0_SMBA | SPI0_MOSI | SPI2_MOSI/I2S2_SD | | | CAN1_RX | USBHS_ULPI_D7 | | | DCI_D10 | | EVENTOUT |
| **PB6** | | | TIMER3_CH0 | | I2C0_SCL | | | USART0_TX | | CAN1_TX | | | | DCI_D5 | | EVENTOUT |
| **PB7** | | | TIMER3_CH1 | | I2C0_SDA | | | USART0_RX | | | | | | DCI_VSYNC | | EVENTOUT |
| **PB8** | | TIMER1_CH0/TIMER1_ETI | TIMER3_CH2 | TIMER9_CH0 | I2C0_SCL | | | | | CAN0_RX | | | SDIO_D4 | DCI_D6 | | EVENTOUT |
| **PB9** | | TIMER1_CH1 | TIMER3_CH3 | TIMER10_CH0 | I2C0_SDA | SPI1_NSS/I2S1_WS | | | | CAN0_TX | | | SDIO_D5 | DCI_D7 | | EVENTOUT |
| **PB10** | | TIMER1_CH2 | | | I2C1_SCL | SPI1_SCK/I2S1_CK | I2S2_MCK | USART2_TX | | | USBHS_ULPI_D3 | | SDIO_D7 | | | EVENTOUT |
| **PB11** | | TIMER1_CH3 | | | I2C1_SDA | I2S_CKIN | | USART2_RX | | | USBHS_ULPI_D4 | | | | | EVENTOUT |
| **PB12** | | TIMER0_BRKIN | | | I2C1_SMBA | SPI1_NSS/I2S1_WS | | USART2_CK | | CAN1_RX | USBHS_ULPI_D5 | | USBHS_ID | | | EVENTOUT |
| **PB13** | | TIMER0_CH0_ON | | | I2C1_TXFRAME | SPI1_SCK/I2S1_CK | | USART2_CTS | | CAN1_TX | USBHS_ULPI_D6 | | | | | EVENTOUT |
| **PB14** | | TIMER0_CH1_ON | | TIMER7_CH1_ON | | SPI1_MISO | I2S1_ADD_SD | USART2_RTS | | TIMER11_CH0 | | | USBHS_DM | | | EVENTOUT |
| **PB15** | RTC_REFIN | TIMER0_CH2_ON | | TIMER7_CH2_ON | | SPI1_MOSI/I2S1_SD | | | | TIMER11_CH1 | | | USBHS_DP | | | EVENTOUT |

**Table 2-9. Port C alternate functions summary**

| Pin Name | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PC0 | | | | | | | | | | | USBHS_ULPI_STP | | | | | EVENTOUT |
| PC1 | | | | | | SPI2_MOSI/I2S2_SD | | SPI1_MOSI/I2S1_SD | | | | | | | | EVENTOUT |
| PC2 | | | | | | SPI1_MISO | I2S1_ADD_SD | | | | USBHS_ULPI_DIR | | | | | EVENTOUT |
| PC3 | | | | | | SPI1_MOSI/I2S1_SD | | | | | USBHS_ULPI_NXT | | | | | EVENTOUT |
| PC4 | | | | | | | | | | | | | | | | EVENTOUT |
| PC5 | | | | | | | | USART2_RX | | | | | | | | EVENTOUT |
| PC6 | | | TIMER2_CH0 | TIMER7_CH0 | | I2S1_MCK | | | USART5_TX | | | | SDIO_D6 | DCI_D0 | | EVENTOUT |
| PC7 | | | TIMER2_CH1 | TIMER7_CH1 | | SPI1_SCK/I2S1_CK | I2S2_MCK | | USART5_RX | | | | SDIO_D7 | DCI_D1 | | EVENTOUT |
| PC8 | TRACED0 | | TIMER2_CH2 | TIMER7_CH2 | | | | | USART5_CK | | | | SDIO_D0 | DCI_D2 | | EVENTOUT |
| PC9 | CK_OUT1 | | TIMER2_CH3 | TIMER7_CH3 | I2C2_SDA | I2S_CKIN | | | | | | | SDIO_D1 | DCI_D3 | | EVENTOUT |
| PC10 | | | | | | | SPI2_SCK/I2S2_CK | USART2_TX | UART3_TX | | | | SDIO_D2 | DCI_D8 | | EVENTOUT |
| PC11 | | | | | | I2S2_ADD_SD | SPI2_MISO | USART2_RX | UART3_RX | | | | SDIO_D3 | DCI_D4 | | EVENTOUT |
| PC12 | | | | | I2C1_SDA | | SPI2_MOSI/I2S2_SD | USART2_CK | UART4_TX | | | | SDIO_CK | DCI_D9 | | EVENTOUT |
| PC13 | | | | | | | | | | | | | | | | EVENTOUT |
| PC14 | | | | | | | | | | | | | | | | EVENTOUT |
| PC15 | | | | | | | | | | | | | | | | EVENTOUT |



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**Table 2-10. Port D alternate functions summary**

| Pin Name | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **PD0** | | | | | | | SPI2_MOSI/I2S2_SD | | | CAN0_RX | | | | | | EVENTOUT |
| **PD1** | | | | | | | | SPI1_NSS/I2S1_WS | | CAN0_TX | | | | | | EVENTOUT |
| **PD2** | | | TIMER2_ETI | | | | | | UART4_RX | | | | SDIO_CMD | DCI_D11 | | EVENTOUT |
| **PD3** | TRACED1 | | | | | SPI1_SCK/I2S1_CK | | USART1_CTS | | | | | | DCI_D5 | | EVENTOUT |
| **PD4** | | | | | | | | USART1_RTS | | | | | | | | EVENTOUT |
| **PD5** | | | | | | | | USART1_TX | | | | | | | | EVENTOUT |
| **PD6** | | | | | | SPI2_MOSI/I2S2_SD | | USART1_RX | | | | | | DCI_D10 | | EVENTOUT |
| **PD7** | | | | | | | | USART1_CK | | | | | | | | EVENTOUT |
| **PD8** | | | | | | | | USART2_TX | | | | | | | | EVENTOUT |
| **PD9** | | | | | | | | USART2_RX | | | | | | | | EVENTOUT |
| **PD10** | | | | | | | | USART2_CK | | | | | | | | EVENTOUT |
| **PD11** | | | | | | | | USART2_CTS | | | | | | | | EVENTOUT |
| **PD12** | | | TIMER3_CH0 | | | | | USART2_RTS | | | | | | | | EVENTOUT |
| **PD13** | | | TIMER3_CH1 | | | | | | | | | | | | | EVENTOUT |
| **PD14** | | | TIMER3_CH2 | | | | | | | | | | | | | EVENTOUT |
| **PD15** | CTC_SYNC | | TIMER3_CH3 | | | | | | | | | | | | | EVENTOUT |



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**Table 2-11. Port E alternate functions summary**

| Pin Name | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **PE0** | | | TIMER3_ETI | | | | | | | | | | | DCI_D2 | | EVENTOUT |
| **PE1** | | TIMER0_CH1_ON | | | | | | | | | | | | DCI_D3 | | EVENTOUT |
| **PE2** | TRACECK | | | | | | | | | | | | | | | EVENTOUT |
| **PE3** | TRACED0 | | | | | | | | | | | | | | | EVENTOUT |
| **PE4** | TRACED1 | | | | | | | | | | | | | DCI_D4 | | EVENTOUT |
| **PE5** | TRACED2 | | | TIMER8_CH0 | | | | | | | | | | DCI_D6 | | EVENTOUT |
| **PE6** | TRACED3 | | | TIMER8_CH1 | | | | | | | | | | DCI_D7 | | EVENTOUT |
| **PE7** | | TIMER0_ETI | | | | | | | | | | | | | | EVENTOUT |
| **PE8** | | TIMER0_CH0_ON | | | | | | | | | | | | | | EVENTOUT |
| **PE9** | | TIMER0_CH0 | | | | | | | | | | | | | | EVENTOUT |
| **PE10** | | TIMER0_CH1_ON | | | | | | | | | | | | | | EVENTOUT |
| **PE11** | | TIMER0_CH1 | | | | | | | | | | | | | | EVENTOUT |
| **PE12** | | TIMER0_CH2_ON | | | | | | | | | | | | | | EVENTOUT |
| **PE13** | | TIMER0_CH2 | | | | | | | | | | | | | | EVENTOUT |
| **PE14** | | TIMER0_CH3 | | | | | | | | | | | | | | EVENTOUT |
| **PE15** | | TIMER0_BRKIN | | | | | | | | | | | | | | EVENTOUT |



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**Table 2-12. Port F alternate functions summary**

| Pin Name | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PF0 | CTC_SYNC | | | | I2C1_SDA | | | | | | | | | | | EVENTOUT |
| PF1 | | | | | I2C1_SCL | | | | | | | | | | | EVENTOUT |
| PF2 | | | | | I2C1_SMBA | | | | | | | | | | | EVENTOUT |
| PF3 | | | | | I2C1_TXFRAME | | | | | | | | | | | EVENTOUT |
| PF4 | | | | | | | | | | | | | | | | EVENTOUT |
| PF5 | | | | | | | | | | | | | | | | EVENTOUT |
| PF6 | | | | TIMER9_CH0 | | | | | | | | | | | | EVENTOUT |
| PF7 | | | | TIMER10_CH0 | | | | | | | | | | | | EVENTOUT |
| PF8 | | | | | | | | | | TIMER12_CH0 | | | | | | EVENTOUT |
| PF9 | | | | | | | | | | TIMER13_CH0 | | | | | | EVENTOUT |
| PF10 | | | | | | | | | | | | | | DCI_D11 | | EVENTOUT |
| PF11 | | | | | | | | | | | | | | DCI_D12 | | EVENTOUT |
| PF12 | | | | | | | | | | | | | | | | EVENTOUT |
| PF13 | | | | | | | | | | | | | | | | EVENTOUT |
| PF14 | | | | | | | | | | | | | | | | EVENTOUT |
| PF15 | | | | | | | | | | | | | | | | EVENTOUT |

**Table 2-13. Port G alternate functions summary**

| Pin Name | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PG0 | | | | | | | | | | | | | | | | EVENTOUT |



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| Pin Name | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PG1 | | | | | | | | | | | | | | | | EVENTOUT |
| PG2 | | | | | | | | | | | | | | | | EVENTOUT |
| PG3 | | | | | | | | | | | | | | | | EVENTOUT |
| PG4 | | | | | | | | | | | | | | | | EVENTOUT |
| PG5 | | | | | | | | | | | | | | | | EVENTOUT |
| PG6 | | | | | | | | | | | | | | DCI_D12 | | EVENTOUT |
| PG7 | | | | | | | | | USART5_CK | | | | | DCI_D13 | | EVENTOUT |
| PG8 | | | | | | | | | USART5_RTS | | | | | | | EVENTOUT |
| PG9 | | | | | | | | | USART5_RX | | | | | DCI_VSYNC | | EVENTOUT |
| PG10 | | | | | | | | | | | | | | DCI_D2 | | EVENTOUT |
| PG11 | | | | | | | | | | | | | | DCI_D3 | | EVENTOUT |
| PG12 | | | | | | | | | USART5_RTS | | | | | | | EVENTOUT |
| PG13 | TRACED2 | | | | | | | | USART5_CTS | | | | | | | EVENTOUT |
| PG14 | TRACED3 | | | | | | | | USART5_TX | | | | | | | EVENTOUT |
| PG15 | | | | | | | | | USART5_CTS | | | | | DCI_D13 | | EVENTOUT |

**Table 2-14. Port H alternate functions summary**

| Pin Name | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PH0 | | | | | | | | | | | | | | | | EVENTOUT |
| PH1 | | | | | | | | | | | | | | | | EVENTOUT |



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# 3. Functional description

## 3.1. Arm® Cortex®-M4 core

The Arm® Cortex®-M4 processor is a high performance embedded processor with DSP instructions which allow efficient signal processing and complex algorithm execution. It brings an efficient, easy-to-use blend of control and signal processing capabilities to meet the digital signal control markets demand. The processor is highly configurable enabling a wide range of implementations from those requiring floating point operations, memory protection and powerful trace technology to cost sensitive devices requiring minimal area, while delivering outstanding computational performance and an advanced system response to interrupts.

32-bit Arm® Cortex®-M4 processor core

- Up to 200 MHz operation frequency
- Single-cycle multiplication and hardware divider
- Floating Point Unit (FPU)
- Integrated DSP instructions
- Integrated Nested Vectored Interrupt Controller (NVIC)
- 24-bit SysTick timer

The Cortex®-M4 processor is based on the Armv7-M architecture and supports both Thumb and Thumb-2 instruction sets. Some system peripherals listed below are also provided by Cortex®-M4:

- Internal Bus Matrix connected with ICode bus, DCode bus, system bus, Private Peripheral Bus (PPB) and debug accesses (AHB-AP)
- Nested Vectored Interrupt Controller (NVIC)
- Flash Patch and Breakpoint (FPB)
- Data Watchpoint and Trace (DWT)
- Instrument Trace Macrocell (ITM)
- Memory Protection Unit (MPU)
- Serial Wire JTAG Debug Port (SWJ-DP)
- Trace Port Interface Unit (TPIU)

## 3.2. On-chip memory

- Up to 3072 Kbytes of Flash memory, including code Flash and data Flash
- 256 KB of SRAM

The Arm® Cortex®-M4 processor is structured in Harvard architecture which can use separate buses to fetch instructions and load/store data. 3072 Kbytes of inner Flash at most, which includes code Flash and data Flash is available for storing programs and data, and accessed (R/W) at CPU clock speed with zero wait states. Up to 256 Kbytes of inner SRAM is composed

of SRAM0 (112KB), SRAM1 (16KB) and SRAM2 (64KB) that can be accessed at same time, and including 64 KB of TCM (tightly-coupled memory) data RAM that can be accessed only by the data bus of the Cortex®-M4 core. The additional 4KB of backup SRAM (BKP SRAM) is implemented in the backup domain, which can keep its content even when the $V_{DD}$ power supply is down. ***Table 2-2. GD32F425xx memory map*** shows the memory map of the GD32F425xx series of devices, including Flash, SRAM, peripheral, and other pre-defined regions.

## 3.3. Clock, reset and supply management

- Internal 16 MHz factory-trimmed RC and external 4 to 32 MHz crystal oscillator
- Internal 48 MHz RC oscillator
- Internal 32 KHz RC calibrated oscillator and external 32.768 KHz crystal oscillator
- Integrated system clock PLL
- 2.6 to 3.6 V application supply and I/Os
- Supply Supervisor: POR (Power On Reset), PDR (Power Down Reset), and low voltage detector (LVD)

The Clock Control Unit (CCU) provides a range of oscillator and clock functions. These include internal RC oscillator and external crystal oscillator, high speed and low speed two types. Several prescalers allow the frequency configuration of the AHB and two APB domains. The maximum frequency of the two AHB domains are 200 MHz. The maximum frequency of the two APB domains including APB1 is 50 MHz and APB2 is 100 MHz. See ***Figure 2-6. GD32F425xx clock tree*** for details on the clock tree.

The Reset Control Unit (RCU) controls three kinds of reset: system reset resets the processor core and peripheral IP components. Power-on reset (POR) and power-down reset (PDR) are always active, and ensures proper operation starting from 2.4 V and down to 1.8V. The device remains in reset mode when $V_{DD}$ is below a specified threshold. The embedded low voltage detector (LVD) monitors the power supply, compares it to the voltage threshold and generates an interrupt as a warning message for leading the MCU into security.

Power supply schemes:

- $V_{DD}$ range: 2.6 to 3.6 V, external power supply for I/Os and the internal regulator. Provided externally through $V_{DD}$ pins.
- $V_{SSA}$, $V_{DDA}$ range: 2.6 to 3.6 V, external analog power supplies for ADC, reset blocks, RCs and PLL. $V_{DDA}$ and $V_{SSA}$ must be connected to $V_{DD}$ and $V_{SS}$, respectively.
- $V_{BAT}$ range: 1.8 to 3.6 V, power supply for RTC, external clock 32 KHz oscillator and backup registers (through power switch) when $V_{DD}$ is not present.

## 3.4. Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from main Flash memory (default)



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- Boot from system memory
- Boot from on-chip SRAM

The boot loader is located in the internal 30KB of information blocks for the boot ROM memory (system memory). It is used to reprogram the Flash memory by using USART0 (PA9 and PA10), USART2 (PB10 and PB11, or PC10 and PC11), and USBFS (PA9, PA10, PA11 and PA12) in device mode. It also can be used to transfer and update the Flash memory code, the data and the vector table sections. In default condition, boot from bank0 of Flash memory is selected. It also supports to boot from bank1 of Flash memory by setting a bit in option bytes.

## 3.5. Power saving modes

The MCU supports three kinds of power saving modes to achieve even lower power consumption. They are sleep mode, deep-sleep mode, and standby mode. These operating modes reduce the power consumption and allow the application to achieve the best balance between the CPU operating time, speed and power consumption.

- **Sleep** mode
  In sleep mode, only the clock of CPU core is off. All peripherals continue to operate and any interrupt/event can wake up the system.
- **Deep-sleep** mode
  In deep-sleep mode, all clocks in the 1.2V domain are off, and all of the high speed crystal oscillator (IRC16M, HXTAL) and PLL are disabled. Only the contents of SRAM and registers are retained. Any interrupt or wakeup event from EXTI lines can wake up the system from the deep-sleep mode including the 16 external lines, the RTC alarm, RTC Tamper and TimeStamp event, the LVD output, RTC wakeup and USB wakeup. When exiting the deep-sleep mode, the IRC16M is selected as the system clock.
- **Standby** mode
  In standby mode, the whole 1.2V domain is power off, the LDO is shut down, and all of IRC16M, HXTAL and PLL are disabled. The contents of SRAM and registers (except backup registers) are lost. There are four wakeup sources for the standby mode, including the external reset from NRST pin, the RTC, the FWDGT reset, and the rising edge on WKUP pin.

## 3.6. Analog to digital converter (ADC)

- 12-bit SAR ADC's conversion rate is up to 2.6 MSPS
- 12-bit, 10-bit, 8-bit or 6-bit configurable resolution
- Hardware oversampling ratio adjustable from 2x to 256x improves resolution to 16-bit
- Input voltage range: $V_{SSA}$ to $V_{DDA}$ (2.6V ≤ $V_{DDA}$ ≤ 3.6V)
- Temperature sensor

Up to three 12-bit 2.6 MSPS multi-channel ADCs are integrated in the device. It has a total of



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19 multiplexed channels: 16 external channels, 1 channel for internal temperature sensor ($V_{SENSE}$), 1 channel for internal reference voltage ($V_{REFINT}$) and 1 channel for external battery power supply ($V_{BAT}$). The input voltage range is between 2.6 V and 3.6 V. An on-chip hardware oversampling scheme improves performance while off-loading the related computational burden from the CPU. An analog watchdog block can be used to detect the channels, which are required to remain within a specific threshold window. A configurable channel management block can be used to perform conversions in single, continuous, scan or discontinuous mode to support more advanced use.

The ADC can be triggered from the events generated by the general level 0 timers (TIMERx) and the advanced-control timers (TIMER0 and TIMER7) with internal connection. The temperature sensor can be used to generate a voltage that varies linearly with temperature. It is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage in a digital value.

## 3.7. Digital to analog converter (DAC)

- Two 12-bit DAC converter of independent output channel
- 8-bit or 12-bit mode in conjunction with the DMA controller

The 12-bit buffered DAC channel is used to generate variable analog outputs. The DACs are designed with integrated resistor strings structure. The DAC channels can be triggered by the timer update outputs or EXTI with DMA support. The maximum output value of the DAC is $V_{REF+}$.

## 3.8. DMA

- 16 channels DMA controller and each channel are configurable (8 for DMA0 and 8 for DMA1)
- Support independent 8, 16, 32-bit memory and peripheral transfer
- Peripherals supported: Timers, ADC, SPIs, I2Cs, USARTs, UARTs, DAC, I2S, SDIO and DCI

The flexible general-purpose DMA controllers provide a hardware method of transferring data between peripherals and/or memory without intervention from the CPU, thereby freeing up bandwidth for other system functions. Three types of access method are supported: peripheral to memory, memory to peripheral, memory to memory.

Each channel is connected to fixed hardware DMA requests. The priorities of DMA channel requests are determined by software configuration and hardware channel number. Transfer size of source and destination are independent and configurable.



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## 3.9. General-purpose inputs/outputs (GPIOs)

- Up to 114 fast GPIOs, all mappable on 16 external interrupt lines
- Analog input/output configurable
- Alternate function input/output configurable

There are up to 114 general purpose I/O pins (GPIO) in GD32F425xx, named PA0 ~ PA15, PB0 ~ PB15, PC0 ~ PC15, PD0 ~ PD15, PE0 ~ PE15, PF0 ~ PF15, PG0 ~ PG15 and PH0 ~ PH1 to implement logic input/output functions. Each of the GPIO ports has related control and configuration registers to satisfy the requirements of specific applications. The external interrupts on the GPIO pins of the device have related control and configuration registers in the Interrupt/event controller (EXTI). The GPIO ports are pin-shared with other alternative functions (AFs) to obtain maximum flexibility on the package pins. Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current capable except for analog inputs.

## 3.10. Timers and PWM generation

- Two 16-bit advanced-control timer (TIMER0 & TIMER7), eight 16-bit general timers (TIMER2, TIMER3, TIMER8 ~ TIMER13), two 32-bit general timers (TIMER1 & TIMER4) and two 16-bit basic timer (TIMER5 & TIMER6)
- Up to 4 independent channels of PWM, output compare or input capture for each general timer and external trigger input
- 16-bit, motor control PWM advanced-control timer with programmable dead-time generation for output match
- Encoder interface controller with two inputs using quadrature decoder
- 24-bit SysTick timer down counter
- 2 watchdog timers (free watchdog timer and window watchdog timer)

The advanced-control timer (TIMER0 & TIMER7) can be used as a three-phase PWM multiplexed on 6 channels. It has complementary PWM outputs with programmable dead-time generation. It can also be used as a complete general timer. The 4 independent channels can be used for input capture, output compare, PWM generation (edge- or center-aligned counting modes) and single pulse mode output. If configured as a general 16-bit timer, it has the same functions as the TIMERx timer. It can be synchronized with external signals or to interconnect with other general timers together which have the same architecture and features.

The general timer, can be used for a variety of purposes including general time, input signal pulse width measurement or output waveform generation such as a single pulse generation or PWM output, up to 4 independent channels for input capture/output compare. TIMER1 & TIMER4 is based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler. TIMER2 &



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TIMER3 is based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. TIMER8 ~ TIMER13 is based on a 16-bit auto-reload upcounter and a 16-bit prescaler. The general timer also supports an encoder interface with two inputs using quadrature decoder.

The basic timer, known as TIMER5 & TIMER6, are mainly used for DAC trigger generation. They can also be used as a simple 16-bit time base.

The GD32F425xx have two watchdog peripherals, free watchdog timer and window watchdog timer. They offer a combination of high safety level, flexibility of use and timing accuracy.

The free watchdog timer includes a 12-bit down-counting counter and an 8-bit prescaler. It is clocked from an independent 32 KHz internal RC and as it operates independently of the main clock, it can operate in deep-sleep and standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management.

The window watchdog timer is based on a 7-bit down counter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early wakeup interrupt capability and the counter can be frozen in debug mode.

The SysTick timer is dedicated for OS, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Auto reload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

## 3.11. Real time clock (RTC) and backup registers

- Independent binary-coded decimal (BCD) format timer/counter with twenty 32-bit backup registers.
- Calendar with sub-second, seconds, minutes, hours, week day, date, year and month automatically correction.
- Alarm function with wake up from deep-sleep and standby mode capability.
- On-the-fly correction for synchronization with master clock. Digital calibration with 1 ppm resolution for compensation of quartz crystal inaccuracy.

The real time clock is an independent timer which provides a set of continuously running counters in backup registers to provide a real calendar function, and provides an alarm interrupt or an expected interrupt. It is not reset by a system or power reset, or when the device wakes up from standby mode. A prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 KHz from external crystal oscillator.



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## 3.12. Inter-integrated circuit (I2C)

- Up to three I2C bus interfaces can support both master and slave mode with a frequency up to 400 KHz (Fast mode).
- Provide arbitration function, optional PEC (packet error checking) generation and checking.
- Supports 7-bit and 10-bit addressing mode and general call addressing mode.

The I2C interface is an internal circuit allowing communication with an external I2C interface which is an industry standard two line serial interface used for connection to external hardware. These two serial lines are known as a serial data line (SDA) and a serial clock line (SCL). The I2C module provides two data transfer rates: 100 KHz of standard mode or 400 KHz of the fast mode. The I2C module also has an arbitration detect function to prevent the situation where more than one master attempts to transmit data to the I2C bus at the same time. A CRC-8 calculator is also provided in I2C interface to perform packet error checking for I2C data.

## 3.13. Serial peripheral interface (SPI)

- Up to three SPI interfaces with a frequency of up to 30 MHz
- Support both master and slave mode
- Hardware CRC calculation and transmit automatic CRC error checking

The SPI interface uses 4 pins, among which are the serial data input and output lines (MISO & MOSI), the clock line (SCK) and the slave select line (NSS). Both SPIs can be served by the DMA controller. The SPI interface may be used for a variety of purposes, including simplex synchronous transfers on two lines with a possible bidirectional data line or reliable communication using CRC checking.

## 3.14. Universal synchronous/asynchronous receiver transmitter (USART/UART)

- Up to four USARTs and two UARTs with operating frequency up to 12.5 MHz
- Supports both asynchronous and clocked synchronous serial communication modes
- IrDA SIR encoder and decoder support
- LIN break generation and detection
- ISO 7816-3 compliant smart card interface

The USART (USART0, USART1, USART2, USART5) and UART (UART3, UART4) are used to transfer data between parallel and serial interfaces, provides a flexible full duplex data exchange using synchronous or asynchronous transfer. It is also commonly used for RS-232 standard communication. The USART/UART includes a programmable baud rate generator



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which is capable of dividing the system clock to produce a dedicated clock for the USART/UART transmitter and receiver. The USART/UART also supports DMA function for high speed data communication.

## 3.15. Inter-IC sound (I2S)

- Two I2S bus Interfaces with sampling frequency from 8 KHz to 192 KHz, multiplexed with SPI1 and SPI2
- Support either master or slave mode Audio
- Sampling frequencies from 8 KHz up to 192 KHz are supported

The Inter-IC sound (I2S) bus provides a standard communication interface for digital audio applications by 4-wire serial lines. GD32F425xx contain an I2S-bus interface that can be operated with 16/32 bit resolution in master or slave mode, pin multiplexed with SPI1 and SPI2. The audio sampling frequencies from 8 KHz to 192 KHz is supported.

## 3.16. Universal serial bus full-speed interface (USBFS)

- One USB device/host/OTG full-speed Interface with frequency up to 12 Mbit/s
- Internal 48 MHz oscillator support crystal-less operation
- Internal main PLL for USB CLK compliantly
- Internal USBFS PHY support

The Universal Serial Bus (USB) is a 4-wire bus with 4 bidirectional endpoints. The device controller enables 12 Mbit/s data exchange with integrated transceivers. Transaction formatting is performed by the hardware, including CRC generation and checking. It supports both host and device modes, as well as OTG mode with Host Negotiation Protocol (HNP) and Session Request Protocol (SRP). The controller contains a full-speed USB PHY internal. For full-speed or low-speed operation, no more external PHY chip is needed. It supports all the four types of transfer (control, bulk, Interrupt and isochronous) defined in USB 2.0 protocol. The required precise 48 MHz clock which can be generated from the internal main PLL (the clock source must use an HXTAL crystal oscillator) or by the internal 48 MHz oscillator in automatic trimming mode that allows crystal-less operation.

## 3.17. Universal serial bus high-speed interface (USBHS)

- One USB device/host/OTG high-speed Interface with frequency up to 480 Mbit/s
- An external PHY device connected to the ULPI is required when using in HS mode

USBHS supports both host and device modes, as well as OTG mode with Host Negotiation Protocol (HNP) and Session Request Protocol (SRP). The controller provides ULPI interface for external USB PHY integration and it also contains a full-speed USB PHY internal. For full-speed or low-speed operation, no more external PHY chip is needed. It supports all the four



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types of transfer (control, bulk, Interrupt and isochronous) defined in USB 2.0 protocol. HUB connection is supported when USBHS operates at high-speed in host mode. There is also a DMA engine operating as an AHB bus master in USBHS to speed up the data transfer between USBHS and system.

## 3.18. Controller area network (CAN)

- Two CAN2.0B interface with communication frequency up to 1 Mbit/s
- Internal main PLL for CAN CLK compliantly

Controller area network (CAN) is a method for enabling serial communication in field bus. The CAN protocol has been used extensively in industrial automation and automotive applications. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. Each CAN has three mailboxes for transmission and two FIFOs of three message deep for reception. It also provides 28 scalable/configurable identifier filter banks for selecting the incoming messages needed and discarding the others.

## 3.19. Secure digital input and output card interface (SDIO)

- Support SD2.0/SDIO2.0/MMC4.2 host interface

The Secure Digital Input and Output Card Interface (SDIO) provides access to external SD memory cards specifications version 2.0, SDIO card specification version 2.0 and multi-media card system specification version 4.2 with DMA supported. In addition, this interface is also compliant with CE-ATA digital protocol rev1.1.

## 3.20. Digital camera interface (DCI)

- Digital video/picture capture
- 8/10/12/14 data width supported
- High transfer efficiency with DMA interface
- Video/picture crop supported
- Various pixel formats supported including JPEG/YCrCb/RGB
- Hard/embedded synchronous signals supported

DCI is an 8-bit to 14-bit parallel interface that able to capture video or picture from a camera via Digital Camera Interface. It supports 8/10/12/14 bits data width through DMA operation.

## 3.21. Debug mode

- Serial wire JTAG debug port (SWJ-DP)

The Arm® SWJ-DP Interface is embedded and is a combined JTAG and serial wire debug



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port that enables either a serial wire debug or a JTAG probe to be connected to the target.

## 3.22. Package and operation temperature

- BGA100 (GDF425VxH), LQFP144 (GD32F425Zx), LQFP100 (GD32F425VxT) and LQFP64 (GD32F425Rx)
- Operation temperature range: -40°C to +85°C (industrial level)



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# 4. Electrical characteristics

## 4.1. Absolute maximum ratings

The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

**Table 4-1. Absolute maximum ratings(1)(4)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{DD}$ | External voltage range(2) | $V_{SS}$ - 0.3 | $V_{SS}$ + 3.6 | V |
| $V_{DDA}$ | External analog supply voltage | $V_{SSA}$ - 0.3 | $V_{SSA}$ + 3.6 | V |
| $V_{BAT}$ | External battery supply voltage | $V_{SS}$ - 0.3 | $V_{SS}$ + 3.6 | V |
| $V_{IN}$ | Input voltage on 5V tolerant pin(3) | $V_{SS}$ - 0.3 | $V_{DD}$ + 3.6 | V |
| | Input voltage on other I/O | $V_{SS}$ - 0.3 | 3.6 | V |
| $\|\Delta V_{DDX}\|$ | Variations between different $V_{DD}$ power pins | — | 50 | mV |
| $\|V_{SSX} - V_{SS}\|$ | Variations between different ground pins | — | 50 | mV |
| $I_{IO}$ | Maximum current for GPIO pins | — | 25 | mA |
| $T_A$ | Operating temperature range | -40 | +85 | °C |
| $P_D$ | Power dissipation at $T_A$ = 85°C of LQFP144 | — | 820 | mW |
| | Power dissipation at $T_A$ = 85°C of BGA100 | — | 511 | |
| | Power dissipation at $T_A$ = 85°C of LQFP100 | — | 697 | |
| | Power dissipation at $T_A$ = 85°C of LQFP64 | — | 772 | |
| $T_{STG}$ | Storage temperature range | -65 | +150 | °C |
| $T_J$ | Maximum junction temperature | — | 125 | °C |

(1) Guaranteed by design, not tested in production.
(2) All main power and ground pins should be connected to an external power source within the allowable range.
(3) $V_{IN}$ maximum value cannot exceed 5.5 V.
(4) It is recommended that $V_{DD}$ and $V_{DDA}$ are powered by the same source. The maximum difference between $V_{DD}$ and $V_{DDA}$ does not exceed 300 mV during power-up and operation.

## 4.2. Operating conditions characteristics

**Table 4-2. DC operating conditions**

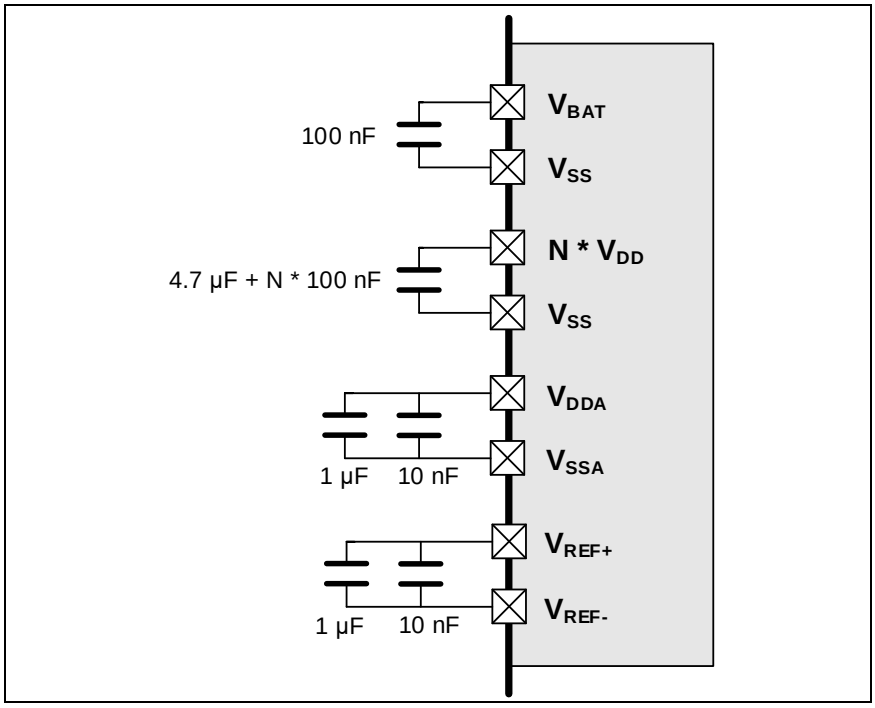
| Symbol | Parameter | Conditions | Min(1) | Typ | Max(1) | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | — | 2.6 | 3.3 | 3.6 | V |
| $V_{DDA}$ | Analog supply voltage | Same as $V_{DD}$ | 2.6 | 3.3 | 3.6 | V |
| $V_{BAT}$ | Battery supply voltage | — | 1.8 | — | 3.6 | V |

(1) Based on characterization, not tested in production.



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**Figure 4-1. Recommended power supply decoupling capacitors(1) (2)**




(1) The $V_{REF+}$ and $V_{REF-}$ pins are only available on no less than 100-pin packages, or else the $V_{REF+}$ and $V_{REF-}$ pins are not available and internally connected to $V_{DDA}$ and $V_{SSA}$ pins.

(2) All decoupling capacitors need to be as close as possible to the pins on the PCB board.

**Table 4-3. Clock frequency(1)**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $f_{HCLK}$ | AHB clock frequency | — | — | 200 | MHz |
| $f_{APB1}$ | APB1 clock frequency | — | — | 50 | MHz |
| $f_{APB2}$ | APB2 clock frequency | — | — | 100 | MHz |

(1) Guaranteed by design, not tested in production.

**Table 4-4. Operating conditions at Power up / Power down(1)**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $t_{VDD}$ | $V_{DD}$ rise time rate | — | 0 | ∞ | µs/ V |
| | $V_{DD}$ fall time rate | | 20 | ∞ | |

(1) Guaranteed by design, not tested in production.

**Table 4-5. Start-up timings of Operating conditions(1)(2)(3)**

| Symbol | Parameter | Conditions | Typ | Unit |
|---|---|---|---|---|
| $t_{start-up}$ | Start-up time | Clock source from HXTAL | 140.6 | ms |
| | | Clock source from IRC16M | 140.2 | |

(1) Based on characterization, not tested in production.

(2) After power-up, the start-up time is the time between the rising edge of NRST high and the main function.

(3) PLL is off.



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**Table 4-6. Power saving mode wakeup timings characteristics(1)(2)**

| Symbol | Parameter | Typ | Unit |
|---|---|---|---|
| $t_{Sleep}$ | Wakeup from Sleep mode | 0.623 | μs |
| $t_{Deep-sleep}$ | Wakeup from Deep-sleep mode（LDO On） | 1.57 | |
| | Wakeup from Deep-sleep mode（LDO in low power mode） | 1.57 | |
| $t_{Standby}$ | Wakeup from Standby mode | 140 | ms |

(1) Based on characterization, not tested in production.

(2) The wakeup time is measured from the wakeup event to the point at which the application code reads the first instruction under the below conditions: $V_{DD}$ = $V_{DDA}$ = 3.3 V, IRC16M = System clock = 16 MHz.

## 4.3. Power consumption

The power measurements specified in the tables represent that code with data executing from on-chip Flash with the following specifications.

**Table 4-7. Power consumption characteristics(2)(3)(4)(5)**

| Symbol | Parameter | Conditions | Min | Typ(1) | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{DD}$+$I_{DDA}$ | Supply current (Run mode) | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System clock = 200 MHz, All peripherals enabled | — | 61.5 | — | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System clock = 200 MHz, All peripherals disabled | — | 37.1 | — | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System clock = 180 MHz, All peripherals enabled | — | 55.9 | — | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System clock = 180 MHz, All peripherals disabled | — | 33.9 | — | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System clock = 168 MHz, All peripherals enabled | — | 52.6 | — | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System clock = 168 MHz, All peripherals disabled | — | 32.0 | — | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System clock = 120 MHz, All peripherals enabled | — | 38.6 | — | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System clock = 120 MHz, All peripherals disabled | — | 23.9 | — | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System clock = 108 MHz, All peripherals enabled | — | 35.2 | — | mA |



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| Symbol | Parameter | Conditions | Min | Typ(1) | Max | Unit |
|---|---|---|---|---|---|---|
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System clock = 108 MHz, All peripherals disabled | — | 22.0 | — | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System clock = 90 MHz, All peripherals enabled | — | 29.9 | — | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System clock = 90 MHz, All peripherals disabled | — | 19.0 | — | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System clock = 60 MHz, All peripherals enabled | — | 21.2 | — | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System clock = 60 MHz, All peripherals disabled | — | 13.9 | — | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System clock = 30 MHz, All peripherals enabled | — | 13.3 | — | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System clock = 30 MHz, All peripherals disabled | — | 9.5 | — | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System clock = 25 MHz, All peripherals enabled | — | 11.7 | — | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System clock = 25 MHz, All peripherals disabled | — | 8.5 | — | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System clock = 16 MHz, All peripherals enabled | — | 8.9 | — | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System clock = 16 MHz, All peripherals disabled | — | 6.9 | — | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System clock = 8 MHz, All peripherals enabled | — | 6.4 | — | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System clock = 8 MHz, All peripherals disabled | — | 5.3 | — | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System clock = 4 MHz, All peripherals enabled | — | 5.0 | — | mA |



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| Symbol | Parameter | Conditions | Min | Typ(1) | Max | Unit |
|---|---|---|---|---|---|---|
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System clock = 4 MHz, All peripherals disabled | — | 4.5 | — | mA |
| | Supply current (Sleep mode) | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System clock = 200 MHz,CPU clock off, All peripherals enabled | — | 42.2 | — | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System clock = 200 MHz, CPU clock off, All peripherals disabled | — | 18.7 | — | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System clock = 180 MHz, CPU clock off, All peripherals enabled | — | 38.5 | — | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System clock = 180 MHz, CPU clock off, All peripherals disabled | — | 17.2 | — | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System clock = 168 MHz, CPU clock off, All peripherals enabled | | 36.2 | | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System clock = 168 MHz, CPU clock off, All peripherals disabled | | 16.4 | | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System clock = 120 MHz, CPU clock off, All peripherals enabled | — | 27.0 | — | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System clock = 120 MHz, CPU clock off, All peripherals disabled | — | 12.8 | — | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System clock = 108 MHz, CPU clock off, All peripherals enabled | — | 24.7 | — | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System clock = 108 MHz, CPU clock off, All peripherals disabled | — | 11.9 | — | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System clock = 90 MHz, CPU clock off, All peripherals enabled | — | 21.2 | — | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System clock = 90 MHz, CPU clock off, All peripherals disabled | — | 10.5 | — | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System clock = 60 MHz, CPU clock off, All peripherals enabled | — | 15.5 | — | mA |



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| Symbol | Parameter | Conditions | Min | Typ(1) | Max | Unit |
|---|---|---|---|---|---|---|
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System clock = 60 MHz, CPU clock off, All peripherals disabled | — | 8.4 | — | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System clock = 30 MHz, CPU clock off, All peripherals enabled | — | 10.5 | — | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System clock = 30 MHz, CPU clock off, All peripherals disabled | — | 6.7 | — | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System clock = 25 MHz, CPU clock off, All peripherals enabled | — | 9.4 | — | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System clock = 25 MHz, CPU clock off, All peripherals disabled | — | 6.2 | — | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System clock = 16 MHz, CPU clock off, All peripherals enabled | — | 7.4 | — | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System clock = 16 MHz, CPU clock off, All peripherals disabled | — | 5.4 | — | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System clock = 8 MHz, CPU clock off, All peripherals enabled | — | 5.7 | — | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System clock = 8 MHz, CPU clock off, All peripherals disabled | — | 4.7 | — | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System clock = 4 MHz, CPU clock off, All peripherals enabled | — | 4.8 | — | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System clock = 4 MHz, CPU clock off, All peripherals disabled | — | 4.3 | — | mA |
| | Supply current (Deep-Sleep mode) | $V_{DD}$ = $V_{DDA}$ = 3.3 V, LDO in run mode and normal driver mode, IRC32K off, RTC off, All GPIOs analog mode | — | 1.39 | — | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, LDO in low power mode and normal driver mode, IRC32K off, RTC off, All GPIOs analog mode | — | 1.36 | 11 | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, LDO in run mode and low driver mode, IRC32K off, RTC off, All GPIOs analog mode | — | 1.33 | — | mA |



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| Symbol | Parameter | Conditions | Min | Typ(1) | Max | Unit |
|---|---|---|---|---|---|---|
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, LDO in low power mode and low driver mode, IRC32K off, RTC off, All GPIOs analog mode | — | 1.30 | — | mA |
| | Supply current (Standby mode) | $V_{DD}$ = $V_{DDA}$ = 3.3 V, LXTAL off, IRC32K on, RTC on, backup SARM LDO ON | — | 9.90 | — | µA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, LXTAL off, IRC32K on, RTC off, backup SARM LDO ON | — | 9.67 | — | µA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, LXTAL off, IRC32K off, RTC off, backup SARM LDO ON | — | 9.19 | — | µA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, LXTAL off, IRC32K off, RTC off, backup SARM LDO OFF | — | 3.26 | — | µA |
| $I_{BAT}$ | Battery supply current (Backup mode) | $V_{DD}$ off, $V_{DDA}$ off, $V_{BAT}$=3.6V, LXTAL on with external crystal, RTC on, LXTAL High driving, backup SARM LDO ON | — | 9.09 | — | µA |
| | | $V_{DD}$ off, $V_{DDA}$ off, $V_{BAT}$=3.3V, LXTAL on with external crystal, RTC on, LXTAL High driving, backup SARM LDO ON | — | 8.93 | — | µA |
| | | $V_{DD}$ off, $V_{DDA}$ off, $V_{BAT}$=2.6V, LXTAL on with external crystal, RTC on, LXTAL High driving, backup SARM LDO ON | — | 8.74 | — | µA |
| | | $V_{DD}$ off, $V_{DDA}$ off, $V_{BAT}$=1.8V, LXTAL on with external crystal, RTC on, LXTAL High driving, backup SARM LDO ON | — | 7.47 | — | µA |
| | | $V_{DD}$ off, $V_{DDA}$ off, $V_{BAT}$ =3.6V, LXTAL on with external crystal, RTC on, LXTAL High driving, backup SARM LDO OFF | — | 2.23 | — | µA |
| | | $V_{DD}$ off, $V_{DDA}$ off, $V_{BAT}$ =3.3V, LXTAL on with external crystal, RTC on, LXTAL High driving, backup SARM LDO OFF | — | 2.13 | — | µA |
| | | $V_{DD}$ off, $V_{DDA}$ off, $V_{BAT}$ =2.6V, LXTAL on with external crystal, RTC on, LXTAL High driving, backup SARM LDO OFF | — | 2 | — | µA |
| | | $V_{DD}$ off, $V_{DDA}$ off, $V_{BAT}$ =1.8V, LXTAL on with external crystal, RTC on, LXTAL High driving, backup SARM LDO OFF | — | 1.89 | — | µA |
| | | $V_{DD}$ off, $V_{DDA}$ off, $V_{BAT}$ =3.6V, LXTAL on with external crystal, RTC on, LXTAL Low driving, backup SARM LDO ON | — | 8.16 | — | µA |
| | | $V_{DD}$ off, $V_{DDA}$ off, $V_{BAT}$ =3.3V, LXTAL on with external crystal, RTC on, LXTAL Low driving, backup SARM LDO ON | — | 8 | — | µA |



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| Symbol | Parameter | Conditions | Min | Typ(1) | Max | Unit |
|---|---|---|---|---|---|---|
| | | $V_{DD}$ off, $V_{DDA}$ off, $V_{BAT}$ =2.6V, LXTAL on with external crystal, RTC on, LXTAL Low driving, backup SARM LDO ON | — | 7.8 | — | μA |
| | | $V_{DD}$ off, $V_{DDA}$ off, $V_{BAT}$ =1.8V, LXTAL on with external crystal, RTC on, LXTAL Low driving, backup SARM LDO ON | — | 6.7 | — | μA |
| | | $V_{DD}$ off, $V_{DDA}$ off, $V_{BAT}$ =3.6V, LXTAL on with external crystal, RTC on, LXTAL Low driving, backup SARM LDO OFF | — | 1.27 | — | μA |
| | | $V_{DD}$ off, $V_{DDA}$ off, $V_{BAT}$ =3.3V, LXTAL on with external crystal, RTC on, LXTAL Low driving, backup SARM LDO OFF | — | 1.18 | — | μA |
| | | $V_{DD}$ off, $V_{DDA}$ off, $V_{BAT}$ =2.6V, LXTAL on with external crystal, RTC on, LXTAL Low driving, backup SARM LDO OFF | — | 1.06 | — | μA |
| | | $V_{DD}$ off, $V_{DDA}$ off, $V_{BAT}$ =1.8V, LXTAL on with external crystal, RTC on, LXTAL Low driving, backup SARM LDO OFF | — | 0.96 | — | μA |

(1) Based on characterization, not tested in production.

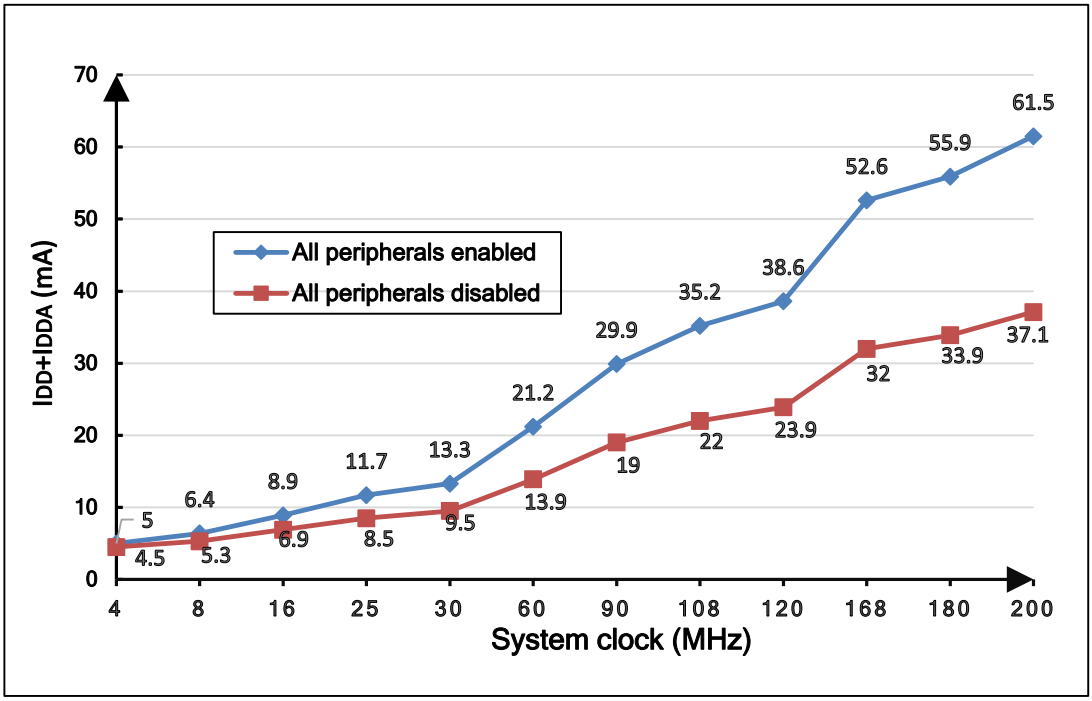
(2) Unless otherwise specified, all values given for $T_A$ = 25 ℃ and test result is mean value.

(3) When System Clock is less than 4 MHz, an external source is used, and the HXTAL bypass function is needed, no PLL.

(4) When System Clock is greater than 8 MHz, a crystal 8 MHz is used, and the HXTAL bypass function is closed, using PLL.

(5) When analog peripheral blocks such as ADCs, DACs, HXTAL, LXTAL, IRC16M, or IRC32K are ON, an additional power consumption should be considered.

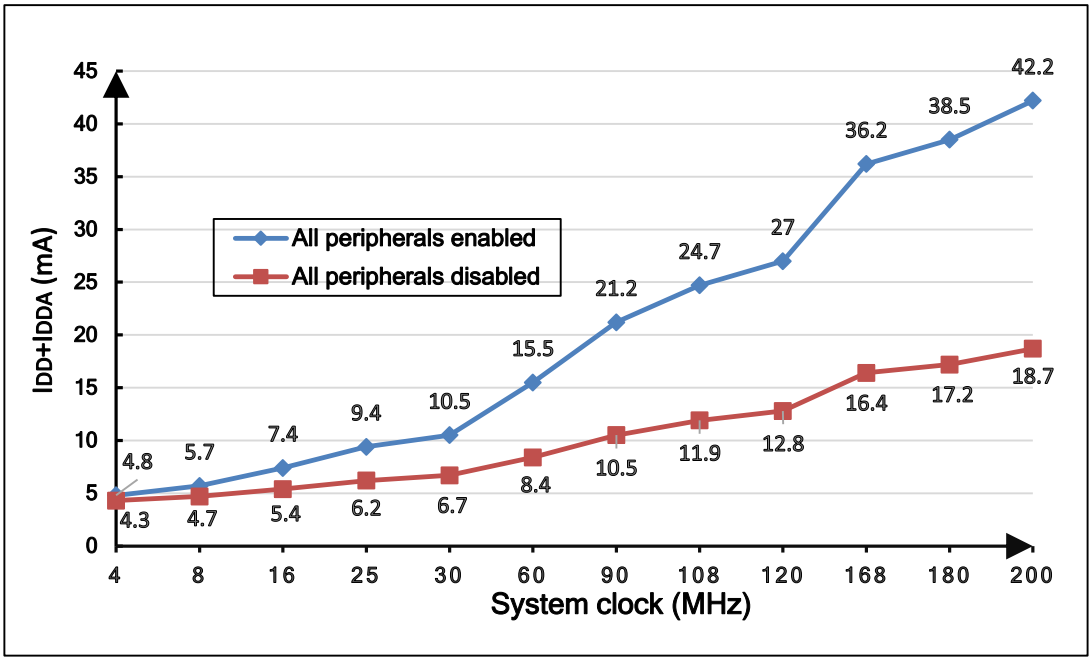
**Figure 4-2. Typical supply current consumption in Run mode**






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**Figure 4-3. Typical supply current consumption in Sleep mode**




## 4.4. EMC characteristics

EMS (electromagnetic susceptibility) includes ESD (Electrostatic discharge, positive and negative) and FTB (Burst of Fast Transient voltage, positive and negative) testing result is given in ***Table 4-8. EMS characteristics***, based on the EMS levels and classes compliant with IEC 61000 series standard.

**Table 4-8. EMS characteristics(1)**

| Symbol | Parameter | Conditions | Level/Class |
|---|---|---|---|
| $V_{ESD}$ | Voltage applied to all device pins to induce a functional disturbance | $V_{DD}$ = 3.3 V, $T_A$ = 25 °C LQFP144, $f_{HCLK}$ = 200 MHz conforms to IEC 61000-4-2 | 3A |
| $V_{FTB}$ | Fast transient voltage burst applied to induce a functional disturbance through 100 pF on $V_{DD}$ and $V_{SS}$ pins | $V_{DD}$ = 3.3 V, $T_A$ = 25 °C LQFP144, $f_{HCLK}$ = 200 MHz conforms to IEC 61000-4-4 | 3A |

(1) Based on characterization, not tested in production.

EMI (Electromagnetic Interference) emission test result is given in the ***Table 4-9. EMI characteristics***(1), The electromagnetic field emitted by the device are monitored while an application, executing EEMBC code, is running. The test is compliant with SAE J1752-3:2017 standard which specifies the test board and the pin loading.



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**Table 4-9. EMI characteristics(1)**

| Symbol | Parameter | Conditions | Tested frequency band | Max vs. [$f_{HXTAL}/f_{HCLK}$] 25/240 MHz | Unit |
|---|---|---|---|---|---|
| $S_{EMI}$ | Peak level | $V_{DD}$ = 3.6 V, $T_A$ = +25 °C, LQFP144, $f_{HCLK}$ = 200 MHz, conforms to SAE J1752-3:2017 | 0.15 MHz to 30 MHz | | dBµV |
| | | | 30 MHz to 130 MHz | | |
| | | | 130 MHz to 1 GHz | | |

(1) Based on characterization, not tested in production.

## 4.5. Power supply supervisor characteristics

**Table 4-10. Power supply supervisor characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{LVD}$(1) | Low voltage Detector level selection | LVDT<2:0> = 000(rising edge) | — | 2.1 | — | V |
| | | LVDT<2:0> = 000(falling edge) | — | 1.98 | — | |
| | | LVDT<2:0> = 001(rising edge) | — | 2.23 | — | |
| | | LVDT<2:0> = 001(falling edge) | — | 2.12 | — | |
| | | LVDT<2:0> = 010(rising edge) | — | 2.36 | — | |
| | | LVDT<2:0> = 010(falling edge) | — | 2.25 | — | |
| | | LVDT<2:0> = 011(rising edge) | — | 2.50 | — | |
| | | LVDT<2:0> = 011(falling edge) | — | 2.38 | — | |
| | | LVDT<2:0> = 100(rising edge) | — | 2.62 | — | |
| | | LVDT<2:0> = 100(falling edge) | — | 2.52 | — | |
| | | LVDT<2:0> = 101(rising edge) | — | 2.74 | — | |
| | | LVDT<2:0> = 101(falling edge) | — | 2.66 | — | |
| | | LVDT<2:0> = 110(rising edge) | — | 2.90 | — | |
| | | LVDT<2:0> = 110(falling edge) | — | 2.80 | — | |
| | | LVDT<2:0> = 111(rising edge) | — | 3.03 | — | |
| | | LVDT<2:0> = 111(falling edge) | — | 2.93 | — | |
| $V_{LVDhyst}$(2) | LVD hystersis | — | — | 100 | — | mV |
| $V_{POR}$(1) | Power on reset threshold | — | — | 2.45 | — | V |
| $V_{PDR}$(1) | Power down reset threshold | — | — | 1.82 | — | V |



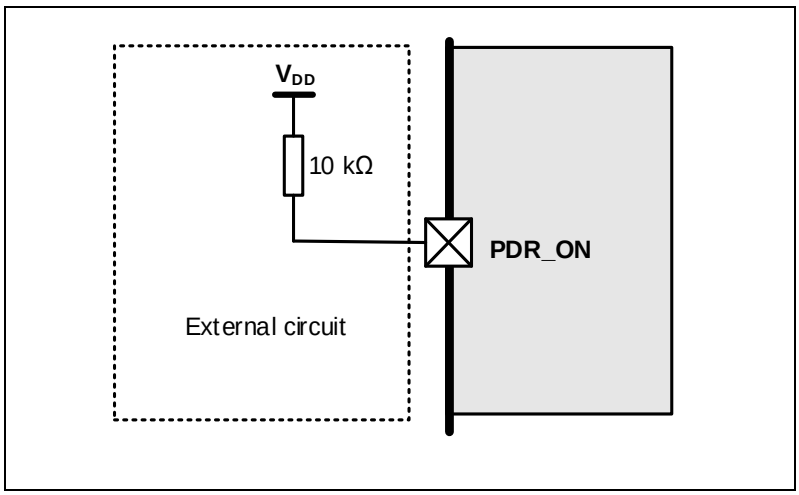
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| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{PDRhyst}$(2) | PDR hysteresis | — | — | 600 | — | mV |
| $V_{BOR3}$(1) | Brownout level 3 threshold | Falling edge | — | 2.80 | — | V |
| | | Rising edge | — | 2.89 | — | V |
| $V_{BOR2}$(1) | Brownout level 2 threshold | Falling edge | — | 2.51 | — | V |
| | | Rising edge | — | 2.59 | — | V |
| $V_{BOR1}$(1) | Brownout level 1 threshold | Falling edge | — | 2.20 | — | V |
| | | Rising edge | — | 2.30 | — | V |
| $V_{BORhyst}$(2) | BOR hysteresis | — | — | 100 | — | mV |
| $t_{RSTTEMPO}$(2) | Reset temporization | — | — | 2 | — | ms |

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

**Figure 4-4. Recommended PDR_ON pin circuit**




(1) The PDR supervisor can be enabled/disabled through PDR_ON pin.

(2) When PDR_ON pin is connected to $V_{SS}$ (Internal Reset OFF), the $V_{BAT}$ functionality is no more available and $V_{BAT}$ pin should be connected to $V_{DD}$.

## 4.6. Electrical sensitivity

The device is strained in order to determine its performance in terms of electrical sensitivity. Electrostatic discharges (ESD) are applied directly to the pins of the sample. Static latch-up (LU) test is based on the two measurement methods.

**Table 4-11. ESD characteristics(1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{ESD(HBM)}$ | Electrostatic discharge voltage (human body model) | $T_A$=25 °C; JS-001-2017 | — | — | 5000 | V |
| $V_{ESD(CDM)}$ | Electrostatic discharge voltage (charge device model) | $T_A$=25 °C; JS-002-2018 | — | — | 1000 | V |



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(1) Based on characterization, not tested in production.

**Table 4-12. Static latch-up characteristics(1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| LU | I-test | $T_A$=105 °C; JESD78 | — | — | ±200 | mA |
| | $V_{supply}$ over voltage | | — | — | 5.4 | V |

(1) Based on characterization, not tested in production.

## 4.7. External clock characteristics

**Table 4-13. High speed external clock (HXTAL) generated from a crystal/ceramic characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{HXTAL}$(1) | Crystal or ceramic frequency | 2.6 V ≤ $V_{DD}$ ≤ 3.6 V | 4 | 25 | 32 | MHz |
| $R_F$(2) | Feedback resistor | $V_{DD}$ = 3.3 V | — | 400 | — | kΩ |
| $C_{HXTAL}$(2) (3) | Recommended matching capacitance on OSCIN and OSCOUT | — | — | 20 | 30 | pF |
| $Ducy_{(HXTAL)}$(2) | Crystal or ceramic duty cycle | — | 30 | 50 | 70 | % |
| $g_m$(2) | Oscillator transconductance | Startup | — | 25 | — | mA/V |
| $I_{DDHXTAL}$(1) | Crystal or ceramic operating current | $V_{DD}$ = 3.3 V | — | 1.2 | — | mA |
| $t_{SUHXTAL}$(1) | Crystal or ceramic startup time | $V_{DD}$ = 3.3 V | — | 0.42 | — | ms |

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

(3) $C_{HXTAL1}$ = $C_{HXTAL2}$ = 2*($C_{LOAD}$ - $C_S$), For $C_{HXTAL1}$ and $C_{HXTAL2}$, it is recommended matching capacitance on OSCIN and OSCOUT. For $C_{LOAD}$, it is crystal/ceramic load capacitance, provided by the crystal or ceramic manufacturer. For $C_S$, it is PCB and MCU pin stray capacitance.

**Table 4-14. High speed external clock characteristics (HXTAL in bypass mode)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{HXTAL_ext}$(1) | External clock source or oscillator frequency | 2.6 V ≤ $V_{DD}$ ≤ 3.6 V | 1 | — | 50 | MHz |
| $V_{HXTALH}$(2) | OSCIN input pin high level voltage | $V_{DD}$ = 3.3 V | 0.7 $V_{DD}$ | — | $V_{DD}$ | V |
| $V_{HXTALL}$(2) | OSCIN input pin low level voltage | | $V_{SS}$ | — | 0.3 $V_{DD}$ | V |
| $t_{H/L(HXTAL)}$ (2) | OSCIN high or low time | — | 5 | — | — | ns |
| $t_{R/F(HXTAL)}$ (2) | OSCIN rise or fall time | — | — | — | 10 | ns |
| $C_{IN}$(2) | OSCIN input capacitance | — | — | 5 | — | pF |
| $Ducy_{(HXTAL)}$ (2) | Duty cycle | — | 40 | — | 60 | % |

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

**Table 4-15. Low speed external clock (LXTAL) generated from a crystal/ceramic**



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**characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{LXTAL}$(1) | Crystal or ceramic frequency | $V_{DD}$ = 3.3 V | — | 32.768 | — | kHz |
| $C_{LXTAL}$(2) (3) | Recommended matching capacitance on OSC32IN and OSC32OUT | — | — | 15 | — | pF |
| $Ducy_{(LXTAL)}$(2) | Crystal or ceramic duty cycle | — | 30 | — | 70 | % |
| $g_m$(2) | Oscillator transconductance | Medium low driving capability | — | 6 | — | μA/V |
| | | Higher driving capability | — | 18 | — | |
| $I_{DDLXTAL}$ (1) | Crystal or ceramic operating current | LXTALDRI= 0 | — | 0.8 | — | μA |
| | | LXTALDRI= 1 | — | 1.6 | — | |
| $t_{SULXTAL}$(1) (4) | Crystal or ceramic startup time | LXTALDRI= 0 | — | 369 | — | ms |
| | | LXTALDRI= 1 | — | 175 | — | ms |

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

(3) $C_{LXTAL1} = C_{LXTAL2} = 2*(C_{LOAD} - C_S)$, For $C_{LXTAL1}$ and $C_{LXTAL2}$, it is recommended matching capacitance on OSC32IN and OSC32OUT. For $C_{LOAD}$, it is crystal/ceramic load capacitance, provided by the crystal or ceramic manufacturer. For $C_S$, it is PCB and MCU pin stray capacitance.

(4) $t_{SULXTAL}$ is the startup time measured from the moment it is enabled (by software) to the 32.768 kHz oscillator stabilization flags is SET. This value varies significantly with the crystal manufacturer.

**Table 4-16. Low speed external user clock characteristics (LXTAL in bypass mode)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{LXTAL_ext}$(1) | External clock source or oscillator frequency | $V_{DD}$ = 3.3 V | — | 32.768 | 1000 | kHz |
| $V_{LXTALH}$(2) | OSC32IN input pin high level voltage | — | 0.7 $V_{DD}$ | — | $V_{DD}$ | V |
| $V_{LXTALL}$(2) | OSC32IN input pin low level voltage | — | $V_{SS}$ | — | 0.3 $V_{DD}$ | |
| $t_{H/L(LXTAL)}$ (2) | OSC32IN high or low time | — | 450 | — | — | ns |
| $t_{R/F(LXTAL)}$ (2) | OSC32IN rise or fall time | — | — | — | 50 | |
| $C_{IN}$(2) | OSC32IN input capacitance | — | — | 5 | — | pF |
| $Ducy_{(LXTAL)}$ (2) | Duty cycle | — | 30 | 50 | 70 | % |

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.



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## 4.8. Internal clock characteristics

**Table 4-17. High speed internal clock (IRC16M) characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{IRC16M}$ | High Speed Internal Oscillator (IRC16M) frequency | $V_{DD}$ = $V_{DDA}$ = 3.3 V | — | 16 | — | MHz |
| $ACC_{IRC16M}$ | IRC16M oscillator Frequency accuracy, Factory-trimmed | $V_{DD}$ = $V_{DDA}$ = 3.3 V, $T_A$ = -40 °C ~ +85 °C | — | -1.73 to +1.1 (1) | — | % |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, $T_A$ = 25 °C | -1.0 | — | +1.0 | % |
| | IRC16M oscillator Frequency accuracy, User trimming step | — | — | 0.5 | — | % |
| $Ducy_{IRC16M}$(2) | IRC16M oscillator duty cycle | $V_{DD}$ = $V_{DDA}$ = 3.3 V | 45 | 50 | 55 | % |
| $I_{DDIRC16M}$ +$I_{DDAIRC16M}$(1) | IRC16M oscillator operating current | $V_{DD}$ = $V_{DDA}$ = 3.3 V, $f_{HCLK}$ =$f_{HXTAL}$ = 25 MHz | — | 47 | — | μA |
| $t_{SUIRC16M}$(1) | IRC16M oscillator startup time | $V_{DD}$ = $V_{DDA}$ = 3.3 V, $f_{HCLK}$ =$f_{HXTAL_PLL}$ = 200 MHz | — | 1.18 | — | μs |

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

**Table 4-18. High speed internal clock (IRC48M) characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{IRC48M}$ | High Speed Internal Oscillator (IRC48M) frequency | $V_{DD}$ = 3.3 V | — | 48 | — | MHz |
| $ACC_{IRC48M}$ | IRC48M oscillator Frequency accuracy, Factory-trimmed | $V_{DD}$ = $V_{DDA}$ = 3.3 V, $T_A$ = -40 °C ~ +85 °C | — | -1.31 to -0.39 (1) | — | % |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, $T_A$ = 25 °C | -2.0 | — | +2.0 | % |
| | IRC48M oscillator Frequency accuracy, User trimming step | — | — | 0.12 | — | % |
| $Ducy_{IRC48M}$(2) | IRC48M oscillator duty cycle | $V_{DD}$ = $V_{DDA}$ = 3.3 V | 45 | 50 | 55 | % |
| $I_{DDIRC48M}$ +$I_{DDAIRC48M}$(1) | IRC48M oscillator operating current | $V_{DD}$ = $V_{DDA}$ = 3.3 V, $f_{HCLK}$ = $f_{IRC16M}$ = 16 MHz | — | 358 | — | μA |
| $t_{SUIRC48M}$(1) | IRC48M oscillator startup time | $V_{DD}$ = $V_{DDA}$ = 3.3 V, $f_{HCLK}$ = $f_{HXTAL_PLL}$ = 200 MHz | — | 1.23 | — | μs |

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.



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**Table 4-19. Low speed internal clock (IRC32K) characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{IRC32K}$(1) | Low Speed Internal oscillator (IRC32K) frequency | $V_{DD}$ = $V_{DDA}$ = 3.3 V, $T_A$ = -40 °C ~ +85 °C | — | 32 | — | kHz |
| $I_{DDAIRC32K}$(2) | IRC32K oscillator operating current | $V_{DD}$ = $V_{DDA}$ = 3.3 V, $f_{HCLK}$ = $f_{IRC16M}$ = 16 MHz, | — | 0.43 | — | μA |
| $t_{SUIRC32K}$(2) | IRC32K oscillator startup time | $V_{DD}$ = $V_{DDA}$ = 3.3 V, $f_{HCLK}$ = $f_{HXTAL_PLL}$ = 200 MHz, | — | 22.1 | — | μs |

(1) Guaranteed by design, not tested in production.

(2) Based on characterization, not tested in production.

## 4.9. PLL characteristics

**Table 4-20. PLL characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{PLLIN}$(1) | PLL input clock frequency | — | 1 | — | 4 | MHz |
| $f_{PLLOUT}$(2) | PLL output clock frequency | — | 100 | — | 500 | MHz |
| $f_{VCO}$(2) | PLL VCO output clock frequency | — | 32 | — | 344 | MHz |
| $t_{LOCK}$(2) | PLL lock time | — | — | — | 400 | μs |
| $I_{DDA}$(1)(3) | Current consumption on VDDA | VCO freq = 400 MHz | — | 797 | — | μA |
| $Jitter_{PLL}$ | Cycle to cycle Jitter(rms) | System clock | — | 40 | — | ps |
| | Cycle to cycle Jitter（peak to peak） | | — | 400 | — | |

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

(3) System clock = HXTAL = 25 MHz, PLL clock source = HXTAL/25 = 1 MHz, $f_{PLLOUT}$ = 100 MHz.

(4) Value given with main PLL running.

**Table 4-21. PLLI2S characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{PLLIN}$(1) | PLLI2S input clock frequency | — | 1 | — | 4 | MHz |
| $f_{PLLOUT}$(2) | PLLI2S output clock frequency | — | 100 | — | 500 | MHz |
| $f_{VCO}$(2) | PLLI2S VCO output clock frequency | — | 32 | — | 344 | MHz |
| $t_{LOCK}$(2) | PLLI2S lock time | — | — | — | 400 | μs |
| $I_{DDA}$(1)(3) | Current consumption on VDDA | VCO freq = 400 MHz | — | 814 | — | μA |
| $Jitter_{PLL}$ | Cycle to cycle Jitter(rms) | System clock | — | 40 | — | ps |
| | Cycle to cycle Jitter（peak to peak） | | — | 400 | — | |



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(1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.
(3) System clock = HXTAL = 25 MHz, PLL clock source = HXTAL/25 = 1 MHz, $f_{PLLOUT}$ = 100 MHz.
(4) Value given with main PLLI2S running.

**Table 4-22. PLLSAI characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{PLLIN}$(1) | PLLSAI input clock frequency | — | 1 | — | 4 | MHz |
| $f_{PLLOUT}$(2) | PLLSAI output clock frequency | — | 100 | — | 500 | MHz |
| $f_{VCO}$(2) | PLLSAI VCO output clock frequency | — | 32 | — | 344 | MHz |
| $t_{LOCK}$(2) | PLLSAI lock time | — | — | — | 400 | μs |
| $I_{DDA}$(1)(3) | Current consumption on VDDA | VCO freq = 400 MHz | — | 796 | — | μA |
| $Jitter_{PLL}$ | Cycle to cycle Jitter(rms) | System clock | — | 40 | — | ps |
| | Cycle to cycle Jitter（peak to peak） | | — | 400 | — | |

(1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.
(3) System clock = HXTAL = 25 MHz, PLL clock source = HXTAL/25 = 1 MHz, $f_{PLLOUT}$ = 100 MHz.
(4) Value given with main PLLSAI running.

**Table 4-23. PLL spread spectrum clock generation (SSCG) characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{mod}$ | Modulation frequency | — | — | — | 10 | KHz |
| mdamp | Peak modulation amplitude | — | — | — | 2 | % |
| MODCNT* MODSTEP | — | — | — | — | $2^{15}$-1 | — |

(1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.

***Equation 1***: SSCG configuration equation:

$$\mathrm{MODCNT} = \mathrm{round}(f_{\mathrm{PLLIN}}/4/f_{\mathrm{mod}})$$

$$\mathrm{MODSTEP} = \mathrm{round}(\mathrm{mdamp} * \mathrm{PLLN} * 2^{14}/(\mathrm{MODCNT} * 100))$$

The formula above (Equation 1) is SSCG configuration equation.



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## 4.10. Memory characteristics

**Table 4-24. Flash memory characteristics**

| Symbol | Parameter | Conditions | Min(1) | Typ(1) | Max(2) | Unit |
|---|---|---|---|---|---|---|
| $PE_{CYC}$ | Number of guaranteed program /erase cycles before failure (Endurance) | $T_A$ = -40 °C ~ +85 °C | 50 | — | — | kcycles |
| $t_{RET}$ | Data retention time | — | — | 20 | — | years |
| $t_{PROG}$ | Word programming time | $T_A$ = -40°C ~ +85 °C | — | 37.5 | 180 | µs |
| $t_{ERASE16kB}$ | Sector(16kB) erase time | $T_A$ = -40°C ~ +85 °C | — | 200 | 2000 | ms |
| $t_{ERASE64kB}$ | Sector(64kB) erase time | | — | 300 | 4000 | |
| $t_{ERASE128kB}$ | Sector(128kB) erase time | | — | 600 | 8000 | |
| $t_{MERASE(512K)}$ | Mass erase time | $T_A$ = -40°C ~ +85 °C | — | 2.4 | 32 | s |
| $t_{MERASE(1MB)}$ | Mass erase time | $T_A$ = -40°C ~ +85 °C | — | 4.8 | 64 | s |
| $t_{MERASE(2MB)}$ | Mass erase time | $T_A$ = -40°C ~ +85 °C | — | 9.6 | 128 | s |
| $t_{MERASE(3MB)}$ | Mass erase time | $T_A$ = -40°C ~ +85 °C | — | 14.4 | 192 | s |

(1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.

## 4.11. NRST pin characteristics

**Table 4-25. NRST pin characteristics**

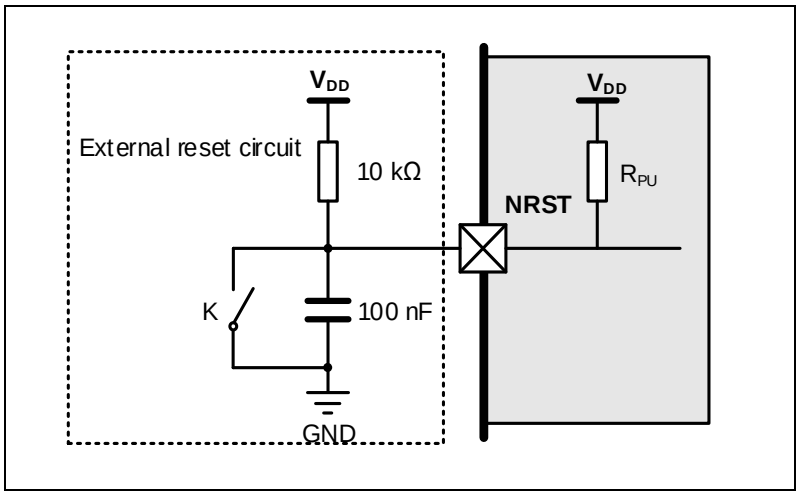
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IL(NRST)}$(1) | NRST Input low level voltage | $V_{DD}$ = $V_{DDA}$ = 2.6 V | -0.3 | — | 0.3 $V_{DD}$ | V |
| $V_{IH(NRST)}$(1) | NRST Input high level voltage | | 0.7 $V_{DD}$ | — | $V_{DD}$ + 0.3 | |
| $V_{hyst}$(1) | Schmidt trigger Voltage hysteresis | | — | 440 | — | mV |
| $V_{IL(NRST)}$(1) | NRST Input low level voltage | $V_{DD}$ = $V_{DDA}$ = 3.3 V | -0.3 | — | 0.3 $V_{DD}$ | V |
| $V_{IH(NRST)}$(1) | NRST Input high level voltage | | 0.7 $V_{DD}$ | — | $V_{DD}$ + 0.3 | |
| $V_{hyst}$(1) | Schmidt trigger Voltage hysteresis | | — | 490 | — | mV |
| $V_{IL(NRST)}$(1) | NRST Input low level voltage | $V_{DD}$ = $V_{DDA}$ = 3.6 V | -0.3 | — | 0.3 $V_{DD}$ | V |
| $V_{IH(NRST)}$(1) | NRST Input high level voltage | | 0.7 $V_{DD}$ | — | $V_{DD}$ + 0.3 | |
| $V_{hyst}$(1) | Schmidt trigger Voltage hysteresis | | — | 510 | — | mV |
| $R_{pu}$(2) | Pull-up equivalent resistor | — | — | 40 | — | kΩ |

(1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.



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**Figure 4-5. Recommended external NRST pin circuit**




## 4.12. GPIO characteristics

**Table 4-26. I/O port DC characteristics(1)(3)**

| Symbol | Parameter | | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{IL}$ | Standard IO Low level input voltage | | 2.6 V ≤ $V_{DD}$ = $V_{DDA}$ ≤ 3.6 V | — | — | 0.3 $V_{DD}$ | V |
| | 5V-tolerant IO Low level input voltage | | 2.6 V ≤ $V_{DD}$ = $V_{DDA}$ ≤ 3.6 V | — | — | 0.3 $V_{DD}$ | V |
| $V_{IH}$ | Standard IO Low level input voltage | | 2.6 V ≤ $V_{DD}$ = $V_{DDA}$ ≤ 3.6 V | 0.7 $V_{DD}$ | — | — | V |
| | 5V-tolerant IO Low level input voltage | | 2.6 V ≤ $V_{DD}$ = $V_{DDA}$ ≤ 3.6 V | 0.7 $V_{DD}$ | — | — | V |
| $R_{PU}$(2) | Internal pull-up resistor | All pins | $V_{IN}$ = $V_{SS}$ | — | 40 | — | kΩ |
| | | PA10 | — | — | 10 | — | |
| $R_{PD}$(2) | Internal pull-down resistor | All pins | $V_{IN}$ = $V_{DD}$ | — | 40 | — | kΩ |
| | | PA10 | — | — | 10 | — | |
| **IO_Speed:level 3** | | | | | | | |
| $V_{OL}$ | Low level output voltage for an IO Pin ($I_{IO}$ = +8 mA) | | $V_{DD}$ = 2.6 V | — | — | 0.11 | V |
| | | | $V_{DD}$ = 3.3 V | — | — | 0.10 | |
| | | | $V_{DD}$ = 3.6 V | — | — | 0.10 | |
| | Low level output voltage for an IO Pin ($I_{IO}$ = +20 mA) | | $V_{DD}$ = 2.6 V | — | — | 0.29 | |
| | | | $V_{DD}$ = 3.3 V | — | — | 0.27 | |
| | | | $V_{DD}$ = 3.6 V | — | — | 0.26 | |
| $V_{OH}$ | High level output voltage for an IO Pin ($I_{IO}$ = +8 mA) | | $V_{DD}$ = 2.6 V | 2.46 | — | — | |
| | | | $V_{DD}$ = 3.3 V | 3.18 | — | — | |
| | | | $V_{DD}$ = 3.6 V | 3.48 | — | — | |
| | High level output voltage for an IO Pin | | $V_{DD}$ = 2.6 V | 2.22 | — | — | |
| | | | $V_{DD}$ = 3.3 V | 2.98 | — | — | |



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| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | ($I_{IO}$ = +20 mA) | $V_{DD}$ = 3.6 V | 3.29 | — | — | |
| **IO_Speed:level 2** | | | | | | |
| $V_{OL}$ | Low level output voltage for an IO Pin ($I_{IO}$ = +8 mA) | $V_{DD}$ = 2.6 V | — | — | 0.16 | V |
| | | $V_{DD}$ = 3.3 V | — | — | 0.14 | |
| | | $V_{DD}$ = 3.6 V | — | — | 0.14 | |
| | Low level output voltage for an IO Pin ($I_{IO}$ = +20 mA) | $V_{DD}$ = 2.6 V | — | — | 0.43 | |
| | | $V_{DD}$ = 3.3 V | — | — | 0.37 | |
| | | $V_{DD}$ = 3.6 V | — | — | 0.36 | |
| $V_{OH}$ | High level output voltage for an IO Pin ($I_{IO}$ = +8 mA) | $V_{DD}$ = 2.6 V | 2.40 | — | — | |
| | | $V_{DD}$ = 3.3 V | 3.12 | — | — | |
| | | $V_{DD}$ = 3.6 V | 3.44 | — | — | |
| | High level output voltage for an IO Pin ($I_{IO}$ = +20 mA) | $V_{DD}$ = 2.6 V | 2.05 | — | — | |
| | | $V_{DD}$ = 3.3 V | 2.84 | — | — | |
| | | $V_{DD}$ = 3.6 V | 3.17 | — | — | |
| **IO_Speed:level 1** | | | | | | |
| $V_{OL}$ | Low level output voltage for an IO Pin ($I_{IO}$ = +8 mA) | $V_{DD}$ = 2.6 V | — | — | 0.28 | V |
| | | $V_{DD}$ = 3.3 V | — | — | 0.28 | |
| | | $V_{DD}$ = 3.6 V | — | — | 0.24 | |
| | ($I_{IO}$ = +15 mA) | $V_{DD}$ = 2.6 V | — | — | 0.57 | |
| | Low level output voltage for an IO Pin ($I_{IO}$ = +20 mA) | $V_{DD}$ = 3.3 V | — | — | 0.66 | |
| | | $V_{DD}$ = 3.6 V | — | — | 0.64 | |
| $V_{OH}$ | High level output voltage for an IO Pin ($I_{IO}$ = +8 mA) | $V_{DD}$ = 2.6 V | 2.23 | — | — | |
| | | $V_{DD}$ = 3.3 V | 3.00 | — | — | |
| | | $V_{DD}$ = 3.6 V | 3.31 | — | — | |
| | ($I_{IO}$ = +15 mA) | $V_{DD}$ = 2.6 V | 1.83 | — | — | |
| | High level output voltage for an IO Pin ($I_{IO}$ = +20 mA) | $V_{DD}$ = 3.3 V | 2.45 | — | — | |
| | | $V_{DD}$ = 3.6 V | 2.81 | — | — | |
| **IO_Speed:level 0** | | | | | | |
| $V_{OL}$ | Low level output voltage for an IO Pin ($I_{IO}$ = +1 mA) | $V_{DD}$ = 2.6 V | — | — | 0.17 | V |
| | | $V_{DD}$ = 3.3 V | — | — | 0.15 | |
| | | $V_{DD}$ = 3.6 V | — | — | 0.15 | |
| | Low level output voltage for an IO Pin ($I_{IO}$ = +4 mA) | $V_{DD}$ = 2.6 V | — | — | 0.80 | |
| | | $V_{DD}$ = 3.3 V | — | — | 0.63 | |
| | | $V_{DD}$ = 3.6 V | — | — | 0.60 | |
| $V_{OH}$ | High level output voltage for an IO Pin ($I_{IO}$ = +1 mA) | $V_{DD}$ = 2.6 V | 2.38 | — | — | |
| | | $V_{DD}$ = 3.3 V | 3.12 | — | — | |
| | | $V_{DD}$ = 3.6 V | 3.42 | — | — | |
| | High level output voltage for an IO Pin | $V_{DD}$ = 2.6 V | 1.45 | — | — | |
| | | $V_{DD}$ = 3.3 V | 2.48 | — | — | |



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| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | ($I_{IO}$ = +4 mA) | $V_{DD}$ = 3.6 V | 2.83 | — | — | |

(1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.
(3) All pins except PC13 / PC14 / PC15 / PI8. Since PC13 to PC15 and PI8 are supplied through the Power Switch, which can only be obtained by a small current, the speed of GPIOs PC13 to PC15 and PI8 should not exceed 2 MHz when they are in output mode(maximum load: 30 pF).

**Table 4-27. I/O port AC characteristics(1)(2)(4)**

| GPIOx_OSPD[1:0] bit value(3) | Parameter | Conditions | Max | Unit |
|---|---|---|---|---|
| GPIOx_OSPD0->OSPDy[1:0] = 00 (IO_Speed:level 0) | $T_{Rise}/T_{Fall}$ | 2.6 ≤ $V_{DD}$ ≤ 3.6 V, $C_L$ = 10 pF | 51 | ns |
| | | 2.6 ≤ $V_{DD}$ ≤ 3.6 V, $C_L$ = 30 pF | 63.2 | |
| | | 2.6 ≤ $V_{DD}$ ≤ 3.6 V, $C_L$ = 50 pF | 74.2 | |
| GPIOx_OSPD0->OSPDy[1:0] = 01 (IO_Speed:level 1) | $T_{Rise}/T_{Fall}$ | 2.6 ≤ $V_{DD}$ ≤ 3.6 V, $C_L$ = 10 pF | 3.6 | ns |
| | | 2.6 ≤ $V_{DD}$ ≤ 3.6 V, $C_L$ = 30 pF | 9.6 | |
| | | 2.6 ≤ $V_{DD}$ ≤ 3.6 V, $C_L$ = 50 pF | 12.2 | |
| GPIOx_OSPD0->OSPDy[1:0] = 10 (IO_Speed: level 2) | $T_{Rise}/T_{Fall}$ | 2.6 ≤ $V_{DD}$ ≤ 3.6 V, $C_L$ = 10 pF | 2.2 | ns |
| | | 2.6 ≤ $V_{DD}$ ≤ 3.6 V, $C_L$ = 30 pF | 3 | |
| | | 2.6 ≤ $V_{DD}$ ≤ 3.6 V, $C_L$ = 50 pF | 3.8 | |
| GPIOx_OSPD0->OSPDy[1:0] = 11 (IO_Speed:level 3) | $T_{Rise}/T_{Fall}$ | 2.6 ≤ $V_{DD}$ ≤ 3.6 V, $C_L$ = 10 pF | 2 | ns |
| | | 2.6 ≤ $V_{DD}$ ≤ 3.6 V, $C_L$ = 30 pF | 2.8 | |
| | | 2.6 ≤ $V_{DD}$ ≤ 3.6 V, $C_L$ = 50 pF | 3.4 | |

(1) Based on characterization, not tested in production.
(2) Unless otherwise specified, all test results given for $T_A$ = 25 °C.
(3) The I/O speed is configured using the GPIOx_OSPD -> OSPDy[1:0] bits.
(4) Only for reference, Depending on user's design.
(5) Max frequency is defined when the sum of rise time plus the fall time is less than 2/3 cycle.



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## 4.13. ADC characteristics

**Table 4-28. ADC characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DDA}$(1) | Operating voltage | — | 2.6 | 3.3 | 3.6 | V |
| $V_{IN}$(1) | ADC input voltage range | — | 0 | — | $V_{REF+}$ | V |
| $V_{REF+}$(2) | Positive Reference Voltage | — | 2.6 | — | $V_{DDA}$ | V |
| $V_{REF-}$(2) | Negative Reference Voltage | — | — | $V_{SSA}$ | — | V |
| $f_{ADC}$(1) | ADC clock | — | 0.1 | — | 40 | MHz |
| $f_S$(1) | Sampling rate | 12-bit | 0.007 | — | 2.6 | MSPS |
| | | 10-bit | 0.008 | — | 3.1 | |
| | | 8-bit | 0.01 | — | 3.6 | |
| | | 6-bit | 0.011 | — | 4.4 | |
| $V_{AIN}$(1) | Analog input voltage | 16 external;3 internal | 0 | — | $V_{REF+}$ | V |
| $R_{AIN}$(2) | External input impedance | See ***Equation 2*** | — | — | 308.6 | kΩ |
| $R_{ADC}$(2) | Input sampling switch resistance | — | — | — | 0.55 | kΩ |
| $C_{ADC}$(2) | Input sampling capacitance | No pin/pad capacitance included | — | — | 4.0 | pF |
| $t_{CAL}$(2) | Calibration time | $f_{ADC}$ = 40 MHz | — | 3.275 | — | μs |
| $t_s$(2) | Sampling time | $f_{ADC}$ = 40 MHz | 0.075 | — | 12 | μs |
| $t_{CONV}$(2) | Total conversion time (including sampling time) | 12-bit | — | 15 | — | 1/$f_{ADC}$ |
| | | 10-bit | — | 13 | — | |
| | | 8-bit | — | 11 | — | |
| | | 6-bit | — | 9 | — | |
| $t_{SU}$(2) | Startup time | — | — | — | 1 | μs |

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

***Equation 2***: $R_{AIN}$ max formula $$R_{AIN} < \frac{T_s}{f_{ADC} * C_{ADC} * \ln(2^{N+2})} - R_{ADC}$$

The formula above (Equation 2) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

**Table 4-29. ADC RAIN max for $f_{ADC}$ = 40 MHz(2)**

| $T_s$ (cycles) | $t_s$ (us) | $R_{AIN\ max}$ (KΩ) |
|---|---|---|
| 3 | 0.075 | 1.3 |
| 15 | 0.375 | 9.1 |
| 28 | 0.7 | 17.4 |
| 55 | 1.375 | 34.8 |
| 84 | 2.1 | 53.5 |
| 112 | 2.8 | 71.5 |
| 144 | 3.6 | 92.1 |
| 480 | 12 | 308.6 |



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(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

**Table 4-30. ADC dynamic accuracy at $f_{ADC}$ = 40 MHz(1)**

| Symbol | Parameter | Test conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| ENOB | Effective number of bits | $f_{ADC}$ = 40 MHz | — | 10.9 | — | bits |
| SNDR | Signal-to-noise and distortion ratio | $V_{DDA}$ = $V_{REF+}$ = 3.3 V | — | 67.3 | — | dB |
| SNR | Signal-to-noise ratio | Input Frequency = 110 kHz | — | 67.7 | — | |
| THD | Total harmonic distortion | Temperature = 25 ℃ | — | -75 | — | |

(1) Based on characterization, not tested in production.

**Table 4-31. ADC static accuracy at $f_{ADC}$ = 40 MHz(1)**

| Symbol | Parameter | Test conditions | Typ | Max | Unit |
|---|---|---|---|---|---|
| Offset | Offset error | $f_{ADC}$ = 40 MHz<br>$V_{DDA}$ = $V_{REF+}$ = 3.3 V | ±1 | — | LSB |
| DNL | Differential linearity error | | ±1 | — | |
| INL | Integral linearity error | | ±1.5 | — | |

(1) Based on characterization, not tested in production.

## 4.14. Temperature sensor characteristics

**Table 4-32. Temperature sensor characteristics(1)**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_L$ | $V_{SENSE}$ linearity with temperature | — | ±1.5 | — | ℃ |
| Avg_Slope | Average slope | — | 4.4 | — | mV/℃ |
| $V_{25}$ | Voltage at 25 °C | — | 1.4 | — | V |
| $t_{S_temp}$ (2) | ADC sampling time when reading the temperature | — | 17.1 | — | μs |

(1) Based on characterization, not tested in production.

(2) Shortest sampling time can be determined in the application by multiple iterations.

## 4.15. DAC characteristics

**Table 4-33. DAC characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DDA}$(1) | Operating voltage | — | 2.6 | 3.3 | 3.6 | V |
| $V_{REF+}$(2) | Positive Reference Voltage | — | 2.6 | — | $V_{DDA}$ | V |
| $V_{REF-}$(2) | Negative Reference Voltage | — | — | $V_{SSA}$ | — | V |
| $R_{LOAD}$(2) | Resistive load | Resistive load with buffer ON | 5 | — | — | kΩ |
| Ro(2) | Impedance output | Impedance output with buffer OFF | — | — | 15 | kΩ |
| $C_{LOAD}$(2) | Capacitive load | Capacitive load with buffer ON | — | — | 50 | pF |
| DAC_OUT min(2) | Lower DAC_OUT voltage | Lower DAC_OUT voltage with buffer ON | 0.2 | — | — | V |



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| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | | Lower DAC_OUT voltage with buffer OFF | 0.5 | — | — | mV |
| DAC_OUT max (2) | Higher DAC_OUT voltage | Higher DAC_OUT voltage with buffer ON | — | — | $V_{DDA}$-0.2 | V |
| | | Higher DAC_OUT voltage with buffer OFF | — | — | $V_{DDA}$-1LSB | V |
| $I_{DDA}$(1) | DAC current consumption in quiescent mode | With no load, middle code(0x800) on the input, $V_{REF+}$ = 3.6 V | — | 350 | — | μA |
| | | With no load, worst code(0xF1C) on the input, $V_{REF+}$ = 3.6 V | — | 430 | — | |
| $I_{DDVREF+}$(1) | DAC current consumption in quiescent mode | With no load, middle code(0x800) on the input, $V_{REF+}$ = 3.6 V | — | 115 | — | μA |
| | | With no load, worst code(0xF1C) on the input, $V_{REF+}$ = 3.6 V | — | 298 | — | |
| DNL(1) | Differential non linearity | 10-bit configuration | — | — | ±0.75 | LSB |
| | | 12-bit configuration | — | — | ±3 | |
| INL(1) | Integral non linearity | 10-bit configuration | — | — | ±1.25 | LSB |
| | | 12-bit configuration | — | — | ±5 | |
| Offset(1) | Offset error | DAC in 12-bit mode | — | — | ±24 | LSB |
| GE(1) | Gain error | DAC in 12-bit mode | — | — | ±1.5 | % |
| $T_{setting}$(1) | Settling time | $C_{LOAD}$ ≤ 50 pF, $R_{LOAD}$ ≥ 5 kΩ | — | 0.5 | 1 | μs |
| $T_{wakeup}$(2) | Wakeup from off state | — | — | 5 | 10 | μs |
| Update rate(2) | Max frequency for a correct DAC_OUT change from code i to i±1LSB | $C_{LOAD}$ ≤ 50 pF, $R_{LOAD}$ ≥ 5 kΩ | — | — | 4 | MS/s |
| PSRR(2) | Power supply rejection ratio(to $V_{DDA}$) | No $R_{Load}$, $C_{LOAD}$=50 pF | — | -90 | — | dB |

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

## 4.16. I2C characteristics

**Table 4-34. I2C characteristics(1)(2)**

| Symbol | Parameter | Conditions | Standard mode | | Fast mode | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| $t_{SCL(H)}$ | SCL clock high time | — | 4.0 | — | 0.6 | — | μs |
| $t_{SCL(L)}$ | SCL clock low time | — | 4.7 | — | 1.3 | — | μs |
| $t_{su(SDA)}$ | SDA setup time | — | 250 | — | 100 | — | ns |



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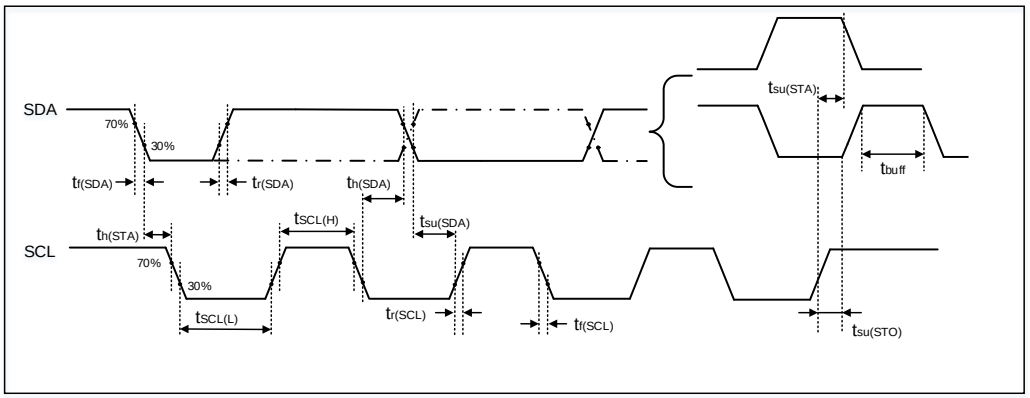
| Symbol | Parameter | Conditions | Standard mode | | Fast mode | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| $t_{h(SDA)}$ | SDA data hold time | — | 0(3) | 3450 | 0 | 900 | ns |
| $t_{r(SDA/SCL)}$ | SDA and SCL rise time | — | — | 1000 | — | 300 | ns |
| $t_{f(SDA/SCL)}$ | SDA and SCL fall time | — | — | 300 | — | 300 | ns |
| $t_{h(STA)}$ | Start condition hold time | — | 4.0 | — | 0.6 | — | μs |
| $t_{s(STA)}$ | Repeated Start condition setup time | — | 4.7 | — | 0.6 | — | μs |
| $t_{s(STO)}$ | Stop condition setup time | — | 4.0 | — | 0.6 | — | μs |
| $t_{buff}$ | Stop to Start condition time (bus free) | — | 4.7 | — | 1.3 | — | μs |

(1) Guaranteed by design, not tested in production.

(2) To ensure the standard mode I2C frequency, $f_{PCLK1}$ must be at least 2 MHz. To ensure the fast mode I2C frequency, $f_{PCLK1}$ must be at least 4 MHz.

(3) The device should provide a data hold time of 300 ns at least in order to bridge the undefined region of the falling edge of SCL.

**Figure 4-6. I2C bus timing diagram**






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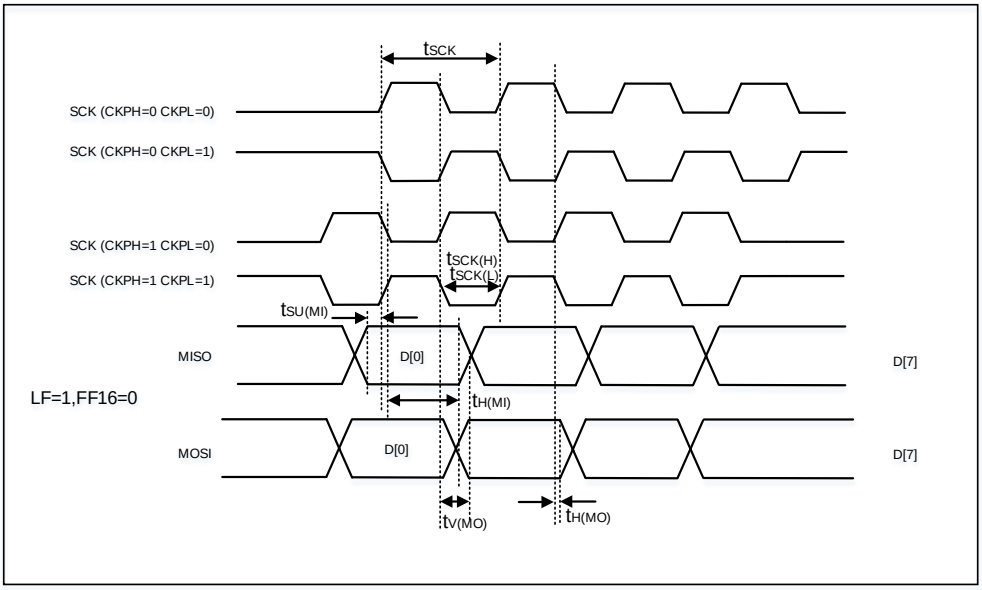
## 4.17. SPI characteristics

**Table 4-35. Standard SPI characteristics(1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{SCK}$ | SCK clock frequency | — | — | — | 30 | MHz |
| $t_{SCK(H)}$ | SCK clock high time | Master mode, $f_{PCLKx}$ = 120 MHz, presc = 4 | 14.67 | 16.67 | 18.67 | ns |
| $t_{SCK(L)}$ | SCK clock low time | Master mode, $f_{PCLKx}$ = 120 MHz, presc = 4 | 14.67 | 16.67 | 18.67 | ns |
| **SPI master mode** | | | | | | |
| $t_{V(MO)}$ | Data output valid time | — | — | — | 8 | ns |
| $t_{SU(MI)}$ | Data input setup time | — | 1 | — | — | ns |
| $t_{H(MI)}$ | Data input hold time | — | 0 | — | — | ns |
| **SPI slave mode** | | | | | | |
| $t_{SU(NSS)}$ | NSS enable setup time | — | 0 | — | — | ns |
| $t_{H(NSS)}$ | NSS enable hold time | — | 1 | — | — | ns |
| $t_{A(SO)}$ | Data output access time | — | — | 9 | — | ns |
| $t_{DIS(SO)}$ | Data output disable time | — | — | 10 | — | ns |
| $t_{V(SO)}$ | Data output valid time | — | — | 11 | — | ns |
| $t_{SU(SI)}$ | Data input setup time | — | 0 | — | — | ns |
| $t_{H(SI)}$ | Data input hold time | — | 2 | — | — | ns |

(1) Based on characterization, not tested in production.

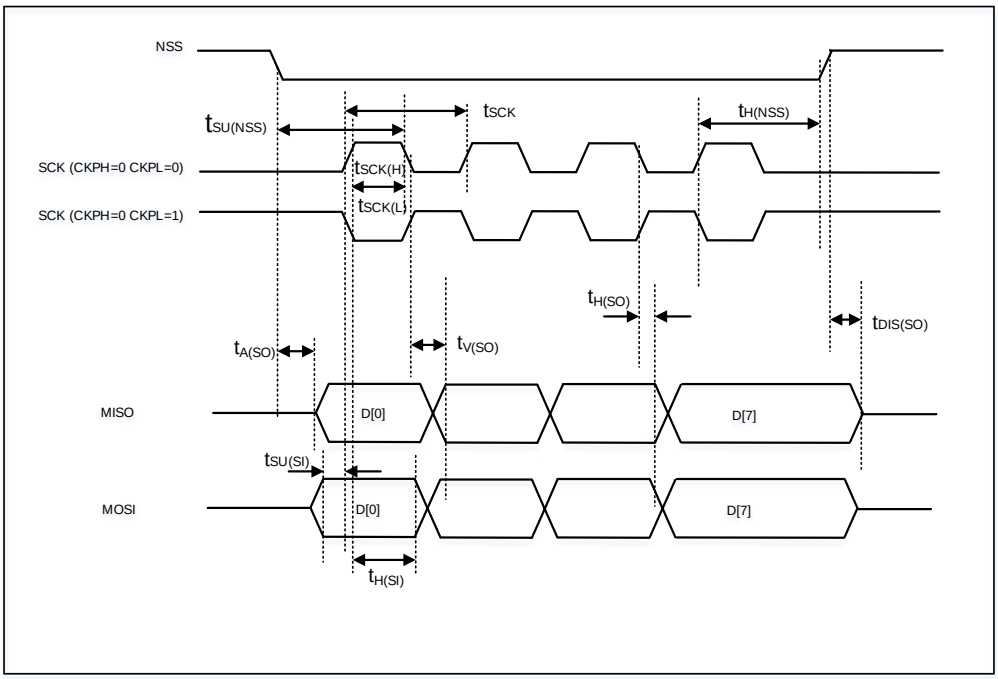
**Figure 4-7. SPI timing diagram - master mode**






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**Figure 4-8. SPI timing diagram - slave mode**






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## 4.18. I2S characteristics

**Table 4-36. I2S characteristics(1)(2)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{CK}$ | Clock frequency | Master mode (data: 32 bits, Audio frequency = 96 kHz) | — | 6.25 | — | MHz |
| | | Slave mode | — | — | 12.5 | |
| $t_H$ | Clock high time | — | — | 80 | — | ns |
| $t_L$ | Clock low time | | — | 80 | — | ns |
| $t_{V(WS)}$ | WS valid time | Master mode | — | 3 | — | ns |
| $t_{H(WS)}$ | WS hold time | Master mode | — | 3 | — | ns |
| $t_{SU(WS)}$ | WS setup time | Slave mode | 0 | — | — | ns |
| $t_{H(WS)}$ | WS hold time | Slave mode | 3 | — | — | ns |
| $Ducy_{(SCK)}$ | I2S slave input clock duty cycle | Slave mode | — | 50 | — | % |
| $t_{SU(SD_MR)}$ | Data input setup time | Master mode | 0 | — | — | ns |
| $t_{su(SD_SR)}$ | Data input setup time | Slave mode | 0 | — | — | ns |
| $t_{H(SD_MR)}$ | Data input hold time | Master receiver | 1 | — | — | ns |
| $t_{H(SD_SR)}$ | | Slave receiver | 3 | — | — | ns |
| $t_{V(SD_ST)}$ | Data output valid time | Slave transmitter (after enable edge) | — | — | 9 | ns |
| $t_{H(SD_ST)}$ | Data output hold time | Slave transmitter (after enable edge) | 6 | — | — | ns |
| $t_{V(SD_MT)}$ | Data output valid time | Master transmitter (after enable edge) | — | — | 6 | ns |
| $t_{H(SD_MT)}$ | Data output hold time | Master transmitter (after enable edge) | 0 | — | — | ns |

(1) Guaranteed by design, not tested in production.

(2) Based on characterization, not tested in production.



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**Figure 4-9. I2S timing diagram - master mode**

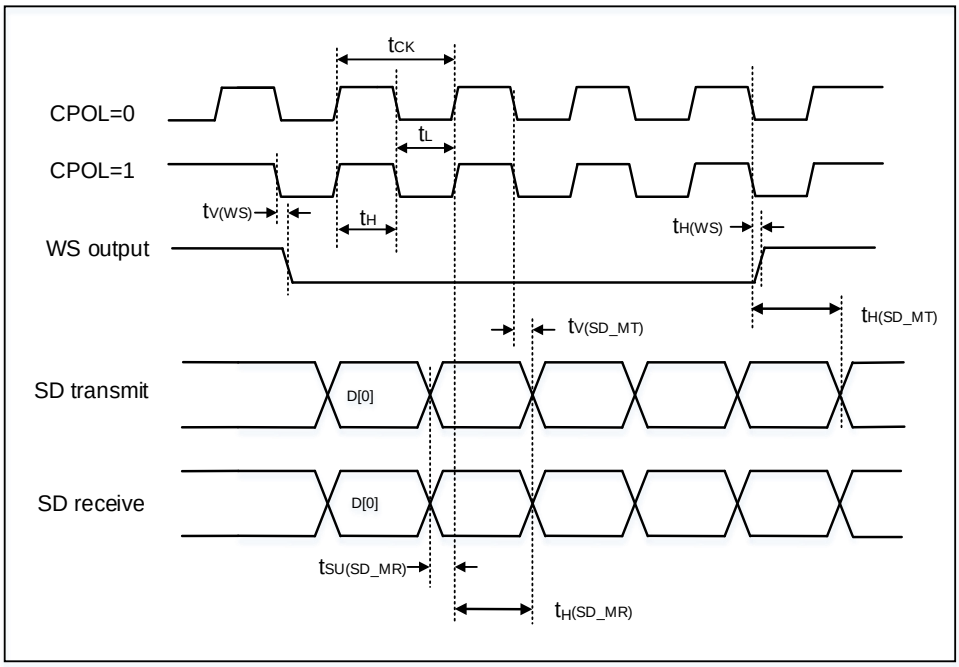
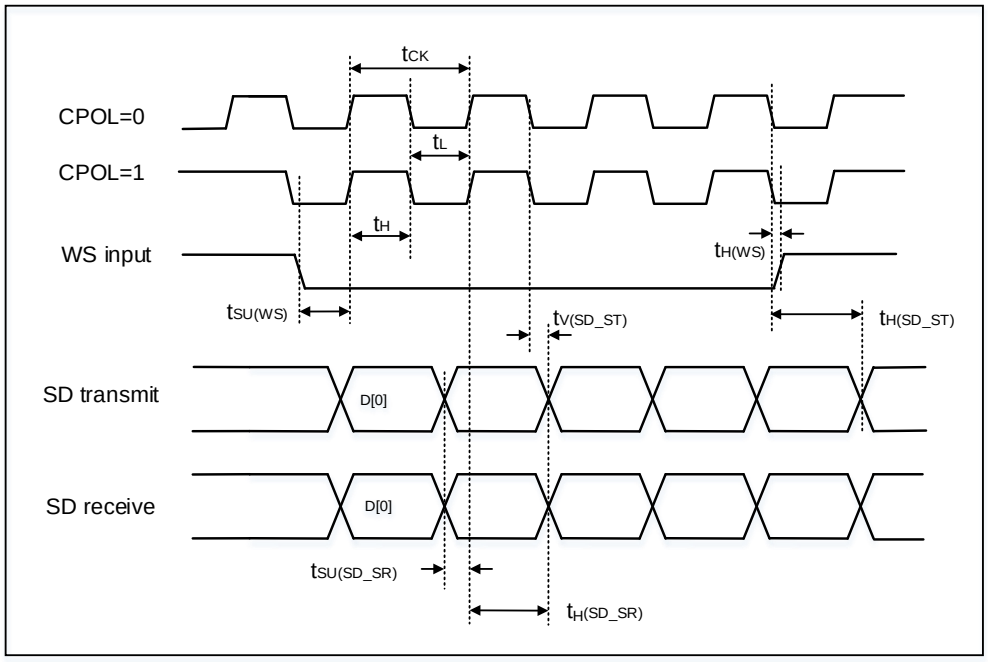



**Figure 4-10. I2S timing diagram - slave mode**






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## 4.19. USART characteristics

**Table 4-37. USART characteristics(1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{SCK}$ | SCK clock frequency | $f_{PCLKx}$ =100MHz | — | — | 50 | MHz |
| $t_{SCK(H)}$ | SCK clock high time | $f_{PCLKx}$ =100MHz | 10 | — | — | ns |
| $t_{SCK(L)}$ | SCK clock low time | $f_{PCLKx}$ =100MHz | 10 | — | — | ns |

(1) Guaranteed by design, not tested in production.

## 4.20. SDIO characteristics

**Table 4-38. SDIO characteristics(1)(2)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{PP}$(3) | Clock frequency in data transfer mode | — | 0 | — | 48 | MHz |
| $t_{W(CKL)}$ (3) | Clock low time | $f_{pp}$ = 48 MHz | 9.5 | 10.5 | — | ns |
| $t_{W(CKH)}$ (3) | Clock high time | $f_{pp}$ = 48 MHz | 9.3 | 10.3 | — | ns |
| CMD, D inputs (referenced to CK) in MMC and SD HS mode | | | | | | |
| $t_{ISU}$(4) | Input setup time HS | $f_{pp}$ = 48 MHz | 4 | — | — | ns |
| $t_{IH}$(4) | Input hold time HS | $f_{pp}$ = 48 MHz | 3 | — | — | ns |
| CMD, D outputs (referenced to CK) in MMC and SD HS mode | | | | | | |
| $t_{OV}$(3) | Output valid time HS | $f_{pp}$ = 48 MHz | — | — | 13.8 | ns |
| $t_{OH}$(3) | Output hold time HS | $f_{pp}$ = 48 MHz | 12 | — | — | ns |
| CMD, D inputs (referenced to CK) in SD default mode | | | | | | |
| $t_{ISUD}$(4) | Input setup time SD | $f_{pp}$ = 24 MHz | 3 | — | — | ns |
| $t_{IHD}$(4) | Input hold time SD | $f_{pp}$ = 24 MHz | 3 | — | — | ns |
| CMD, D outputs (referenced to CK) in SD default mode | | | | | | |
| $t_{OVD}$(3) | Output valid default time SD | $f_{pp}$ = 24 MHz | — | 2.4 | 2.8 | ns |
| $t_{OHD}$(3) | Output hold default time SD | $f_{pp}$ = 24 MHz | 2 | — | — | ns |

(1) CLK timing is measured at 50% of $V_{DD}$.
(2) Capacitive load $C_L$ = 30 pF.
(3) Based on characterization, not tested in production.
(4) Guaranteed by design, not tested in production.

## 4.21. CAN characteristics

Refer to ***Table 4-26.*** for more details on the input/output alternate function characteristics (CANTX and CANRX).



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## 4.22. USBFS characteristics

**Table 4-39. USBFS start up time**

| Symbol | Parameter | Max | Unit |
|---|---|---|---|
| $t_{STARTUP}$(1) | USBFS startup time | 1 | μs |

(1) Guaranteed by design, not tested in production.

**Table 4-40. USBFS DC electrical characteristics**

| Symbol | | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Input levels(1) | $V_{DD}$ | USBFS operating voltage | — | 3 | — | 3.6 | V |
| | $V_{DI}$ | Differential input sensitivity | — | 0.2 | — | — | V |
| | $V_{CM}$ | Differential common mode range | Includes $V_{DI}$ range | 0.8 | — | 2.5 | |
| | $V_{SE}$ | Single ended receiver threshold | — | 1.3 | — | 2.0 | |
| Output levels (2) | $V_{OL}$ | Static output level low | $R_L$ of 1.0 kΩ to 3.6 V | — | 0.06 | 0.3 | V |
| | $V_{OH}$ | Static output level high | $R_L$ of 15 kΩ to $V_{SS}$ | 2.8 | 3.3 | 3.6 | |
| $R_{PD}$(2) | | PA11, PA12(USBFS_DM/DP)<br>PB14, PB15(USBHS_ DM/DP) | $V_{IN}$ = $V_{DD}$ | 17 | 21 | 25 | kΩ |
| | | PA9(USBFS_VBUS)<br>PB13(USBHS_VBUS) | | 0.72 | 0.9 | 1.1 | |
| $R_{PU}$(2) | | PA11, PA12(USBFS_DM/DP)<br>PB14, PB15(USBHS_ DM/DP) | $V_{IN}$ = $V_{SS}$ | 1.2 | 1.5 | 1.8 | |
| | | PA9(USBFS_VBUS)<br>PB13(USBHS_VBUS) | | 0.24 | 0.3 | 0.33 | |

(1) Guaranteed by design, not tested in production.

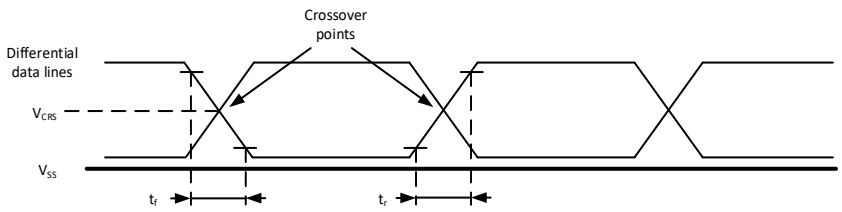
(2) Based on characterization, not tested in production.

**Table 4-41. USBFS full speed-electrical characteristics(1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_R$ | Rise time | $C_L$ = 50 pF | 4 | — | 20 | ns |
| $t_F$ | Fall time | $C_L$ = 50 pF | 4 | — | 20 | ns |
| $t_{RFM}$ | Rise / fall time matching | $t_R$ / $t_F$ | 90 | — | 110 | % |
| $V_{CRS}$ | Output signal crossover voltage | — | 1.3 | — | 2.0 | V |

(1) Guaranteed by design, not tested in production.

**Figure 4-11. USBFS timings: definition of data signal rise and fall time**






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## 4.23. USBHS characteristics

**Table 61. USBHS clock timing parameters(1)**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | USBHS operating voltage | 3.0 | — | 3.6 | V |
| $f_{HCLK}$ | $f_{HCLK}$ value to guarantee proper operation of USBHS interface | 30 | — | — | MHz |
| $F_{START_8BIT}$ | Frequency (first transition) 8-bit ± 10% | 54 | 60 | 66 | MHz |
| $F_{STEADY}$ | Frequency (steady state) ±500 ppm | 59.97 | 60 | 60.63 | MHz |
| $D_{START_8BIT}$ | Duty cycle (first transition) 8-bit ± 10% | 40 | 50 | 60 | % |
| $D_{STEADY}$ | Duty cycle (steady state) ±500 ppm | 49.975 | 50 | 50.025 | % |

(1) Guaranteed by design, not tested in production.

**Table 62. USB-ULPI Dynammic characteristics**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{SC}$ | Control in (ULPI_DIR, ULPI_NXT) setup time | — | — | 2 | ns |
| $t_{HC}$ | Control in (ULPI_DIR, ULPI_NXT) hold time | 0.5 | — | — | ns |
| $t_{SD}$ | Data in setup time | — | — | 2 | ns |
| $t_{HD}$ | Data in hold time | 0 | — | — | ns |

(1) Guaranteed by design, not tested in production.

## 4.24. TIMER characteristics

**Table 4-42. TIMER characteristics(1)**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $t_{res}$ | Timer resolution time | — | 1 | — | $t_{TIMERxCLK}$ |
| | | $f_{TIMERxCLK}$ = 200 MHz | 5 | — | ns |
| $f_{EXT}$ | Timer external clock frequency | — | 0 | $f_{TIMERxCLK}/2$ | MHz |
| | | $f_{TIMERxCLK}$ = 200 MHz | 0 | 100 | MHz |
| RES | Timer resolution | TIMERx (except TIMER1 & TIMER4) | — | 16 | bit |
| | | TIMER1 & TIMER4 | — | 32 | bit |
| $t_{COUNTER}$ | 16-bit counter clock period when internal clock is selected | — | 1 | 65536 | $t_{TIMERxCLK}$ |
| | | $f_{TIMERxCLK}$ = 200 MHz | 0.005 | 327.68 | μs |
| $t_{MAX_COUNT}$ | Maximum possible count | — | — | 65536x65536 | $t_{TIMERxCLK}$ |
| | | $f_{TIMERxCLK}$ = 200 MHz | — | 21.47 | s |

(1) Guaranteed by design, not tested in production.



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## 4.25. DCI characteristics

**Table 4-43. DCI characteristics(1)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| Frequency ratio | DCI_PIXCLK /fHCLK | — | 0.4 | — |
| DCI_PIXCLK | Pixel clock input | — | 80 | MHz |
| DPixel | Pixel clock input duty cycle | 30 | 70 | % |
| tsu(DATA) | Data input setup time | 2.5 | — | ns |
| th(DATA) | Data output valid time | 1 | — | ns |
| tsu(HS) | DCI_HS input setup time | 2 | — | ns |
| tsu(VS) | DCI_VS input setup time | 2 | — | ns |
| th(HS) | DCI_HS input hold time | 0.5 | — | ns |
| th(VS) | DCI_VS input hold time | 0.5 | — | ns |

(1) Guaranteed by design, not tested in production.

## 4.26. WDGT characteristics

**Table 4-44. FWDGT min/max timeout period at 32 kHz (IRC32K)(1)**

| Prescaler divider | PSC[2:0] bits | Min timeout RLD[11:0] = 0x000 | Max timeout RLD[11:0] = 0xFFF | Unit |
|---|---|---|---|---|
| 1/4 | 000 | 0.03125 | 511.90625 | ms |
| 1/8 | 001 | 0.03125 | 1023.7812 | |
| 1/16 | 010 | 0.03125 | 2047.53125 | |
| 1/32 | 011 | 0.03125 | 4095.03125 | |
| 1/64 | 100 | 0.03125 | 8190.03125 | |
| 1/128 | 101 | 0.03125 | 16380.03125 | |
| 1/256 | 110 or 111 | 0.03125 | 32760.03125 | |

(1) Guaranteed by design, not tested in production.

**Table 4-45. WWDGT min-max timeout value at 50 MHz ($f_{PCLK1}$)(1)**

| Prescaler divider | PSC[1:0] | Min timeout value CNT[6:0] = 0x40 | Unit | Max timeout value CNT[6:0] = 0x7F | Unit |
|---|---|---|---|---|---|
| 1/1 | 00 | 81.92 | µs | 5.24 | ms |
| 1/2 | 01 | 163.84 | | 10.48 | |
| 1/4 | 10 | 327.68 | | 20.96 | |
| 1/8 | 11 | 655.36 | | 41.92 | |

(1) Guaranteed by design, not tested in production.

## 4.27. Parameter conditions

Unless otherwise specified, all values given for $V_{DD}$ = $V_{DDA}$ = 3.3 V, $T_A$ = 25 °C.



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# 5. Package information

## 5.1. LQFP144 package outline dimensions

**Figure 5-1. LQFP144 package outline**

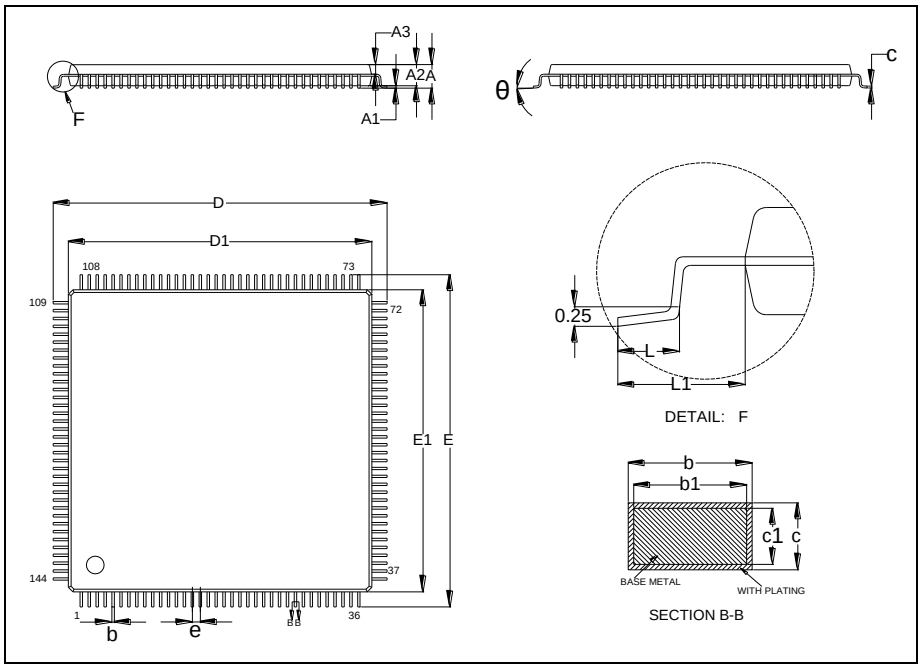



**Table 5-1. LQFP144 package dimensions**

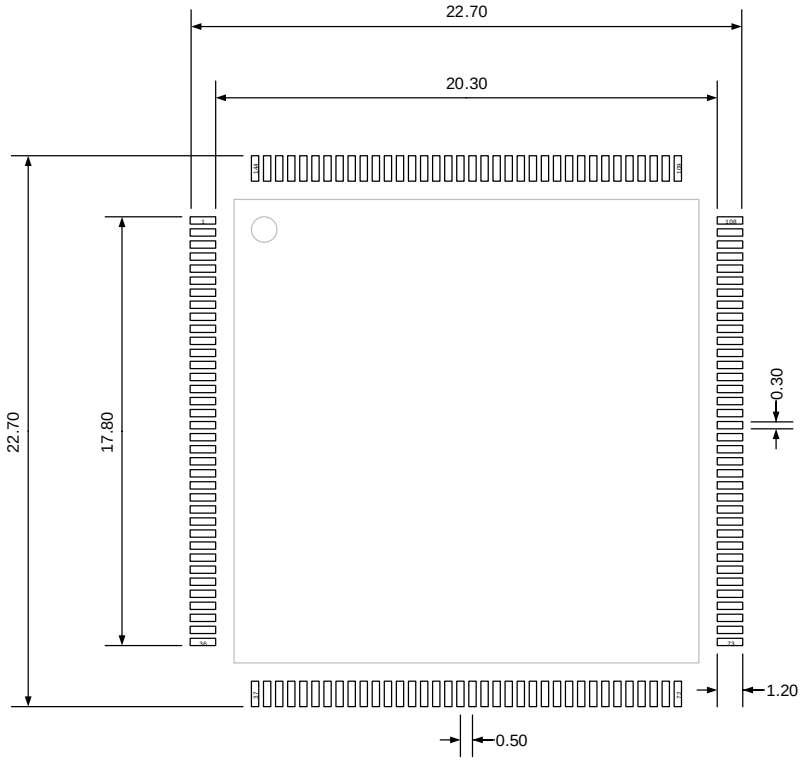
| Symbol | Min | Typ | Max |
|---|---|---|---|
| A | — | — | 1.60 |
| A1 | 0.05 | — | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 |
| A3 | 0.59 | 0.64 | 0.69 |
| b | 0.18 | — | 0.26 |
| b1 | 0.17 | 0.20 | 0.23 |
| c | 0.13 | — | 0.17 |
| c1 | 0.12 | 0.13 | 0.14 |
| D | 21.80 | 22.00 | 22.20 |
| D1 | 19.90 | 20.00 | 20.10 |
| E | 21.80 | 22.00 | 22.20 |
| E1 | 19.90 | 20.00 | 20.10 |
| e | — | 0.50 | — |
| L | 0.45 | — | 0.75 |
| L1 | — | 1.00 | — |
| θ | 0° | — | 7° |

(Original dimensions are in millimeters)



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**Figure 5-2. LQFP144 recommended footprint**




(Original dimensions are in millimeters



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## 5.2. BGA100 package outline dimensions

**Figure 5-3. BGA100 package outline**

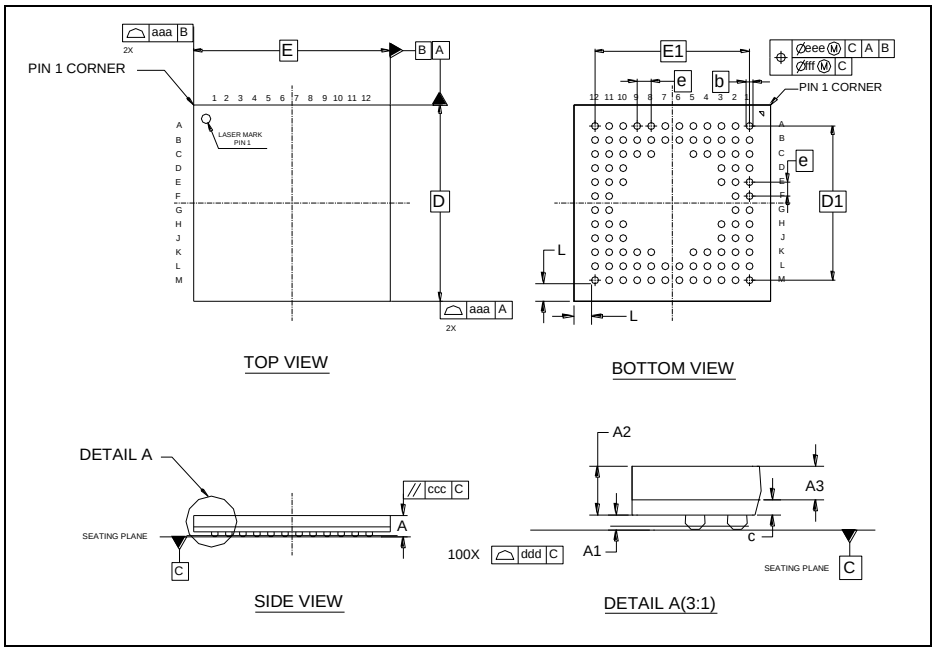



**Table 5-2. BGA100 package dimensions**

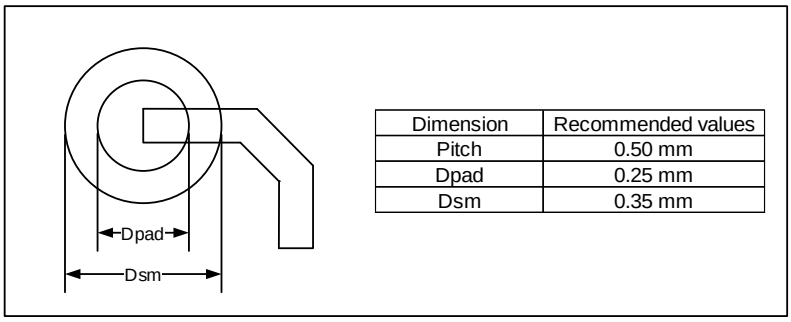
| Symbol | Min | Typ | Max |
|---|---|---|---|
| A | — | — | 0.84 |
| A1 | 0.13 | 0.18 | 0.23 |
| A2 | 0.53 | 0.58 | 0.63 |
| A3 | — | 0.40 | — |
| b | 0.20 | 0.25 | 0.30 |
| c | 0.15 | 0.18 | 0.21 |
| D | 6.90 | 7.00 | 7.10 |
| D1 | — | 5.50 | — |
| E | 6.90 | 7.00 | 7.10 |
| E1 | — | 5.50 | — |
| e | — | 0.50 | — |
| L | — | 0.625 | — |
| aaa | — | 0.10 | — |
| ccc | — | 0.20 | — |
| ddd | — | 0.08 | — |
| eee | — | 0.15 | — |
| fff | — | 0.08 | — |

(Original dimensions are in millimeters)



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**Figure 5-4. BGA100 recommended footprint**




| Dimension | Recommended values |
|---|---|
| Pitch | 0.50 mm |
| Dpad | 0.25 mm |
| Dsm | 0.35 mm |

(Original dimensions are in millimeters)



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## 5.3. LQFP100 package outline dimensions

**Figure 5-5. LQFP100 package outline**

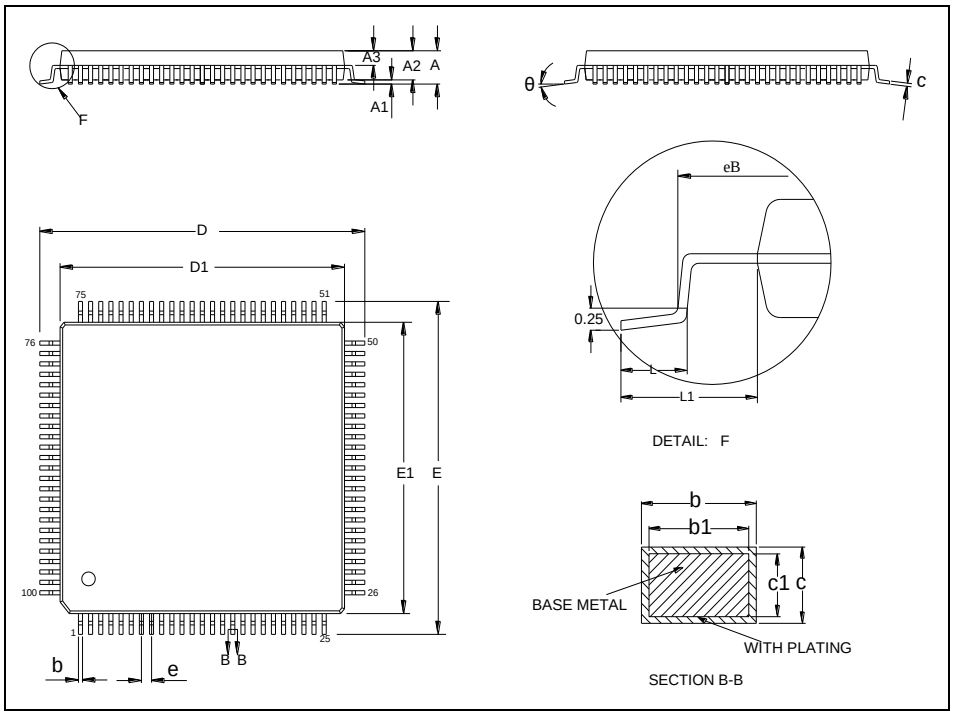



**Table 5-3. LQFP100 package dimensions**

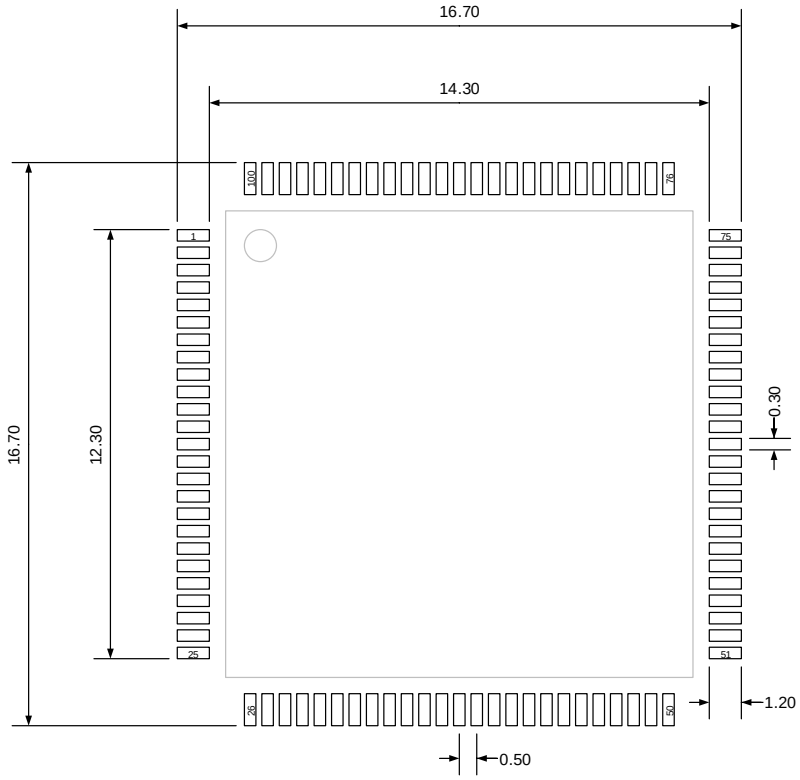
| Symbol | Min | Typ | Max |
|---|---|---|---|
| A | — | — | 1.60 |
| A1 | 0.05 | — | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 |
| A3 | 0.59 | 0.64 | 0.69 |
| b | 0.18 | — | 0.26 |
| b1 | 0.17 | 0.20 | 0.23 |
| c | 0.13 | — | 0.17 |
| c1 | 0.12 | 0.13 | 0.14 |
| D | 15.80 | 16.00 | 16.20 |
| D1 | 13.90 | 14.00 | 14.10 |
| E | 15.80 | 16.00 | 16.20 |
| E1 | 13.90 | 14.00 | 14.10 |
| e | — | 0.50 | — |
| eB | 15.05 | — | 15.35 |
| L | 0.45 | — | 0.75 |
| L1 | — | 1.00 | — |
| θ | 0° | — | 7° |

(Original dimensions are in millimeters)



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**Figure 5-6. LQFP100 recommended footprint**




(Original dimensions are in millimeters)



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## 5.4. LQFP64 package outline dimensions

**Figure 5-7. LQFP64 package outline**

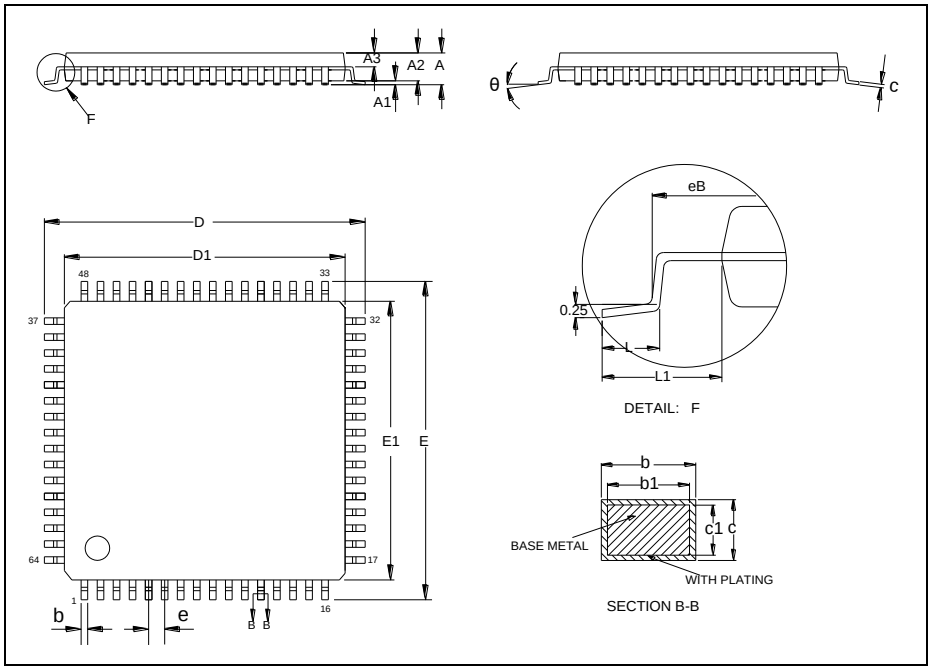



**Table 5-4. LQFP64 package dimensions**

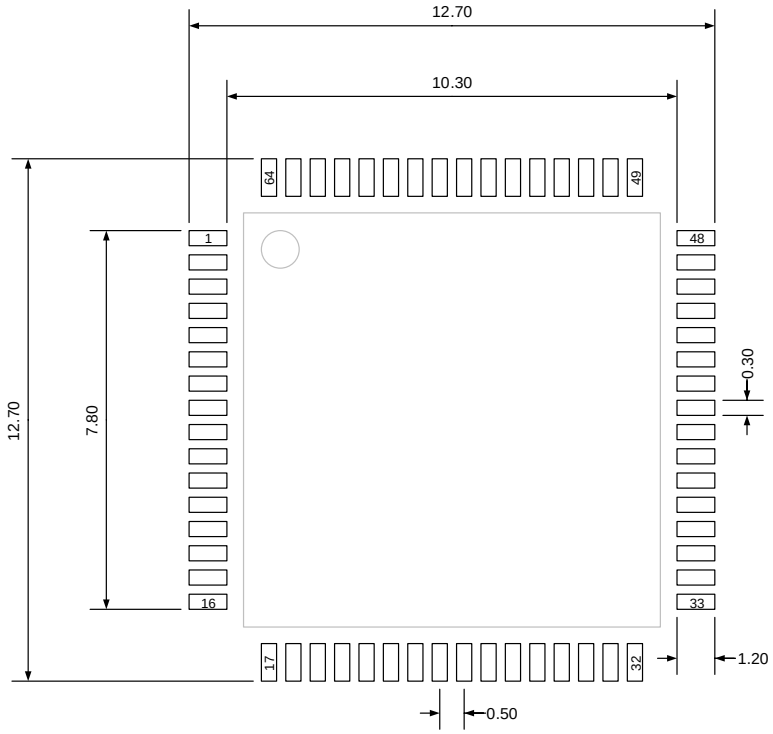
| Symbol | Min | Typ | Max |
|---|---|---|---|
| A | — | — | 1.60 |
| A1 | 0.05 | — | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 |
| A3 | 0.59 | 0.64 | 0.69 |
| b | 0.18 | — | 0.26 |
| b1 | 0.17 | 0.20 | 0.23 |
| c | 0.13 | — | 0.17 |
| c1 | 0.12 | 0.13 | 0.14 |
| D | 11.80 | 12.00 | 12.20 |
| D1 | 9.90 | 10.00 | 10.10 |
| E | 11.80 | 12.00 | 12.20 |
| E1 | 9.90 | 10.00 | 10.10 |
| e | — | 0.50 | — |
| eB | 11.25 | — | 11.45 |
| L | 0.45 | — | 0.75 |
| L1 | — | 1.00 | — |
| θ | 0° | — | 7° |

(Original dimensions are in millimeters)



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**Figure 5-8. LQFP64 recommended footprint**




(Original dimensions are in millimeters)



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## 5.5. Thermal characteristics

Thermal resistance is used to characterize the thermal performance of the package device, which is represented by the Greek letter “θ”. For semiconductor devices, thermal resistance represents the steady-state temperature rise of the chip junction due to the heat dissipated on the chip surface.

$\theta_{JA}$: Thermal resistance, junction-to-ambient.

$\theta_{JB}$: Thermal resistance, junction-to-board.

$\theta_{JC}$: Thermal resistance, junction-to-case.

$\Psi_{JB}$: Thermal characterization parameter, junction-to-board.

$\Psi_{JT}$: Thermal characterization parameter, junction-to-top center.

$$\theta_{JA}=(T_J-T_A)/P_D \quad (5\text{-}1)$$

$$\theta_{JB}=(T_J-T_B)/P_D \quad (5\text{-}2)$$

$$\theta_{JC}=(T_J-T_C)/P_D \quad (5\text{-}3)$$

Where, $T_J$ = Junction temperature.

$T_A$ = Ambient temperature

$T_B$ = Board temperature

$T_C$ = Case temperature which is monitoring on package surface

$P_D$ = Total power dissipation

$\theta_{JA}$ represents the resistance of the heat flows from the heating junction to ambient air. It is an indicator of package heat dissipation capability. Lower $\theta_{JA}$ can be considerate as better overall thermal performance. $\theta_{JA}$ is generally used to estimate junction temperature.

$\theta_{JB}$ is used to measure the heat flow resistance between the chip surface and the PCB board.

$\theta_{JC}$ represents the thermal resistance between the chip surface and the package top case. $\theta_{JC}$ is mainly used to estimate the heat dissipation of the system (using heat sink or other heat dissipation methods outside the device package).

**Table 5-5. Package thermal characteristics(1)**

| Symbol | Condition | Package | Value | Unit |
|---|---|---|---|---|
| $\theta_{JA}$ | Natural convection, 2S2P PCB | LQFP144 | 48.76 | °C/W |
| | | BGA100 | 78.32 | |
| | | LQFP100 | 57.42 | |
| | | LQFP64 | 51.81 | |
| $\theta_{JB}$ | Cold plate, 2S2P PCB | LQFP144 | 35.00 | °C/W |
| | | BGA100 | 55.27 | |
| | | LQFP100 | 31.68 | |



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| Symbol | Condition | Package | Value | Unit |
|---|---|---|---|---|
| | | LQFP64 | 33.36 | |
| $\theta_{JC}$ | Cold plate, 2S2P PCB | LQFP144 | 12.03 | °C/W |
| | | BGA100 | 20.15 | |
| | | LQFP100 | 13.85 | |
| | | LQFP64 | 11.25 | |
| $\Psi_{JB}$ | Natural convection, 2S2P PCB | LQFP144 | 35.32 | °C/W |
| | | BGA100 | 55.74 | |
| | | LQFP100 | 41.28 | |
| | | LQFP64 | 33.53 | |
| $\Psi_{JT}$ | Natural convection, 2S2P PCB | LQFP144 | 1.86 | °C/W |
| | | BGA100 | 1.74 | |
| | | LQFP100 | 0.75 | |
| | | LQFP64 | 0.49 | |

(1) Thermal characteristics are based on simulation, and meet JEDEC specification.



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# 6. Ordering information

**Table 6-1. Part ordering code for GD32F425xx devices**

| Ordering code | Flash (KB) | Package | Package type | Temperature operating range |
|---|---|---|---|---|
| GD32F425ZKT6 | 3072 | LQFP144 | Green | Industrial -40°C to +85°C |
| GD32F425ZGT6 | 1024 | LQFP144 | Green | Industrial -40°C to +85°C |
| GD32F425VKH6 | 3072 | BGA100 | Green | Industrial -40°C to +85°C |
| GD32F425VGH6 | 1024 | BGA100 | Green | Industrial -40°C to +85°C |
| GD32F425VKT6 | 3072 | LQFP100 | Green | Industrial -40°C to +85°C |
| GD32F425VGT6 | 1024 | LQFP100 | Green | Industrial -40°C to +85°C |
| GD32F425RKT6 | 3072 | LQFP64 | Green | Industrial -40°C to +85°C |
| GD32F425RGT6 | 1024 | LQFP64 | Green | Industrial -40°C to +85°C |
| GD32F425RET6 | 512 | LQFP64 | Green | Industrial -40°C to +85°C |



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# 7. Revision history

**Table 7-1. Revision history**

| Revision No. | Description | Date |
|---|---|---|
| 1.0 | Initial Release | Feb. 22, 2022 |
| 1.1 | 1. Add ***Figure 7-1. Recommended PDR_ON pin circuit*** in chapter ***4.5. Power supply supervisor characteristics***.<br>2. Add description of EMI in chapter ***4.4. EMC characteristics***.<br>3. Modify the BGA100 and BGA64 footprint parameters in chapter ***5. Package information***.<br>4. Mofidy the I2C timing parameters in ***4.16. I2C characteristics***.<br>5. Modify $f_{sck}$ maximum value in ***Table 4 37. USART characteristics(1)***.<br>6. Modify the erase cycles in ***Table 4 24. Flash memory characteristics***.<br>7. Modify the value of $V_{ESD(HBM)}$ and $V_{ESD(CDM)}$ in ***Table 4 11. ESD characteristics(1)***. | May.24, 2022 |



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