GigaDevice Semiconductor Inc.

GD32F405xx
ARM® Cortex®-M4 32-bit MCU

Datasheet

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Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com
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1 Introduction

The GD32F405xx device belongs to the connectivity line of GD32 MCU Family. It is a new 32-bit general-purpose microcontroller based on the ARM® Cortex®-M4 RISC core with best cost-performance ratio in terms of enhanced processing capacity, reduced power consumption and peripheral set. The Cortex®-M4 core features a Floating Point Unit (FPU) that accelerates single precision floating point math operations and supports all ARM® single precision instructions and data types. It implements a full set of DSP instructions to address digital signal control markets that demand an efficient, easy-to-use blend of control and signal processing capabilities. It also provides a Memory Protection Unit (MPU) and powerful trace technology for enhanced application security and advanced debug support.

The GD32F405xx device incorporates the ARM® Cortex®-M4 32-bit processor core operating at 168 MHz frequency with Flash accesses zero wait states to obtain maximum efficiency. It provides up to 3072 KB on-chip Flash memory and 192 KB SRAM memory. An extensive range of enhanced I/Os and peripherals connected to two APB buses. The devices offer up to three 12-bit 2.6M SPS ADCs, two 12-bit DACs, up to eight general-purpose 16-bit timers, two 16-bit PWM advanced-control timers , two 32-bit general-purpose timers, and two 16-bit basic timers, as well as standard and advanced communication interfaces: up to three SPIs, three I2Cs, four USARTs and two UARTs, two I2Ss, two CANs, a SDIO, USB device/host/OTG FS and HS. Additional peripherals as Digital camera interface (DCI) is included.

The device operates from a 2.6 to 3.6V power supply and available in –40 to +85 °C temperature range. Three power saving modes provide the flexibility for maximum optimization of power consumption, an especially important consideration in low power applications.

The above features make GD32F405xx devices suitable for a wide range of interconnection and advanced applications, especially in areas such as industrial control, consumer and handheld equipment, embedded modules, human machine interface, security and alarm systems, graphic display, automotive navigation, drone, IoT and so on.



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2 Device overview

2.1 Device information

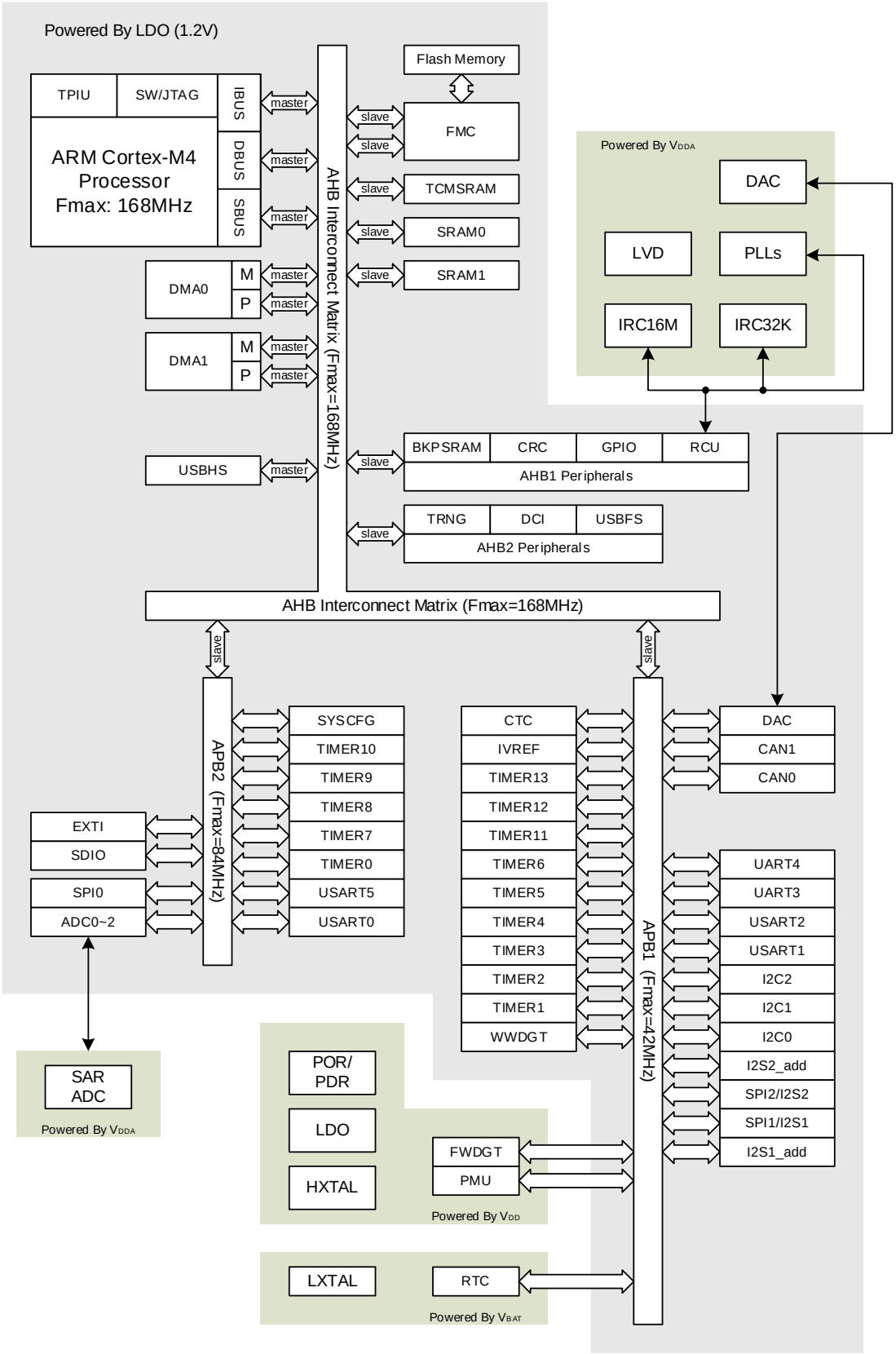
Table 1. GD32F405xx devices features and peripheral list

Part Number		GD32F405xx								
		RE	RG	RK	VG	VK	VG	VK	ZG	ZK
Flash	Code Area (KB)	512	512	512	512	512	512	512	512	512
	Data Area (KB)	0	512	2560	512	2560	512	2560	512	2560
	Total (KB)	512	1024	3072	1024	3072	1024	3072	1024	3072
SRAM (KB)		192	192	192	192	192	192	192	192	192
Timers	16-bit GPTM	8	8	8	8	8	8	8	8	8
	32-bit GPTM	2	2	2	2	2	2	2	2	2
	Adv. 16-bit TM	2	2	2	2	2	2	2	2	2
	Basic TM	2	2	2	2	2	2	2	2	2
	SysTick	1	1	1	1	1	1	1	1	1
	Watchdog	2	2	2	2	2	2	2	2	2
	RTC	1	1	1	1	1	1	1	1	1
Connectivity	USART+UART	4+2	4+2	4+2	4+2	4+2	4+2	4+2	4+2	4+2
	I2C	3	3	3	3	3	3	3	3	3
	SPI/I2S	3/2	3/2	3/2	3/2	3/2	3/2	3/2	3/2	3/2
	SDIO	1	1	1	1	1	1	1	1	1
	CAN 2.0B	2	2	2	2	2	2	2	2	2
	USB OTG	FS+HS	FS+HS	FS+HS	FS+HS	FS+HS	FS+HS	FS+HS	FS+HS	FS+HS
	Digital Camera	1	1	1	1	1	1	1	1	1
GPIO		51	51	51	82	82	82	82	114	114
ADC Unit (CHs)		3(16)	3(16)	3(16)	3(16)	3(16)	3(16)	3(16)	3(24)	3(24)
DAC		2	2	2	2	2	2	2	2	2
Package		LQFP64			LQFP100		BGA100		LQFP144	

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2.2 Block diagram

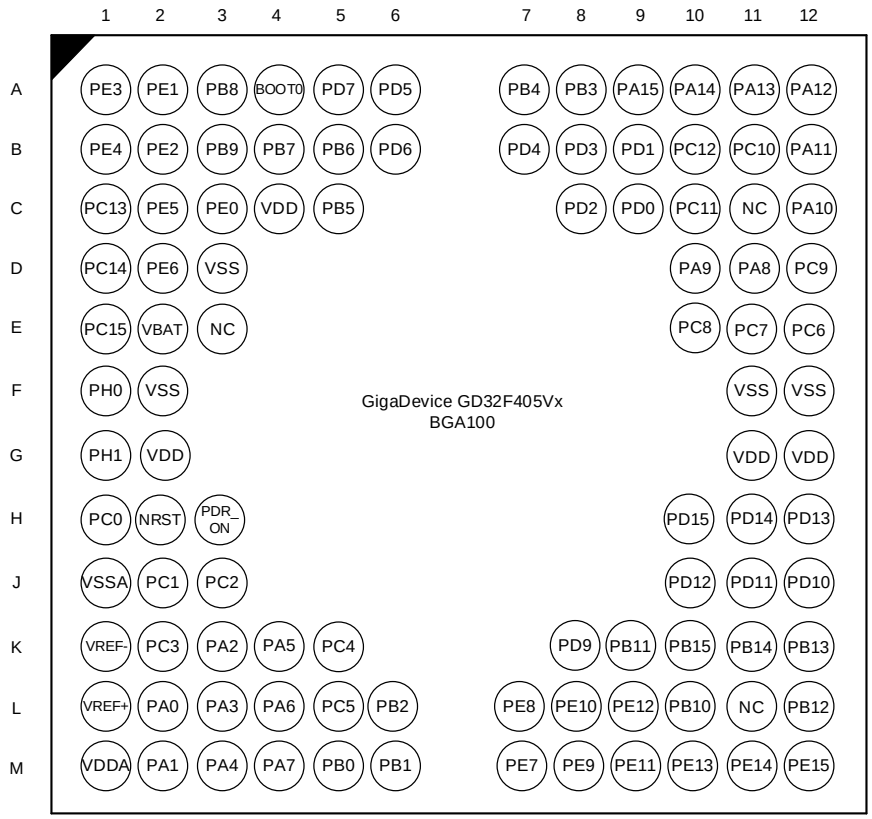
Figure 1. GD32F405xx block diagram



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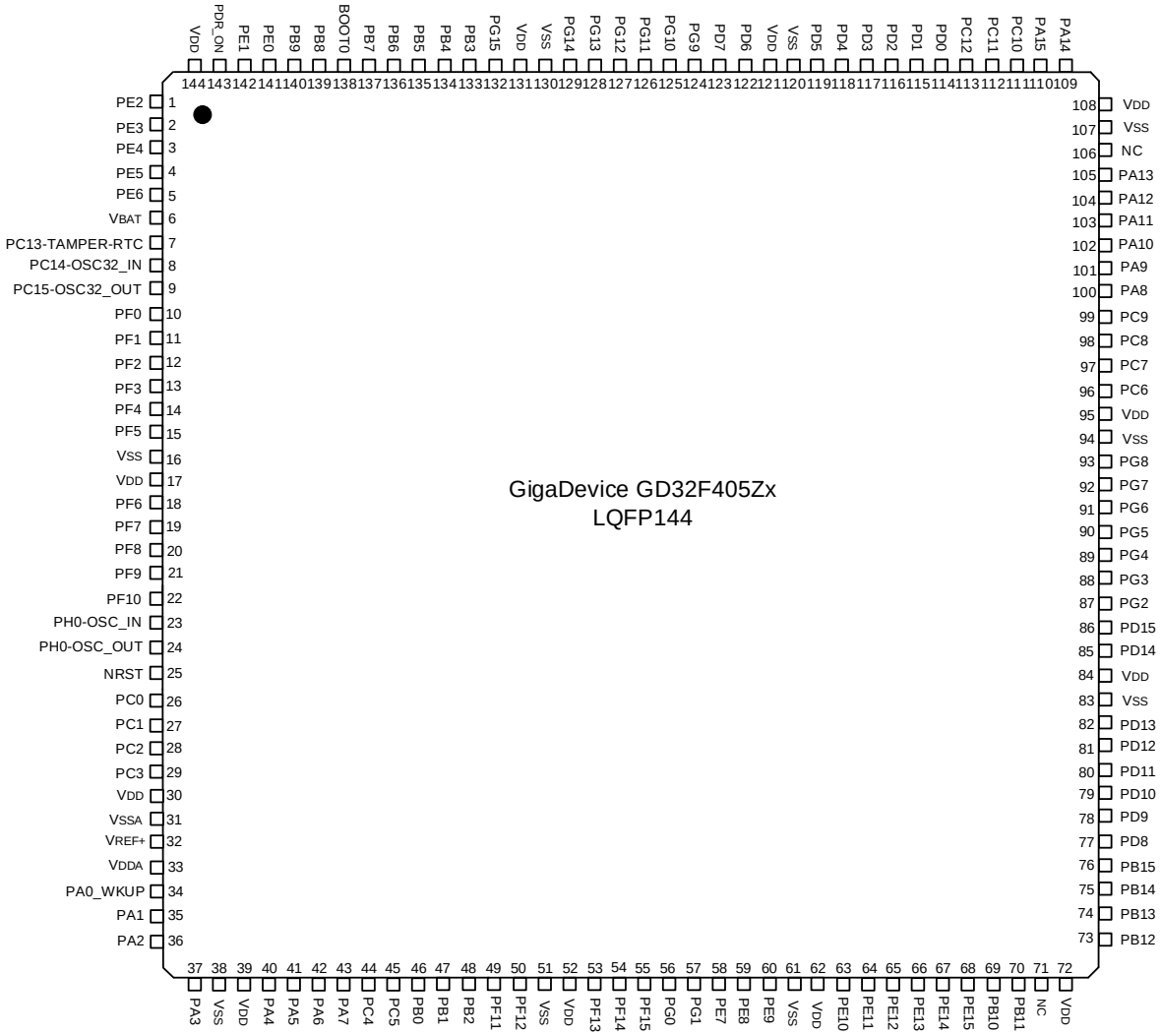
2.3 Pinouts and pin assignment

Figure 2. GD32F405Vx BGA100 pinouts



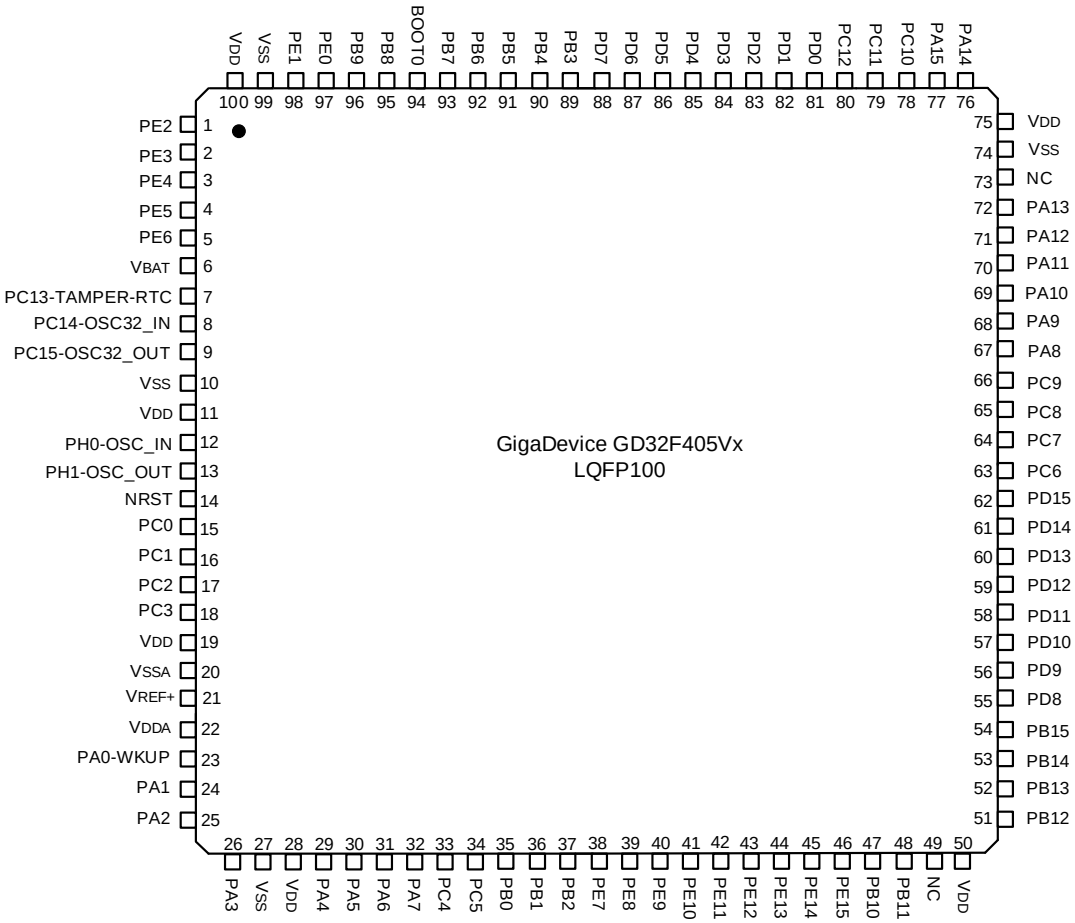
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Figure 3. GD32F405Zx LQFP144 pinouts



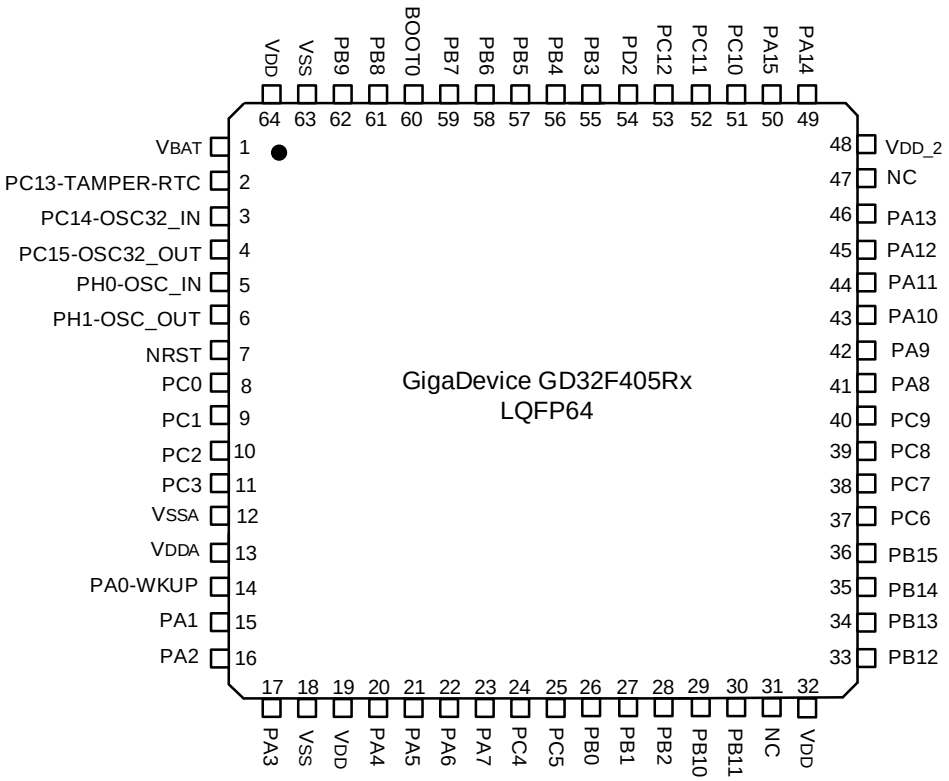
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Figure 4. GD32F405Vx LQFP100 pinouts



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Figure 5. GD32F405Rx LQFP64 pinouts



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2.4 Memory map

Figure 6. GD32F405xx memory map

Pre-defined Regions	Bus	Address	Peripherals
External Device	AHB matrix	0xC000 0000 - 0xDFFF FFFF	EXMC - SDRAM
		0xA000 1000 - 0xBFFF FFFF	Reserved
		0xA000 0000 - 0xA000 0FFF	Reserved
External RAM		0x9000 0000 - 0x9FFF FFFF	Reserved
		0x7000 0000 - 0x8FFF FFFF	Reserved
		0x6000 0000 - 0x6FFF FFFF	Reserved
Peripheral	AHB2	0x5006 0C00 - 0x5FFF FFFF	Reserved
		0x5006 0800 - 0x5006 0BFF	TRNG
		0x5005 0400 - 0x5006 07FF	Reserved
		0x5005 0000 - 0x5005 03FF	DCI
		0x5004 0000 - 0x5004 FFFF	Reserved
		0x5000 0000 - 0x5003 FFFF	USBFS
	AHB1	0x4008 0000 - 0x4FFF FFFF	Reserved
		0x4004 0000 - 0x4007 FFFF	USBHS
		0x4002 BC00 - 0x4003 FFFF	Reserved
		0x4002 B000 - 0x4002 BBFF	Reserved
		0x4002 A000 - 0x4002 AFFF	Reserved
		0x4002 8000 - 0x4002 9FFF	Reserved
		0x4002 6800 - 0x4002 7FFF	Reserved
		0x4002 6400 - 0x4002 67FF	DMA1
		0x4002 6000 - 0x4002 63FF	DMA0
		0x4002 5000 - 0x4002 5FFF	Reserved
		0x4002 4000 - 0x4002 4FFF	BKPSRAM
		0x4002 3C00 - 0x4002 3FFF	FMC
		0x4002 3800 - 0x4002 3BFF	RCU
		0x4002 3400 - 0x4002 37FF	Reserved
		0x4002 3000 - 0x4002 33FF	CRC
		0x4002 2400 - 0x4002 2FFF	Reserved
		0x4002 2000 - 0x4002 23FF	GPIOI
		0x4002 1C00 - 0x4002 1FFF	GPIOH
		0x4002 1800 - 0x4002 1BFF	GPIOG
		0x4002 1400 - 0x4002 17FF	GPIOF
		0x4002 1000 - 0x4002 13FF	GPIOE
		0x4002 0C00 - 0x4002 0FFF	GPIOD
		0x4002 0800 - 0x4002 0BFF	GPIOC
		0x4002 0400 - 0x4002 07FF	GPIOB
		0x4002 0000 - 0x4002 03FF	GPIOA

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Pre-defined Regions	Bus	Address	Peripherals
	APB2	0x4001 6C00 - 0x4001 FFFF	Reserved
		0x4001 6800 - 0x4001 6BFF	Reserved
		0x4001 5800 - 0x4001 67FF	Reserved
		0x4001 5400 - 0x4001 57FF	Reserved
		0x4001 5000 - 0x4001 53FF	Reserved
		0x4001 4C00 - 0x4001 4FFF	Reserved
		0x4001 4800 - 0x4001 4BFF	TIMER10
		0x4001 4400 - 0x4001 47FF	TIMER9
		0x4001 4000 - 0x4001 43FF	TIMER8
		0x4001 3C00 - 0x4001 3FFF	EXTI
		0x4001 3800 - 0x4001 3BFF	SYSCFG
		0x4001 3400 - 0x4001 37FF	Reserved
		0x4001 3000 - 0x4001 33FF	SPI0
		0x4001 2C00 - 0x4001 2FFF	SDIO
		0x4001 2400 - 0x4001 2BFF	Reserved
		0x4001 2000 - 0x4001 23FF	ADC
		0x4001 1800 - 0x4001 1FFF	Reserved
		0x4001 1400 - 0x4001 17FF	USART5
		0x4001 1000 - 0x4001 13FF	USART0
		0x4001 0800 - 0x4001 0FFF	Reserved
		0x4001 0400 - 0x4001 07FF	TIMER7
		0x4001 0000 - 0x4001 03FF	TIMER0
	APB1	0x4000 C800 - 0x4000 FFFF	Reserved
		0x4000 C400 - 0x4000 C7FF	IVREF
		0x4000 8000 - 0x4000 C3FF	Reserved
		0x4000 7C00 - 0x4000 7FFF	Reserved
		0x4000 7800 - 0x4000 7BFF	Reserved
		0x4000 7400 - 0x4000 77FF	DAC
		0x4000 7000 - 0x4000 73FF	PMU
		0x4000 6C00 - 0x4000 6FFF	CTC
		0x4000 6800 - 0x4000 6BFF	CAN1
		0x4000 6400 - 0x4000 67FF	CAN0
		0x4000 6000 - 0x4000 63FF	Reserved
		0x4000 5C00 - 0x4000 5FFF	I2C2
		0x4000 5800 - 0x4000 5BFF	I2C1
		0x4000 5400 - 0x4000 57FF	I2C0
		0x4000 5000 - 0x4000 53FF	UART4
		0x4000 4C00 - 0x4000 4FFF	UART3
		0x4000 4800 - 0x4000 4BFF	USART2
		0x4000 4400 - 0x4000 47FF	USART1

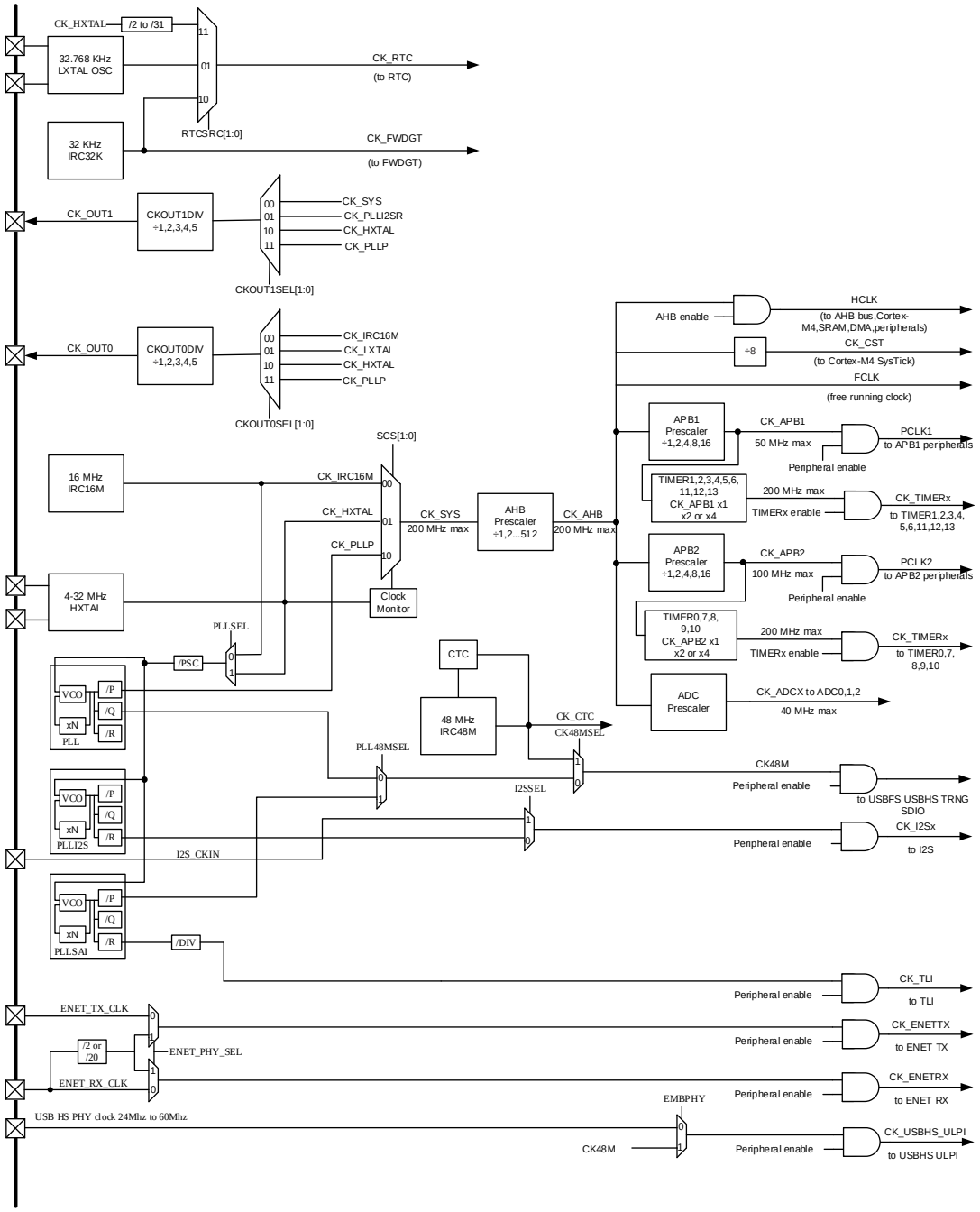
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Pre-defined Regions	Bus	Address	Peripherals
		0x4000 4000 - 0x4000 43FF	I2S2_add
		0x4000 3C00 - 0x4000 3FFF	SPI2/I2S2
		0x4000 3800 - 0x4000 3BFF	SPI1/I2S1
		0x4000 3400 - 0x4000 37FF	I2S1_add
		0x4000 3000 - 0x4000 33FF	FWDGT
		0x4000 2C00 - 0x4000 2FFF	WWDGT
		0x4000 2800 - 0x4000 2BFF	RTC
		0x4000 2400 - 0x4000 27FF	Reserved
		0x4000 2000 - 0x4000 23FF	TIMER13
		0x4000 1C00 - 0x4000 1FFF	TIMER12
		0x4000 1800 - 0x4000 1BFF	TIMER11
		0x4000 1400 - 0x4000 17FF	TIMER6
		0x4000 1000 - 0x4000 13FF	TIMER5
		0x4000 0C00 - 0x4000 0FFF	TIMER4
		0x4000 0800 - 0x4000 0BFF	TIMER3
		0x4000 0400 - 0x4000 07FF	TIMER2
		0x4000 0000 - 0x4000 03FF	TIMER1
SRAM	AHB matrix	0x2007 0000 - 0x3FFF FFFF	Reserved
		0x2003 0000 - 0x2006 FFFF	Reserved
		0x2002 0000 - 0x2002 FFFF	Reserved
		0x2001 C000 - 0x2001 FFFF	SRAM1(16KB)
		0x2000 0000 - 0x2001 BFFF	SRAM0(112KB)
Code	AHB matrix	0x1FFF C010 - 0x1FFF FFFF	Reserved
		0x1FFF C000 - 0x1FFF C00F	Option bytes(Bank 0)
		0x1FFF 7A10 - 0x1FFF BFFF	Reserved
		0x1FFF 7800 - 0x1FFF 7A0F	OTP(528B)
		0x1FFF 0000 - 0x1FFF 77FF	Boot loader(30KB)
		0x1FFE C010 - 0x1FFE FFFF	Reserved
		0x1FFE C000 - 0x1FFE C00F	Option bytes(Bank 1)
		0x1001 0000 - 0x1FFE BFFF	Reserved
		0x1000 0000 - 0x1000 FFFF	TCMSRAM(64KB)
		0x0830 0000 - 0x0FFF FFFF	Reserved
		0x0800 0000 - 0x082F FFFF	Main Flash(3072KB)
		0x0000 0000 - 0x07FF FFFF	Aliased to the boot device

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2.5 Clock tree

Figure 7. GD32F405xx clock tree



Legend:

HXTAL: High speed crystal oscillator

LXTAL: Low speed crystal oscillator

IRC16M: Internal 16M RC oscillators

IRC48M: Internal 48M RC oscillators

IRC32K: Internal 32K RC oscillator

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2.6 Pin definitions

Table 2. GD32F405xx pin definitions

Pin Name	Pins				Pin Type(1)	I/O(2) Level	Functions description
	BGA100	LQFP144	LQFP100	LQFP64			
PE2	B2	1	1	-	I/O	5VT	Default: PE2 Alternate: TRACECLK, EVENTOUT
PE3	A1	2	2	-	I/O	5VT	Default: PE3 Alternate:TRACED0, EVENTOUT
PE4	B1	3	3	-	I/O	5VT	Default: PE4 Alternate:TRACED1, DCI_D4, EVENTOUT
PE5	C2	4	4	-	I/O	5VT	Default: PE5 Alternate:TRACED2,TIMER8_CH0, DCI_D6, EVENTOUT
PE6	D2	5	5	-	I/O	5VT	Default: PE6 Alternate:TRACED3,TIMER8_CH1, DCI_D7, EVENTOUT
V_{BAT}	E2	6	6	1	P	-	Default: V_{BAT}
PC13-TAMPER-RTC	C1	7	7	2	I/O	5VT	Default: PC13 Alternate: EVENTOUT Additional: RTC_TAMP0, RTC_OUT, RTC_TS
PC14-OSC32IN	D1	8	8	3	I/O	5VT	Default: PC14 Alternate: EVENTOUT Additional: OSC32IN
PC15-OSC32OUT	E1	9	9	4	I/O	5VT	Default: PC15 Alternate: EVENTOUT Additional: OSC32OUT
PF0	-	10	-	-	I/O	5VT	Default: PF0 Alternate:I2C1_SDA, EVENTOUT, CTC_SYNC
PF1	-	11	-	-	I/O	5VT	Default: PF1 Alternate: I2C1_SCL, EVENTOUT
PF2	-	12	-	-	I/O	5VT	Default: PF2 Alternate: I2C1_SMBA, EVENTOUT
PF3	-	13	-	-	I/O	5VT	Default: PF3 Alternate: EVENTOUT, I2C1_TXFRAME Additional: ADC2_IN9
PF4	-	14	-	-	I/O	5VT	Default: PF4 Alternate: EVENTOUT Additional: ADC2_IN14
PF5	-	15	-	-	I/O	5VT	Default: PF5 Alternate: EVENTOUT Additional: ADC2_IN15

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Pin Name	Pins				Pin Type(1)	I/O(2) Level	Functions description
	BGA100	LQFP144	LQFP100	LQFP64			
V_{SS}	F2	16	10	-	P	-	Default: V_{SS}
V_{DD}	G2	17	11	-	P	-	Default: V_{DD}
PF6	-	18	-	-	I/O	5VT	Default: PF6 Alternate:TIMER9_CH0, EVENTOUT Additional: ADC2_IN4
PF7	-	19	-	-	I/O	5VT	Default: PF7 Alternate:TIMER10_CH0, EVENTOUT Additional: ADC2_IN5
PF8	-	20	-	-	I/O	5VT	Default: PF8 Alternate: TIMER12_CH0, EVENTOUT Additional: ADC2_IN6
PF9	-	21	-	-	I/O	5VT	Default: PF9 Alternate: TIMER13_CH0, EVENTOUT Additional: ADC2_IN7
PF10	-	22	-	-	I/O	5VT	Default: PF10 Alternate: DCI_D11, EVENTOUT Additional: ADC2_IN8
PH0	F1	23	12	5	I/O	5VT	Default: PH0, OSCIN Alternate: EVENTOUT Additional: OSCIN
PH1	G1	24	13	6	I/O	5VT	Default: PH1, OSCOUT Alternate: EVENTOUT Additional: OSCOUT
NRST	H2	25	14	7	-	-	Default: NRST
PC0	H1	26	15	8	I/O	5VT	Default: PC0 Alternate: USBHS_ULPI_STP, EVENTOUT Additional: ADC012_IN10
PC1	J2	27	16	9	I/O	5VT	Default: PC1 Alternate:SPI2_MOSI, I2S2_SD, SPI1_MOSI, I2S1_SD, EVENTOUT Additional: ADC012_IN11
PC2	J3	28	17	10	I/O	5VT	Default: PC2 Alternate:SPI1_MISO,I2S1_ADD_SD,USBHS_ULPI_DIR, EVENTOUT Additional: ADC012_IN12
PC3	K2	29	18	11	I/O	5VT	Default: PC3 Alternate:SPI1_MOSI,I2S1_SD,USBHS_ULPI_NXT, EVENTOUT Additional: ADC012_IN13
V_{DD}	-	30	19	-	P	-	Default: V_{DD}
V_{SSA}	J1	31	20	12	P	-	Default: V_{SSA}
V_{REFN}	K1	-	-	-	P	-	Default: V_{REF-}

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Pin Name	Pins				Pin Type(1)	I/O(2) Level	Functions description
	BGA100	LQFP144	LQFP100	LQFP64			
V_{REFP}	L1	32	21	-	P	-	Default: V_{REF+}
V_{DDA}	M1	33	22	13	P	-	Default: V_{DDA}
PA0-WKUP	L2	34	23	14	I/O	5VT	Default: PA0 Alternate:TIMER1_CH0,TIMER1_ETI,TIMER4_CH0, TIMER7_ETI,USART1_CTS, UART3_TX, EVENTOUT Additional: ADC012_IN0, WKUP
PA1	M2	35	24	15	I/O	5VT	Default: PA1 Alternate:TIMER1_CH1, TIMER4_CH1, USART1_RTS, UART3_RX, EVENTOUT Additional: ADC012_IN1
PA2	K3	36	25	16	I/O	5VT	Default: PA2 Alternate:TIMER1_CH2,TIMER4_CH2,TIMER8_CH0, I2S_CKIN, USART1_TX, EVENTOUT Additional: ADC012_IN2
PA3	L3	37	26	17	I/O	5VT	Default: PA3 Alternate:TIMER1_CH3,TIMER4_CH3,TIMER8_CH1, I2S1_MCK,USART1_RX,USBHS_ULPI_D0, EVENTOUT Additional: ADC012_IN3
V_{SS}	-	38	27	18	P	-	Default: V_{SS}
NC	E3	-	-	-	-	-	-
V_{DD}	-	39	28	19	P	-	Default: V_{DD}
PA4	M3	40	29	20	I/O	TTa	Default: PA4 Alternate:SPI0_NSS,SPI2_NSS, I2S2_WS, USART1_CK, USBHS_SOF, DCI_HSYNC, EVENTOUT Additional: ADC01_IN4, DAC_OUT0
PA5	K4	41	30	21	I/O	TTa	Default: PA5 Alternate:TIMER1_CH0,TIMER1_ETI, TIMER7_CH0_ON, SPI0_SCK, USBHS_ULPI_CK, EVENTOUT Additional: ADC01_IN5, DAC_OUT1
PA6	L4	42	31	22	I/O	5VT	Default: PA6 Alternate:TIMER0_BRKIN,TIMER2_CH0,TIMER7_BRKIN,SPI0_MISO, I2S1_MCK, TIMER12_CH0, SDIO_CMD, DCI_PIXCLK, EVENTOUT Additional: ADC01_IN6
PA7	M4	43	32	23	I/O	5VT	Default: PA7 Alternate:TIMER0_CH0_ON,TIMER2_CH1, TIMER7_CH0_ON,SPI0_MOSI,TIMER13_CH0, EVENTOUT Additional: ADC01_IN7
PC4	K5	44	33	24	I/O	5VT	Default: PC4 Alternate: EVENTOUT

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	BGA100	LQFP144	LQFP100	LQFP64			
							Additional: ADC01_IN14
PC5	L5	45	34	25	I/O	5VT	Default: PC5 Alternate:USART2_RX, EVENTOUT Additional: ADC01_IN15
PB0	M5	46	35	26	I/O	5VT	Default: PB0 Alternate:TIMER0_CH1_ON,TIMER2_CH2,TIMER7_CH1_ON,SPI2_MOSI,I2S2_SD,USBHS_ULPI_D1, SDIO_D1, EVENTOUT Additional: ADC01_IN8, IREF
PB1	M6	47	36	27	I/O	5VT	Default: PB1 Alternate:TIMER0_CH2_ON,TIMER2_CH3,TIMER7_CH2_ON,USBHS_ULPI_D2, SDIO_D2, EVENTOUT Additional: ADC01_IN9
PB2	L6	48	37	28	I/O	5VT	Default: PB2, BOOT1 Alternate:TIMER1_CH3,SPI2_MOSI,I2S2_SD,USBHS_ULPI_D4, SDIO_CK, EVENTOUT
PF11	-	49	-	-	I/O	5VT	Default: PF11 Alternate: DCI_D12, EVENTOUT
PF12	-	50	-	-	I/O	5VT	Default: PF12 Alternate: EVENTOUT
V_{SS}	-	51	-	-	P	-	Default: V_{SS}
V_{DD}	-	52	-	-	P	-	Default: V_{DD}
PF13	-	53	-	-	I/O	5VT	Default: PF13 Alternate: EVENTOUT
PF14	-	54	-	-	I/O	5VT	Default: PF14 Alternate: EVENTOUT
PF15	-	55	-	-	I/O	5VT	Default: PF15 Alternate: EVENTOUT
PG0	-	56	-	-	I/O	5VT	Default: PG0 Alternate: EVENTOUT
PG1	-	57	-	-	I/O	5VT	Default: PG1 Alternate: EVENTOUT
PE7	M7	58	38	-	I/O	5VT	Default: PE7 Alternate: TIMER0_ETI, EVENTOUT
PE8	L7	59	39	-	I/O	5VT	Default: PE8 Alternate: TIMER0_CH0_ON, EVENTOUT
PE9	M8	60	40	-	I/O	5VT	Default: PE9 Alternate: TIMER0_CH0, EVENTOUT
V_{SS}	-	61	-	-	P	-	Default: V_{SS}
V_{DD}	-	62	-	-	P	-	Default: V_{DD}

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	BGA100	LQFP144	LQFP100	LQFP64			
PE10	L8	63	41	-	I/O	5VT	Default: PE10 Alternate: TIMER0_CH1_ON, EVENTOUT
PE11	M9	64	42	-	I/O	5VT	Default: PE11 Alternate:TIMER0_CH1, EVENTOUT
PE12	L9	65	43	-	I/O	5VT	Default: PE12 Alternate:TIMER0_CH2_ON, EVENTOUT
PE13	M10	66	44	-	I/O	5VT	Default: PE13 Alternate:TIMER0_CH2, EVENTOUT
PE14	M11	67	45	-	I/O	5VT	Default: PE14 Alternate:TIMER0_CH3, EVENTOUT
PE15	M12	68	46	-	I/O	5VT	Default: PE15 Alternate: TIMER0_BRKIN, EVENTOUT
PB10	L10	69	47	29	I/O	5VT	Default: PB10 Alternate:TIMER1_CH2,I2C1_SCL, SPI1_SCK, I2S1_CK, I2S2_MCK,USART2_TX,USBHS_ULPI_D3, SDIO_D7, EVENTOUT
PB11	K9	70	48	30	I/O	5VT	Default: PB11 Alternate:TIMER1_CH3,I2C1_SDA,I2S_CKIN,USART2_RX,USBHS_ULPI_D4, EVENTOUT
NC	L11	71	49	31	P	-	Default: V_{CORE}
V_{SS}	F12	-	-	-	P	-	Default: V_{SS}
V_{DD}	G12	72	50	32	P	-	Default: V_{DD}
PB12	L12	73	51	33	I/O	5VT	Default: PB12 Alternate:TIMER0_BRKIN,I2C1_SMBA,SPI1_NSS, I2S1_WS, USART2_CK, CAN1_RX, USBHS_ULPI_D5, USBHS_ID, EVENTOUT
PB13	K12	74	52	34	I/O	5VT	Default: PB13 Alternate:TIMER0_CH0_ON,SPI1_SCK,I2S1_CK, USART2_CTS,CAN1_TX,USBHS_ULPI_D6, EVENTOUT, I2C1_TXFRAME Additional: USBHS_VBUS
PB14	K11	75	53	35	I/O	5VT	Default: PB14 Alternate:TIMER0_CH1_ON,TIMER7_CH1_ON,SPI1_MISO,I2S1_ADD_SD,USART2_RTS,TIMER11_CH0,USBHS_DM, EVENTOUT
PB15	K10	76	54	36	I/O	5VT	Default: PB15 Alternate:RTC_REFIN,TIMER0_CH2_ON,TIMER7_CH2_ON, SPI1_MOSI, I2S1_SD, TIMER11_CH1, USBHS_DP, EVENTOUT
PD8	-	77	55	-	I/O	5VT	Default: PD8 Alternate: USART2_TX, EVENTOUT
PD9	K8	78	56	-	I/O	5VT	Default: PD9 Alternate: USART2_RX, EVENTOUT

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	BGA100	LQFP144	LQFP100	LQFP64			
PD10	J12	79	57	-	I/O	5VT	Default: PD10 Alternate: USART2_CK, EVENTOUT
PD11	J11	80	58	-	I/O	5VT	Default: PD11 Alternate: USART2_CTS, EVENTOUT
PD12	J10	81	59	-	I/O	5VT	Default: PD12 Alternate:TIMER3_CH0,USART2_RTS , EVENTOUT
PD13	H12	82	60	-	I/O	5VT	Default: PD13 Alternate: TIMER3_CH1, EVENTOUT
V_{SS}	-	83	-	-	P	-	Default: V_{SS}
V_{DD}	-	84	-	-	P	-	Default: V_{DD}
PD14	H11	85	61	-	I/O	5VT	Default: PD14 Alternate: TIMER3_CH2, EVENTOUT
PD15	H10	86	62	-	I/O	5VT	Default: PD15 Alternate:TIMER3_CH3, EVENTOUT, CTC_SYNC
PG2	-	87	-	-	I/O	5VT	Default: PG2 Alternate: EVENTOUT
PG3	-	88	-	-	I/O	5VT	Default: PG3 Alternate: EVENTOUT
PG4	-	89	-	-	I/O	5VT	Default: PG4 Alternate: EVENTOUT
PG5	-	90	-	-	I/O	5VT	Default: PG5 Alternate: EVENTOUT
PG6	-	91	-	-	I/O	5VT	Default: PG6 Alternate: DCI_D12, EVENTOUT
PG7	-	92	-	-	I/O	5VT	Default: PG7 Alternate:USART5_CK, DCI_D13, EVENTOUT
PG8	-	93	-	-	I/O	5VT	Default: PG8 Alternate:USART5_RTS, EVENTOUT
V_{SS}	-	94	-	-	P	-	Default: V_{SS}
V_{DD}	-	95	-	-	P	-	Default: V_{DD}
PC6	E12	96	63	37	I/O	5VT	Default: PC6 Alternate:TIMER2_CH0,TIMER7_CH0,I2S1_MCK,USART5_TX, SDIO_D6, DCI_D0, EVENTOUT
PC7	E11	97	64	38	I/O	5VT	Default: PC7 Alternate:TIMER2_CH1,TIMER7_CH1,SPI1_SCK,I2S1_CK,I2S2_MCK, USART5_RX,SDIO_D7,DCI_D1,EVENTOUT
PC8	E10	98	65	39	I/O	5VT	Default: PC8 Alternate:TRACED0,TIMER2_CH2,TIMER7_CH2, USART5_CK, SDIO_D0, DCI_D2, EVENTOUT

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	BGA100	LQFP144	LQFP100	LQFP64			
PC9	D12	99	66	40	I/O	5VT	Default: PC9 Alternate:CK_OUT1,TIMER2_CH3,TIMER7_CH3,I2C2_SDA, I2S_CKIN, SDIO_D1, DCI_D3, EVENTOUT
PA8	D11	100	67	41	I/O	5VT	Default: PA8 Alternate:CK_OUT0,TIMER0_CH0,I2C2_SCL,USART0_CK, USBFS_SOF, SDIO_D1, EVENTOUT, CTC_SYNC
PA9	D10	101	68	42	I/O	5VT	Default: PA9 Alternate:TIMER0_CH1,I2C2_SMBA,SPI1_SCK, I2S1_CK, USART0_TX, SDIO_D2, DCI_D0, EVENTOUT Additional: USBFS_VBUS
PA10	C12	102	69	43	I/O	5VT	Default: PA10 Alternate:TIMER0_CH2,USART0_RX,USBFS_ID,DCI_D1, EVENTOUT, I2C2_TXFRAME
PA11	B12	103	70	44	I/O	5VT	Default: PA11 Alternate:TIMER0_CH3,USART0_CTS,USART5_TX,CAN0_RX, USBFS_DM, EVENTOUT
PA12	A12	104	71	45	I/O	5VT	Default: PA12 Alternate:TIMER0_ETI,USART0_RTS,USART5_RX, CAN0_TX, USBFS_DP, EVENTOUT
PA13	A11	105	72	46	I/O	5VT	Default: JTMS, SWDIO, PA13 Alternate: EVENTOUT
NC	C11	106	73	47	-	-	-
V_{SS}	F11	107	74	-	P	-	Default: V_{SS}
V_{DD}	G11	108	75	48	P	-	Default: V_{DD}
PA14	A10	109	76	49	I/O	5VT	Default: JTCK, SWCLK, PA14 Alternate: EVENTOUT
PA15	A9	110	77	50	I/O	5VT	Default: JTDI, PA15 Alternate:TIMER1_CH0,TIMER1_ETI,SPI0_NSS, SPI2_NSS, I2S2_WS, USART0_TX, EVENTOUT
PC10	B11	111	78	51	I/O	5VT	Default: PC10 Alternate:SPI2_SCK,I2S2_CK,USART2_TX, UART3_TX, SDIO_D2, DCI_D8, EVENTOUT
PC11	C10	112	79	52	I/O	5VT	Default: PC11 Alternate:I2S2_ADD_SD,SPI2_MISO,USART2_RX, UART3_RX, SDIO_D3, DCI_D4, EVENTOUT
PC12	B10	113	80	53	I/O	5VT	Default: PC12 Alternate:I2C1_SDA,SPI2_MOSI,I2S2_SD,USART2_CK, UART4_TX, SDIO_CK, DCI_D9, EVENTOUT
PD0	C9	114	81	-	I/O	5VT	Default: PD0

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Pin Name	Pins				Pin Type(1)	I/O(2) Level	Functions description
	BGA100	LQFP144	LQFP100	LQFP64			
							Alternate:SPI2_MOSI, I2S2_SD, CAN0_RX, EVENTOUT
PD1	B9	115	82	-	I/O	5VT	Default: PD1 Alternate: SPI1_NSS, I2S1_WS, CAN0_TX, EVENTOUT
PD2	C8	116	83	54	I/O	5VT	Default: PD2 Alternate:TIMER2_ETI,UART4_RX,SDIO_CMD,DCI_D11, EVENTOUT
PD3	B8	117	84	-	I/O	5VT	Default: PD3 Alternate:TRACED1,SPI1_SCK,I2S1_CK, USART1_CTS, DCI_D5,EVENTOUT
PD4	B7	118	85	-	I/O	5VT	Default: PD4 Alternate: USART1_RTS, EVENTOUT
PD5	A6	119	86	-	I/O	5VT	Default: PD5 Alternate: USART1_TX, EVENTOUT
V_{SS}	-	120	-	-	P	-	Default: V_{SS}
V_{DD}	-	121	-	-	P	-	Default: V_{DD}
PD6	B6	122	87	-	I/O	5VT	Default: PD6 Alternate:SPI2_MOSI,I2S2_SD,USART1_RX, DCI_D10, EVENTOUT
PD7	A5	123	88	-	I/O	5VT	Default: PD7 Alternate:USART1_CK, EVENTOUT
PG9	-	124	-	-	I/O	5VT	Default: PG9 Alternate:USART5_RX, DCI_VSYNC, EVENTOUT
PG10	-	125	-	-	I/O	5VT	Default: PG10 Alternate: DCI_D2,EVENTOUT
PG11	-	126	-	-	I/O	5VT	Default: PG11 Alternate: DCI_D3, EVENTOUT
PG12	-	127	-	-	I/O	5VT	Default: PG12 Alternate: USART5_RTS, EVENTOUT
PG13	-	128	-	-	I/O	5VT	Default: PG13 Alternate:TRACED2, USART5_CTS, EVENTOUT
PG14	-	129	-	-	I/O	5VT	Default: PG14 Alternate:TRACED3, USART5_TX, EVENTOUT
V_{SS}	-	130	-	-	P	-	Default: V_{SS}
V_{DD}	-	131	-	-	P	-	Default: V_{DD}
PG15	-	132	-	-	I/O	5VT	Default: PG15 Alternate:USART5_CTS,DCI_D13, EVENTOUT
PB3	A8	133	89	55	I/O	5VT	Default: JTDO, PB3 Alternate:TRACESWO,TIMER1_CH1,SPI0_SCK,SPI2_SCK, I2S2_CK, USART0_RX, I2C1_SDA, EVENTOUT
PB4	A7	134	90	56	I/O	5VT	Default: NJTRST, PB4 Alternate:TIMER2_CH0,SPI0_MISO,SPI2_MISO,

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	BGA100	LQFP144	LQFP100	LQFP64			
							I2S2_ADD_SD,I2C2_SDA,SDIO_D0,EVENTOUT, I2C0_TXFRAME
PB5	C5	135	91	57	I/O	5VT	Default: PB5 Alternate:TIMER2_CH1,I2C0_SMBA,SPI0_MOSI,SPI2_MOSI,I2S2_SD, CAN1_RX,USBHS_ULPI_D7,ETH_PPS_OUT, DCI_D10, EVENTOUT
PB6	B5	136	92	58	I/O	5VT	Default: PB6 Alternate:TIMER3_CH0,I2C0_SCL,USART0_TX,CAN1_TX, DCI_D5, EVENTOUT
PB7	B4	137	93	59	I/O	5VT	Default: PB7 Alternate:TIMER3_CH1,I2C0_SDA,USART0_RX, DCI_VSYNC, EVENTOUT
BOOT0	A4	138	94	60	I/O	5VT	Default: BOOT0
PB8	A3	139	95	61	I/O	5VT	Default: PB8 Alternate:TIMER1_CH0, TIMER1_ETI, TIMER3_CH2, TIMER9_CH0, I2C0_SCL, CAN0_RX, SDIO_D4, DCI_D6, EVENTOUT
PB9	B3	140	96	62	I/O	5VT	Default: PB9 Alternate:TIMER1_CH1, TIMER3_CH3, TIMER10_CH0, I2C0_SDA, SPI1_NSS, I2S1_WS, CAN0_TX, SDIO_D5, DCI_D7, EVENTOUT
PE0	C3	141	97	-	I/O	5VT	Default: PE0 Alternate:TIMER3_ETI, DCI_D2, EVENTOUT
PE1	A2	142	98	-	I/O	5VT	Default: PE1 Alternate:TIMER0_CH1_ON, DCI_D3, EVENTOUT
V_{SS}	D3	-	99	63	P	-	Default: V_{SS}
PDR_ON	H3	143	-	-	P	-	Default: PDR_ON
V_{DD}	C4	144	100	64	P	-	Default: V_{DD}

Notes:

1. Type: I = input, O = output, P = power.
2. I/O Level: 5VT = 5 V tolerant.

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Email:sales@manduic.com

Table 3. Port A alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PA0		TIMER1_CH0/TIMER1_ETI	TIMER4_CH0	TIMER7_ETI				USART1_CTS	UART3_TX							EVENTOUT
PA1		TIMER1_CH1	TIMER4_CH1					USART1_RTS	UART3_RX							EVENTOUT
PA2		TIMER1_CH2	TIMER4_CH2	TIMER8_CH0		I2S_CKIN		USART1_TX								EVENTOUT
PA3		TIMER1_CH3	TIMER4_CH3	TIMER8_CH1		I2S1_MCK		USART1_RX			USBHS_ULPI_D0					EVENTOUT
PA4						SPI0_NSS	SPI2_NSS/I2S2_WS	USART1_CK					USBHS_SOF	DCI_HSYNC		EVENTOUT
PA5		TIMER1_CH0/TIMER1_ETI		TIMER7_CH0_ON		SPI0_SCK					USBHS_ULPI_CK					EVENTOUT
PA6		TIMER0_BRKIN	TIMER2_CH0	TIMER7_BRKIN		SPI0_MISO	I2S1_MCK			TIMER12_CH0			SDIO_CMD	DCI_PIXCLK		EVENTOUT
PA7		TIMER0_CH0_ON	TIMER2_CH1	TIMER7_CH0_ON		SPI0_MOSI				TIMER13_CH0						EVENTOUT
PA8	CK_OUT0	TIMER0_CH0			I2C2_SCL			USART0_CK		CTC_SYNC	USBFS_SOF		SDIO_D1			EVENTOUT
PA9		TIMER0_CH1			I2C2_SMBA	SPI1_SCK/I2S1_CK		USART0_TX					SDIO_D2	DCI_D0		EVENTOUT
PA10		TIMER0_CH2			I2C2_TXFRAME			USART0_RX			USBFS_ID			DCI_D1		EVENTOUT
PA11		TIMER0_CH3						USART0_CTS	USART5_TX	CAN0_RX	USBFS_DM					EVENTOUT
PA12		TIMER0_ETI						USART0_RTS	USART5_RX	CAN0_TX	USBFS_DP					EVENTOUT
PA13	JTMS/SWDIO															EVENTOUT
PA14	JTCK/SWCLK															EVENTOUT
PA15	JTDI	TIMER1_CH0/TIMER1_ETI				SPI0_NSS	SPI2_NSS/I2S2_WS	USART0_TX								EVENTOUT

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Table 4. Port B alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PB0		TIMER0_CH1_ON	TIMER2_CH2	TIMER7_CH1_ON				SPI2_MOSI/I2S2_SD			USBHS_ULPI_D1		SDIO_D1			EVENTOUT
PB1		TIMER0_CH2_ON	TIMER2_CH3	TIMER7_CH2_ON							USBHS_ULPI_D2		SDIO_D2			EVENTOUT
PB2		TIMER1_CH3						SPI2_MOSI/I2S2_SD			USBHS_ULPI_D4		SDIO_CK			EVENTOUT
PB3	JTDO/TRACESWO	TIMER1_CH1				SPI0_SCK	SPI2_SCK/I2S2_CK	USART0_RX		I2C1_SDA						EVENTOUT
PB4	NJTRST		TIMER2_CH0		I2C0_TXFRAME	SPI0_MISO	SPI2_MISO	I2S2_ADD_SD		I2C2_SDA			SDIO_D0			EVENTOUT
PB5			TIMER2_CH1		I2C0_SMBA	SPI0_MOSI	SPI2_MOSI/I2S2_SD			CAN1_RX	USBHS_ULPI_D7			DCI_D10		EVENTOUT
PB6			TIMER3_CH0		I2C0_SCL			USART0_TX		CAN1_TX				DCI_D5		EVENTOUT
PB7			TIMER3_CH1		I2C0_SDA			USART0_RX						DCI_VSYNC		EVENTOUT
PB8		TIMER1_CH0/TIMER1_ETI	TIMER3_CH2	TIMER9_CH0	I2C0_SCL					CAN0_RX			SDIO_D4	DCI_D6		EVENTOUT
PB9		TIMER1_CH1	TIMER3_CH3	TIMER10_CH0	I2C0_SDA	SPI1_NSS/I2S1_WS				CAN0_TX			SDIO_D5	DCI_D7		EVENTOUT
PB10		TIMER1_CH2			I2C1_SCL	SPI1_SCK/I2S1_CK	I2S2_MCK	USART2_TX			USBHS_ULPI_D3		SDIO_D7			EVENTOUT
PB11		TIMER1_CH3			I2C1_SDA	I2S_CKIN		USART2_RX			USBHS_ULPI_D4					EVENTOUT
PB12		TIMER0_BRKIN			I2C1_SMBA	SPI1_NSS/I2S1_WS		USART2_CK		CAN1_RX	USBHS_ULPI_D5		USBHS_ID			EVENTOUT
PB13		TIMER0_CH0_ON			I2C1_TXFRAME	SPI1_SCK/I2S1_CK		USART2_CTS		CAN1_TX	USBHS_ULPI_D6					EVENTOUT
PB14		TIMER0_CH1_ON		TIMER7_CH1_ON		SPI1_MISO	I2S1_ADD_SD	USART2_RTS		TIMER11_CH0			USBHS_DM			EVENTOUT
PB15	RTC_REFIN	TIMER0_CH2_ON		TIMER7_CH2_ON		SPI1_MOSI/I2S1_SD				TIMER11_CH1			USBHS_DP			EVENTOUT

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Tel:150-1290-5940
Email:sales@manduic.com

Table 5. Port C alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PC0											USBHS_ULPI_STP					EVENTOUT
PC1						SPI2_MOSI/I2S2_SD		SPI1_MOSI/I2S1_SD								EVENTOUT
PC2						SPI1_MISO	I2S1_ADD_SD				USBHS_ULPI_DIR					EVENTOUT
PC3						SPI1_MOSI/I2S1_SD					USBHS_ULPI_NXT					EVENTOUT
PC4																EVENTOUT
PC5								USART2_RX								EVENTOUT
PC6			TIMER2_CH0	TIMER7_CH0		I2S1_MCK			USART5_TX				SDIO_D6	DCI_D0		EVENTOUT
PC7			TIMER2_CH1	TIMER7_CH1		SPI1_SCK/I2S1_CK	I2S2_MCK		USART5_RX				SDIO_D7	DCI_D1		EVENTOUT
PC8	TRACED0		TIMER2_CH2	TIMER7_CH2					USART5_CK				SDIO_D0	DCI_D2		EVENTOUT
PC9	CK_OUT1		TIMER2_CH3	TIMER7_CH3	I2C2_SDA	I2S_CKIN							SDIO_D1	DCI_D3		EVENTOUT
PC10							SPI2_SCK/I2S2_CK	USART2_TX	UART3_TX				SDIO_D2	DCI_D8		EVENTOUT
PC11						I2S2_ADD_SD	SPI2_MISO	USART2_RX	UART3_RX				SDIO_D3	DCI_D4		EVENTOUT
PC12					I2C1_SDA		SPI2_MOSI/I2S2_SD	USART2_CK	UART4_TX				SDIO_CK	DCI_D9		EVENTOUT
PC13																EVENTOUT
PC14																EVENTOUT
PC15																EVENTOUT

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Table 6. Port D alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PD0							SPI2_MOSI/I2S2_SD			CAN0_RX						EVENTOUT
PD1								SPI1_NSS/I2S1_WS		CAN0_TX						EVENTOUT
PD2			TIMER2_ETI						UART4_RX				SDIO_CMD	DCI_D11		EVENTOUT
PD3	TRACED1					SPI1_SCK/I2S1_CK		USART1_CTS						DCI_D5		EVENTOUT
PD4								USART1_RTS								EVENTOUT
PD5								USART1_TX								EVENTOUT
PD6						SPI2_MOSI/I2S2_SD		USART1_RX						DCI_D10		EVENTOUT
PD7								USART1_CK								EVENTOUT
PD8								USART2_TX								EVENTOUT
PD9								USART2_RX								EVENTOUT
PD10								USART2_CK								EVENTOUT
PD11								USART2_CTS								EVENTOUT
PD12			TIMER3_CH0					USART2_RTS								EVENTOUT
PD13			TIMER3_CH1													EVENTOUT
PD14			TIMER3_CH2													EVENTOUT
PD15	CTC_SYNC		TIMER3_CH3													EVENTOUT

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Table 7. Port E alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PE0			TIMER3_ETI											DCI_D2		EVENTOUT
PE1		TIMER0_CH1_ON												DCI_D3		EVENTOUT
PE2	TRACECLK															EVENTOUT
PE3	TRACED0															EVENTOUT
PE4	TRACED1													DCI_D4		EVENTOUT
PE5	TRACED2			TIMER8_CH0										DCI_D6		EVENTOUT
PE6	TRACED3			TIMER8_CH1										DCI_D7		EVENTOUT
PE7		TIMER0_ETI														EVENTOUT
PE8		TIMER0_CH0_ON														EVENTOUT
PE9		TIMER0_CH0														EVENTOUT
PE10		TIMER0_CH1_ON														EVENTOUT
PE11		TIMER0_CH1														EVENTOUT
PE12		TIMER0_CH2_ON														EVENTOUT
PE13		TIMER0_CH2														EVENTOUT
PE14		TIMER0_CH3														EVENTOUT
PE15		TIMER0_BRKIN														EVENTOUT

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Table 8. Port F alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PF0	CTC_SYNC				I2C1_SDA											EVENTOUT
PF1					I2C1_SCL											EVENTOUT
PF2					I2C1_SMBA											EVENTOUT
PF3					I2C1_TXFRAME											EVENTOUT
PF4																EVENTOUT
PF5																EVENTOUT
PF6				TIMER9_CH0												EVENTOUT
PF7				TIMER10_CH0												EVENTOUT
PF8										TIMER12_CH0						EVENTOUT
PF9										TIMER13_CH0						EVENTOUT
PF10														DCI_D11		EVENTOUT
PF11														DCI_D12		EVENTOUT
PF12																EVENTOUT
PF13																EVENTOUT
PF14																EVENTOUT
PF15																EVENTOUT

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Table 9. Port G alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PG0																EVENTOUT
PG1																EVENTOUT
PG2																EVENTOUT
PG3																EVENTOUT
PG4																EVENTOUT
PG5																EVENTOUT
PG6														DCI_D12		EVENTOUT
PG7									USART5_CK					DCI_D13		EVENTOUT
PG8									USART5_RTS							EVENTOUT
PG9									USART5_RX					DCI_VSYNC		EVENTOUT
PG10														DCI_D2		EVENTOUT
PG11														DCI_D3		EVENTOUT
PG12									USART5_RTS							EVENTOUT
PG13	TRACED2								USART5_CTS							EVENTOUT
PG14	TRACED3								USART5_TX							EVENTOUT
PG15									USART5_CTS					DCI_D13		EVENTOUT

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3 Functional description

3.1 ARM® Cortex®-M4 core

The ARM® Cortex®-M4 processor is a high performance embedded processor with DSP instructions which allow efficient signal processing and complex algorithm execution. It brings an efficient, easy-to-use blend of control and signal processing capabilities to meet the digital signal control markets demand. The processor is highly configurable enabling a wide range of implementations from those requiring floating point operations, memory protection and powerful trace technology to cost sensitive devices requiring minimal area, while delivering outstanding computational performance and an advanced system response to interrupts.

32-bit ARM® Cortex®-M4 processor core

- Up to 168 MHz operation frequency
- Single-cycle multiplication and hardware divider
- Floating Point Unit (FPU)
- Integrated DSP instructions
- Integrated Nested Vectored Interrupt Controller (NVIC)
- 24-bit SysTick timer

The Cortex®-M4 processor is based on the ARMv7-M architecture and supports both Thumb and Thumb-2 instruction sets. Some system peripherals listed below are also provided by Cortex®-M4:

- Internal Bus Matrix connected with ICode bus, DCode bus, system bus, Private Peripheral Bus (PPB) and debug accesses (AHB-AP)
- Nested Vectored Interrupt Controller (NVIC)
- Flash Patch and Breakpoint (FPB)
- Data Watchpoint and Trace (DWT)
- Instrument Trace Macrocell (ITM)
- Memory Protection Unit (MPU)
- Serial Wire JTAG Debug Port (SWJ-DP)
- Trace Port Interface Unit (TPIU)

3.2 On-chip memory

- Up to 3072 Kbytes of Flash memory, including code Flash and data Flash
- 512B of OTP (one-time programmable) memory
- 192 KB of SRAM

The ARM® Cortex®-M4 processor is structured in Harvard architecture which can use separate buses to fetch instructions and load/store data. 3072 Kbytes of inner Flash at most, which includes code Flash and data Flash is available for storing programs and data, and

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accessed (R/W) at CPU clock speed with zero wait states. Up to 192 Kbytes of inner SRAM is composed of SRAM0 (112KB) and SRAM1 (16KB) that can be accessed at same time, and including 64 KB of TCM (tightly-coupled memory) data RAM that can be accessed only by the data bus of the Cortex®-M4 core. The additional 4KB of backup SRAM (BKP SRAM) is implemented in the backup domain, which can keep its content even when the V_{DD} power supply is down. The Figure of GD32F405xx memory map shows the memory map of the GD32F405xx series of devices, including Flash, SRAM, peripheral, and other pre-defined regions.

3.3 Clock, reset and supply management

- Internal 16 MHz factory-trimmed RC and external 4 to 32 MHz crystal oscillator
- Internal 48 MHz RC oscillator
- Internal 32 KHz RC calibrated oscillator and external 32.768 KHz crystal oscillator
- Integrated system clock PLL
- 2.6 to 3.6 V application supply and I/Os
- Supply Supervisor: POR (Power On Reset), PDR (Power Down Reset), and low voltage detector (LVD)

The Clock Control Unit (CCU) provides a range of oscillator and clock functions. These include internal RC oscillator and external crystal oscillator, high speed and low speed two types. Several prescalers allow the frequency configuration of the AHB and two APB domains. The maximum frequency of the two AHB domains are 168 MHz. The maximum frequency of the two APB domains including APB1 is 42 MHz and APB2 is 84 MHz. See Figure 6 for details on the clock tree.

The Reset Control Unit (RCU) controls three kinds of reset: system reset resets the processor core and peripheral IP components. Power-on reset (POR) and power-down reset (PDR) are always active, and ensures proper operation starting from 2.4 V and down to 1.8V. The device remains in reset mode when V_{DD} is below a specified threshold. The embedded low voltage detector (LVD) monitors the power supply, compares it to the voltage threshold and generates an interrupt as a warning message for leading the MCU into security.

Power supply schemes:

- V_{DD} range: 2.6 to 3.6 V, external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} range: 2.6 to 3.6 V, external analog power supplies for ADC, reset blocks, RCs and PLL. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.
- V_{BAT} range: 1.8 to 3.6 V, power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

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3.4 Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from main Flash memory (default)
- Boot from system memory
- Boot from on-chip SRAM

The boot loader is located in the internal 30KB of information blocks for the boot ROM memory (system memory). It is used to reprogram the Flash memory by using USART0, USART2, and USB Device FS in device mode. It also can be used to transfer and update the Flash memory code, the data and the vector table sections. In default condition, boot from bank 0 of Flash memory is selected. It also supports to boot from bank 2 of Flash memory by setting a bit in option bytes.

3.5 Power saving modes

The MCU supports three kinds of power saving modes to achieve even lower power consumption. They are Sleep mode, Deep-sleep mode, and Standby mode. These operating modes reduce the power consumption and allow the application to achieve the best balance between the CPU operating time, speed and power consumption.

- **Sleep** mode
  In sleep mode, only the clock of CPU core is off. All peripherals continue to operate and any interrupt/event can wake up the system.
- **Deep-sleep** mode
  In Deep-sleep mode, all clocks in the 1.2V domain are off, and all of the high speed crystal oscillator (IRC16M, HXTAL) and PLL are disabled. Only the contents of SRAM and registers are retained. Any interrupt or wakeup event from EXTI lines can wake up the system from the Deep-sleep mode including the 23 external lines, the RTC alarm, the LVD output, and USB wakeup. When exiting the Deep-sleep mode, the IRC16M is selected as the system clock.
- **Standby** mode
  In Standby mode, the whole 1.2V domain is power off, the LDO is shut down, and all of IRC16M, HXTAL and PLL are disabled. The contents of SRAM and registers (except Backup Registers) are lost. There are four wakeup sources for the Standby mode, including the external reset from NRST pin, the RTC, the FWDG reset, and the rising edge on WKUP pin.

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3.6 Analog to digital converter (ADC)

- 12-bit SAR ADC's conversion rate is up to 2.6MSPS
- 12-bit, 10-bit, 8-bit or 6-bit configurable resolution
- Hardware oversampling ratio adjustable from 2 to 256x improves resolution to 16-bit
- Input voltage range: V_{SSA} to V_{DDA} (2.6 to 3.6 V)
- Temperature sensor

Up to three 12-bit 2.6MSPS multi-channel ADCs are integrated in the device. It has a total of 19 multiplexed channels: 16 external channels, 1 channel for internal temperature sensor (V_{SENSE}), 1 channel for internal reference voltage (V_{REFINT}) and 1 channel for external battery power supply (V_{BAT}). The input voltage range is between 2.6 V and 3.6 V. An on-chip hardware oversampling scheme improves performance while off-loading the related computational burden from the CPU. An analog watchdog block can be used to detect the channels, which are required to remain within a specific threshold window. A configurable channel management block can be used to perform conversions in single, continuous, scan or discontinuous mode to support more advanced use.

The ADC can be triggered from the events generated by the general-purpose level 0 timers (TMx) and the advanced-control timers (TM0 and TM7) with internal connection. The temperature sensor can be used to generate a voltage that varies linearly with temperature. It is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage in a digital value.

3.7 Digital to analog converter (DAC)

- Two 12-bit DAC converter of independent output channel
- 8-bit or 12-bit mode in conjunction with the DMA controller

The 12-bit buffered DAC channel is used to generate variable analog outputs. The DACs are designed with integrated resistor strings structure. The DAC channels can be triggered by the timer update outputs or EXTI with DMA support. The maximum output value of the DAC is V_{REF+}.

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3.8 DMA

- 16 channels DMA controller and each channel are configurable (8 for DMA0 and 8 for DMA1)
- Support independent 8, 16, 32-bit memory and peripheral transfer
- Peripherals supported: Timers, ADC, SPIs, I2Cs, USARTs, DAC, I2S, SDIO and DCI

The flexible general-purpose DMA controllers provide a hardware method of transferring data between peripherals and/or memory without intervention from the CPU, thereby freeing up bandwidth for other system functions. Three types of access method are supported: peripheral to memory, memory to peripheral, memory to memory

Each channel is connected to fixed hardware DMA requests. The priorities of DMA channel requests are determined by software configuration and hardware channel number. Transfer size of source and destination are independent and configurable.

3.9 General-purpose inputs/outputs (GPIOs)

- Up to 114 fast GPIOs, all mappable on 16 external interrupt vectors (EXTI)
- Analog input/output configurable
- Alternate function input/output configurable

There are up to 140 general purpose I/O pins (GPIO) in GD32F405xx, named PA0 ~ PA15, PB0 ~ PB15, PC0 ~ PC15, PD0 ~ PD15, PE0 ~ PE15, PF0 ~ PF15, PG0 ~ PG15, PH0 ~ PH15 to implement logic input/output functions. Each of the GPIO ports has related control and configuration registers to satisfy the requirements of specific applications. The external interrupts on the GPIO pins of the device have related control and configuration registers in the External Interrupt Control Unit (EXTI). The GPIO ports are pin-shared with other alternative functions (AFs) to obtain maximum flexibility on the package pins. Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current capable except for analog inputs.

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3.10 Timers and PWM generation

- Two 16-bit advanced-control timer (TM0 & TM7), eight 16-bit general-purpose timers (TM2, TM3, TM8 ~ TM13), two 32-bit general-purpose timers (TM1 & TM4) and two 16-bit basic timer (TM5 & TM6)
- Up to 4 independent channels of PWM, output compare or input capture for each general-purpose timer (GPTM) and external trigger input
- 16-bit, motor control PWM advanced-control timer with programmable dead-time generation for output match
- Encoder interface controller with two inputs using quadrature decoder
- 24-bit SysTick timer down counter
- 2 watchdog timers (Free watchdog and window watchdog)

The advanced-control timer (TM0 & TM7) can be used as a three-phase PWM multiplexed on 6 channels. It has complementary PWM outputs with programmable dead-time generation. It can also be used as a complete general-purpose timer. The 4 independent channels can be used for input capture, output compare, PWM generation (edge- or center-aligned counting modes) and single pulse mode output. If configured as a general-purpose 16-bit timer, it has the same functions as the TMx timer. It can be synchronized with external signals or to interconnect with other GPTMs together which have the same architecture and features.

The general-purpose timer (GPTM), can be used for a variety of purposes including general time, input signal pulse width measurement or output waveform generation such as a single pulse generation or PWM output, up to 4 independent channels for input capture/output compare. TM1 & TM4 is based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler. TM2 & TM3 is based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. TM9 ~ TM13 is based on a 16-bit auto-reload upcounter and a 16-bit prescaler. The GPTM also supports an encoder interface with two inputs using quadrature decoder.

The basic timer, known as TM5 & TM6, are mainly used for DAC trigger generation. They can also be used as a simple 16-bit time base.

The GD32F405xx have two watchdog peripherals, free watchdog and window watchdog. They offer a combination of high safety level, flexibility of use and timing accuracy.

The free watchdog timer includes a 12-bit down-counting counter and a 8-bit prescaler, It is clocked from an independent 32 kHz internal RC and as it operates independently of the main clock, it can operate in deep sleep and standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management.

The window watchdog is based on a 7-bit down counter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

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The SysTick timer is dedicated for OS, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Auto reload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

3.11 Real time clock (RTC) and backup registers

- Independent binary-coded decimal (BCD) format timer/counter with twenty 32-bit backup registers.
- Calendar with subsecond, seconds, minutes, hours, week day, date, year and month automatically correction
- Alarm function with wake up from deep-sleep and standby mode capability
- On-the-fly correction for synchronization with master clock. Digital calibration with 1 ppm resolution for compensation of quartz crystal inaccuracy.

The real time clock is an independent timer which provides a set of continuously running counters in backup registers to provide a real calendar function, and provides an alarm interrupt or an expected interrupt. It is not reset by a system or power reset, or when the device wakes up from standby mode. A prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 kHz from external crystal oscillator.

3.12 Inter-integrated circuit (I2C)

- Up to three I2C bus interfaces can support both master and slave mode with a frequency up to 400 kHz (Fast mode)
- Provide arbitration function, optional PEC (packet error checking) generation and checking
- Supports 7-bit and 10-bit addressing mode and general call addressing mode

The I2C interface is an internal circuit allowing communication with an external I2C interface which is an industry standard two line serial interface used for connection to external hardware. These two serial lines are known as a serial data line (SDA) and a serial clock line (SCL). The I2C module provides two data transfer rates: 100 kHz of standard mode or 400 kHz of the fast mode. The I2C module also has an arbitration detect function to prevent the situation where more than one master attempts to transmit data to the I2C bus at the same time. A CRC-8 calculator is also provided in I2C interface to perform packet error checking for I2C data.

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3.13 Serial peripheral interface (SPI)

- Up to three SPI interfaces with a frequency of up to 30 MHz
- Support both master and slave mode
- Hardware CRC calculation and transmit automatic CRC error checking

The SPI interface uses 4 pins, among which are the serial data input and output lines (MISO & MOSI), the clock line (SCK) and the slave select line (NSS). Both SPIs can be served by the DMA controller. The SPI interface may be used for a variety of purposes, including simplex synchronous transfers on two lines with a possible bidirectional data line or reliable communication using CRC checking.

3.14 Universal synchronous/asynchronous receiver transmitter (USART/UART)

- Up to four USARTs and two UARTs with operating frequency up to 9 MHz
- Supports both asynchronous and clocked synchronous serial communication modes
- IrDA SIR encoder and decoder support
- LIN break generation and detection
- ISO 7816-3 compliant smart card interface

The USART (USART0, USART1, USART2, USART5) and UART (UART3, UART4) are used to translate data between parallel and serial interfaces, provides a flexible full duplex data exchange using synchronous or asynchronous transfer. It is also commonly used for RS-232 standard communication. The USART/UART includes a programmable baud rate generator which is capable of dividing the system clock to produce a dedicated clock for the USART/UART transmitter and receiver. The USART/UART also supports DMA function for high speed data communication.

3.15 Inter-IC sound (I2S)

- Two I2S bus Interfaces with sampling frequency from 8 kHz to 192 kHz, multiplexed with SPI1 and SPI2
- Support either master or slave mode Audio
- Sampling frequencies from 8 kHz up to 192 kHz are supported.

The Inter-IC sound (I2S) bus provides a standard communication interface for digital audio applications by 4-wire serial lines. GD32F405xx contain an I2S-bus interface that can be operated with 16/32 bit resolution in master or slave mode, pin multiplexed with SPI1 and SPI2. The audio sampling frequencies from 8 kHz to 192 kHz is supported.

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3.16 Universal serial bus on-the-go full-speed (USB OTG FS)

- One USB device/host/OTG full-speed Interface with frequency up to 12 Mbit/s
- Internal 48 MHz oscillator support crystal-less operation
- Internal main PLL for USB CLK compliantly
- Internal USB OTG FS PHY support

The Universal Serial Bus (USB) is a 4-wire bus with 4 bidirectional endpoints. The device controller enables 12 Mbit/s data exchange with integrated transceivers. Transaction formatting is performed by the hardware, including CRC generation and checking. It supports both host and device modes, as well as OTG mode with Host Negotiation Protocol (HNP) and Session Request Protocol (SRP). The controller contains a full-speed USB PHY internal. For full-speed or low-speed operation, no more external PHY chip is needed. It supports all the four types of transfer (control, bulk, Interrupt and isochronous) defined in USB 2.0 protocol. The required precise 48 MHz clock which can be generated from the internal main PLL (the clock source must use an HXTAL crystal oscillator) or by the internal 48 MHz oscillator in automatic trimming mode that allows crystal-less operation.

3.17 Universal serial bus on-the-go high-speed (USB OTG HS)

- One USB device/host/OTG high-speed Interface with frequency up to 480 Mbit/s
- An external PHY device connected to the ULPI is required when using in HS mode

USB OTG HS supports both host and device modes, as well as OTG mode with Host Negotiation Protocol (HNP) and Session Request Protocol (SRP). The controller provides ULPI interface for external USB PHY integration and it also contains a full-speed USB PHY internal. For full-speed or low-speed operation, no more external PHY chip is needed. It supports all the four types of transfer (control, bulk, Interrupt and isochronous) defined in USB 2.0 protocol. HUB connection is supported when USB HS operates at high-speed in host mode. There is also a DMA engine operating as an AHB bus master in USBHS to speed up the data transfer between USB HS and system.

3.18 Controller area network (CAN)

- Two CAN2.0B interface with communication frequency up to 1 Mbit/s
- Internal main PLL for CAN CLK compliantly

Controller area network (CAN) is a method for enabling serial communication in field bus. The CAN protocol has been used extensively in industrial automation and automotive applications. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. Each CAN has three mailboxes for transmission and two FIFOs of three message deep for reception. It also provides 28 scalable/configurable identifier filter banks for selecting the incoming messages needed and discarding the others.

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3.19 Secure digital input and output card interface (SDIO)

- Support SD2.0/SDIO2.0/MMC4.2 host interface

The Secure Digital Input and Output Card Interface (SDIO) provides access to external SD memory cards specifications version 2.0, SDIO card specification version 2.0 and multi-media card system specification version 4.2 with DMA supported. In addition, this interface is also compliant with CE-ATA digital protocol rev1.1.

3.20 Digital camera interface (DCI)

- Digital video/picture capture
- 8/10/12/14 data width supported
- High transfer efficiency with DMA interface
- Video/picture crop supported
- Various pixel formats supported including JPEG/YCrCb/RGB
- Hard/embedded synchronous signals supported

DCI is an 8-bit to 14-bit parallel interface that able to capture video or picture from a camera via Digital Camera Interface. It supports 8/10/12/14 bits data width through DMA operation.

3.21 Debug mode

- Serial wire JTAG debug port (SWJ-DP)

The ARM® SWJ-DP Interface is embedded and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

3.22 Package and operation temperature

- BGA100 (GDF405VxH), LQFP144 (GD32F405Zx), LQFP100 (GD32F405Vx) and LQFP64 (GD32F405Rx)
- Operation temperature range: -40°C to +85°C (industrial level)

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4 Electrical characteristics

4.1 Absolute maximum ratings

The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 10. Absolute maximum ratings

Symbol	Parameter	Min	Max	Unit
V_{DD}	External voltage range	V_{SS} - 0.3	V_{SS} + 3.6	V
V_{DDA}	External analog supply voltage	V_{SSA} - 0.3	V_{SSA} + 3.6	V
V_{BAT}	External battery supply voltage	V_{SS} - 0.3	V_{SS} + 3.6	V
V_{IN}	Input voltage on 5V tolerant pin	V_{SS} - 0.3	V_{DD} + 4.0	V
	Input voltage on other I/O	V_{SS} - 0.3	4.0	V
I_{IO}	Maximum current for GPIO pins	—	25	mA
T_A	Operating temperature range	-40	+85	°C
T_{STG}	Storage temperature range	-55	+150	°C
T_J	Maximum junction temperature	—	125	°C

4.2 Recommended DC characteristics

Table 11. DC operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	Supply voltage	—	2.6	3.3	3.6	V
V_{DDA}	Analog supply voltage	Same as V_{DD}	2.6	3.3	3.6	V
V_{BAT}	Battery supply voltage	—	1.8	—	3.6	V

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4.3 Power consumption

The power measurements specified in the tables represent that code with data executing from on-chip Flash with the following specifications.

Table 12. Power consumption characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	Supply current (Run mode)	V_{DD}=V_{DDA}=3.3V, HXTAL=25MHz, System clock=168MHz, All peripherals enabled	—	99.2	—	mA
		V_{DD}=V_{DDA}=3.3V, HXTAL =25MHz, System clock =168MHz, All peripherals disabled	—	60.1	—	mA
		V_{DD}=V_{DDA}=3.3V, HXTAL =25MHz, System clock =108MHz, All peripherals enabled	-—	56.3	—	mA
		V_{DD}=V_{DDA}=3.3V, HXTAL =25MHz, System Clock =108MHz, All peripherals disabled	—	35.2	—	mA
	Supply current (Sleep mode)	V_{DD}=V_{DDA}=3.3V, HXTAL =25MHz, CPU clock off, System clock=168MHz, All peripherals enabled	—	67.9	—	mA
		V_{DD}=V_{DDA}=3.3V, HXTAL =25MHz, CPU clock off, System clock=168MHz, All peripherals disabled	—	30	—	mA
	Supply current (Deep-Sleep mode)	V_{DD}=V_{DDA}=3.3V, Regulator in run mode, IRC32K on, RTC on, All GPIOs analog mode	—	1.57	—	mA
		V_{DD}=V_{DDA}=3.3V, Regulator in low power mode, IRC32K on, RTC on, All GPIOs analog mode	—	1.55	—	mA
	Supply current (Standby mode)	V_{DD}=V_{DDA}=3.3V, LXTAL off, IRC32K on, RTC on	—	5.36	—	µA
		V_{DD}=V_{DDA}=3.3V, LXTAL off, IRC32K on, RTC off	—	5.03	—	µA
		V_{DD}=V_{DDA}=3.3V, LXTAL off, IRC32K off, RTC off	—	4.45	—	µA
I_{BAT}	Battery supply current	V_{DD} not available, V_{BAT}=3.6 V, LXTAL on with external crystal, RTC on, Higher driving	—	2.03	—	µA
		V_{DD} not available, V_{BAT}=3.3 V, LXTAL on with external crystal, RTC on, Higher driving	—	1.73	—	µA
		V_{DD} not available, V_{BAT}=2.6 V, LXTAL on with external crystal, RTC on, Higher driving	—	1.43	—	µA
		V_{DD} not available, V_{BAT}=3.6 V, LXTAL on with external crystal, RTC on, Lower driving	—	1.43	—	µA

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		V_{DD} not available, V_{BAT}=3.3 V, LXTAL on with external crystal, RTC on, Lower driving	—	1.15	—	µA
		V_{DD} not available, V_{BAT}=2.6 V, LXTAL on with external crystal, RTC on, Lower driving	—	0.83	—	µA

4.4 EMC characteristics

EMS (electromagnetic susceptibility) includes ESD (Electrostatic discharge, positive and negative) and FTB (Burst of Fast Transient voltage, positive and negative) testing result is given in the following table, based on the EMS levels and classes compliant with IEC 61000 series standard.

Table 13. EMS characteristics

Symbol	Parameter	Conditions	Level/Class
V_{ESD}	Voltage applied to all device pins to induce a functional disturbance	VDD = 3.3 V, TA = +25 °C conforms to IEC 61000-4-2	3B
V_{FTB}	Fast transient voltage burst applied to induce a functional disturbance through 100 pF on V_{DD} and V_{SS} pins	VDD = 3.3 V, TA = +25 °C conforms to IEC 61000-4-4	4A

EMI (Electromagnetic Interference) emission testing result is given in the following table, compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 14. EMI characteristics

Symbol	Parameter	Conditions	Tested frequency band	Conditions		Unit
				24M	48M	
S_{EMI}	Peak level	VDD = 5.0 V, TA = +25 °C, compliant with IEC 61967-2	0.1 to 2 MHz	<0	<0	dBµV
			2 to 30 MHz	-3.9	-2.8	
			30 to 130 MHz	-7.2	-8	
			130 MHz to 1GHz	-7	-7	

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4.5 Power supply supervisor characteristics

Table 15. Power supply supervisor characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{POR}	Power on reset threshold	—	2.30	2.40	2.48	V
V_{PDR}	Power down reset threshold		1.72	1.80	1.88	V
V_{HYST}	PDR hysteresis		—	0.6	—	V
$T_{RSTTEMP}$	Reset temporization		—	2	—	ms

4.6 Electrical sensitivity

The device is strained in order to determine its performance in terms of electrical sensitivity. Electrostatic discharges (ESD) are applied directly to the pins of the sample. Static latch-up (LU) test is based on the two measurement methods.

Table 16. ESD characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A=25 °C; JESD22-A114	—	—	7000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A=25 °C; JESD22-C101	—	—	800	V

Table 17. Static latch-up characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
LU	I-test	T_A=25 °C; JESD78	—	—	±200	mA
	V_{supply} over voltage		—	—	5.4	V

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4.7 External clock characteristics

Table 18. High speed external clock (HXTAL) generated from a crystal/ceramic characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HXTAL}	High Speed External oscillator (HXTAL) frequency	V_{DD}=5.0V	4	8	32	MHz
C_{HXTAL}	Recommended load capacitance on OSC_IN and OSC_OUT	—	—	20	30	pF
R_{FHXTAL}	Recommended external feedback resistor between OSC_IN and OSC_OUT	—	—	400	—	KΩ
D_{HXTAL}	HXTAL oscillator duty cycle	—	30	50	70	%
$I_{DDHXTAL}$	HXTAL oscillator operating current	V_{DD}=3.3V, T_A=25°C	—	1	—	mA
$t_{SUHXTAL}$	HXTAL oscillator startup time	V_{DD}=3.3V, T_A=25°C	—	2	—	ms

Table 19. Low speed external clock (LXTAL) generated from a crystal/ceramic characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LXTAL}	Low Speed External oscillator (LXTAL) frequency	V_{DD}=V_{BAT}=3.3V	—	32.768	—	KHz
C_{LXTAL}	Recommended load capacitance on OSC32_IN and OSC32_OUT	—	—	—	15	pF
D_{LXTAL}	LXTAL oscillator duty cycle	—	30	50	70	%
$I_{DDLXTAL}$	LXTAL oscillator operating current	Low Drive	—	0.7	—	µA
		High Drive	—	1.3	—	
$t_{SULXTAL}$	LXTAL oscillator startup time	V_{DD}=V_{BAT}=3.3V	—	2	—	s

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4.8 Internal clock characteristics

Table 20. High speed internal clock (IRC16M) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{IRC16M}	High Speed Internal Oscillator (IRC16M) frequency	V_{DD}=3.3V	—	16	—	MHz
ACC_{IRC16M}	IRC16M oscillator Frequency accuracy, Factory-trimmed	V_{DD}=3.3V, T_A=-40°C ~+105°C	-4.0	—	+5.0	%
		V_{DD}=3.3V, T_A=0°C ~ +85°C	-2.0	—	+2.0	%
		V_{DD}=3.3V, T_A=25°C	-1.0	—	+1.0	%
	IRC16M oscillator Frequency accuracy, User trimming step	—	—	0.5	—	%
D_{IRC16M}	IRC16M oscillator duty cycle	V_{DD}=3.3V, f_{IRC16M}=16MHz	45	50	55	%
$I_{DDIRC16M}$	IRC16M oscillator operating current	V_{DD}=3.3V, f_{IRC16M}=16MHz	—	66	80	μA
$t_{SUIRC16M}$	IRC16M oscillator startup time	V_{DD}=3.3V, f_{IRC16M}=16MHz	—	2.5	4	us

Table 21. High speed internal clock (IRC48M) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{IRC48M}	High Speed Internal Oscillator (IRC48M) frequency	V_{DD}=3.3V	—	48	—	MHz
ACC_{IRC48M}	IRC48M oscillator Frequency accuracy, Factory-trimmed	V_{DD}=3.3V, T_A=-40°C ~+105°C	-4.0	—	+5.0	%
		V_{DD}=3.3V, T_A=0°C ~ +85°C	-3.0	—	+3.0	%
		V_{DD}=3.3V, T_A=25°C	-2.0	—	+2.0	%
	IRC48M oscillator Frequency accuracy, User trimming step	—	—	0.12	—	%
D_{IRC48M}	IRC48M oscillator duty cycle	V_{DD}=3.3V, f_{IRC48M}=16MHz	45	50	55	%
$I_{DDIRC48M}$	IRC48M oscillator operating current	V_{DD}=3.3V, f_{IRC48M}=16MHz	—	240	300	μA
$t_{SUIRC48M}$	IRC48M oscillator startup time	V_{DD}=3.3V, f_{IRC48M}=16MHz	—	2.5	4	us

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Table 22. Low speed internal clock (IRC32K) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{IRC32K}	Low Speed Internal oscillator (IRC32K) frequency	V_{DD}=V_{BAT}=3.3V, T_A=-40°C ~ +85°C	20	32	45	KHz
$I_{DDIRC32K}$	IRC32K oscillator operating current	V_{DD}=V_{BAT}=3.3V, T_A=25°C	—	0.4	0.6	μA
$t_{SUIRC32K}$	IRC32K oscillator startup time	V_{DD}=V_{BAT}=3.3V, T_A=25°C	—	110	130	μs

4.9 PLL characteristics

Table 23. PLL characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLLIN}	PLL input clock frequency	—	1	—	4	MHz
f_{PLL}	PLL output clock frequency	—	100	—	500	MHz
t_{LOCK}	PLL lock time	VCO freq=100MHz	—	80	168	μs
		VCO freq=500MHz	—	100	300	
I_{DD}	Current consumption on VDD	VCO freq=500MHz	—	750	—	μA
I_{DDA}	Current consumption on VDDA	VCO freq=500MHz	—	1100	—	μA
$Jitter_{PLL}$	Cycle to cycle Jitter	System clock 120MHz	—	30	—	ps

Table 24. PLL spread spectrum clock generation (SSCG) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{MOD}	Modulation frequency	—	—	—	10	KHz
Mdamp	Peak modulation amplitude	—	—	—	2	%
MODCNT* MODSTEP	—	—	—	—	2^{15}-1	—

Equation 1: SSCG configuration equation:

$$MODCNT = round(f_{PLLIN} / 4 / f_{mod})$$

$$MODSTEP = round\left(mdamp * PLLN * 2^{14} / \left(MODCNT * 100\right)\right)$$

The formula above (Equation 1) is SSCG configuration equation.

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4.10 Memory characteristics

Table 25. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PE_{CYC}	Number of guaranteed program /erase cycles before failure (Endurance)	T_A=-40°C ~ +85°C	100	—	—	kcycles
t_{RET}	Data retention time	T_A=125°C	20	—	—	years
t_{PROG}	Word programming time	T_A=-40°C ~ +85°C	200	—	400	us
t_{ERASE}	Page erase time	T_A=-40°C ~ +85°C	60	100	450	ms
t_{MERASE}	Mass erase time	T_A=-40°C ~ +85°C	3.2	—	9.6	s

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4.11 GPIO characteristics

Table 26. I/O port characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Standard IO Low level input voltage	V_{DD}=2.6V	—	—	1.27	V
		V_{DD}=3.3V	—	—	1.58	
		V_{DD}=3.6V	—	—	1.71	
	High Voltage tolerant IO Low level input voltage	V_{DD}=2.6V	—	—	1.27	V
		V_{DD}=3.3V	—	—	1.58	
		V_{DD}=3.6V	—	—	1.71	
V_{IH}	Standard IO High level input voltage	V_{DD}=2.6V	1.40	—	—	V
		V_{DD}=3.3V	1.71	—	—	
		V_{DD}=3.6V	1.84	—	—	
	High Voltage tolerant IO High level input voltage	V_{DD}=2.6V	1.40	—	—	V
		V_{DD}=3.3V	1.71	—	—	
		V_{DD}=3.6V	1.84	—	—	
V_{OL}	Low level output voltage	V_{DD}=2.6V, I_{IO}=8mA	—	—	0.17	V
		V_{DD}=3.3V, I_{IO}=8mA	—	—	0.16	
		V_{DD}=3.6V, I_{IO}=8mA	—	—	0.16	
		V_{DD}=2.6V, I_{IO}=20mA	—	—	0.46	
		V_{DD}=3.3V, I_{IO}=20mA	—	—	0.40	
		V_{DD}=3.6V, I_{IO}=20mA	—	—	0.40	
V_{OH}	High level output voltage	V_{DD}=2.6V, I_{IO}=8mA	2.39	—	—	V
		V_{DD}=3.3V, I_{IO}=8mA	3.12	—	—	
		V_{DD}=3.6V, I_{IO}=8mA	3.41	—	—	
		V_{DD}=2.6V, I_{IO}=20mA	2.05	—	—	
		V_{DD}=3.3V, I_{IO}=20mA	2.84	—	—	
		V_{DD}=3.6V, I_{IO}=20mA	3.12	—	—	
R_{PU}	Internal pull-up resistor	V_{IN}=V_{SS}	30	40	50	kΩ
R_{PD}	Internal pull-down resistor	V_{IN}=V_{DD}	30	40	50	kΩ

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4.12 ADC characteristics

Table 27. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Operating voltage	—	2.6	3.3	3.6	V
V_{ADCIN}	ADC input voltage range	—	0	—	V_{REF+}	V
f_{ADC}	ADC clock	—	0.1	—	40	MHz
f_S	Sampling rate	12-bit	0.007	—	2.6	MSPS
		10-bit	0.008	—	3.1	
		8-bit	0.01	—	3.6	
		6-bit	0.011	—	4.4	
V_{IN}	Analog input voltage	16 external;3 internal	0	—	V_{DDA}	V
V_{REF+}	Positive Reference Voltage	—	—	V_{DDA}	—	V
V_{REF-}	Negative Reference Voltage	—	—	0	—	V
R_{AIN}	External input impedance	See ***Equation 2***	—	—	52.1	kΩ
R_{ADC}	Input sampling switch resistance	—	—	—	0.55	kΩ
C_{ADC}	Input sampling capacitance	No pin/pad capacitance included	—	—	5.5	pF
t_{CAL}	Calibration time	f_{ADC}=40MHz	—	3.275	—	µs
t_s	Sampling time	f_{ADC}=40MHz	0.075	—	12	µs
t_{CONV}	Total conversion time (including sampling time)	12-bit	—	15	—	1/ f_{ADC}
		10-bit	—	13	—	
		8-bit	—	11	—	
		6-bit	—	9	—	
t_{SU}	Startup time	—	—	—	1	µs

Equation 2: R_{AIN} max formula $R_{AIN} < \frac{T_s}{f_{ADC} * C_{ADC} * \ln(2^{N+2})} - R_{ADC}$

The formula above (Equation 2) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N=12 (from 12-bit resolution).

Table 28. ADC $R_{AIN\ max}$ for f_{ADC}=40MHz

T_s (cycles)	t_s (us)	$R_{AIN\ max}$ (KΩ)
3	0.075	0.85
15	0.375	6.5
28	0.7	12.6
55	1.375	25.7
84	2.1	38.8
112	2.8	51.9
144	3.6	N/A
480	12	N/A

Note: Guaranteed by design, not tested in production.

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Table 29. ADC dynamic accuracy at f_{ADC} = 30 MHz

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ENOB	Effective number of bits	f_{ADC}=30MHz	10.5	10.6	—	bits
SNDR	Signal-to-noise and distortion ratio	V_{DDA}=V_{REFP}=2.6V	65	65.6	—	dB
SNR	Signal-to-noise ratio	Input Frequency=110KHz	65.5	66	—	
THD	Total harmonic distortion	Temperature=25℃	-74	-76	—	

Table 30. ADC dynamic accuracy at f_{ADC} = 30 MHz

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ENOB	Effective number of bits	f_{ADC}=30MHz	10.7	10.8	—	bits
SNDR	Signal-to-noise and distortion ratio	V_{DDA}=V_{REFP}=3.3V	66.2	65.8	—	dB
SNR	Signal-to-noise ratio	Input Frequency=110KHz	66.8	67.4	—	
THD	Total harmonic distortion	Temperature=25℃	-71	-75	—	

Table 31. ADC dynamic accuracy at f_{ADC} = 36 MHz

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ENOB	Effective number of bits	f_{ADC}=36MHz	10.3	10.4	—	bits
SNDR	Signal-to-noise and distortion ratio	V_{DDA}=V_{REFP}=3.3V	63.8	64.4	—	dB
SNR	Signal-to-noise ratio	Input Frequency=110KHz	64.2	65	—	
THD	Total harmonic distortion	Temperature=25℃	-70	-72	—	

Table 32. ADC dynamic accuracy at f_{ADC} = 40 MHz

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ENOB	Effective number of bits	f_{ADC}=40MHz	9.9	10.0	—	bits
SNDR	Signal-to-noise and distortion ratio	V_{DDA}=V_{REFP}=3.3V	61.4	62	—	dB
SNR	Signal-to-noise ratio	Input Frequency=110KHz	62	62.4	—	
THD	Total harmonic distortion	Temperature=25℃	-68	-70	—	

Table 33. ADC static accuracy at f_{ADC} = 15 MHz

Symbol	Parameter	Test conditions	Typ	Max	Unit
Offset	Offset error	f_{ADC}=15MHz V_{DDA}=V_{REFP}=3.3V	±2	±3	LSB
DNL	Differential linearity error		±0.9	±1.2	
INL	Integral linearity error		±1.1	±1.5	

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4.13 DAC characteristics

Table 34. DAC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Operating voltage	—	2.6	3.3	3.6	V
R_{LOAD}	Resistive load	Resistive load with buffer ON	5	—	—	kΩ
R_O	Impedance output	Impedance output with buffer OFF	—	—	15	kΩ
C_{LOAD}	Capacitive load	Capacitive load with buffer ON	—	—	50	pF
DAC_OUT_{min}	Lower DAC_OUT voltage	Lower DAC_OUT voltage with buffer ON	0.2	—	—	V
		Lower DAC_OUT voltage with buffer OFF	0.5	—	—	mV
DAC_OUT_{max}	Higher DAC_OUT voltage	Higher DAC_OUT voltage with buffer ON	—	—	V_{DDA}-0.2	V
		Higher DAC_OUT voltage with buffer OFF	—	—	V_{DDA}-1LSB	V
I_{DDA}	DC current consumption in quiescent mode with no load	Middle code on the input	—	—	500	μA
		Worst code on the input	—	—	560	
DNL	Differential non linearity	10-bit configuration	—	—	±0.5	LSB
		12-bit configuration	—	—	±2	
INL	Integral non linearity	10-bit configuration	—	—	±1	LSB
		12-bit configuration	—	—	±4	
Gain error	Gain error	—	—	±0.5	—	%
$T_{SETTLING}$	Settling time	C_{LOAD}≤50pF, R_{LOAD}≥5kΩ	—	0.5	1	μs
Update rate	Max frequency for a correct DAC_OUT change from code i to i±1LSB	C_{LOAD}≤50pF, R_{LOAD}≥5kΩ	—	—	4	MS/s
T_{WAKEUP}	Wakeup time from off state	C_{LOAD}≤50pF, R_{LOAD}≥5kΩ	—	1	2	μs
PSRR	Power supply rejection ratio	No R_{Load}, C_{LOAD}=50pF	—	-90	-75	dB

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4.14 SPI characteristics

Table 35. SPI characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency	—	—	—	30	MHz
$TSI_{K(H)}$	SCK clock high time	—	19	—	—	ns
$TSI_{K(L)}$	SCK clock low time	—	19	—	—	ns
SPI master mode						
$t_{V(MO)}$	Data output valid time	—	—	—	25	ns
$t_{H(MO)}$	Data output hold time	—	2	—	—	ns
$t_{SU(MI)}$	Data input setup time	—	5	—	—	ns
$t_{H(MI)}$	Data input hold time	—	5	—	—	ns
SPI slave mode						
$t_{SU(NSS)}$	NSS enable setup time	f_{PCLK}=54MHz	74	—	—	ns
$t_{H(NSS)}$	NSS enable hold time	f_{PCLK}=54MHz	37	—	—	ns
$t_{A(SO)}$	Data output access time	f_{PCLK}=54MHz	0	—	55	ns
$t_{DIS(SO)}$	Data output disable time	—	3	—	10	ns
$t_{V(SO)}$	Data output valid time	—	—	—	25	ns
$t_{H(SO)}$	Data output hold time	—	15	—	—	ns
$t_{SU(SI)}$	Data input setup time	—	5	—	—	ns
$t_{H(SI)}$	Data input hold time	—	4	—	—	ns

4.15 I2C characteristics

Table 36. I2C characteristics

Symbol	Parameter	Conditions	Standard mode		Fast mode		Unit
			Min	Max	Min	Max	
f_{SCL}	SCL clock frequency	—	0	100	0	400	KHz
$TSI_{L(H)}$	SCL clock high time	—	4.0	—	0.6	—	ns
$TSI_{L(L)}$	SCL clock low time	—	4.7	—	1.3	—	ns

4.16 USART characteristics

Table 37. USART characteristics

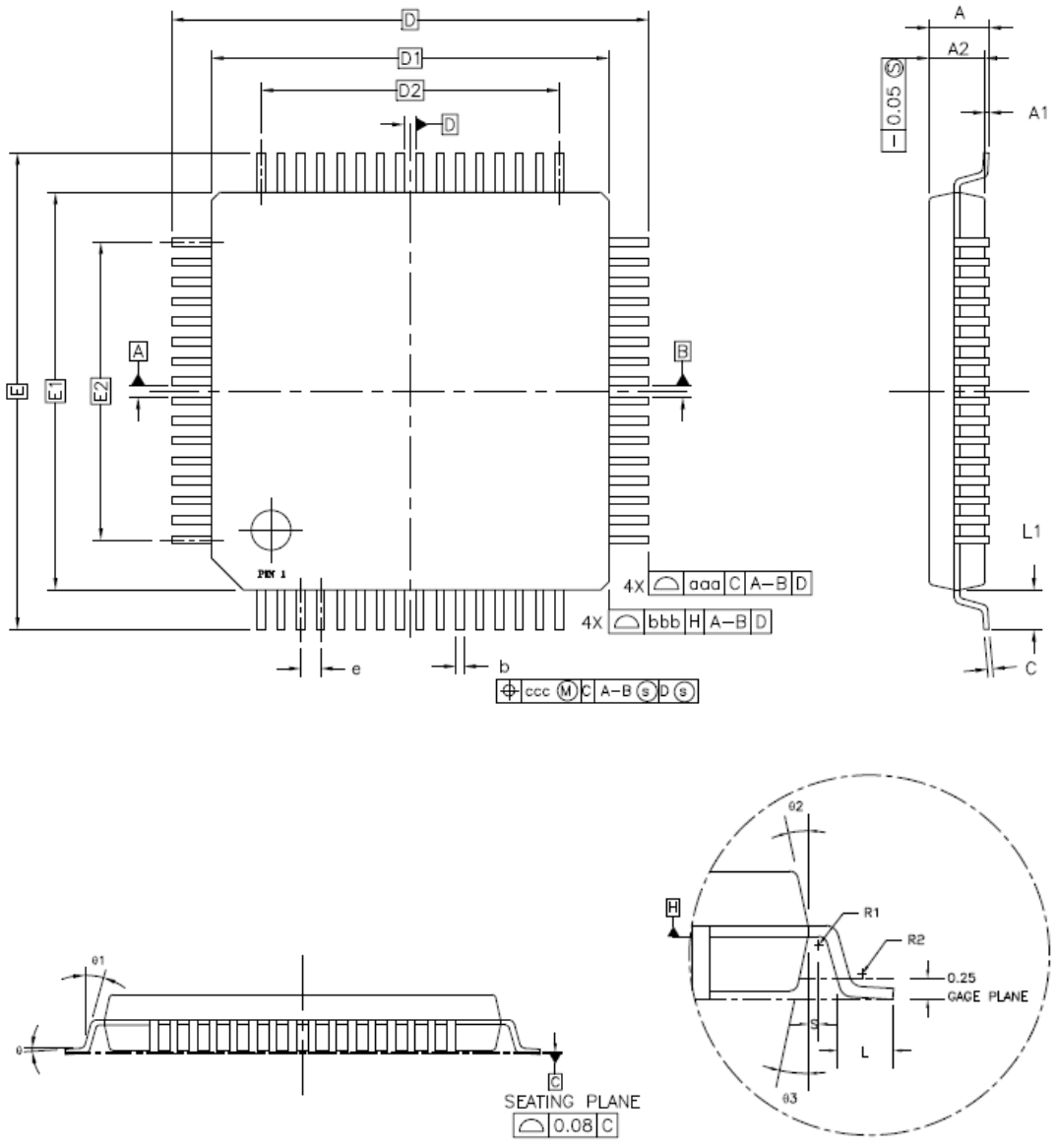
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency	—	—	—	36	MHz
$TSI_{K(H)}$	SCK clock high time	—	13	—	—	ns
$TSI_{K(L)}$	SCK clock low time	—	13	—	—	ns

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5 Package information

5.1 LQFP package outline dimensions

Figure 8. LQFP package outline



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Table 38. LQFP package dimensions

Symbol	LQFP64			LQFP100			LQFP144		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
A	-	-	1.60	-	-	1.60	-	-	1.60
A1	0.05	-	0.15	0.05	-	0.15	0.05	-	0.15
A2	1.35	1.40	1.45	1.35	1.40	1.45	1.35	1.40	1.45
D	-	12.00	-	-	16.00	-	-	22.00	-
D1	-	10.00	-	-	14.00	-	-	20.00	-
E	-	12.00	-	-	16.00	-	-	22.00	-
E1	-	10.00	-	-	14.00	-	-	20.00	-
R1	0.08	-	-	0.08	-	-	0.08	-	-
R2	0.08	-	0.20	0.08	-	0.20	0.08	-	0.20
θ	0°	3.5°	7°	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	-	-	0°	-	-	0°	-	-
θ2	11°	12°	13°	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°	11°	12°	13°
c	0.09	-	0.20	0.09	-	0.20	0.09	-	0.20
L	0.45	0.60	0.75	0.45	0.60	0.75	0.45	0.60	0.75
L1	-	1.00	-	-	1.00	-	-	1.00	-
S	0.20	-	-	0.20	-	-	0.20	-	-
b	0.17	0.20	0.27	0.17	0.20	0.27	0.17	0.20	0.27
e	-	0.50	-	-	0.50	-	-	0.50	-
D2	-	7.50	-	-	12.00	-	-	17.50	-
E2	-	7.50	-	-	12.00	-	-	17.50	-
aaa	0.20			0.20			0.20		
bbb	0.20			0.20			0.20		
ccc	0.08			0.08			0.08		

(Original dimensions are in millimeters)

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5.2 BGA package outline dimensions

Figure 9. BGA package outline

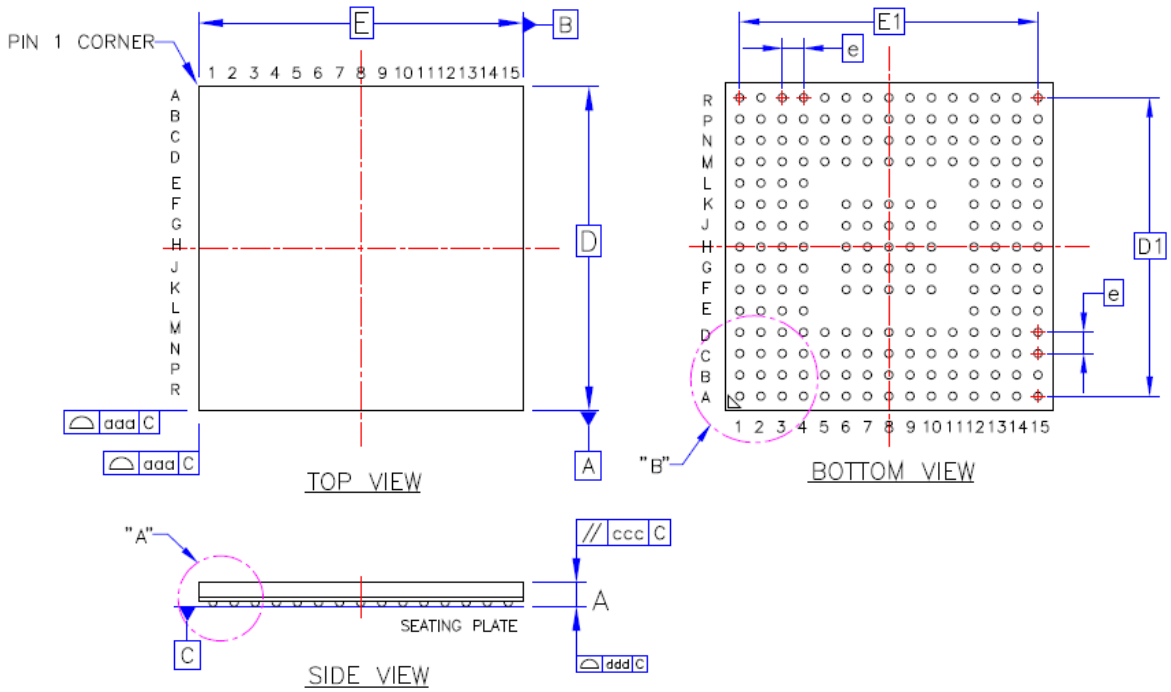


Table 39. BGA package dimensions

Symbol	BGA100		
	Min	Typ	Max
A	-	0.74	0.84
A1	0.11	0.16	0.21
A2	-	0.45	-
A3	0.10	0.13	0.16
D	6.90	7.00	7.10
E	6.90	7.00	7.10
e	-	0.50	-
b	0.20	0.25	0.30
D1	-	5.50	-
E1	-	5.50	-
aaa	0.10		
bbb	-		
ccc	0.10		
ddd	0.08		
eee	0.15		
fff	0.05		

(Original dimensions are in millimeters)

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6 Ordering information

Table 40. Part ordering code for GD32F405xx devices

Ordering code	Flash (KB)	Package	Package type	Temperature operating range
GD32F405RET6	512	LQFP64	Green	Industrial -40°C to +85°C
GD32F405RGT6	1024	LQFP64	Green	Industrial -40°C to +85°C
GD32F405RKT6	3072	LQFP64	Green	Industrial -40°C to +85°C
GD32F405VGT6	1024	LQFP100	Green	Industrial -40°C to +85°C
GD32F405VKT6	3072	LQFP100	Green	Industrial -40°C to +85°C
GD32F405VGH6	1024	BGA100	Green	Industrial -40°C to +85°C
GD32F405VKH6	3072	BGA100	Green	Industrial -40°C to +85°C
GD32F405ZGT6	1024	LQFP144	Green	Industrial -40°C to +85°C
GD32F405ZKT6	3072	LQFP144	Green	Industrial -40°C to +85°C

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7 Revision history

Table 41. Revision history

Revision No.	Description	Date
1.0	Initial Release	Oct. 25, 2016

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Email:sales@manduic.com