# GigaDevice Semiconductor Inc.

# GD32F405RGH6
# Arm® Cortex®-M4 32-bit MCU

SPEC

Preliminary

| | | | |
|---|---|---|---|
| **Document Level** | □ Manual ■ Datasheet/SPEC/Report/Flow<br>□ Application Note/ Operation Instruction | | |
| **Security Level** | ■ Internal Only | **Author** | Eric Jin |
| **Revision** | Initial R2 | **Release Date** | May. 22, 2019 |

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# 1. Device overview

## 1.1. Device information

**Table 2-1.GD32F405RGH6 devices features and peripheral list**

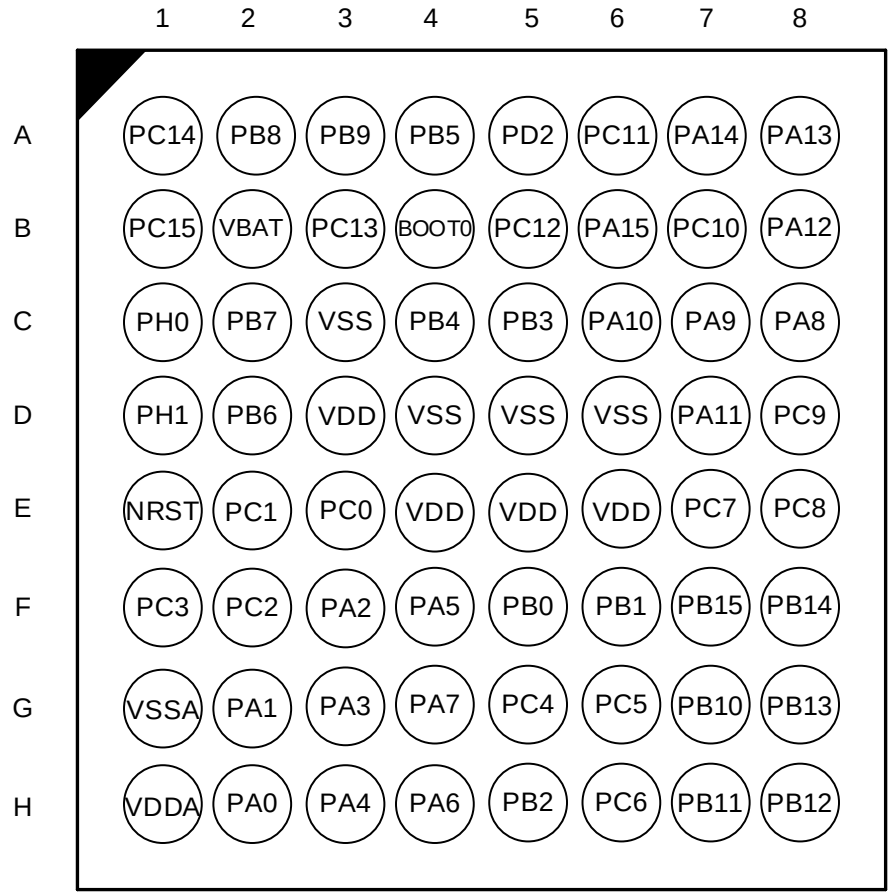
| Part Number | | GD32F405RGH6 |
|---|---|---|
| Flash | Code area (KB) | 256 |
| | Data area (KB) | 768 |
| | Total (KB) | 1024 |
| SRAM (KB) | | 512 |
| Timers | General timer(16-bit) | 8 |
| | General timer(32-bit) | 2 |
| | Advanced timer(16-bit) | 2 |
| | Basic timer(16-bit) | 2 |
| | SysTick | 1 |
| | Watchdog | 2 |
| | RTC | 1 |
| Connectivity | USART | 4 |
| | UART | 2 |
| | I2C | 3 |
| | SPI/I2S | 3/2 |
| | SDIO | 1 |
| | CAN 2.0B | 2 |
| | USB OTG | FS+HS |
| | Digital Camera | 1 |
| GPIO | | 51 |
| Anal | ADC Unit (CHs) | 3(16) |
| | DAC | 2 |
| EXTI | | 16 |
| Package | | BGA64 |



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## 1.2. Pinouts and pin assignment

**Figure 1-1. GD32F405RGH6 pinouts**






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## 1.1 Pin definitions

### 1.1.1 GD32F405RGH6 pin definitions

**Table 1-1. GD32F405RGH6 pin definitions**

| Pin Name | Pins | Pin Type(1) | I/O Level(2) | Functions description |
|---|---|---|---|---|
| $V_{BAT}$ | B2 | P | - | Default: $V_{BAT}$ |
| PC13-TAMPER-RTC | B3 | I/O | 5VT | Default: PC13<br>Alternate: EVENTOUT<br>Additional: RTC_TAMP0, RTC_OUT, RTC_TS |
| PC14-OSC32IN | A1 | I/O | 5VT | Default: PC14<br>Alternate: EVENTOUT<br>Additional: OSC32IN |
| PC15-OSC32OUT | B1 | I/O | 5VT | Default: PC15<br>Alternate: EVENTOUT<br>Additional: OSC32OUT |
| PH0 | C1 | I/O | 5VT | Default: PH0, OSCIN<br>Alternate: EVENTOUT<br>Additional: OSCIN |
| PH1 | D1 | I/O | 5VT | Default: PH1, OSCOUT<br>Alternate: EVENTOUT<br>Additional: OSCOUT |
| NRST | E1 | - | - | Default: NRST |
| PC0 | E3 | I/O | 5VT | Default: PC0<br>Alternate: USBHS_ULPI_STP, EVENTOUT<br>Additional: ADC012_IN10 |
| PC1 | E2 | I/O | 5VT | Default: PC1<br>Alternate:SPI2_MOSI, I2S2_SD, SPI1_MOSI, I2S1_SD, EVENTOUT<br>Additional: ADC012_IN11 |
| PC2 | F2 | I/O | 5VT | Default: PC2<br>Alternate:SPI1_MISO,I2S1_ADD_SD,USBHS_ULPI_DIR, EVENTOUT<br>Additional: ADC012_IN12 |
| PC3 | F1 | I/O | 5VT | Default: PC3<br>Alternate:SPI1_MOSI,I2S1_SD,USBHS_ULPI_NXT, EVENTOUT<br>Additional: ADC012_IN13 |
| $V_{SSA}$ | G1 | P | - | Default: $V_{SSA}$ |
| $V_{DDA}$ | H1 | P | - | Default: $V_{DDA}$ |
| PA0-WKUP | H2 | I/O | 5VT | Default: PA0<br>Alternate:TIMER1_CH0,TIMER1_ETI,TIMER4_CH0, |



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| Pin Name | Pins | Pin Type(1) | I/O Level(2) | Functions description |
|---|---|---|---|---|
| | | | | TIMER7_ETI,USART1_CTS, UART3_TX, EVENTOUT<br>Additional: ADC012_IN0, WKUP |
| PA1 | G2 | I/O | 5VT | Default: PA1<br>Alternate:TIMER1_CH1, TIMER4_CH1, USART1_RTS, UART3_RX, EVENTOUT<br>Additional: ADC012_IN1 |
| PA2 | F3 | I/O | 5VT | Default: PA2<br>Alternate:TIMER1_CH2,TIMER4_CH2,TIMER8_CH0, I2S_CKIN, USART1_TX, EVENTOUT<br>Additional: ADC012_IN2 |
| PA3 | G3 | I/O | 5VT | Default: PA3<br>Alternate:TIMER1_CH3,TIMER4_CH3,TIMER8_CH1, I2S1_MCK,USART1_RX,USBHS_ULPI_D0, EVENTOUT<br>Additional: ADC012_IN3 |
| $V_{SS}$ | D4 | P | - | Default: $V_{SS}$ |
| $V_{DD}$ | E4 | P | - | Default: $V_{DD}$ |
| PA4 | H3 | I/O | | Default: PA4<br>Alternate:SPI0_NSS,SPI2_NSS, I2S2_WS, USART1_CK, USBHS_SOF, DCI_HSYNC, EVENTOUT<br>Additional: ADC01_IN4, DAC_OUT0 |
| PA5 | F4 | I/O | | Default: PA5<br>Alternate:TIMER1_CH0,TIMER1_ETI, TIMER7_CH0_ON, SPI0_SCK, USBHS_ULPI_CK, EVENTOUT<br>Additional: ADC01_IN5, DAC_OUT1 |
| PA6 | H4 | I/O | 5VT | Default: PA6<br>Alternate:TIMER0_BRKIN,TIMER2_CH0,TIMER7_BRKIN,SPI0_MISO, I2S1_MCK, TIMER12_CH0, SDIO_CMD, DCI_PIXCLK, EVENTOUT<br>Additional: ADC01_IN6 |
| PA7 | G4 | I/O | 5VT | Default: PA7<br>Alternate:TIMER0_CH0_ON,TIMER2_CH1, TIMER7_CH0_ON,SPI0_MOSI,TIMER13_CH0, EVENTOUT<br>Additional: ADC01_IN7 |
| PC4 | G5 | I/O | 5VT | Default: PC4<br>Alternate: EVENTOUT<br>Additional: ADC01_IN14 |
| PC5 | G6 | I/O | 5VT | Default: PC5<br>Alternate:USART2_RX, EVENTOUT<br>Additional: ADC01_IN15 |
| PB0 | F5 | I/O | 5VT | Default: PB0<br>Alternate:TIMER0_CH1_ON,TIMER2_CH2,TIMER7_CH1_ON,S |



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| Pin Name | Pins | Pin Type(1) | I/O Level(2) | Functions description |
|---|---|---|---|---|
| | | | | PI2_MOSI,I2S2_SD,USBHS_ULPI_D1, SDIO_D1, EVENTOUT<br>Additional: ADC01_IN8, IREF |
| PB1 | F6 | I/O | 5VT | Default: PB1<br>Alternate:TIMER0_CH2_ON,TIMER2_CH3,TIMER7_CH2_ON,USBHS_ULPI_D2, SDIO_D2, EVENTOUT<br>Additional: ADC01_IN9 |
| PB2 | H5 | I/O | 5VT | Default: PB2, BOOT1<br>Alternate:TIMER1_CH3,SPI2_MOSI,I2S2_SD,USBHS_ULPI_D4, SDIO_CK, EVENTOUT |
| PB10 | G7 | I/O | 5VT | Default: PB10<br>Alternate:TIMER1_CH2,I2C1_SCL, SPI1_SCK, I2S1_CK, I2S2_MCK,USART2_TX,USBHS_ULPI_D3, SDIO_D7, EVENTOUT |
| PB11 | H7 | I/O | 5VT | Default: PB11<br>Alternate:TIMER1_CH3,I2C1_SDA,I2S_CKIN,USART2_RX,USBHS_ULPI_D4, EVENTOUT |
| Vss | D5 | P | - | Default: $V_{SS}$ |
| $V_{DD}$ | E5 | P | - | Default: $V_{DD}$ |
| PB12 | H8 | I/O | 5VT | Default: PB12<br>Alternate:TIMER0_BRKIN,I2C1_SMBA,SPI1_NSS, I2S1_WS, USART2_CK, CAN1_RX, USBHS_ULPI_D5, USBHS_ID, EVENTOUT |
| PB13 | G8 | I/O | 5VT | Default: PB13<br>Alternate:TIMER0_CH0_ON,SPI1_SCK,I2S1_CK, USART2_CTS,CAN1_TX,USBHS_ULPI_D6, EVENTOUT, I2C1_TXFRAME<br>Additional: USBHS_VBUS |
| PB14 | F8 | I/O | 5VT | Default: PB14<br>Alternate:TIMER0_CH1_ON,TIMER7_CH1_ON,SPI1_MISO,I2S1_ADD_SD,USART2_RTS,TIMER11_CH0,USBHS_DM, EVENTOUT |
| PB15 | F7 | I/O | 5VT | Default: PB15<br>Alternate:RTC_REFIN,TIMER0_CH2_ON,TIMER7_CH2_ON, SPI1_MOSI, I2S1_SD, TIMER11_CH1, USBHS_DP, EVENTOUT |
| PC6 | H6 | I/O | 5VT | Default: PC6<br>Alternate:TIMER2_CH0,TIMER7_CH0,I2S1_MCK,USART5_TX, SDIO_D6, DCI_D0, EVENTOUT |
| PC7 | E7 | I/O | 5VT | Default: PC7<br>Alternate:TIMER2_CH1,TIMER7_CH1,SPI1_SCK,I2S1_CK,I2S2_MCK,USART5_RX,SDIO_D7,DCI_D1,EVENTOUT |
| PC8 | E8 | I/O | 5VT | Default: PC8 |



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| Pin Name | Pins | Pin Type(1) | I/O Level(2) | Functions description |
|---|---|---|---|---|
| | | | | Alternate:TRACED0,TIMER2_CH2,TIMER7_CH2, USART5_CK, SDIO_D0, DCI_D2, EVENTOUT |
| PC9 | D8 | I/O | 5VT | Default: PC9<br>Alternate:CK_OUT1,TIMER2_CH3,TIMER7_CH3,I2C2_SDA, I2S_CKIN, SDIO_D1, DCI_D3, EVENTOUT |
| PA8 | C8 | I/O | 5VT | Default: PA8<br>Alternate:CK_OUT0,TIMER0_CH0,I2C2_SCL,USART0_CK, USBFS_SOF, SDIO_D1, EVENTOUT, CTC_SYNC |
| PA9 | C7 | I/O | 5VT | Default: PA9<br>Alternate:TIMER0_CH1,I2C2_SMBA,SPI1_SCK, I2S1_CK, USART0_TX, SDIO_D2, DCI_D0, EVENTOUT<br>Additional: USBFS_VBUS |
| PA10 | C6 | I/O | 5VT | Default: PA10<br>Alternate:TIMER0_CH2,USART0_RX,USBFS_ID,DCI_D1, EVENTOUT, I2C2_TXFRAME |
| PA11 | D7 | I/O | 5VT | Default: PA11<br>Alternate:TIMER0_CH3,USART0_CTS,USART5_TX,CAN0_RX, USBFS_DM, EVENTOUT |
| PA12 | B8 | I/O | 5VT | Default: PA12<br>Alternate:TIMER0_ETI,USART0_RTS,USART5_RX, CAN0_TX, USBFS_DP, EVENTOUT |
| PA13 | A8 | I/O | 5VT | Default: JTMS, SWDIO, PA13<br>Alternate: EVENTOUT |
| $V_{SS}$ | D6 | P | - | Default: $V_{SS}$ |
| $V_{DD}$ | E6 | P | - | Default: $V_{DD}$ |
| PA14 | A7 | I/O | 5VT | Default: JTCK, SWCLK, PA14<br>Alternate: EVENTOUT |
| PA15 | B6 | I/O | 5VT | Default: JTDI, PA15<br>Alternate:TIMER1_CH0,TIMER1_ETI,SPI0_NSS, SPI2_NSS, I2S2_WS, USART0_TX, EVENTOUT |
| PC10 | B7 | I/O | 5VT | Default: PC10<br>Alternate:SPI2_SCK,I2S2_CK,USART2_TX, UART3_TX, SDIO_D2, DCI_D8, EVENTOUT |
| PC11 | A6 | I/O | 5VT | Default: PC11<br>Alternate:I2S2_ADD_SD,SPI2_MISO,USART2_RX, UART3_RX, SDIO_D3, DCI_D4, EVENTOUT |
| PC12 | B5 | I/O | 5VT | Default: PC12<br>Alternate:I2C1_SDA,SPI2_MOSI,I2S2_SD,USART2_CK, UART4_TX, SDIO_CK, DCI_D9, EVENTOUT |
| PD2 | A5 | I/O | 5VT | Default: PD2<br>Alternate:TIMER2_ETI,UART4_RX,SDIO_CMD,DCI_D11, |



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| Pin Name | Pins | Pin Type(1) | I/O Level(2) | Functions description |
|---|---|---|---|---|
| | | | | EVENTOUT |
| PB3 | C5 | I/O | 5VT | Default: JTDO, PB3<br>Alternate:TRACESWO,TIMER1_CH1,SPI0_SCK,SPI2_SCK,<br>I2S2_CK, USART0_RX, I2C1_SDA, EVENTOUT |
| PB4 | C4 | I/O | 5VT | Default: NJTRST, PB4<br>Alternate:TIMER2_CH0,SPI0_MISO,SPI2_MISO,<br>I2S2_ADD_SD,I2C2_SDA,SDIO_D0,EVENTOUT,<br>I2C0_TXFRAME |
| PB5 | A4 | I/O | 5VT | Default: PB5<br>Alternate:TIMEC2R2_CH1,I2C0_SMBA,SPI0_MOSI,SPI2_MOSI<br>,I2S2_SD,CAN1_RX,USBHS_ULPI_D7, DCI_D10, EVENTOUT |
| PB6 | D2 | I/O | 5VT | Default: PB6<br>Alternate:TIMER3_CH0,I2C0_SCL,USART0_TX,CAN1_TX,<br>DCI_D5, EVENTOUT |
| PB7 | C2 | I/O | 5VT | Default: PB7<br>Alternate:TIMER3_CH1,I2C0_SDA,USART0_RX, DCI_VSYNC,<br>EVENTOUT |
| BOOT0 | B4 | I/O | 5VT | Default: BOOT0 |
| PB8 | A2 | I/O | 5VT | Default: PB8<br>Alternate:TIMER1_CH0, TIMER1_ETI, TIMER3_CH2,<br>TIMER9_CH0, I2C0_SCL, CAN0_RX, SDIO_D4, DCI_D6,<br>EVENTOUT |
| PB9 | A3 | I/O | 5VT | Default: PB9<br>Alternate:TIMER1_CH1, TIMER3_CH3, TIMER10_CH0,<br>I2C0_SDA, SPI1_NSS, I2S1_WS, CAN0_TX, SDIO_D5,<br>DCI_D7, EVENTOUT |
| $V_{SS}$ | C3 | P | - | Default: $V_{SS}$ |
| $V_{DD}$ | D3 | P | - | Default: $V_{DD}$ |

**Notes:**

(1) Type: I = input, O = output, P = power.

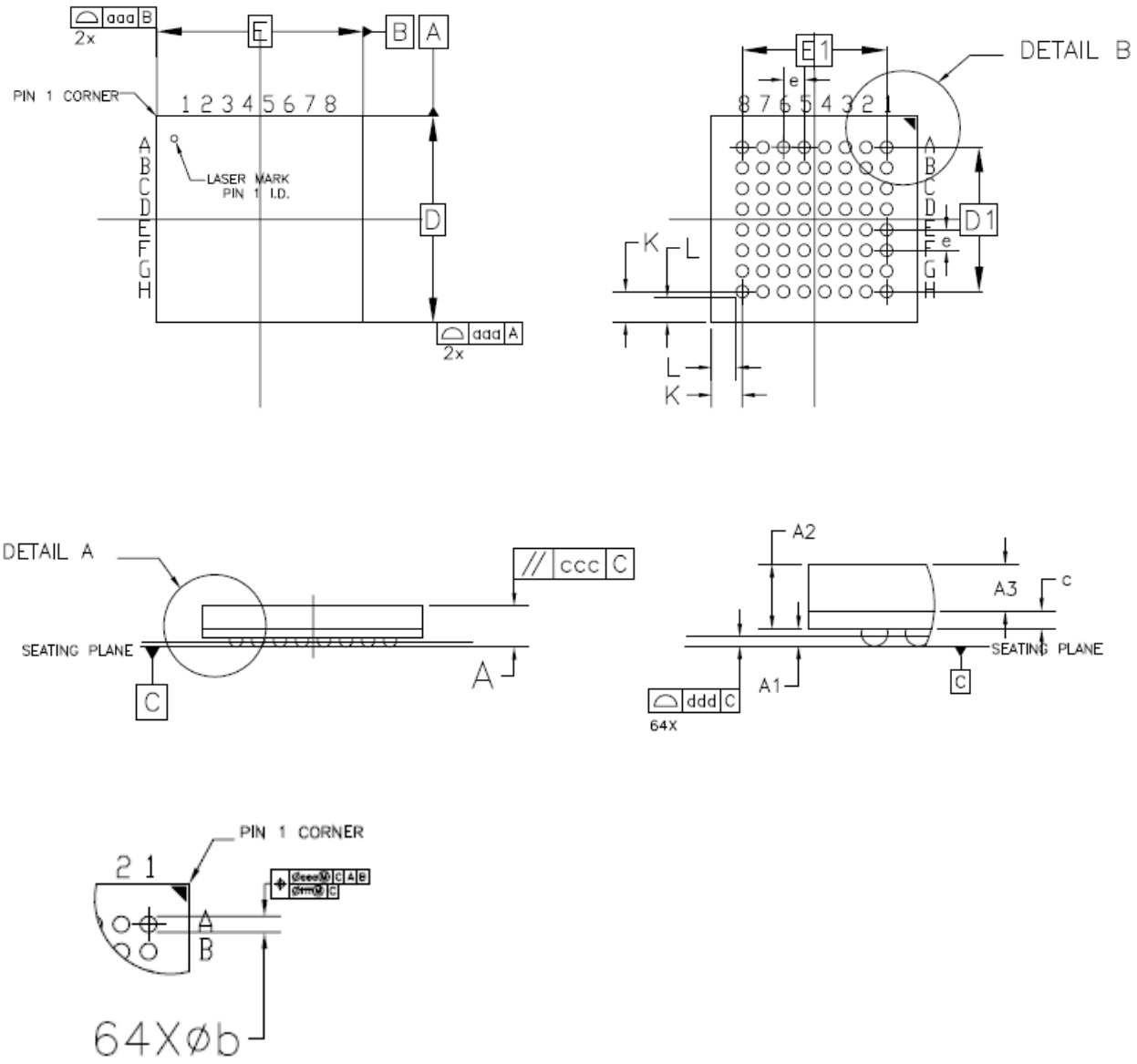
(2) I/O Level: 5VT = 5 V tolerant.



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## 1.2 BGA package outline dimensions

**Figure 1-2. BGA package outline**






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**Table 1-2. BGA package dimensions**

| Symbol | BGA64 | | |
|---|---|---|---|
| | Min | Typ | Max |
| A | 0.830 | 0.910 | 0.990 |
| A1 | 0.130 | 0.180 | 0.230 |
| A2 | 0.680 | 0.730 | 0.780 |
| A3 | 0.480 | 0.530 | 0.580 |
| c | 0.170 | 0.200 | 0.230 |
| D | 4.900 | 5.000 | 5.100 |
| E | 4.900 | 5.000 | 5.100 |
| D1 | 3.400 | 3.500 | 3.600 |
| E1 | 3.400 | 3.500 | 3.600 |
| e | 0.450 | 0.500 | 0.550 |
| b | 0.200 | 0.250 | 0.300 |
| L | 0.625 REF | | |
| K | 0.750 REF | | |
| aaa | 0.150 REF | | |
| ccc | 0.100 REF | | |
| ddd | 0.080 REF | | |
| eee | 0.150 REF | | |
| fff | 0.080 REF | | |

(Original dimensions are in millimeters)



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