# GigaDevice Semiconductor Inc.

# GD32F170xx
# ARM® Cortex®-M3 32-bit MCU

Datasheet

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# Table of Contents

**List of Figures** ..... **3**

**List of Tables** ..... **4**

**1 General description** ..... **5**

**2 Device overview** ..... **6**

2.1 Device information ..... 6
2.2 Block diagram ..... 7
2.3 Pinouts and pin assignment ..... 8
2.4 Memory map ..... 10
2.5 Clock tree ..... 11
2.6 Pin definitions ..... 12

**3 Functional description** ..... **19**

3.1 ARM® Cortex®-M3 core ..... 19
3.2 On-chip memory ..... 19
3.3 Clock, reset and supply management ..... 20
3.4 Boot modes ..... 20
3.5 Power saving modes ..... 21
3.6 Analog to digital converter (ADC) ..... 21
3.7 DMA ..... 22
3.8 General-purpose inputs/outputs (GPIOs) ..... 22
3.9 Timers and PWM generation ..... 22
3.10 Real time clock (RTC) ..... 23
3.11 Inter-integrated circuit (I2C) ..... 24
3.12 Serial peripheral interface (SPI) ..... 24
3.13 Universal synchronous asynchronous receiver transmitter (USART) ..... 25
3.14 Controller area network (CAN) ..... 25
3.15 Debug mode ..... 25
3.16 Package and operation temperature ..... 25

**4 Electrical characteristics** ..... **26**

4.1 Absolute maximum ratings ..... 26
4.2 Recommended DC characteristics ..... 26
4.3 Power consumption ..... 27
4.4 EMC characteristics ..... 28
4.5 Power supply supervisor characteristics ..... 28
4.6 Electrical sensitivity ..... 29
4.7 External clock characteristics ..... 29
4.8 Internal clock characteristics ..... 30
4.9 PLL characteristics ..... 31
4.10 Memory characteristics ..... 31



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4.11 GPIO characteristics ..... 32
4.12 ADC characteristics ..... 33
4.13 SPI characteristics ..... 34
4.14 I2C characteristics ..... 34
4.15 USART characteristics ..... 34
**5 Package information ..... 35**
5.1 QFN package outline dimensions ..... 35
5.2 LQFP package outline dimensions ..... 36
**6 Ordering Information ..... 38**
**7 Revision History ..... 39**



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# List of Figures

Figure 1. GD32F170xx block diagram ..... 7
Figure 2. GD32F170Rx LQFP64 pinouts ..... 8
Figure 3. GD32F170Cx LQFP48 pinouts ..... 8
Figure 4. GD32F170Tx QFN36 pinouts ..... 9
Figure 5. GD32F170xx memory map ..... 10
Figure 6. GD32F170xx clock tree ..... 11
Figure 7. QFN package outline ..... 35
Figure 8. LQFP package outline ..... 36



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# List of Tables

Table 1. GD32F170xx devices features and peripheral list ..... 6
Table 2. GD32F170xx pin definitions ..... 12
Table 3. Port A alternate functions summary ..... 16
Table 4. Port B alternate functions summary ..... 17
Table 5. Port C & D & F alternate functions summary ..... 18
Table 6. Absolute maximum ratings ..... 26
Table 7. DC operating conditions ..... 26
Table 8. Power consumption characteristics ..... 27
Table 9. EMS characteristics ..... 28
Table 10. EMI characteristics ..... 28
Table 11. Power supply supervisor characteristics ..... 28
Table 12. ESD characteristics ..... 29
Table 13. Static latch-up characteristics ..... 29
Table 14. High speed external clock (HSE) generated from a crystal/ceramic characteristics ..... 29
Table 15. Low speed external clock (LSE) generated from a crystal/ceramic characteristics ..... 30
Table 16. High speed internal clock (HSI) characteristics ..... 30
Table 17. Low speed internal clock (LSI) characteristics ..... 30
Table 18. PLL characteristics ..... 31
Table 19. Flash memory characteristics ..... 31
Table 20. I/O port characteristics ..... 32
Table 21. ADC characteristics ..... 33
Table 22. ADC $R_{AIN\ max}$ for $f_{ADC}$=28MHz ..... 33
Table 23. SPI characteristics ..... 34
Table 24. I2C characteristics ..... 34
Table 25. USART characteristics ..... 34
Table 26. QFN package dimensions ..... 35
Table 27. LQFP package dimensions ..... 37
Table 28. Part ordering code for GD32F170xx devices ..... 38
Table 29. Revision history ..... 39



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# 1 General description

The GD32F170xx device belongs to the 5V value line of GD32 MCU family. It is a 32-bit general-purpose microcontroller based on the high performance ARM® Cortex®-M3 RISC core with best ratio in terms of processing power, reduced power consumption and peripheral set. The Cortex®-M3 is a next generation processor core which is tightly coupled with a Nested Vectored Interrupt Controller (NVIC), SysTick timer and advanced debug support.

The GD32F170xx device incorporates the ARM® Cortex®-M3 32-bit processor core operating at 48 MHz frequency with Flash accesses zero wait states to obtain maximum efficiency. It provides up to 64 KB on-chip Flash memory and up to 8 KB SRAM memory. An extensive range of enhanced I/Os and peripherals connected to two APB buses. The device offer one 12-bit ADC, up to five general-purpose 16-bit timers, a general-purpose 32-bit timer, a PWM advanced-control timer, as well as standard and advanced communication interfaces: up to three SPIs, three $I^2C$s and two USARTs, two CAN2.0B with a CAN PHY.

The device operates from a 2.5 to 5.5V power supply and available in –40 to +85 °C temperature range. Several power saving modes provide the flexibility for maximum optimization between wakeup latency and power consumption, an especially important consideration in low power applications.

The above features make the GD32F170xx devices suitable for a wide range of applications, especially in areas such as industrial control, motor drives, user interface, power monitor and alarm systems, consumer and handheld equipment, home appliances, E-bike and so on.






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# 2 Device overview

## 2.1 Device information

**Table 1. GD32F170xx devices features and peripheral list**

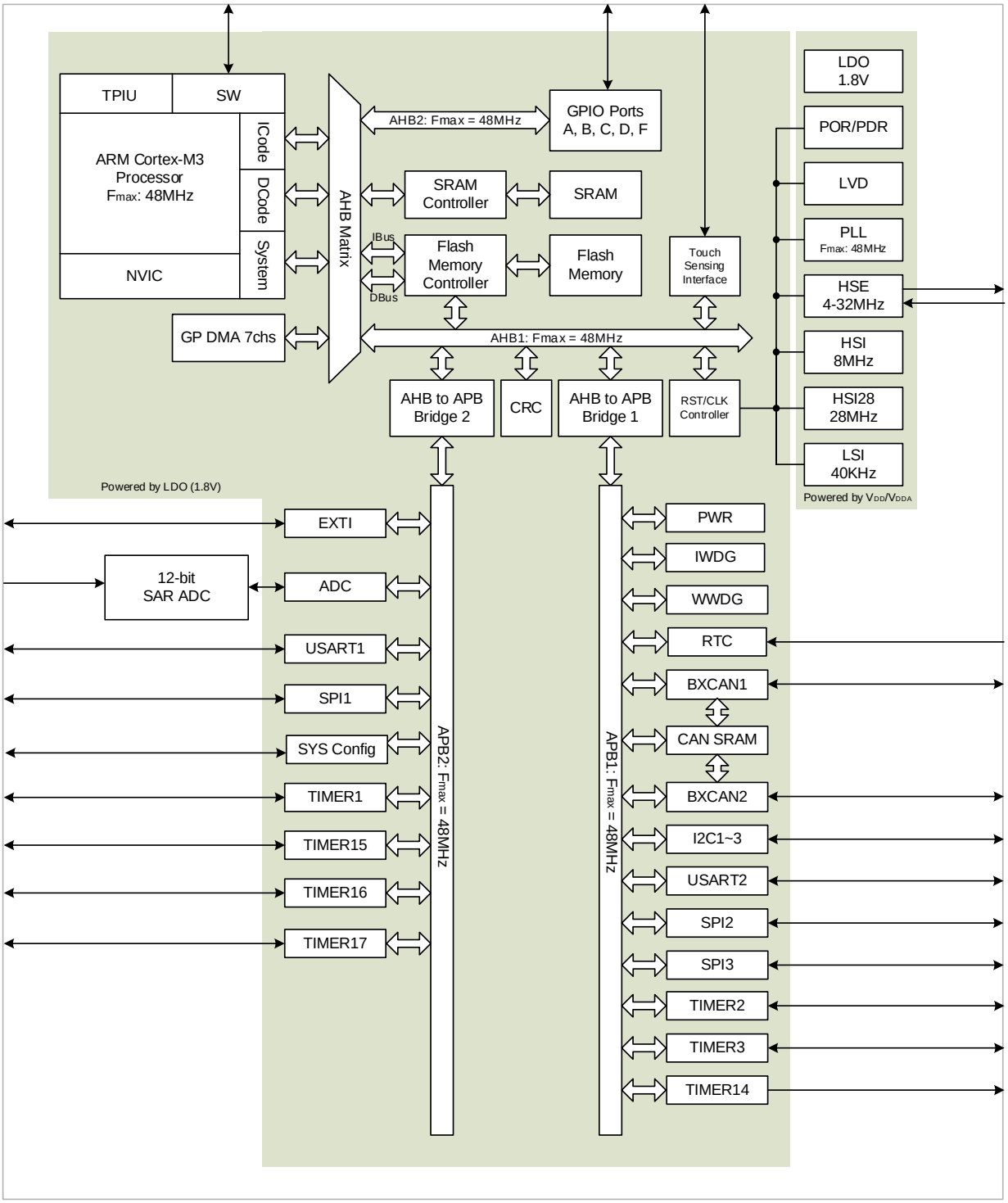
| Part Number | | GD32F170xx | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | T4 | T6 | T8 | C4 | C6 | C8 | R8 |
| Flash (KB) | | 16 | 32 | 64 | 16 | 32 | 64 | 64 |
| SRAM (KB) | | 4 | 4 | 8 | 4 | 4 | 8 | 8 |
| Timers | 32-bit GP | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | 16-bit GP | 4 | 4 | 5 | 4 | 4 | 5 | 5 |
| | 16-bit Adv. | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | SysTick | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | Watchdog | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| | RTC | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Connectivity | USART | 1 | 2 | 2 | 1 | 2 | 2 | 2 |
| | I2C | 1 | 1 | 3 | 1 | 1 | 3 | 3 |
| | SPI | 1 | 1 | 3 | 1 | 1 | 3 | 3 |
| | CAN 2.0B | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| GPIO | | 28 | 28 | 28 | 39 | 39 | 39 | 55 |
| EXTI | | 16 | 16 | 16 | 16 | 16 | 16 | 16 |
| ADC | Units | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | Channels (Ext.) | 10 | 10 | 10 | 10 | 10 | 10 | 16 |
| | Channels (Int.) | 3 | 3 | 3 | 3 | 3 | 3 | 3 |
| Package | | QFN36 | | | LQFP48 | | | LQFP64 |



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## 2.2 Block diagram

**Figure 1. GD32F170xx block diagram**






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## 2.3 Pinouts and pin assignment

**Figure 2. GD32F170Rx LQFP64 pinouts**

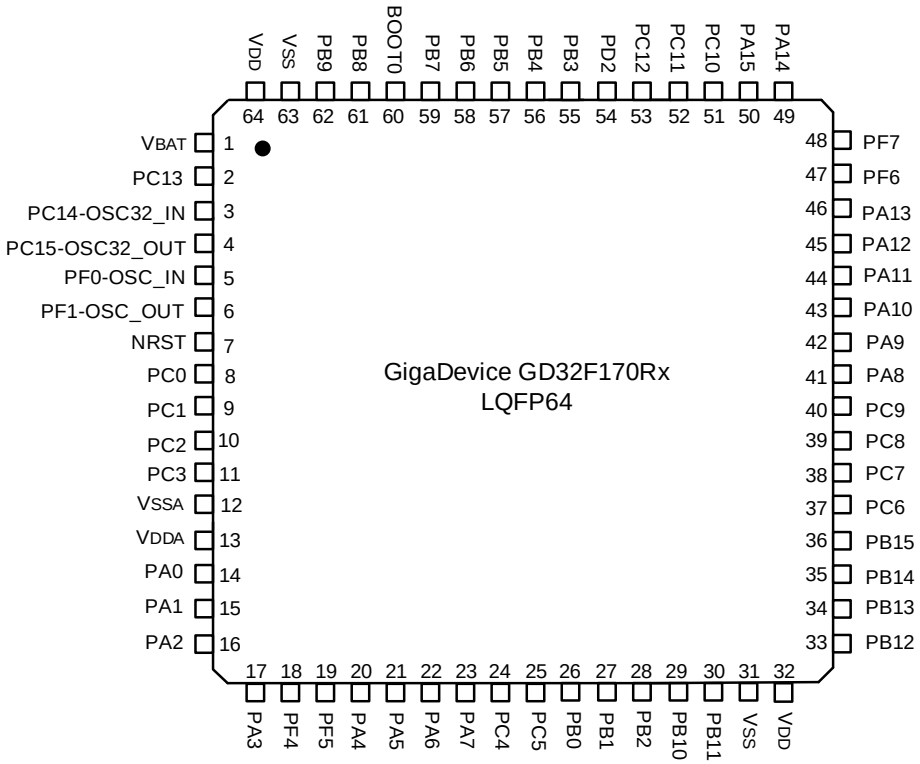
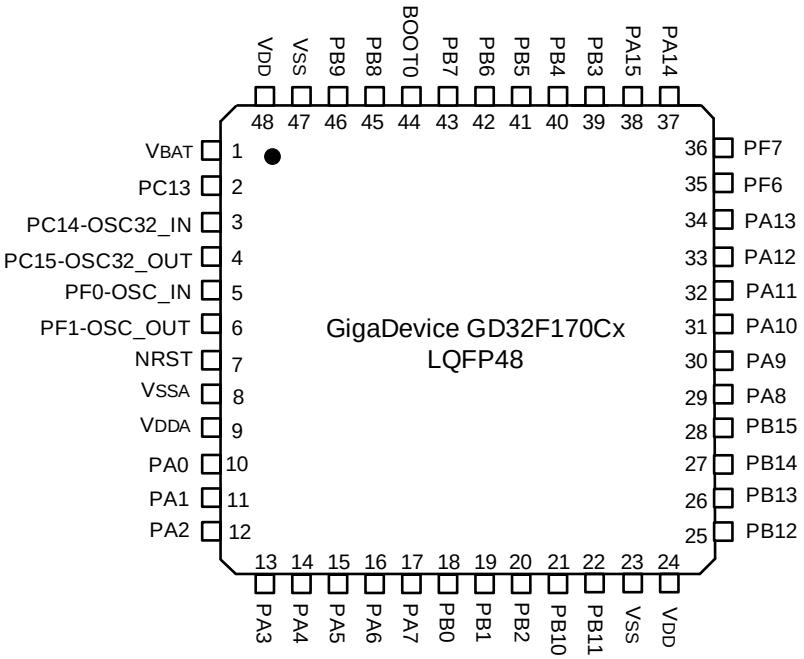


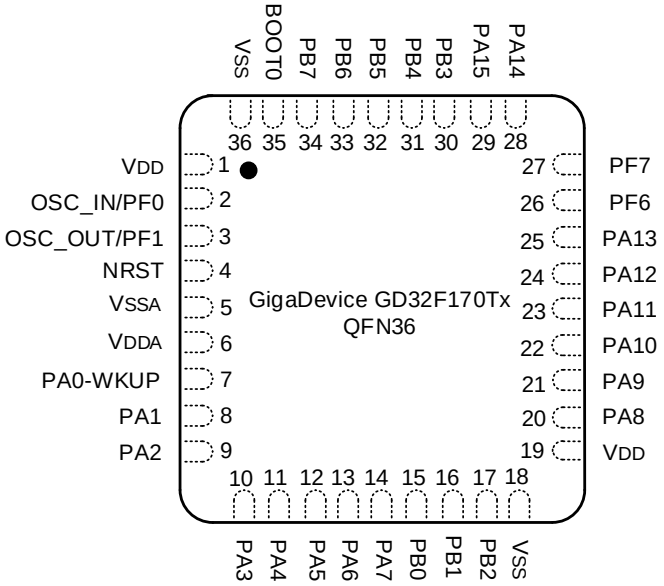

**Figure 3. GD32F170Cx LQFP48 pinouts**






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**Figure 4. GD32F170Tx QFN36 pinouts**

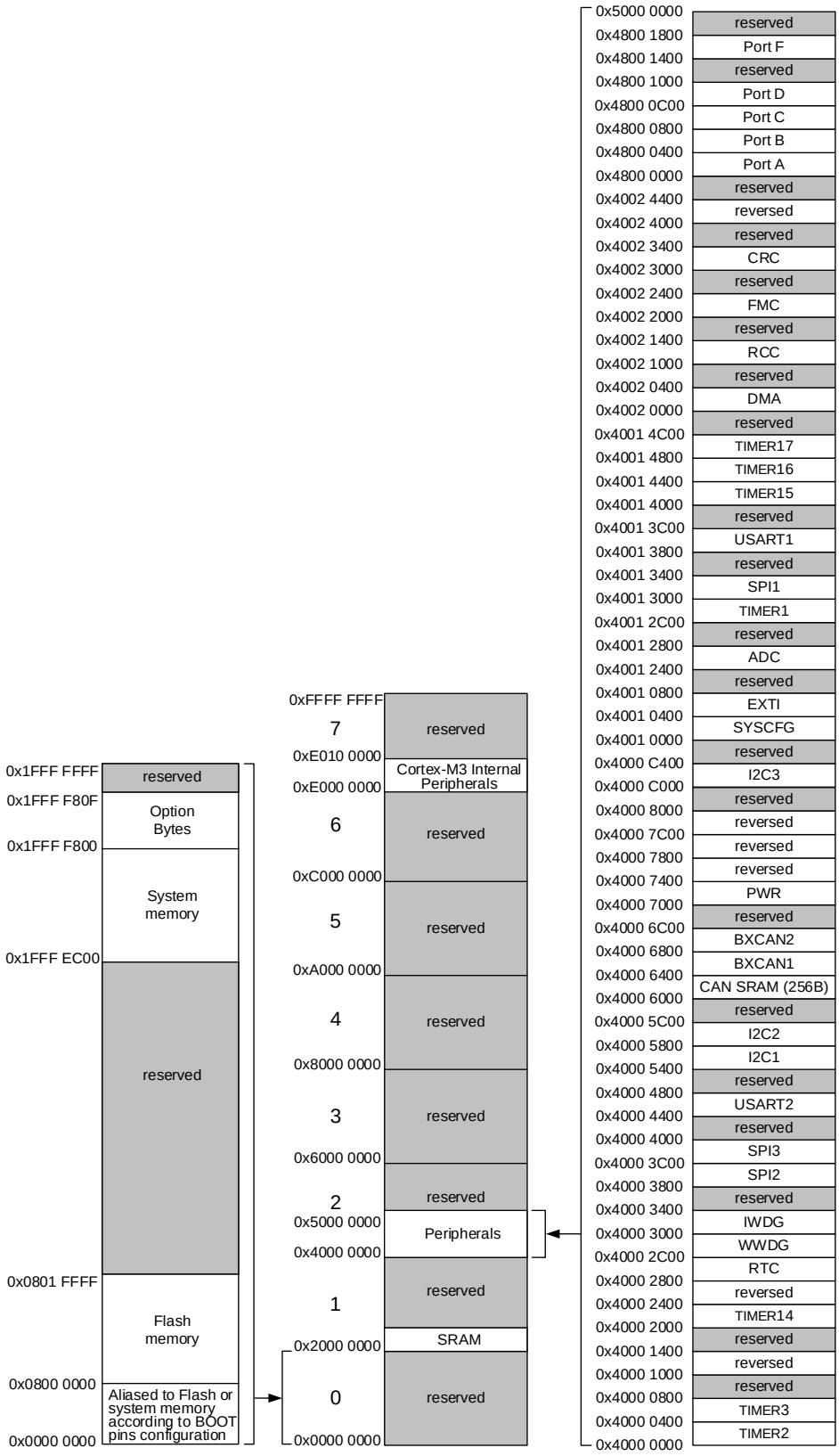





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## 2.4 Memory map

**Figure 5. GD32F170xx memory map**

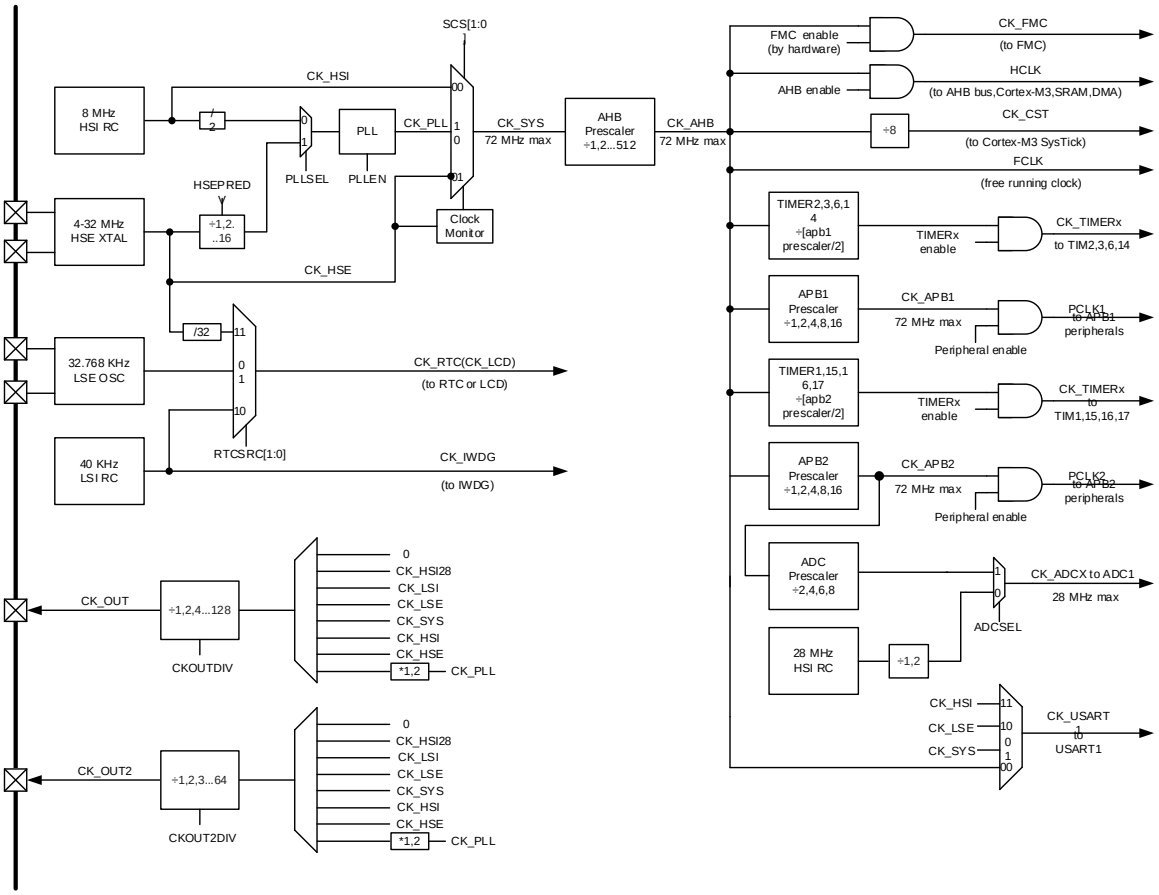





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## 2.5 Clock tree

**Figure 6. GD32F170xx clock tree**




**Legend:**

HSE = High speed external clock

HSI = High speed internal clock

LSE = Low speed external clock

LSI = Low speed internal clock



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## 2.6 Pin definitions

**Table 2. GD32F170xx pin definitions**

| Pin Name | Pins | | | Pin Type(1) | I/O(2) Level | Functions description |
|---|---|---|---|---|---|---|
| | LQFP64 | LQFP48 | QFN36 | | | |
| $V_{BAT}$ | 1 | 1 | - | P | | Default: $V_{BAT}$ |
| PC13-TAMPER-RTC | 2 | 2 | - | I/O | | Default: PC13<br>Additional: RTC_TAMP1, RTC_TS, RTC_OUT, WKUP2 |
| PC14-OSC32_IN | 3 | 3 | - | I/O | | Default: PC14<br>Additional: OSC32_IN |
| PC15-OSC32_OUT | 4 | 4 | - | I/O | | Default: PC15<br>Additional: OSC32_OUT |
| PF0-OSC_IN | 5 | 5 | 2 | I/O | HVT | Default: PF0<br>Additional: OSC_IN |
| PF1-OSC_OUT | 6 | 6 | 3 | I/O | HVT | Default: PF1<br>Additional: OSC_OUT |
| NRST | 7 | 7 | 4 | I/O | | Default: NRST |
| PC0 | 8 | - | - | I/O | | Default: PC0<br>Alternate: EVENTOUT, I2C3_SCL<br>Additional: ADC_IN10 |
| PC1 | 9 | - | - | I/O | | Default: PC1<br>Alternate: EVENTOUT, I2C3_SDA<br>Additional: ADC_IN11 |
| PC2 | 10 | - | - | I/O | | Default: PC2<br>Alternate: EVENTOUT, I2C3_SMBA<br>Additional: ADC_IN12 |
| PC3 | 11 | - | - | I/O | | Default: PC3<br>Alternate: EVENTOUT<br>Additional: ADC_IN13, I2C3_TXFRAME |
| $V_{SSA}$ | 12 | 8 | 5 | P | | Default: $V_{SSA}$ |
| $V_{DDA}$ | 13 | 9 | 6 | P | | Default: $V_{DDA}$ |
| PA0-WKUP | 14 | 10 | 7 | I/O | | Default: PA0<br>Alternate: USART1_CTS(3), USART2_CTS(4), TM2_CH1_ETR, I2C2_SCL,<br>Additional: ADC_IN0, RTC_TAMP2, WKUP1 |
| PA1 | 15 | 11 | 8 | I/O | | Default: PA1<br>Alternate: USART1_RTS(3), USART2_RTS(4), TM2_CH2, I2C2_SDA, EVENTOUT<br>Additional: ADC_IN1 |
| PA2 | 16 | 12 | 9 | I/O | | Default: PA2<br>Alternate: USART1_TX(3), USART2_TX(4), TM2_CH3, TM15_CH1, I2C2_SMBA |



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| Pin Name | Pins | | | Pin Type(1) | I/O(2) Level | Functions description |
|---|---|---|---|---|---|---|
| | LQFP64 | LQFP48 | QFN36 | | | |
| | | | | | | Additional: ADC_IN2 |
| PA3 | 17 | 13 | 10 | I/O | | Default: PA3<br>Alternate: USART1_RX(3), USART2_RX(4), TM2_CH4, TM15_CH2, I2C2_TXFRAME<br>Additional: ADC_IN3 |
| PF4 | 18 | - | - | I/O | HVT | Default: PF4<br>Alternate: EVENTOUT |
| PF5 | 19 | - | - | I/O | HVT | Default: PF5<br>Alternate: EVENTOUT |
| PA4 | 20 | 14 | 11 | I/O | | Default: PA4<br>Alternate: SPI1_NSS, USART1_CK(3), USART2_CK(4), TM14_CH1, SPI2_NSS , SPI3_NSS<br>Additional: ADC_IN4 |
| PA5 | 21 | 15 | 12 | I/O | | Default: PA5<br>Alternate: SPI1_SCK, TM2_CH1_ETR<br>Additional: ADC_IN5, CANH |
| PA6 | 22 | 16 | 13 | I/O | | Default: PA6<br>Alternate: SPI1_MISO, TM3_CH1, TM1_BKIN, TM16_CH1, EVENTOUT<br>Additional: ADC_IN6, CANL |
| PA7 | 23 | 17 | 14 | I/O | | Default: PA7<br>Alternate: SPI1_MOSI, TM3_CH2, TM14_CH1, TM1_CH1N, TM17_CH1, EVENTOUT<br>Additional: ADC_IN7 |
| PC4 | 24 | - | - | I/O | | Default: PC4<br>Alternate: EVENTOUT<br>Additional: ADC_IN14 |
| PC5 | 25 | - | - | I/O | | Default: PC5<br>Alternate: TSI_G3_IO1<br>Additional: ADC_IN15 |
| PB0 | 26 | 18 | 15 | I/O | | Default: PB0<br>Alternate: TM3_CH3, TM1_CH2N, USART2_RX, EVENTOUT SPI3_NSS<br>Additional: ADC_IN8, IREF |
| PB1 | 27 | 19 | 16 | I/O | | Default: PB1<br>Alternate: TM3_CH4, TM14_CH1, TM1_CH3N, SPI2_SCK<br>Additional: ADC_IN9, VREF |
| PB2 | 28 | 20 | 17 | I/O | HVT | Default: PB2 |
| PB10 | 29 | 21 | - | I/O | HVT | Default: PB10<br>Alternate: I2C2_SCL(4), TIM2_CH3, I2C1_SCL(3), SPI2_IO2 |
| PB11 | 30 | 22 | - | I/O | HVT | Default: PB11<br>Alternate: I2C2_SDA(4), TM2_CH4, EVENTOUT, I2C1_SDA(3), SPI2_IO3 |



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| Pin Name | Pins | | | Pin Type(1) | I/O(2) Level | Functions description |
|---|---|---|---|---|---|---|
| | LQFP64 | LQFP48 | QFN36 | | | |
| $V_{SS}$ | 31 | 23 | 18 | P | | Default: $V_{SS}$ |
| $V_{DD}$ | 32 | 24 | 19 | P | | Default: $V_{DD}$ |
| PB12 | 33 | 25 | - | I/O | HVT | Default: PB12<br>Alternate: SPI1_NSS(3), SPI2_NSS(4), TM1_BKIN, I2C2_SMBA, EVENTOUT, CAN2_RX |
| PB13 | 34 | 26 | - | I/O | HVT | Default: PB13<br>Alternate: SPI1_SCK(3), SPI2_SCK(4), TM1_CH1N, I2C2_TXFRAME, CAN2_TX |
| PB14 | 35 | 27 | - | I/O | HVT | Default: PB14<br>Alternate: SPI1_MISO(3), SPI2_MISO(4), TM1_CH2N, TM15_CH1 |
| PB15 | 36 | 28 | - | I/O | HVT | Default: PB15<br>Alternate: SPI1_MOSI(3), SPI2_MOSI(4), TIM1_CH3N, TM15_CH1N, TM15_CH2<br>Additional: RTC_REFIN |
| PC6 | 37 | - | - | I/O | HVT | Default: PC6<br>Alternate: TM3_CH1, SEG24, I2C3_TXFRAME |
| PC7 | 38 | - | - | I/O | HVT | Default: PC7<br>Alternate: TM3_CH2, I2C3_SCL |
| PC8 | 39 | - | - | I/O | HVT | Default: PC8<br>Alternate: TM3_CH3, I2C3_SDA |
| PC9 | 40 | - | - | I/O | HVT | Default: PC9<br>Alternate: TM3_CH4, I2C3_SMBA, MCO2 |
| PA8 | 41 | 29 | 20 | I/O | HVT | Default: PA8<br>Alternate: USART1_CK, TM1_CH1, MCO, USART2_TX, EVENTOUT, I2C1_TXFRAME |
| PA9 | 42 | 30 | 21 | I/O | HVT | Default: PA9<br>Alternate: USART1_TX, TM1_CH2, TM15_BKIN , I2C1_SCL, SPI2_IO2 |
| PA10 | 43 | 31 | 22 | I/O | HVT | Default: PA10<br>Alternate: USART1_RX, TM1_CH3, TM17_BKIN, I2C1_SDA, SPI2_IO3 |
| PA11 | 44 | 32 | 23 | I/O | HVT | Default: PA11<br>Alternate: USART1_CTS, TM1_CH4, EVENTOUT, CAN1_RX |
| PA12 | 45 | 33 | 24 | I/O | HVT | Default: PA12<br>Alternate: USART1_RTS, TM1_ETR, EVENTOUT, CAN1_TX |
| PA13 | 46 | 34 | 25 | I/O | HVT | Default: PA13/SWDAT<br>Alternate: IR_OUT, SWDAT, SPI2_MISO, I2C1_SMBA |
| PF6 | 47 | 35 | 26 | I/O | HVT | Default: PF6<br>Alternate: I2C2_SCL(4), I2C1_SCL(3) |
| PF7 | 48 | 36 | 27 | I/O | HVT | Default: PF7<br>Alternate: I2C2_SDA(4), I2C1_SDA(3) |
| PA14 | 49 | 37 | 28 | I/O | HVT | Default: PA14/SWCLK |



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| Pin Name | Pins | | | Pin Type(1) | I/O(2) Level | Functions description |
|---|---|---|---|---|---|---|
| | LQFP64 | LQFP48 | QFN36 | | | |
| | | | | | | Alternate: USART1_TX(3), USART2_TX(4), SWCLK, SPI2_MOSI |
| PA15 | 50 | 38 | 29 | I/O | HVT | Default: PA15<br>Alternate: SPI1_NSS , USART1_RX(3), USART2_RX(4), TM2_CH1_ETR, SPI2_NSS, EVENTOUT, SPI3_NSS, I2C1_SMBA |
| PC10 | 51 | - | - | I/O | HVT | Default: PC10<br>Alternate: SPI3_SCK |
| PC11 | 52 | - | - | I/O | HVT | Default: PC11<br>Alternate: SPI3_MISO |
| PC12 | 53 | - | - | I/O | HVT | Default: PC12<br>Alternate: SPI3_MOSI |
| PD2 | 54 | - | - | I/O | HVT | Default: PD2<br>Alternate: TM3_ETR |
| PB3 | 55 | 39 | 30 | I/O | HVT | Default: PB3<br>Alternate: SPI1_SCK, TM2_CH2, EVENTOUT, SPI3_SCK, I2C1_TXFRAME |
| PB4 | 56 | 40 | 31 | I/O | HVT | Default: PB4<br>Alternate: SPI1_MISO, TM3_CH1, EVENTOUT, SPI3_MISO, I2C3_SMBA |
| PB5 | 57 | 41 | 32 | I/O | HVT | Default: PB5<br>Alternate: SPI1_MOSI, I2C1_SMBA, TM16_BKIN, TM3_CH2, SPI3_MOSI, I2C3_TXFRAME, CAN2_RX |
| PB6 | 58 | 42 | 33 | I/O | HVT | Default: PB6<br>Alternate: I2C1_SCL, USART1_TX, TM16_CH1N, I2C3_SCL, CAN2_TX |
| PB7 | 59 | 43 | 34 | I/O | HVT | Default: PB7<br>Alternate: I2C1_SDA, USART1_RX, TM17_CH1N, I2C3_SDA |
| BOOT0 | 60 | 44 | 35 | I | | Default: BOOT0 |
| PB8 | 61 | 45 | - | I/O | HVT | Default: PB8<br>Alternate: I2C1_SCL, TM16_CH1, CAN1_RX |
| PB9 | 62 | 46 | - | I/O | HVT | Default: PB9<br>Alternate: I2C1_SDA, IR_OUT, TM17_CH1, EVENTOUT, COM3, CAN1_TX |
| $V_{SS}$ | 63 | 47 | 36 | P | | Default: $V_{SS}$ |
| $V_{DD}$ | 64 | 48 | 1 | P | | Default: $V_{DD}$ |

Notes:

1. Type: I = input, O = output, P = power.
2. I/O Level: HVT = High Voltage Tolerant.
3. This feature is available on GD32F170x4 devices only.
4. This feature is available on GD32F170x8 and GD32F170x6 devices only.



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**Table 3. Port A alternate functions summary**

| Pin Name | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF9 |
|---|---|---|---|---|---|---|---|---|---|
| PA0 | | USART1_CTS(1) USART2_CTS(2) | TM2_CH1_ ETR | | I2C2_SCL | | | | |
| PA1 | EVENTOUT | USART1_RTS(1) USART2_RTS(2) | TM2_CH2 | | I2C2_SDA | | | | |
| PA2 | TM15_CH1 | USART1_TX(1) USART2_TX(2) | TM2_CH3 | | I2C2_SMBA | | | | |
| PA3 | TM15_CH2 | USART1_RX(1) USART2_RX(2) | TM2_CH4 | | I2C2_TXFRAME | | | | |
| PA4 | SPI1_NSS | USART1_CK(1) USART2_CK(2) | | | TM14_CH1 | SPI3_NSS | SPI2_NSS | | |
| PA5 | SPI1_SCK | | TM2_CH1_ ETR | | | | | | |
| PA6 | SPI1_MISO | TM3_CH1 | TM1_BKIN | | | TM16_CH1 | EVENTOUT | | |
| PA7 | SPI1_MOSI | TM3_CH2 | TM1_CH1N | | TM14_CH1 | TM17_CH1 | EVENTOUT | | |
| PA8 | MCO | USART1_CK | TM1_CH1 | EVENTOUT | USART2_TX | I2C1_TXFRAME | | | |
| PA9 | TM15_BKIN | USART1_TX | TM1_CH2 | | I2C1_SCL | | SPI2_IO2 | | |
| PA10 | TM17_BKIN | USART1_RX | TM1_CH3 | | I2C1_SDA | | SPI2_IO3 | | |
| PA11 | EVENTOUT | USART1_CTS | TM1_CH4 | | | | | | CAN1_RX |
| PA12 | EVENTOUT | USART1_RTS | TM1_ETR | | | | | | CAN1_TX |
| PA13 | SWDAT | IR_OUT | | | | I2C1_SMBA | SPI2_MISO | | |
| PA14 | SWCLK | USART1_TX(1) USART2_TX(2) | | | | | SPI2_MOSI | | |
| PA15 | SPI1_NSS | USART1_RX(1) USART2_RX(2) | TM2_CH1_ ETR | EVENTOUT | I2C1_SMBA | SPI3_NSS | SPI2_NSS | | |

1. This feature is available on GD32F170x4 devices only.
2. This feature is available on GD32F170x8 and GD32F170x6 devices only.



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**Table 4. Port B alternate functions summary**

| Pin Name | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF9 |
|---|---|---|---|---|---|---|---|---|---|
| PB0 | EVENTOUT | TM3_CH3 | TM1_CH2N | | USART2_RX | SPI3_NSS | | | |
| PB1 | TM14_CH1 | TM3_CH4 | TM1_CH3N | | | | SPI2_SCK | | |
| PB2 | | | | | | | | | |
| PB3 | SPI1_SCK | EVETOUT | TM2_CH2 | | I2C1_TXFRAME | SPI3_SCK | | | |
| PB4 | SPI1_MISO | TM3_CH1 | EVENTOUT | | I2C3_SMBA | SPI3_MISO | | | |
| PB5 | SPI1_MOSI | TM3_CH2 | TM16_BKIN | I2C1_SMBA | I2C3_TXFRAME | SPI3_MOSI | | | CAN2_RX |
| PB6 | USART1_TX | I2C1_SCL | TM16_CH1N | | I2C3_SCL | | | | CAN2_TX |
| PB7 | USART1_RX | I2C1_SDA | TM17_CH1N | | I2C3_SDA | | | | |
| PB8 | | I2C1_SCL | TM16_CH1 | | | | | | CAN1_RX |
| PB9 | IR_OUT | I2C1_SDA | TM17_CH1 | EVENTOUT | | | | | CAN1_TX |
| PB10 | | I2C1_SCL(1) I2C2_SCL(2 | TM2_CH3 | | | | SPI2_IO2 | | |
| PB11 | EVENTOUT | I2C1_SDA(1) I2C2_SDA(2) | TM2_CH4 | | | | SPI2_IO3 | | |
| PB12 | SPI1_NSS(1) SPI2_NSS(2) | EVENTOUT | TM1_BKIN | | I2C2_SMBA | | | | CAN2_RX |
| PB13 | SPI1_SCK(1) SPI2_SCK(2) | | TM1_CH1N | | I2C2_TXFRAME | | | | CAN2_TX |
| PB14 | SPI1_MISO(1) SPI2_MISO(2) | TM15_CH1 | TM1_CH2N | | | | | | |
| PB15 | SPI1_MOSI(1) SPI2_MOSI(2) | TM15_CH2 | TM1_CH3N | TM15_CH1N | | | | | |

1. This feature is available on GD32F170x4 devices only.
2. This feature is available on GD32F170x8 and GD32F170x6 devices only.



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**Table 5. Port C & D & F alternate functions summary**

| Pin Name | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF9 |
|---|---|---|---|---|---|---|---|---|---|
| PC0 | EVENTOUT | I2C3_SCL | | | | | | | |
| PC1 | EVENTOUT | I2C3_SDA | | | | | | | |
| PC2 | EVENTOUT | I2C3_SMBA | | | | | | | |
| PC3 | EVENTOUT | I2C3_TXFRAME | | | | | | | |
| PC4 | EVENTOUT | | | | | | | | |
| PC5 | | | | | | | | | |
| PC6 | TM3_CH1 | I2C3_TXFRAME | | | | | | | |
| PC7 | TM3_CH2 | I2C3_SCL | | | | | | | |
| PC8 | TM3_CH3 | I2C3_SDA | | | | | | | |
| PC9 | TM3_CH4 | I2C3_SMBA | | MCO2 | | | | | |
| PC10 | SPI3_SCK | | | | | | | | |
| PC11 | SPI3_MISO | | | | | | | | |
| PC12 | SPI3_MOSI | | | | | | | | |
| PD2 | TM3_ETR | | | | | | | | |
| PF4 | EVENTOUT | | | | | | | | |
| PF5 | EVENTOUT | | | | | | | | |
| PF6 | I2C1_SCL(1)<br>I2C2_SCL(2) | | | | | | | | |
| PF7 | I2C1_SDA(1)<br>I2C2_SDA(2) | | | | | | | | |

1. This feature is available on GD32F170x4 devices only.
2. This feature is available on GD32F170x8 and GD32F170x6 devices only.



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# 3 Functional description

## 3.1 ARM® Cortex®-M3 core

The Cortex®-M3 processor is the latest generation of ARM® processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

- 32-bit ARM® Cortex®-M3 processor core
- Up to 48 MHz operation frequency
- Single-cycle multiplication and hardware divider
- Integrated Nested Vectored Interrupt Controller (NVIC)
- 24-bit SysTick timer

The Cortex®-M3 processor is based on the ARMv7 architecture and supports both Thumb and Thumb-2 instruction sets. Some system peripherals listed below are also provided by Cortex®-M3:

- Internal Bus Matrix connected with ICode bus, DCode bus, system bus, Private Peripheral Bus (PPB) and debug accesses (AHB-AP)
- Nested Vectored Interrupt Controller (NVIC)
- Flash Patch and Breakpoint (FPB)
- Data Watchpoint and Trace (DWT)
- Instrument Trace Macrocell (ITM)
- Serial Wire JTAG Debug Port (SWJ-DP)
- Trace Port Interface Unit (TPIU)

## 3.2 On-chip memory

- Up to 64 Kbytes of Flash memory
- Up to 8 Kbytes of SRAM with hardware parity checking

The ARM® Cortex®-M3 processor is structured in Harvard architecture which can use separate buses to fetch instructions and load/store data. 64 Kbytes of inner Flash and 8 Kbytes of inner SRAM at most is available for storing programs and data, both accessed (R/W) at CPU clock speed with zero wait states. The Figure 5. GD32F170xx memory map shows the memory map of the GD32F170xx series of devices, including code, SRAM, peripheral, and other pre-defined regions.



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## 3.3 Clock, reset and supply management

- Internal 8 MHz factory-trimmed RC and external 4 to 32 MHz crystal oscillator
- Internal 40 KHz RC calibrated oscillator and external 32.768 KHz crystal oscillator
- Integrated system clock PLL
- 2.5 to 5.5 V application supply and I/Os
- Supply Supervisor: POR (Power On Reset), PDR (Power Down Reset), and low voltage detector (LVD)

The Clock Control Unit (CCU) provides a range of oscillator and clock functions. These include speed internal RC oscillator and external crystal oscillator, high speed and low speed two types. Several prescalers allow the frequency configuration of the AHB and two APB domains. The maximum frequency of the AHB and two APB domains is 72 MHz. See Figure 9 for details on the clock tree.

The Reset Control Unit (RCU) controls three kinds of reset: system reset resets the processor core and peripheral IP components. Power-on reset (POR) and power-down reset (PDR) are always active, and ensures proper operation starting from 1.95V and down to 1.9V. The device remains in reset mode when $V_{DD}$ is below a specified threshold. The embedded low voltage detector (LVD) monitors the power supply, compares it to the voltage threshold and generates an interrupt as a warning message for leading the MCU into security.

Power supply schemes:

- $V_{DD}$ range: 2.5 to 5.5 V, external power supply for I/Os and the internal regulator. Provided externally through $V_{DD}$ pins.
- $V_{DDA}$ range: 2.5 to 5.5 V, external analog power supplies for ADC, reset blocks, RCs and PLL. $V_{DDA}$ and $V_{SSA}$ must be connected to $V_{DD}$ and $V_{SS}$, respectively.
- $V_{BAT}$ range: 1.8 to 5.5 V, power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when $V_{DD}$ is not present.

## 3.4 Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from main Flash memory (default)
- Boot from system memory
- Boot from on-chip SRAM

In default condition, boot from main Flash memory is selected. The boot loader is located in the internal boot ROM memory (system memory). It is used to reprogram the Flash memory by using USART1 in device mode.



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## 3.5 Power saving modes

The MCU supports three kinds of power saving modes to achieve even lower power consumption. They are Sleep mode, Deep-sleep mode, and Standby mode. These operating modes reduce the power consumption and allow the application to achieve the best balance between the CPU operating time, speed and power consumption.

- **Sleep** mode
  In sleep mode, only the clock of CPU core is off. All peripherals continue to operate and any interrupt/event can wake up the system.
- **Deep-sleep** mode
  In Deep-sleep mode, all clocks in the 1.8V domain are off, and all of the high speed crystal oscillator (HSI, HSE) and PLL are disabled. Only the contents of SRAM and registers are retained. Any interrupt or wakeup event from EXTI lines can wake up the system from the Deep-sleep mode including the 16 external lines, the RTC alarm and the LVD output,. When exiting the Deep-sleep mode, the HSI is selected as the system clock.
- **Standby** mode
  In Standby mode, the whole 1.8V domain is power off, the LDO is shut down, and all of HSI, HSE and PLL are disabled. The contents of SRAM and registers (except Backup Registers) are lost. There are four wakeup sources for the Standby mode, including the external reset from NRST pin, the RTC alarm, the IWDG reset, and the rising edge on WKUP pin.

## 3.6 Analog to digital converter (ADC)

- 12-bit SAR ADC engine with up to 2M SPS conversion rate
- 12-bit, 10-bit, 8-bit or 6-bit configurable resolution
- Hardware oversampling ratio adjustable from 2 to 256x improves resolution to 16-bit
- Conversion range: $V_{SSA}$ to $V_{DDA}$ (3.0 to 5.5 V)
- Temperature sensor

A 12-bit 2M SPS multi-channel ADC are integrated in the device. It is a total of up to 16 multiplexed external channels with 2 internal channels for temperature sensor and voltage reference measurement. The conversion range is between 3.0 V < $V_{DDA}$ < 5.5 V. An on-chip 16-bit hardware oversample scheme improves performances while off-loading the related computational burden from the MCU. An analog watchdog block can be used to detect the channels, which are required to remain within a specific threshold window. A configurable channel management block of analog inputs also can be used to perform conversions in single, continuous, scan or discontinuous mode to support more advanced usages.

The ADC can be triggered from the events generated by the general-purpose timers (TMx) and the advanced-control timer (TM1) with internal connection. The temperature sensor can be used to generate a voltage that varies linearly with temperature. It is internally connected



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to the ADC_IN16 input channel which is used to convert the sensor output voltage into a digital value.

## 3.7 DMA

- 7 channel DMA controller
- Peripherals supported: Timers, ADC, SPIs, $I^2Cs$, USARTs

The flexible general-purpose DMA controllers provide a hardware method of transferring data between peripherals and/or memory without intervention from the CPU, thereby freeing up bandwidth for other system functions. Three types of access method are supported: peripheral to memory, memory to peripheral, memory to memory

Each channel is connected to fixed hardware DMA requests. The priorities of DMA channel requests are determined by software configuration and hardware channel number. Transfer size of source and destination are independent and configurable.

## 3.8 General-purpose inputs/outputs (GPIOs)

- Up to 55 fast GPIOs, all mappable on 16 external interrupt vectors (EXTI)
- Analog input/output configurable
- Alternate function input/output configurable

There are up to 55 general purpose I/O pins (GPIO) in GD32F170xx, named PA0 ~ PA15 and PB0 ~ PB15, PC0 ~ PC15, PD2, PF0, PF1, PF4-PF7 to implement logic input/output functions. Each of the GPIO ports has related control and configuration registers to satisfy the requirements of specific applications. The external interrupts on the GPIO pins of the device have related control and configuration registers in the External Interrupt Control Unit (EXTI). The GPIO ports are pin-shared with other alternative functions (AFs) to obtain maximum flexibility on the package pins. Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current capable except for analog inputs.

## 3.9 Timers and PWM generation

- One 16-bit advanced-control timer (TM1), one 32-bit general-purpose timer (TM2), five 16-bit general-purpose timers (TM3, TM14 ~ TM17)
- Up to 4 independent channels of PWM, output compare or input capture for each general-purpose timer (GPTM) and external trigger input
- 16-bit, motor control PWM advanced-control timer with programmable dead-time generation for output match
- Encoder interface controller with two inputs using quadrature decoder



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- 24-bit SysTick timer down counter
- 2 watchdog timers (Independent watchdog and window watchdog)

The advanced-control timer (TM1) can be used as a three-phase PWM multiplexed on 6 channels. It has complementary PWM outputs with programmable dead-time generation. It can also be used as a complete general-purpose timer. The 4 independent channels can be used for input capture, output compare, PWM generation (edge- or center-aligned counting modes) and single pulse mode output. If configured as a general-purpose 16-bit timer, it has the same functions as the TMx timer. It can be synchronized with external signals or to interconnect with other GPTMs together which have the same architecture and features.

The general-purpose timer (GPTM) can be used for a variety of purposes including general time, input signal pulse width measurement or output waveform generation such as a single pulse generation or PWM output, up to 4 independent channels for input capture/output compare. TM2 is based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler. TM3 is based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. TM14 ~ TM17 is based on a 16-bit auto-reload upcounter and a 16-bit prescaler. The GPTM also supports an encoder interface with two inputs using quadrature decoder.

The GD32F170xx provides two watchdog peripherals, Independent watchdog and window watchdog. They offer a combination of high safety level, flexibility of use and timing accuracy.

The independent watchdog timer includes a 12-bit down-counting counter and a 8-bit prescaler, It is clocked from an independent 40 kHz internal RC and as it operates independently of the main clock, it can operate in stop and standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management.

The window watchdog is based on a 7-bit down counter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

The SysTick timer is dedicated for OS, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Auto reload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

## 3.10 Real time clock (RTC)

- Independent binary-coded decimal (BCD) format timer/counter with five 32-bit backup registers.
- Calendar with sub-seconds, seconds, minutes, hours, week day, date, year and month automatically correction



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- Alarm function with wake up from deep-sleep and standby mode capability
- On-the-fly correction for synchronization with master clock. Digital calibration with 1 ppm resolution for compensation of quartz crystal inaccuracy.

The real time clock is an independent timer which provides a set of continuously running counters in backup registers to provide a real calendar function, and provides an alarm interrupt or an expected interrupt. It is not reset by a system or power reset, or when the device wakes up from standby mode. A 20-bit prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 kHz from external crystal oscillator.

## 3.11 Inter-integrated circuit (I2C)

- Up to three I2C bus interfaces can support both master and slave mode with a frequency up to 400 kHz
- Provide arbitration function, optional PEC (packet error checking) generation and checking
- Supports 7-bit and 10-bit addressing mode and general call addressing mode
- Hardware support specifications of secure access and control module interface applied in validation for resident ID cards

The I2C interface is an internal circuit allowing communication with an external I2C interface which is an industry standard two line serial interface used for connection to external hardware. These two serial lines are known as a serial data line (SDA) and a serial clock line (SCL). The I2C module provides two data transfer rates: 100 kHz of standard mode or 400 kHz of the fast mode. The I2C module also has an arbitration detect function to prevent the situation where more than one master attempts to transmit data to the I2C bus at the same time. A CRC-8 calculator is also provided in I2C interface to perform packet error checking for I2C data.

## 3.12 Serial peripheral interface (SPI)

- Up to three SPI interfaces with a frequency of up to 30 MHz
- Support both master and slave mode
- Hardware CRC calculation and transmit automatic CRC error checking
- Quad wire configuration available in master mode (SPI2)

The SPI interface uses 4 pins, among which are the serial data input and output lines (MISO & MOSI), the clock line (SCK) and the slave select line (NSS). Both SPIs can be served by the DMA controller. The SPI interface may be used for a variety of purposes, including simplex synchronous transfers on two lines with a possible bidirectional data line or reliable communication using CRC checking.



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## 3.13 Universal synchronous asynchronous receiver transmitter (USART)

- Up to two USARTs with operating frequency up to 9 MHz
- Supports both asynchronous and clocked synchronous serial communication modes
- IrDA SIR encoder and decoder support
- LIN break generation and detection
- ISO 7816-3 compliant smart card interface

The USART (USART1, USART2) are used to translate data between parallel and serial interfaces, provides a flexible full duplex data exchange using synchronous or asynchronous transfer. It is also commonly used for RS-232 standard communication. The USART includes a programmable baud rate generator which is capable of dividing the system clock to produce a dedicated clock for the USART transmitter and receiver. The USART also supports DMA function for high speed data communication.

## 3.14 Controller area network (CAN)

- Two CAN2.0B interface with communication frequency up to 1 Mbit/s
- Internal main PLL for USB CLK compliantly
- A hardware CAN2.0B PHY integrated (CAN1)

Controller area network (CAN) is a method for enabling serial communication in field bus. The CAN protocol has been used extensively in industrial automation and automotive applications. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. Each CAN has three mailboxes for transmission and two FIFOs of three message deep for reception. It also provides 14 scalable/configurable identifier filter banks for selecting the incoming messages needed and discarding the others. The integrated hardware CAN PHY can be enabled by register setting and this mode only used for CAN1.

## 3.15 Debug mode

- Serial wire JTAG debug port (SWJ-DP)

The ARM® SWJ-DP Interface is embedded and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

## 3.16 Package and operation temperature

- LQFP64 (GD32F170Rx), LQFP48 (GD32F170Cx) and QFN36 (GD32F170Tx)
- Operation temperature range: -40°C to +85°C (industrial level)



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# 4 Electrical characteristics

## 4.1 Absolute maximum ratings

The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

**Table 6. Absolute maximum ratings**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{DD}$ | External voltage range | $V_{SS}$ - 0.3 | $V_{SS}$ + 5.5 | V |
| $V_{DDA}$ | External analog supply voltage | $V_{SSA}$ - 0.3 | $V_{SSA}$ + 5.5 | V |
| $V_{BAT}$ | External battery supply voltage | $V_{SS}$ - 0.3 | $V_{SS}$ + 5.5 | V |
| $V_{IN}$ | Input voltage on 5V tolerant pin | $V_{SS}$ - 0.3 | $V_{SS}$ + 7.5 | V |
| | Input voltage on other I/O | $V_{SS}$ - 0.3 | 5.5 | V |
| $I_{IO}$ | Maximum current for GPIO pins | — | 25 | mA |
| $T_A$ | Operating temperature range | -40 | +85 | °C |
| $T_{STG}$ | Storage temperature range | -55 | +150 | °C |
| $T_J$ | Maximum junction temperature | — | 125 | °C |

## 4.2 Recommended DC characteristics

**Table 7. DC operating conditions**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | — | 2.5 | 5.0 | 5.5 | V |
| $V_{DDA}$ | Analog supply voltage | Same as $V_{DD}$ | 2.5 | 5.0 | 5.5 | V |
| $V_{BAT}$ | Battery supply voltage | — | 2.0 | — | 5.5 | V |



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## 4.3 Power consumption

The power measurements specified in the tables represent that code with data executing from on-chip Flash with the following specifications.

**Table 8. Power consumption characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{DD}$ | Supply current (Run mode) | $V_{DD}$=$V_{DDA}$=5.0V, HSE=8MHz, System clock=72 MHz, All peripherals enabled | — | 59.23 | — | mA |
| | | $V_{DD}$=$V_{DDA}$=5.0V, HSE=8MHz, System clock =72 MHz, All peripherals disabled | — | 38.71 | — | mA |
| | | $V_{DD}$=$V_{DDA}$=5.0V, HSE=8MHz, System clock =48 MHz, All peripherals enabled | -— | 40.46 | — | mA |
| | | $V_{DD}$=$V_{DDA}$=5.0V, HSE=8MHz, System Clock =48 MHz, All peripherals disabled | — | 26.72 | — | mA |
| | Supply current (Sleep mode) | $V_{DD}$=$V_{DDA}$=5.0V, HSE=8MHz, CPU clock off, System clock=72MHz, All peripherals enabled | — | 35.17 | — | mA |
| | | $V_{DD}$=$V_{DDA}$=5.0V, HSE=8MHz, CPU clock off, System clock=72MHz, All peripherals disabled | — | 13.00 | — | mA |
| | Supply current (Deep-Sleep mode) | $V_{DD}$=$V_{DDA}$=5.0V, Regulator in run mode, LSI on, RTC on, All GPIOs analog mode | — | 119.81 | — | µA |
| | | $V_{DD}$=$V_{DDA}$=5.0V, Regulator in low power mode, LSI on, RTC on, All GPIOs analog mode | — | 105.35 | — | µA |
| | Supply current (Standby mode) | $V_{DD}$=$V_{DDA}$=5.0V, LSE off, LSI on, RTC on | — | 11.08 | — | µA |
| | | $V_{DD}$=$V_{DDA}$=5.0V, LSE off, LSI on, RTC off | — | 10.56 | — | µA |
| | | $V_{DD}$=$V_{DDA}$=5.0V, LSE off, LSI off, RTC off | — | 8.54 | — | µA |
| $I_{BAT}$ | Battery supply current | $V_{DD}$ not available, $V_{BAT}$=5.5 V, LSE on with external crystal, RTC on, Higher driving | — | 2.30 | — | µA |
| | | $V_{DD}$ not available, $V_{BAT}$=5.0 V, LSE on with external crystal, RTC on, Higher driving | — | 2.06 | — | µA |
| | | $V_{DD}$ not available, $V_{BAT}$=3.3 V, LSE on with external crystal, RTC on, Higher driving | — | 1.56 | — | µA |
| | | $V_{DD}$ not available, $V_{BAT}$=2.5 V, LSE on with external crystal, RTC on, Higher driving | — | 1.41 | — | µA |
| | | $V_{DD}$ not available, $V_{BAT}$=5.0 V, LSE on with external crystal, RTC on, Lower driving | — | 1.32 | — | µA |
| | | $V_{DD}$ not available, $V_{BAT}$=3.3 V, LSE on with external crystal, RTC on, Lower driving | — | 0.88 | — | µA |
| | | $V_{DD}$ not available, $V_{BAT}$=2.5 V, LSE on with external crystal, RTC on, Lower driving | — | 0.75 | — | µA |



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## 4.4 EMC characteristics

EMS (electromagnetic susceptibility) includes ESD (Electrostatic discharge, positive and negative) and FTB (Burst of Fast Transient voltage, positive and negative) testing result is given in the following table, based on the EMS levels and classes compliant with IEC 61000 series standard.

**Table 9. EMS characteristics**

| Symbol | Parameter | Conditions | Level/Class |
|---|---|---|---|
| $V_{ESD}$ | Voltage applied to all device pins to induce a functional disturbance | VDD = 5.0 V, TA = +25 °C conforms to IEC 61000-4-2 | 3B |
| $V_{FTB}$ | Fast transient voltage burst applied to induce a functional disturbance through 100 pF on $V_{DD}$ and $V_{SS}$ pins | VDD = 5.0 V, TA = +25 °C conforms to IEC 61000-4-4 | 4A |

EMI (Electromagnetic Interference) emission testing result is given in the following table, compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

**Table 10. EMI characteristics**

| Symbol | Parameter | Conditions | Tested frequency band | Conditions | | Unit |
|---|---|---|---|---|---|---|
| | | | | 24M | 48M | |
| $S_{EMI}$ | Peak level | VDD = 5.0 V, TA = +25 °C, compliant with IEC 61967-2 | 0.1 to 2 MHz | <0 | <0 | dBµV |
| | | | 2 to 30 MHz | -3.9 | -2.8 | |
| | | | 30 to 130 MHz | -7.2 | -8 | |
| | | | 130 MHz to 1GHz | -7 | -7 | |

## 4.5 Power supply supervisor characteristics

**Table 11. Power supply supervisor characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{POR}$ | Power on reset threshold | — | 1.87 | 1.94 | 2.01 | V |
| $V_{PDR}$ | Power down reset threshold | | 1.82 | 1.89 | 1.96 | V |
| $V_{HYST}$ | PDR hysteresis | | — | 0.05 | — | V |
| $T_{RSTTEMP}$ | Reset temporization | | — | 2 | — | ms |



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## 4.6 Electrical sensitivity

The device is strained in order to determine its performance in terms of electrical sensitivity. Electrostatic discharges (ESD) are applied directly to the pins of the sample. Static latch-up (LU) test is based on the two measurement methods.

**Table 12. ESD characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{ESD(HBM)}$ | Electrostatic discharge voltage (human body model) | $T_A$=25 °C; JESD22-A114 | — | — | 7000 | V |
| $V_{ESD(CDM)}$ | Electrostatic discharge voltage (charge device model) | $T_A$=25 °C; JESD22-C101 | — | — | 1000 | V |

**Table 13. Static latch-up characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| LU | I-test | $T_A$=25 °C; JESD78 | — | — | ±200 | mA |
| | $V_{supply}$ over voltage | | — | — | 8.25 | V |

## 4.7 External clock characteristics

**Table 14. High speed external clock (HSE) generated from a crystal/ceramic characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{HSE}$ | High Speed External oscillator (HSE) frequency | $V_{DD}$=5.0V | 4 | 8 | 32 | MHz |
| $C_{HSE}$ | Recommended load capacitance on OSC_IN and OSC_OUT | — | — | 20 | 30 | pF |
| $R_{FHSE}$ | Recommended external feedback resistor between XTALIN and XTALOUT | — | — | 200 | — | KΩ |
| $D_{HSE}$ | HSE oscillator duty cycle | — | 30 | 50 | 70 | % |
| $I_{DDHSE}$ | HSE oscillator operating current | $V_{DD}$=5.0V, $T_A$=25°C | — | 1.7 | — | mA |
| $t_{SUHSE}$ | HSE oscillator startup time | $V_{DD}$=5.0V, $T_A$=25°C | — | 2 | — | ms |



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**Table 15. Low speed external clock (LSE) generated from a crystal/ceramic characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{LSE}$ | Low Speed External oscillator (LSE) frequency | $V_{DD}$=$V_{BAT}$=5.0V | — | 32.768 | 1000 | KHz |
| $C_{LSE}$ | Recommended load capacitance on OSC32_IN and OSC32_OUT | — | — | — | 15 | pF |
| $D_{LSE}$ | LSE oscillator duty cycle | — | 30 | 50 | 70 | % |
| $I_{DDLSE}$ | LSE oscillator operating current | LSEDRV[1:0]=00 | — | 0.7 | — | µA |
| | | LSEDRV[1:0]=01 | — | 0.8 | — | |
| | | LSEDRV[1:0]=10 | — | 1.1 | — | |
| | | LSEDRV[1:0]=11 | — | 1.4 | — | |
| $t_{SULSE}$ | LSE oscillator startup time | $V_{DD}$=$V_{BAT}$=5.0V | — | 3 | — | s |

## 4.8 Internal clock characteristics

**Table 16. High speed internal clock (HSI) characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{HSI}$ | High Speed Internal Oscillator (HSI) frequency | $V_{DD}$=5.0V | — | 8 | — | MHz |
| $ACC_{HSI}$ | HSI oscillator Frequency accuracy, Factory-trimmed | $V_{DD}$=5.0V, $T_A$=-40°C ~+105°C | -3.5 | — | +3.0 | % |
| | | $V_{DD}$=5.0V, $T_A$=0°C ~ +85°C | -2.0 | — | +2.0 | % |
| | | $V_{DD}$=5.0V, $T_A$=25°C | -1.0 | — | +1.0 | % |
| $D_{HSI}$ | HSI oscillator duty cycle | $V_{DD}$=5.0V, $f_{HSI}$=8MHz | 48 | 50 | 52 | % |
| $I_{DDHSI}$ | HSI oscillator operating current | $V_{DD}$=5.0V, $f_{HSI}$=8MHz | — | 80 | 100 | µA |
| $t_{SUHSI}$ | HSI oscillator startup time | $V_{DD}$=5.0V, $f_{HSI}$=8MHz | 1 | — | 2 | us |

**Table 17. Low speed internal clock (LSI) characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{LSI}$ | Low Speed Internal oscillator (LSI) frequency | $V_{DD}$=$V_{BAT}$=5.0V, $T_A$=-40°C ~ +85°C | 30 | 40 | 60 | KHz |
| $I_{DDLSI}$ | LSI oscillator operating current | $V_{DD}$=$V_{BAT}$=5.0V, $T_A$=25°C | — | 1 | 2 | µA |
| $t_{SULSI}$ | LSI oscillator startup time | $V_{DD}$=$V_{BAT}$=5.0V, $T_A$=25°C | — | — | 80 | µs |



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## 4.9 PLL characteristics

**Table 18. PLL characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{PLLIN}$ | PLL input clock frequency | — | 1 | 8 | 25 | MHz |
| $f_{PLL}$ | PLL output clock frequency | — | 16 | — | 72 | MHz |
| $t_{LOCK}$ | PLL lock time | — | — | | 200 | μs |
| $Jitter_{PLL}$ | Cycle to cycle Jitter | — | | | 300 | ps |

## 4.10 Memory characteristics

**Table 19. Flash memory characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $PE_{CYC}$ | Number of guaranteed program /erase cycles before failure (Endurance) | $T_A$=-40°C ~ +85°C | 100 | — | — | kcycles |
| $t_{RET}$ | Data retention time | $T_A$=125°C | 20 | — | — | years |
| $t_{PROG}$ | Word programming time | $T_A$=-40°C ~ +85°C | 200 | — | 400 | us |
| $t_{ERASE}$ | Page erase time | $T_A$=-40°C ~ +85°C | 60 | 100 | 450 | ms |
| $t_{MERASE}$ | Mass erase time | $T_A$=-40°C ~ +85°C | 3.2 | — | 9.6 | s |



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## 4.11 GPIO characteristics

**Table 20. I/O port characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Standard IO Low level input voltage | $V_{DD}$=2.5V | — | — | 0.83 | V |
| | | $V_{DD}$=3.3V | — | — | 1.24 | |
| | | $V_{DD}$=5.0V | — | — | 1.97 | |
| | | $V_{DD}$=5.5V | — | — | 2.22 | |
| | High Voltage tolerant IO Low level input voltage | $V_{DD}$=2.5V | — | — | 0.65 | V |
| | | $V_{DD}$=3.3V | — | — | 0.93 | |
| | | $V_{DD}$=5.0V | — | — | 1.46 | |
| | | $V_{DD}$=5.5V | — | — | 1.66 | |
| $V_{IH}$ | Standard IO High level input voltage | $V_{DD}$=2.5V | 1.67 | — | — | V |
| | | $V_{DD}$=3.3V | 2.01 | — | — | |
| | | $V_{DD}$=5.0V | 2.91 | — | — | |
| | | $V_{DD}$=5.5V | 3.13 | — | — | |
| | High Voltage tolerant IO High level input voltage | $V_{DD}$=2.5V | 1.42 | — | — | V |
| | | $V_{DD}$=3.3V | 1.70 | — | — | |
| | | $V_{DD}$=5.0V | 2.38 | — | — | |
| | | $V_{DD}$=5.5V | 2.54 | — | — | |
| $V_{OL}$ | Low level output voltage | $V_{DD}$=2.5V, $I_{IO}$=8mA | — | — | 0.29 | V |
| | | $V_{DD}$=3.3V, $I_{IO}$=8mA | — | — | 0.22 | |
| | | $V_{DD}$=5.0V, $I_{IO}$=8mA | — | — | 0.17 | |
| | | $V_{DD}$=5.5V, $I_{IO}$=8mA | — | — | 0.16 | |
| | | $V_{DD}$=2.5V, $I_{IO}$=20mA | — | — | 1.10 | |
| | | $V_{DD}$=3.3V, $I_{IO}$=20mA | — | — | 0.59 | |
| | | $V_{DD}$=5.0V, $I_{IO}$=20mA | — | — | 0.42 | |
| | | $V_{DD}$=5.5V, $I_{IO}$=20mA | — | — | 0.40 | |
| $V_{OH}$ | High level output voltage | $V_{DD}$=2.5V, $I_{IO}$=8mA | 2.24 | — | — | V |
| | | $V_{DD}$=3.3V, $I_{IO}$=8mA | 3.12 | — | — | |
| | | $V_{DD}$=5.0V, $I_{IO}$=8mA | 4.87 | — | — | |
| | | $V_{DD}$=5.5V, $I_{IO}$=8mA | 5.37 | — | — | |
| | | $V_{DD}$=2.5V, $I_{IO}$=20mA | 1.68 | — | — | |
| | | $V_{DD}$=3.3V, $I_{IO}$=20mA | 2.80 | — | — | |
| | | $V_{DD}$=5.0V, $I_{IO}$=20mA | 4.64 | — | — | |
| | | $V_{DD}$=5.5V, $I_{IO}$=20mA | 5.17 | — | — | |
| $R_{PU}$ | Internal pull-up resistor | $V_{IN}$=$V_{SS}$ | 30 | 40 | 50 | kΩ |
| $R_{PD}$ | Internal pull-down resistor | $V_{IN}$=$V_{DD}$ | 30 | 40 | 50 | kΩ |



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## 4.12 ADC characteristics

**Table 21. ADC characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DDA}$ | Operating voltage | — | 3.0 | 5.0 | 5.5 | V |
| $V_{ADCIN}$ | ADC input voltage range | — | 0 | — | $V_{REF+}$ | V |
| $f_{ADC}$ | ADC clock | — | 0.1 | — | 28 | MHz |
| $f_S$ | Sampling rate | 12-bit | 0.007 | — | 2 | MSPS |
| | | 10-bit | 0.008 | — | 2.3 | |
| | | 8-bit | 0.01 | — | 2.8 | |
| | | 6-bit | 0.013 | — | 3.5 | |
| $V_{IN}$ | Analog input voltage | 16 external;3 internal | 0 | — | $V_{DDA}$ | V |
| $V_{REF+}$ | Positive Reference Voltage | — | — | $V_{DDA}$ | — | V |
| $V_{REF-}$ | Negative Reference Voltage | — | — | 0 | — | V |
| $R_{AIN}$ | External input impedance | See ***Equation 1*** | — | — | 38 | kΩ |
| $R_{ADC}$ | Input sampling switch resistance | — | — | — | 0.5 | kΩ |
| $C_{ADC}$ | Input sampling capacitance | No pin/pad capacitance included | — | 5.2 | — | pF |
| $t_{CAL}$ | Calibration time | $f_{ADC}$=28MHz | — | 3 | — | μs |
| $t_s$ | Sampling time | $f_{ADC}$=28MHz | 0.053 | — | 9.554 | μs |
| $t_{CONV}$ | Total conversion time (including sampling time) | 12-bit | — | 14 | — | 1/ $f_{ADC}$ |
| | | 10-bit | — | 12 | — | |
| | | 8-bit | — | 10 | — | |
| | | 6-bit | — | 8 | — | |
| $t_{SU}$ | Startup time | — | — | — | 1 | μs |

***Equation 1***: $R_{AIN}$ max formula $$R_{AIN} < \frac{T_S}{f_{ADC} * C_{ADC} * \ln(2^{N+2})} - R_{ADC}$$

The formula above (Equation 1) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N=12 (from 12-bit resolution).

**Table 22. ADC $R_{AIN\ max}$ for $f_{ADC}$=28MHz**

| $T_s$ (cycles) | $t_s$ (us) | $R_{AIN\ max}$ (KΩ) |
|---|---|---|
| 1.5 | 0.0536 | 0.5 |
| 7.5 | 0.2679 | 4.8 |
| 13.5 | 0.4821 | 9 |
| 28.5 | 1.018 | 19 |
| 41.5 | 1.482 | 28 |
| 55.5 | 1.982 | 38 |
| 71.5 | 2.554 | N/A |
| 239.5 | 8.554 | N/A |

*Note: Guaranteed by design, not tested in production.*



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## 4.13 SPI characteristics

**Table 23. SPI characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{SCK}$ | SCK clock frequency | — | — | — | 30 | MHz |
| $TSI_{K(H)}$ | SCK clock high time | — | 19 | — | — | ns |
| $TSI_{K(L)}$ | SCK clock low time | — | 19 | — | — | ns |
| **SPI master mode** | | | | | | |
| $t_{V(MO)}$ | Data output valid time | — | — | — | 25 | ns |
| $t_{H(MO)}$ | Data output hold time | — | 2 | — | — | ns |
| $t_{SU(MI)}$ | Data input setup time | — | 5 | — | — | ns |
| $t_{H(MI)}$ | Data input hold time | — | 5 | — | — | ns |
| **SPI slave mode** | | | | | | |
| $t_{SU(NSS)}$ | NSS enable setup time | $f_{PCLK}$=54MHz | 74 | — | — | ns |
| $t_{H(NSS)}$ | NSS enable hold time | $f_{PCLK}$=54MHz | 37 | — | — | ns |
| $t_{A(SO)}$ | Data output access time | $f_{PCLK}$=54MHz | 0 | — | 55 | ns |
| $t_{DIS(SO)}$ | Data output disable time | — | 3 | — | 10 | ns |
| $t_{V(SO)}$ | Data output valid time | — | — | — | 25 | ns |
| $t_{H(SO)}$ | Data output hold time | — | 15 | — | — | ns |
| $t_{SU(SI)}$ | Data input setup time | — | 5 | — | — | ns |
| $t_{H(SI)}$ | Data input hold time | — | 4 | — | — | ns |

## 4.14 I2C characteristics

**Table 24. I2C characteristics**

| Symbol | Parameter | Conditions | Standard mode | | Fast mode | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| $f_{SCL}$ | SCL clock frequency | — | 0 | 100 | 0 | 400 | KHz |
| $TSI_{L(H)}$ | SCL clock high time | — | 4.0 | — | 0.6 | — | ns |
| $TSI_{L(L)}$ | SCL clock low time | — | 4.7 | — | 1.3 | — | ns |

## 4.15 USART characteristics

**Table 25. USART characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{SCK}$ | SCK clock frequency | — | — | — | 36 | MHz |
| $TSI_{K(H)}$ | SCK clock high time | — | 13 | — | — | ns |
| $TSI_{K(L)}$ | SCK clock low time | — | 13 | — | — | ns |



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# 5 Package information

## 5.1 QFN package outline dimensions

**Figure 7. QFN package outline**

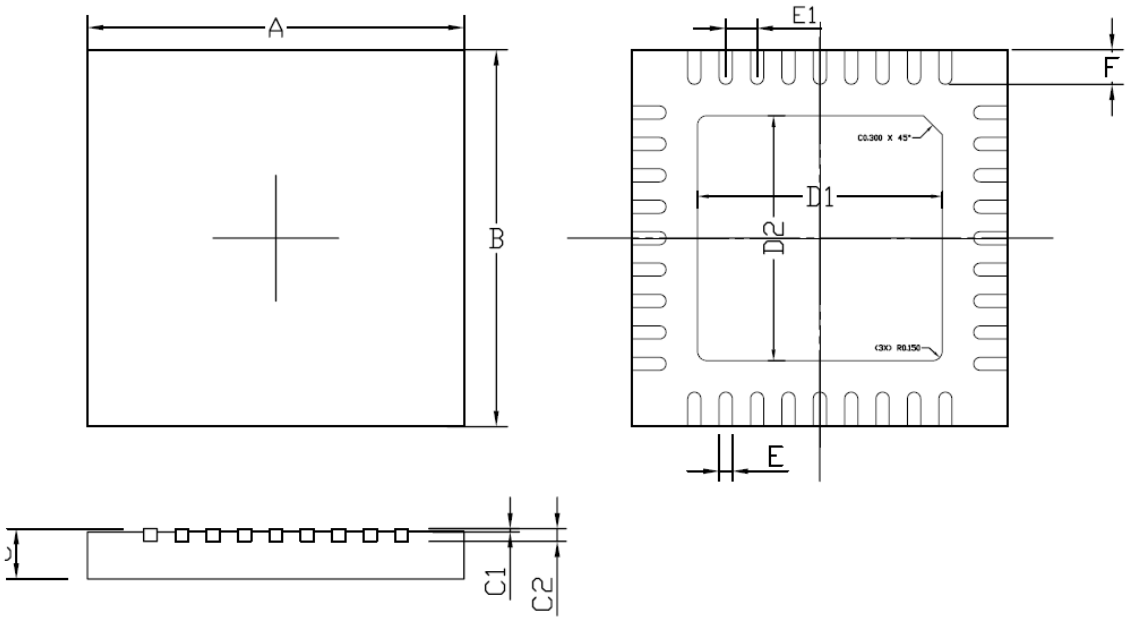



**Table 26. QFN package dimensions**

| Symbol | QFN36 | | Symbol | QFN36 | |
|---|---|---|---|---|---|
| | min | max | | min | max |
| A | 6.0 ± 0.1 | | D1 | 3.90 Typ | |
| B | 6.0 ± 0.1 | | D2 | 3.90 Typ | |
| C | 0.85 | 0.95 | E | 0.210 ± 0.025 | |
| C1 | 0～0.050 | | E1 | 0.500 Typ | |
| C2 | 0.203 Typ | | F | 0.550 Typ | |

(Original dimensions are in millmeters)

Note:

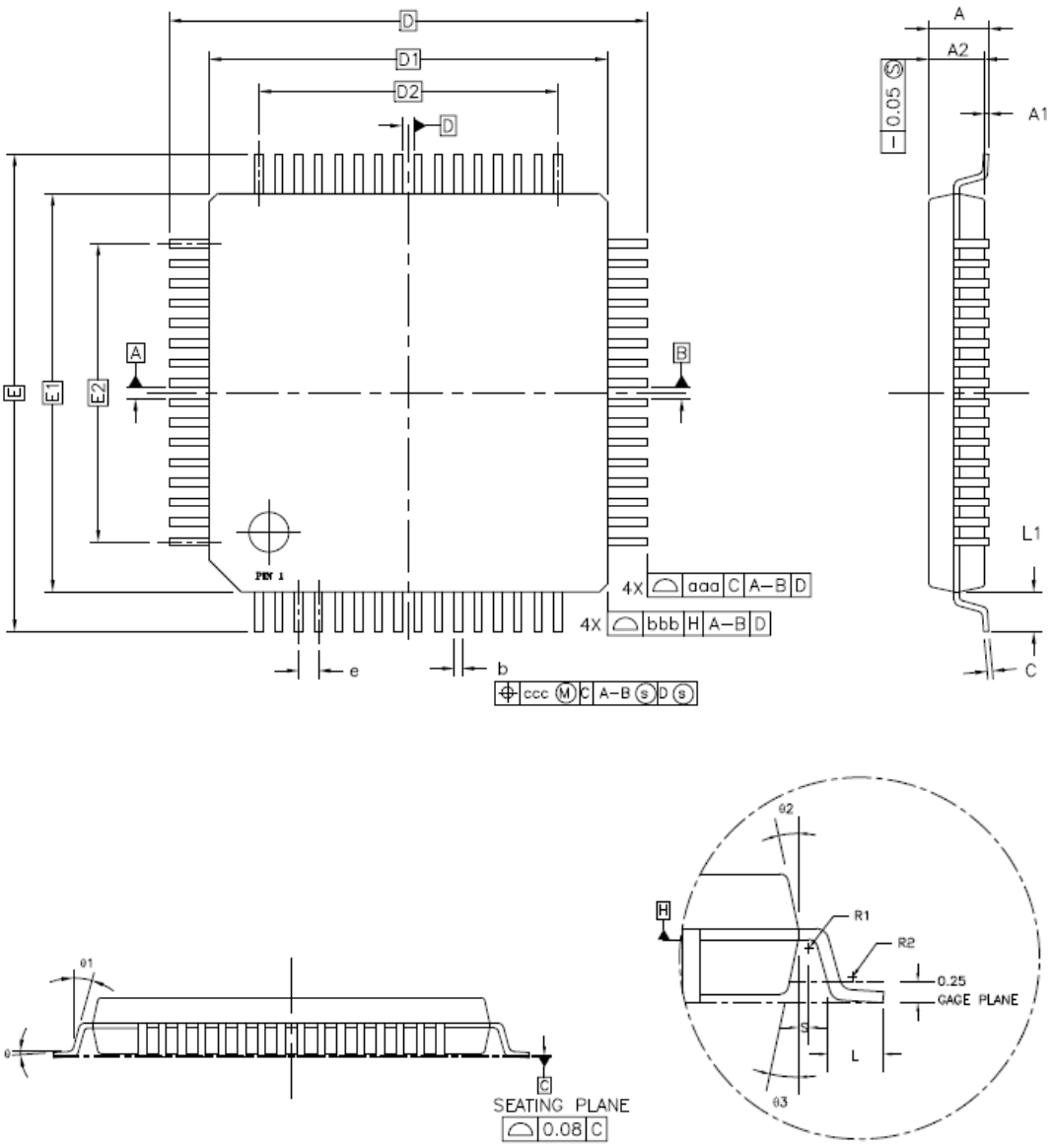
1. Formed lead shall be planar with respect to one another within 0.004 inches.
2. Both package length and width do not include mold flash and metal burr.



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## 5.2 LQFP package outline dimensions

**Figure 8. LQFP package outline**






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**Table 27. LQFP package dimensions**

| Symbol | LQFP48 | | |
|---|---|---|---|
| | Min | Typ | Max |
| A | - | - | 1.20 |
| A1 | 0.05 | - | 0.15 |
| A2 | 0.95 | 1.00 | 1.05 |
| D | - | 9.00 | - |
| D1 | - | 7.00 | - |
| E | - | 9.00 | - |
| E1 | - | 7.00 | - |
| R1 | 0.08 | - | - |
| R2 | 0.08 | - | 0.20 |
| θ | 0° | 3.5° | 7° |
| θ1 | 0° | - | - |
| θ2 | 11° | 12° | 13° |
| θ3 | 11° | 12° | 13° |
| c | 0.09 | - | 0.20 |
| L | 0.45 | 0.60 | 0.75 |
| L1 | - | 1.00 | - |
| S | 0.20 | - | - |
| b | 0.17 | 0.22 | 0.27 |
| e | - | 0.50 | - |
| D2 | - | 5.50 | - |
| E2 | - | 5.50 | - |
| aaa | 0.20 | | |
| bbb | 0.20 | | |
| ccc | 0.08 | | |

| Symbol | LQFP64 | | |
|---|---|---|---|
| | Min | Typ | Max |
| A | - | - | 1.60 |
| A1 | 0.05 | - | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 |
| D | - | 12.00 | - |
| D1 | - | 10.00 | - |
| E | - | 12.00 | - |
| E1 | - | 10.00 | - |
| R1 | 0.08 | - | - |
| R2 | 0.08 | - | 0.20 |
| θ | 0° | 3.5° | 7° |
| θ1 | 0° | - | - |
| θ2 | 11° | 12° | 13° |
| θ3 | 11° | 12° | 13° |
| c | 0.09 | - | 0.20 |
| L | 0.45 | 0.60 | 0.75 |
| L1 | - | 1.00 | - |
| S | 0.20 | - | - |
| b | 0.17 | 0.20 | 0.27 |
| e | - | 0.50 | - |
| D2 | - | 7.50 | - |
| E2 | - | 7.50 | - |
| aaa | 0.20 | | |
| bbb | 0.20 | | |
| ccc | 0.08 | | |

(Original dimensions are in millmeters)



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# 6 Ordering Information

**Table 28. Part ordering code for GD32F170xx devices**

| Ordering code | Flash (KB) | Package | Package type | Temperature operating range |
|---|---|---|---|---|
| GD32F170T4U6 | 16 | QFN36 | Green | Industrial -40°C to +85°C |
| GD32F170T6U6 | 32 | QFN36 | Green | Industrial -40°C to +85°C |
| GD32F170T8U6 | 64 | QFN36 | Green | Industrial -40°C to +85°C |
| GD32F170C4T6 | 16 | LQFP48 | Green | Industrial -40°C to +85°C |
| GD32F170C6T6 | 32 | LQFP48 | Green | Industrial -40°C to +85°C |
| GD32F170C8T6 | 64 | LQFP48 | Green | Industrial -40°C to +85°C |
| GD32F170R8T6 | 64 | LQFP64 | Green | Industrial -40°C to +85°C |



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# 7 Revision History

**Table 29. Revision history**

| Revision No. | Description | Date |
|---|---|---|
| 1.0 | Initial Release | Jan.8, 2016 |



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