GigaDevice Semiconductor Inc.

GD32E232xx
ARM® Cortex®-M23 32-bit MCU

Datasheet

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1 General description

The GD32E232xx device belongs to the value line of GD32 MCU family. It is a new 32-bit general-purpose microcontroller based on the ARM® Cortex®-M23 core. The Cortex-M23 processor is an energy-efficient processor with a very low gate count. It is intended to be used for microcontroller and deeply embedded applications that require an area-optimized processor. The processor delivers high energy efficiency through a small but powerful instruction set and extensively optimized design, providing high-end processing hardware including a single-cycle multiplier and a 17-cycle divider.

The GD32E232xx device incorporates the ARM® Cortex®-M23 32-bit processor core operating at up to 72 MHz frequency with flash accesses 0~2 wait states to obtain maximum efficiency. It provides up to 64 KB embedded flash memory and up to 8 KB SRAM memory. An extensive range of enhanced I/Os and peripherals connected to two APB buses. The devices offer one 12-bit ADC, two DACs, four CLAs and one comparator, up to five general 16-bit timers, one general 32-bit timer, two basic timers, a PWM advanced timer, as well as standard and advanced communication interfaces: two I2Cs, two USARTs, up to two SPIs, and an I2S.

The device operates from a 1.8 to 3.6 V power supply and available in –40 to +105 °C temperature range. Several power saving modes provide the flexibility for maximum optimization between wakeup latency and power consumption, an especially important consideration in low power applications.

The above features make the GD32E232xx devices suitable for a wide range of applications, especially in areas such as industrial control, motor drives, user interface, power monitor and alarm systems, consumer and handheld equipment, gaming and GPS, E-bike, optical module and so on.



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2 Device overview

2.1 Device information

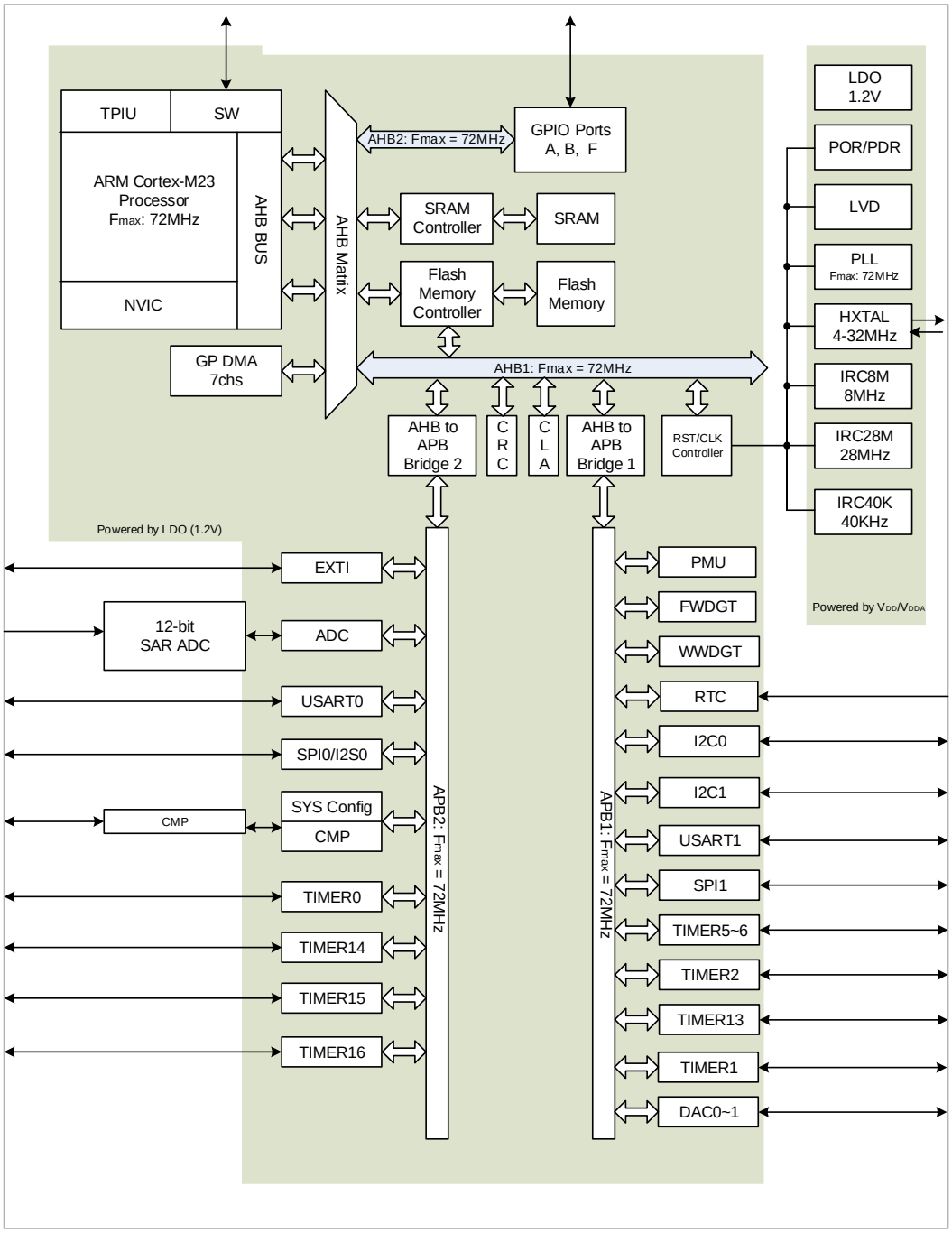
Table 2-1. GD32E232xx device features and peripheral list

Part Number		GD32E232xx					
		E4U7	E6U7	E8U7	K4Q7	K6Q7	K8Q7
FLASH (KB)		16	32	64	16	32	64
SRAM (KB)		4	6	8	4	6	8
Timers	General timer(16-bit)	4 (2,13,15,16)	4 (2,13,15,16)	5 (2,13-16)	4 (2,13,15,16)	4 (2,13,15,16)	5 (2,13-16)
	General timer(32-bit)	1 (1)	1 (1)	1 (1)	1 (1)	1 (1)	1 (1)
	Advanced timer(16-bit)	1 (0)	1 (0)	1 (0)	1 (0)	1 (0)	1 (0)
	SysTick	1	1	1	1	1	1
	Basic timer(16-bit)	2 (5,6)	2 (5,6)	2 (5,6)	2 (5,6)	2 (5,6)	2 (5,6)
	Watchdog	2	2	2	2	2	2
	RTC	1	1	1	1	1	1
Connectivity	USART	2	2	2	2	2	2
	I2C	2	2	2	2	2	2
	SPI/I2S	1/1 (0)/(0)	1/1 (0)/(0)	2/1 (0-1)/(0)	1/1 (0)/(0)	1/1 (0)/(0)	2/1 (0-1)/(0)
GPIO		18	18	18	28	28	28
CMP		1	1	1	1	1	1
EXTI		12	12	12	16	16	16
DAC	Units	2	2	2	2	2	2
	Channels	4	4	4	4	4	4
CLA		3	3	3	4	4	4
ADC	Units	1	1	1	1	1	1
	Channels (External)	9	9	9	16	16	16
	Channels (Internal)	2	2	2	2	2	2
Package		QFN24			QFN32		

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2.2 Block diagram

Figure 2-1. GD32E232xx block diagram



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2.3 Pinouts and pin assignment

Figure 2-2. GD32E232Kx QFN32 pinouts

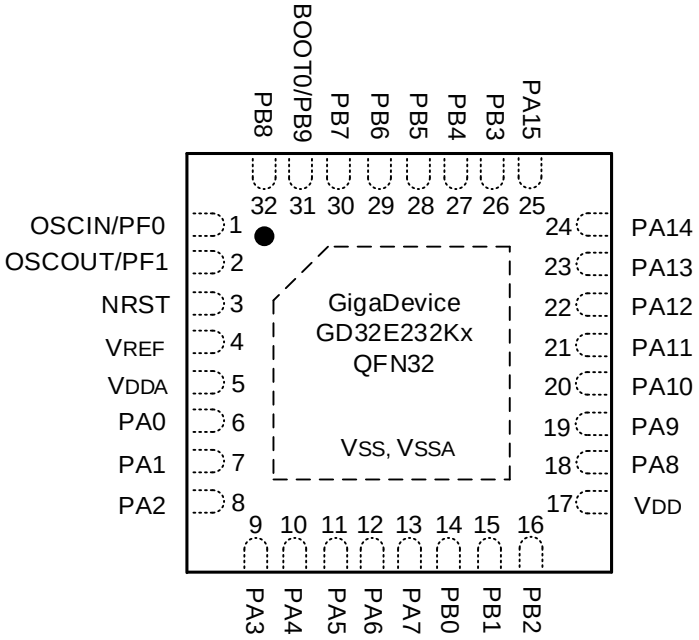
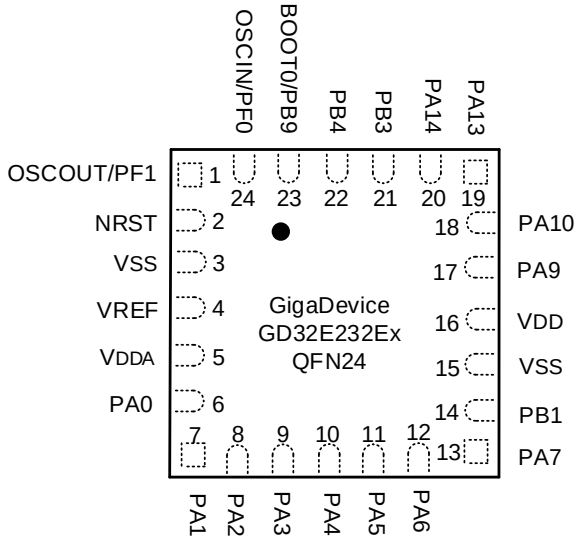


Figure 2-3. GD32E232Ex QFN24 pinouts



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2.4 Memory map

Table 2-2. GD32E232xx memory map

Pre-defined Regions	Bus	ADDRESS	Peripherals
		0xE000 0000 - 0xE00F FFFF	Cortex M23 internal peripherals
External Device		0xA000 0000 - 0xDFFF FFFF	Reserved
External RAM		0x60000000 - 0x9FFFFFFF	Reserved
Peripherals	AHB1	0x5004 0000 - 0x5FFF FFFF	Reserved
		0x5000 0000 - 0x5003 FFFF	Reserved
	AHB2	0x4800 1800 - 0x4FFF FFFF	Reserved
		0x4800 1400 - 0x4800 17FF	GPIOF
		0x4800 1000 - 0x4800 13FF	Reserved
		0x4800 0C00 - 0x4800 0FFF	Reserved
		0x4800 0800 - 0x4800 0BFF	Reserved
		0x4800 0400 - 0x4800 07FF	GPIOB
		0x4800 0000 - 0x4800 03FF	GPIOA
	AHB1	0x4003 8400 - 0x47FF FFFF	Reserved
		0x4003 8000 - 0x4003 83FF	CLA
		0x4002 4400 - 0x4003 7FFF	Reserved
		0x4002 4000 - 0x4002 43FF	Reserved
		0x4002 3400 - 0x4002 3FFF	Reserved
		0x4002 3000 - 0x4002 33FF	CRC
		0x4002 2400 - 0x4002 2FFF	Reserved
		0x4002 2000 - 0x4002 23FF	FMC
		0x4002 1400 - 0x4002 1FFF	Reserved
		0x4002 1000 - 0x4002 13FF	RCU
		0x4002 0400 - 0x4002 0FFF	Reserved
		0x4002 0000 - 0x4002 03FF	DMA
	APB2	0x4001 8000 - 0x4001 FFFF	Reserved
		0x4001 5C00 - 0x4001 7FFF	Reserved
		0x4001 5800 - 0x4001 5BFF	DBG
		0x4001 4C00 - 0x4001 57FF	Reserved
		0x4001 4800 - 0x4001 4BFF	TIMER16
		0x4001 4400 - 0x4001 47FF	TIMER15
		0x4001 4000 - 0x4001 43FF	TIMER14
		0x4001 3C00 - 0x4001 3FFF	Reserved
		0x4001 3800 - 0x4001 3BFF	USART0
		0x4001 3400 - 0x4001 37FF	Reserved
		0x4001 3000 - 0x4001 33FF	SPI0/I2S0
		0x4001 2C00 - 0x4001 2FFF	TIMER0
		0x4001 2800 - 0x4001 2BFF	Reserved

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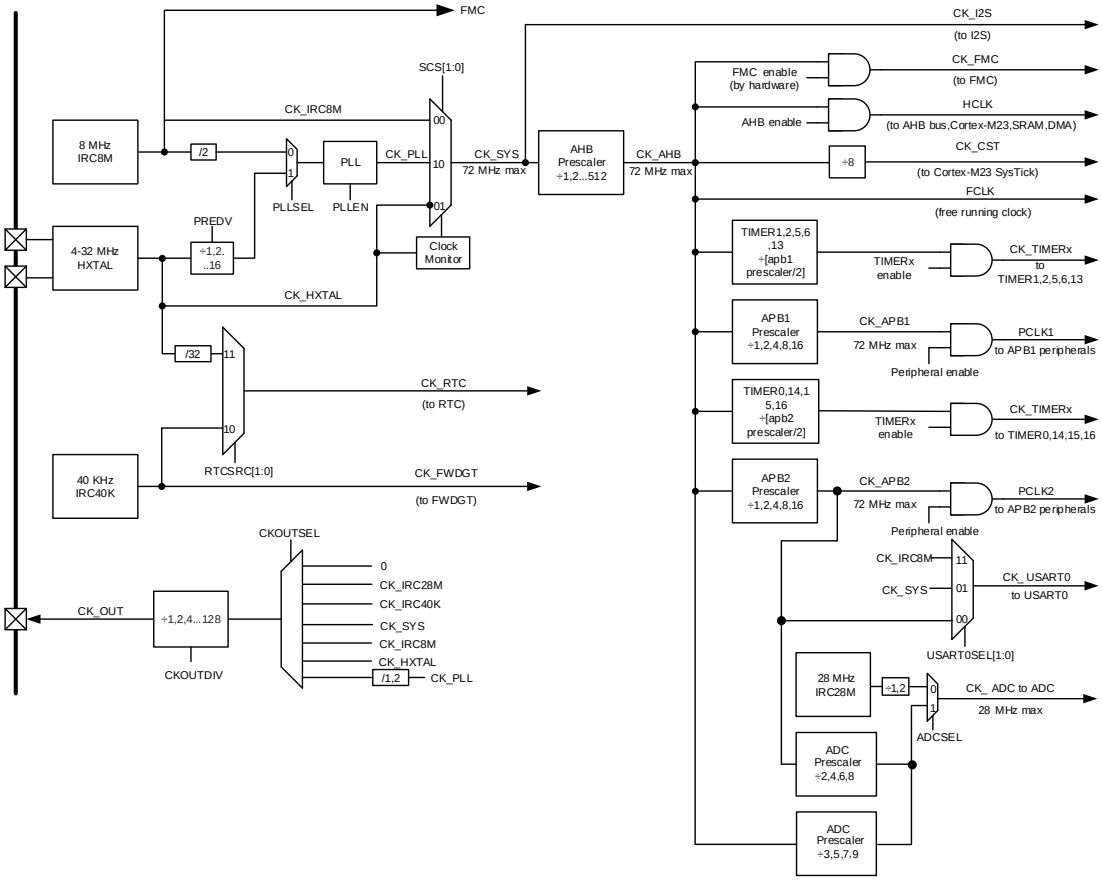
Pre-defined Regions	Bus	ADDRESS	Peripherals
		0x4001 2400 - 0x4001 27FF	ADC
		0x4001 0800 - 0x4001 23FF	Reserved
		0x4001 0400 - 0x4001 07FF	EXTI
		0x4001 0000 - 0x4001 03FF	SYSCFG + CMP
	APB1	0x4000 D000 - 0x4000 FFFF	Reserved
		0x4000 CC00 - 0x4000 CFFF	DAC1
		0x4000 C800 - 0x4000 CBFF	Reserved
		0x4000 C400 - 0x4000 C7FF	Reserved
		0x4000 C000 - 0x4000 C3FF	Reserved
		0x4000 8000 - 0x4000 BFFF	Reserved
		0x4000 7C00 - 0x4000 7FFF	Reserved
		0x4000 7800 - 0x4000 7BFF	Reserved
		0x4000 7400 - 0x4000 77FF	DAC0
		0x4000 7000 - 0x4000 73FF	PMU
		0x4000 6400 - 0x4000 6FFF	Reserved
		0x4000 6000 - 0x4000 63FF	Reserved
		0x4000 5C00 - 0x4000 5FFF	Reserved
		0x4000 5800 - 0x4000 5BFF	I2C1
		0x4000 5400 - 0x4000 57FF	I2C0
		0x4000 4800 - 0x4000 53FF	Reserved
		0x4000 4400 - 0x4000 47FF	USART1
		0x4000 4000 - 0x4000 43FF	Reserved
		0x4000 3C00 - 0x4000 3FFF	Reserved
		0x4000 3800 - 0x4000 3BFF	SPI1
		0x4000 3400 - 0x4000 37FF	Reserved
		0x4000 3000 - 0x4000 33FF	FWDGT
		0x4000 2C00 - 0x4000 2FFF	WWDGT
		0x4000 2800 - 0x4000 2BFF	RTC
		0x4000 2400 - 0x4000 27FF	Reserved
		0x4000 2000 - 0x4000 23FF	TIMER13
		0x4000 1800 - 0x4000 1FFF	Reserved
		0x4000 1400 - 0x4000 17FF	TIMER6
		0x4000 1000 - 0x4000 13FF	TIMER5
		0x4000 0800 - 0x4000 0FFF	Reserved
		0x4000 0400 - 0x4000 07FF	TIMER2
		0x4000 0000 - 0x4000 03FF	TIMER1
SRAM		0x2000 2000 - 0x3FFF FFFF	Reserved
		0x2000 0000 - 0x2000 1FFF	SRAM
Code		0x1FFF F810 - 0x1FFF FFFF	Reserved
		0x1FFF F800 - 0x1FFF F80F	Option bytes

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Pre-defined Regions	Bus	ADDRESS	Peripherals
		0x1FFF EC00 - 0x1FFF F7FF	System memory
		0x0801 0000 - 0x1FFF EBFF	Reserved
		0x0800 0000 - 0x0800 FFFF	Main Flash memory
		0x0001 0000 - 0x07FF FFFF	Reserved
		0x00000000 - 0x0000FFFF	Aliased to Flash or system memory

2.5 Clock tree

Figure 2-4. GD32E232xx clock tree



Note:

If the APB prescaler is 1, the timer clock frequencies are set to AHB frequency divide by 1. Otherwise, they are set to the AHB frequency divide by half of APB prescaler.

Legend:

HXTAL: High speed crystal oscillator

IRC8M: Internal 8M RC oscillator

IRC40K: Internal 40K RC oscillator

IRC28M: Internal 28M RC oscillator

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2.6 Pin definitions

2.6.1 GD32E232Kx QFN32 pin definitions

Table 2-3. GD32E232Kx QFN32 pin definitions

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
PF0-OSCIN	1	I/O	5VT	Default: PF0 Alternate: I2C0_SDA Additional: OSCIN, CLAIN16
PF1-OSCOUT	2	I/O	5VT	Default: PF1 Alternate: I2C0_SCL Additional: OSCOUT,CLAIN17
NRST	3	I/O		Default: NRST
V_{REF}	4	P		Default: V_{REF}
V_{DDA}	5	P		Default: V_{DDA}
PA0-WKUP	6	I/O		Default: PA0 Alternate: USART0_CTS(4), USART1_CTS, CMP_OUT, I2C1_SCL, TIMER1_CH0_ETI Additional: ADC_IN0, CMP_IM6, RTC_TAMP1, WKUP0, CLAIN18
PA1	7	I/O		Default: PA1 Alternate: USART0_RTS(4), USART1_RTS, I2C1_SDA, EVENTOUT, TIMER14_CH0_ON(5), TIMER1_CH1 Additional: ADC_IN1, CMP_IP, CLAIN19
PA2	8	I/O		Default: PA2 Alternate: USART0_TX(4), USART1_TX, TIMER14_CH0(5), TIMER1_CH2, CLA0OUT Additional: ADC_IN2, CMP_IM7
PA3	9	I/O		Default: PA3 Alternate: USART0_RX(4), USART1_RX, TIMER14_CH1(5), TIMER1_CH3 Additional: ADC_IN3
PA4	10	I/O		Default: PA4 Alternate: SPI0_NSS, I2S0_WS, USART0_CK(4), USART1_CK, TIMER13_CH0, I2C1_SCL, SPI1_NSS(5) Additional: CMP_IM4, DAC0_OUT0
PA5	11	I/O		Default: PA5 Alternate: SPI0_SCK, I2S0_CK, TIMER1_CH0_ETI, I2C1_SDA Additional: CMP_IM5, DAC0_OUT1
PA6	12	I/O		Default: PA6 Alternate: SPI0_MISO, I2S0_MCK, TIMER2_CH0, TIMER0_BRKIN, TIMER15_CH0, EVENTOUT, CMP_OUT Additional: DAC1_OUT0

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Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
PA7	13	I/O		Default: PA7 Alternate: SPI0_MOSI, I2S0_SD, TIMER2_CH1, TIMER13_CH0, TIMER0_CH0_ON, TIMER16_CH0, EVENTOUT, CLA1OUT Additional: DAC1_OUT1
PB0	14	I/O		Default: PB0 Alternate: TIMER2_CH2, TIMER0_CH1_ON, USART1_RX, EVENTOUT, CLA1OUT Additional: ADC_IN8, CLAIN8
PB1	15	I/O		Default: PB1 Alternate: TIMER2_CH3, TIMER13_CH0, TIMER0_CH2_ON, SPI1_SCK(5) Additional: ADC_IN9, CLAIN9
PB2	16	I/O	5VT	Default: PB2 Alternate: TIMER2_ETI Additional: ADC_IN10, CLAIN10
V_{DD}	17	P		Default: V_{DD}
PA8	18	I/O	5VT	Default: PA8 Alternate: USART0_CK, TIMER0_CH0, CK_OUT, USART1_TX, EVENTOUT Additional: ADC_IN11, CLAIN11
PA9	19	I/O	5VT	Default: PA9 Alternate: USART0_TX, TIMER0_CH1, TIMER14_BRKIN(5), I2C0_SCL, CK_OUT Additional: ADC_IN12, CLAIN12
PA10	20	I/O	5VT	Default: PA10 Alternate: USART0_RX, TIMER0_CH2, TIMER16_BRKIN, I2C0_SDA, CLA2OUT Additional: ADC_IN13, CLAIN13
PA11	21	I/O	5VT	Default: PA11 Alternate: USART0_CTS, TIMER0_CH3, CMP_OUT, EVENTOUT, SPI1_IO2(5), I2C0_SMBA, I2C1_SCL, CLA3OUT Additional: ADC_IN14, CLAIN14
PA12	22	I/O	5VT	Default: PA12 Alternate: USART0_RTS, TIMER0_ETI, EVENTOUT, SPI1_IO3(5), I2C0_TXFRAME, I2C1_SDA Additional: ADC_IN15, CLAIN15
PA13	23	I/O	5VT	Default: PA13/SWDIO Alternate: SWDIO, IFRP_OUT, SPI1_MISO(5)
PA14	24	I/O	5VT	Default: PA14/SWCLK Alternate: USART0_TX(4), USART1_TX, SWCLK, SPI1_MOSI(5)
PA15	25	I/O	5VT	Default: PA15 Alternate: SPI0_NSS, I2S0_WS, USART0_RX(4), USART1_RX, SPI1_NSS(5), EVENTOUT,

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Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
				TIMER1_CH0_ETI, CLA3OUT Additional: ADC_IN4, CLAIN0
PB3	26	I/O	5VT	Default: PB3 Alternate: SPI0_SCK, I2S0_CK, EVENTOUT, TIMER1_CH1, I2C1_SCL , CLA0OUT Additional: ADC_IN5, CLAIN1
PB4	27	I/O	5VT	Default: PB4 Alternate: SPI0_MISO, I2S0_MCK, TIMER2_CH0, EVENTOUT, I2C0_TXFRAME, TIMER16_BRKIN, I2C1_SDA , CLA1OUT Additional: ADC_IN6, CLAIN2
PB5	28	I/O	5VT	Default: PB5 Alternate: SPI0_MOSI, I2S0_SD, I2C0_SMBA, TIMER15_BRKIN, TIMER2_CH1, CLA2OUT Additional: WKUP5, ADC_IN7, CLAIN3
PB6	29	I/O	5VT	Default: PB6 Alternate: I2C0_SCL, USART0_TX, TIMER15_CH0_ON, I2C1_SCL Additional: CLAIN4
PB7	30	I/O	5VT	Default: PB7 Alternate:I2C0_SDA, USART0_RX, TIMER16_CH0_ON, I2C1_SDA Additional: CLAIN5
BOOT0/ PB9(3)	31	I/O		Default: BOOT0 Alternate：IFRP_OUT, I2C0_SDA, TIMER16_CH0, EVENTOUT, I2S0_MCK, SPI1_NSS Additional: PB9, CLAIN7
PB8	32	I/O	5VT	Default: PB8 Alternate: I2C0_SCL, TIMER15_CH0, CLA3OUT Additional: CLAIN6

Notes:

(1) Type: I = input, O = output, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

(3) When power reset, this pin must be used as BOOT0. When system reset and PIN_RSTMD bit in SYSCFG_CFG2 is set to 0, this pin must be used as BOOT0. At other times, this pin can be used as BOOT0 or PB9 according to BOOT0_PB9_RMP bit in SYSCFG_CFG0. Specially, when PIN_RSTMD bit and BOOT0_PB9_RMP bit are both set, the boot0 function is tied to 0 by hardware after system reset. In this case, the system will boot from main flash without regard to the input value from the BOOT0 pin.

(4) Functions are available on GD32E232K4 devices only.

(5) Functions are available on GD32E230K8 devices only.

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2.6.2 GD32E232Ex QFN24 pin definitions

Table 2-4. GD32E232Ex QFN24 pin definitions

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
PF1-OSCOUT	1	I/O	5VT	Default: PF1 Alternate: I2C0_SCL Additional: OSCOUT,CLAIN17
NRST	2	I/O		Default: NRST
V_{SS}	3	P		Default: V_{SS}
V_{REF}	4	P		Default: V_{REF}
V_{DDA}	5	P		Default: V_{DDA}
PA0-WKUP	6	I/O		Default: PA0 Alternate: USART0_CTS(4), USART1_CTS, CMP_OUT, I2C1_SCL, TIMER1_CH0_ETI Additional: ADC_IN0, CMP_IM6, RTC_TAMP1, WKUP0, CLAIN18
PA1	7	I/O		Default: PA1 Alternate: USART0_RTS(4), USART1_RTS, I2C1_SDA, EVENTOUT, TIMER14_CH0_ON(5), TIMER1_CH1 Additional: ADC_IN1, CMP_IP, CLAIN19
PA2	8	I/O		Default: PA2 Alternate:USART0_TX(4),USART1_TX,TIMER14_CH0(5), TIMER1_CH2, CLA0OUT Additional: ADC_IN2, CMP_IM7
PA3	9	I/O		Default: PA3 Alternate: USART0_RX(4), USART1_RX, TIMER14_CH1(5), TIMER1_CH3 Additional: ADC_IN3
PA4	10	I/O		Default: PA4 Alternate: SPI0_NSS, I2S0_WS, USART0_CK(4), USART1_CK, TIMER13_CH0, I2C1_SCL, SPI1_NSS(5) Additional: CMP_IM4, DAC0_OUT0
PA5	11	I/O		Default: PA5 Alternate: SPI0_SCK, I2S0_CK, TIMER1_CH0_ETI, I2C1_SDA Additional: CMP_IM5, DAC0_OUT1
PA6	12	I/O		Default: PA6 Alternate: SPI0_MISO, I2S0_MCK, TIMER2_CH0, TIMER0_BRKIN, TIMER15_CH0, EVENTOUT, CMP_OUT Additional: DAC1_OUT0
PA7	13	I/O		Default: PA7 Alternate: SPI0_MOSI, I2S0_SD, TIMER2_CH1, TIMER13_CH0, TIMER0_CH0_ON, TIMER16_CH0, EVENTOUT, CLA1OUT Additional: DAC1_OUT1

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Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
PB1	14	I/O		Default: PB1 Alternate: TIMER2_CH3, TIMER13_CH0, TIMER0_CH2_ON, SPI1_SCK Additional: ADC_IN9, CLAIN9
V_{SS}	15	P		Default: V_{SS}
V_{DD}	16	P		Default: V_{DD}
PA9	17	I/O	5VT	Default: PA9 Alternate: USART0_TX, TIMER0_CH1, TIMER14_BRKIN(5), I2C0_SCL, CK_OUT Additional: ADC_IN12, CLAIN12
PA10	18	I/O	5VT	Default: PA10 Alternate: USART0_RX, TIMER0_CH2, TIMER16_BRKIN, I2C0_SDA, CLA2OUT Additional: ADC_IN13, CLAIN13
PA13	19	I/O	5VT	Default: PA13/SWDIO Alternate: SWDIO, IFRP_OUT, SPI1_MISO(5)
PA14	20	I/O	5VT	Default: PA14/SWCLK Alternate: USART0_TX(4), USART1_TX, SWCLK, SPI1_MOSI(5)
PB3	21	I/O	5VT	Default: PB3 Alternate: SPI0_SCK, I2S0_CK, EVENTOUT, TIMER1_CH1, I2C1_SCL , CLA0OUT Additional: ADC_IN5, CLAIN1
PB4	22	I/O	5VT	Default: PB4 Alternate: SPI0_MISO, I2S0_MCK, TIMER2_CH0, EVENTOUT, I2C0_TXFRAME, TIMER16_BRKIN, I2C1_SDA, CLA1OUT Additional: ADC_IN6, CLAIN2
BOOT0/ PB9(3)	23	I/O		Default: BOOT0 Alternate：IFRP_OUT, I2C0_SDA, TIMER16_CH0, EVENTOUT, I2S0_MCK, SPI1_NSS(5) Additional: PB9, CLAIN7
PF0-OSCIN	1	I/O	5VT	Default: PF0 Alternate: I2C0_SDA Additional: OSCIN, CLAIN16

Notes:

(1) Type: I = input, O = output, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

(3) When power reset, this pin must be used as BOOT0. When system reset and PIN_RSTMD bit in SYSCFG_CFG2 is set to 0, this pin must be used as BOOT0. At other times, this pin can be used as BOOT0 or PB9 according to BOOT0_PB9_RMP bit in SYSCFG_CFG0. Specially, when PIN_RSTMD bit and BOOT0_PB9_RMP bit are both set, the boot0 function is tied to 0 by hardware after system reset. In this case, the system will boot from main flash without regard to the input value from the BOOT0 pin.

(4) Functions are available on GD32E232E4 devices only.

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(5) Functions are available on GD32E230E8 devices only.

2.6.3 GD32E232xx pin alternate functions

Table 2-5. Port A alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA0		USART0_CTS(1) /USART1_CTS	TIMER1_CH 0_ETI		I2C1_SCL			CMP_ OUT
PA1	EVENTOUT	USART0_RTS(1) /USART1_RTS	TIMER1_CH 1		I2C1_SDA	TIMER14 _CH0_O N(2)		
PA2	TIMER14_C H0(2)	USART0_TX(1)/ USART1_TX	TIMER1_CH 2	CLA0O UT				
PA3	TIMER14_C H1(2)	USART0_RX(1)/ USART1_RX	TIMER1_CH 3					
PA4	SPI0_NSS/I 2S0_WS	USART0_CK(1)/ USART1_CK			TIMER13_ CH0		SPI1_N SS(2)	I2C1_ SCL
PA5	SPI0_SCK/I 2S0_CK		TIMER1_CH 0_ETI					I2C1_ SDA
PA6	SPI0_MISO/ I2S0_MCK	TIMER2_CH0	TIMER0_BR KIN			TIMER15 _CH0	EVENT OUT	CMP_ OUT
PA7	SPI0_MOSI/ I2S0_SD	TIMER2_CH1	TIMER0_CH 0_ON	CLA1O UT	TIMER13_ CH0	TIMER16 _CH0	EVENT OUT	
PA8	CK_OUT	USART0_CK	TIMER0_CH 0	EVENT OUT	USART1_T X			
PA9	TIMER14_B RKIN(2)	USART0_TX	TIMER0_CH 1		I2C0_SCL	CK_OUT		
PA10	TIMER16_B RKIN	USART0_RX	TIMER0_CH 2	CLA2O UT	I2C0_SDA			
PA11	EVENTOUT	USART0_CTS	TIMER0_CH 3	CLA3O UT	I2C0_SMB A	I2C1_SC L	SPI1_I O2(2)	CMP_ OUT
PA12	EVENTOUT	USART0_RTS	TIMER0_ETI		I2C0_TXF RAME	I2C1_SD A	SPI1_I O3(2)	
PA13	SWDIO	IFRP_OUT					SPI1_M ISO(2)	
PA14	SWCLK	USART0_TX(1)/ USART1_TX					SPI1_M OSI(2)	
PA15	SPI0_NSS/I 2S0_WS	USART0_RX(1)/ USART1_RX	TIMER1_CH 0_ETI	EVENT OUT			SPI1_N SS(2)	CLA3 OUT

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Table 2-6. Port B alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PB0	EVENTOUT	TIMER2_CH2	TIMER0_CH1_ON	CLA1OUT	USART1_RX			
PB1	TIMER13_CH0	TIMER2_CH3	TIMER0_CH2_ON				SPI1_SCK(2)	
PB2		TIMER2_ETI						
PB3	SPI0_SCK/I2S0_CK	EVENTOUT	TIMER1_CH1	CLA0OUT				I2C1_SCL
PB4	SPI0_MISO/I2S0_MCK	TIMER2_CH0	EVENTOUT	CLA1OUT	I2C0_TXFRAME		TIMER16_BRKIN	I2C1_SDA
PB5	SPI0_MOSI/I2S0_SD	TIMER2_CH1	TIMER15_BRKIN	I2C0_SMBA				CLA2OUT
PB6	USART0_TX	I2C0_SCL	TIMER15_CH0_ON					I2C1_SCL
PB7	USART0_RX	I2C0_SDA	TIMER16_CH0_ON					I2C1_SDA
PB8		I2C0_SCL	TIMER15_CH0	CLA3OUT				
PB9	IFRP_OUT	I2C0_SDA	TIMER16_CH0	EVENTOUT		I2S0_MCK		SPI1_NSS(2)

Table 2-7. Port F alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6
PF0		I2C0_SDA					
PF1		I2C0_SCL					

Notes:

(1) Functions are available on GD32E232x4 devices only.

(2) Functions are available on GD32E232x8 devices only.

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3 Functional description

3.1 ARM® Cortex®-M23 core

The Cortex-M23 processor is an energy-efficient processor with a very low gate count. It is intended to be used for microcontroller and deeply embedded applications that require an area-optimized processor. The processor is highly configurable enabling a wide range of implementations from those requiring memory protection and powerful trace technology to cost sensitive devices requiring minimal area, while delivering outstanding computational performance and an advanced system response to interrupts.

32-bit ARM® Cortex®-M23 processor core

- Up to 72 MHz operation frequency
- Single-cycle multiplication and hardware divider
- Ultra-low power, energy-efficient operation
- Excellent code density
- Integrated Nested Vectored Interrupt Controller (NVIC)
- 24-bit SysTick timer

The Cortex®-M23 processor is based on the ARMv8-M architecture and supports both Thumb and Thumb-2 instruction sets. Some system peripherals listed below are also provided by Cortex®-M23:

- Internal Bus Matrix connected with AHB master, Serial Wire Debug Port and Single-cycle IO port
- Nested Vectored Interrupt Controller (NVIC)
- Breakpoint Unit(BPU)
- Data Watchpoint and Trace (DWT)
- Serial Wire Debug Port

3.2 Embedded memory

- Up to 64 Kbytes of flash memory
- Up to 8 Kbytes of SRAM with hardware parity checking

64 Kbytes of inner flash and 8 Kbytes of inner SRAM at most is available for storing programs and data, both accessed (R/W) at CPU clock speed with 0~2 wait states. ***Table 2-2. GD32E232xx memory map*** shows the memory map of the GD32E232xx series of devices, including code, SRAM, peripheral, and other pre-defined regions.

3.3 Clock, reset and supply management

- Internal 8 MHz factory-trimmed RC and external 4 to 32 MHz crystal oscillator

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- Internal 28 MHz RC oscillator
- Internal 40 kHz RC calibrated oscillator
- Integrated system clock PLL
- 1.8 to 3.6 V application supply and I/Os
- Supply Supervisor: POR (Power On Reset), PDR (Power Down Reset), and low voltage detector (LVD)

The Clock Control Unit (CCU) provides a range of oscillator and clock functions. These include speed internal RC oscillator and external crystal oscillator, high speed and low speed two types. Several prescalers allow the frequency configuration of the AHB and two APB domains. The maximum frequency of the AHB, APB2 and APB1 domains is 72 MHz/72 MHz/72 MHz. See ***Figure 2-4. GD32E232xx clock tree*** for details on the clock tree.

The Reset Control Unit (RCU) controls three kinds of reset: system reset resets the processor core and peripheral IP components. Power-on reset (POR) and power-down reset (PDR) are always active, and ensures proper operation starting from 1.71 V and down to 1.67V. The device remains in reset mode when V_{DD} is below a specified threshold. The embedded low voltage detector (LVD) monitors the power supply, compares it to the voltage threshold and generates an interrupt as a warning message for leading the MCU into security.

Power supply schemes:

- V_{DD} range: 1.8 to 3.6 V, external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} range: 1.8 to 3.6 V, external analog power supplies for ADC, reset blocks, RCs and PLL.

3.4 Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from main flash memory (default)
- Boot from system memory
- Boot from on-chip SRAM

In default condition, boot from main flash memory is selected. The boot loader is located in the internal boot ROM memory (system memory). It is used to reprogram the flash memory by using I2C0 (PB6 and PB7 for GD32E232Kx or PA9 and PA10 for GD32E232Ex).

3.5 Power saving modes

The MCU supports three kinds of power saving modes to achieve even lower power consumption. They are sleep mode, deep-sleep mode, and standby mode. These operating modes reduce the power consumption and allow the application to achieve the best balance between the CPU operating time, speed and power consumption.

- **Sleep** mode

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In sleep mode, only the clock of CPU core is off. All peripherals continue to operate and any interrupt/event can wake up the system.

- **Deep-sleep** mode
  In deep-sleep mode, all clocks in the 1.2 V domain are off, and all of the high speed crystal oscillator (IRC8M, HXTAL) and PLL are disabled. Only the contents of SRAM and registers are retained. Any interrupt or wakeup event from EXTI lines can wake up the system from the deep-sleep mode including the up to 16 external lines, the RTC alarm, RTC tamper, CMP output, LVD output and USART wakeup. When exiting the deep-sleep mode, the IRC8M is selected as the system clock.
- **Standby** mode
  In standby mode, the whole 1.2 V domain is power off, the LDO is shut down, and all of IRC8M, HXTAL and PLL are disabled. The contents of SRAM and registers (except backup registers) are lost. There are four wakeup sources for the standby mode, including the external reset from NRST pin, the RTC alarm, the FWDGT reset, and the rising edge on WKUP pin.

3.6 Analog to digital converter (ADC)

- 12-bit SAR ADC's conversion rate is up to 2 MSPS
- 12-bit, 10-bit, 8-bit or 6-bit configurable resolution
- Hardware oversampling ratio adjustable from 2 to 256x improves resolution to 16-bit
- Support references from internal 2.5 V precision reference or external V_{REF} pin.
- Input voltage range: 0 to V_{REF}
- Temperature sensor

One 12-bit 2 MSPS multi-channel ADC is integrated in the device. It has a total of 18 multiplexed channels: up to 16 external channels, 1 channel for internal temperature sensor (V_{SENSE}) and 1 channel for internal reference voltage (V_{REFINT}). The input voltage range is between 0 and V_{REF}. An on-chip hardware oversampling scheme improves performance while off-loading the related computational burden from the CPU. An analog watchdog block can be used to detect the channels, which are required to remain within a specific threshold window. A configurable channel management block can be used to perform conversions in single, continuous, scan or discontinuous mode to support more advanced use.

The ADC can be triggered from the events generated by the general level 0 timers (TIMERx) and the advanced timer (TIMER0) with internal connection. The temperature sensor can be used to generate a voltage that varies linearly with temperature. It is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage in a digital value.

3.7 Digital to analog converter (DAC)

- Two 12-bit DACs with four independent output channels

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- 8-bit or 12-bit mode in conjunction with the DMA controller
- DACs output can be configured to retention when system reset
- Support references from internal 2.5 V precision reference or external V_{REF} pin.

The 12-bit buffered DAC is used to generate variable analog outputs. The DAC channels can be triggered by the timer or EXTI with DMA support. In dual DAC channel operation, conversions could be done independently or simultaneously. The maximum output value of the DAC is V_{REF}.

3.8 DMA

- 7 channels DMA controller
- Peripherals supported: Timers, ADC, DACs, SPIs, I2Cs, USARTs and I2S

The flexible general-purpose DMA controllers provide a hardware method of transferring data between peripherals and/or memory without intervention from the CPU, thereby freeing up bandwidth for other system functions. Three types of access method are supported: peripheral to memory, memory to peripheral, memory to memory.

Each channel is connected to fixed hardware DMA requests. The priorities of DMA channel requests are determined by software configuration and hardware channel number. Transfer size of source and destination are independent and configurable.

3.9 General-purpose inputs/outputs (GPIOs)

- Up to 28 fast GPIOs, all mappable on 16 external interrupt lines
- Analog input/output configurable
- Alternate function input/output configurable
- GPIO state retention when system reset

There are up to 28 general purpose I/O pins (GPIO) in GD32E232xx, named PA0 ~ PA15 and PB0 ~ PB9, PF0 ~ PF1 to implement logic input/output functions. Each of the GPIO ports has related control and configuration registers to satisfy the requirements of specific applications. The external interrupts on the GPIO pins of the device have related control and configuration registers in the Interrupt/event controller (EXTI). The GPIO ports are pin-shared with other alternative functions (AFs) to obtain maximum flexibility on the package pins. Each of the GPIO pins can be configured by software as output (push-pull open-drain or analog), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current capable except for analog inputs.

3.10 Timers and PWM generation

- One 16-bit advanced timer (TIMER0), one 32-bit general timer (TIMER1), up to five 16-

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bit general timers (TIMER2, TIMER13 ~ TIMER16), and two 16-bit basic timer (TIMER5, TIMER6)

- Up to 4 independent channels of PWM, output compare or input capture for each general timer and external trigger input
- 16-bit, motor control PWM advanced timer with programmable dead-time generation for output match
- Encoder interface controller with two inputs using quadrature decoder
- 24-bit SysTick timer down counter
- 2 watchdog timers (free watchdog timer and window watchdog timer)

The advanced timer (TIMER0) can be used as a three-phase PWM multiplexed on 6 channels. It has complementary PWM outputs with programmable dead-time generation. It can also be used as a complete general timer. The 4 independent channels can be used for input capture, output compare, PWM generation (edge- or center- aligned counting modes) and single pulse mode output. If configured as a general 16-bit timer, it has the same functions as the TIMERx timer. It can be synchronized with external signals or to interconnect with other general timers together which have the same architecture and features.

The general timer can be used for a variety of purposes including general time, input signal pulse width measurement or output waveform generation such as a single pulse generation or PWM output, up to 4 independent channels for input capture/output compare. TIMER1 is based on a 32-bit auto-reload up/down counter and a 16-bit prescaler. TIMER2 is based on a 16-bit auto-reload up/down counter and a 16-bit prescaler. TIMER13 ~ TIMER16 is based on a 16-bit auto-reload up counter and a 16-bit prescaler. The general timer also supports an encoder interface with two inputs using quadrature decoder.

The basic timer, known as TIMER5 &TIMER6, are mainly used for DAC trigger generation. They can also be used as a simple 16-bit time base.

The GD32E232xx have two watchdog peripherals, free watchdog and window watchdog. They offer a combination of high safety level, flexibility of use and timing accuracy.

The free watchdog timer includes a 12-bit down-counting counter and an 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently of the main clock, it can operate in deep-sleep and standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management.

The window watchdog is based on a 7-bit down counter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early wakeup interrupt capability and the counter can be frozen in debug mode.

The SysTick timer is dedicated for OS, but could also be used as a standard down counter. The features are shown below:

- A 24-bit down counter
- Auto reload capability

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- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

3.11 Real time clock (RTC)

- Independent binary-coded decimal (BCD) format timer/counter with five 32-bit backup registers.
- Calendar with subsecond, second, minute, hour, week day, date, year and month automatically correction
- Alarm function with wake up from deep-sleep and standby mode capability
- On-the-fly correction for synchronization with master clock. Digital calibration with 0.954 ppm resolution for compensation of quartz crystal inaccuracy.

The real time clock is an independent timer which provides a set of continuously running counters in backup registers to provide a real calendar function, and provides an alarm interrupt or an expected interrupt. It is not reset by a system or power reset, or when the device wakes up from standby mode. In the RTC unit, there are two prescalers used for implementing the calendar and other functions. One prescaler is a 7-bit asynchronous prescaler and the other is a 15-bit synchronous prescaler.

3.12 Inter-integrated circuit (I2C)

- Two I2C bus interfaces can support both master and slave mode with a frequency up to 1 MHz (Fast mode plus)
- Provide arbitration function, optional PEC (packet error checking) generation and checking
- Support 7-bit and 10-bit addressing mode and general call addressing mode
- Support SAM_V mode

The I2C interface is an internal circuit allowing communication with an external I2C interface which is an industry standard two line serial interface used for connection to external hardware. These two serial lines are known as a serial data line (SDA) and a serial clock line (SCL). The I2C module provides different data transfer rates: up to 100 kHz in standard mode, up to 400 kHz in the fast mode and up to 1 MHz in the fast mode plus. The I2C module also has an arbitration detect function to prevent the situation where more than one master attempts to transmit data to the I2C bus at the same time. A CRC-8 calculator is also provided in I2C interface to perform packet error checking for I2C data.

3.13 Serial peripheral interface (SPI)

- Up to two SPI interfaces with a frequency of up to 18 MHz
- Support both master and slave mode
- Hardware CRC calculation and transmit automatic CRC error checking

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- Separate transmit and receive 32-bit FIFO with DMA capability (only in SPI1)
- Data frame size can be 4 to 16 bits (only in SPI1)
- Quad-SPI configuration available in master mode (only in SPI1)

The SPI interface uses 4 pins, among which are the serial data input and output lines (MISO & MOSI), the clock line (SCK) and the slave select line (NSS). Both SPIs can be served by the DMA controller. The SPI interface may be used for a variety of purposes, including simplex synchronous transfers on two lines with a possible bidirectional data line or reliable communication using CRC checking. Specially, SPI1 has separate transmit and receive 32-bit FIFO with DMA capability and its data frame size can be 4 to 16 bits. Quad-SPI master mode is also supported in SPI1.

3.14 Universal synchronous asynchronous receiver transmitter (USART)

- Two USARTs with operating frequency up to 4.5 MBits/s
- Supports both asynchronous and clocked synchronous serial communication modes
- IrDA SIR encoder and decoder support
- LIN break generation and detection
- ISO 7816-3 compliant smart card interface

The USART (USART0, USART1) are used to translate data between parallel and serial interfaces, provides a flexible full duplex data exchange using synchronous or asynchronous transfer. It is also commonly used for RS-232 standard communication. The USART includes a programmable baud rate generator which is capable of dividing the system clock to produce a dedicated clock for the USART transmitter and receiver. The USART also supports DMA function for high speed data communication.

3.15 Inter-IC sound (I2S)

- One I2S bus Interfaces with sampling frequency from 8 kHz to 192 kHz, multiplexed with SPI0
- Support either master or slave mode

The Inter-IC sound (I2S) bus provides a standard communication interface for digital audio applications by 3-wire serial lines. GD32E232xx contain an I2S-bus interface that can be operated with 16/32 bit resolution in master or slave mode, pin multiplexed with SPI0. The audio sampling frequency from 8 kHz to 192 kHz is supported with less than 0.5% accuracy error.

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3.16 Comparators (CMP)

- One fast rail-to-rail low-power comparators with software configurable
- Programmable reference voltage (internal or external I/O)

One comparator (CMP) is implemented within the devices. It can wake up from deep-sleep mode to generate interrupts and breaks for the timers and also can be combined as a window comparator. The internal voltage reference is also connected to ADC_IN17 input channel of the ADC.

3.17 Configurable logic array (CLA)

- Four independent CLA units, with two input multiplexers, supporting 16 input signals, including external pins, timer channels, ADC, and CLA asynchronous outputs
- A Look-up table(LUT) providing 256 programmable digital logic functions is implemented in each CLA units
- Programmable asynchronous and synchronous output
- CLA output can be configured to synchronize with external pins and timers
- Four CLA units can be combined and support complicated logic operations

The configurable logic array provides 256 programmable digital logic operations for external pins, ADC and timers without intervention from the CPU. Four independent CLA units are implemented in this module. Each CLA unit supports configurable asynchronous and synchronous output for GPIO pins.

3.18 Debug mode

- Serial wire debug port

Debug capabilities can be accessed by a debug tool via Serial Wire (SW - Debug Port).

3.19 Package and operation temperature

- QFN32 (GD32E232KxQ7) and QFN24 (GD32E232ExU7).
- Operation temperature range: -40°C to +105°C (industrial level)

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4 Electrical characteristics

4.1 Absolute maximum ratings

The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 4-1. Absolute maximum ratings(1) (4)

Symbol	Parameter	Min	Max	Unit
V_{DD}	External voltage range(2)	V_{SS} - 0.3	V_{SS} + 3.6	V
V_{DDA}	External analog supply voltage	V_{SSA} - 0.3	V_{SSA} + 3.6	V
V_{IN}	Input voltage on 5V tolerant pin(3)	V_{SS} - 0.3	V_{DD} + 3.6	V
	Input voltage on other I/O	V_{SS} - 0.3	3.6	V
$\|\Delta V_{DDx}\|$	Variations between different V_{DD} power pins	—	50	mV
$\|V_{SSX} - V_{SS}\|$	Variations between different ground pins	—	50	mV
I_{IO}	Maximum current for GPIO pin	—	±25	mA
T_A	Operating temperature range	-40	+105	°C
T_{STG}	Storage temperature range	-55	+150	°C
T_J	Maximum junction temperature	—	125	°C

(1). Guaranteed by design, not tested in production.

(2). All main power and ground pins should be connected to an external power source within the allowable range.

(3). V_{IN} maximum value cannot exceed 6.5 V.

(4). It is recommended that V_{DD} and V_{DDA} are powered by the same source. The maximum difference between V_{DD} and V_{DDA} does not exceed 300 mV during power-up and operation.

4.2 Operating conditions characteristics

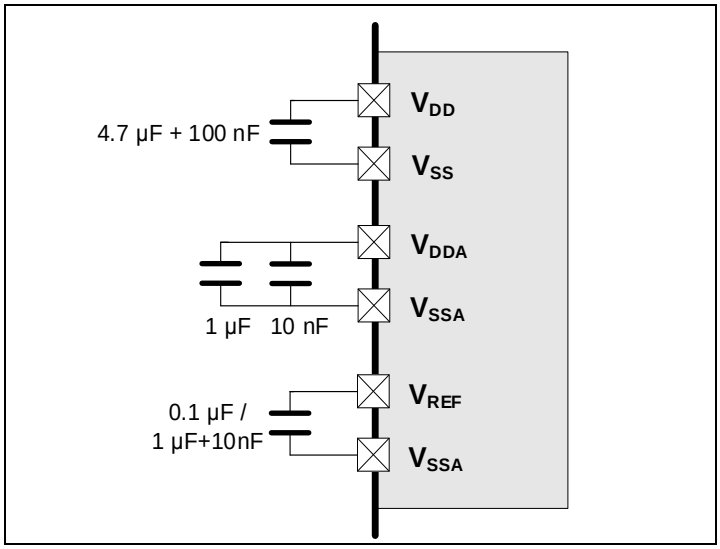
Table 4-2. DC operating conditions

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
V_{DD}	Supply voltage	—	1.8	3.3	3.6	V
V_{DDA}	Analog supply voltage ADC not used	—	1.8	3.3	3.6	V
	Analog supply voltage ADC used		2.4	3.3	3.6	

(1). Based on characterization, not tested in production.

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Figure 4-1. Recommended power supply decoupling capacitors(1) (2)



(1). When using precision internal reference voltage, and a bypass capacitor about 0.1 µF (or 1 µF and 10 nF connected in parallel, which is recommended) to ground is required.

(2). All decoupling capacitors need to be as close as possible to the pins on the PCB board.

Table 4-3. Clock frequency

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK1}	AHB1 clock frequency	—	—	72	MHz
f_{HCLK2}	AHB2 clock frequency	—	—	72	MHz
f_{APB1}	APB1 clock frequency	—	—	72	MHz
f_{APB2}	APB2 clock frequency	—	—	72	MHz

Table 4-4. Operating conditions at Power up/ Power down(1)

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	—	0	∞	µs /V
	V_{DD} fall time rate		20	∞	

(1). Based on characterization, not tested in production.

Table 4-5. Start-up timings of Operating conditions(1) (2) (3)

Symbol	Parameter	Conditions	Typ	Unit
$t_{start-up}$	Start-up time	Clock source from HXTAL	600	µs
		Clock source from IRC8M	64.8	

(1). Based on characterization, not tested in production.

(2). After power-up, the start-up time is the time between the rising edge of NRST high and the main function.

(3). PLL is off.

Table 4-6. Power saving mode wakeup timings characteristics(1) (2)

Symbol	Parameter	Typ	Unit
t_{Sleep}	Wakeup from Sleep mode	3.2	µs
$t_{Deep-sleep}$	Wakeup from Deep-sleep mode（LDO On）	16.3	
	Wakeup from Deep-sleep mode（LDO in low power mode）	16.3	
$t_{Standby}$	Wakeup from Standby mode	70.9	

(1). Based on characterization, not tested in production.

(2). The wakeup time is measured from the wakeup event to the point at which the application code reads the first

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instruction under the below conditions: V_{DD} = V_{DDA} = 3.3 V, IRC8M = System clock = 8 MHz.

4.3 Power consumption

The power measurements specified in the tables represent that code with data executing from on-chip Flash with the following specifications.

Table 4-7. Power consumption characteristics(1) (2) (3) (4) (5)

Symbol	Parameter	Conditions	Typ			Max	Unit
			T_A = 25℃	T_A = 85℃	T_A = 105℃		
I_{DD}+I_{DDA}	Supply current (Run mode)	V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 72 MHz, All peripherals enabled	9.8	9.8	10.0	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 72 MHz, All peripherals disabled	5.9	6.1	6.2	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 48 MHz, All peripherals enabled	7.1	7.2	7.3	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 48 MHz, All peripherals disabled	4.5	4.6	4.7	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 36 MHz, All peripherals enabled	5.7	5.8	5.9	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 36 MHz, All peripherals disabled	3.8	3.9	4.0	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 24 MHz, All peripherals enabled	4.4	4.5	4.6	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 24 MHz, All peripherals disabled	3.1	3.2	3.3	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 16 MHz, All peripherals enabled	3.5	3.6	3.7	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 16 MHz, All peripherals disabled	2.6	2.7	2.8	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 8 MHz, All peripherals enabled	2.4	2.5	2.6	—	mA

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Symbol	Parameter	Conditions	Typ			Max	Unit
			T_A = 25℃	T_A = 85℃	T_A = 105℃		
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 8 MHz, All peripherals disabled	1.9	1.9	2.0	-—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 4 MHz, System clock = 4 MHz, All peripherals enabled	0.8	0.9	1.0	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 4 MHz, System clock = 4 MHz, All peripherals disabled	0.6	0.7	0.8	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 2 MHz, System clock = 2 MHz, All peripherals enabled	0.6	0.7	0.8	-—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 2 MHz, System clock = 2 MHz, All peripherals disabled	0.5	0.6	0.7	—	mA
	Supply current (Sleep mode)	V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, CPU clock off, System clock = 72 MHz, All peripherals enabled	8.3	8.4	8.5	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, CPU clock off, System clock = 72 MHz, All peripherals disabled	3.7	3.9	4.0	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, CPU clock off, System clock = 48 MHz, All peripherals enabled	6.1	6.2	6.3	-—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, CPU clock off, System clock = 48 MHz, All peripherals disabled	3.0	3.2	3.3	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, CPU clock off, System clock = 36 MHz, All peripherals enabled	4.9	5.0	5.1	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, CPU clock off, System clock = 36 MHz, All peripherals disabled	2.7	2.9	3.0	-—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, CPU clock off, System clock = 24 MHz, All peripherals enabled	3.9	4.0	4.1	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, CPU clock off, System clock = 24 MHz, All peripherals disabled	2.4	2.6	2.7	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, CPU clock off, System clock = 16 MHz, All peripherals enabled	3.1	3.2	3.3	-—	mA

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Symbol	Parameter	Conditions	Typ			Max	Unit
			T_A = 25℃	T_A = 85℃	T_A = 105℃		
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, CPU clock off, System clock = 16 MHz, All peripherals disabled	2.1	2.3	2.4	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, CPU clock off, System clock = 8 MHz, All peripherals enabled	2.2	2.3	2.4	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, CPU clock off, System clock = 8 MHz, All peripherals disabled	1.7	1.9	2.0	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 4 MHz, CPU clock off, System clock = 4 MHz, All peripherals enabled	0.7	0.8	0.9	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 4 MHz, CPU clock off, System clock = 4 MHz, All peripherals disabled	0.5	0.6	0.7	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 2 MHz, CPU clock off, System clock = 2 MHz, All peripherals enabled	0.5	0.6	0.7	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 2 MHz, CPU clock off, System clock = 2 MHz, All peripherals disabled	0.4	0.5	0.6	—	mA
	Supply current (Deep-sleep mode)	V_{DD} = V_{DDA} = 3.3 V, LDO in run mode, IRC40K off, RTC off, All GPIOs analog mode	25.2	55.1	155.2	—	μA
		V_{DD} = V_{DDA} = 3.3 V, LDO in low power mode, IRC40K off, RTC off, All GPIOs analog mode	11.4	38.5	130.7	—	μA
	Supply current (Standby mode)	V_{DD} = V_{DDA} = 3.3 V, IRC40K on, RTC on, V_{DDA} Monitor on	3.9	4.2	6.9	—	μA
		V_{DD} = V_{DDA} = 3.3 V, IRC40K on, RTC off, V_{DDA} Monitor on	3.7	4.0	6.7	—	μA
		V_{DD} = V_{DDA} = 3.3 V, IRC40K off, RTC off, V_{DDA} Monitor on	3.1	3.5	6.2	—	μA
		V_{DD} = V_{DDA} = 3.3 V, IRC40K off, RTC off, V_{DDA} Monitor off	1.5	1.8	4.5	—	μA

(1). Based on characterization, not tested in production.

(2). Unless otherwise specified, all values given for T_A condition and test result is mean value.

(3). When System Clock is less than 4 MHz, an external source is used, and the HXTAL bypass function is needed, no PLL.

(4). When System Clock is greater than 8 MHz, a crystal 8 MHz is used, and the HXTAL bypass function is closed, using PLL.

(5). When analog peripheral blocks such as ADCs, DACs, HXTAL, IRC8M, or IRC40K are ON, an additional power consumption should be considered.

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Figure 4-2. Typical supply current consumption in Run mode (All peripherals enabled)

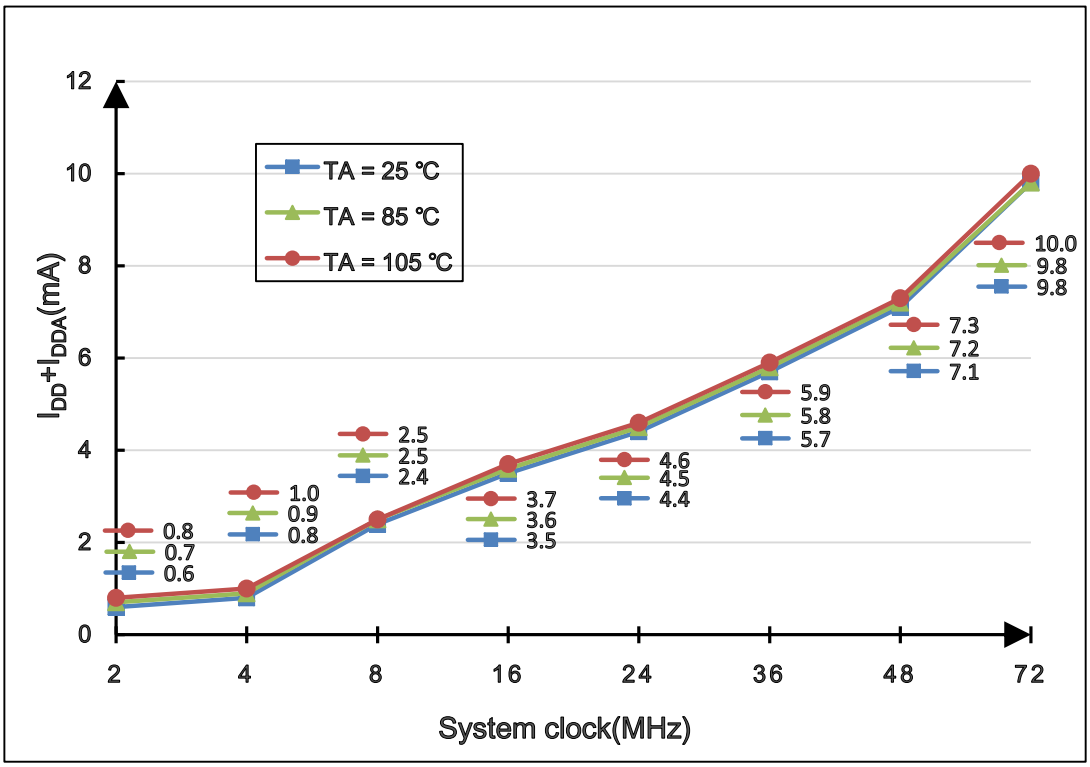
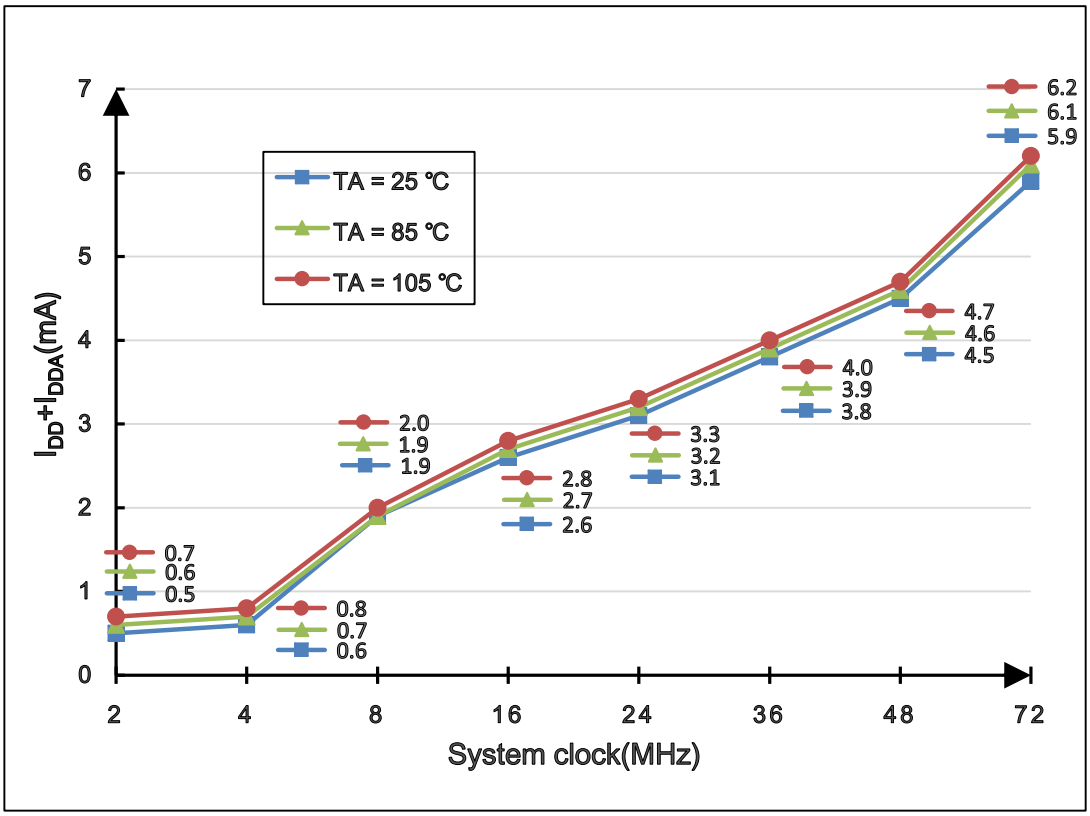


Figure 4-3. Typical supply current consumption in Run mode (All peripherals disabled)



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Figure 4-4. Typical supply current consumption in Sleep mode (All peripherals enabled)

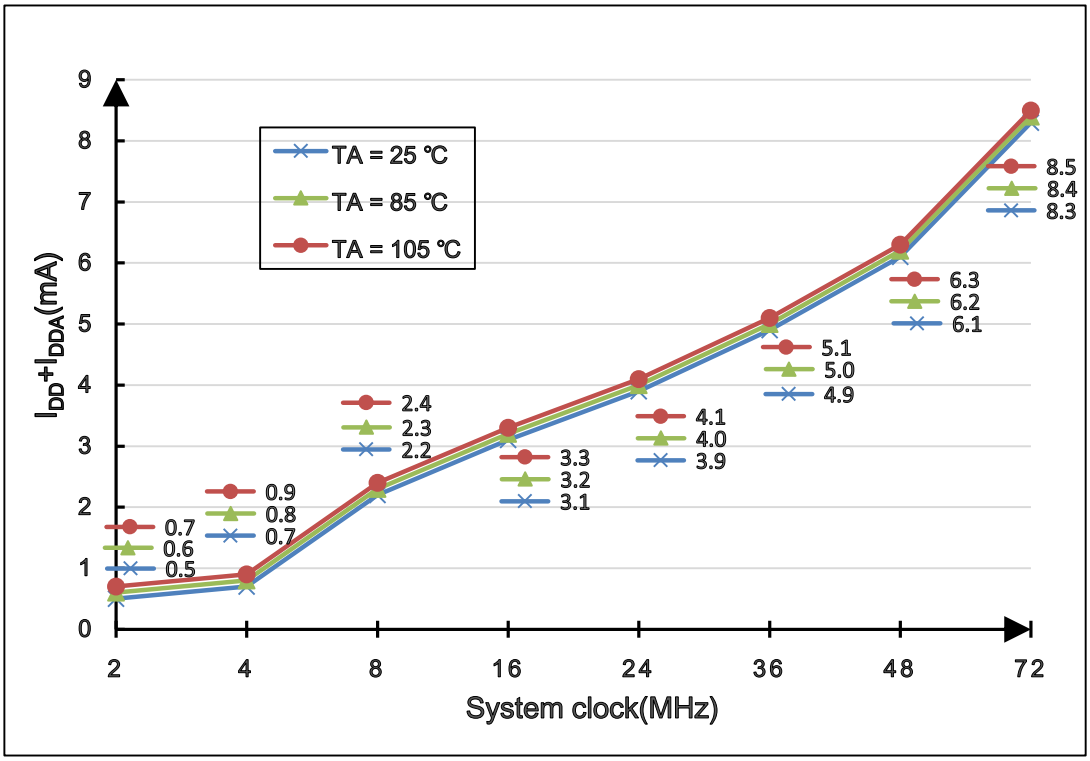
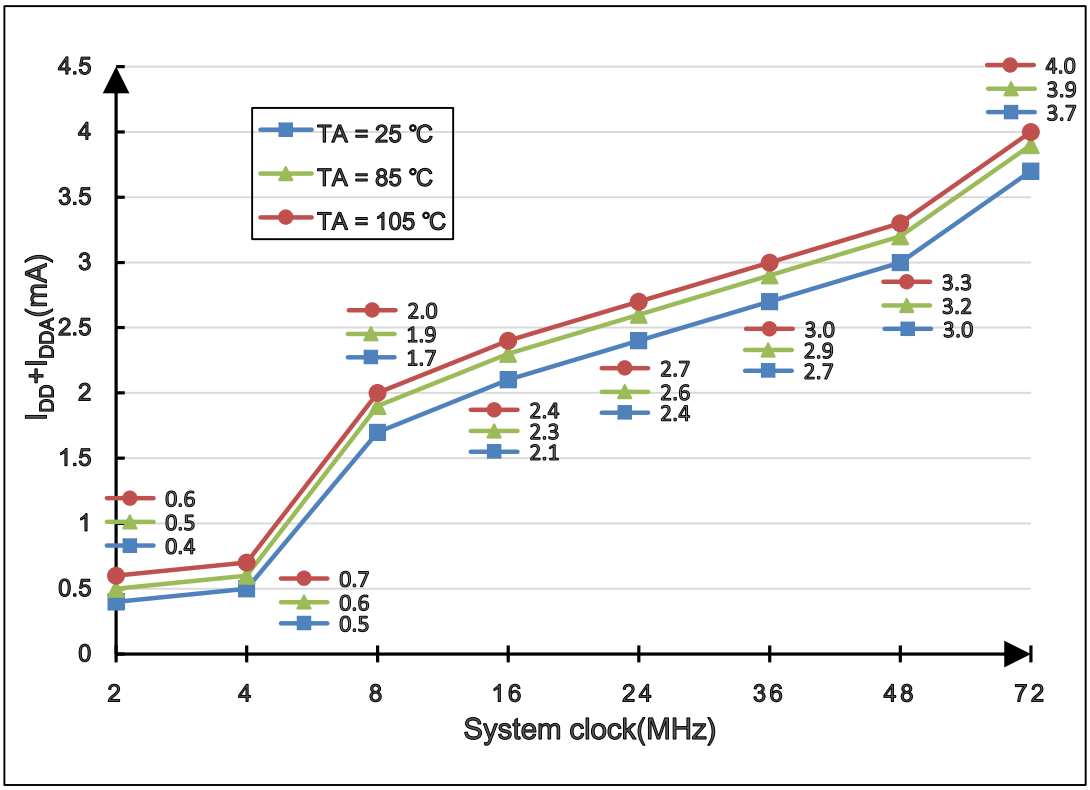


Figure 4-5. Typical supply current consumption in Sleep mode (All peripherals disabled)



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4.4 EMC characteristics

EMS (electromagnetic susceptibility) includes ESD (Electrostatic discharge, positive and negative) and FTB (Burst of Fast Transient voltage, positive and negative) testing result is given in ***Table 4-8. EMS characteristics(1)***, based on the EMS levels and classes compliant with IEC 61000 series standard.

Table 4-8. EMS characteristics(1)

Symbol	Parameter	Conditions	Level/Class
V_{ESD}	Voltage applied to all device pins to induce a functional disturbance	V_{DD} = 3.3 V, T_A = 25 °C, QFN32, f_{HCLK} = 72 MHz conforms to IEC 61000-4-2	3A
V_{FTB}	Fast transient voltage burst applied to induce a functional disturbance through 100 pF on V_{DD} and V_{SS} pins	V_{DD} = 3.3 V, T_A = 25 °C, QFN32, f_{HCLK} = 72 MHz conforms to IEC 61000-4-4	4A

(1). Based on characterization, not tested in production.

4.5 Power supply supervisor characteristics

Table 4-9. Power supply supervisor characteristics

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{LVD}(1)	Low Voltage Detector Threshold	LVDT[2:0] = 000, rising edge	—	2.18	—	V
		LVDT[2:0] = 000, falling edge	—	2.07	—	V
		LVDT[2:0] = 001, rising edge	—	2.32	—	V
		LVDT[2:0] = 001, falling edge	—	2.21	—	V
		LVDT[2:0] = 010, rising edge	—	2.47	—	V
		LVDT[2:0] = 010, falling edge	—	2.35	—	V
		LVDT[2:0] = 011, rising edge	—	2.61	—	V
		LVDT[2:0] = 011, falling edge	—	2.50	—	V
		LVDT[2:0] = 100, rising edge	—	2.75	—	V
		LVDT[2:0] = 100, falling edge	—	2.64	—	V
		LVDT[2:0] = 101, rising edge	—	2.89	—	V
		LVDT[2:0] = 101, falling edge	—	2.78	—	V
		LVDT[2:0] = 110, rising edge	—	3.03	—	V
		LVDT[2:0] = 110, falling edge	—	2.93	—	V
		LVDT[2:0] = 111, rising edge	—	3.18	—	V
		LVDT[2:0] = 111, falling edge	—	3.07	—	V
$V_{LVDhyst}$(2)	LVD hysteresis	—	—	100	—	mV
V_{POR}(1)	Power on reset threshold	—	—	1.71	—	V
V_{PDR}(1)	Power down reset threshold		—	1.66	—	V
$V_{PDRhyst}$(2)	PDR hysteresis		—	40	—	mV
$t_{RSTTEMPO}$(2)	Reset temporization		—	2	—	ms

(1). Based on characterization, not tested in production.

(2). Guaranteed by design, not tested in production.

4.6 Electrical sensitivity

The device is strained in order to determine its performance in terms of electrical sensitivity. Electrostatic discharges (ESD) are applied directly to the pins of the sample. Static latch-up (LU) test is based on the two measurement methods.

Table 4-10. ESD characteristics(1)

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = 25 °C; JESD22-A114	—	—	6000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = 25 °C; JESD22-C101	—	—	2000	V

(1). Based on characterization, not tested in production.

Table 4-11. Static latch-up characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
LU	I-test	T_A = 25 °C; JESD78	—	—	±200	mA
	V_{supply} over voltage		—	—	5.4	V

(1). Based on characterization, not tested in production.

4.7 External clock characteristics

Table 4-12. High speed external clock (HXTAL) generated from a crystal/ceramic characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HXTAL}(1)	Crystal or ceramic frequency	V_{DD} = 3.3 V	4	8	32	MHz
R_F(2)	Feedback resistor	V_{DD} = 3.3 V	—	400	—	kΩ
C_{HXTAL}(2)(3)	Recommended matching capacitance on OSCIN and OSCOUT	—	—	20	30	pF
$Ducy_{(HXTAL)}$(2)	Crystal or ceramic duty cycle	—	30	50	70	%
$I_{DD(HXTAL)}$(1)	Crystal or ceramic operating current	V_{DD} = 3.3 V, T_A = 25 °C	—	1.0	—	mA
$t_{SUHXTAL}$(1)	Crystal or ceramic startup time	V_{DD} = 3.3 V, T_A = 25 °C	—	1.8	—	ms

(1). Based on characterization, not tested in production.

(2). Guaranteed by design, not tested in production.

(3). $C_{HXTAL1} = C_{HXTAL2} = 2*(C_{LOAD} - C_S)$, For C_{HXTAL1} and C_{HXTAL2}, it is recommended matching capacitance on OSCIN and OSCOUT. For C_{LOAD}, it is crystal/ceramic load capacitance, provided by the crystal or ceramic manufacturer. For C_S, it is PCB and MCU pin stray capacitance.

Table 4-13. High speed external user clock characteristics (HXTAL in bypass mode)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HXTAL_ext}(1)	External clock source or oscillator frequency	V_{DD} = 3.3 V	1	8	50	MHz
V_{HXTALH}(2)	OSCIN input pin high level voltage	V_{DD} = 3.3 V	0.7 V_{DD}	—	V_{DD}	V
V_{HXTALL}(2)	OSCIN input pin low level voltage		V_{SS}	—	0.3 V_{DD}	
$t_{H/L(HXTAL)}$(2)	OSCIN high or low time	—	5	—	—	ns
$t_{R/F(HXTAL)}$(2)	OSCIN rise or fall time	—	—	—	10	
C_{IN}(1)	OSCIN input capacitance	—	—	5	—	pF
$Ducy_{(HXTAL)}$ (2)	Duty cycle	—	30	50	70	%

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(1). Based on characterization, not tested in production.
(2). Guaranteed by design, not tested in production.

4.8 Internal clock characteristics

Table 4-14. High speed internal clock (IRC8M) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{IRC8M}	High Speed Internal Oscillator (IRC8M) frequency	V_{DD} = V_{DDA} = 3.3 V	—	8	—	MHz
ACC_{IRC8M}	IRC8M oscillator Frequency accuracy, Factory-trimmed	2.7 V ≤ V_{DD} = V_{DDA} ≤ 3.6 V, T_A = -40 °C ~ +105 °C	-2.0	—	+2.0	%
		V_{DD} = V_{DDA} = 3.3 V, T_A = 25°C	-1.0	—	+1.0	%
	IRC8M oscillator Frequency accuracy, User trimming step(1)	—	—	0.5	—	%
$Ducy_{IRC8M}$(2)	IRC8M oscillator duty cycle	V_{DD} = V_{DDA} = 3.3 V, f_{IRC8M} = 8 MHz	45	50	55	%
$I_{DDAIRC8M}$(1)	IRC8M oscillator operating current	V_{DD} = V_{DDA} = 3.3 V, f_{IRC8M} = 8 MHz	—	55	—	μA
$t_{SUIRC8M}$(1)	IRC8M oscillator startup time	V_{DD} = V_{DDA} = 3.3 V, f_{IRC8M} = 8 MHz	—	1.5	—	μs

(1). Based on characterization, not tested in production.
(2). Guaranteed by design, not tested in production.

Table 4-15. Low speed internal clock (IRC40K) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{IRC40K}(1)	Low Speed Internal oscillator (IRC40K) frequency	V_{DD} = V_{DDA} = 3.3 V, T_A = -40°C ~ +105 °C	30	40	60	kHz
$I_{DDAIRC40K}$(2)	IRC40K oscillator operating current	V_{DD} = V_{DDA} = 3.3 V, T_A = 25 °C	—	0.56	—	μA
$t_{SUIRC40K}$(2)	IRC40K oscillator startup time	V_{DD} = V_{DDA} = 3.3 V, T_A = 25 °C	—	33	—	μs

(1). Guaranteed by design, not tested in production.
(2). Based on characterization, not tested in production.

Table 4-16. High speed internal clock (IRC28M) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{IRC28M}	High Speed Internal Oscillator (IRC28M) frequency	V_{DD} = V_{DDA} = 3.3 V	—	28	—	MHz
ACC_{IRC28M}	IRC28M oscillator Frequency accuracy, Factory-trimmed	2.7 V ≤ V_{DD} = V_{DDA} ≤ 3.6 V, T_A = -40 °C ~ +105 °C	-4.0	—	+4.0	%

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		V_{DD} = V_{DDA} = 3.3 V, T_A = 25 °C	-1.5	—	+1.5	%
	IRC28M oscillator Frequency accuracy, User trimming step(1)	—	—	0.5	—	%
D_{IRC28M}(2)	IRC28M oscillator duty cycle	V_{DD} = V_{DDA} = 3.3 V, f_{IRC28M} = 28 MHz	45	50	55	%
$I_{DDAIRC28M}$(1)	IRC28M oscillator operating current	V_{DD} = V_{DDA} = 3.3 V, f_{IRC28M} = 28 MHz	—	140	—	μA
$t_{SUIRC28M}$(1)	IRC28M oscillator startup time	V_{DD} = V_{DDA} = 3.3 V, f_{IRC28M} = 28 MHz	—	1.5	—	μs

(1). Based on characterization, not tested in production.
(2). Guaranteed by design, not tested in production.

4.9 PLL characteristics

Table 4-17. PLL characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLLIN}(1)	PLL input clock frequency	—	1	—	25	MHz
f_{PLLOUT}	PLL output clock frequency	—	16	—	72	MHz
f_{VCO}	PLL VCO output clock frequency	—	—	—	72	MHz
t_{LOCK}	PLL lock time	—	—	—	300	μs
I_{DD}(2)	Current consumption on V_{DD}	VCO freq = 72 MHz	—	130	—	μA
I_{DDA}(1)	Current consumption on V_{DDA}	—	—	260	—	μA
$Jitter_{PLL}$(3)	Cycle to cycle Jitter（rms）	System clock	—	50	—	ps
	Cycle to cycle Jitter（peak to peak）		—	500	—	

(1). Based on characterization, not tested in production.
(2). Guaranteed by design, not tested in production.
(3). Value given with main PLL running.

4.10 Memory characteristics

Table 4-18. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PE_{CYC}(1)	Number of guaranteed program /erase cycles before failure(Endurance)	T_A = -40 °C ~ +85 °C	100	—	—	kcycles

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{RET}(1)	Data retention time	10k cycles at T_A = 85 °C	10	—	—	years
t_{PROG}(2)	Double word programming time	T_A = -40 °C ~ +105 °C	37	—	44	μs
t_{ERASE}(2)	Page erase time	T_A = -40 °C ~ +105 °C	3.2	—	4	ms
t_{MERASE}(2)	Mass erase time	T_A = -40 °C ~ +105 °C	8	—	10	ms

(1). Based on characterization, not tested in production.
(2). Guaranteed by design, not tested in production.

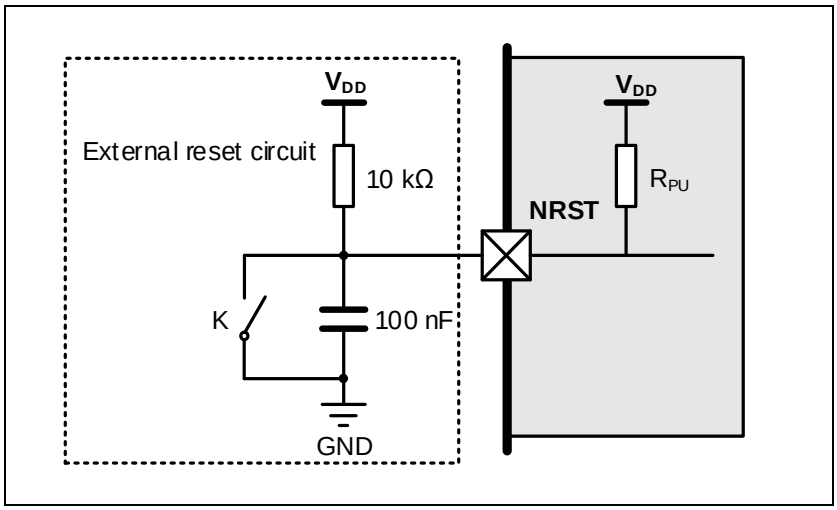
4.11 NRST pin characteristics

Table 4-19. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST Input low level voltage	V_{DD} = V_{DDA} = 2.5 V	-0.5	—	0.35 V_{DD}	V
$V_{IH(NRST)}$	NRST Input high level voltage		0.65 V_{DD}	—	V_{DD} + 0.5	
V_{hyst}	Schmidt trigger Voltage hysteresis		—	190	—	mV
$V_{IL(NRST)}$	NRST Input low level voltage	V_{DD} = V_{DDA} = 3.3 V	-0.5	—	0.35 V_{DD}	V
$V_{IH(NRST)}$	NRST Input high level voltage		0.65 V_{DD}	—	V_{DD} + 0.5	
V_{hyst}	Schmidt trigger Voltage hysteresis		—	210	—	mV
$V_{IL(NRST)}$	NRST Input low level voltage	V_{DD} = V_{DDA} = 3.6 V	-0.5	—	0.35 V_{DD}	V
$V_{IH(NRST)}$	NRST Input high level voltage		0.65 V_{DD}	—	V_{DD} + 0.5	
V_{hyst}	Schmidt trigger Voltage hysteresis		—	230	—	mV
R_{pu}(1)	Pull-up equivalent resistor	—	—	40	—	kΩ

(1). Guaranteed by design, not tested in production.

Figure 4-6. Recommended external NRST pin circuit



4.12 GPIO characteristics

Table 4-20. I/O port DC characteristics in T_A = -40 ℃

Symbol	Parameter	Conditions			Min	Typ	Max	Unit
V_{IL}(1)	Standard IO Low level input voltage	1.8 V ≤ V_{DD} = V_{DDA} ≤ 3.6 V		IO_Speed = 2 MHz	—	—	0.35 V_{DD}	V
				IO_Speed = 10 MHz	—	—	0.35 V_{DD}	
				IO_Speed = 50 MHz	—	—	0.3 V_{DD}	
	5V-tolerant IO Low level input voltage	1.8 V ≤ V_{DD} = V_{DDA} ≤ 3.6 V		IO_Speed = 2 MHz	—	—	0.35 V_{DD}	V
				IO_Speed = 10 MHz	—	—	0.35 V_{DD}	
				IO_Speed = 50 MHz	—	—	0.3 V_{DD}	
V_{IH}(1)	Standard IO High level input voltage	1.8 V ≤ V_{DD} = V_{DDA} ≤ 3.6 V		IO_Speed = 2 MHz	0.65 V_{DD}	—	—	V
				IO_Speed = 10 MHz	0.65 V_{DD}	—	—	
				IO_Speed = 50 MHz	0.7 V_{DD}	—	—	
	5V-tolerant IO High level input voltage	1.8 V ≤ V_{DD} = V_{DDA} ≤ 3.6 V		IO_Speed = 2 MHz	0.65 V_{DD}	—	—	V
				IO_Speed = 10 MHz	0.65 V_{DD}	—	—	
				IO_Speed = 50 MHz	0.7 V_{DD}	—	—	
V_{OL}(1)	Low level output voltage for an IO Pin	V_{DD} = 1.8 V	IO_Speed = 50 MHz	I_{IO} = +8 mA	—	—	0.5	V
				I_{IO} = +20 mA	—	—	1.0	
		V_{DD} = 2.5 V	IO_Speed = 2 MHz	I_{IO} = +2 mA	—	—	0.6	
				I_{IO} = +3 mA	—	—	0.8	
			IO_Speed = 10 MHz	I_{IO} = +8 mA	—	—	0.6	
				I_{IO} = +16 mA	—	—	1.1	
			IO_Speed = 50 MHz	I_{IO} = +8 mA	—	—	0.4	
				I_{IO} = +20 mA	—	—	0.7	
		V_{DD} = 3.3 V	IO_Speed = 2 MHz	I_{IO} = +2 mA	—	—	0.5	
				I_{IO} = +3 mA	—	—	0.7	
			IO_Speed = 10 MHz	I_{IO} = +8 mA	—	—	0.6	
				I_{IO} = +16 mA	—	—	0.9	
			IO_Speed = 50 MHz	I_{IO} = +8 mA	—	—	0.4	
				I_{IO} = +20 mA	—	—	0.7	
		V_{DD} = 3.6 V	IO_Speed = 2 MHz	I_{IO} = +2 mA	—	—	0.5	
				I_{IO} = +3 mA	—	—	0.7	
			IO_Speed = 10 MHz	I_{IO} = +8 mA	—	—	0.6	
				I_{IO} = +16 mA	—	—	0.9	

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Symbol	Parameter	Conditions			Min	Typ	Max	Unit
			IO_Speed = 50 MHz	I_{IO} = +8 mA	—	—	0.4	
				I_{IO} = +20 mA	—	—	0.7	
V_{OH}(1)	High level output voltage for an IO Pin	V_{DD} = 1.8 V	IO_Speed = 50 MHz	I_{IO} = +8 mA	1.3	—	—	V
				I_{IO} = +20 mA	1.1	—	—	
		V_{DD} = 2.5 V	IO_Speed = 2 MHz	I_{IO} = +2 mA	1.8	—	—	
				I_{IO} = +3 mA	1.5	—	—	
			IO_Speed = 10 MHz	I_{IO} = +8 mA	1.8	—	—	
				I_{IO} = +16 mA	1.0	—	—	
			IO_Speed = 50 MHz	I_{IO} = +8 mA	2.1	—	—	
				I_{IO} = +20 mA	1.7	—	—	
		V_{DD} = 3.3 V	IO_Speed = 2 MHz	I_{IO} = +2 mA	2.7	—	—	
				I_{IO} = +3 mA	2.5	—	—	
			IO_Speed = 10 MHz	I_{IO} = +8 mA	2.7	—	—	
				I_{IO} = +16 mA	2.2	—	—	
			IO_Speed = 50 MHz	I_{IO} = +8 mA	2.9	—	—	
				I_{IO} = +20 mA	2.6	—	—	
		V_{DD} = 3.6 V	IO_Speed = 2 MHz	I_{IO} = +2 mA	3.0	—	—	
				I_{IO} = +3 mA	2.8	—	—	
			IO_Speed = 10 MHz	I_{IO} = +8 mA	3.0	—	—	
				I_{IO} = +16 mA	2.5	—	—	
			IO_Speed = 50 MHz	I_{IO} = +8 mA	3.2	—	—	
				I_{IO} = +20 mA	2.9	—	—	
R_{PU}(2)	Internal pull-up resistor	—			—	40	—	kΩ
R_{PD}(2)	Internal pull-down resistor	—			—	40	—	kΩ

(1). Based on characterization, not tested in production.

(2). Guaranteed by design, not tested in production

Table 4-21. I/O port DC characteristics in T_A = 25 ℃

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IL}(1)	Standard IO Low level input voltage	1.8 V ≤ V_{DD} = V_{DDA} ≤ 3.6 V	IO_Speed = 2 MHz	—	—	0.35 V_{DD}	V
			IO_Speed = 10 MHz	—	—	0.35 V_{DD}	
			IO_Speed = 50 MHz	—	—	0.3 V_{DD}	
	5V-tolerant IO Low level input voltage	1.8 V ≤ V_{DD} = V_{DDA} ≤ 3.6 V	IO_Speed = 2 MHz	—	—	0.35 V_{DD}	V
			IO_Speed = 10 MHz	—	—	0.35 V_{DD}	
			IO_Speed =	—	—	0.3 V_{DD}	

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Symbol	Parameter	Conditions			Min	Typ	Max	Unit
				50 MHz				
V_{IH}(1)	Standard IO High level input voltage	1.8 V ≤ V_{DD} = V_{DDA} ≤ 3.6 V		IO_Speed = 2 MHz	0.65 V_{DD}	—	—	V
				IO_Speed = 10 MHz	0.65 V_{DD}	—	—	
				IO_Speed = 50 MHz	0.7 V_{DD}	—	—	
	5V-tolerant IO High level input voltage	1.8 V ≤ V_{DD} = V_{DDA} ≤ 3.6 V		IO_Speed = 2 MHz	0.65 V_{DD}	—	—	V
				IO_Speed = 10 MHz	0.65 V_{DD}	—	—	
				IO_Speed = 50 MHz	0.7 V_{DD}	—	—	
V_{OL}	Low level output voltage for an IO Pin	V_{DD} = 1.8 V	IO_Speed = 50 MHz(1)	I_{IO} = +8 mA	—	—	0.5	V
				I_{IO} = +20 mA	—	—	0.9	
		V_{DD} = 2.5 V	IO_Speed = 2 MHz(1)	I_{IO} = +2 mA	—	—	0.7	
				I_{IO} = +3 mA	—	—	0.9	
			IO_Speed = 10 MHz(1)	I_{IO} = +8 mA	—	—	0.7	
				I_{IO} = +16 mA	—	—	1.5	
			IO_Speed = 50 MHz	I_{IO} = +8 mA	—	—	0.4	
				I_{IO} = +20 mA	—	—	0.7	
		V_{DD} = 3.3 V	IO_Speed = 2 MHz(1)	I_{IO} = +2 mA	—	—	0.6	
				I_{IO} = +3 mA	—	—	0.8	
			IO_Speed = 10 MHz(1)	I_{IO} = +8 mA	—	—	0.6	
				I_{IO} = +16 mA	—	—	1.0	
			IO_Speed = 50 MHz	I_{IO} = +8 mA	—	—	0.4	
				I_{IO} = +20 mA	—	—	0.6	
		V_{DD} = 3.6 V	IO_Speed = 2 MHz(1)	I_{IO} = +2 mA	—	—	0.6	
				I_{IO} = +3 mA	—	—	0.8	
			IO_Speed = 10 MHz(1)	I_{IO} = +8 mA	—	—	0.6	
				I_{IO} = +16 mA	—	—	1.0	
			IO_Speed = 50 MHz	I_{IO} = +8 mA	—	—	0.4	
				I_{IO} = +20 mA	—	—	0.6	
V_{OH}	High level output voltage for an IO Pin	V_{DD} = 1.8 V	IO_Speed = 50 MHz(1)	I_{IO} = +8 mA	1.2	—	—	V
				I_{IO} = +20 mA	1.0	—	—	
		V_{DD} = 2.5 V	IO_Speed = 2 MHz(1)	I_{IO} = +2 mA	1.7	—	—	
				I_{IO} = +3 mA	1.3	—	—	
			IO_Speed = 10 MHz(1)	I_{IO} = +8 mA	1.7	—	—	
				I_{IO} = +12 mA	1.4	—	—	
			IO_Speed = 50 MHz	I_{IO} = +8 mA	2.0	—	—	
				I_{IO} = +20 mA	1.6	—	—	

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Symbol	Parameter	Conditions			Min	Typ	Max	Unit
		V_{DD} = 3.3 V	IO_Speed = 2 MHz(1)	I_{IO} = +2 mA	2.6	—	—	
				I_{IO} = +3 mA	2.4	—	—	
			IO_Speed = 10 MHz(1)	I_{IO} = +8 mA	2.6	—	—	
				I_{IO} = +16 mA	2.0	—	—	
			IO_Speed = 50 MHz	I_{IO} = +8 mA	2.8	—	—	
				I_{IO} = +20 mA	2.5	—	—	
		V_{DD} = 3.6 V	IO_Speed = 2 MHz(1)	I_{IO} = +2 mA	2.9	—	—	
				I_{IO} = +3 mA	2.7	—	—	
			IO_Speed = 10 MHz(1)	I_{IO} = +8 mA	2.9	—	—	
				I_{IO} = +16 mA	2.4	—	—	
			IO_Speed = 50 MHz	I_{IO} = +8 mA	3.2	—	—	
				I_{IO} = +20 mA	2.8	—	—	
R_{PU}(2)	Internal pull-up resistor	—			—	40	—	kΩ
R_{PD}(2)	Internal pull-down resistor	—			—	40	—	kΩ

(1). Based on characterization, not tested in production.

(2). Guaranteed by design, not tested in production.

Table 4-22. I/O port DC characteristics in T_A = 105 ℃

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IL}(1)	Standard IO Low level input voltage	1.8 V ≤ V_{DD} = V_{DDA} ≤ 3.6 V	IO_Speed = 2 MHz	—	—	0.35 V_{DD}	V
			IO_Speed = 10 MHz	—	—	0.35 V_{DD}	
			IO_Speed = 50 MHz	—	—	0.3 V_{DD}	
	5V-tolerant IO Low level input voltage	1.8 V ≤ V_{DD} = V_{DDA} ≤ 3.6 V	IO_Speed = 2 MHz	—	—	0.35 V_{DD}	V
			IO_Speed = 10 MHz	—	—	0.35 V_{DD}	
			IO_Speed = 50 MHz	—	—	0.3 V_{DD}	
V_{IH}(1)	Standard IO High level input voltage	1.8 V ≤ V_{DD} = V_{DDA} ≤ 3.6 V	IO_Speed = 2 MHz	0.65 V_{DD}	—	—	V
			IO_Speed = 10 MHz	0.65 V_{DD}	—	—	
			IO_Speed = 50 MHz	0.7 V_{DD}	—	—	
	5V-tolerant IO High level input voltage	1.8 V ≤ V_{DD} = V_{DDA} ≤ 3.6 V	IO_Speed = 2 MHz	0.65 V_{DD}	—	—	V
			IO_Speed = 10 MHz	0.65 V_{DD}	—	—	

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Symbol	Parameter	Conditions			Min	Typ	Max	Unit
				IO_Speed = 50 MHz	0.7 V_{DD}	—	—	
V_{OL}(1)	Low level output voltage for an IO Pin	V_{DD} = 1.8 V	IO_Speed = 50 MHz	I_{IO} = +8 mA	—	—	0.5	V
				I_{IO} = +20 mA	—	—	1.0	
		V_{DD} = 2.5 V	IO_Speed = 2 MHz	I_{IO} = +2 mA	—	—	0.8	
				I_{IO} = +3 mA	—	—	1.3	
			IO_Speed = 10 MHz	I_{IO} = +8 mA	—	—	0.9	
				I_{IO} = +12 mA	—	—	1.5	
			IO_Speed = 50 MHz	I_{IO} = +8 mA	—	—	0.4	
				I_{IO} = +20 mA	—	—	0.7	
		V_{DD} = 3.3 V	IO_Speed = 2 MHz	I_{IO} = +2 mA	—	—	0.7	
				I_{IO} = +3 mA	—	—	1.0	
			IO_Speed = 10 MHz	I_{IO} = +8 mA	—	—	0.7	
				I_{IO} = +16 mA	—	—	1.4	
			IO_Speed = 50 MHz	I_{IO} = +8 mA	—	—	0.4	
				I_{IO} = +20 mA	—	—	0.6	
		V_{DD} = 3.6 V	IO_Speed = 2 MHz	I_{IO} = +2 mA	—	—	0.7	
				I_{IO} = +3 mA	—	—	0.9	
			IO_Speed = 10 MHz	I_{IO} = +8 mA	—	—	0.7	
				I_{IO} = +16 mA	—	—	1.3	
			IO_Speed = 50 MHz	I_{IO} = +8 mA	—	—	0.4	
				I_{IO} = +20 mA	—	—	0.6	
V_{OH}(1)	High level output voltage for an IO Pin	V_{DD} = 1.8 V	IO_Speed = 50 MHz	I_{IO} = +8 mA	1.1	—	—	V
				I_{IO} = +20 mA	0.8	—	—	
		V_{DD} = 2.5 V	IO_Speed = 2 MHz	I_{IO} = +2 mA	2.1	—	—	
				I_{IO} = +3 mA	2.0	—	—	
			IO_Speed = 10 MHz	I_{IO} = +8 mA	1.5	—	—	
				I_{IO} = +12 mA	0.8	—	—	
			IO_Speed = 50 MHz	I_{IO} = +8 mA	1.9	—	—	
				I_{IO} = +20 mA	1.5	—	—	
		V_{DD} = 3.3 V	IO_Speed = 2 MHz	I_{IO} = +2 mA	2.9	—	—	
				I_{IO} = +3 mA	2.9	—	—	
			IO_Speed = 10 MHz	I_{IO} = +8 mA	2.5	—	—	
				I_{IO} = +16 mA	1.7	—	—	
			IO_Speed = 50 MHz	I_{IO} = +8 mA	2.8	—	—	
				I_{IO} = +20 mA	2.3	—	—	
		V_{DD} = 3.6 V	IO_Speed = 2 MHz	I_{IO} = +2 mA	3.2	—	—	
				I_{IO} = +3 mA	3.2	—	—	
			IO_Speed = 10 MHz	I_{IO} = +8 mA	2.8	—	—	
				I_{IO} = +16 mA	2.1	—	—	
			IO_Speed =	I_{IO} = +8 mA	3.1	—	—	

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Symbol	Parameter	Conditions			Min	Typ	Max	Unit
			50 MHz	I_{IO} = +20 mA	2.7	—	—	
R_{PU}(2)	Internal pull-up resistor	—			—	40	—	kΩ
R_{PD}(2)	Internal pull-down resistor	—			—	40	—	kΩ

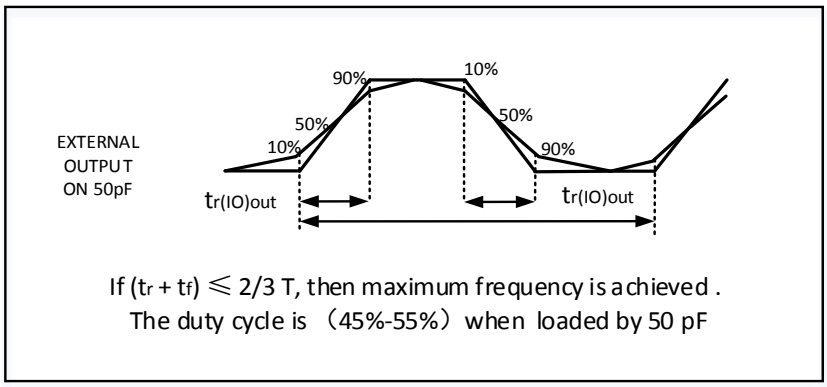
(1). Based on characterization, not tested in production.
(2). Guaranteed by design, not tested in production.

Table 4-23. I/O port AC characteristics(1)(2)

GPIOx_OSPD[1:0] bit value(3)	Parameter	Conditions	Max	Unit
GPIOx_OSPD0->OSPDy[1:0] = X0 （IO_Speed = 2 MHz）	Maximum frequency(4)	1.8 ≤ V_{DD} ≤ 3.6 V, C_L = 10 pF	4	MHz
		1.8 ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF	3	
		1.8 ≤ V_{DD} ≤ 3.6 V, C_L = 50 pF	2	
GPIOx_OSPD0->OSPDy[1:0] = 01 （IO_Speed = 10 MHz）	Maximum frequency(4)	1.8 ≤ V_{DD} ≤ 3.6 V, C_L = 10 pF	24	MHz
		1.8 ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF	16	
		1.8 ≤ V_{DD} ≤ 3.6 V, C_L = 50 pF	14	
GPIOx_OSPD0->OSPDy[1:0] = 11 （IO_Speed = 50 MHz）	Maximum frequency(4)	1.8 ≤ V_{DD} ≤ 3.6 V, C_L = 10 pF	72	MHz
		1.8 ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF	72	
		1.8 ≤ V_{DD} ≤ 3.6 V, C_L = 50 pF	72	

(1). Based on characterization, not tested in production.
(2). Unless otherwise specified, all test results given for T_A = 25 ℃.
(3). The I/O speed is configured using the GPIOx_OSPD0->OSPDy [1:0] bits. Refer to the GD32E232 user manual which is selected to set the GPIO port output speed.
(4). The maximum frequency is defined in ***Figure 4-7. I/O port AC characteristics definition***, and maximum frequency cannot exceed 72 MHz.

Figure 4-7. I/O port AC characteristics definition



4.13 ADC characteristics

Table 4-24. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}(1)	Operating voltage	—	2.4	3.3	3.6	V
V_{IN}(1)	ADC input voltage range	—	0	—	V_{REF}	V

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{ADC}(1)	ADC clock	—	0.1	—	28	MHz
f_S(1)	Sampling rate	12-bit	0.007	—	2	MSPS
		10-bit	0.008	—	2.3	
		8-bit	0.01	—	2.8	
		6-bit	0.011	—	3.5	
V_{AIN}(1)	Analog input voltage	up to 16 external; 2 internal	0	—	V_{REF}	V
R_{AIN}(2)	External input impedance	See ***Equation 1***	—	—	50.6	kΩ
R_{ADC}(2)	Input sampling switch resistance	—	—	—	0.5	kΩ
C_{ADC}(2)	Input sampling capacitance	No pin/ pad capacitance included	—	—	5.5	pF
t_{CAL}(2)	Calibration time	f_{ADC} = 28 MHz	—	4.68	—	μs
t_s(2)	Sampling time	f_{ADC} = 28 MHz	0.05	—	8.55	μs
t_{CONV}(2)	Total conversion time(including sampling time)	12-bit	—	14	—	1/ f_{ADC}
		10-bit	—	12	—	
		8-bit	—	10	—	
		6-bit	—	8	—	
t_{SU}(2)	Startup time	—	—	—	1	μs

(1). Based on characterization, not tested in production.

(2). Guaranteed by design, not tested in production.

Equation 1: R_{AIN} max formula $R_{AIN} < \frac{T_s}{f_{ADC} * C_{ADC} * \ln(2^{N+2})} - R_{ADC}$

The formula above (Equation 1) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

Table 4-25. ADC R_{AIN} max for f_{ADC} = 28 MHz(1)

T_s(cycles)	t_s(μs)	R_{AINmax} (kΩ)
1.5	0.05	0.88
7.5	0.27	6.4
13.5	0.48	11.9
28.5	1.02	25.7
41.5	1.48	37.7
55.5	1.98	50.6
71.5	2.55	NA
239.5	8.55	NA

(1). Based on characterization, not tested in production.

Table 4-26. ADC dynamic accuracy at f_{ADC} = 14 MHz(1)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ENOB	Effective number of bits	f_{ADC} = 14 MHz, V_{DDA} = 3.3 V, Input Frequency = 20 kHz,	—	10.5	—	bits
SNDR	Signal-to-noise and distortion ratio		—	65.0	—	dB
SNR	Signal-to-noise ratio		—	65.7	—	
THD	Total harmonic distortion		—	-74.0	—	

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Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
		Temperature = 25 ℃				

(1). Based on characterization, not tested in production.

Table 4-27. ADC static accuracy at f_{ADC} = 14 MHz

Symbol	Parameter	Test conditions	Typ	Max	Unit
Offset	Offset error	f_{ADC} = 14 MHz, V_{DDA} = 3.3 V	±1	—	LSB
DNL	Differential linearity error		±1.1	±3	
INL	Integral linearity error		±1.6	±5	

4.14 Temperature sensor characteristics

Table 4-28. Temperature sensor characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
T_L	V_{SENSE} linearity with temperature	—	±1.5	—	℃
Avg_Slope	Average slope	—	4.3	—	mV/℃
V_{25}	Voltage at 25 °C	—	1.45	—	V
t_{START}	Startup time	—	—	—	μs
t_{S_temp} (2)	ADC sampling time when reading the temperature	—	17.1	—	μs

(1). Based on characterization, not tested in production.

(2). Shortest sampling time can be determined in the application by multiple iterations.

4.15 DAC characteristics

Table 4-29. DAC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}(1)	Operating voltage	—	1.8	3.3	3.6	V
R_{LOAD}(2)	Load resistance	Resistive load with buffer ON	1	—	—	kΩ
Ro(2)	Impedance output with buffer OFF	—	—	—	35	kΩ
C_{LOAD}(2)	Load capacitance	No pin/pad capacitance included	—	—	100	pF
DAC_OUT min(2)	Lower DAC_OUT voltage with buffer ON	—	0.2	—	—	V
DAC_OUT max(2)	Higher DAC_OUT voltage with buffer ON	—	—	—	V_{REF} - 0.2	V
DAC_OUT min(2)	Lower DAC_OUT voltage with buffer OFF	—	—	0.5	—	mV
DAC_OUT max(2)	Higher DAC_OUT voltage with buffer OFF	—	—	—	V_{REF} - 1LSB	V
I_{DDA}(1)	DAC current consumption in quiescent mode	With no load, middle code(0x800) on the input,	—	420	—	μA

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		V_{DDA} = 3.6 V				
		With no load, worst code(0xF1C) on the input, V_{DDA} = 3.6 V	—	500	—	μA
I_{DDVREF}(1)	DAC current consumption in quiescent mode	With no load, middle code(0x800) on the input, V_{DDA} = 3.6 V	—	40	—	μA
		With no load, worst code(0xF1C) on the input, V_{DDA} = 3.6 V	—	110	—	μA
DNL	Differential non-linearity error	DAC in 12-bit mode	—	±1	±3	LSB
INL	Integral non-linearity	DAC in 12-bit mode	—	±3	±5	LSB
Offset(1)	Offset error	DAC in 12-bit mode	—	—	±12	LSB
GE(1)	Gain error	DAC in 12-bit mode	—	—	±0.5	%
$T_{setting}$(1)	Settling time	$C_{LOAD} \leqslant$ 50 pF, $R_{LOAD} \geqslant$ 5 kΩ	—	0.3	1	μs
Update rate(2)	Max frequency for a correct DAC_OUT change from code i to i±1LSBs	$C_{LOAD} \leqslant$ 50 pF, $R_{LOAD} \geqslant$ 5 kΩ	—	—	2	MS/s
PSRR(2)	Power supply rejection ratio (to V_{DDA})	—	55	70	—	dB

(1). Based on characterization, not tested in production.

(2). Guaranteed by design, not tested in production.

4.16 VREF characteristics

Table 4-30. VREF characteristics

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}(1)	Analog Supply Voltage	—	2.7	3.3	3.6	V
V_{REF}	Output Reference Voltage	V_{DDA} = 3.3 V, T_A = 25 °C	2.498	2.500	2.502	V
		All V_{DDA}, All Temp.	2.47	2.50	2.53	
PSRR(1)	Power Supply Rejection	DC (I_O = 0)	—	73	—	dB
		DC (I_O = 200 μA)	—	68	—	
T_{SU}(1)	Setup Time	C_L = 0.1 μF	—	—	100	μs
		C_L = 0.1 μF + 4.7 μF	—	—	800	
I_{LOAD_R}(1)	Load Regulation	I_{LOAD} from 0 to 200 μA	—	5	—	μV/μA
C_{LOAD}(1)	Load Capacitor	—	0.1	—	—	μF
I_{LINE_R}(1)	Line Regulation	I_{LOAD} = 0	—	1	—	μV/V
		I_{LOAD} = 200 μA	—	1.2	—	
TRIM(1)	Trim Step	—	—	2	—	mV

(1). Guaranteed by design, not tested in production.

4.17 Comparators characteristics

Table 4-31. CMP characteristics

Symbol	Parameter	Conditions	Min	Typ	Max(1)	Unit
V_{DDA}	Operating voltage	—	1.8	3.3	3.6	V
V_{IN}	Input voltage range	—	0	—	V_{DDA}	V
V_{BG}	Scaler input voltage	—	—	1.2	—	V
V_{SC}	Scaler offset voltage	—	—	—	—	mV
t_D	Propagation delay for 200mV step with 100 mV overdrive	Ultra-low power mode	—	0.98	—	μs
		Low power mode	—	0.25	—	μs
		Medium power mode	—	0.12	—	μs
		High speed power mode	—	33	—	μs
I_{DD}	Current consumption	Ultra-low power mode	—	2.2	—	μA
		Low power mode	—	3.2	—	
		Medium power mode	—	8.1	—	
		High speed power mode	—	46.9	—	
V_{offset}	Offset error	—	—	±4	—	mV
V_{hyst}	Hysteresis Voltage	No Hysteresis	—	0	—	mV
		Low Hysteresis	—	11	—	
		Medium Hysteresis	—	22	—	

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Symbol	Parameter	Conditions	Min	Typ	Max(1)	Unit
		High Hysteresis	—	43	—	

(1). Based on characterization, not tested in production.

4.18 I2C characteristics

Table 4-32. I2C characteristics(1)(2)(3)

Symbol	Parameter	Conditions	Standard mode		Fast mode		Fast mode plus		Unit
			Min	Max	Min	Max	Min	Max	
$t_{SCL(H)}$	SCL clock high time	—	4.0	—	0.6	—	0.2	—	μs
$t_{SCL(L)}$	SCL clock low time	—	4.7	—	1.3	—	0.5	—	μs
$t_{su(SDA)}$	SDA setup time	—	250	—	100	—	0.1	—	ns
$t_{h(SDA)}$	SDA data hold time	—	0(3)	3450	0	900	130	—	ns
$t_{r(SDA/SCL)}$	SDA and SCL rise time	—	—	1000	—	300	—	120	ns
$t_{f(SDA/SCL)}$	SDA and SCL fall time	—	—	300	—	300	4	120	ns
$t_{h(STA)}$	Start condition hold time	—	4.0	—	0.6	—	0.26	—	μs

(1). Guaranteed by design, not tested in production.

(2). To ensure the standard mode I2C frequency, f_{PCLK1} must be at least 2 MHz, To ensure the fast mode I2C frequency, f_{PCLK1} must be at least 4 MHz. To ensure the fast mode plus I2C frequency, f_{PCLK1} must be at least a multiple of 10 MHz.

(3). The device should provide a data hold time of 300 ns at least in order to bridge the undefined region of the falling edge of SCL.

4.19 SPI characteristics

Table 4-33. Standard SPI characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency	—	—	—	18	MHz
$t_{sck(H)}$	SCK clock high time	—	25	27	29	ns
$t_{sck\ (L)}$	SCK clock low time	—	25	27	29	ns
SPI master mode						
$t_{V(MO)}$	Data output valid time	—	—	—	2	ns
$t_{SU(MI)}$	Data input setup time	—	5	—	—	ns
$t_{H(MI)}$	Data input hold time	—	5	—	—	ns
SPI slave mode						
$t_{SU(NSS)}$	NSS enable setup time	f_{PCLK} = 72 MHz	$4T_{PCLK}$	—	—	ns
$t_{H(NSS)}$	NSS enable hold time	f_{PCLK} = 72 MHz	$2T_{PCLK}$	—	—	ns

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{A(SO)}$	Data output access time	f_{PCLK} = 72 MHz	2	—	55	ns
$t_{DIS(SO)}$	Data output disable time	—	3	—	10	ns
$t_{V(SO)}$	Data output valid time	—	—	—	29	ns
$t_{SU(SI)}$	Data input setup time	—	2	—	—	ns
$t_{H(SI)}$	Data input hold time	—	0	—	—	ns

(1). Based on characterization, not tested in production.

4.20 I2S characteristics

Table 4-34. I2S characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CK}	Clock frequency	Master mode (data: 16 bits, Audio frequency = 48 kHz)	—	—	6	MHz
		Slave mode	—	—	6	
t_H	Clock high time	f_{CK} = 6 MHz	—	—	83.33	ns
t_L	Clock low time		—	—	83.33	ns
$t_{V(WS)}$	WS valid time	Master mode	0	—	2	ns
$t_{H(WS)}$	WS hold time	Master mode	0	—	—	ns
$t_{SU(WS)}$	WS setup time	Slave mode	0	—	—	ns
$t_{H(WS)}$	WS hold time	Slave mode	0.5	—	—	ns
$Ducy_{(SCK)}$	I2S slave input clock duty cycle	Slave mode	30	—	70	%
$t_{SU(SD_MR)}$	Data input setup time	Master mode	2	—	—	ns
$t_{su(SD_SR)}$	Data input setup time	Slave mode	0	—	—	ns
$t_{H(SD_MR)}$	Data input hold time	Master receiver	1.5	—	—	ns
$t_{H(SD_SR)}$		Slave receiver	1.5	—	—	ns
$t_{v(SD_ST)}$	Data output valid time	Slave transmitter (after enable edge)	—	—	11	ns
$t_{h(SD_ST)}$	Data output hold time	Slave transmitter (after enable edge)	3	—	—	ns
$t_{v(SD_MT)}$	Data output valid time	Master transmitter (after enable edge)	—	—	11	ns
$t_{h(SD_MT)}$	Data output hold time	Master transmitter (after enable edge)	0	—	—	ns

(1). Based on characterization, not tested in production.

4.21 USART characteristics

Table 4-35. USART characteristics(1)

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency	f_{PCLKx} = 72 MHz	—	—	36	MHz
$t_{SCK(H)}$	SCK clock high time	f_{PCLKx} = 72 MHz	13.5	—	—	ns
$t_{SCK(L)}$	SCK clock low time	f_{PCLKx} = 72 MHz	13.5	—	—	ns

(1). Guaranteed by design, not tested in production.

4.22 TIMER characteristics

Table 4-36. TIMER characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
t_{res}	Timer resolution time	—	1	—	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 72 MHz	13.9	—	ns
f_{EXT}	Timer external clock frequency	—	0	$f_{TIMERxCLK}/2$	MHz
		$f_{TIMERxCLK}$ = 72 MHz	0	36	MHz
RES	Timer resolution	—	—	16/ 32	bit
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected	—	1	65536	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 72 MHz	0.0139	910	μs
t_{MAX_COUNT}	Maximum possible count	—	—	65536 × 65536	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 72 MHz	—	59.6	s

(1). Guaranteed by design, not tested in production.

4.23 WDGT characteristics

Table 4-37. FWDGT min/max timeout period at 40 kHz (IRC40K) (1)

Prescaler divider	PR[2:0] bits	Min timeout RLD[11:0] = 0x000	Max timeout RLD[11:0] = 0xFFF	Unit
1/4	000	0.1	409.6	ms
1/8	001	0.2	819.2	
1/16	010	0.4	1638.4	
1/32	011	0.8	3276.8	
1/64	100	1.6	6553.6	
1/128	101	3.2	13107.2	
1/256	110 or 111	6.4	26214.4	

(1). Guaranteed by design, not tested in production.

Table 4-38. WWDGT min-max timeout value at 72 MHz (f_{PCLK1}) (1)

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Prescaler divider	PSC[2:0]	Min timeout value CNT[6:0] = 0x40	Unit	Max timeout value CNT[6:0] = 0x7F	Unit
1/1	00	56.9	µs	3.64	ms
1/2	01	113.8		7.28	
1/4	10	227.6		14.56	
1/8	11	455.2		29.12	

(1). Guaranteed by design, not tested in production.

4.24 Parameter conditions

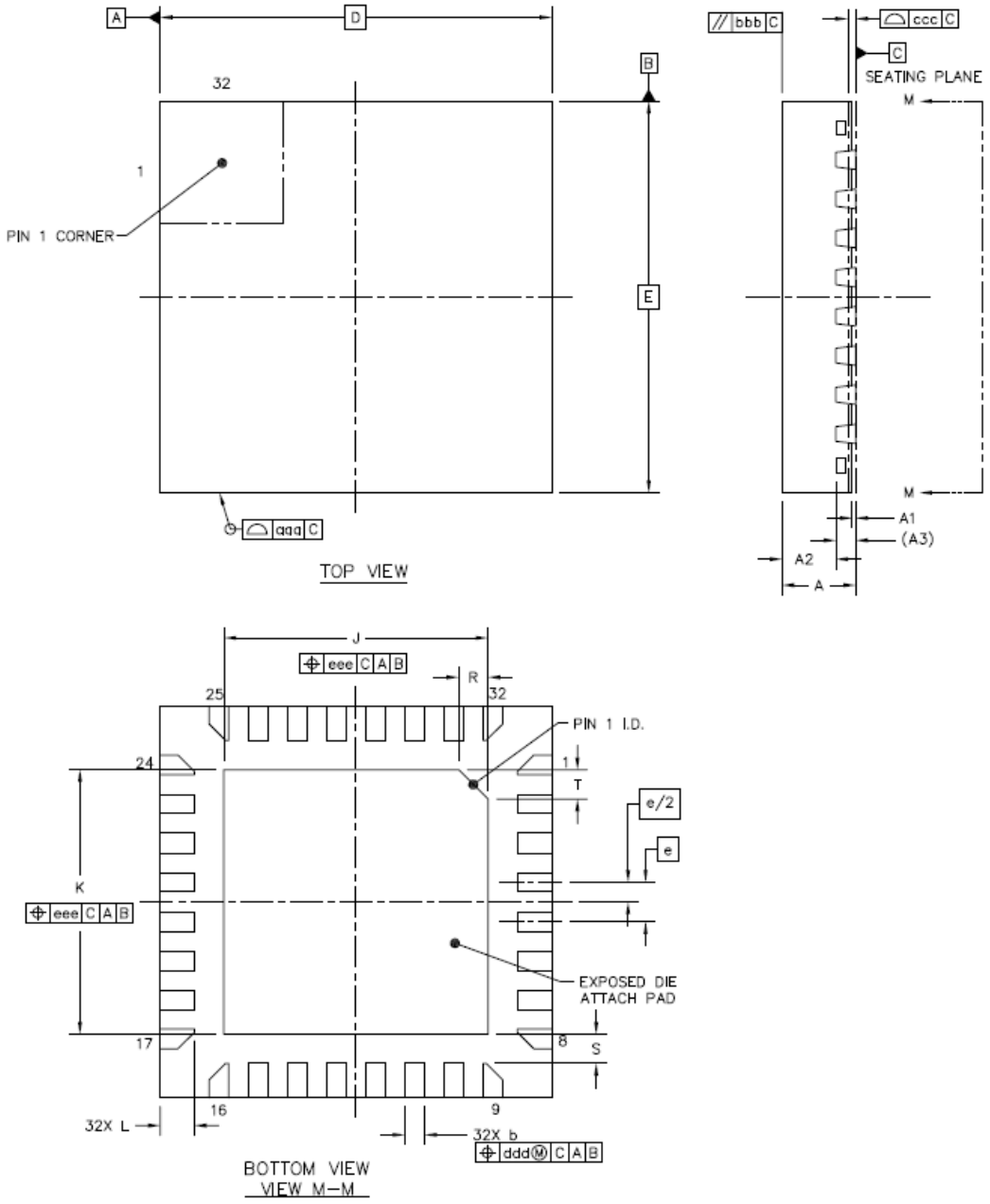
Unless otherwise specified, all values given for V_{DD} = V_{DDA} = 3.3 V, T_A = 25 ℃.

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5 Package information

5.1 QFN32 package outline dimensions

Figure 5-1. QFN32 package outline



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Table 5-1. QFN32 package dimensions

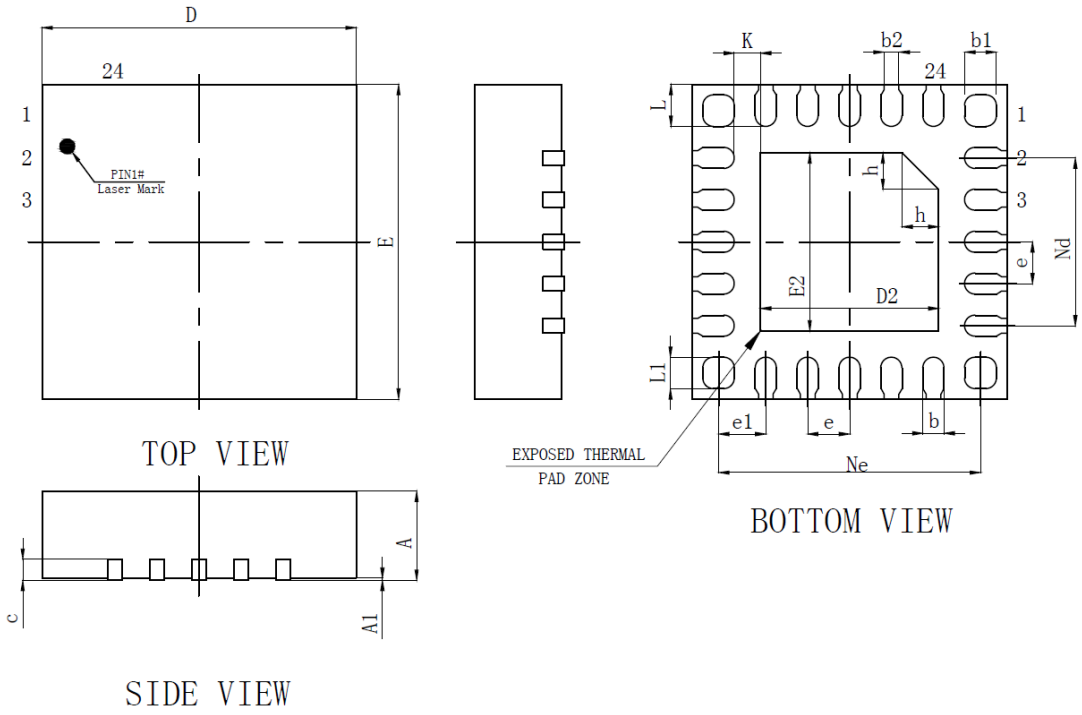
Symbol	Min	Typ	Max
A	0.70	0.75	0.80
A1	0	0.035	0.05
A2	—	0.55	—
A3	0.203 REF		
D	4.00 BSC		
E	4.00 BSC		
J	2.60	2.70	2.80
K	2.60	2.70	2.80
L	0.30	0.35	0.40
e	0.40 BCS		
b	0.15	0.20	0.25
aaa	0.10		
bbb	0.10		
ccc	0.08		
ddd	0.10		
eee	0.10		
S	0.30 REF		
R	0.30 REF		
T	0.30 REF		

(Original dimensions are in millimeters)

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5.2 QFN24 package outline dimensions

Figure 5-2. QFN24 package outline



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Table 5-2. QFN24 package dimensions

Symbol	Min	Typ	Max
A	0.80	0.85	0.90
A1	0	0.02	0.05
b	0.15	0.20	0.25
b1	0.25	0.30	0.35
b2	0.14 REF		
c	0.18	0.20	0.25
D	2.90	3.00	3.10
D2	1.60	1.70	1.80
Ne	2.50 BSC		
Nd	1.60 BSC		
e	0.40 BSC		
e1	0.45 BSC		
E	2.90	3.00	3.10
E2	1.60	1.70	1.80
L	0.35	0.40	0.45
L1	0.25	0.30	0.35
h	0.30	0.35	0.40
K	0.20	0.25	0.30

(Original dimensions are in millimeters)

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6 Ordering information

Table 6-1. Part ordering code for GD32E232xx devices

Ordering code	Flash (KB)	Package	Package type	Temperature operating range
GD32E232E4U7	16	QFN24	Green	Industrial -40 °C to +105 °C
GD32E232E6U7	32	QFN24	Green	Industrial -40 °C to +105 °C
GD32E232E8U7	64	QFN24	Green	Industrial -40 °C to +105 °C
GD32E232K4Q7	16	QFN32	Green	Industrial -40 °C to +105 °C
GD32E232K6Q7	32	QFN32	Green	Industrial -40 °C to +105 °C
GD32E232K8Q7	64	QFN32	Green	Industrial -40 °C to +105 °C

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7 Revision history

Table 7-1. Revision history

Revision No.	Description	Date
1.0	Initial Release	Sept.18, 2019
1.1	Add information about GD32E232Ex and GD32E232Kx.	Oct.22, 2019
1.2	Add information about CLA and update GD32E232Ex QFN24 pinouts.	Dec.19, 2019
1.3	Add boot mode pins for GD32E232Ex in chapter3.4 and modify the number of ADC external channels in Table 7-2.	Jan.2, 2020
1.4	Update the number of I2C and USART.	Mar.10, 2020

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