GigaDevice Semiconductor Inc.

GD32C211xx
Arm® Cortex®-M23 32-bit MCU

For Internal Use

Datasheet

Revision 0.0

(May 2025)

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com
微信扫码咨询客服

Table of Contents

Table of Contents 1
List of Figures 4
List of Tables 5
1. General description 7
2. Device overview 8
2.1. Device information 8
2.2. Block diagram 9
2.3. Pinouts and pin assignment 10
2.4. Memory map 12
2.5. Clock tree 15
2.6. Pin definitions 16
2.6.1. GD32C211Ex QFN24 pin definitions 16
2.6.2. GD32C211Ex TSSOP24 pin definitions 19
2.6.3. GD32C211Fx QFN20 pin definitions 22
2.6.4. GD32C211Fx TSSOP20 definitions 25
2.6.5. GD32C211Jx SOP8 pin definitions 28
2.6.6. GD32C211xx pin alternate functions 30
3. Functional description 32
3.1. Arm® Cortex®-M23 core 32
3.2. Embedded memory 32
3.3. Clock, reset and supply management 33
3.4. Boot modes 33
3.5. Power saving modes 33
3.6. General-purpose inputs/outputs (GPIOs) 35
3.7. CRC calculation unit (CRC) 35
3.8. Direct memory access controller (DMA) 35
3.9. DMA request multiplexer (DMAMUX) 36
3.10. Analog to digital converter (ADC) 36
3.11. Real time clock (RTC) 37
3.12. Timers and PWM generation 37
3.13. Universal synchronous/asynchronous receiver transmitter (USART/UART)

Preliminary version
Confidential, under NDA for engineering evaluation only

For Internal Use

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

38
3.14. Inter-integrated circuit (I2C) 38
3.15. Serial peripheral interface (SPI) 39
3.16. Debug mode 39
3.17. Package and operation temperature 39
4 Electrical characteristics 41
4.1. Parameter introduction 41
4.2. Absolute maximum ratings 42
4.3. General operating conditions 43
4.4. Power supply requirement characteristics 44
4.5. Start-up timings of Operating conditions 44
4.6. Wake-up times from power saving modes 44
4.7. Power consumption 45
4.8. EMC characteristics 55
4.9. Power supply supervisor characteristics 56
4.10. External clock characteristics 57
4.11. Internal clock characteristics 60
4.12. Memory characteristics 61
4.13. NRST pin characteristics 61
4.14. GPIO current injection characteristics 62
4.15. GPIO characteristics 63
4.16. Internal reference voltage characteristics 64
4.17. ADC characteristics 65
4.18. TIMER characteristics 68
4.19. I2C characteristics 69
4.20. SPI characteristics 69
4.21. USART characteristics 71
4.22. WDGT characteristics 72
4.23. SWD Timing 73
5 Package information 74
5.1 QFN24 package outline dimensions 74
5.2 TSSOP24 package outline dimensions 76

For Internal Use

Preliminary version
Confidential, under NDA for engineering evaluation only

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

5.3 QFN20 package outline dimensions 78
5.4 TSSOP20 package outline dimensions 80
5.5 SOP8 package outline dimensions 82
5.6 Thermal characteristics 84
6 Ordering information 86
7 Revision history 87

For Internal Use

Preliminary version
Confidential, under NDA for engineering evaluation only

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

List of Figures

Figure 2-1. GD32C211xx block diagram 9
Figure 2-2. GD32C211Ex QFN24 pinouts 10
Figure 2-3. GD32C211Ex TSSOP24 pinouts 10
Figure 2-4. GD32C211Fx QFN20 pinouts 11
Figure 2-5. GD32C211Fx TSSOP20 pinouts 11
Figure 2-6. GD32C211Jx TSSOP8 pinouts 11
Figure 2-7. GD32C211xx clock tree 15
Figure 4-1. Recommended power supply decoupling capacitors (1) 43
Figure 4-2. Rise and fall gradient and ripple frequency characteristics 44
Figure 4-3. Power consumption measurement diagram 46
Figure 4-4. Recommended external clock 57
Figure 4-5. Internal structure diagram of OSC32IN and OSC32OUT pin 57
Figure 4-6. Recommended external OSC32IN and OSC32OUT pins circuit for crystal 59
Figure 4-7. Recommended external OSC32IN and OSC32OUT pins circuit for oscillator 59
Figure 4-8. Recommended external NRST pin circuit (1) 62
Figure 4-9. Differential linearity error 67
Figure 4-10. Integral linearity error 68
Figure 4-11. I2C bus timing diagram 69
Figure 4-12. SPI timing diagram - master mode 70
Figure 4-13. SPI timing diagram - slave mode (CKPH=0) 71
Figure 4-14. SPI timing diagram - slave mode (CKPH=1) 71
Figure 4-15. SWD SWCLK Timings 73
Figure 5-1. QFN24 package outline 74
Figure 5-2. QFN24 recommended footprint 75
Figure 5-3. TSSOP24 package outline 76
Figure 5-4. TSSOP24 recommended footprint 77
Figure 5-5. QFN20 package outline 78
Figure 5-6. QFN20 recommended footprint 79
Figure 5-7. TSSOP20 package outline 80
Figure 5-8. TSSOP20 recommended footprint 81
Figure 5-9. SOP8 package outline 82
Figure 5-10. SOP8 recommended footprint 83

For Internal Use

Preliminary version
Confidential, under NDA for engineering evaluation only

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

List of Tables

Table 2-1. GD32C211xx devices features and peripheral list 8
Table 2-2. GD32C211xx memory map 12
Table 2-3. GD32C211Ex QFN24 pin definitions 16
Table 2-4. GD32C211Ex TSSOP24 pin definitions 19
Table 2-5. GD32C211Fx QFN20 pin definitions 22
Table 2-6. GD32C211Fx TSSOP20 pin definitions 25
Table 2-7. GD32C211Jx SOP8 pin definitions 28
Table 2-8. Port A alternate functions summary 30
Table 2-9. Port B alternate functions summary 31
Table 2-10. Port C alternate functions summary 31
Table 4-1. Abbreviations 41
Table 4-2. Absolute maximum ratings (1) 42
Table 4-3. General operating conditions (1) 43
Table 4-4. Power supply requirement characteristics(1) 44
Table 4-5. Start-up timings of Operating conditions (1)(2) 44
Table 4-6. Wake-up times from power saving modes (1)(2) 44
Table 4-7. Power consumption in Run mode and 1 Run mode (1)(2)(3) 47
Table 4-8. Power consumption in Run mode with different codes(1)(2)(3) 48
Table 4-9. Power consumption in Sleep mode and Sleep 1 mode(1)(2) 49
Table 4-10. Power consumption in Deep-sleep mode(1)(2) 50
Table 4-11. Power consumption in Deep-sleep 1 mode(1)(2) 52
Table 4-12. Peripheral current consumption characteristics(1) 54
Table 4-13. System level ESD and EFT characteristics (1) 55
Table 4-14. EMI characteristics (1) 55
Table 4-15. Power supply supervisor characteristics (1) 56
Table 4-16. External clock characteristics (1) 57
Table 4-17. Low speed external clock (LXTAL) generated from a crystal/ceramic characteristics(1) 58
Table 4-18. Low speed external user clock characteristics (LXTAL in bypass mode) (1) 58
Table 4-19. High speed internal clock (IRC48M) characteristics 60
Table 4-20. Low speed internal clock (IRC32K) characteristics 60
Table 4-21. Flash memory characteristics (1) 61
Table 4-22. NRST pin characteristics (1) 61
Table 4-23. GPIO current injection susceptibility 62
Table 4-24. I/O static characteristics 63
Table 4-25. Output voltage characteristics for all I/Os (1) 63
Table 4-26. I/O port AC characteristics (1)(2)(3)(4) 64
Table 4-27. Internal reference voltage characteristics(1) 64
Table 4-28. Internal reference voltage calibration values 65
Table 4-29. ADC characteristics (1) 65

Preliminary version
Confidential, under NDA for engineering evaluation only

For Internal Use

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

Table 4-30. ADC RAIN max for f_{ADC} = 16 MHz (1)(2) 66
Table 4-31. ADC accuracy at f_{ADC} = 16 MHz (1)(2)(3) 67
Table 4-32. TIMER characteristics (1) 68
Table 4-33. I2C characteristics (1)(2) 69
Table 4-34. Standard SPI characteristics (1) 69
Table 4-35. USART characteristics in Synchronous mode (1) 71
Table 4-36. FWDGT min/max timeout period at 32 kHz (IRC32K) (1) 72
Table 4-37. WWDGT min-max timeout value at 48 MHz (f_{PCLK}) (1) 72
Table 4-38. SWD Interface Timing (1) 73
Table 5-1. QFN24 package dimensions 74
Table 5-2. TSSOP24 package dimensions 76
Table 5-3. QFN20 package dimensions 78
Table 5-4. TSSOP20 package dimensions 80
Table 5-5. SOP8 package dimensions 82
Table 5-6. Package thermal characteristics(1) 84
Table 6-1. Part ordering code for GD32C221xx devices 86
Table 7-1. Revision history 87

For Internal Use

Preliminary version
Confidential, under NDA for engineering evaluation only

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

1. General description

The GD32C211xx device belongs to the value line of GD32 MCU family. It is a new 32-bit general-purpose microcontroller based on the Arm® Cortex®-M23 core. The Cortex-M23 processor is an energy-efficient processor with a very low gate count. It is intended to be used for microcontroller and deeply embedded applications that require an area-optimized processor. The processor delivers high energy efficiency through a small but powerful instruction set and extensively optimized design, providing high-end processing hardware including a single-cycle multiplier and a 17-cycle divider.

The GD32C211xx device incorporates the Arm® Cortex®-M23 32-bit processor core operating at up to 48 MHz frequency with Flash accesses 0~1 wait states to obtain maximum efficiency. It provides up to 32 KB embedded main Flash memory, 2 KB data flash and up to 6 KB SRAM memory. An extensive range of enhanced I/Os and peripherals connected to one APB bus. The devices offer one 12-bit ADC, up to four general 16-bit timers, one 16-bit PWM advanced timer, as well as standard and advanced communication interfaces: one SPI, one I2C and three USARTs.

The device operates from a 2.3 to 5.5 V power supply and available in –40 to +85 °C temperature range. Several power saving modes provide the flexibility for maximum optimization between wakeup latency and power consumption, an especially important consideration in low power applications.

The above features make the GD32C211xx devices suitable for a wide range of applications, especially in areas such as industrial control, motor drives, user interface, power monitor and alarm systems, consumer and handheld equipment, gaming and GPS, E-bike and so on.

For Internal Use

Preliminary version
Confidential, under NDA for engineering evaluation only

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

2. Device overview

2.1. Device information

Table 2-1. GD32C211xx devices features and peripheral list

Part Number		GD32C211xx									
		E4U6TR	E6U6TR	E4P6TR	E6P6TR	F4U6TR	F6U6TR	F4P6TR	F6P6TR	J4M6TR	J6M6TR
Main FLASH (KB)		16	32	16	32	16	32	16	32	16	32
Data FLASH (KB)		2	2	2	2	2	2	2	2	2	2
SRAM (KB)		6	6	6	6	6	6	6	6	6	6
Timers	General timer(16-bit)	4 (2, 13, 15,16)	4 (2, 13, 15,16)	4 (2, 13, 15,16)	4 (2, 13, 15,16)	4 (2, 13, 15,16)	4 (2, 13, 15,16)	4 (2, 13, 15,16)	4 (2, 13, 15,16)	4 (2, 13, 15,16)	4 (2, 13, 15,16)
	SysTick	1	1	1	1	1	1	1	1	1	1
	Advanced timer(16-bit)	1 (0)	1 (0)	1 (0)	1 (0)	1 (0)	1 (0)	1 (0)	1 (0)	1 (0)	1 (0)
	Watchdog	2	2	2	2	2	2	2	2	2	2
	RTC	1	1	1	1	1	1	1	1	1	1
Connectivity	USART	3 (0, 1, 2)	3 (0, 1, 2)	3 (0, 1, 2)	3 (0, 1, 2)	3 (0, 1, 2)	3 (0, 1, 2)	3 (0, 1, 2)	3 (0, 1, 2)	2 (0, 1)	2 (0, 1)
	I2C	1	1	1	1	1	1	1	1	1	1
	SPI	1	1	1	1	1	1	1	1	1	1
GPIO		22	22	22	22	18	18	18	18	6	6
ADC	Units	1	1	1	1	1	1	1	1	1	1
	Channels (External)	9	9	9	9	9	9	9	9	2	2
	Channels (Internal)	1	1	1	1	1	1	1	1	1	1
Package		QFN24		TSSOP24		QFN20		TSSOP20		SOP8	

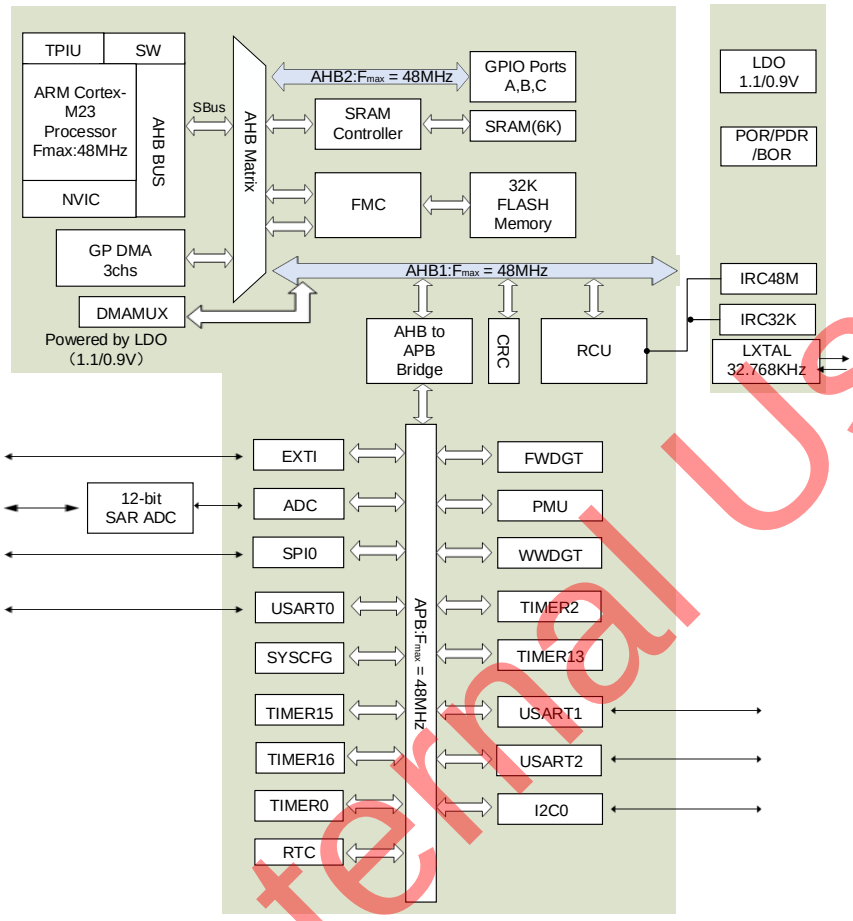
For Internal Use

Preliminary version
Confidential, under NDA for engineering evaluation only

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

2.2. Block diagram

Figure 2-1. GD32C211xx block diagram



For Internal Use

Preliminary version
Confidential, under NDA for engineering evaluation only

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

2.3. Pinouts and pin assignment

Figure 2-2. GD32C211Ex QFN24 pinouts

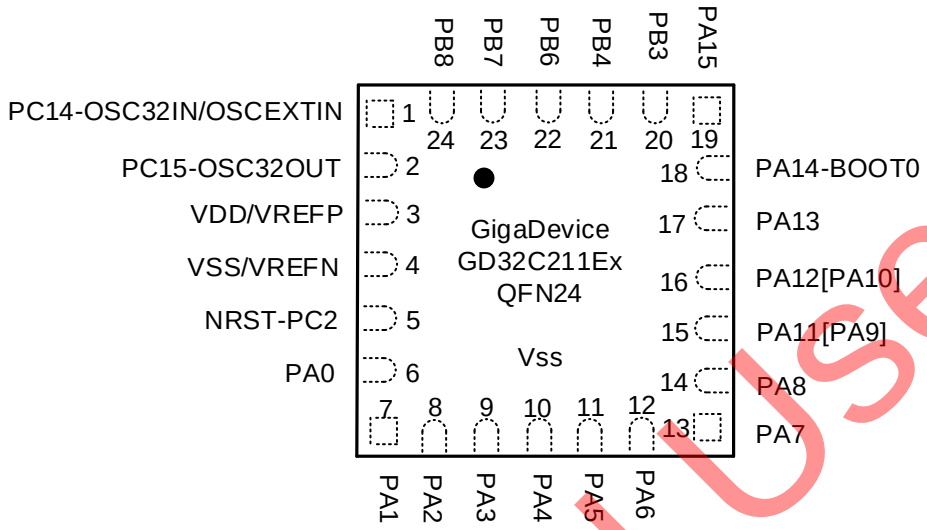
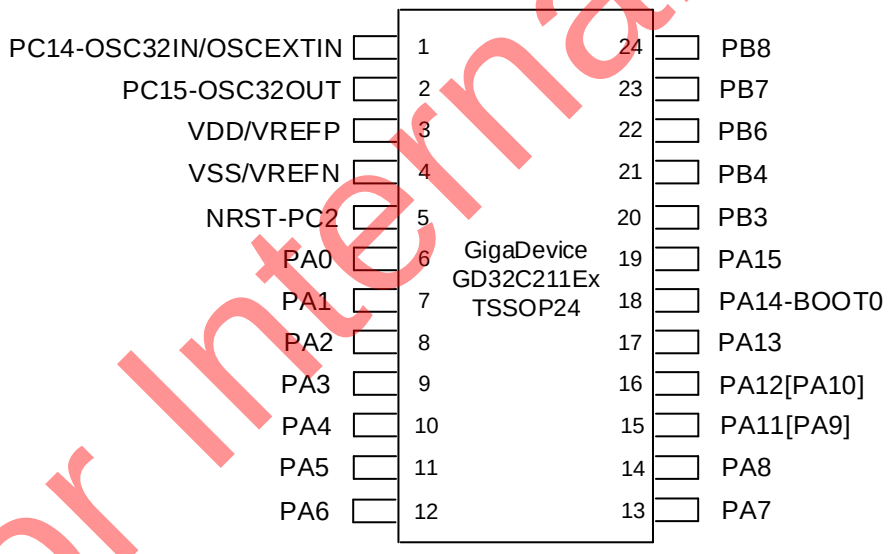


Figure 2-3. GD32C211Ex TSSOP24 pinouts



For Internal Use

Preliminary version
Confidential, under NDA for engineering evaluation only

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

Figure 2-4. GD32C211Fx QFN20 pinouts

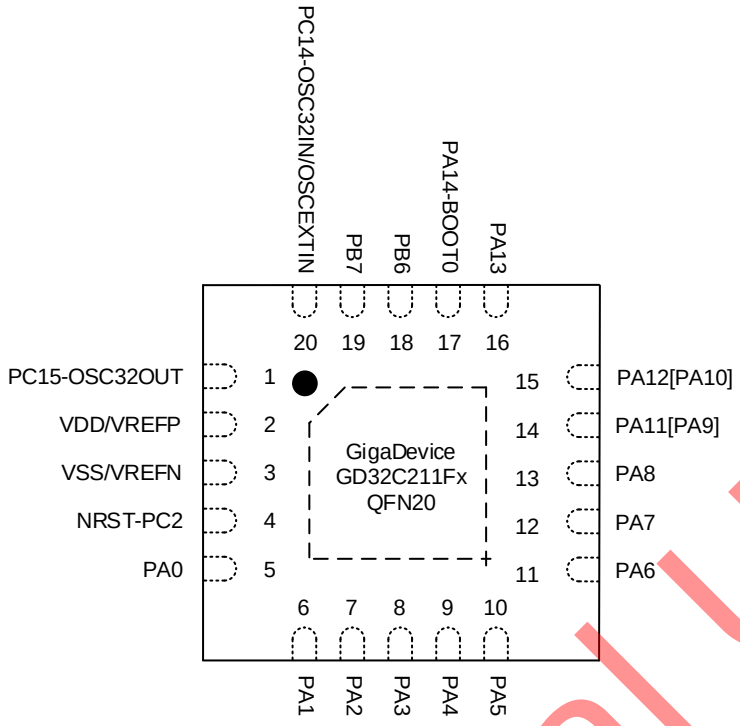


Figure 2-5. GD32C211Fx TSSOP20 pinouts

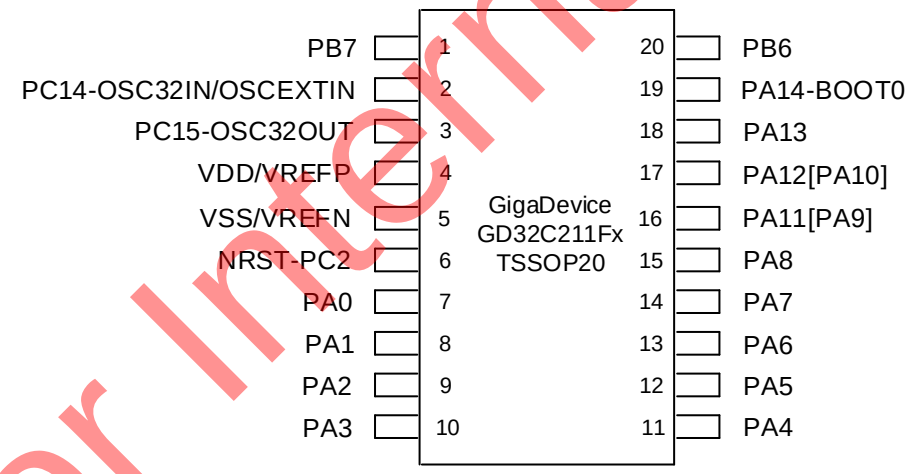
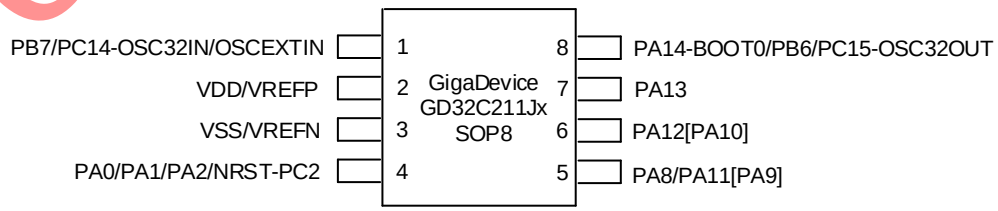


Figure 2-6. GD32C211Jx TSSOP8 pinouts



For Internal Use

Preliminary version
Confidential, under NDA for engineering evaluation only

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

2.4. Memory map

Table 2-2. GD32C211xx memory map

Pre-defined Regions	Bus	ADDRESS	Peripherals
		0xE000 0000 - 0xE00F FFFF	Cortex M23 internal peripherals
External Device		0xA000 0000 - 0xDFFF FFFF	Reserved
External RAM		0x60000000 - 0x9FFFFFFF	Reserved
Peripherals	AHB2	0x5004 0000 - 0x5FFF FFFF	Reserved
		0x5000 0000 - 0x5003 FFFF	Reserved
		0x4800 1800 - 0x4FFF FFFF	Reserved
		0x4800 1400 - 0x4800 17FF	Reserved
		0x4800 1000 - 0x4800 13FF	Reserved
		0x4800 0C00 - 0x4800 0FFF	Reserved
		0x4800 0800 - 0x4800 0BFF	GPIOC
		0x4800 0400 - 0x4800 07FF	GPIOB
		0x4800 0000 - 0x4800 03FF	GPIOA
	AHB1	0x4003 8400 - 0x47FF FFFF	Reserved
		0x4003 8000 - 0x4003 83FF	Reserved
		0x4002 4000 - 0x4003 7FFF	Reserved
		0x4002 3400 - 0x4002 3FFF	Reserved
		0x4002 3000 - 0x4002 33FF	CRC
		0x4002 2400 - 0x4002 2FFF	Reserved
		0x4002 2000 - 0x4002 23FF	FMC
		0x4002 1400 - 0x4002 1FFF	Reserved
		0x4002 1000 - 0x4002 13FF	RCU
		0x4002 0C00 - 0x4002 0FFF	Reserved
		0x4002 0800 - 0x4002 0BFF	DMAMUX
		0x4002 0400 - 0x4002 07FF	Reserved
		0x4002 0000 - 0x4002 03FF	DMA
	APB	0x4001 8000 - 0x4001 FFFF	Reserved
		0x4001 7C00 - 0x4001 7FFF	Reserved
		0x4001 7800 - 0x4001 7BFF	Reserved
		0x4001 7400 - 0x4001 77FF	Reserved
		0x4001 7000 - 0x4001 73FF	Reserved
		0x4001 6C00 - 0x4001 6FFF	Reserved
		0x4001 6800 - 0x4001 6BFF	Reserved
		0x4001 5C00 - 0x4001 67FF	Reserved
		0x4001 5800 - 0x4001 5BFF	DBG
		0x4001 5400 - 0x4001 57FF	Reserved
		0x4001 5000 - 0x4001 53FF	Reserved

For Internal Use

Preliminary version
Confidential, under NDA for engineering evaluation only

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

Pre-defined Regions	Bus	ADDRESS	Peripherals
		0x4001 4C00 - 0x4001 4FFF	Reserved
		0x4001 4800 - 0x4001 4BFF	TIMER16
		0x4001 4400 - 0x4001 47FF	TIMER15
		0x4001 3C00 - 0x4001 43FF	Reserved
		0x4001 3800 - 0x4001 3BFF	USART0
		0x4001 3400 - 0x4001 37FF	Reserved
		0x4001 3000 - 0x4001 33FF	SPI0
		0x4001 2C00 - 0x4001 2FFF	TIMER0
		0x4001 2800 - 0x4001 2BFF	Reserved
		0x4001 2400 - 0x4001 27FF	ADC
		0x4001 2000 - 0x4001 23FF	Reserved
		0x4001 1C00 - 0x4001 1FFF	Reserved
		0x4001 1800 - 0x4001 1BFF	Reserved
		0x4001 1400 - 0x4001 17FF	Reserved
		0x4001 1000 - 0x4001 13FF	Reserved
		0x4001 0C00 - 0x4001 0FFF	Reserved
		0x4001 0800 - 0x4001 23FF	Reserved
		0x4001 0400 - 0x4001 07FF	EXTI
		0x4001 0000 - 0x4001 03FF	SYSCFG
		0x4000 C000 - 0x4000 FFFF	Reserved
		0x4000 7400 - 0x4000 BFFF	Reserved
		0x4000 7000 - 0x4000 73FF	PMU
		0x4000 5C00 - 0x4000 6FFF	Reserved
		0x4000 5800 - 0x4000 5BFF	Reserved
		0x4000 5400 - 0x4000 57FF	I2C0
		0x4000 4C00 - 0x4000 53FF	Reserved
		0x4000 4800 - 0x4000 4BFF	USART2
		0x4000 4400 - 0x4000 47FF	USART1
		0x4000 3C00 - 0x4000 43FF	Reserved
		0x4000 3800 - 0x4000 3BFF	Reserved
		0x4000 3400 - 0x4000 37FF	Reserved
		0x4000 3000 - 0x4000 33FF	FWDGT
		0x4000 2C00 - 0x4000 2FFF	WWDGT
		0x4000 2800 - 0x4000 2BFF	RTC
		0x4000 2400 - 0x4000 27FF	Reserved
		0x4000 2000 - 0x4000 23FF	TIMER13
		0x4000 0800 - 0x4000 1FFF	Reserved
		0x4000 0400 - 0x4000 07FF	TIMER2
		0x4000 0000 - 0x4000 03FF	Reserved
SRAM		0x2000 1800 - 0x3FFF FFFF	Reserved

For Internal Use

Preliminary version
Confidential, under NDA for engineering evaluation only

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

Pre-defined Regions	Bus	ADDRESS	Peripherals
		0x2000 0000 - 0x2000 17FF	SRAM(6KB)
Code		0x1FFF 7880 - 0x1FFF FFFF	Reserved
		0x1FFF 7800 - 0x1FFF 787F	Option bytes(128B)
		0x1FFF 7200 - 0x1FFF 77FF	Reserved
		0x1FFF 7000 - 0x1FFF 71FF	OTP bytes(512B)
		0x1FFF 0C00 - 0x1FFF 6FFF	Reserved
		0x1FFE F000 - 0x1FFF 0BFF	System memory(7KB)
		0x0880 0800 - 0x1FFE EFFF	Reserved
		0x0880 0000 - 0x0880 07FF	Data Flash(2KB)
		0x0800 8000 - 0x087F FFFF	Reserved
		0x0800 0000 - 0x0800 7FFF	Flash memory(32KB)
		0x0000 0000 - 0x07FF FFFF	Aliased to Flash or system memory

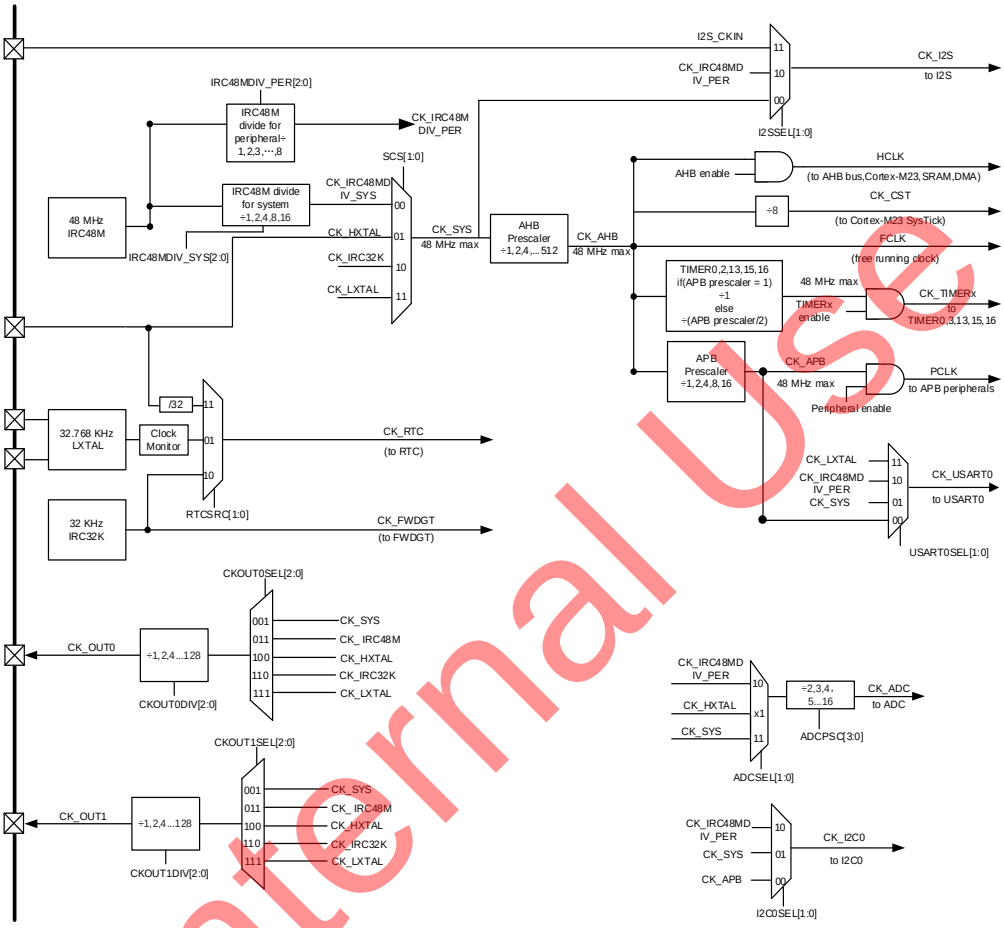
For Internal Use

Preliminary version
Confidential, under NDA for engineering evaluation only

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

2.5. Clock tree

Figure 2-7. GD32C211xx clock tree



Legend:

HXTAL: High speed crystal oscillator

LXTAL: Low speed crystal oscillator

IRC48M: Internal 48M RC oscillator

IRC32K: Internal 32K RC oscillator

For Internal Use

Preliminary version
Confidential, under NDA for engineering evaluation only

2.6. Pin definitions

2.6.1. GD32C211Ex QFN24 pin definitions

Table 2-3. GD32C211Ex QFN24 pin definitions

GD32C211Ex QFN24				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PC14-OSC32IN/OSCEXTIN	1	I/O	5VT	Default: PC14 Alternate: USART0_TX, TIMER0_ETI, TIMER0_BRKIN1, USART1_RTS_DE_CK, TIMER16_CH0, TIMER2_CH1, EVENTOUT Additional: OSC32IN, OSCEXTIN
PC15-OSC32OUT	2	I/O	5VT	Default: PC15 Alternate: OSC32EN, OSCEN, TIMER0_ETI, TIMER2_CH2 Additional: OSC32OUT
VDD/VREFP	3	P	-	Default: VDD/VREFP
VSS/VREFN	4	P	-	Default: VSS/VREFN
NRST-PC2	5	I/O	5VT	Default: NRST Alternate: CK_OUT0, TIMER0_CH3 Additional: PC2(3)
PA0	6	I/O	5VT	Default: PA0 Alternate: USART1_CTS, TIMER15_CH0, USART0_TX, TIMER0_CH0 Additional: ADC_IN0
PA1	7	I/O	5VT	Default: PA1 Alternate: SPI0_SCK, USART1_RTS_DE_CK, TIMER16_CH0, USART0_RX, TIMER0_CH1, I2C0_SMBA, EVENTOUT Additional: ADC_IN1
PA2	8	I/O	5VT	Default: PA2 Alternate: SPI0_MOSI, USART1_TX, TIMER15_CH0_ON, TIMER2_ETI, TIMER0_CH2, USART2_TX Additional: ADC_IN2
PA3	9	I/O		Default: PA3 Alternate: USART1_RX, TIMER0_CH0_ON, TIMER0_CH3, EVENTOUT, USART2_RX Additional: ADC_IN3
PA4	10	I/O		Default: PA4 Alternate: SPI0_NSS, USART1_TX, TIMER0_CH1_ON, TIMER13_CH0, TIMER16_CH0_ON, EVENTOUT Additional: ADC_IN4, RTC_OUT0
PA5	11	I/O		Default: PA5 Alternate: SPI0_SCK, USART1_RX, TIMER0_CH2_

For Internal Use

Preliminary version
Confidential, under NDA for engineering evaluation only

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

GD32C211Ex QFN24				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				ON, TIMER0_CH0, EVENTOUT Additional: ADC_IN5
PA6	12	I/O		Default: PA6 Alternate: SPI0_MISO, TIMER2_CH0, TIMER0_BRKIN0, TIMER15_CH0, USART2_CTS Additional: ADC_IN6
PA7	13	I/O	5VT	Default: PA7 Alternate: SPI0_MOSI, TIMER2_CH1, TIMER0_CH0_ON, TIMER13_CH0, TIMER16_CH0, USART2_RTS_DE_CK Additional: ADC_IN7
PA8	14	I/O	5VT	Default: PA8 Alternate: CK_OUT0, USART1_TX, TIMER0_CH0, EVENTOUT, SPI0_NSS, TIMER0_CH1_ON, TIMER0_CH2_ON, TIMER2_CH2, TIMER2_CH3, TIMER13_CH0, USART0_RX, CK_OUT1
PA11[PA9](4)	15	I/O	5VT	Default: PA11 Alternate: SPI0_MISO, USART0_CTS, TIMER0_CH3, TIMER0_BRKIN1
				Remap: PA9 Alternate: CK_OUT0, USART0_TX, TIMER0_CH1, TIMER2_ETI, I2C0_SCL, EVENTOUT
PA12[PA10](4)	16	I/O	5VT	Default: PA12 Alternate: SPI0_MOSI, USART0_RTS_DE_CK, TIMER0_ETI Additional: ADC_IN8
				Remap: PA10 Alternate: USART0_RX, TIMER0_CH2, CK_OUT1, TIMER16_BRKIN0, I2C0_SDA, EVENTOUT
PA13	17	I/O		Default: PA13, SWDIO Alternate: SWDIO, TIMER2_ETI, USART1_RX, EVENTOUT
PA14-BOOT0	18	I/O	5VT	Default: PA14, SWCLK Alternate: SWCLK, USART1_TX, EVENTOUT, SPI0_NSS, USART1_RX, TIMER0_CH0, CK_OUT1, USART0_RTS_DE_CK Additional: BOOT0
PA15	19	I/O		Default: PA15 Alternate: SPI0_NSS, USART1_RX, TIMER0_CH0, CK_OUT1, USART0_RTS_DE_CK, EVENTOUT
PB3	20	I/O		Default: PB3 Alternate: SPI0_SCK, TIMER0_CH1, TIMER2_CH1, USART0_RTS_DE_CK, EVENTOUT
PB4	21	I/O		Default: PB4

For Internal Use

Preliminary version
Confidential, under NDA for engineering evaluation only

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

GD32C211Ex QFN24				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Alternate: SPI0_MISO, TIMER2_CH0, USART0_CTS, TIMER16_BRKIN0, EVENTOUT
PB6	22	I/O	5VT	Default: PB6 Alternate: USART0_TX, TIMER0_CH2, TIMER15_CH0_ON, TIMER2_CH2, USART0_RTS_DE_CK, USART0_CTS, I2C0_SCL, I2C0_SMBA, SPI0_MOSI, SPI0_MISO, SPI0_SCK, TIMER0_CH1, TIMER2_CH0, TIMER2_CH1, TIMER15_BRKIN0, TIMER16_BRKIN0
PB7	23	I/O	5VT	Default: PB7 Alternate: USART0_RX, TIMER0_CH3, TIMER16_CH0_ON, TIMER2_CH3, I2C0_SDA, EVENTOUT, USART1_CTS, TIMER15_CH0, TIMER2_CH0, I2C0_SCL
PB8	24	I/O	5VT	Default: PB8 Alternate: USART1_CTS, TIMER15_CH0, TIMER2_CH0, I2C0_SCL, EVENTOUT

Note:

(1) Type: I = input, O = output, A = analog, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

(3) Refer to the description of the NRST_MDSEL[1:0] field in FMC_OBCTL register of GD32C2x1_User_Manual to configure the NRST-PC2 pin as a PC2 general GPIO function.

(4) Refer to the description of the PA12_RMP or PA11_RMP field in SYSCFG_CFG0 register of GD32C2x1_User_Manual.

For Internal Use

Preliminary version
Confidential, under NDA for engineering evaluation only

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

2.6.2. GD32C211Ex TSSOP24 pin definitions

Table 2-4. GD32C211Ex TSSOP24 pin definitions

GD32C211Ex TSSOP24				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PC14-OSC32IN/OSCEXTIN	1	I/O	5VT	Default: PC14 Alternate: USART0_TX, TIMER0_ETI, TIMER0_BRKIN1, USART1_RTS_DE_CK, TIMER16_CH0, TIMER2_CH1, EVENTOUT Additional: OSC32IN
PC15-OSC32OUT	2	I/O	5VT	Default: PC15 Alternate: OSC32EN, OSCEN, TIMER0_ETI, TIMER2_CH2 Additional: OSC32OUT
VDD/VREFP	3	P	-	Default: VDD/VREFP
VSS/VREFN	4	P	-	Default: VSS/VREFN
NRST-PC2	5	I/O	5VT	Default: NRST Alternate: CK_OUT0, TIMER0_CH3 Additional: PC2(3)
PA0	6	I/O	5VT	Default: PA0 Alternate: USART1_CTS, TIMER15_CH0, USART0_TX, TIMER0_CH0 Additional: ADC_IN0
PA1	7	I/O	5VT	Default: PA1 Alternate: SPI0_SCK, USART1_RTS_DE_CK, TIMER16_CH0, USART0_RX, TIMER0_CH1, I2C0_SMBA, EVENTOUT Additional: ADC_IN1
PA2	8	I/O	5VT	Default: PA2 Alternate: SPI0_MOSI, USART1_TX, TIMER15_CH0_ON, TIMER2_ETI, TIMER0_CH2, USART2_TX Additional: ADC_IN2
PA3	9	I/O		Default: PA3 Alternate: USART1_RX, TIMER0_CH0_ON, TIMER0_CH3, EVENTOUT, USART2_RX Additional: ADC_IN3
PA4	10	I/O		Default: PA4 Alternate: SPI0_NSS, USART1_TX, TIMER0_CH1_ON, TIMER13_CH0, TIMER16_CH0_ON, EVENTOUT Additional: ADC_IN4, RTC_OUT0
PA5	11	I/O		Default: PA5 Alternate: SPI0_SCK, USART1_RX, TIMER0_CH2_ON, TIMER0_CH0, EVENTOUT Additional: ADC_IN5
PA6	12	I/O		Default: PA6

For Internal Use

Preliminary version
Confidential, under NDA for engineering evaluation only

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

GD32C211Ex TSSOP24				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Alternate: SPI0_MISO, TIMER2_CH0, TIMER0_BRKIN0, TIMER15_CH0, USART2_CTS Additional: ADC_IN6
PA7	13	I/O	5VT	Default: PA7 Alternate: SPI0_MOSI, TIMER2_CH1, TIMER0_CH0_ON, TIMER13_CH0, TIMER16_CH0, USART2_RTS_DE_CK Additional: ADC_IN7
PA8	14	I/O	5VT	Default: PA8 Alternate: CK_OUT0, USART1_TX, TIMER0_CH0, EVENTOUT, SPI0_NSS, TIMER0_CH1_ON, TIMER0_CH2_ON, TIMER2_CH2, TIMER2_CH3, TIMER13_CH0, USART0_RX, CK_OUT1
PA11[PA9](4)	15	I/O	5VT	Default: PA11 Alternate: SPI0_MISO, USART0_CTS, TIMER0_CH3, TIMER0_BRKIN1
				Remap: PA9 Alternate: CK_OUT0, USART0_TX, TIMER0_CH1, TIMER2_ETI, I2C0_SCL, EVENTOUT
PA12[PA10](4)	16	I/O	5VT	Default: PA12 Alternate: SPI0_MOSI, USART0_RTS_DE_CK, TIMER0_ETI Additional: ADC_IN8
				Remap: PA10 Alternate: USART0_RX, TIMER0_CH2, CK_OUT1, TIMER16_BRKIN0, I2C0_SDA, EVENTOUT
PA13	17	I/O		Default: PA13, SWDIO Alternate: SWDIO, TIMER2_ETI, USART1_RX, EVENTOUT
PA14-BOOT0	18	I/O	5VT	Default: PA14, SWCLK Alternate: SWCLK, USART1_TX, EVENTOUT, SPI0_NSS, USART1_RX, TIMER0_CH0, CK_OUT1, USART0_RTS_DE_CK Additional: BOOT0
PA15	19	I/O		Default: PA15 Alternate: SPI0_NSS, USART1_RX, TIMER0_CH0, CK_OUT1, USART0_RTS_DE_CK, EVENTOUT
PB3	20	I/O		Default: PB3 Alternate: SPI0_SCK, TIMER0_CH1, TIMER2_CH1, USART0_RTS_DE_CK, EVENTOUT
PB4	21	I/O		Default: PB4 Alternate: SPI0_MISO, TIMER2_CH0, USART0_CTS, TIMER16_BRKIN0, EVENTOUT
PB6	22	I/O	5VT	Default: PB6

For Internal Use

Preliminary version
Confidential, under NDA for engineering evaluation only

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

GD32C211Ex TSSOP24				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Alternate: USART0_TX, TIMER0_CH2, TIMER15_CH0_ON, TIMER2_CH2, USART0_RTS_DE_CK, USART0_CTS, I2C0_SCL, I2C0_SMBA, SPI0_MOSI, SPI0_MISO, SPI0_SCK, TIMER0_CH1, TIMER2_CH0, TIMER2_CH1, TIMER15_BRKIN0, TIMER16_BRKIN0
PB7	23	I/O	5VT	Default: PB7 Alternate: USART0_RX, TIMER0_CH3, TIMER16_CH0_ON, TIMER2_CH3, I2C0_SDA, EVENTOUT, USART1_CTS, TIMER15_CH0, TIMER2_CH0, I2C0_SCL
PB8	24	I/O	5VT	Default: PB8 Alternate: USART1_CTS, TIMER15_CH0, TIMER2_CH0, I2C0_SCL, EVENTOUT

Note:

(1) Type: I = input, O = output, A = analog, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

(3) Refer to the description of the NRST_MDSEL[1:0] field in FMC_OBCTL register of GD32C2x1_User_Manual to configure the NRST-PC2 pin as a PC2 general GPIO function.

(4) Refer to the description of the PA12_RMP or PA11_RMP field in SYSCFG_CFG0 register of GD32C2x1_User_Manual.

For Internal Use

Preliminary version
Confidential, under NDA for engineering evaluation only

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

2.6.3. GD32C211Fx QFN20 pin definitions

Table 2-5. GD32C211Fx QFN20 pin definitions

GD32C211Fx QFN20				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PC15-OSC32OUT	1	I/O	5VT	Default: PC15 Alternate: OSC32EN, OSCEN, TIMER0_ETI, TIMER2_CH2 Additional: OSC32OUT
VDD/VREFP	2	P	-	Default: VDD/VREFP
VSS/VREFN	3	P	-	Default: VSS/VREFN
NRST-PC2	4	I/O	5VT	Default: NRST Alternate: CK_OUT0, TIMER0_CH3 Additional: PC2(3)
PA0	5	I/O	5VT	Default: PA0 Alternate: USART1_CTS, TIMER15_CH0, USART0_TX, TIMER0_CH0 Additional: ADC_IN0
PA1	6	I/O	5VT	Default: PA1 Alternate: SPI0_SCK, USART1_RTS_DE_CK, TIMER16_CH0, USART0_RX, TIMER0_CH1, I2C0_SMBA, EVENTOUT Additional: ADC_IN1
PA2	7	I/O	5VT	Default: PA2 Alternate: SPI0_MOSI, USART1_TX, TIMER15_CH0_ON, TIMER2_ETI, TIMER0_CH2, USART2_TX Additional: ADC_IN2
PA3	8	I/O		Default: PA3 Alternate: USART1_RX, TIMER0_CH0_ON, TIMER0_CH3, EVENTOUT, USART2_RX Additional: ADC_IN3
PA4	9	I/O		Default: PA4 Alternate: SPI0_NSS, USART1_TX, TIMER0_CH1_ON, TIMER13_CH0, TIMER16_CH0_ON, EVENTOUT Additional: ADC_IN4, RTC_OUT0
PA5	10	I/O		Default: PA5 Alternate: SPI0_SCK, USART1_RX, TIMER0_CH2_ON, TIMER0_CH0, EVENTOUT Additional: ADC_IN5
PA6	11	I/O		Default: PA6 Alternate: SPI0_MISO, TIMER2_CH0, TIMER0_BRKIN0, TIMER15_CH0, USART2_CTS Additional: ADC_IN6
PA7	12	I/O	5VT	Default: PA7 Alternate: SPI0_MOSI, TIMER2_CH1, TIMER0_CH0

For Internal Use

Preliminary version
Confidential, under NDA for engineering evaluation only

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

GD32C211Fx QFN20				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				_ON, TIMER13_CH0, TIMER16_CH0, USART2_RTS_DE_CK Additional: ADC_IN7
PA8	13	I/O	5VT	Default: PA8 Alternate: CK_OUT0, USART1_TX, TIMER0_CH0, EVENTOUT, SPI0_NSS, TIMER0_CH1_ON, TIMER0_CH2_ON, TIMER2_CH2, TIMER2_CH3, TIMER13_CH0, USART0_RX, CK_OUT1
PA11[PA9](4)	14	I/O	5VT	Default: PA11 Alternate: SPI0_MISO, USART0_CTS, TIMER0_CH3, TIMER0_BRKIN1
				Remap: PA9 Alternate: CK_OUT0, USART0_TX, TIMER0_CH1, TIMER2_ETI, I2C0_SCL, EVENTOUT
PA12[PA10](4)	15	I/O	5VT	Default: PA12 Alternate: SPI0_MOSI, USART0_RTS_DE_CK, TIMER0_ETI Additional: ADC_IN8
				Remap: PA10 Alternate: USART0_RX, TIMER0_CH2, CK_OUT1, TIMER16_BRKIN0, I2C0_SDA, EVENTOUT
PA13	16	I/O		Default: PA13, SWDIO Alternate: SWDIO, TIMER2_ETI, USART1_RX, EVENTOUT
PA14-BOOT0	17	I/O	5VT	Default: PA14, SWCLK Alternate: SWCLK, USART1_TX, EVENTOUT, SPI0_NSS, USART1_RX, TIMER0_CH0, CK_OUT1, USART0_RTS_DE_CK Additional: BOOT0
PB6	18	I/O	5VT	Default: PB6 Alternate: USART0_TX, TIMER0_CH2, TIMER15_CH0_ON, TIMER2_CH2, USART0_RTS_DE_CK, USART0_CTS, I2C0_SCL, I2C0_SMBA, SPI0_MOSI, SPI0_MISO, SPI0_SCK, TIMER0_CH1, TIMER2_CH0, TIMER2_CH1, TIMER15_BRKIN0, TIMER16_BRKIN0
PB7	19	I/O	5VT	Default: PB7 Alternate: USART0_RX, TIMER0_CH3, TIMER16_CH0_ON, TIMER2_CH3, I2C0_SDA, EVENTOUT, USART1_CTS, TIMER15_CH0, TIMER2_CH0, I2C0_SCL
PC14-OSC32IN/OSCEXTIN	20	I/O	5VT	Default: PC14 Alternate: USART0_TX, TIMER0_ETI, TIMER0_BRKIN1, USART1_RTS_DE_CK, TIMER16_CH0, TIMER2_CH1, EVENTOUT

Preliminary version
Confidential, under NDA for engineering evaluation only

For Internal Use

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

GD32C211Fx QFN20				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Additional: OSC32IN

Note:

(1) Type: I = input, O = output, A = analog, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

(3) Refer to the description of the NRST_MDSEL[1:0] field in FMC_OBCTL register of GD32C2x1_User_Manual to configure the NRST-PC2 pin as a PC2 general GPIO function.

(4) Refer to the description of the PA12_RMP or PA11_RMP field in SYSCFG_CFG0 register of GD32C2x1_User_Manual.

For Internal Use

Preliminary version
Confidential, under NDA for engineering evaluation only

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

2.6.4. GD32C211Fx TSSOP20 definitions

Table 2-6. GD32C211Fx TSSOP20 pin definitions

GD32C211Fx TSSOP20				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PC15-OSC32OUT	1	I/O	5VT	Default: PC15 Alternate: OSC32EN, OSCEN, TIMER0_ETI, TIMER2_CH2 Additional: OSC32OUT
VDD/VREFP	2	P	-	Default: VDD/VREFP
VSS/VREFN	3	P	-	Default: VSS/VREFN
NRST-PC2	4	I/O	5VT	Default: NRST Alternate: CK_OUT0, TIMER0_CH3 Additional: PC2(3)
PA0	5	I/O	5VT	Default: PA0 Alternate: USART1_CTS, TIMER15_CH0, USART0_TX, TIMER0_CH0 Additional: ADC_IN0
PA1	6	I/O	5VT	Default: PA1 Alternate: SPI0_SCK, USART1_RTS_DE_CK, TIMER16_CH0, USART0_RX, TIMER0_CH1, I2C0_SMBA, EVENTOUT Additional: ADC_IN1
PA2	7	I/O	5VT	Default: PA2 Alternate: SPI0_MOSI, USART1_TX, TIMER15_CH0_ON, TIMER2_ETI, TIMER0_CH2, USART2_TX Additional: ADC_IN2
PA3	8	I/O		Default: PA3 Alternate: USART1_RX, TIMER0_CH0_ON, TIMER0_CH3, EVENTOUT, USART2_RX Additional: ADC_IN3
PA4	9	I/O		Default: PA4 Alternate: SPI0_NSS, USART1_TX, TIMER0_CH1_ON, TIMER13_CH0, TIMER16_CH0_ON, EVENTOUT Additional: ADC_IN4, RTC_OUT0
PA5	10	I/O		Default: PA5 Alternate: SPI0_SCK, USART1_RX, TIMER0_CH2_ON, TIMER0_CH0, EVENTOUT Additional: ADC_IN5
PA6	11	I/O		Default: PA6 Alternate: SPI0_MISO, TIMER2_CH0, TIMER0_BRKIN0, TIMER15_CH0, USART2_CTS Additional: ADC_IN6
PA7	12	I/O	5VT	Default: PA7 Alternate: SPI0_MOSI, TIMER2_CH1, TIMER0_CH0

For Internal Use

Preliminary version
Confidential, under NDA for engineering evaluation only

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

GD32C211Fx TSSOP20				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				_ON, TIMER13_CH0, TIMER16_CH0, USART2_RTS_DE_CK Additional: ADC_IN7
PA8	13	I/O	5VT	Default: PA8 Alternate: CK_OUT0, USART1_TX, TIMER0_CH0, EVENTOUT, SPI0_NSS, TIMER0_CH1_ON, TIMER0_CH2_ON, TIMER2_CH2, TIMER2_CH3, TIMER13_CH0, USART0_RX, CK_OUT1
PA11[PA9](4)	14	I/O	5VT	Default: PA11 Alternate: SPI0_MISO, USART0_CTS, TIMER0_CH3, TIMER0_BRKIN1
				Remap: PA9 Alternate: CK_OUT0, USART0_TX, TIMER0_CH1, TIMER2_ETI, I2C0_SCL, EVENTOUT
PA12[PA10](4)	15	I/O	5VT	Default: PA12 Alternate: SPI0_MOSI, USART0_RTS_DE_CK, TIMER0_ETI Additional: ADC_IN8
				Remap: PA10 Alternate: USART0_RX, TIMER0_CH2, CK_OUT1, TIMER16_BRKIN0, I2C0_SDA, EVENTOUT
PA13	16	I/O		Default: PA13, SWDIO Alternate: SWDIO, TIMER2_ETI, USART1_RX, EVENTOUT
PA14-BOOT0	17	I/O	5VT	Default: PA14, SWCLK Alternate: SWCLK, USART1_TX, EVENTOUT, SPI0_NSS, USART1_RX, TIMER0_CH0, CK_OUT1, USART0_RTS_DE_CK Additional: BOOT0
PB6	18	I/O	5VT	Default: PB6 Alternate: USART0_TX, TIMER0_CH2, TIMER15_CH0_ON, TIMER2_CH2, USART0_RTS_DE_CK, USART0_CTS, I2C0_SCL, I2C0_SMBA, SPI0_MOSI, SPI0_MISO, SPI0_SCK, TIMER0_CH1, TIMER2_CH0, TIMER2_CH1, TIMER15_BRKIN0, TIMER16_BRKIN0
PB7	19	I/O	5VT	Default: PB7 Alternate: USART0_RX, TIMER0_CH3, TIMER16_CH0_ON, TIMER2_CH3, I2C0_SDA, EVENTOUT, USART1_CTS, TIMER15_CH0, TIMER2_CH0, I2C0_SCL
PC14-OSC32IN/OSCEXTIN	20	I/O	5VT	Default: PC14 Alternate: USART0_TX, TIMER0_ETI, TIMER0_BRKIN1, USART1_RTS_DE_CK, TIMER16_CH0, TIMER2_CH1, EVENTOUT

Preliminary version
Confidential, under NDA for engineering evaluation only

For Internal Use

GD32C211Fx TSSOP20				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Additional: OSC32IN

Note:

(1) Type: I = input, O = output, A = analog, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

(3) Refer to the description of the NRST_MDSEL[1:0] field in FMC_OBCTL register of GD32C2x1_User_Manual to configure the NRST-PC2 pin as a PC2 general GPIO function.

(4) Refer to the description of the PA12_RMP or PA11_RMP field in SYSCFG_CFG0 register of GD32C2x1_User_Manual.

For Internal Use

Preliminary version
Confidential, under NDA for engineering evaluation only

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

2.6.5. GD32C211Jx SOP8 pin definitions

Table 2-7. GD32C211Jx SOP8 pin definitions

GD32C211Jx SOP8				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PB7/PC14-OSC32IN/OSCEXTIN(5)	1	I/O	5VT	Default: PB7 Alternate: USART0_RX, TIMER0_CH3, TIMER16_CH0_ON, TIMER2_CH3, I2C0_SDA, EVENTOUT, USART1_CTS, TIMER15_CH0, TIMER2_CH0, I2C0_SCL
				Default: PC14 Alternate: USART0_TX, TIMER0_ETI, TIMER0_BRKIN1, USART1_RTS_DE_CK, TIMER16_CH0, TIMER2_CH1, EVENTOUT Additional: OSC32IN
VDD/VREFP	2	P	-	Default: VDD/VREFP
VSS/VREFN	3	P	-	Default: VSS/VREFN
PA0/PA1/PA2/NRST-PC2(5)	4	I/O	5VT	Default: PA0 Alternate: USART1_CTS, TIMER15_CH0, USART0_TX, TIMER0_CH0 Additional: ADC_IN0
				Default: PA1 Alternate: SPI0_SCK, USART1_RTS_DE_CK, TIMER16_CH0, USART0_RX, TIMER0_CH1, I2C0_SMBA, EVENTOUT Additional: ADC_IN1
				Default: PA2 Alternate: SPI0_MOSI, USART1_TX, TIMER15_CH0_ON, TIMER2_ETI, TIMER0_CH2 Additional: ADC_IN2
				Default: NRST Alternate: CK_OUT0, TIMER0_CH3 Additional: PC2(3)
PA8/PA11[PA9](4)(5)	5	I/O	5VT	Default: PA8 Alternate: CK_OUT0, USART1_TX, TIMER0_CH0, EVENTOUT, SPI0_NSS, TIMER0_CH1_ON, TIMER0_CH2_ON, TIMER2_CH2, TIMER2_CH3, TIMER13_CH0, USART0_RX, CK_OUT1
				Default: PA11 Alternate: SPI0_MISO, USART0_CTS, TIMER0_CH3, TIMER0_BRKIN1
				Remap: PA9 Alternate: CK_OUT0, USART0_TX, TIMER0_CH1, TIMER2_ETI, I2C0_SCL, EVENTOUT
	6	I/O	5VT	Default: PA12 Alternate: SPI0_MOSI, USART0_RTS_DE_CK, TIME

For Internal Use

Preliminary version
Confidential, under NDA for engineering evaluation only

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

GD32C211Jx SOP8				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PA12[PA10](4)				R0_ETI Additional: ADC_IN8
				Remap: PA10 Alternate: USART0_RX, TIMER0_CH2, CK_OUT1, TIMER16_BRKIN0, I2C0_SDA, EVENTOUT
PA13	7	I/O		Default: PA13, SWDIO Alternate: SWDIO, TIMER2_ETI, USART1_RX, EVENTOUT
PA14-BOOT0/PB6/PC15-OSC32OUT(5)	8	I/O	5VT	Default: PA14, SWCLK Alternate: SWCLK, USART1_TX, EVENTOUT, SPI0_NSS, USART1_RX, TIMER0_CH0, CK_OUT1, USART0_RTS_DE_CK Additional: BOOT0
				Default: PB6 Alternate: USART0_TX, TIMER0_CH2, TIMER15_CH0_ON, TIMER2_CH2, USART0_RTS_DE_CK, USART0_CTS, I2C0_SCL, I2C0_SMBA, SPI0_MOSI, SPI0_MISO, SPI0_SCK, TIMER0_CH1, TIMER2_CH0, TIMER2_CH1, TIMER15_BRKIN0, TIMER16_BRKIN0
				Default: PC15 Alternate: OSC32EN, OSCEN, TIMER0_ETI, TIMER2_CH2 Additional: OSC32OUT

Note:

(1) Type: I = input, O = output, A = analog, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

(3) Refer to the description of the NRST_MDSEL[1:0] field in FMC_OBCTL register of GD32C2x1_User_Manual to configure the NRST-PC2 pin as a PC2 general GPIO function.

(4) Refer to the description of the PA12_RMP or PA11_RMP field in SYSCFG_CFG0 register of GD32C2x1_User_Manual.

(5) Refer to the description of the PINMUXx[1:0](x = 0, 1, 2, 3) field in SYSCFG_CFG3 register of GD32C2x1_User_Manual.

For Internal Use

Preliminary version
Confidential, under NDA for engineering evaluation only

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

2.6.6. GD32C211xx pin alternate functions

Table 2-8. Port A alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PA0		USART1_CTS	TIMER15_CH0		USART0_TX	TIMER0_CH0										
PA1	SPI0_SCK	USART1_RTS_DE_CK	TIMER16_CH0		USART0_RX	TIMER0_CH1	I2C0_SMBA	EVENTOUT								
PA2	SPI0_MOSI	USART1_TX	TIMER15_CH0_ON	TIMER2_ETI		TIMER0_CH2	USART2_TX									
PA3		USART1_RX	TIMER0_CH0_ON			TIMER0_CH3	USART2_RX	EVENTOUT								
PA4	SPI0_NSS	USART1_TX	TIMER0_CH1_ON		TIMER13_CH0	TIMER16_CH0_ON		EVENTOUT								
PA5	SPI0_SCK	USART1_RX	TIMER0_CH2_ON			TIMER0_CH0		EVENTOUT								
PA6	SPI0_MISO	TIMER2_CH0	TIMER0_BRKIN0			TIMER15_CH0	USART2_CTS									
PA7	SPI0_MOSI	TIMER2_CH1	TIMER0_CH0_ON		TIMER13_CH0	TIMER16_CH0	USART2_RTS_DE_CK									
PA8	CK_OUT0	USART1_TX	TIMER0_CH0					EVENTOUT	SPI0_NSS	TIMER0_CH1_ON	TIMER0_CH2_ON	TIMER2_CH2	TIMER2_CH3	TIMER13_CH0	USART0_RX	CK_OUT1
PA9	CK_OUT0	USART0_TX	TIMER0_CH1	TIMER2_ETI			I2C0_SCL	EVENTOUT								
PA10		USART0_RX	TIMER0_CH2	CK_OUT1		TIMER16_BRKIN0	I2C0_SDA	EVENTOUT								
PA11	SPI0_MISO	USART0_CTS	TIMER0_CH3			TIMER0_BRKIN1										
PA12	SPI0_MOSI	USART0_RTS_DE_CK	TIMER0_ETI													
PA13	SWDIO			TIMER2_ETI	USART1_RX			EVENTOUT								
PA14	SWCLK	USART1_TX						EVENTOUT	SPI0_NSS	USART1_RX	TIMER0_CH0	CK_OUT1	USART0_RTS_DE_			

For Internal Use
Preliminary version
Confidential, under NDA for engineering evaluation only

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
													CK			
PA15	SPI0_NSS	USART1_RX	TIMER0_CH0	CK_OUT1	USART0_RTS_DE_CK			EVENTOUT								

Table 2-9. Port B alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PB3	SPI0_SCK	TIMER0_CH1		TIMER2_CH1	USART0_RTS_DE_CK			EVENTOUT								
PB4	SPI0_MISO	TIMER2_CH0			USART0_CTS	TIMER16_BRKIN0		EVENTOUT								
PB6	USART0_TX	TIMER0_CH2	TIMER15_CH0_ON	TIMER2_CH2	USART0_RTS_DE_CK	USART0_CTS	I2C0_SCL	I2C0_SMBA	SPI0_MOSI	SPI0_MISO	SPI0_SCK	TIMER0_CH1	TIMER2_CH0	TIMER2_CH1	TIMER15_BRKIN0	TIMER16_BRKIN0
PB7	USART0_RX	TIMER0_CH3	TIMER16_CH0_ON	TIMER2_CH3			I2C0_SDA	EVENTOUT		USART1_CTS	TIMER15_CH0	TIMER2_CH0			I2C0_SCL	
PB8		USART1_CTS	TIMER15_CH0	TIMER2_CH0			I2C0_SCL	EVENTOUT								

Table 2-10. Port C alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PC2	CK_OUT0	TIMER0_CH3														
PC14	USART0_TX	TIMER0_ETI	TIMER0_BRKIN1							USART1_RTS_DE_CK	TIMER16_CH0	TIMER2_CH1				EVENTOUT
PC15	OSC32EN	OSCEN	TIMER0_ETI	TIMER2_CH2												

For Internal Use

Preliminary version
Confidential, under NDA for engineering evaluation only

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

3. Functional description

3.1. Arm® Cortex®-M23 core

The Cortex-M23 processor is an energy-efficient processor with a very low gate count. It is intended to be used for microcontroller and deeply embedded applications that require an area-optimized processor. The processor is highly configurable enabling a wide range of implementations from those requiring memory protection and powerful trace technology to cost sensitive devices requiring minimal area, while delivering outstanding computational performance and an advanced system response to interrupts.

32-bit Arm® Cortex®-M23 processor core

- Up to 48 MHz operation frequency.
- Single-cycle multiplication and 17-cycle hardware divider.
- Ultra-low power, energy-efficient operation.
- Excellent code density.
- Integrated Nested Vectored Interrupt Controller (NVIC).
- 24-bit SysTick timer.

The Cortex®-M23 processor is based on the ARMv8-M architecture and supports both Thumb and Thumb-2 instruction sets. Some system peripherals listed below are also provided by Cortex®-M23:

- Internal Bus Matrix connected with AHB master, Serial Wire Debug Port and Single-cycle IO port.
- Nested Vectored Interrupt Controller (NVIC).
- Breakpoint Unit(BPU).
- Data Watchpoint and Trace (DWT).
- Serial Wire Debug Port.

3.2. Embedded memory

- Up to 32Kbytes of main Flash memory and 2KB data Flash.
- Up to 6 Kbytes of SRAM with ECC.

32 Kbytes of inner main Flash memory and 2KB data Flash, and 6 Kbytes of inner SRAM at most is available for storing programs and data, and Flash is accessed (read) at CPU clock speed with 0~1 wait states. ***Table 2-2. GD32C211xx memory map*** shows the memory map of the GD32C211xx series of devices, including code, SRAM, peripheral, and other pre-defined regions.

Preliminary version
Confidential, under NDA for engineering evaluation only

For Internal Use

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

3.3. Clock, reset and supply management

- Internal 48 MHz factory-trimmed RC.
- Internal 32 KHz RC calibrated oscillator and external 32.768 KHz crystal oscillator.
- 2.3 to 5.5 V application supply and I/Os.
- Supply Supervisor: POR (Power On Reset), PDR (Power Down Reset).

The Clock Control Unit (CCTL) provides a range of oscillator and clock functions. These include speed internal RC oscillator and external crystal oscillator, high speed and low speed two types. Several prescalers allow the frequency configuration of the AHB and APB domains. The maximum frequency of the AHB, APB domains is 48 MHz/48 MHz. See ***Figure 2-7. GD32C211xx clock tree*** for details on the clock tree.

The Reset Control Unit (RCU) controls three kinds of reset: system reset resets the processor core and peripheral IP components. Power-on reset (POR) and power-down reset (PDR) are always active, and ensures proper operation starting from 1.633 V and down to 1.593V. The device remains in reset mode when V_{DD} is below a specified threshold.

Power supply schemes:

- V_{DD}/V_{DDA} range: 2.3 to 5.5 V, external power supply for I/Os and the internal regulator. Provided externally through V_{DD}/V_{DDA} pins, external analog power supplies for ADC, reset blocks, RCs.
- V_{SS} is 0 V.

3.4. Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from main Flash memory (default).
- Boot from system memory.
- Boot from on-chip SRAM.

In default condition, boot from main Flash memory is selected. The boot loader is located in the internal boot ROM memory (system memory). It is used to reprogram the Flash memory by using USART0 (PA11/PA12) or USART1 (PA2 and PA3) or I2C0 (PB6 and PB7).

Note: When booting from system memory, the USART RX pins (PA12, PA3) are in input level detection mode. Therefore, unused USART RX pins (PA12, PA3) need to be kept at a stable logic level to prevent false triggering.

3.5. Power saving modes

The MCU supports five kinds of power saving modes to achieve even lower power

Preliminary version
Confidential, under NDA for engineering evaluation only

For Internal Use

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

consumption. They are Run1, Sleep, Sleep1, Deep-sleep and Deep-sleep 1 mode. These operating modes reduce the power consumption and allow the application to achieve the best balance between the CPU operating time, speed and power consumption.

- **Run1 mode**

  When in Run1 mode, the NPLDO is off and LPLDO is on, the system clock source should be IRC32K. Before entering the RUN1 mode, the flash power off is completed by software.

- **Sleep mode**

  The Sleep mode is corresponding to the SLEEPING mode of the Cortex®-M23. In Sleep mode, only clock of Cortex®-M23 is off. To enter the Sleep mode, it is only necessary to clear the SLEEPDEEP bit in the Cortex®-M23 System Control Register, and execute a WFI or WFE instruction. If the Sleep mode is entered by executing a WFI instruction, any interrupt can wake up the system. If it is entered by executing a WFE instruction, any wakeup event can wake up the system (If SEVONPEND is 1, any interrupt can wake up the system, refer to Cortex®-M23 Technical Reference Manual). The mode offers the lowest wakeup time as no time is wasted in interrupt entry or exit.

- **Sleep1 mode**

  The Sleep1 mode is corresponding to the SLEEPING mode of the Cortex®-M23 When in Run1 mode. In this mode the NPLDO is off and LPLDO is on, the system clock source is IRC32K.

- **Deep-sleep mode**

  The Deep-sleep mode is based on the SLEEPDEEP mode of the Cortex®-M23. In Deep-sleep mode, all clocks in the 1.2V domain are off, and all of IRC48M is disabled. The contents of SRAM and registers are preserved. The NPLDO is on. Before entering the Deep-sleep mode, it is necessary to set the SLEEPDEEP bit in the Cortex®-M23 System Control Register, and set LPMOD bits to “00” in the PMU_CTL0 register. Then, the device enters the Deep-sleep mode after a WFI or WFE instruction is executed. If the Deep-sleep mode is entered by executing a WFI instruction, any interrupt from EXTI lines can wake up the system. If it is entered by executing a WFE instruction, any wakeup event from EXTI lines can wake up the system (If SEVONPEND is 1, any interrupt from EXTI lines can wake up the system, refer to Cortex®-M23 Technical Reference Manual). When exiting the Deep-sleep mode, the IRC48M is selected as the system clock.

- **Deep-sleep 1 mode**

  The Deep-sleep1 mode is based on the SLEEPDEEP mode of the Cortex®-M23. In Deep-sleep1 mode, all clocks in the 1.2V domain are off, and all of IRC48M is disabled. The contents of SRAM and registers are preserved. The NPLDO is off and LPLDO is on. Before entering the Deep-sleep1 mode, it is necessary to set the SLEEPDEEP bit in the Cortex®-M23 System Control Register, and set LPMOD bits to “01” in the PMU_CTL0 register. Then, the device enters the Deep-sleep1 mode after a WFI or WFE instruction is executed. If the Deep-sleep1 mode is entered by executing a WFI instruction, any interrupt from EXTI lines can wake up the system. If it is entered by executing a WFE instruction, any wakeup event from EXTI lines can wake up the system (If SEVONPEND is 1, any interrupt from EXTI lines can wake up the system, refer to Cortex®-M23

Preliminary version
Confidential, under NDA for engineering evaluation only

For Internal Use

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

Technical Reference Manual). When exiting the Deep-sleep1 mode, the IRC48M is selected as the system clock.

3.6. General-purpose inputs/outputs (GPIOs)

- Up to 22 fast GPIOs, all mappable on 16 external interrupt lines.
- Analog input/output configurable.
- Alternate function input/output configurable.

There are up to 22 general purpose I/O pins (GPIO) in GD32C211xx, named PA0 ~ PA8, PA11 ~ PA15, PB3, PB4, PB6 ~ PB8, PC2, PC14, PC15 to implement logic input/output functions. Each GPIO port has related control and configuration registers to satisfy the requirements of specific applications. The external interrupts on the GPIO pins of the device have related control and configuration registers in the Interrupt/Event Controller Unit (EXTI). The GPIO ports are pin-shared with other alternative functions (AFs) to obtain maximum flexibility on the package pins.

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), input, peripheral alternate function or analog mode. Most of the GPIO pins are shared with digital or analog alternate functions.

3.7. CRC calculation unit (CRC)

- 32-bit data input and 32-bit data output. Calculation period is 4 AHB clock cycles for 32-bit input data size from data entered to the calculation result available.
- Free 8-bit register is unrelated to calculation and can be used for any other goals by any other peripheral devices.
- Fixed polynomial: 0x4C11DB7.

A cyclic redundancy check (CRC) is an error-detecting code commonly used in digital networks and storage devices to detect accidental changes to raw data. This CRC calculation unit can be used to calculate 7/8/16/32 bit CRC code within user configurable polynomial.

3.8. Direct memory access controller (DMA)

- 3 channels for DMA controller.
- DMA request from DMAMUX: peripherals (Timers, ADC, SPIs, I2Cs and USARTs) and request generator.

The flexible general-purpose DMA controllers provide a hardware method of transferring data between peripherals and/or memory without intervention from the CPU, thereby increasing system performance by off-loading the MCU from copying large amounts of data and avoiding frequent interrupts to serve peripherals needing more data or having available data. Three

Preliminary version
Confidential, under NDA for engineering evaluation only

For Internal Use

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

types of access method are supported: peripheral to memory, memory to peripheral, memory to memory.

Each channel is connected to flexible hardware DMA requests. The priorities of DMA channel requests are determined by software configuration and hardware channel number. Transfer size of source and destination are independent and configurable.

3.9. DMA request multiplexer (DMAMUX)

- 3 channels for DMAMUX request multiplexer.
- 4 channels for DMAMUX request generator.
- Support 24 trigger inputs and 24 synchronization inputs.

DMAMUX is a transmission scheduler for DMA requests. The DMAMUX request multiplexer is used for routing a DMA request line between the peripherals / generated DMA request (from the DMAMUX request generator) and the DMA controller. Each DMAMUX request multiplexer channel selects a unique DMA request line, unconditionally or synchronously with events from its DMAMUX synchronization inputs. The DMA request is pending until it is served by the DMA controller which generates a DMA acknowledge signal (the DMA request signal is de-asserted).

3.10. Analog to digital converter (ADC)

- 12-bit SAR ADC's conversion rate is up to 1.60 MSPS.
- Hardware oversampling ratio adjustable from 2x to 256x improves resolution to 12-bit.
- Input voltage range: V_{SS}/V_{SSA} to V_{DD}/V_{DDA}.

A 12-bit multi-channel ADC is integrated in the device. It has a total of 10 multiplexed channels: up to 9 external channels, 1 channel for internal reference voltage (V_{REFINT}). The input voltage range is between V_{SS}/V_{SSA} and V_{DD}/V_{DDA}. An on-chip hardware oversampling scheme improves performance while off-loading the related computational burden from the CPU. The analog watchdog allows the application to detect whether the input voltage goes outside the user-defined higher or lower thresholds. A configurable channel management block can be used to perform conversions in single, continuous, scan or discontinuous mode to support more advanced use.

The ADC can be triggered from the events generated by the general level 0 timer (TIMER2) and the advanced timers (TIMER0) with internal connection.

To ensure a high accuracy on ADC, the independent power supply V_{DDA} is implemented to achieve better performance of analog circuits. V_{DDA} can be externally connected to V_{DD} through the external filtering circuit that avoids noise on V_{DDA}.

For Internal Use

Preliminary version
Confidential, under NDA for engineering evaluation only

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

3.11. Real time clock (RTC)

- 32-bit programmable counter with a programmable 20-bit prescaler.
- Alarm function.

The real time clock is an independent timer which provides a set of continuously running counters in backup registers to provide a real calendar function, and provides an alarm interrupt. The RTC features a 32-bit programmable counter for long-term measurement using the compare register to generate an alarm. A 20-bit prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock of HXTAL clock divided by 128, or LXTAL oscillator clock, or IRC32K oscillator clock.

3.12. Timers and PWM generation

- Up to four 16-bit general timers (TIMER2 TIMER13, TIMER15, TIMER16), and one 16-bit advanced timer (TIMER0).
- Up to 4 independent channels of PWM, output compare or input capture for each general timer and external trigger input.
- Encoder interface controller with two inputs using quadrature decoder.
- 24-bit SysTick timers down counter.
- 2 watchdog timers (free watchdog timer and window watchdog timer).

The advanced timer (TIMER0) can be used as a three-phase PWM multiplexed on 4 channels. It has complementary PWM outputs with programmable dead-time generation. It can also be used as a complete general timer. The 4 independent channels can be used for input capture, output compare, PWM generation (edge-aligned or center-aligned counting modes) and single pulse mode output. If configured as a general 16-bit timer, it has the same functions as the TIMERx timer. It can be synchronized with external signals or to interconnect with other general timers together which have the same architecture and features.

The general timer can be used for a variety of purposes including general time, input signal pulse width measurement or output waveform generation such as a single pulse generation or PWM output, up to 4 independent channels for input capture/output compare. TIMER2 is based on a 16-bit auto-reload up/down/center-aligned counter and a 16-bit prescaler. TIMER13, TIMER15 and TIMER16 is based on a 16-bit auto-reload up counter and a 16-bit prescaler.

The TIMER0 and TIMER2 also support an encoder interface with two inputs using quadrature decoder.

The GD32C211xx have two watchdog peripherals, free watchdog timer and window watchdog timer. They offer a combination of high safety level, flexibility of use and timing accuracy.

The free watchdog timer includes a 12-bit down-counting counter and an 8-stage prescaler.

For Internal Use

Preliminary version
Confidential, under NDA for engineering evaluation only

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

It is clocked from an independent 32 KHz internal RC and as it operates independently of the main clock, it can operate in deep-sleep and standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management.

The window watchdog is based on a 7-bit down counter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early wakeup interrupt capability and the counter can be frozen in debug mode.

The SysTick timer is dedicated for OS, but could also be used as a standard down counter. The features are shown below:

- A 24-bit down counter.
- Auto reload capability.
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source.

3.13. Universal synchronous/asynchronous receiver transmitter (USART/UART)

- Up to three USARTs with operating frequency up to 6 MBits/s.
- Supports both asynchronous and clocked synchronous serial communication modes.
- IrDA SIR encoder and decoder support (only for USART0).
- LIN break generation and detection (only for USART0).
- ISO 7816-3 compliant smart card interface (only for USART0).
- Dual clock domain.
- Wake up from Deep-sleep mode.

The USART (USART0, USART1, USART2) are used to translate data between parallel and serial interfaces, provides a flexible full duplex data exchange using synchronous or asynchronous transfer. It is also commonly used for RS-232 standard communication. The USART includes a programmable baud rate generator which is capable of dividing the system clock to produce a dedicated clock for the USART transmitter and receiver. The USART also supports DMA function for high speed data communication.

3.14. Inter-integrated circuit (I2C)

- Supports standard mode (up to 100 kHz) and fast mode (up to 400 kHz).
- Both master and slave functions with the same interface.
- Provide arbitration function, optional PEC (packet error checking) generation and checking.
- Supports 7-bit and 10-bit addressing mode and general call addressing mode.

Preliminary version
Confidential, under NDA for engineering evaluation only

For Internal Use

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

- Multiple 7-bit slave addresses (2 addresses with configurable mask).
- Wakeup from Deep-sleep / Deep-sleep1 mode on I2C address match.

The I2C interface is an internal circuit allowing communication with an external I2C interface which is an industry standard two lines serial interface used for connection to external hardware. These two serial lines are known as a serial data line (SDA) and a serial clock line (SCL). The I2C module provides different data transfer rates: up to 100 KHz in standard mode, up to 400 KHz in the fast mode. The I2C module also has an arbitration detect function to prevent the situation where more than one master attempts to transmit data to the I2C bus at the same time. A CRC-8 calculator is also provided in I2C interface to perform packet error checking for I2C data.

3.15. Serial peripheral interface (SPI)

- Master or slave operation with full-duplex or simplex mode
- Support both master and slave mode.
- Hardware CRC calculation and transmit automatic CRC error checking.
- Separate transmit and receive buffer, 16 bits wide (only in SPI0).
- Separate transmission and reception 32-bit FIFO (only in SPI1)
- Data frame size can be 8 or 16 bits (only in SPI0).
- Data frame size can be 4 to 16 bits (only in SPI1).
- Transmission and reception using DMA.
- SPI TI mode supported.
- SPI NSS pulse mode supported.
- Quad-SPI configuration available in master mode (only in SPI1).

The SPI interface uses 4 pins, among which are the serial data input and output lines (MISO & MOSI), the clock line (SCK) and the slave select line (NSS). All SPIs can be served by the DMA controller. The SPI interface may be used for a variety of purposes, including simplex synchronous transfers on two lines with a possible bidirectional data line or reliable communication using CRC checking. Quad-SPI master mode is also supported in SPI1.

3.16. Debug mode

- Serial wire debug port (SW-DP).

Debug capabilities can be accessed by a debug tool via Serial Wire (SW - Debug Port).

3.17. Package and operation temperature

- QFN24 (GD32C211ExUxTR), TSSOP24 (GD32C211ExPxTR), QFN20 (GD32C211FxUxTR), TSSOP20 (GD32C211FxPxTR), SOP8 (GD32C211JxMxTR).

Preliminary version
Confidential, under NDA for engineering evaluation only

For Internal Use

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

- Operation temperature range: -40°C to +85°C (industrial level).

For Internal Use

Preliminary version
Confidential, under NDA for engineering evaluation only

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

4 Electrical characteristics

4.1. Parameter introduction

- Parameter conditions: Unless otherwise specified, all values given for V_{DD} = 5 V, T_A = 25°C, and all voltages are referenced to V_{SS}.
- Value guaranteed by design, not 100% tested in production indicates that the value is derived from design or simulation and/or process characteristics.
- Value guaranteed by characterization, not 100% tested in production indicates that the value is derived from comprehensive evaluation after random test.
- Value guaranteed by sample, not 100% tested in production indicates that the value is derived from testing parameters with a small sample size.
- Guaranteed by characterization, the minimum and maximum values refer to random tests and represent the mean value plus or minus three times the standard deviation (mean ±3σ).
- If the value is not specially indicated, it means the value guaranteed by 100% tested in production.

See the following table for some abbreviation terms and their descriptions in this chapter.

Table 4-1. Abbreviations

Acronym	Description
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
DMA	Direct Memory Access
ADC	Analog-to-Digital Converter
GPIO	General Purpose Input/Output
SPI	Serial Peripheral Interface
I2C	Inter-Integrated Circuit Interface
USART	Universal Synchronous / Asynchronous Receiver / Transmitter
FWDGT	Free Watchdog Timer
WWDGT	Window Watchdog Timer

For Internal Use

Preliminary version
Confidential, under NDA for engineering evaluation only

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

4.2. Absolute maximum ratings

The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly beyond the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 4-2. Absolute maximum ratings (1)

Symbol	Description	Min	Max	Unit
V_{DD}	External voltage range(2)	V_{SS} - 0.3	V_{SS} + 5.9	V
V_{IN}	Input voltage on 5V tolerant pin	V_{SS} - 0.3	V_{SS} + 5.9	V
	Input voltage on other I/O	V_{SS} – 0.3	V_{DD} + 0.3	V
I_{IO}	Maximum current for GPIO pins	—	20	mA
$\sum I_{IO}$	Maximum current sunk/sourced by all GPIO pin	—	80	
I_{DD}	Maximum current into VDD pin	—	100	
I_{SS}	Maximum current into VSS pin	—	100	
I_{INJ}	Injected current on each GPIO pin(3)	—	TBD	
$\sum I_{INJ}$	Total injected current on all GPIO pins(4)	—	TBD	
T_{STG}	Storage temperature range	-65	150	°C
T_J	Maximum junction temperature	—	110	°C

(1) Value guaranteed by design, not 100% tested in production.

(2) All main power and ground pins should be connected to an external power source within the allowable range.

(3) I_{INJ} must never be exceeded. Negative injection on any analog input pins disturbs the analog performance of the device.

(4) When several inputs are submitted to a current injection, the maximum ΣI_{INJ} is the absolute sum of the positive and negative injected currents (instantaneous values).

For Internal Use

Preliminary version
Confidential, under NDA for engineering evaluation only

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

4.3. General operating conditions

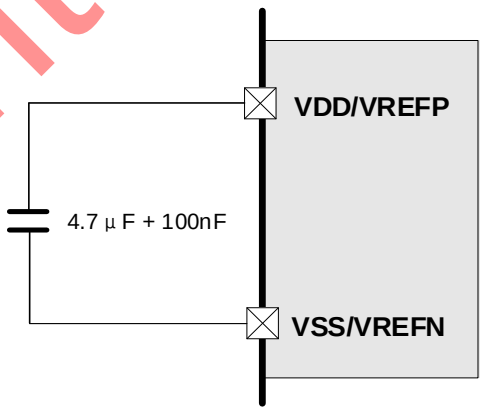
Table 4-3. General operating conditions (1)

Symbol	Description	Conditions	Min	Max	Unit
V_{DD}	Supply voltage	—	2.3	5.5	V
f_{CPU}	Core clock frequency	—	—	48	MHz
f_{HCLK}	AHB clock frequency	—	—	48	MHz
f_{PCLK}	APB clock frequency	—	—	48	MHz
P_D	Power dissipation at T_A = 105°C of QFN24	—	—	TBD	mW
	Power dissipation at T_A = 105°C of TSSOP24		—	TBD	
	Power dissipation at T_A = 105°C of QFN20		—	TBD	
	Power dissipation at T_A = 105°C of TSSOP20		—	TBD	
	Power dissipation at T_A = 105°C of SOP8		—	TBD	
T_A	Operating temperature range for grade 7 device	—	-40	105	°C
T_J(2)	Junction temperature	—	-40	110	

(1) Value guaranteed by design, not 100% tested in production.

(2) The device junction temperature must be kept below maximum T_J, otherwise it may cause permanent damage to the device.

Figure 4-1. Recommended power supply decoupling capacitors (1)



(1) All decoupling capacitors need to be as close as possible to the pins on the PCB board.

For Internal Use

Preliminary version
Confidential, under NDA for engineering evaluation only

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

4.4. Power supply requirement characteristics

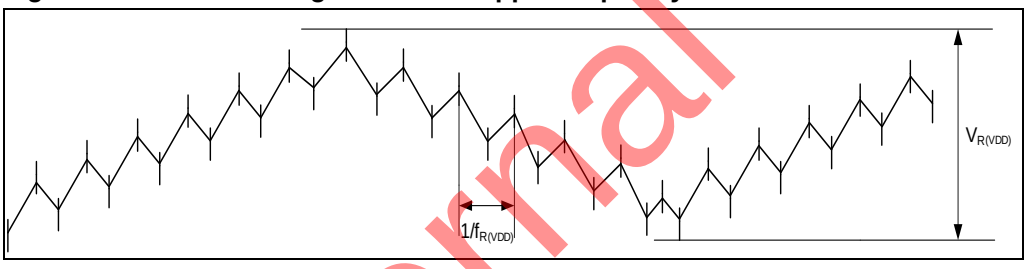
Table 4-4. Power supply requirement characteristics(1)

Symbol	Description	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	—	TBD	TBD	μs/V
	V_{DD} fall time rate		TBD	TBD	
$f_{R(VDD)}$	Allowable ripple frequency	$V_{R(VDD)} \leq 0.2\ V_{DD}$	—	TBD	kHz
		$V_{R(VDD)} \leq 0.08\ V_{DD}$	—	TBD	MHz
		$V_{R(VDD)} \leq 0.06\ V_{DD}$	—	TBD	
ΔV_{DD}(2)	Allowable voltage change rising and falling gradient	When V_{DD} change exceeds V_{DD} ± 10%	TBD	—	ms/V

(1) Value guaranteed by design, not 100% tested in production.

(2) The ripple voltage must meet the allowable ripple frequency $f_{R(VDD)}$ within the range between the V_{DD} lower limit (2.30 V) and upper limit (5.5 V). When the V_{DD} change exceeds V_{DD} ± 10%, the allowable voltage change rising and falling gradient ΔV_{DD} must be met.

Figure 4-2. Rise and fall gradient and ripple frequency characteristics



4.5. Start-up timings of Operating conditions

Table 4-5. Start-up timings of Operating conditions (1)(2)

Symbol	Description	Conditions	Typ	Unit
t_{ST}	Start-up time	Clock source from IRC48M	TBD	μs

(1) Value guaranteed by characterization, not 100% tested in production.

(2) After power-up, the start-up time is the time between the rising edge of NRST high and the first I/O instruction conversion in SystemInit function.

4.6. Wake-up times from power saving modes

Table 4-6. Wake-up times from power saving modes (1)(2)

Symbol	Description	Conditions	Typ	Unit
t_{Sleep}	Wakeup from Sleep mode to Run mode	Transiting to Run mode executing from EFLASH, EFLASH power on during Sleep mode	TBD	μs
		Transiting to Run mode executing from EFLASH, EFLASH power off during Sleep	TBD	

For Internal Use

Preliminary version
Confidential, under NDA for engineering evaluation only

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

Symbol	Description	Conditions	Typ	Unit
		mode		
	Wakeup from Sleep 1 mode to Run 1 mode	Transiting to Run 1 mode executing from SRAM, EFLASH power on during Sleep 1 mode	TBD	
		Transiting to Run 1 mode executing from SRAM, EFLASH power off during Sleep 1 mode	TBD	
$t_{Deep-sleep}$	Wakeup from Deep-sleep mode to Run mode	Transiting to Run mode executing from EFLASH, EFLASH power on during Deep-sleep mode	TBD	
		Transiting to Run mode executing from EFLASH, EFLASH power off during Deep-sleep mode	TBD	
		Transiting to Run mode executing from SRAM, EFLASH power off	TBD	
	Wakeup from Deep-sleep 1 mode to Run mode	Transiting to Run mode executing from EFLASH, EFLASH power on during Deep-sleep 1 mode	TBD	
		Transiting to Run mode executing from EFLASH, EFLASH power off during Deep-sleep 1 mode	TBD	
		Transiting to Run mode executing from SRAM, EFLASH power off	TBD	

(1) Value guaranteed by characterization, not 100% tested in production.

(2) The wakeup time is measured from the wakeup event to the point at which the application code reads the first instruction under the below conditions except sleep 1 mode: V_{DD} 5 V, System clock = f_{IRC48M}/4= f_{HCLK}= 12 MHz.

4.7. Power consumption

The power consumption is measured as described in ***Figure 4 1. Power consumption measurement diagram***. The current consumption values are derived from the tests powered by V_{DD}, while the current is I_{DD}. Unless otherwise stated, V_{DD} = 5 V is applied to supply pins in typical current consumption columns, and V_{DD} = 5.5V is applied in maximum current consumption columns.

The MCU is configured under the following conditions:

- All I/O pins are in analog input mode.
- All peripherals are disabled except when explicitly mentioned.
- Configure the WSCNT bits in the FMC_WS register correctly depend on the AHB clock frequency (refer to the table “The relation between WSCNT and AHB clock frequency” available in the GD32C211_User_Manual).

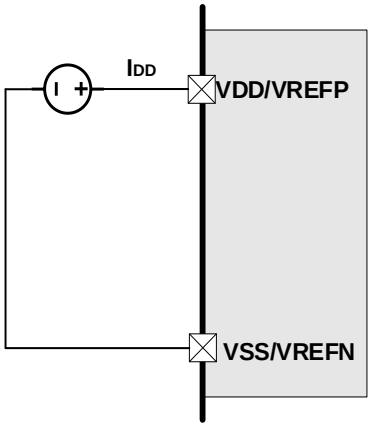
Preliminary version
Confidential, under NDA for engineering evaluation only

For Internal Use

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

- When the peripherals are enabled $f_{PCLK} = f_{HCLK}$.

Figure 4-3. Power consumption measurement diagram



For Internal Use

Preliminary version
Confidential, under NDA for engineering evaluation only

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

Table 4-7. Power consumption in Run mode and 1 Run mode [1][2][3]

Symbol	Description	Conditions			Typ				Max[4]				Unit
		Execute from	General	f_{HCLK}	25°C	55°C	85°C	105°C	25°C	55°C	85°C	105°C	
I_{DD}	Supply current from VDD (Run mode)	EFLASH[5]	IRC48M = 48 MHz, System clock = $f_{IRC48MDIV_SYS} = f_{HCLK}$	48MHz[6]	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
				48MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				24MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				12MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				6MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				3MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				1.5MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				750kHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				375kHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			IRC32K = 32 kHz, System clock = $f_{IRC32K} = f_{HCLK}$	32kHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
		SRAM[7]	IRC48M = 48 MHz, System clock = $f_{IRC48MDIV_SYS} = f_{HCLK}$	48MHz[6]	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				48MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				24MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				12MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				6MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				3MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				1.5MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				750kHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				375kHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			IRC32K = 32 kHz, System clock = $f_{IRC32K} = f_{HCLK}$	32kHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	

For Internal Use

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

Symbol	Description	Conditions			Typ				Max(4)				Unit
		Execute from	General	f_{HCLK}	25°C	55°C	85°C	105°C	25°C	55°C	85°C	105°C	
	Supply current from VDD (Run 1 mode)	SRAM(7)	IRC32K = 32 kHz, System clock = f_{IRC32K} = f_{HCLK}	32kHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	μA
			IRC32K = 32 kHz, System clock = f_{IRC32K} = f_{HCLK}, EFLASH power off	32kHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	

(1) Value guaranteed by characterization, not 100% tested in production.
(2) During power consumption test, GPIO needs to be configure as Analog Input mode.
(3) All peripherals are disabled except when explicitly mentioned.
(4) V_{DD} = 5.5 V for values in Max columns.
(5) The Flash memory access time is adjusted with the correctly wait states number.
(6) All peripherals enabled.
(7) EFLASH power on in Run mode when executing from SRAM.

Table 4-8. Power consumption in Run mode with different codes(1)(2)(3)

Symbol	Description	Conditions			Typ	Unit	Typ	Unit
		Execute from	General	Code				
I_{DD}	Supply current from VDD (Run mode)	EFLASH	IRC48M = 48 MHz, System clock = $f_{IRC48MDIV_SYS}$ = f_{HCLK} = 48 MHz	Coremark	TBD	mA	TBD	μA/MHz
				Dhrystone 2.1	TBD		TBD	
				While (1)(5)	TBD		TBD	
			IRC48M = 48 MHz, System clock = $f_{IRC48MDIV_SYS}$ = f_{HCLK} = 12 MHz	Coremark	TBD		TBD	
				Dhrystone 2.1	TBD		TBD	
				While (1) (5)	TBD		TBD	
			IRC48M = 48 MHz, System clock = $f_{IRC48MDIV_SYS}$ = f_{HCLK} = 3 MHz	Coremark	TBD		TBD	
				Dhrystone 2.1	TBD		TBD	

For Internal Use
Preliminary version
Confidential, under NDA for engineering evaluation only

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

Symbol	Description	Conditions			Typ	Unit	Typ	Unit
		Execute from	General	Code				
				While (1) (5)	TBD		TBD	
		SRAM(4)	IRC48M = 48 MHz, System clock = $f_{IRC48MDIV_SYS}$ = f_{HCLK} = 48 MHz	Coremark	TBD		TBD	
				Dhrystone 2.1	TBD		TBD	
				While (1) (5)	TBD		TBD	
			IRC48M = 48 MHz, System clock = $f_{IRC48MDIV_SYS}$ = f_{HCLK} = 12 MHz	Coremark	TBD		TBD	
				Dhrystone 2.1	TBD		TBD	
				While (1) (5)	TBD		TBD	
			IRC48M = 48 MHz, System clock = $f_{IRC48MDIV_SYS}$ = f_{HCLK} = 3 MHz	Coremark	TBD		TBD	
				Dhrystone 2.1	TBD		TBD	
				While (1) (5)	TBD		TBD	

(1) Value guaranteed by characterization, not 100% tested in production.
(2) During power consumption test, GPIO needs to be configure as Analog Input mode.
(3) All peripherals disabled.
(4) EFLASH power on in Run mode when executing from SRAM.
(5) The code of While (1) used for results provided in ***Table 4-7***.

Table 4-9. Power consumption in Sleep mode and Sleep 1 mode(1)(2)

Symbol	Description	Conditions		Typ(1)				Max(3)				Unit
		General	f_{HCLK}	25°C	55°C	85°C	105°C	25°C	55°C	85°C	105°C	
I_{DD}	Supply current from VDD (Sleep mode)	IRC48M = 48 MHz, System clock = $f_{IRC48MDIV_SYS}$ = f_{HCLK} (f_{HCLK} ≥ 375kHz); IRC32K = 32 kHz, System clock = f_{IRC32K} = f_{HCLK} (f_{HCLK} = 32kHz)	48MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			24MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			12MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			6MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			3MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	

For Internal Use

Preliminary version
Confidential, under NDA for engineering evaluation only

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

Symbol	Description	Conditions		Typ(1)				Max(3)				Unit
		General	f_{HCLK}	25°C	55°C	85°C	105°C	25°C	55°C	85°C	105°C	
			1.5MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			750kHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			375kHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			32kHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
		IRC48M = 48 MHz, System clock = $f_{IRC48MDIV_SYS}$ = f_{HCLK} (f_{HCLK} ≥ 375kHz); IRC32K = 32 kHz, System clock = f_{IRC32K} = f_{HCLK} (f_{HCLK} = 32kHz). EFLASH power off	48MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			24MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			12MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			6MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			3MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			1.5MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			750kHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			375kHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			32kHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
	Supply current from VDD (Sleep 1 mode)	IRC32k = 32 kHz, System clock = f_{IRC32K} = f_{HCLK}	32kHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA
		IRC32k = 32 kHz, System clock = f_{IRC32K} = f_{HCLK}, EFLASH power off	32kHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	

(1) Value guaranteed by characterization, not 100% tested in production.
(2) During power consumption test, GPIO needs to be configure as Analog Input mode.
(3) V_{DD} = 5.5 V for values in Max columns.

Table 4-10. Power consumption in Deep-sleep mode(1)(2)

Symbol	Description	Conditions		Typ(1)				Max				Unit
		General	V_{DD}	25°C	55°C	85°C	105°C	25°C	55°C	85°C	105°C	
I_{DD}			3.3V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA

For Internal Use
Preliminary version
Confidential, under NDA for engineering evaluation only

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

Symbol	Description	Conditions		Typ(1)				Max				Unit
		General	V_{DD}	25°C	55°C	85°C	105°C	25°C	55°C	85°C	105°C	
	Supply current from VDD (Deep-sleep mode)	All clocks off, V_{CORE} set to 1.0 V (PMU_CTL0->DSMODVS[1:0] = 01)	5V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			5.5V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
		All clocks off, V_{CORE} set to 1.1 V (PMU_CTL0->DSMODVS[1:0] = 10)	3.3V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			5V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			5.5V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
		All clocks off, V_{CORE} set to 1.2 V (PMU_CTL0->DSMODVS[1:0] = 11)	3.3V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			5V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			5.5V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
		All clocks off, EFLASH power off, V_{CORE} set to 1.0V (PMU_CTL0->DSMODVS[1:0] = 01)	3.3V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			5V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			5.5V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
		All clocks off, EFLASH power off, V_{CORE} set to 1.1V (PMU_CTL0->DSMODVS[1:0] = 10)	3.3V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			5V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			5.5V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
		All clocks off, EFLASH power off, V_{CORE} set to 1.2V (PMU_CTL0->DSMODVS[1:0] = 11)	3.3V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			5V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			5.5V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
		IRC32K off, LXTAL bypass, RTC on, RTC supplied with LXTAL bypass (32.768kHz)	3.3V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			5V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			5.5V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
		IRC32K off, LXTAL bypass, RTC on, RTC supplied with LXTAL bypass (32.768kHz), EFLASH power off	3.3V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			5V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			5.5V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	

(1) Value guaranteed by characterization, not 100% tested in production.

(2) During power consumption test, GPIO needs to be configure as Analog Input mode.

For Internal Use

Preliminary version
Confidential, under NDA for engineering evaluation only

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

Table 4-11. Power consumption in Deep-sleep 1 mode(1)(2)

Symbol	Description	Conditions		Typ(1)				Max				Unit
		General	V_{DD}	25°C	55°C	85°C	105°C	25°C	55°C	85°C	105°C	
I_{DD}	Supply current from VDD (Deep-sleep 1 mode)	All clocks off, V_{CORE} set to 0.9 V (PMU_CTL0->DSMODVS[1:0] = 00)	3.3V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	μA
			5V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			5.5V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
		All clocks off, V_{CORE} set to 1.0 V (PMU_CTL0->DSMODVS[1:0] = 01)	3.3V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			5V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			5.5V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
		All clocks off, V_{CORE} set to 1.1 V (PMU_CTL0->DSMODVS[1:0] = 10)	3.3V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			5V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			5.5V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
		All clocks off, V_{CORE} set to 1.2 V (PMU_CTL0->DSMODVS[1:0] = 11)	3.3V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			5V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			5.5V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
		All clocks off, EFLASH power off, V_{CORE} set to 0.9 V (PMU_CTL0->DSMODVS[1:0] = 00)	3.3V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			5V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			5.5V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
		All clocks off, EFLASH power off, V_{CORE} set to 1.0V (PMU_CTL0->DSMODVS[1:0] = 01)	3.3V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			5V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			5.5V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
		All clocks off, EFLASH power off, V_{CORE} set to 1.1V (PMU_CTL0->DSMODVS[1:0] = 10)	3.3V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			5V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			5.5V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
		All clocks off, EFLASH power off, V_{CORE} set to 1.2V (PMU_CTL0->DSMODVS[1:0] = 11)	3.3V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			5V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			5.5V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	

For Internal Use

Preliminary version
Confidential, under NDA for engineering evaluation only

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

Symbol	Description	Conditions		Typ(1)				Max				Unit
		General	V_{DD}	25°C	55°C	85°C	105°C	25°C	55°C	85°C	105°C	
		IRC32K off, LXTAL bypass, RTC on, RTC supplied with LXTAL bypass (32.768kHz)	3.3V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			5V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			5.5V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
		IRC32K off, LXTAL bypass, RTC on, RTC supplied with LXTAL bypass (32.768kHz), EFLASH power off	3.3V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			5V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			5.5V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	

(1) Value guaranteed by characterization, not 100% tested in production.

(2) During power consumption test, GPIO needs to be configure as Analog Input mode.

For Internal Use

Preliminary version
Confidential, under NDA for engineering evaluation only

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

The current consumption of the on-chip peripherals is given in the following table. To avoid adding the CPU dynamic power consumption to the peripheral power consumption, the MCU needs to enter sleep mode to stop the CPU operation during current measurement. The MCU is configured under the following conditions:

- All I/O pins are in analog input mode
- The given value is in the table calculated by measuring the difference of the current consumptions:
  -- The target peripheral is clocked on and enters sleep mode
  -- All peripherals are clocked off and enter sleep mode

The power consumption of the digital part of the on-chip peripherals is given in the following table. The power consumption of the analog part of the peripherals (where applicable) is indicated in each related section of the datasheet.

Table 4-12. Peripheral current consumption characteristics(1)

Bus	Peripherials	Typical consumption	Unit
AHB1	FMC	TBD	μA/MHz
	CRC	TBD	
	DMA	TBD	
	DMAMUX	TBD	
AHB2	GPIOA	TBD	
	GPIOB	TBD	
	GPIOC	TBD	
	GPIOF	TBD	
APB	SYSCFG	TBD	
	WWDGT	TBD	
	ADC	TBD	
	TIMER0	TBD	
	TIMER2	TBD	
	SPI0	TBD	
	USART0	TBD	
	USART1	TBD	
	TIMER13	TBD	
	TIMER15	TBD	
	TIMER16	TBD	
	USART2	TBD	
	I2C0	TBD	
	DBG	TBD	
	PMU	TBD	

(1) Value guaranteed by characterization, not 100% tested in production.

For Internal Use

Preliminary version
Confidential, under NDA for engineering evaluation only

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

4.8. EMC characteristics

System level ESD (Electrostatic discharge, according to IEC 61000-4-2) and EFT (Electrical Fast Transient/burst, according to IEC 61000-4-4) testing result is given in the ***Table 4-13. System level ESD and EFT characteristics*** (1). System level ESD is for end-customer operation, it includes ESD field events on system level occur in an unprotected area (outside EPA). System level ESD protection necessary to satisfy higher ESD levels.

Table 4-13. System level ESD and EFT characteristics (1)

Symbol	Description	Conditions	Max	Unit	Level
V_{ESD}	Contact / Air mode high voltage stressed on few special I/O pins	V_{DD} = 5 V, T_A = 25 °C TBD, f_{HCLK} = TBD MHz IEC 61000-4-2	CD TBD AD TBD	V	TBD
V_{EFT}	Fast transient high voltage burst stressed on Power and GND	V_{DD} = 5 V, T_A = 25 °C TBD, f_{HCLK} = TBD MHz IEC 61000-4-4	TBD	V	TBD

(1) Value guaranteed by characterization, not 100% tested in production.

EMI (Electromagnetic Interference) emission test result is given in the ***Table 4-14. EMI characteristics*** (1), The electromagnetic field emitted by the device are monitored while an application, executing EEMBC code, is running. The test is compliant with SAE J1752-3:2017 standard which specifies the test board and the pin loading.

Table 4-14. EMI characteristics (1)

Symbol	Parameter	Conditions	Package	Max vs. [f_{HCLK}] 48 MHz			Unit
				0.1-30MHz	30-130MHz	130MHz-1GHz	
S_{EMI}	Peak level	V_{DD} = 5.5 V, T_J = +25 °C, f_{HCLK} = TBD MHz, conforms to SAE J1752-3:2017	TBD	TBD	TBD	TBD	dBµV

(1) Value guaranteed by characterization, not 100% tested in production.

Component level ESD include HBM (Human body model, according to ANSI/ESDA/JEDEC JS-001) and CDM (ANSI/ESDA/JEDEC JS-002), that ESD field events during manufacturing in an ESD protected area, such as PCB assembly/repair, IC assembly/test and Fab environment. The ESD protected area (EPA) has many measures, for instance ESD protective packaging, grounding person wrist strap to ground (or flooring/footwear), grounded work surface and ionizer.

Static latch-up (LU, according to JEDEC78) test is based on the two measurement methods, I/O current injection value (I-test) and power supply over-voltage value.

For Internal Use

Preliminary version
Confidential, under NDA for engineering evaluation only

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

Table 4-14. Component level ESD and latch-up characteristics(1)

Symbol	Description	Conditions	Package	Max	Unit	Level
V_{HBM}	Human body model electrostatic discharge voltage (Any pin combination)	T_A = 25 °C; JS-001-2017	TBD	TBD	V	TBD
V_{CDM}	Charge device model electrostatic discharge voltage (All pins)	T_A = 25 °C; JS-002-2018	TBD	TBD	V	TBD
LU	I-test	T_A = 25 °C; JESD78	TBD	TBD	mA	Class TBD
	V_{supply} over voltage			TBD	V	Level TBD

(1) Value guaranteed by characterization, not 100% tested in production.

4.9. Power supply supervisor characteristics

Table 4-15. Power supply supervisor characteristics (1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{POR}	Power on reset threshold	—	—	1.62	TBD(2)	V
V_{PDR}	Power down reset threshold	—	TBD(2)	1.58	—	
V_{BOR1}	Brown-out reset threshold 1	rising edge	—	2.1	—	V
		falling edge	—	2.0	—	
V_{BOR2}	Brown-out reset threshold 2	rising edge	—	2.3	—	V
		falling edge	—	2.2	—	
V_{BOR3}	Brown-out reset threshold 3	rising edge	—	2.6	—	V
		falling edge	—	2.5	—	
V_{BOR4}	Brown-out reset threshold 4	rising edge	—	2.9	—	V
		falling edge	—	2.8	—	
$V_{POR(HYST)}$	POR hysteresis	—	—	40	—	mV
$V_{BOR(HYST)}$	BOR hysteresis	—	—	100	—	mV
$t_{RST(TEMPO)}$	Reset temporization	—	—	500	—	µs

(1) Value guaranteed by design, not 100% tested in production.

(2) Value guaranteed by characterization, not 100% tested in production.

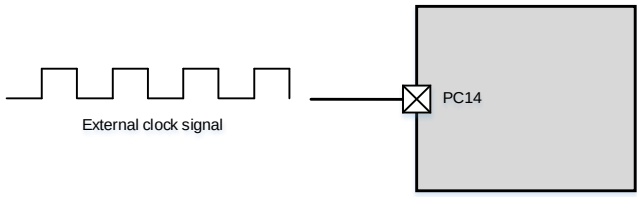
For Internal Use

Preliminary version
Confidential, under NDA for engineering evaluation only

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

4.10. External clock characteristics

Figure 4-4. Recommended external clock



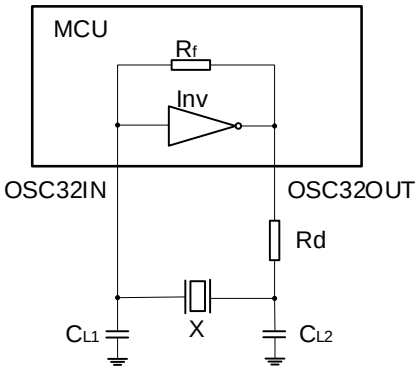
PC14 can be used as a standard GPIO to input an external clock, and the external clock signal has to respect the characteristics below.

Table 4-16. External clock characteristics (1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{EXT_CLK}	External clock frequency	2.3 V ≤ V_{DD} ≤ 5.5 V	—	—	50	MHz
$V_{H(EXT_CLK)}$	External clock input pin high level voltage	2.3 V ≤ V_{DD} ≤ 5.5 V	0.7V_{DD}	—	5.5	V
$V_{L(EXT_CLK)}$	External clock input pin low level voltage		V_{SS}-0.3	—	0.3V_{DD}	
$t_{H/L(EXT_CLK)}$	External clock signal high or low time	—	1/(6*f_{EXT_CLK})	—	—	ns
$t_{R/F(EXT_CLK)}$	External clock signal rise or fall time	—	—	—	1/(3*f_{EXT_CLK})	
C_{IN}	External clock input capacitance	—	—	2.7	—	pF
$Duty_{EXT_CLK}$	Duty cycle	—	45	—	55	%

(1) Value guaranteed by design, not 100% tested in production.

Figure 4-5. Internal structure diagram of OSC32IN and OSC32OUT pin



It is strongly recommended to meature the oscillation allowance (negative resistance) in the final target system (layout) to determine which load capacitors will best tune their

Preliminary version
Confidential, under NDA for engineering evaluation only

For Internal Use

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

resonator/crystal to the microcontroller device for optimum start-up and operation over temperature/voltage extremes.

Table 4-17. Low speed external clock (LXTAL) generated from a crystal/ceramic characteristics(1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{LXTAL}	Crystal or ceramic frequency	2.3 V ≤ V_{DD} ≤ 5.5 V	—	32.768	—	kHz
C_{LXTAL}(2)	Recommended matching capacitance on OSC32IN and OSC32OUT	—	—	10	—	pF
$Duty_{LXTAL}$	Crystal or ceramic duty cycle	—	30	—	70	%
g_m(3)	Oscillator transconductance	LXTALDRI= 0	—	7	—	μA/V
		LXTALDRI= 1	—	14	—	
$I_{DD(LXTAL)}$	Crystal or ceramic operating current	LXTALDRI= 0	—	760	—	nA
		LXTALDRI= 1	—	1140	—	
$t_{ST(LXTAL)}$(4)	Crystal or ceramic startup time	LXTALDRI= 0	—	0.4	—	s
		LXTALDRI= 1	—	0.25	—	

(1) Value guaranteed by design, not 100% tested in production.

(2) $C_{LXTAL1} = C_{LXTAL2} = 2*(C_{LOAD} - C_S)$, For C_{LXTAL1} and C_{LXTAL2}, it is recommended matching capacitance on OSC32IN and OSC32OUT. For C_{LOAD}, it is crystal/ceramic load capacitance, provided by the crystal or ceramic manufacturer. For C_S, it is PCB and MCU pin stray capacitance.

(3) More details about g_m could be found in ***AN052 GD32 MCU Resonator-Based Clock Circuits***.

(4) $t_{START\ (LXTAL)}$ is the startup time measured from the moment it is enabled (by software) to the 32.768 kHz oscillator stabilization flags is SET. This value varies significantly with the crystal manufacturer.

Table 4-18. Low speed external user clock characteristics (LXTAL in bypass mode) (1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
$f_{LXTAL(EXT)}$	External clock source or oscillator frequency	2.3 V ≤ V_{DD} ≤ 5.5 V	—	32.768	1000	kHz
$V_{H(LXTAL)}$	OSC32IN input pin high level voltage	2.3 V ≤ V_{DD} ≤ 5.5 V	0.7V_{DD}	—	V_{DD}	V
$V_{L(LXTAL)}$	OSC32IN input pin low level voltage		V_{SS}	—	0.3 V_{DD}	
$t_{H/L(LXTAL)}$	OSC32IN high or low time	—	250	—	—	ns
$t_{R/F(LXTAL)}$	OSC32IN rise or fall time	—	—	—	50	
C_{IN}	OSC32IN input capacitance	—	—	5	—	pF
$Duty_{LXTAL}$	Duty cycle	—	30	—	70	%

(1) Value guaranteed by design, not 100% tested in production.

For Internal Use

Preliminary version
Confidential, under NDA for engineering evaluation only

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

Figure 4-6. Recommended external OSC32IN and OSC32OUT pins circuit for crystal

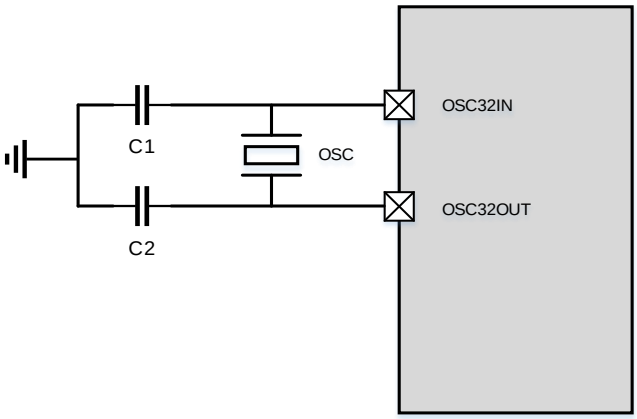
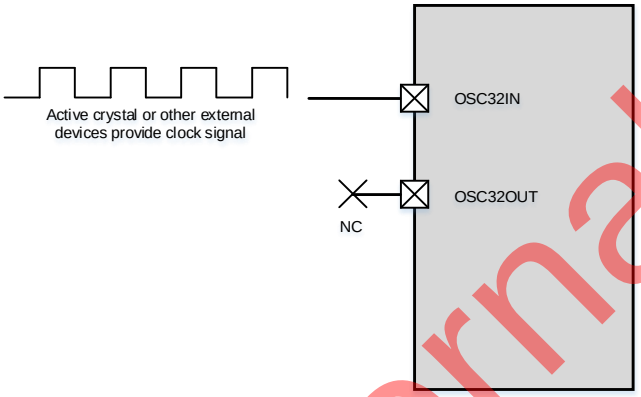


Figure 4-7. Recommended external OSC32IN and OSC32OUT pins circuit for oscillator



For Internal Use

Preliminary version
Confidential, under NDA for engineering evaluation only

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

4.11. Internal clock characteristics

Table 4-19. High speed internal clock (IRC48M) characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{IRC48M}	High Speed Internal Oscillator (IRC48M) frequency	V_{DD} = 5V, T_A = 25 °C	TBD	48	TBD	MHz
$Drift_{IRC48M}$	IRC48M oscillator Frequency Drift, Factory-trimmed(1)	T_A = -40 °C ~ +105 °C	TBD	—	TBD	%
	IRC48M oscillator Frequency accuracy, User trimming step(2)	—	—	0.3	—	%
$Duty_{IRC48M}$(2)	IRC48M oscillator duty cycle	—	45	50	55	%
$I_{DD(IRC48M)}$(2)	IRC48M oscillator operating current	f_{IRC48M} = 48 MHz	—	130	—	μA
$t_{ST(IRC48M)}$(2)	IRC48M oscillator startup time	f_{IRC48M} = 48 MHz	—	2.2	—	μs

(1) Value guaranteed by characterization, not 100% tested in production.
(2) Value guaranteed by design, not 100% tested in production.

Table 4-20. Low speed internal clock (IRC32K) characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{IRC32K}	Low Speed Internal oscillator (IRC32K) frequency	V_{DD} = 5V, T_A = 25 °C	TBD	32	TBD	kHz
		2.3 V ≤ V_{DD} ≤ 5.5 V, T_A = -40 °C ~ 105 °C(1)	TBD	—	TBD	
$I_{DD(IRC32K)}$(2)	IRC32K oscillator operating current	—	—	470	—	nA
$t_{ST(IRC32K)}$(2)	IRC32K oscillator startup time	—	—	50	—	μs

(1) Value guaranteed by characterization, not 100% tested in production.
(2) Value guaranteed by design, not 100% tested in production.

For Internal Use

Preliminary version
Confidential, under NDA for engineering evaluation only

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

4.12. Memory characteristics

Table 4-21. Flash memory characteristics (1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
$I_{DD(FLASH)}$	Average supply current from V_{DD} during FLASH operation	Erasing	—	0.5	—	mA
		Programming	—	0.7	—	mA
PE_{CYC}	Number of guaranteed program /erase cycles before failure (Endurance)	—	10	—	—	kcycles
t_{RET}	Data retention time	T_A = 25 °C	100	—	—	years
		T_A = 85 °C	20	—	—	
		T_A = 105 °C	4	—	—	
N_{WS}(2)	Flash wait state counter during read operation	f_{HCLK} ≤ 24MHz	—	0	—	HCLK cycles
		24MHz < f_{HCLK} ≤ 48MHz	—	1	—	
t_{PROG}	Word programming time	TA = -40 °C ~ + 105 °C	—	85	—	μs
t_{PROG_ROW}	Row (8 double word) programming time	Normal programming	—	0.68	—	ms
		Fast programming	—	0.4	—	
t_{PROG_PAGE}	Page (512 byte) programming time	Normal programming	—	5.44	—	ms
		Fast programming	—	3.2	—	
t_{ERASE}	Page erase time	T_A = -40 °C ~ + 105 °C	2	—	3	ms
t_{MERASE}	Mass erase time	T_A = -40 °C ~ + 105°C	30	—	40	ms

(1) Value guaranteed by design, not 100% tested in production.

4.13. NRST pin characteristics

Table 4-22. NRST pin characteristics (1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST Input low level voltage	—	—	—	0.3 V_{DD}	V
$V_{IH(NRST)}$	NRST Input high level voltage	—	0.7 V_{DD}	—	—	
V_{HYST}	Schmidt trigger Voltage hysteresis	V_{DD} = 3.3 V	—	400	—	mV
		V_{DD} = 5.0 V	—	458	—	
		V_{DD} = 5.5 V	—	478	—	
R_{PU}	Pull-up equivalent resistor	—	—	40	—	kΩ
$t_{F(NRST)}$	NRST input filtered pulse	2.3V < V_{DD} < 5.5 V	—	—	66	ns
$t_{NF(NRST)}$	NRST input not filtered pulse	2.3V < V_{DD} < 5.5 V	350	—	—	ns

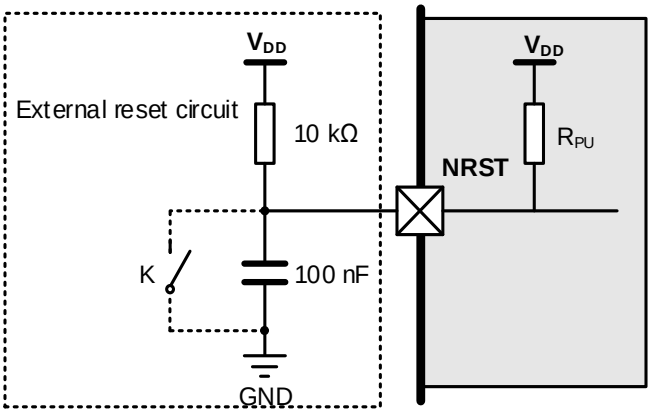
(1) Value guaranteed by design, not 100% tested in production.

For Internal Use

Preliminary version
Confidential, under NDA for engineering evaluation only

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

Figure 4-8. Recommended external NRST pin circuit (1)



(1) Unless the voltage on NRST pin go below $V_{IL(NRST)}$ level, the device would not generate a reliable reset.

4.14. GPIO current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures. The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of the -5 µA/+0 µA range) or other functional failure (for example reset occurrence or oscillator frequency deviation).

Negative induced leakage current is caused by negative injection and positive induced leakage current is caused by positive injection.

Table 4-23. GPIO current injection susceptibility

Symbol	Description		Functional susceptibility		Unit
			Negative injection	Positive injection	
I_{INJ}(1)	Injected current on pin	Input current on 5V tolerant pin	TBD	TBD	mA
		Input current on other I/O(Except BOOT0)	TBD	TBD	
		BOOT0	TBD	TBD	

Preliminary version
Confidential, under NDA for engineering evaluation only

For Internal Use

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

(1) Value guaranteed by design, not 100% tested in production.

4.15. GPIO characteristics

More details about GPIO could be found in ***AN092 GD32 MCU GPIO structure and precautions.***

Table 4-24. I/O static characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{IL}(1)	CMOS Low level input voltage	2.3 V ≤ V_{DD} ≤ 5.5 V	—	—	0.3V_{DD}	V
	TTL Low level input voltage	2.7 V ≤ V_{DD} ≤ 3.6 V	—	—	0.8	
V_{IH}(1)	CMOS High level input voltage	2.3 V ≤ V_{DD} ≤ 5.5 V	0.7V_{DD}	—	—	V
	TTL High level input voltage	2.7 V ≤ V_{DD} ≤ 3.6 V	2.0	—	—	
V_{HYS}(1)	Input hysteresis	2.3 V ≤ V_{DD} ≤ 5.5 V	—	355	—	mV
I_{LEAK}(2)	IO input leakage current	V_{SS} ≤ V_{IN} ≤ V_{DD}	-2	—	2	μA
R_{PU}(1)	Weak pull-up equivalent resistor	V_{IN} = V_{SS}	—	40	—	kΩ
R_{PD}(1)	Weak pull-down equivalent resistor	V_{IN} = V_{DD}	—	40	—	kΩ

(1) Value guaranteed by design, not 100% tested in production.
(2) Value guaranteed by characterization, not 100% tested in production.

Table 4-25. Output voltage characteristics for all I/Os (1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{OL} (GPIO_OSPD = 0)	Low level output voltage for an IO Pin (I_{IO} = +3 mA)	V_{DD} = 3.3 V	TBD	TBD	TBD	V
		V_{DD} = 5 V	TBD	TBD	TBD	
		V_{DD} = 5.5 V	TBD	TBD	TBD	
	Low level output voltage for an IO Pin (I_{IO} = +8 mA)	V_{DD} = 3.3 V	TBD	TBD	TBD	
		V_{DD} = 5 V	TBD	TBD	TBD	
		V_{DD} = 5.5 V	TBD	TBD	TBD	
V_{OH} (GPIO_OSPD = 0)	High level output voltage for an IO Pin (I_{IO} = +3 mA)	V_{DD} = 3.3 V	TBD	TBD	TBD	V
		V_{DD} = 5 V	TBD	TBD	TBD	
		V_{DD} = 5.5 V	TBD	TBD	TBD	
	High level output voltage for an IO Pin (I_{IO} = +8 mA)	V_{DD} = 3.3 V	TBD	TBD	TBD	
		V_{DD} = 5 V	TBD	TBD	TBD	
		V_{DD} = 5.5 V	TBD	TBD	TBD	
V_{OL} (GPIO_OSPD = 1)	Low level output voltage for an IO Pin (I_{IO} = +8 mA)	V_{DD} = 3.3 V	TBD	TBD	TBD	V
		V_{DD} = 5 V	TBD	TBD	TBD	
		V_{DD} = 5.5 V	TBD	TBD	TBD	
	Low level output	V_{DD} = 3.3 V	TBD	TBD	TBD	

Preliminary version
Confidential, under NDA for engineering evaluation only

For Internal Use

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

Symbol	Description	Conditions	Min	Typ	Max	Unit
	voltage for an IO Pin (I_{IO} = +20 mA)	V_{DD} = 5 V	TBD	TBD	TBD	
		V_{DD} = 5.5 V	TBD	TBD	TBD	
V_{OH} (GPIO_OSPD = 1)	High level output voltage for an IO Pin (I_{IO} = +8 mA)	V_{DD} = 3.3 V	TBD	TBD	TBD	V
		V_{DD} = 5 V	TBD	TBD	TBD	
		V_{DD} = 5.5 V	TBD	TBD	TBD	
	High level output voltage for an IO Pin (I_{IO} = +20 mA)	V_{DD} = 3.3 V	TBD	TBD	TBD	
		V_{DD} = 5 V	TBD	TBD	TBD	
		V_{DD} = 5.5 V	TBD	TBD	TBD	

(1) Value guaranteed by characterization, not 100% tested in production.

Table 4-26. I/O port AC characteristics (1)(2)(3)(4)

Speed	Symbol	Description	Conditions	Min	Max	Unit
0	t_R/t_F	Output high to low level fall time and output low to high level rise time	2.7 V ≤ V_{DD} ≤ 5.5 V, C_L = 10 pF, Fmax=15MHz	—	4.6	ns
			2.3 V ≤ V_{DD} ≤ 5.5 V, C_L = 30 pF, Fmax=10MHz	—	20.5	
			2.7 V ≤ V_{DD} ≤ 5.5 V, C_L = 50 pF, Fmax=10Mz	—	17.4	
			2.3 V ≤ V_{DD} ≤ 5.5 V, C_L = 50 pF, Fmax=2Mz	—	33.0	
1	t_R/t_F	Output high to low level fall time and output low to high level rise time	2.70 V ≤ V_{DD} ≤ 5.5 V, C_L = 30 pF, Fmax=50MHz	—	5.0	ns
			2.3 V ≤ V_{DD} ≤ 5.5 V, C_L = 10 pF, Fmax=40MHz	—	2.6	
			2.70 V ≤ V_{DD} ≤ 5.5 V, C_L = 50 pF, Fmax=30MHz	—	7.4	
			2.3V ≤ V_{DD} ≤ 5.5 V, C_L = 30 pF, Fmax=30MHz	—	9.4	

(1) The maximum frequency is defined with the following conditions: (tr+tf) ≤ 2/3 T Skew ≤ 1/20 T 45% < Duty cycle < 55%.

(2) The fall and rise times are defined between 90% and 10% and between 10% and 90% of the output waveform, respectively.

(3) Value guaranteed by design, not 100% tested in production.

(4) The data is for reference only, and the specific values are related to PCB Layout.

4.16. Internal reference voltage characteristics

Table 4-27. Internal reference voltage characteristics(1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	T_A = -40°C ~ +105 °C	1.1	1.2	1.3	V
$t_{S_VREFINT}$(1)(2)	ADC sampling time when reading the internal	—	4	—	—	μs

Preliminary version
Confidential, under NDA for engineering evaluation only

For Internal Use

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

Symbol	Description	Conditions	Min	Typ	Max	Unit
	reference voltage					
$t_{STA_VREFINT}$(1)	Start time of reference voltage buffer when ADC is enable	—	—	8	12	μs
$I_{DD(VREFINT_BUF)}$(1)	V_{REFINT} buffer consumption from V_{DD} when converted by ADC	—	—	10	—	μA
ΔV_{REFINT}(1)	Internal reference voltage spread over the temperature range	—	—	10.5	—	mV

(1) Value guaranteed by design, not 100% tested in production.

(2) The shortest sampling time can be determined in the application by multiple iterations.

Table 4-28. Internal reference voltage calibration values

Symbol	Test conditions	Memory address
V_{REFINT}(1)	V_{DD} = 5 V (± 10mV), Temperature = 25 °C (± 5 °C)	TBD

(1) V_{REFINT} is internally connected to the ADC_IN17 input channel.

4.17. ADC characteristics

Table 4-29. ADC characteristics (1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{DD}	Operating voltage	—	2	—	5.5	V
V_{REFP}(2)	Positive Reference Voltage	—	2	—	V_{DD}	V
V_{IN}	ADC input voltage range	—	0	—	V_{REFP}	V
f_{ADC}	ADC clock	—	—	—	16	MHz
f_S	Sampling rate	12-bit	—	—	1	MSPS
		10-bit	—	—	1.14	
		8-bit	—	—	1.33	
		6-bit	—	—	1.6	
R_{AIN}	External input impedance	See *Equation 1*	—	—	128	kΩ
R_{ADC}	Input sampling switch resistance	—	—	—	1.2	kΩ
C_{ADC}	Input capacitance	No pin/pad capacitance included	—	2.9	—	pF
t_S	Sampling time	f_{ADC} = 16 MHz	0.219	—	10	μs
t_{CONV}	Total conversion time(including sampling time)	12-bit	—	16	—	1/ f_{ADC}
		10-bit	—	14	—	
		8-bit	—	12	—	
		6-bit	—	10	—	

For Internal Use

Preliminary version
Confidential, under NDA for engineering evaluation only

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

Symbol	Description	Conditions	Min	Typ	Max	Unit
$I_{DD(ADC)}$	ADC consumption from V_{DD}	V_{DD} = 5 V	—	700	—	μA
$t_{ST(ADC)}$	Startup time	—	—	1	—	μs

(1) Value guaranteed by design, not 100% tested in production.
(2) VREFP and VDD are connected internally.

Equation 1: R_{AIN} max formula $R_{AIN} < \frac{T_s}{f_{ADC} * C_{ADC} * \ln(2^{N+2})} - R_{ADC}$

The formula above (***Equation 1***) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

Table 4-30. ADC RAIN max for f_{ADC} = 16 MHz (1)(2)

Resolution	Sampling cycles	t_S (μs)	R_{AIN} max (kΩ)
12 bits	3.5	0.219	1.61
	7.5	0.469	4.83
	12.5	0.781	8.86
	19.5	1.219	14.49
	39.5	2.469	30.6
	79.5	4.968	62.8
	160.5	10.03	128
10 bits	3.5	0.219	2.08
	7.5	0.469	5.84
	12.5	0.781	10.5
	19.5	1.219	17.11
	39.5	2.469	35.9
	79.5	4.968	73.47
	160.5	10.03	149.55
8 bits	3.5	0.219	2.74
	7.5	0.469	7.25
	12.5	0.781	12.88
	19.5	1.219	20.77
	39.5	2.469	43.32
	79.5	4.968	88.4
	160.5	10.03	179.7
6 bits	3.5	0.219	3.73
	7.5	0.469	9.36
	12.5	0.781	16.41
	19.5	1.219	26.27
	39.5	2.469	54.45
	79.5	4.968	110.8
	160.5	10.03	224.9

(1) Value guaranteed by design, not 100% tested in production.

Preliminary version
Confidential, under NDA for engineering evaluation only

For Internal Use

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

(2) The R_{AIN} value was calculated by theory and stray capacitance of actual pcb has not been taken into account.

Table 4-31. ADC accuracy at f_{ADC} = 16 MHz (1)(2)(3)

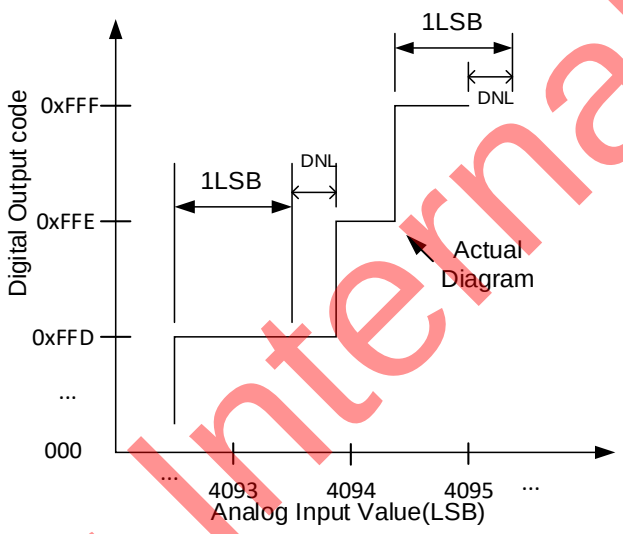
Symbol	Description	Test conditions(3)	Typ	Unit
EO	Offset error	V_{DD} = 5 V, f_{ADC} = 16 MHz, f_S < 1 Msps, T_A = 25 °C	TBD	LSB
DNL	Differential linearity error		TBD	
INL	Integral linearity error		TBD	
ENOB	Effective number of bits		TBD	Bits
SNDR	Signal-to-noise and distortion ratio		TBD	dB
SNR	Signal-to-noise ratio		TBD	
THD	Total harmonic distortion		TBD	

(1) Value guaranteed by characterization, not 100% tested in production.

(2) Some guidance is provided to improve the sampling accuracy of ADC. Refer to AN059 Methods to improve ADC sampling accuracy.

(3) Guaranteed by characterization results for QFN24 packages.

Figure 4-9. Differential linearity error

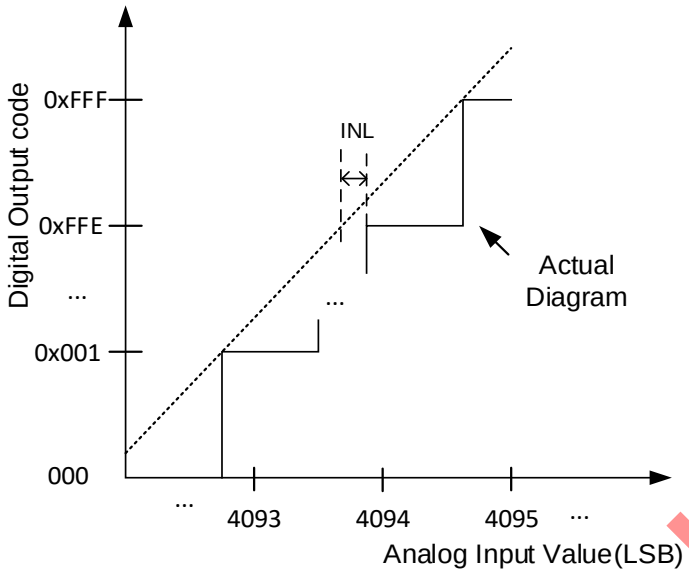


For Internal Use

Preliminary version
Confidential, under NDA for engineering evaluation only

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

Figure 4-10. Integral linearity error



4.18. TIMER characteristics

Table 4-32. TIMER characteristics (1)

Symbol	Description	Conditions	Min	Max	Unit
t_{RES}	Timer resolution time	—	1	—	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 48 MHz	20.833	—	ns
f_{EXT}	Timer external clock frequency	—	0	$f_{TIMERxCLK}$ /4	MHz
		$f_{TIMERxCLK}$ = 48 MHz	0	12	MHz
RES	Timer resolution	—	—	16	bit
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected	—	1	65536	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 48 MHz	0.0208	1365	μs
t_{MAX_COUNT}	Maximum possible count	—	—	65536 x65536	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 48 MHz	—	89.48	s

(1) Value guaranteed by design, not 100% tested in production.

For Internal Use

Preliminary version
Confidential, under NDA for engineering evaluation only

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

4.19. I2C characteristics

Table 4-33. I2C characteristics (1)(2)

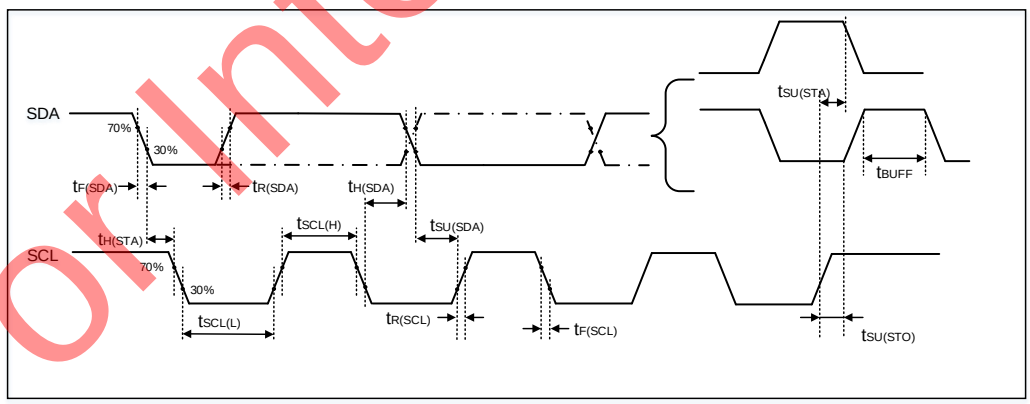
Symbol	Description	Conditions	Standard mode		Fast mode		Unit
			Min	Max	Min	Max	
$t_{SCL(H)}$	SCL clock high time	—	4.0	—	0.6	—	μs
$t_{SCL(L)}$	SCL clock low time	—	4.7	—	1.3	—	μs
$t_{SU(SDA)}$	SDA setup time	—	250	—	100	—	ns
$t_{H(SDA)}$	SDA data hold time	—	0 (3)	3450	0	900	ns
$t_{R(SDA/SCL)}$	SDA and SCL rise time	—	—	1000	—	300	ns
$t_{F(SDA/SCL)}$	SDA and SCL fall time	—	—	300	—	300	ns
$t_{H(STA)}$	Start condition hold time	—	4.0	—	0.6	—	μs
$t_{SU(STA)}$	Repeated Start condition setup time	—	4.7	—	0.6	—	μs
$t_{SU(STO)}$	Stop condition setup time	—	4.0	—	0.6	—	μs
t_{BUFF}	Stop to Start condition time (bus free)	—	4.7	—	1.3	—	μs

(1) Value guaranteed by design, not 100% tested in production.

(2) To ensure the standard mode I2C frequency, f_{PCLK} must be at least 2 MHz. To ensure the fast mode I2C frequency, f_{PCLK} must be at least 4 MHz.

(3) The device should provide a data hold time of 300 ns at least in order to bridge the undefined region of the falling edge of SCL.

Figure 4-11. I2C bus timing diagram



4.20. SPI characteristics

Table 4-34. Standard SPI characteristics (1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency	—	—	—	24	MHz

For Internal Use

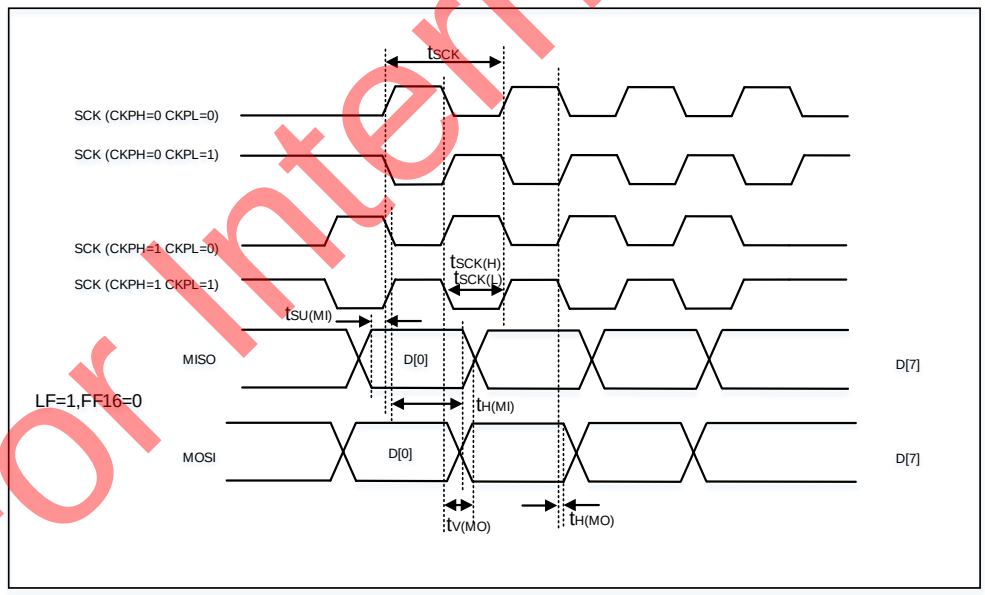
Preliminary version
Confidential, under NDA for engineering evaluation only

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

Symbol	Description	Conditions	Min	Typ	Max	Unit
$t_{SCK(H)}$	SCK clock high time	Master mode, f_{PCLK} = 48 MHz, presc = 2	—	20.761	—	ns
$t_{SCK\ (L)}$	SCK clock low time	Master mode, f_{PCLK} = 48 MHz, presc = 2	—	20.761	—	ns
SPI master mode						
$t_{V(MO)}$	Data output valid time	—	—	—	6.3	ns
$t_{H(MO)}$	Data output hold time	—	0	—	—	ns
$t_{SU(MI)}$	Data input setup time	—	1	—	—	ns
$t_{H(MI)}$	Data input hold time	—	2	—	—	ns
SPI slave mode						
$t_{SU(NSS)}$	NSS enable setup time	—	2	—	—	ns
$t_{H(NSS)}$	NSS enable hold time	—	3	—	—	ns
$t_{A(SO)}$	Data output access time	—	—	8	—	ns
$t_{DIS(SO)}$	Data output disable time	—	—	9	—	ns
$t_{V(SO)}$	Data output valid time	—	—	8	—	ns
$t_{SU(SI)}$	Data input setup time	—	2	—	—	ns
$t_{H(SI)}$	Data input hold time	—	3	—	—	ns

(1) Value guaranteed by design, not 100% tested in production.

Figure 4-12. SPI timing diagram - master mode



For Internal Use

Preliminary version
Confidential, under NDA for engineering evaluation only

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

Figure 4-13. SPI timing diagram - slave mode (CKPH=0)

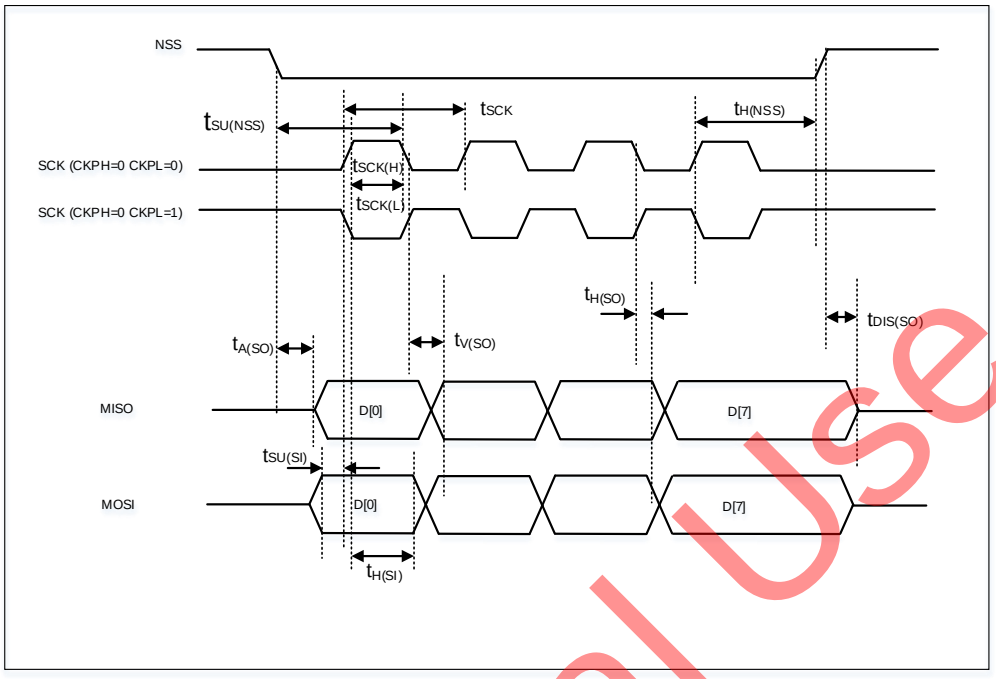
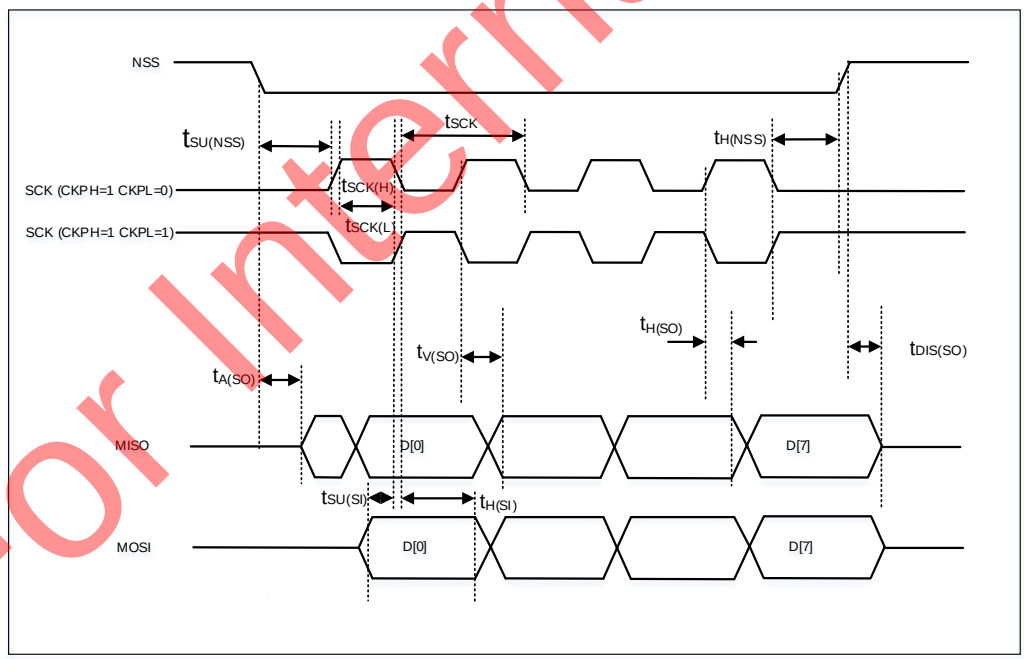


Figure 4-14. SPI timing diagram - slave mode (CKPH=1)



For Internal Use

4.21. USART characteristics

Table 4-35. USART characteristics in Synchronous mode (1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency	Master mode	—	—	6	MHz

Preliminary version
Confidential, under NDA for engineering evaluation only

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

Symbol	Description	Conditions	Min	Typ	Max	Unit
$t_{H(SCK)}$	SCK clock high time	Master mode	82.333	—	—	ns
$t_{L(SCK)}$	SCK clock low time	Master mode	82.333	—	—	ns
$t_{V(TX)}$	Data output valid time	Master mode	—	1	2	
$t_{H(TX)}$	Data output hold time	Master mode	0	—	—	

(1) Guaranteed by design, not 100% tested in production.

4.22. WDGT characteristics

Table 4-36. FWDGT min/max timeout period at 32 kHz (IRC32K) (1)

Prescaler divider	PSC[2:0] bits	Min timeout RLD[11:0]= 0x000	Max timeout RLD[11:0]= 0xFFF	Unit
1/4	000	0.03125	511.90625	ms
1/8	001	0.03125	1023.78125	
1/16	010	0.03125	2047.53125	
1/32	011	0.03125	4095.03125	
1/64	100	0.03125	8190.03125	
1/128	101	0.03125	16380.03125	
1/256	110 or 111	0.03125	32760.03125	

(1) Value guaranteed by design, not 100% tested in production.

Table 4-37. WWDGT min-max timeout value at 48 MHz (f_{PCLK}) (1)

Prescaler divider	PSC[3:0]	Min timeout value CNT[6:0] = 0x40	Unit	Max timeout value CNT[6:0] = 0x7F	Unit
1/1	0000	85.33	µs	5.461	ms
1/2	0001	170.67		10.923	
1/4	0010	341.33		21.845	
1/8	0011	682.67		43.691	
1/16	0100	1.365	ms	87.382	
1/32	0101	2.731		174.764	
1/64	0110	5.461		349.528	
1/128	0111	10.922		699.056	
1/256	1000	21.854		1398.112	
1/512	1001	43.691		2796.224	
1/1024	1010	87.381		5592.448	
1/2048	1011	174.763		11184.896	
1/4096	1100	349.525		22369.792	
1/8192	1101	699.051		44739.584	
1/1	1110	85.33	µs	5.461	
1/1	1111	85.33		5.461	

(1) Value guaranteed by design, not 100% tested in production.

For Internal Use

Preliminary version
Confidential, under NDA for engineering evaluation only

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

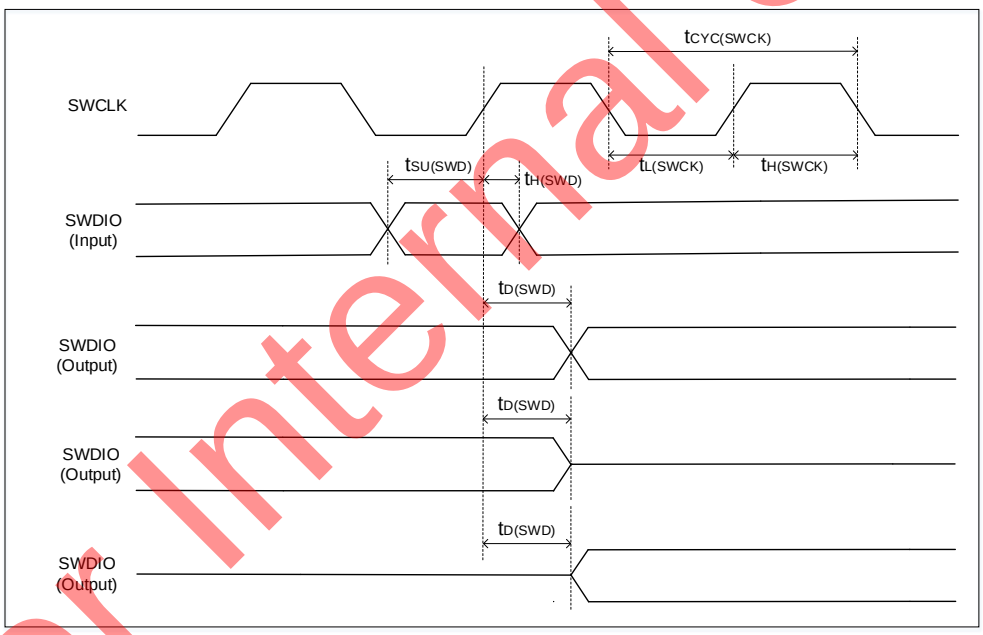
4.23. SWD Timing

Table 4-38. SWD Interface Timing (1)

Symbol	Description	Min	Max	Unit
$t_{CYC(SWCK)}$	SWCLK clock cycle time	40	—	ns
$t_{H(SWCK)}$	SWCLK clock high pulse width	17	—	ns
$t_{L(SWCK)}$	SWCLK clock low pulse width	17	—	ns
$t_{R(SWCK)}$	SWCLK clock rise time	—	1	ns
$t_{F(SWCK)}$	SWCLK clock fall time	—	1	ns
$t_{SU(SWD)}$	SWDIO setup time	15	—	ns
$t_{H(SWD)}$	SWDIO hold time	1	—	ns
$t_{D(SWD)}$	SWDIO data delay time	10	12	ns

(1) Guaranteed by design, not 100% tested in production

Figure 4-15. SWD SWCLK Timings



For Internal Use

Preliminary version
Confidential, under NDA for engineering evaluation only

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

5 Package information

5.1 QFN24 package outline dimensions

Figure 5-1. QFN24 package outline

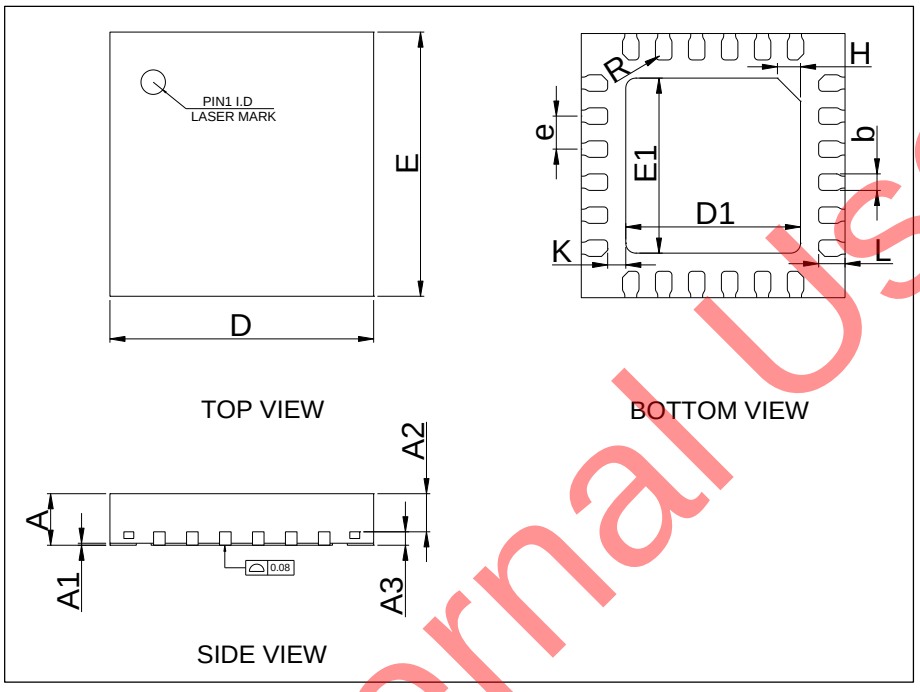


Table 5-1. QFN24 package dimensions

Symbol	Min	Typ	Max
A	0.70	0.75	0.80
A1	0	0.02	0.05
A2	0.50	0.55	0.60
A3	—	0.203	—
b	0.20	0.25	0.30
D	3.90	4.00	4.10
D1	2.20	2.25	2.30
E	3.90	4.00	4.10
E1	2.20	2.25	2.30
e	—	0.50	—
H	—	0.35	—
K	—	0.475	—
L	0.35	0.40	0.45
R	—	0.09	—

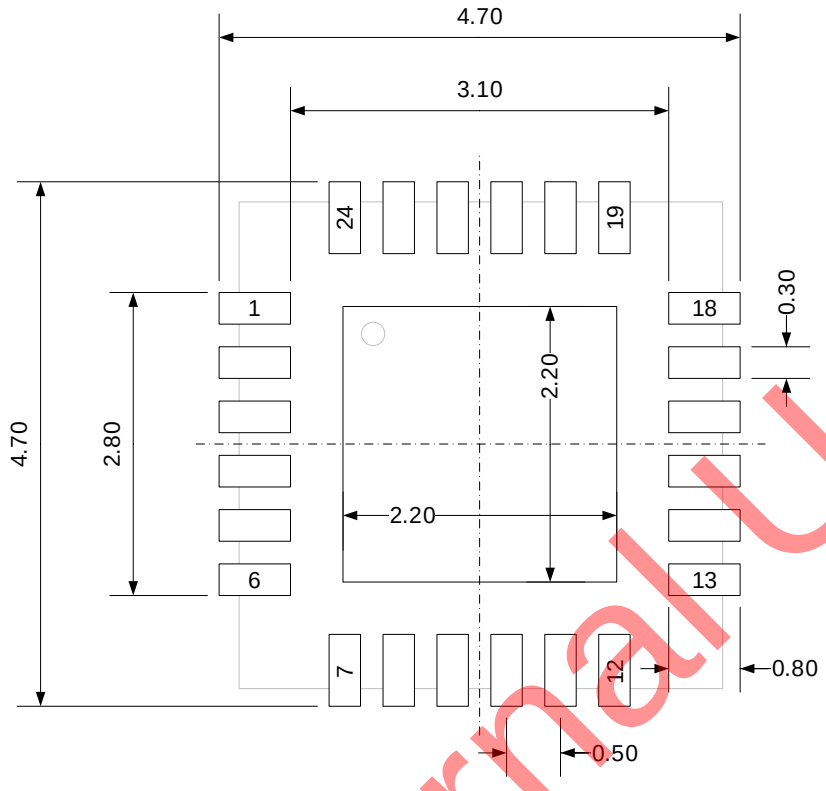
(Original dimensions are in millimeters)

For Internal Use

Preliminary version
Confidential, under NDA for engineering evaluation only

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

Figure 5-2. QFN24 recommended footprint



(Original dimensions are in millimeters)

For Internal Use

Preliminary version
Confidential, under NDA for engineering evaluation only

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

5.2 TSSOP24 package outline dimensions

Figure 5-3. TSSOP24 package outline

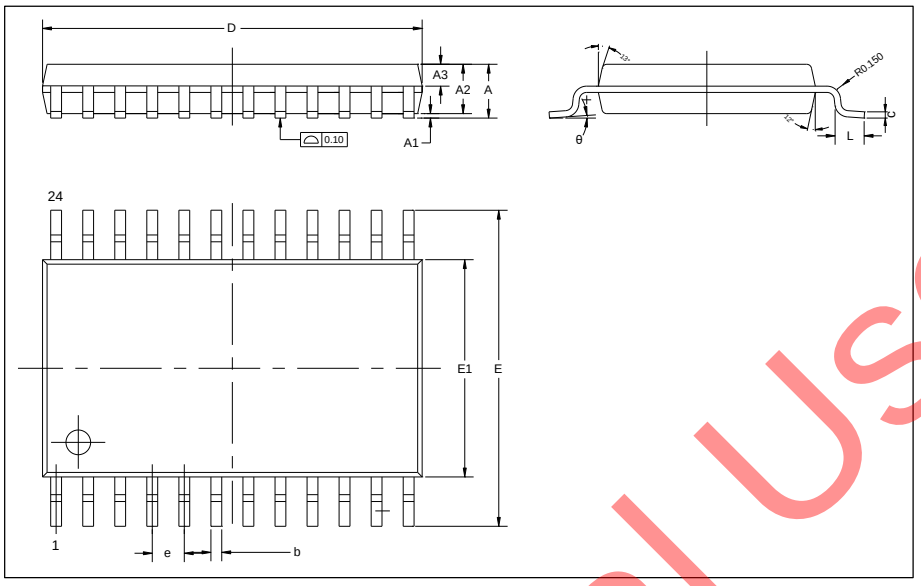


Table 5-2. TSSOP24 package dimensions

Symbol	Min	Typ	Max
A	—	—	1.20
A1	0.05	—	0.15
A2	0.80	0.90	1.00
A3	0.34	0.39	0.44
b	0.19	—	0.30
c	0.09	—	0.20
D	7.70	7.80	7.90
E	6.25	6.40	6.55
E1	4.30	4.40	4.50
e	—	0.65	—
L	0.45	—	0.75
θ	0°	—	8°

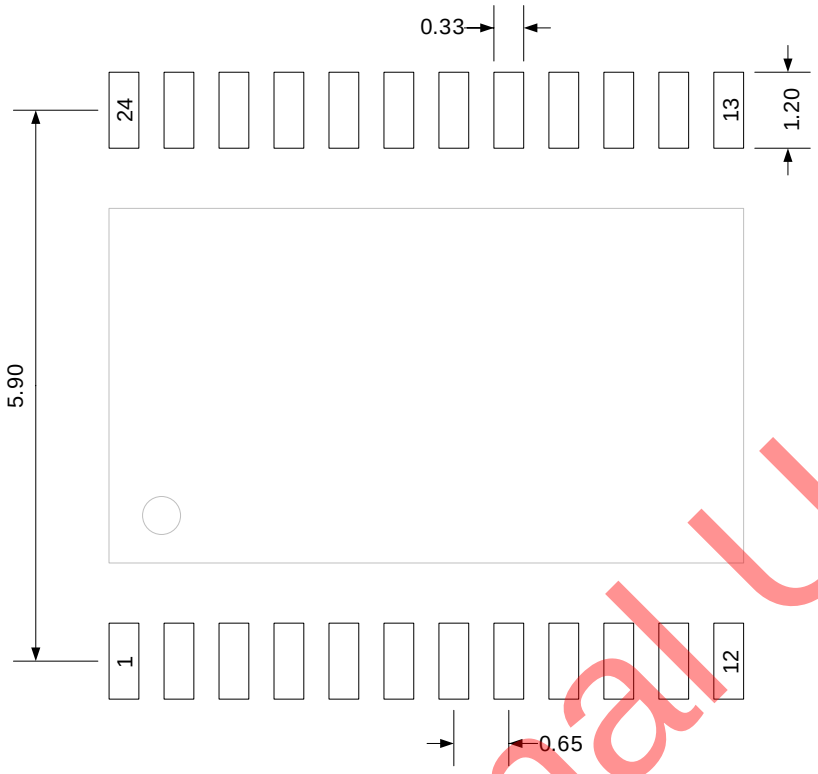
(Original dimensions are in millimeters)

For Internal Use

Preliminary version
Confidential, under NDA for engineering evaluation only

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

Figure 5-4. TSSOP24 recommended footprint



(Original dimensions are in millimeters)

For Internal Use

Preliminary version
Confidential, under NDA for engineering evaluation only

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

5.3 QFN20 package outline dimensions

Figure 5-5. QFN20 package outline

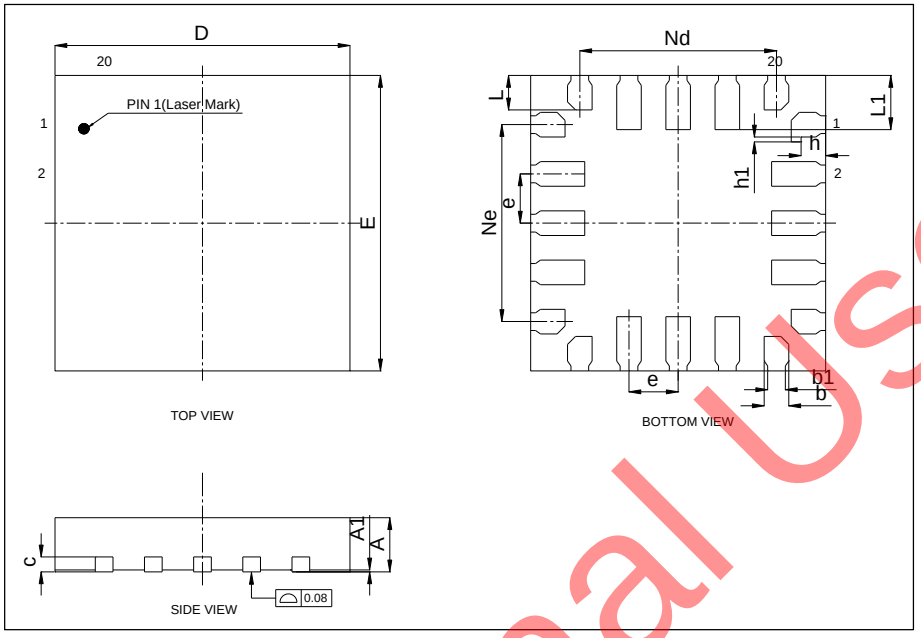


Table 5-3. QFN20 package dimensions

Symbol	Min	Typ	Max
A	0.50	0.55	0.60
A1	0	0.02	0.05
b	0.20	0.25	0.30
b1	—	0.18	—
c	—	0.152	—
D	2.90	3.00	3.10
E	2.90	3.00	3.10
e	—	0.50	—
h	0.20	0.25	0.30
h1	—	0.05	—
L	0.30	0.35	0.40
L1	0.50	0.55	0.60
Nd	—	2.00	—
Ne	—	2.00	—

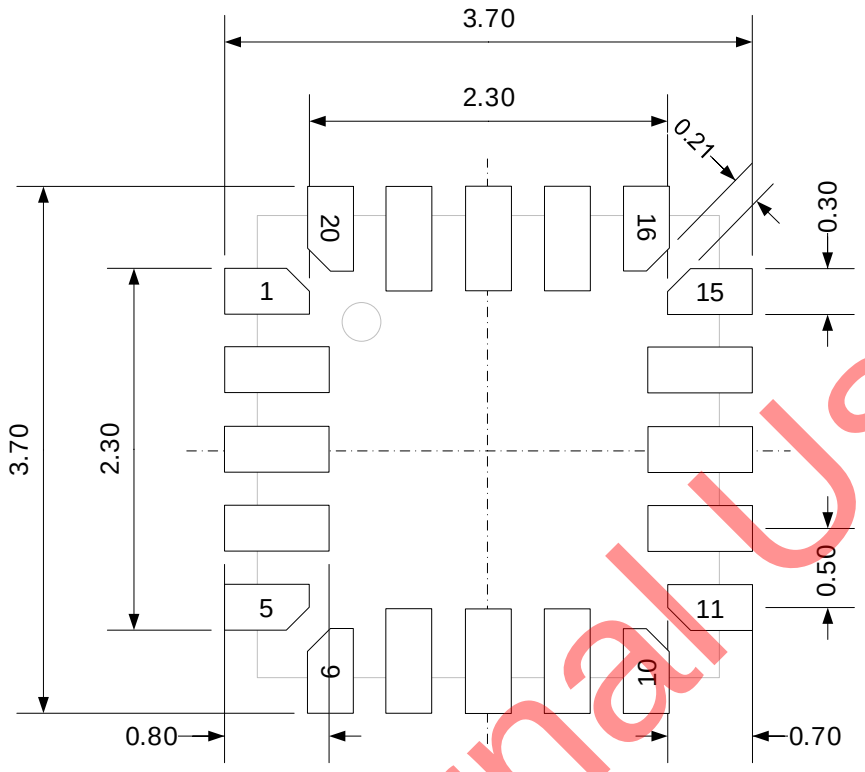
(Original dimensions are in millimeters)

For Internal Use

Preliminary version
Confidential, under NDA for engineering evaluation only

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

Figure 5-6. QFN20 recommended footprint



(Original dimensions are in millimeters)

For Internal Use

Preliminary version
Confidential, under NDA for engineering evaluation only

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

5.4 TSSOP20 package outline dimensions

Figure 5-7. TSSOP20 package outline

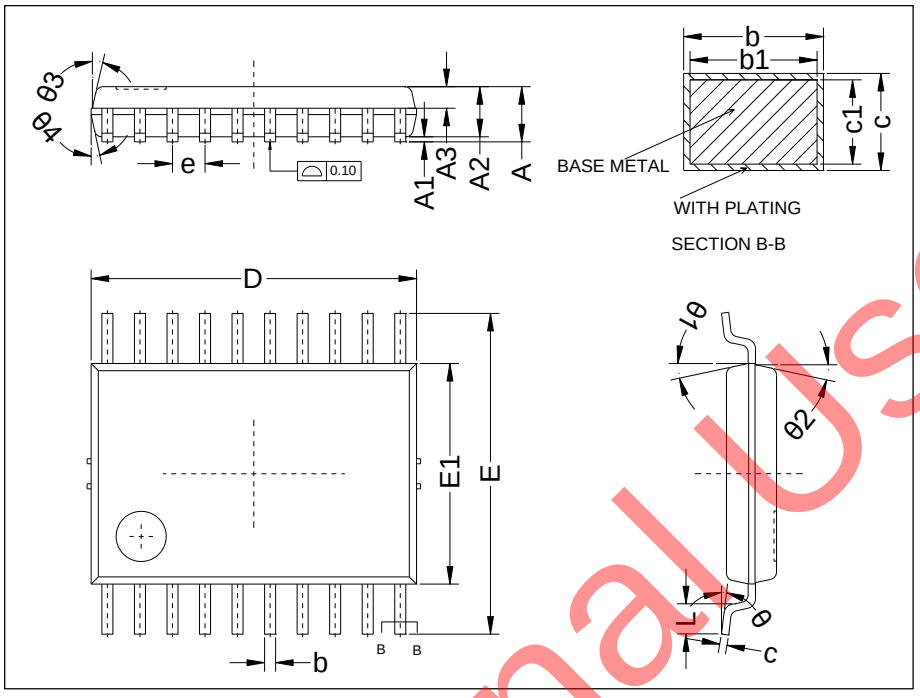


Table 5-4. TSSOP20 package dimensions

Symbol	Min	Typ	Max
A	—	—	1.20
A1	0.05	0.10	0.15
A2	0.80	1.00	1.05
A3	0.38	0.43	0.48
b	0.17	—	0.27
b1	0.16	0.22	0.26
c	0.13	—	0.15
c1	0.12	0.13	0.14
D	6.40	6.50	6.60
E	6.25	6.40	6.55
E1	4.30	4.40	4.50
e	—	0.65	—
L	0.45	0.60	0.75
θ	0°	—	8°
θ1	10°	—	14°
θ2	10°	—	14°
θ3	10°	—	14°
θ4	10°	—	14°

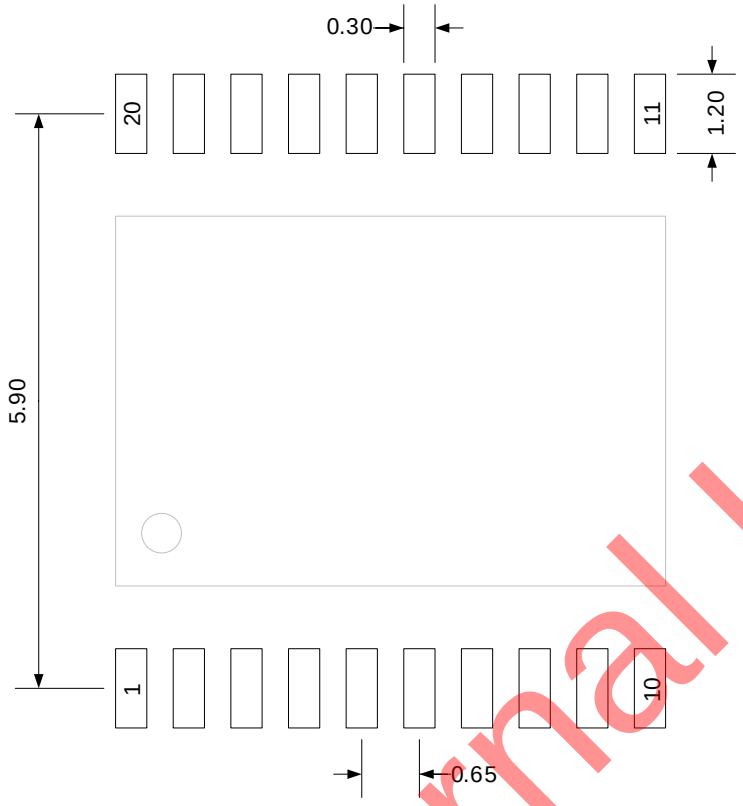
For Internal Use

Preliminary version
Confidential, under NDA for engineering evaluation only

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

(Original dimensions are in millimeters)

Figure 5-8. TSSOP20 recommended footprint



(Original dimensions are in millimeters)

For Internal Use

Preliminary version
Confidential, under NDA for engineering evaluation only

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

5.5 SOP8 package outline dimensions

Figure 5-9. SOP8 package outline

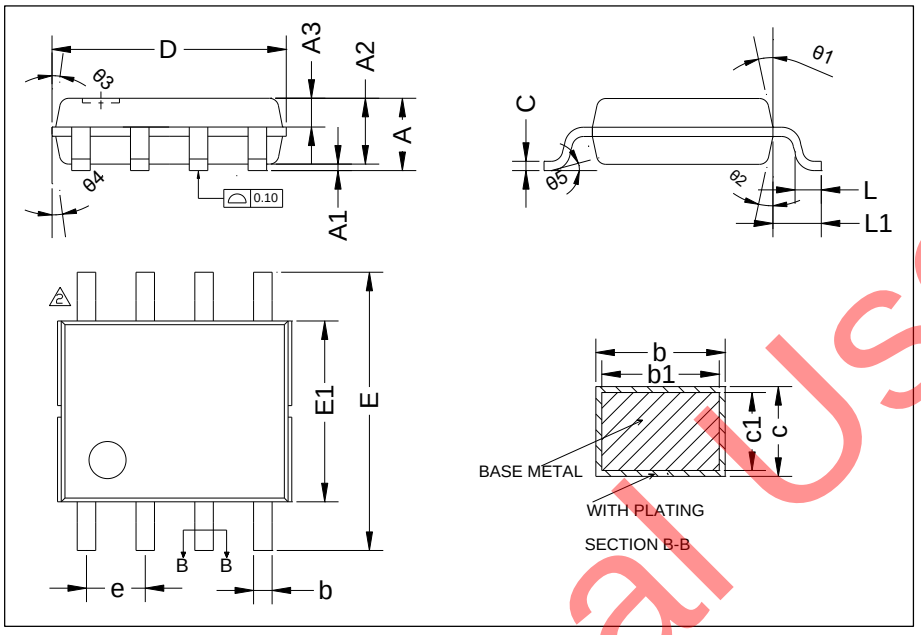


Table 5-5. SOP8 package dimensions

Symbol	Min	Typ	Max
A	—	—	1.65
A1	0.10	—	0.25
A2	1.40	1.42	1.50
A3	0.57	0.62	0.67
b	0.33	—	0.47
b1	0.32	0.41	0.44
c	0.20	—	0.24
c1	0.19	0.20	0.21
D	4.80	4.90	5.00
E	5.90	6.00	6.20
E1	3.85	3.90	4.00
e	—	1.27	—
L	0.50	0.60	0.70
L1	—	1.05	—
θ1	9°	—	15°
θ2	9°	—	15°
θ3	8°	—	14°
θ4	8°	—	14°
θ5	0°	—	6°

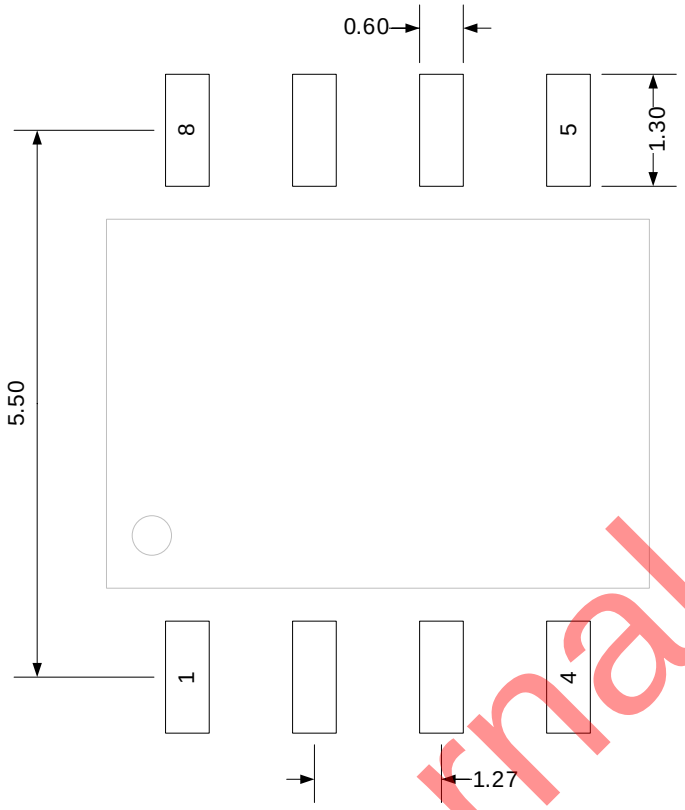
For Internal Use

Preliminary version
Confidential, under NDA for engineering evaluation only

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

(Original dimensions are in millimeters)

Figure 5-10. SOP8 recommended footprint



(Original dimensions are in millimeters)

For Internal Use

Preliminary version
Confidential, under NDA for engineering evaluation only

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

5.6 Thermal characteristics

Thermal resistance is used to characterize the thermal performance of the package device, which is represented by the Greek letter “θ”. For semiconductor devices, thermal resistance represents the steady-state temperature rise of the chip junction due to the heat dissipated on the chip surface.

θ_{JA}: Thermal resistance, junction-to-ambient.

θ_{JB}: Thermal resistance, junction-to-board.

θ_{JC}: Thermal resistance, junction-to-case.

Ψ_{JB}: Thermal characterization parameter, junction-to-board.

Ψ_{JT}: Thermal characterization parameter, junction-to-top center.

$$\theta_{JA}=(T_J-T_A)/P_D \quad (5\text{-}1)$$

$$\theta_{JB}=(T_J-T_B)/P_D \quad (5\text{-}2)$$

$$\theta_{JC}=(T_J-T_C)/P_D \quad (5\text{-}3)$$

Where, T_J = Junction temperature.

T_A = Ambient temperature

T_B = Board temperature

T_C = Case temperature which is monitoring on package surface

P_D = Total power dissipation

θ_{JA} represents the resistance of the heat flows from the heating junction to ambient air. It is an indicator of package heat dissipation capability. Lower θ_{JA} can be considerate as better overall thermal performance. θ_{JA} is generally used to estimate junction temperature.

θ_{JB} is used to measure the heat flow resistance between the chip surface and the PCB board.

θ_{JC} represents the thermal resistance between the chip surface and the package top case. θ_{JC} is mainly used to estimate the heat dissipation of the system (using heat sink or other heat dissipation methods outside the device package).

Table 5-6. Package thermal characteristics(1)

Symbol	Condition	Package	Value	Unit
θ_{JA}	Natural convection, 2S2P PCB	QFN24		°C/W
		TSSOP24		
		QFN20		
		TSSOP20		
		SOP8		
θ_{JB}	Cold plate, 2S2P PCB	QFN24		°C/W

Preliminary version
Confidential, under NDA for engineering evaluation only

For Internal Use

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

Symbol	Condition	Package	Value	Unit
		TSSOP24		
		QFN20		
		TSSOP20		
		SOP8		
θ_{JC}	Cold plate, 2S2P PCB	QFN24		°C/W
		TSSOP24		
		QFN20		
		TSSOP20		
		SOP8		
Ψ_{JB}	Natural convection, 2S2P PCB	QFN24		°C/W
		TSSOP24		
		QFN20		
		TSSOP20		
		SOP8		
Ψ_{JT}	Natural convection, 2S2P PCB	QFN24		°C/W
		TSSOP24		
		QFN20		
		TSSOP20		
		SOP8		

(1) Thermal characteristics are based on simulation, and meet JEDEC specification.

For Internal Use

Preliminary version
Confidential, under NDA for engineering evaluation only

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

6 Ordering information

Table 6-1. Part ordering code for GD32C211xx devices

Ordering code	Flash (KB)	Package	Package type	Temperature operating range
GD32C211E6U6TR	32	QFN24	Green	Industrial -40°C to +85°C
GD32C211E4U6TR	16	QFN24	Green	Industrial -40°C to +85°C
GD32C211E6P6TR	32	TSSOP24	Green	Industrial -40°C to +85°C
GD32C211E4P6TR	16	TSSOP24	Green	Industrial -40°C to +85°C
GD32C211F6U6TR	32	QFN20	Green	Industrial -40°C to +85°C
GD32C211F4U6TR	16	QFN20	Green	Industrial -40°C to +85°C
GD32C211F6P6TR	32	TSSOP20	Green	Industrial -40°C to +85°C
GD32C211F4P6TR	16	TSSOP20	Green	Industrial -40°C to +85°C
GD32C211J6M6TR	32	SOP8	Green	Industrial -40°C to +85°C
GD32C211J4M6TR	16	SOP8	Green	Industrial -40°C to +85°C

For Internal Use

Preliminary version
Confidential, under NDA for engineering evaluation only

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

7 Revision history

Table 7-1. Revision history

Revision No.	Description	Date
0.0	Initial Release	May 30, 2025

For Internal Use

Preliminary version
Confidential, under NDA for engineering evaluation only

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

Important Notice

This document is the property of GigaDevice Semiconductor Inc. and its subsidiaries (the "Company"). This document, including any product of the Company described in this document (the “Product”), is owned by the Company according to the laws of the People’s Republic of China and other applicable laws. The Company reserves all rights under such laws and no Intellectual Property Rights are transferred (either wholly or partially) or licensed by the Company (either expressly or impliedly) herein. The names and brands of third party referred thereto (if any) are the property of their respective owner and referred to for identification purposes only.

To the maximum extent permitted by applicable law, the Company makes no representations or warranties of any kind, express or implied, with regard to the merchantability and the fitness for a particular purpose of the Product, nor does the Company assume any liability arising out of the application or use of any Product. Any information provided in this document is provided only for reference purposes. It is the sole responsibility of the user of this document to determine whether the Product is suitable and fit for its applications and products planned, and properly design, program, and test the functionality and safety of its applications and products planned using the Product. The Product is designed, developed, and/or manufactured for ordinary business, industrial, personal, and/or household applications only, and the Product is not designed or intended for use in (i) safety critical applications such as weapons systems, nuclear facilities, atomic energy controller, combustion controller, aeronautic or aerospace applications, traffic signal instruments, pollution control or hazardous substance management; (ii) life-support systems, other medical equipment or systems (including life support equipment and surgical implants); (iii) automotive applications or environments, including but not limited to applications for active and passive safety of automobiles (regardless of front market or aftermarket), for example, EPS, braking, ADAS (camera/fusion), EMS, TCU, BMS, BSG, TPMS, Airbag, Suspension, DMS, ICMS, Domain, ESC, DCDC, e-clutch, advanced-lighting, etc.. Automobile herein means a vehicle propelled by a self-contained motor, engine or the like, such as, without limitation, cars, trucks, motorcycles, electric cars, and other transportation devices; and/or (iv) other uses where the failure of the device or the Product can reasonably be expected to result in personal injury, death, or severe property or environmental damage (collectively "Unintended Uses"). Customers shall take any and all actions to ensure the Product meets the applicable laws and regulations. The Company is not liable for, in whole or in part, and customers shall hereby release the Company as well as its suppliers and/or distributors from, any claim, damage, or other liability arising from or related to all Unintended Uses of the Product. Customers shall indemnify and hold the Company, and its officers, employees, subsidiaries, affiliates as well as its suppliers and/or distributors harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of the Product.

Information in this document is provided solely in connection with the Product. The Company reserves the right to make changes, corrections, modifications or improvements to this document and the Product described herein at any time without notice. The Company shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to them. Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2025 GigaDevice Semiconductor Inc. – All rights reserved

Preliminary version
Confidential, under NDA for engineering evaluation only

For Internal Use

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com