GD25LQ40E/20E

DATASHEET

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1 FEATURES

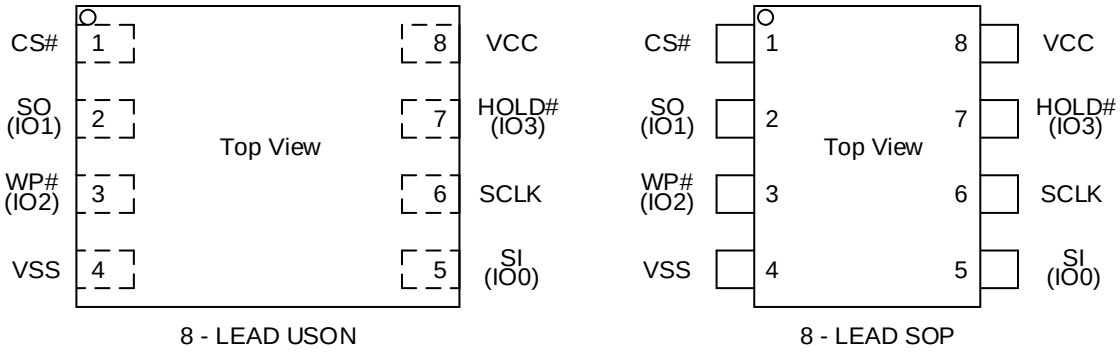
- 4M/2M-bit Serial Flash
  - 512K/256K-Byte
  - 256 Bytes per programmable page
- Standard, Dual, Quad SPI
  - Standard SPI: SCLK, CS#, SI, SO, WP#, HOLD#
  - Dual SPI: SCLK, CS#, IO0, IO1, WP#, HOLD#
  - Quad SPI: SCLK, CS#, IO0, IO1, IO2, IO3
- High Speed Clock Frequency
  - 133MHz for fast read
  - Dual I/O Data transfer up to 266Mbits/s
  - Quad I/O Data transfer up to 532Mbits/s
- Software/Hardware Write Protection
  - Write protect all/portion of memory via software
  - Enable/Disable protection with WP# Pin
  - Top/Bottom Block protection
- Endurance and Data Retention
  - Minimum 100,000 Program/Erase Cycles
  - 20-year data retention typical
- Allows XiP (eXecute In Place) Operation
  - High speed Read reduce overall XiP instruction fetch time
  - Continuous Read with Wrap further reduce data latency to fill up SoC cache
- Fast Program/Erase Speed
  - Page Program time: 0.4ms typical
  - Sector Erase time: 40ms typical
  - Block Erase time: 0.15s/0.2s typical
  - Chip Erase time: 1s/0.5s typical
- Flexible Architecture
  - Uniform Sector of 4K-Byte
  - Uniform Block of 32/64K-Byte
- Low Power Consumption
  - 10μA typical standby current
  - 1μA typical deep power down current
- Advanced Security Features
  - 128-bit Unique ID for each device
  - Serial Flash Discoverable parameters (SFDP) register
  - 3x512-Byte Security Registers With OTP Locks
- Single Power Supply Voltage
  - Full voltage range: 1.65-2.0V
- Package Information
  - SOP8 150mil
  - SOP8 208mil
  - USON8 (1.5x1.5mm)
  - USON8 (3x2mm)
  - USON8 (3x4mm)

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2 GENERAL DESCRIPTIONS

The GD25LQ40E/20E (4M/2M-bit) Serial flash supports the standard Serial Peripheral Interface (SPI), and the Dual/Quad SPI: Serial Clock, Chip Select, Serial Data I/O0 (SI), I/O1 (SO), I/O2 (WP#), I/O3 (HOLD#). The Dual I/O data is transferred with speed of 266Mbit/s, and the Quad I/O data is transferred with speed of 532Mbit/s.

CONNECTION DIAGRAM



PIN DESCRIPTION

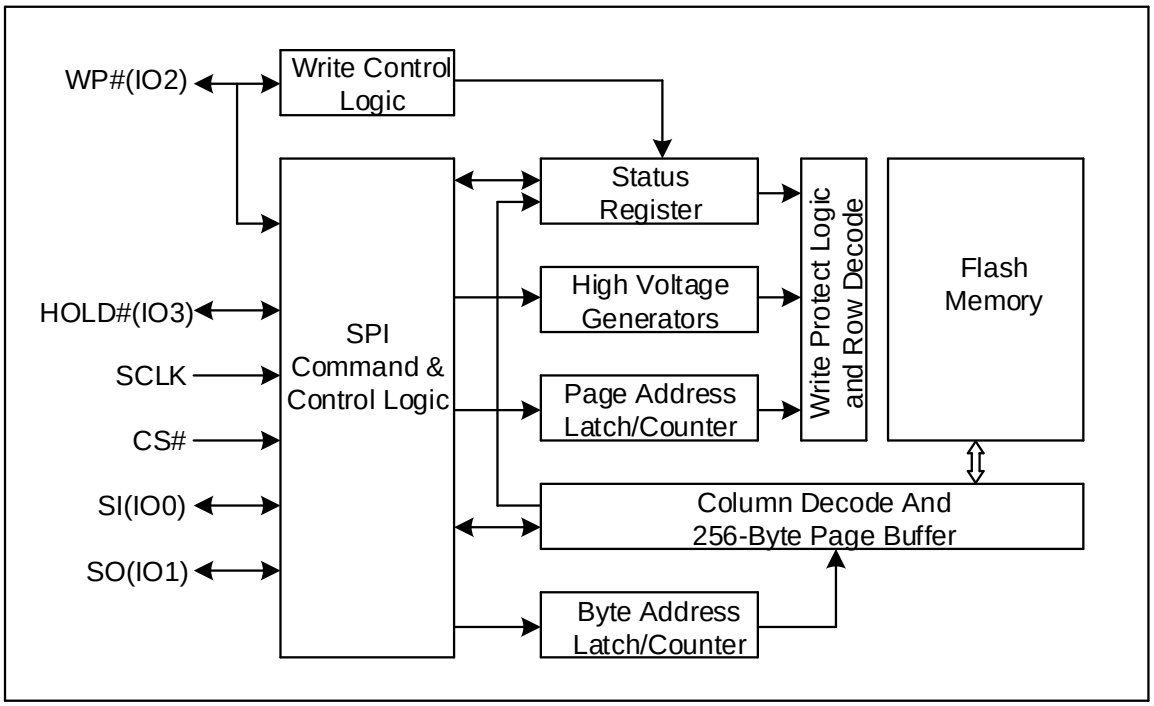
Table 1. Pin Description for SOP8/USON8 Package

Pin No.	Pin Name	I/O	Description
1	CS#	I	Chip Select Input
2	SO (IO1)	I/O	Data Output (Data Input Output 1)
3	WP# (IO2)	I/O	Write Protect Input (Data Input Output 2)
4	VSS		Ground
5	SI (IO0)	I/O	Data Input (Data Input Output 0)
6	SCLK	I	Serial Clock Input
7	HOLD# (IO3)	I/O	Hold Input (Data Input Output 3)
8	VCC		Power Supply

Note: CS# must be driven high if chip is not selected. Please don't leave CS# floating any time after power is on.

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BLOCK DIAGRAM



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3 MEMORY ORGANIZATION

GD25LQ40E

Each device has	Each block has	Each sector has	Each page has	
512K	64/32K	4K	256	Bytes
2K	256/128	16	-	pages
128	16/8	-	-	sectors
8/16	-	-	-	blocks

GD25LQ20E

Each device has	Each block has	Each sector has	Each page has	
256K	64/32K	4K	256	Bytes
1K	256/128	16	-	pages
64	16/8	-	-	sectors
4/8	-	-	-	blocks

UNIFORM BLOCK SECTOR ARCHITECTURE

GD25LQ40E 64K Bytes Block Sector Architecture

Block	Sector	Address range	
7	127	07F000H	07FFFFH
	.....	.....	.....
	112	070000H	070FFFH
6	111	06F000H	06FFFFH
	.....	.....	.....
	96	060000H	060FFFH
.....	.....	.....	.....
	.....	.....	.....
	.....	.....	.....
.....	.....	.....	.....
	.....	.....	.....
	.....	.....	.....
2	47	02F000H	02FFFFH
	.....	.....	.....
	32	020000H	020FFFH
1	31	01F000H	01FFFFH
	.....	.....	.....
	16	010000H	010FFFH
0	15	00F000H	00FFFFH
	.....	.....	.....
	0	000000H	000FFFH

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GD25LQ20E 64K Bytes Block Sector Architecture

Block	Sector	Address range	
3	64	03F000H	03FFFFH
	.....	.....	.....
	.....	.....	.....
2	47	02F000H	02FFFFH
	.....	.....	.....
	32	020000H	020FFFH
1	31	01F000H	01FFFFH
	.....	.....	.....
	16	010000H	010FFFH
0	15	00F000H	00FFFFH
	.....	.....	.....
	0	000000H	000FFFH

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4 DEVICE OPERATIONS

4.1 SPI Mode

Standard SPI

The GD25LQ40E/20E features a serial peripheral interface on 4 signals bus: Serial Clock (SCLK), Chip Select (CS#), Serial Data Input (SI) and Serial Data Output (SO). Both SPI bus mode 0 and 3 are supported. Input data is latched on the rising edge of SCLK and data shifts out on the falling edge of SCLK.

Dual SPI

The GD25LQ40E/20E supports Dual SPI operation when using the “Dual Output Fast Read” and “Dual I/O Fast Read” (3BH and BBH) commands. These commands allow data to be transferred to or from the device at twice the rate of the standard SPI. When using the Dual SPI commands, the SI and SO pins become bidirectional I/O pins: IO0 and IO1.

Quad SPI

The GD25LQ40E/20E supports Quad SPI operation when using the “Quad Output Fast Read”, “Quad I/O Fast Read” (6BH, EBH) commands. These commands allow data to be transferred to or from the device at four times the rate of the standard SPI. When using the Quad SPI commands, the SI and SO pins become bidirectional I/O pins: IO0 and IO1, and the WP# and HOLD# pins become bidirectional I/O pins: IO2 and IO3. The Quad SPI commands require the non-volatile Quad Enable bit (QE) in Status Register set to 1.

4.2 HOLD Function

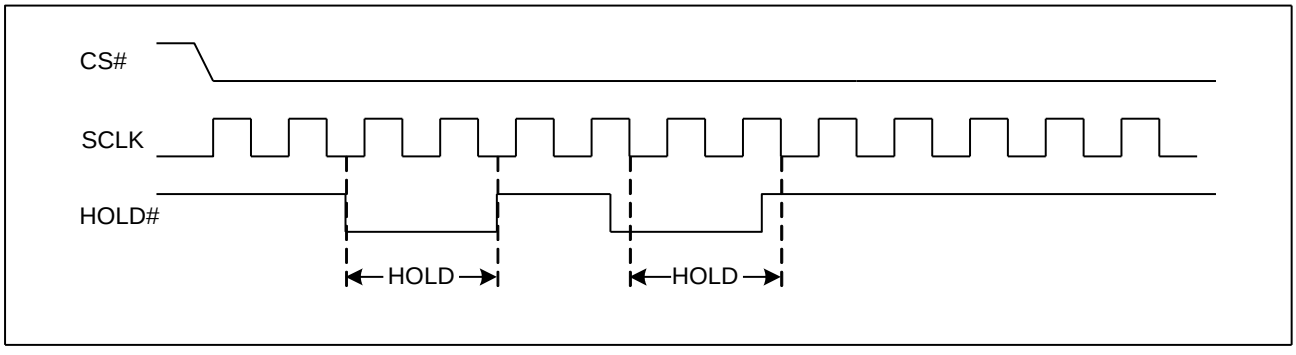
The HOLD function is available when QE=0. If QE=1, The HOLD function is disabled, and the HOLD# pin acts as dedicated data I/O pin.

The HOLD# signal goes low to stop any serial communications with the device, except the operation of write status register, programming, or erasing in progress.

The operation of HOLD needs CS# keep low, and starts on falling edge of the HOLD# signal, with SCLK signal being low. If SCLK is not low, HOLD operation will not start until SCLK is low. The HOLD condition ends on rising edge of HOLD# signal with SCLK being low. If SCLK is not low, HOLD operation will not end until SCLK is low.

The SO is high impedance, both SI and SCLK don’t care during the HOLD operation. If CS# is driven high during HOLD operation, it will reset the internal logic of the device. To re-start communication with the chip, the HOLD# must be at high and then CS# must be at low.

Figure 1 HOLD Condition



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5 DATA PROTECTION

The GD25LQ40E/20E provide the following data protection methods:

- Write Enable (WREN) command: The WREN command is set the Write Enable Latch bit (WEL). The WEL bit will return to reset by the following situation:
  -Power-Up / Software Reset (66H+99H)
  -Write Disable (WRDI)
  -Write Status Register (WRSR)
  -Page Program (PP)
  -Sector Erase (SE) / Block Erase (BE) / Chip Erase (CE)
- Software Protection Mode: The Block Protect bits (BP4-BP0) define the section of the memory array that can be read but not changed.
- Hardware Protection Mode: WP# goes low to protect the Block Protect bits (BP4-BP0) and the SRP bits (SRP1 and SRP0).
- Deep Power-Down Mode: In Deep Power-Down Mode, all commands are ignored except the Release from Deep Power-Down Mode command and Software Reset (66H+99H).
- Write Inhibit Voltage (VWI): Device would reset automatically when VCC is below a certain threshold VWI.

Table 2. GD25LQ40E Protected area size (CMP=0)

Status Register Content					Memory Content			
BP4	BP3	BP2	BP1	BP0	Blocks	Addresses	Density	Portion
X	X	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	1	7	070000H-07FFFFH	64KB	Upper 1/8
0	0	0	1	0	6 and 7	060000H-07FFFFH	128KB	Upper 1/4
0	0	0	1	1	4 to 7	040000H-07FFFFH	256KB	Upper 1/2
0	1	0	0	1	0	000000H-00FFFFH	64KB	Lower 1/8
0	1	0	1	0	0 and 1	000000H-01FFFFH	128KB	Lower 1/4
0	1	0	1	1	0 to 3	000000H-03FFFFH	256KB	Lower 1/2
0	X	1	X	X	0 to 7	000000H-07FFFFH	512KB	ALL
1	0	0	0	1	7	07F000H-07FFFFH	4KB	Upper 1/128
1	0	0	1	0	7	07E000H-07FFFFH	8KB	Upper 1/64
1	0	0	1	1	7	07C000H-07FFFFH	16KB	Upper 1/32
1	0	1	0	X	7	078000H-07FFFFH	32KB	Upper 1/16
1	0	1	1	0	7	078000H-07FFFFH	32KB	Upper 1/16
1	1	0	0	1	0	000000H-000FFFH	4KB	Lower 1/128
1	1	0	1	0	0	000000H-001FFFH	8KB	Lower 1/64
1	1	0	1	1	0	000000H-003FFFH	16KB	Lower 1/32
1	1	1	0	X	0	000000H-007FFFH	32KB	Lower 1/16
1	1	1	1	0	0	000000H-007FFFH	32KB	Lower 1/16
1	X	1	1	1	0 to 7	000000H-07FFFFH	512KB	ALL

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Table 3. GD25LQ40E Protected area size (CMP=1)

Status Register Content					Memory Content			
BP4	BP3	BP2	BP1	BP0	Blocks	Addresses	Density	Portion
X	X	0	0	0	0 to 7	000000H-07FFFFH	512KB	ALL
0	0	0	0	1	0 to 6	000000H-06FFFFH	448KB	Lower 7/8
0	0	0	1	0	0 to 5	000000H-05FFFFH	384KB	Lower 3/4
0	0	0	1	1	0 to 3	000000H-03FFFFH	256KB	Lower 1/2
0	1	0	0	1	1 to 7	010000H-07FFFFH	448KB	Upper 7/8
0	1	0	1	0	2 to 7	020000H-07FFFFH	384KB	Upper 3/4
0	1	0	1	1	4 to 7	040000H-07FFFFH	256KB	Upper 1/2
0	X	1	X	X	NONE	NONE	NONE	NONE
1	0	0	0	1	0 to 7	000000H-07EFFFH	508KB	Lower 127/128
1	0	0	1	0	0 to 7	000000H-07DFFFH	504KB	Lower 63/64
1	0	0	1	1	0 to 7	000000H-07BFFFH	496KB	Lower 31/32
1	0	1	0	X	0 to 7	000000H-077FFFH	480KB	Lower 15/16
1	0	1	1	0	0 to 7	000000H-077FFFH	480KB	Lower 15/16
1	1	0	0	1	0 to 7	001000H-07FFFFH	508KB	Upper 127/128
1	1	0	1	0	0 to 7	002000H-07FFFFH	504KB	Upper 63/64
1	1	0	1	1	0 to 7	004000H-07FFFFH	496KB	Upper 31/32
1	1	1	0	X	0 to 7	008000H-07FFFFH	480KB	Upper 15/16
1	1	1	1	0	0 to 7	008000H-07FFFFH	480KB	Upper 15/16
1	X	1	1	1	NONE	NONE	NONE	NONE

Table 4. GD25LQ20E Protected area size (CMP=0)

Status Register Content					Memory Content			
BP4	BP3	BP2	BP1	BP0	Blocks	Addresses	Density	Portion
0	X	X	0	0	NONE	NONE	NONE	NONE
0	0	X	0	1	3	030000H-03FFFFH	64KB	Upper 1/4
0	0	X	1	0	2 and 3	020000H-03FFFFH	128KB	Upper 1/2
0	1	X	0	1	0	000000H-00FFFFH	64KB	Lower 1/4
0	1	X	1	0	0 and 1	000000H-01FFFFH	128KB	Lower 1/2
0	X	X	1	1	0 to 3	000000H-03FFFFH	256KB	ALL
1	X	0	0	0	NONE	NONE	NONE	NONE
1	0	0	0	1	3	03F000H-03FFFFH	4KB	Upper 1/64
1	0	0	1	0	3	03E000H-03FFFFH	8KB	Upper 1/32
1	0	0	1	1	3	03C000H-03FFFFH	16KB	Upper 1/16
1	0	1	0	X	3	038000H-03FFFFH	32KB	Upper 1/8
1	0	1	1	0	3	038000H-03FFFFH	32KB	Upper 1/8
1	1	0	0	1	0	000000H-000FFFH	4KB	Lower 1/64
1	1	0	1	0	0	000000H-001FFFH	8KB	Lower 1/32
1	1	0	1	1	0	000000H-003FFFH	16KB	Lower 1/16

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1	1	1	0	X	0	000000H-007FFFH	32KB	Lower 1/8
1	1	1	1	0	0	000000H-007FFFH	32KB	Lower 1/8
1	X	1	1	1	0 to 3	000000H-03FFFFH	256KB	ALL
1	X	1	1	1	0 to 3	000000H-03FFFFH	256KB	ALL

Table 5. GD25LQ20E Protected area size (CMP=1)

Status Register Content					Memory Content			
BP4	**BP3**	**BP2**	**BP1**	**BP0**	**Blocks**	**Addresses**	**Density**	**Portion**
0	X	X	0	0	0 to 3	000000H-03FFFFH	256KB	ALL
0	0	X	0	1	0 to 2	000000H-02FFFFH	192KB	Lower 3/4
0	0	X	1	0	0 and 1	000000H-01FFFFH	128KB	Lower 1/2
0	1	X	0	1	1 to 3	010000H-03FFFFH	192KB	Upper 3/4
0	1	X	1	0	2 and 3	020000H-03FFFFH	128KB	Upper 1/2
0	X	X	1	1	NONE	NONE	NONE	NONE
1	X	0	0	0	0 to 3	000000H-03FFFFH	256KB	ALL
1	0	0	0	1	0 to 3	000000H-03EFFFH	252KB	Lower 63/64
1	0	0	1	0	0 to 3	000000H-03DFFFH	248KB	Lower 31/32
1	0	0	1	1	0 to 3	000000H-03BFFFH	240KB	Lower 15/16
1	0	1	0	X	0 to 3	000000H-037FFFH	224KB	Lower 7/8
1	0	1	1	0	0 to 3	000000H-037FFFH	224KB	Lower 7/8
1	1	0	0	1	0 to 3	001000H-03FFFFH	252KB	Upper 63/64
1	1	0	1	0	0 to 3	002000H-03FFFFH	248KB	Upper 31/32
1	1	0	1	1	0 to 3	004000H-03FFFFH	240KB	Upper 15/16
1	1	1	0	X	0 to 3	008000H-03FFFFH	224KB	Upper 7/8
1	1	1	1	0	0 to 3	008000H-03FFFFH	224KB	Upper 7/8
1	X	1	1	1	NONE	NONE	NONE	NONE
1	X	1	1	1	NONE	NONE	NONE	NONE

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6 STATUS REGISTER

Table 6. Status Register-SR No.1

No.	Name	Description	Note
S7	SRP0	Status Register Protection Bit	Non-volatile writable
S6	BP4	Block Protect Bit	Non-volatile writable
S5	BP3	Block Protect Bit	Non-volatile writable
S4	BP2	Block Protect Bit	Non-volatile writable
S3	BP1	Block Protect Bit	Non-volatile writable
S2	BP0	Block Protect Bit	Non-volatile writable
S1	WEL	Write Enable Latch	Volatile, read only
S0	WIP	Erase/Write In Progress	Volatile, read only

Table 7. Status Register-SR No.2

No.	Name	Description	Note
S15	SUS1	Erase Suspend Bit	Volatile, read only
S14	CMP	Complement Protect Bit	Non-volatile writable
S13	LB3	Security Register Lock Bit	Non-volatile writable (OTP)
S12	LB2	Security Register Lock Bit	Non-volatile writable (OTP)
S11	LB1	Security Register Lock Bit	Non-volatile writable (OTP)
S10	SUS2	Program Suspend Bit	Volatile, read only
S9	QE	Quad Enable Bit	Non-volatile writable
S8	SRP1	Status Register Protection Bit	Non-volatile writable

The status and control bits of the Status Register are as follows:

WIP bit

The Write in Progress (WIP) bit indicates whether the memory is busy in program/erase/write status register progress. When WIP bit sets to 1, means the device is busy in program/erase/write status register progress, when WIP bit sets 0, means the device is not in program/erase/write status register progress.

WEL bit

The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1 the internal Write Enable Latch is set, when set to 0 the internal Write Enable Latch is reset and no Write Status Register, Program or Erase command is accepted.

BP4, BP3, BP2, BP1, BP0 bits

The Block Protect (BP4, BP3, BP2, BP1, and BP0) bits are non-volatile. They define the size of the area to be software protected against Program and Erase commands. These bits are written with the Write Status Register (WRSR) command. When the Block Protect (BP4, BP3, BP2, BP1, BP0) bits are set to 1, the relevant memory area (as defined in Table 2~5) becomes protected against Page Program (PP), Sector Erase (SE) and Block Erase (BE) commands. The Block Protect (BP4, BP3, BP2, BP1, and BP0) bits can be written provided that the Hardware Protected mode has not been set. The Chip

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Erase (CE) command is executed, if the Block Protect (BP2, BP1, and BP0) bits are 0 and CMP=0 or the Block Protect (BP2, BP1, and BP0) bits are 1 and CMP=1.

SRP1, SRP0 bits

The Status Register Protect (SRP1 and SRP0) bits are non-volatile Read/Write bits in the status register. The SRP bits control the method of write protection: software protection, hardware protection, power supply lock-down or one time programmable protection.

SRP1	SRP0	#WP	Status Register	Description
0	0	X	Software Protected	The Status Register can be written to after a Write Enable command, WEL=1.(Default)
0	1	0	Hardware Protected	WP#=0, the Status Register locked and cannot be written to.
0	1	1	Hardware Unprotected	WP#=1, the Status Register is unlocked and can be written to after a Write Enable command, WEL=1.
1	0	X	Power Supply Lock-Down(1)(2)	Status Register is protected and cannot be written to again until the next Power-Down, Power-Up cycle.
1	1	X	One Time Program(2)	Status Register is permanently protected and cannot be written to.

NOTE:

1. When SRP1, SRP0= (1, 0), a Power-Down, Power-Up cycle will change SRP1, SRP0 to (0, 0) state.
2. This feature is available on special order. Please contact GigaDevice for details.

QE bit

The Quad Enable (QE) bit is a non-volatile Read/Write bit in the Status Register that allows Quad operation. When the QE bit is set to 0 (Default) the WP# pin and HOLD# pin are enable. When the QE pin is set to 1, the Quad IO2 and IO3 pins are enabled. (It is best to set the QE bit to 0 to avoid short issues if the WP# or HOLD# pin is tied directly to the power supply or ground.)

LB3, LB2, LB1 bits

The LB3, LB2 and LB1 bits are non-volatile One Time Program (OTP) bits in Status Register (S13, S12 and S11) that provide the write protect control and status to the Security Registers. The default state of LB3, LB2 and LB1 bits are 0, the security registers are unlocked. The LB3, LB2 and LB1 bits can be set to 1 individually using the Write Register instruction. The LB3, LB2 and LB1 bits are One Time Programmable, once they are set to 1, the Security Registers will become read-only permanently.

CMP bit

The CMP bit is a non-volatile Read/Write bit in the Status Register (S14). It is used in conjunction with the BP4-BP0 bits to provide more flexibility for the array protection. Please see the Status registers Memory Protection table for details. The default setting is CMP=0.

SUS1, SUS2 bits

The SUS1 and SUS2 bits are read only bits in the status register (S15 and S10) that are set to 1 after executing an Erase/ Program Suspend (75H) command (The Erase Suspend will set the SUS1 bit to 1, and the Program Suspend will set the

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SUS2 bit to 1). The SUS1 and SUS2 bits are cleared to 0 by Erase/Program Resume (7AH) command, software reset (66H+99H) command, as well as a power-down, power-up cycle.

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7 COMMAND DESCRIPTIONS

All commands, addresses and data are shifted in and out of the device, beginning with the most significant bit on the first rising edge of SCLK after CS# is driven low. Then, the one-byte command code must be shifted in to the device, with most significant bit first on SI, and each bit is latched on the rising edges of SCLK.

Every command sequence starts with a one-byte command code. Depending on the command, this might be followed by address bytes, or by data bytes, or by both or none. CS# must be driven high after the last bit of the command sequence has been completed. For the command of Read, Fast Read, Read Status Register or Release from Deep Power-Down, and Read Device ID, the shifted-in command sequence is followed by a data-out sequence. All read instruction can be completed after any bit of the data-out sequence is being shifted out, and then CS# must be driven high to return to deselected status.

For the command of Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Write Enable, Write Disable or Deep Power-Down command, CS# must be driven high exactly at a byte boundary, otherwise the command is rejected, and is not executed. That is CS# must be driven high when the number of clock pulses after CS# being driven low is an exact multiple of eight. For Page Program, if at any time the input byte is not a full byte, nothing will happen and WEL will not be reset.

Table 8. Commands

Command Name	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	Byte 8	Byte 9
Write Enable	06H								
Write Disable	04H								
Read Status Register-1	05H	(S7-S0)	(cont.)						
Read Status Register-2	35H	(S15-S8)	(cont.)						
Write Status Register-1&2	01H	S7-S0	S15-S8						
Volatile SR write Enable	50H								
Read Data	03H	A23-A16	A15-A8	A7-A0	(D7-D0)	(cont.)			
Fast Read	0BH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(cont.)		
Dual Output Fast Read	3BH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)(1)	(cont.)		
Quad Output Fast Read	6BH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)(2)	(cont.)		
Dual I/O Fast Read	BBH	A23-A16(3)	A15-A8(3)	A7-A0(3)	M7-M0(4)	(D7-D0)(1)	(cont.)		
Quad I/O Fast Read	EBH	A23-A16(5)	A15-A8(5)	A7-A0(5)	M7-M0(6)	dummy	dummy	(D7-D0)(2)	(cont.)
Set Burst with Wrap	77H	dummy(7)	dummy(7)	dummy(7)	W7-W0(7)				
Page Program	02H	A23-A16	A15-A8	A7-A0	D7-D0	Next Byte			
Quad Page Program	32H	A23-A16	A15-A8	A7-A0	D7-D0(8)	Next Byte			
Sector Erase	20H	A23-A16	A15-A8	A7-A0					
Block Erase (32K)	52H	A23-A16	A15-A8	A7-A0					
Block Erase (64K)	D8H	A23-A16	A15-A8	A7-A0					

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Chip Erase	C7/60H								
Read Manufacturer/ Device ID	90H	00H	00H	00H	(MID7-MID0)	(ID7-ID0)	(cont.)		
Read Identification	9FH	(MID7-MID0)	(ID15-ID8)	(ID7-ID0)	(cont.)				
Read Unique ID	4BH	00H	00H	00H	dummy	(UID7-UID0)	(cont.)		
Erase Security Registers(9)	44H	A23-A16	A15-A8	A7-A0					
Program Security Registers(9)	42H	A23-A16	A15-A8	A7-A0	D7-D0	Next Byte			
Read Security Registers(9)	48H	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(cont.)		
Enable Reset	66H								
Reset	99H								
Program/Erase Suspend	75H								
Program/Erase Resume	7AH								
Deep Power-Down	B9H								
Release From Deep Power-Down	ABH								
Release From Deep Power-Down and Read Device ID	ABH	dummy	dummy	dummy	(ID7-ID0)	(cont.)			
Read Serial Flash Discoverable Parameter	5AH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(cont.)		

Note:

1. Dual Output data

IO0 = (D6, D4, D2, D0)

IO1 = (D7, D5, D3, D1)

2. Quad Output Data

IO0 = (D4, D0, …)

IO1 = (D5, D1, …)

IO2 = (D6, D2, …)

IO3 = (D7, D3, …)

3. Dual Input Address

IO0 = A22, A20, A18, A16, A14, A12, A10, A8 A6, A4, A2, A0

IO1 = A23, A21, A19, A17, A15, A13, A11, A9 A7, A5, A3, A1

4. Dual Input Mode bit

IO0 = M6, M4, M2, M0

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IO1 = M7, M5, M3, M1

5. Quad Input Address

IO0 = A20, A16, A12, A8, A4, A0

IO1 = A21, A17, A13, A9, A5, A1

IO2 = A22, A18, A14, A10, A6, A2

IO3 = A23, A19, A15, A11, A7, A3

6. Quad Input Mode bit

IO0 = M4, M0

IO1 = M5, M1

IO2 = M6, M2

IO3 = M7, M3

7. Dummy bits and Wrap Bits

IO0 = (x, x, x, x, x, x, W4, x)

IO1 = (x, x, x, x, x, x, W5, x)

IO2 = (x, x, x, x, x, x, W6, x)

IO3 = (x, x, x, x, x, x, x, x)

8. Quad Output Data

IO0 = D4, D0, …

IO1 = D5, D1, …

IO2 = D6, D2, …

IO3 = D7, D3, …

9. Security Registers Address

Security Register1: A23-A16=00H, A15-A12=1H, A11-A9 = 000b, A8-A0= Byte Address;

Security Register2: A23-A16=00H, A15-A12=2H, A11-A9 = 000b, A8-A0= Byte Address;

Security Register3: A23-A16=00H, A15-A12=3H, A11-A9 = 000b, A8-A0= Byte Address;

TABLE OF ID DEFINITIONS

GD25LQ40E

Operation Code	MID7-MID0	ID15-ID8	ID7-ID0
9FH	C8	60	13
90H	C8		12
ABH			12

GD25LQ20E

Operation Code	MID7-MID0	ID15-ID8	ID7-ID0
9FH	C8	60	12
90H	C8		11
ABH			11

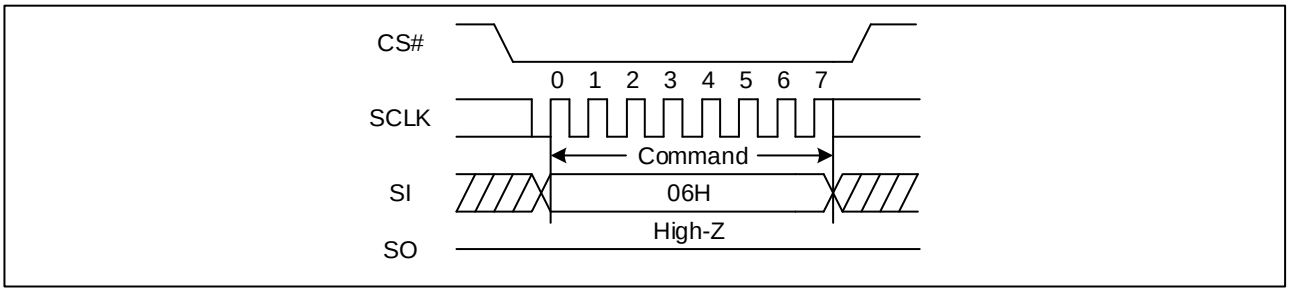
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7.1 Write Enable (WREN) (06H)

The Write Enable (WREN) command is for setting the Write Enable Latch (WEL) bit. The Write Enable Latch (WEL) bit must be set prior to every Page Program (PP), Quad Page Program (QPP), Sector Erase (SE), Block Erase (BE), Chip Erase (CE), Write Status Register (WRSR) and Erase/Program Security Registers command.

The Write Enable (WREN) command sequence: CS# goes low → sending the Write Enable command → CS# goes high.

Figure 2. Write Enable Sequence Diagram



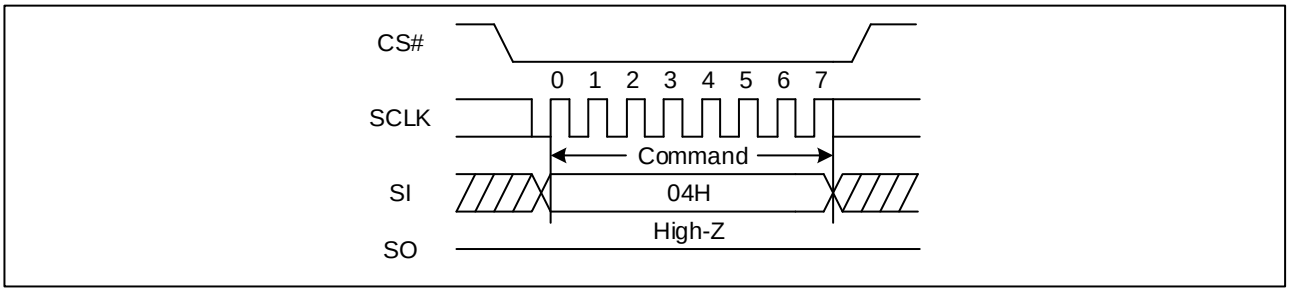
7.2 Write Disable (WRDI) (04H)

The Write Disable command is for resetting the Write Enable Latch (WEL) bit. The Write Enable Latch (WEL) bit may be set to 0 by issuing the Write Disable (WRDI) command to disable Page Program (PP), Quad Page Program (QPP), Sector Erase (SE), Block Erase (BE), Chip Erase (CE), Write Status Register (WRSR), that require WEL be set to 1 for execution. The WRDI command can be used by the user to protect memory areas against inadvertent writes that can possibly corrupt the contents of the memory. The WRDI command is ignored during an embedded operation while WIP bit =1.

The WEL bit is reset by following condition: Write Disable command (WRDI), Power-up, and upon completion of the Write Status Register, Page Program, Sector Erase, Block Erase and Chip Erase commands.

The Write Disable command sequence: CS# goes low →Sending the Write Disable command →CS# goes high.

Figure 3. Write Disable Sequence Diagram

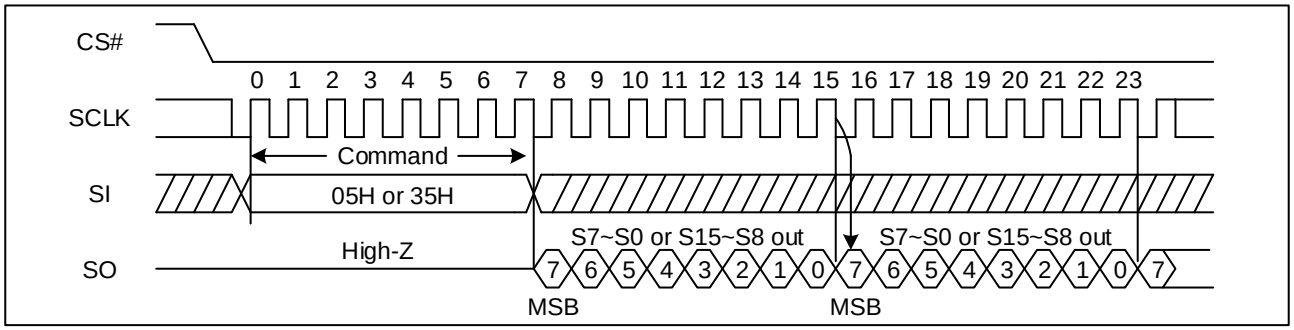


7.3 Read Status Register (RDSR) (05H or 35H)

The Read Status Register (RDSR) command is for reading the Status Register. The Status Register may be read at any time, even while a Program, Erase or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write in Progress (WIP) bit before sending a new command to the device. It is also possible to read the Status Register continuously. For command code “05H”, the SO will output Status Register bits S7~S0. The command code “35H”, the SO will output Status Register bits S15~S8.

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Figure 4. Read Status Register Sequence Diagram



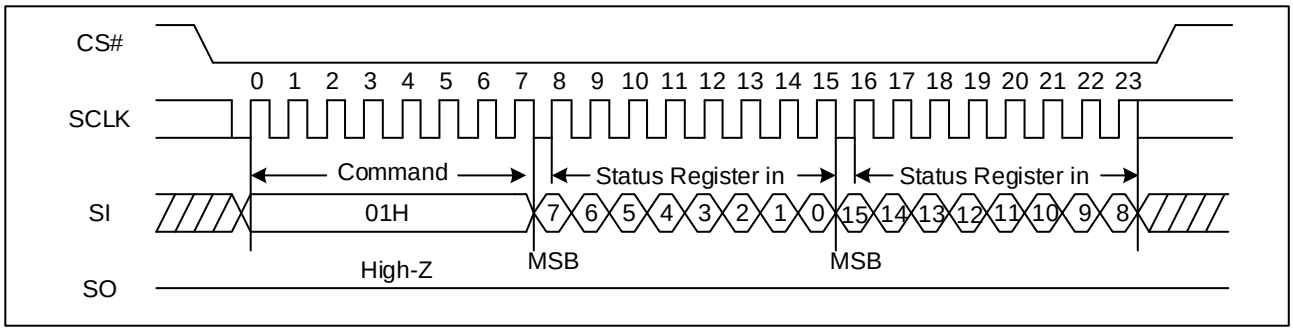
7.4 Write Status Register (WRSR) (01H)

The Write Status Register (WRSR) command allows new values to be written to the Status Register. Before it can be accepted, a Write Enable (WREN) command must previously have been executed. After the Write Enable (WREN) command has been decoded and executed, the device sets the Write Enable Latch (WEL).

The Write Status Register (WRSR) command has no effect on S15, S10, S1 and S0 of the Status Register. CS# must be driven high after the eighth or sixteenth bit of the data byte has been latched in. Otherwise, the Write Status Register (WRSR) command is not executed. If CS# is driven high after eighth bit of the data byte, the alterable bits in Status Register-2 (S15~S8) will be cleared to 0. As soon as CS# is driven high, the self-timed Write Status Register cycle (whose duration is t_W) is initiated. While the Write Status Register cycle is in progress, the Status Register may still be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Write Status Register cycle, and is 0 when it is completed. When the cycle is completed, the Write Enable Latch (WEL) is reset.

The Write Status Register (WRSR) command allows the user to change the values of the Block Protect (BP4, BP3, BP2, BP1, and BP0) bits, to define the size of the area that is to be treated as read-only. The Write Status Register (WRSR) command also allows the user to set or reset the Status Register Protect (SRP1 and SRP0) bits in accordance with the Write Protect (WP#) signal. The Status Register Protect (SRP1 and SRP0) bits and Write Protect (WP#) signal allow the device to be put in the Hardware Protected Mode. The Write Status Register (WRSR) command is not executed once the Hardware Protected Mode is entered.

Figure 5. Write Status Register Sequence Diagram



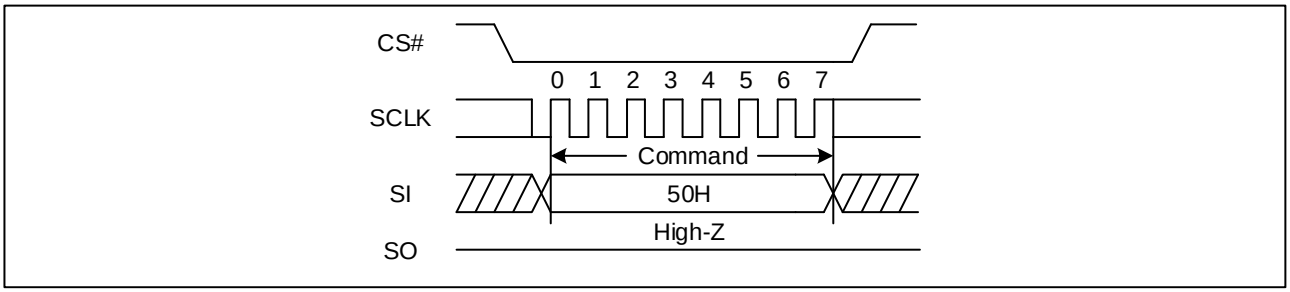
7.5 Write Enable for Volatile Status Register (50H)

The non-volatile Status Register bits can also be written to as volatile bits. This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits. The Write Enable for Volatile Status Register command must be issued prior to a Write Status Register command and any other commands can't be inserted between them. Otherwise, Write Enable for Volatile Status Register will be cleared. The Write Enable for Volatile Status Register command will not set

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the Write Enable Latch bit, it is only valid for the Write Status Register command to change the volatile Status Register bit values.

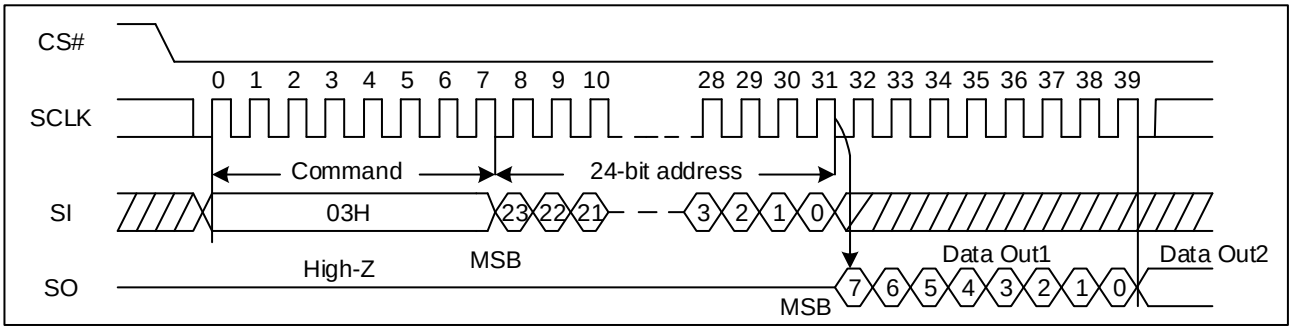
Figure 6. Write Enable for Volatile Status Register Sequence Diagram



7.6 Read Data Bytes (READ) (03H)

The Read Data Bytes (READ) command is followed by a 3-byte address (A23-A0), and each bit is latched-in on the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, and each bit is shifted out, at a Max frequency f_R, on the falling edge of SCLK. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes (READ) command. Any Read Data Bytes (READ) command, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 7. Read Data Bytes Sequence Diagram

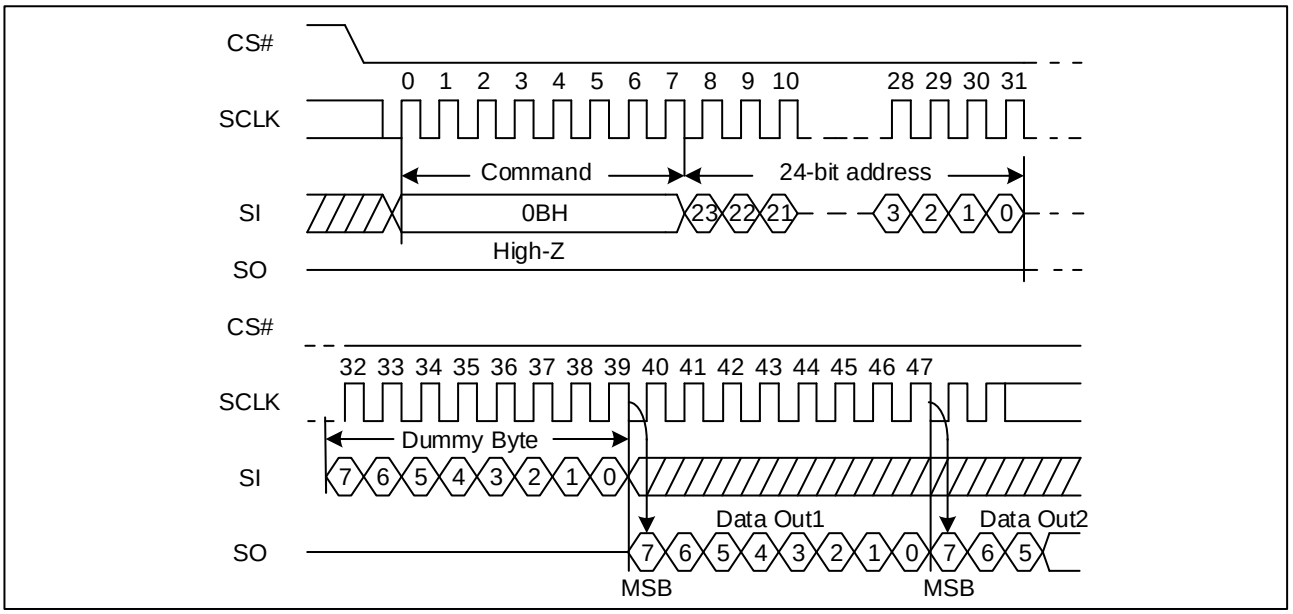


7.7 Read Data Bytes at Higher Speed (Fast Read) (0BH)

The Read Data Bytes at Higher Speed (Fast Read) command is for quickly reading data out. It is followed by a 3-byte address (A23-A0) and a dummy byte, and each bit is latched-in on the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, and each bit is shifted out, at a Max frequency f_C, on the falling edge of SCLK. The first byte address can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out.

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Figure 8. Read Data Bytes at Higher Speed Sequence Diagram

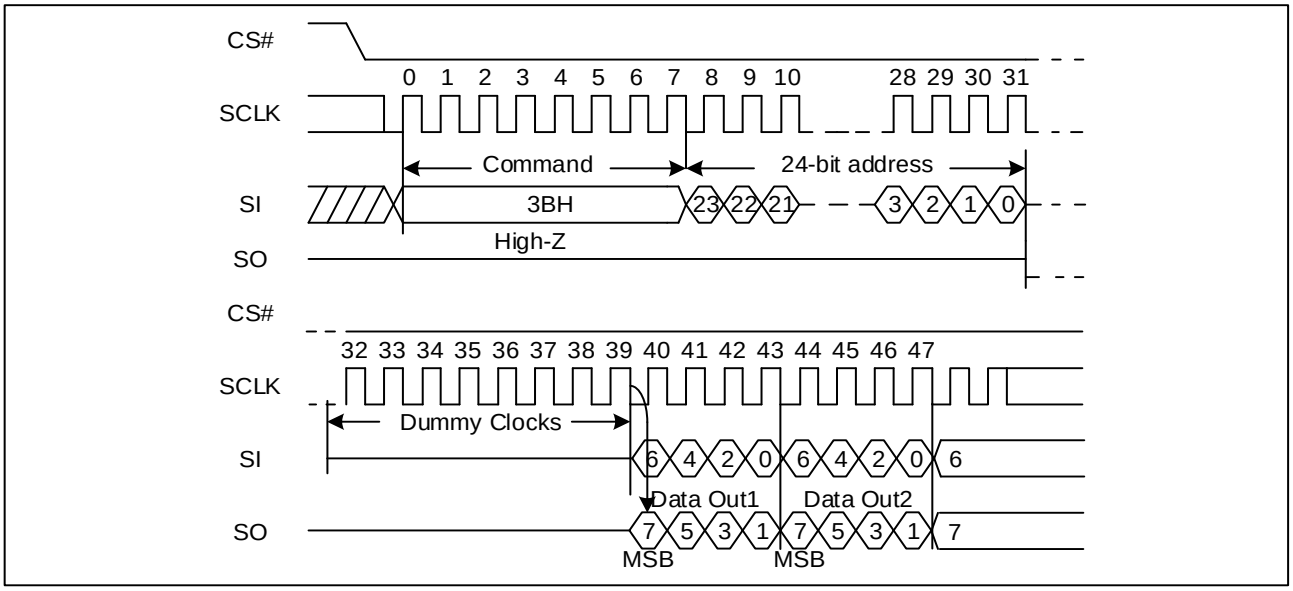


7.8 Dual Output Fast Read (3BH)

The Dual Output Fast Read command is followed by 3-byte address (A23-A0) and a dummy byte, and each bit is latched in on the rising edge of SCLK, then the memory contents are shifted out 2-bit per clock cycle from SI and SO.

The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out.

Figure 9. Dual Output Fast Read Sequence Diagram

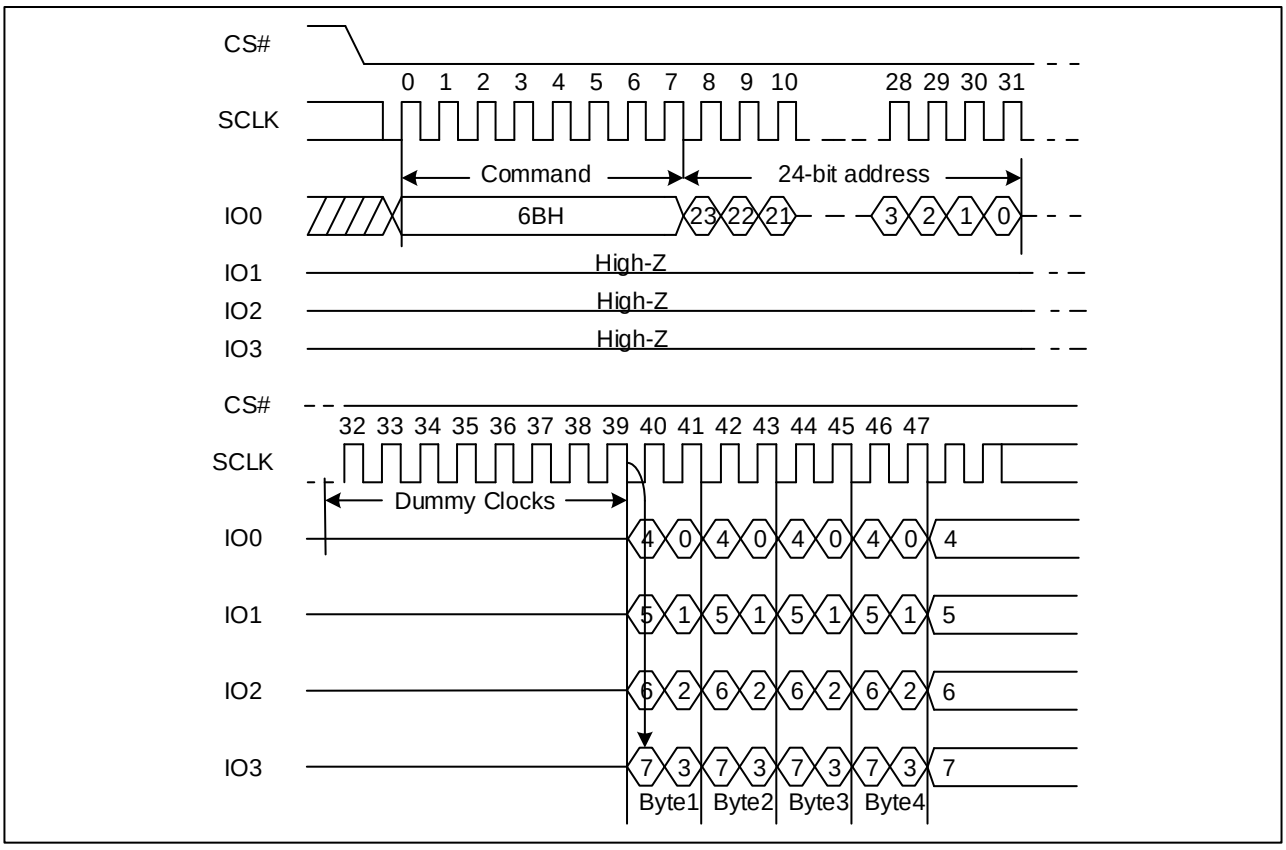


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7.9 Quad Output Fast Read (6BH)

The Quad Output Fast Read command is followed by 3-byte address (A23-A0) and a dummy byte, and each bit is latched in on the rising edge of SCLK, then the memory contents are shifted out 4-bit per clock cycle from IO3, IO2, IO1 and IO0. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The Quad Enable bit (QE) of Status Register (S9) must be set to enable for the Quad Output Fast Read command.

Figure 10. Quad Output Fast Read Sequence Diagram



7.10 Dual I/O Fast Read (BBH)

The Dual I/O Fast Read command is similar to the Dual Output Fast Read command but with the capability to input the 3-byte address (A23-0) and a “Continuous Read Mode” byte 2-bit per clock by SI and SO, and each bit is latched in on the rising edge of SCLK, then the memory contents are shifted out 2-bit per clock cycle from SI and SO. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out.

Dual I/O Fast Read with “Continuous Read Mode”

The Dual I/O Fast Read command can further reduce command overhead through setting the “Continuous Read Mode” bits (M7-0) after the input 3-byte address (A23-A0). If the “Continuous Read Mode” bits (M5-4) = (1, 0), then the next Dual I/O Fast Read command (after CS# is raised and then lowered) does not require the BBH command code. If the “Continuous Read Mode” bits (M5-4) ≠ (1, 0), the next command requires the command code, thus returning to normal operation. A Reset command can be also used to reset (M7-0) before issuing normal command.

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Figure 11. Dual I/O Fast Read Sequence Diagram ((M5-4) ≠ (1, 0))

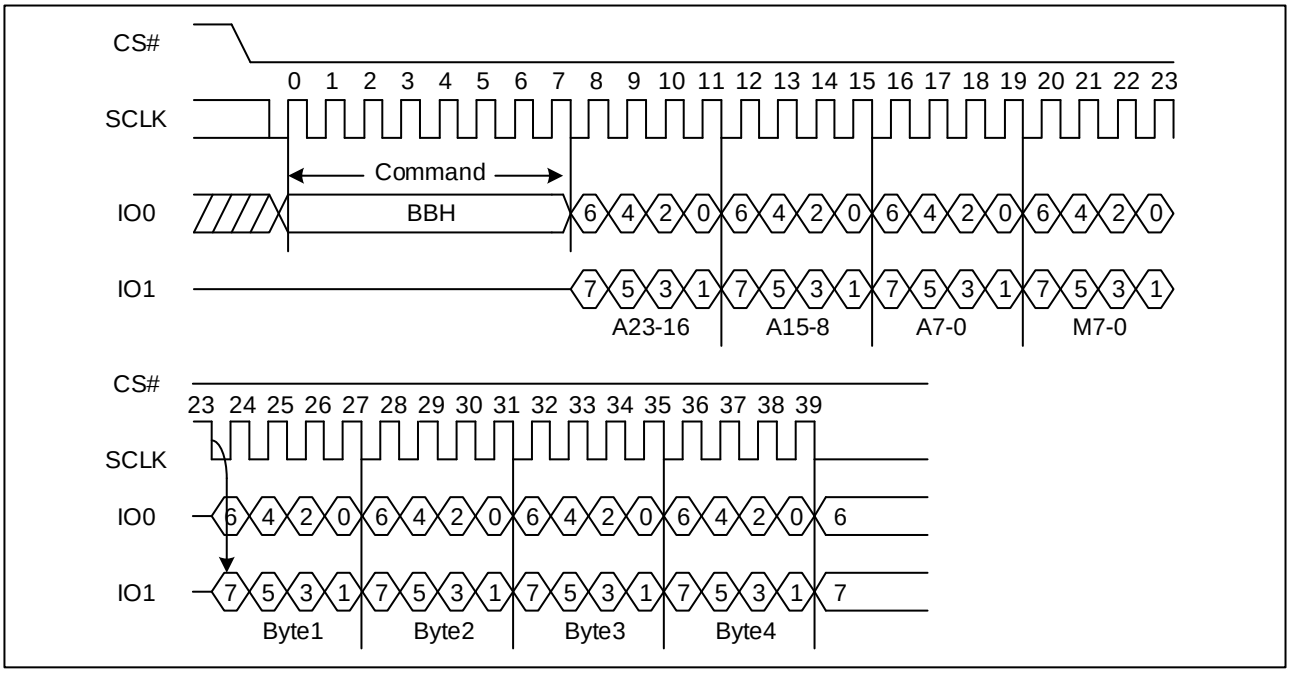
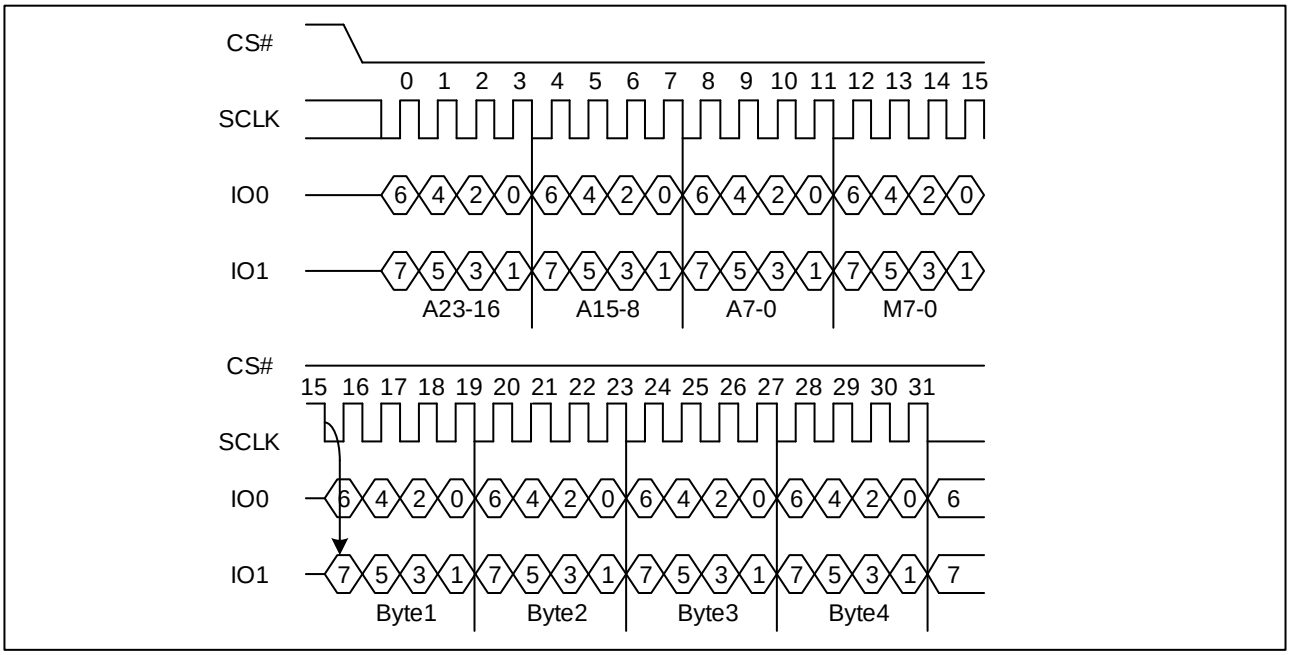


Figure 12. Dual I/O Fast Read Sequence Diagram ((M5-4) = (1, 0))



7.11 Quad I/O Fast Read (EBH)

The Quad I/O Fast Read command is similar to the Dual I/O Fast Read command but with the capability to input the 3-byte address (A23-0) and a “Continuous Read Mode” byte and 4-dummy clock 4-bit per clock by IO0, IO1, IO2, IO3, and each bit is latched in on the rising edge of SCLK, then the memory contents are shifted out 4-bit per clock cycle from IO0, IO1, IO2, IO3. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The Quad Enable bit (QE) of Status Register (S9) must be set to enable for the Quad I/O Fast read command.

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Quad I/O Fast Read with "Continuous Read Mode"

The Quad I/O Fast Read command can further reduce command overhead through setting the "Continuous Read Mode" bits (M7-0) after the input 3-byte address (A23-A0). If the "Continuous Read Mode" bits (M5-4) = (1, 0), then the next Quad I/O Fast Read command (after CS# is raised and then lowered) does not require the EBH command code. If the "Continuous Read Mode" bits (M5-4) ≠ (1, 0), the next command requires the command code, thus returning to normal operation. A Reset command can be also used to reset (M7-0) before issuing normal command.

Figure 13. Quad I/O Fast Read Sequence Diagram ((M5-4) ≠ (1, 0))

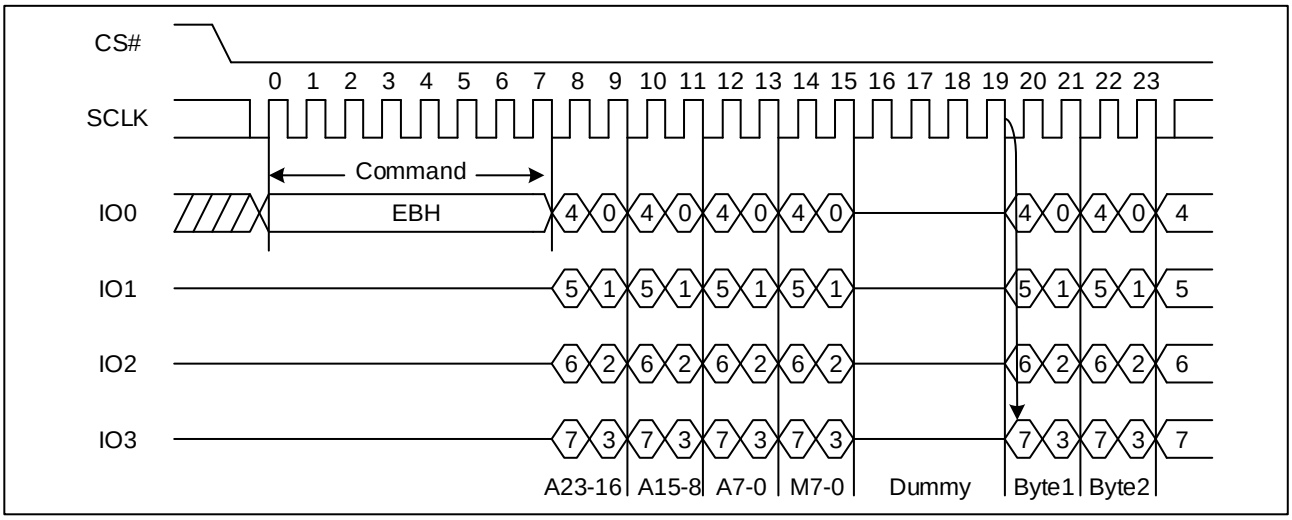
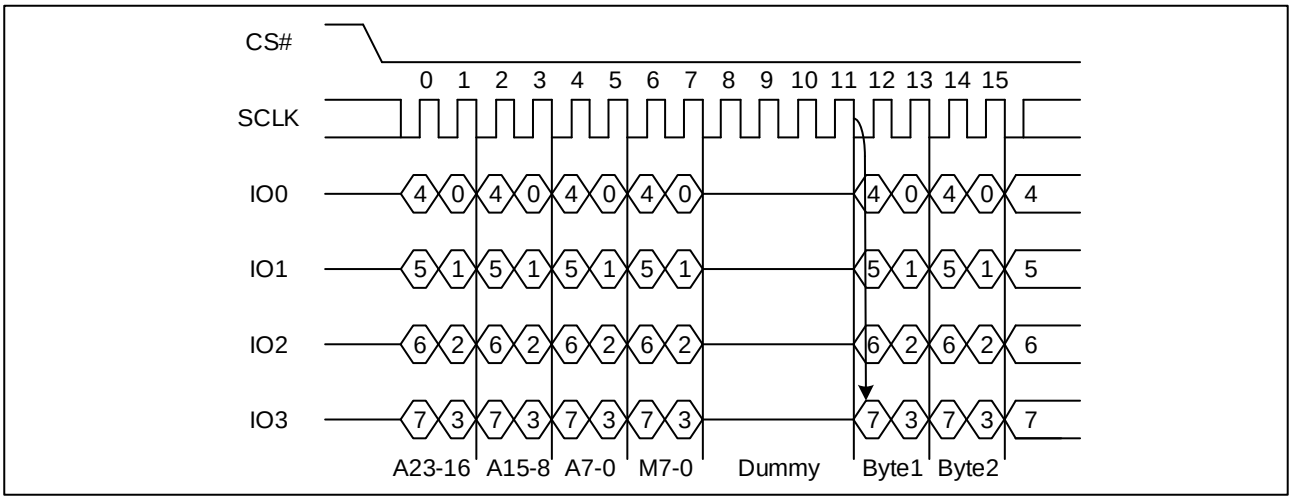


Figure 14. Quad I/O Fast Read Sequence Diagram ((M5-4) = (1, 0))



Quad I/O Fast Read with "8/16/32/64-Byte Wrap Around" in Standard SPI mode

The Quad I/O Fast Read command can be used to access a specific portion within a page by issuing "Set Burst with Wrap" (77H) commands prior to EBH. The "Set Burst with Wrap" (77H) command can either enable or disable the "Wrap Around" feature for the following EBH commands. When "Wrap Around" is enabled, the data being accessed can be limited to either an 8/16/32/64-byte section of a 256-byte page. The output data starts at the initial address specified in the command, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around the beginning boundary automatically until CS# is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands. The "Set Burst with Wrap"

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command allows three “Wrap Bits” W6-W4 to be set. The W4 bit is used to enable or disable the “Wrap Around” operation while W6-W5 is used to specify the length of the wrap around section within a page.

7.12 Set Burst with Wrap (77H)

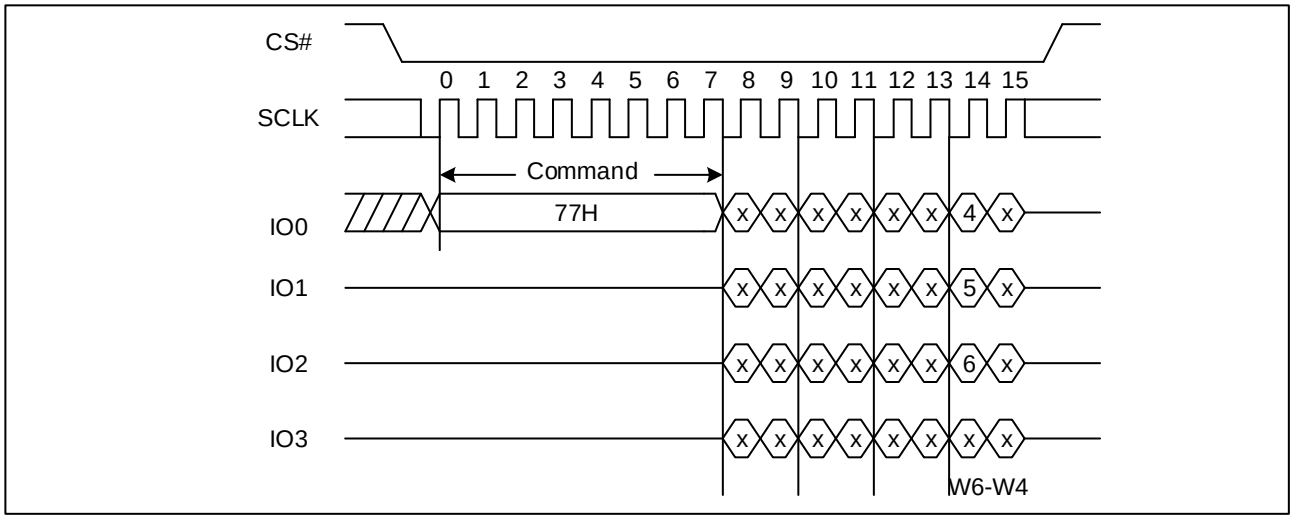
The Set Burst with Wrap command is used in conjunction with “Quad I/O Fast Read” command to access a fixed length of 8/16/32/64-byte section within a 256-byte page, in standard SPI mode.

The Set Burst with Wrap command sequence: CS# goes low → Send Set Burst with Wrap command → Send 24 dummy bits → Send 8 bits “Wrap bits” → CS# goes high.

W6,W5	W4=0		W4=1 (default)	
	Wrap Around	Wrap Length	Wrap Around	Wrap Length
0, 0	Yes	8-byte	No	N/A
0, 1	Yes	16-byte	No	N/A
1, 0	Yes	32-byte	No	N/A
1, 1	Yes	64-byte	No	N/A

If the W6-W4 bits are set by the Set Burst with Wrap command, all the following “Quad I/O Fast Read” command will use the W6-W4 setting to access the 8/16/32/64-byte section within any page. To exit the “Wrap Around” function and return to normal read operation, another Set Burst with Wrap command should be issued to set W4=1.

Figure 15. Set Burst with Wrap Sequence Diagram



7.13 Page Program (PP) (02H)

The Page Program (PP) command is for programming the memory. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Page Program command.

The Page Program (PP) command is entered by driving CS# Low, followed by the command code, three address bytes and at least one data byte on SI. If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 8 least significant bits (A7-A0) are all zero). CS# must be driven low for the entire duration of the sequence. The Page Program command sequence: CS# goes low → sending Page Program command → 3-byte address on SI → at least 1 byte data on SI → CS# goes high. If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page.

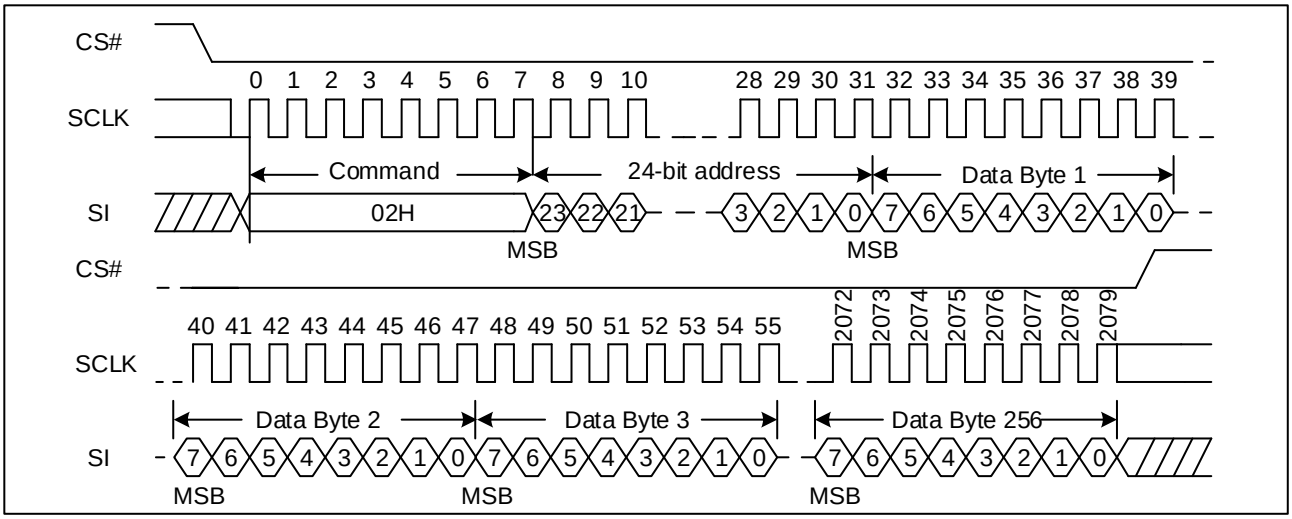
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CS# must be driven high after the eighth bit of the last data byte has been latched in; otherwise the Page Program (PP) command is not executed.

As soon as CS# is driven high, the self-timed Page Program cycle (whose duration is t_{PP}) is initiated. While the Page Program cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Page Program (PP) command applied to a page which is protected by the Block Protect (BP4, BP3, BP2, BP1, and BP0) is not executed.

Figure 16. Page Program Sequence Diagram



7.14 Quad Page Program (32H)

The Quad Page Program command is for programming the memory using four pins: IO0, IO1, IO2, and IO3. To use Quad Page Program the Quad enable in status register Bit9 must be set (QE=1). A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Page Program command. The quad Page Program command is entered by driving CS# Low, followed by the command code (32H), three address bytes and at least one data byte on IO pins.

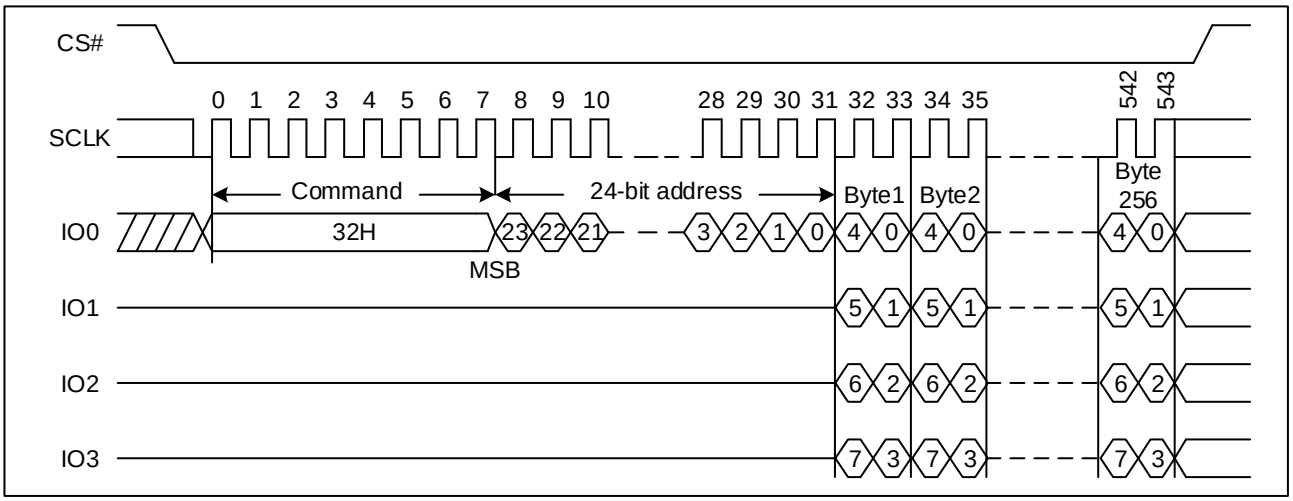
If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page. CS# must be driven high after the eighth bit of the last data byte has been latched in; otherwise the Quad Page Program (PP) command is not executed.

As soon as CS# is driven high, the self-timed Quad Page Program cycle (whose duration is t_{PP}) is initiated. While the Quad Page Program cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Quad Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Quad Page Program command applied to a page which is protected by the Block Protect (BP4, BP3, BP2, BP1, and BP0) is not executed.

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Figure 17. Quad Page Program Sequence Diagram

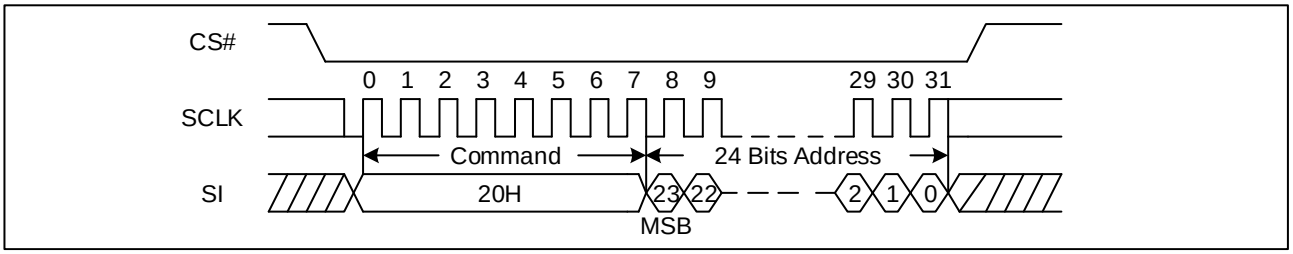


7.15 Sector Erase (SE) (20H)

The Sector Erase (SE) command is for erasing the all data of the chosen sector. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The Sector Erase (SE) command is entered by driving CS# low, followed by the command code, and 3-address byte on SI. Any address inside the sector is a valid address for the Sector Erase (SE) command. CS# must be driven low for the entire duration of the sequence.

The Sector Erase command sequence: CS# goes low → sending Sector Erase command → 3-byte address on SI → CS# goes high. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the Sector Erase (SE) command is not executed. As soon as CS# is driven high, the self-timed Sector Erase cycle (whose duration is t_{SE}) is initiated. While the Sector Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Sector Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A Sector Erase (SE) command applied to a sector which is protected by the Block Protect (BP4, BP3, BP2, BP1, and BP0) bit is not executed.

Figure 18. Sector Erase Sequence Diagram



7.16 32KB Block Erase (BE32) (52H)

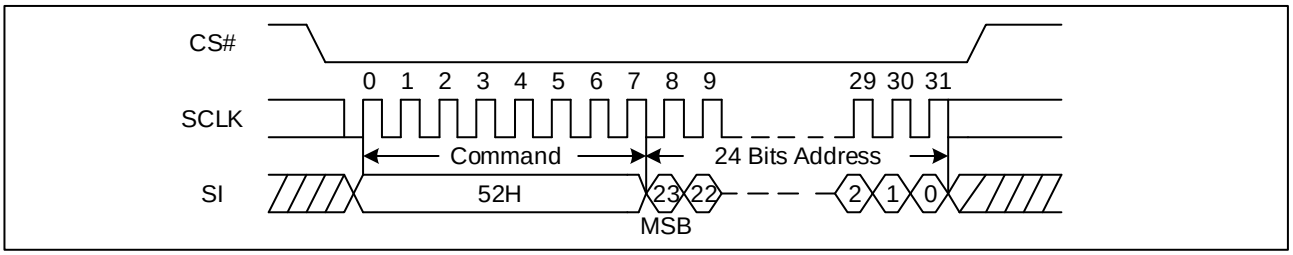
The 32KB Block Erase command is for erasing the all data of the chosen block. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The 32KB Block Erase command is entered by driving CS# low, followed by the command code, and three address bytes on SI. Any address inside the block is a valid address for the 32KB Block Erase command. CS# must be driven low for the entire duration of the sequence.

The 32KB Block Erase command sequence: CS# goes low → sending 32KB Block Erase command → 3-byte address on SI → CS# goes high. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise

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the 32KB Block Erase command is not executed. As soon as CS# is driven high, the self-timed Block Erase cycle (whose duration is t_{BE1}) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A 32KB Block Erase command applied to a block which is protected by the Block Protect (BP4, BP3, BP2, BP1, and BP0) bits is not executed.

Figure 19. 32KB Block Erase Sequence Diagram

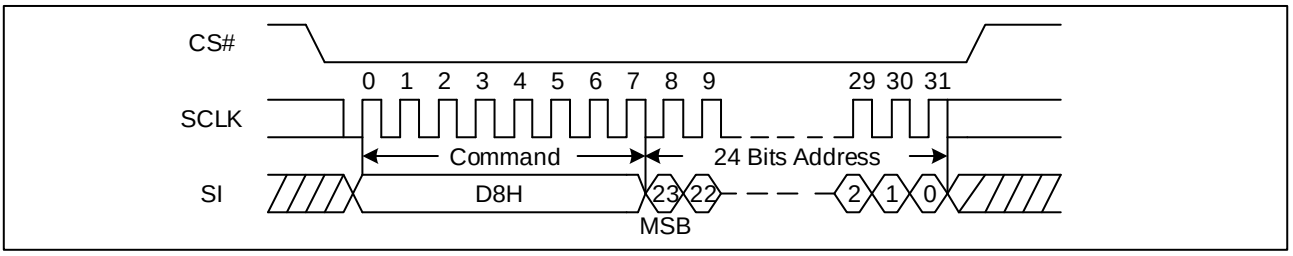


7.17 64KB Block Erase (BE64) (D8H)

The 64KB Block Erase command is for erasing the all data of the chosen block. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The 64KB Block Erase command is entered by driving CS# low, followed by the command code, and three address bytes on SI. Any address inside the block is a valid address for the 64KB Block Erase command. CS# must be driven low for the entire duration of the sequence.

The 64KB Block Erase command sequence: CS# goes low → sending 64KB Block Erase command → 3-byte address on SI → CS# goes high. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the 64KB Block Erase command is not executed. As soon as CS# is driven high, the self-timed Block Erase cycle (whose duration is t_{BE2}) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A 64KB Block Erase command applied to a block which is protected by the Block Protect (BP4, BP3, BP2, BP1, and BP0) bits is not executed.

Figure 20. 64KB Block Erase Sequence Diagram



7.18 Chip Erase (CE) (60/C7H)

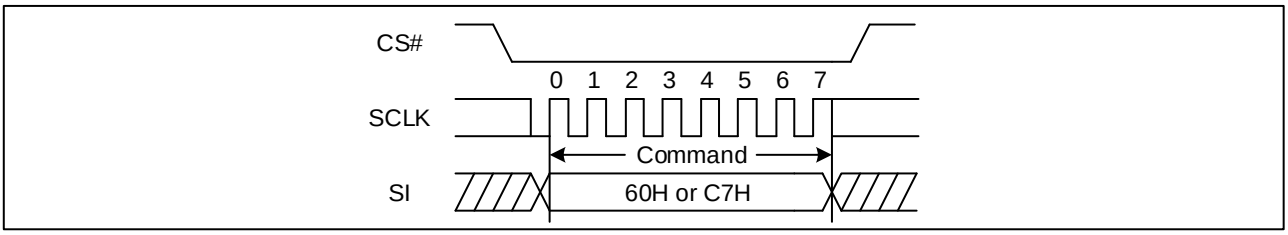
The Chip Erase (CE) command is for erasing the all data of the chip. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit .The Chip Erase (CE) command is entered by driving CS# Low, followed by the command code on Serial Data Input (SI). CS# must be driven Low for the entire duration of the sequence.

The Chip Erase command sequence: CS# goes low → sending Chip Erase command → CS# goes high. CS# must be driven high after the eighth bit of the command code has been latched in; otherwise the Chip Erase command is not executed.

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As soon as CS# is driven high, the self-timed Chip Erase cycle (whose duration is t_{CE}) is initiated. While the Chip Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Chip Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. The Chip Erase (CE) command is executed, if the Block Protect (BP2, BP1, and BP0) bits are 0 and CMP=0 or the Block Protect (BP2, BP1, and BP0) bits are 1 and CMP=1. The Chip Erase (CE) command is ignored if one or more sectors are protected.

Figure 21. Chip Erase Sequence Diagram

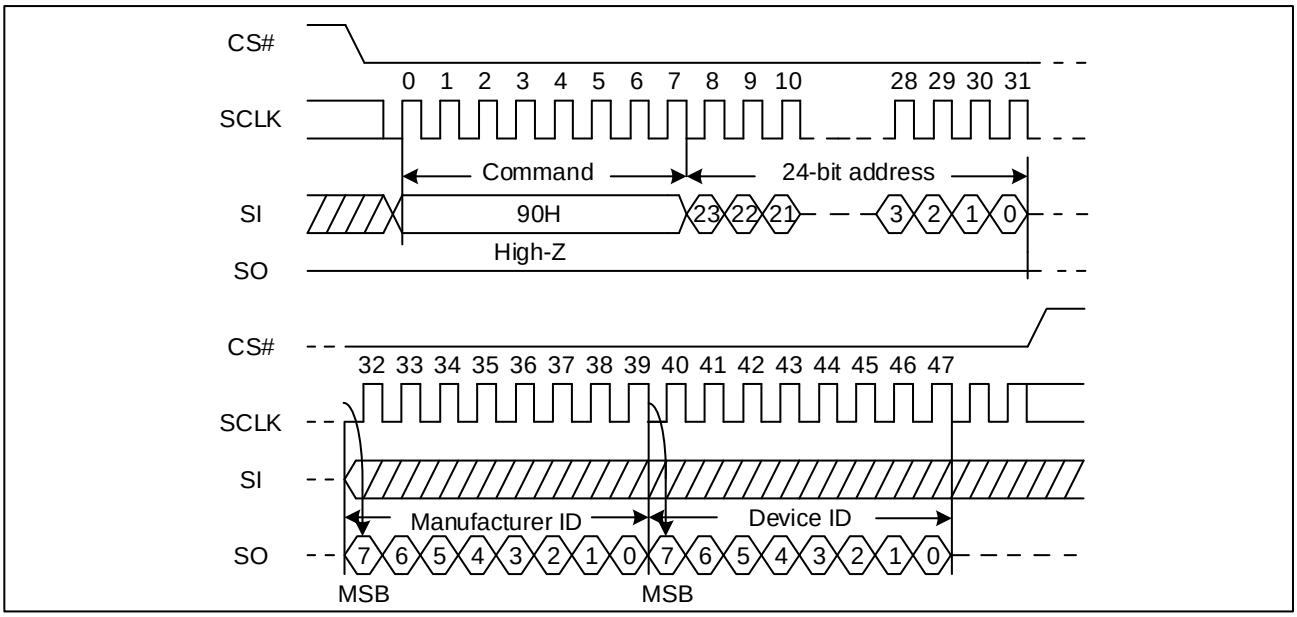


7.19 Read Manufacture ID/ Device ID (REMS) (90H)

The Read Manufacturer/Device ID command is an alternative to the Release from Power-Down / Device ID command that provides both the JEDEC assigned Manufacturer ID and the specific Device ID.

The command is initiated by driving the CS# pin low and shifting the command code “90H” followed by a 24-bit address (A23-A0) of 000000H. After which, the Manufacturer ID and the Device ID are shifted out on the falling edge of SCLK with most significant bit (MSB) first.

Figure 22. Read Manufacture ID/ Device ID Sequence Diagram



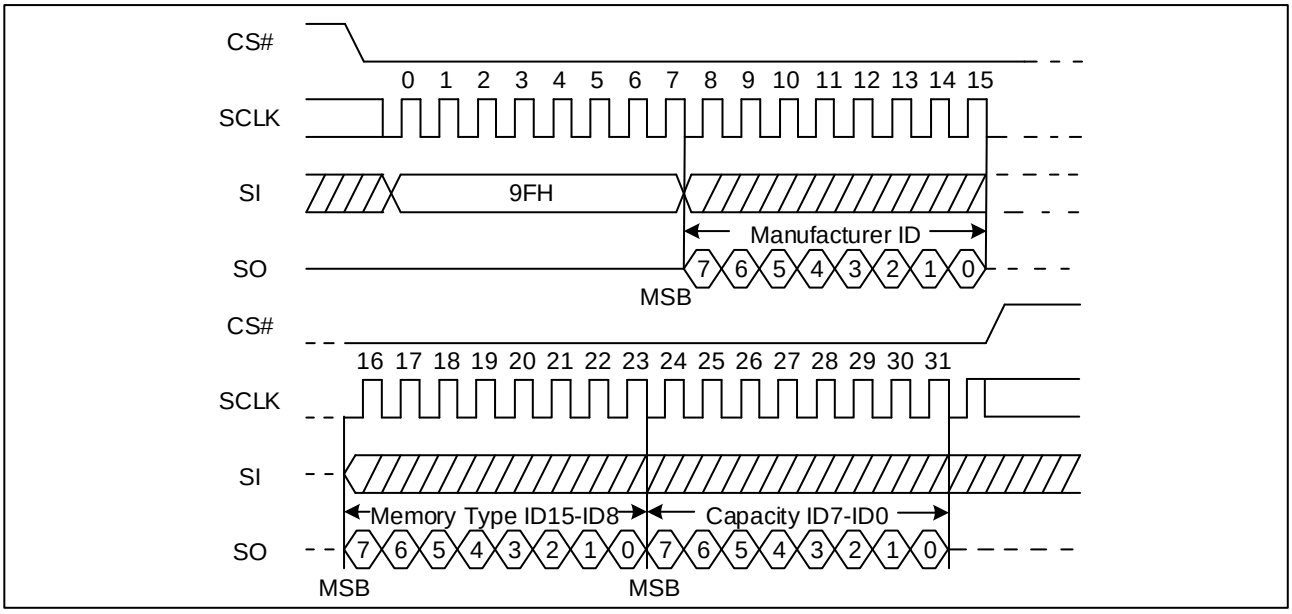
7.20 Read Identification (RDID) (9FH)

The Read Identification (RDID) command allows the 8-bit manufacturer identification to be read, followed by two bytes of device identification. The device identification indicates the memory type in the first byte, and the memory capacity of the device in the second byte. The Read Identification (RDID) command while an Erase or Program cycle is in progress, is not decoded, and has no effect on the cycle that is in progress. The Read Identification (RDID) command should not be issued while the device is in Deep Power-Down Mode.

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The device is first selected by driving CS# low. Then, the 8-bit command code for the command is shifted in. This is followed by the 24-bit device identification, stored in the memory. Each bit is shifted out on the falling edge of Serial Clock. The Read Identification (RDID) command is terminated by driving CS# high at any time during data output. When CS# is driven high, the device is in the Standby Mode. Once in the Standby Mode, the device waits to be selected, so that it can receive, decode and execute commands.

Figure 23. Read Identification ID Sequence Diagram

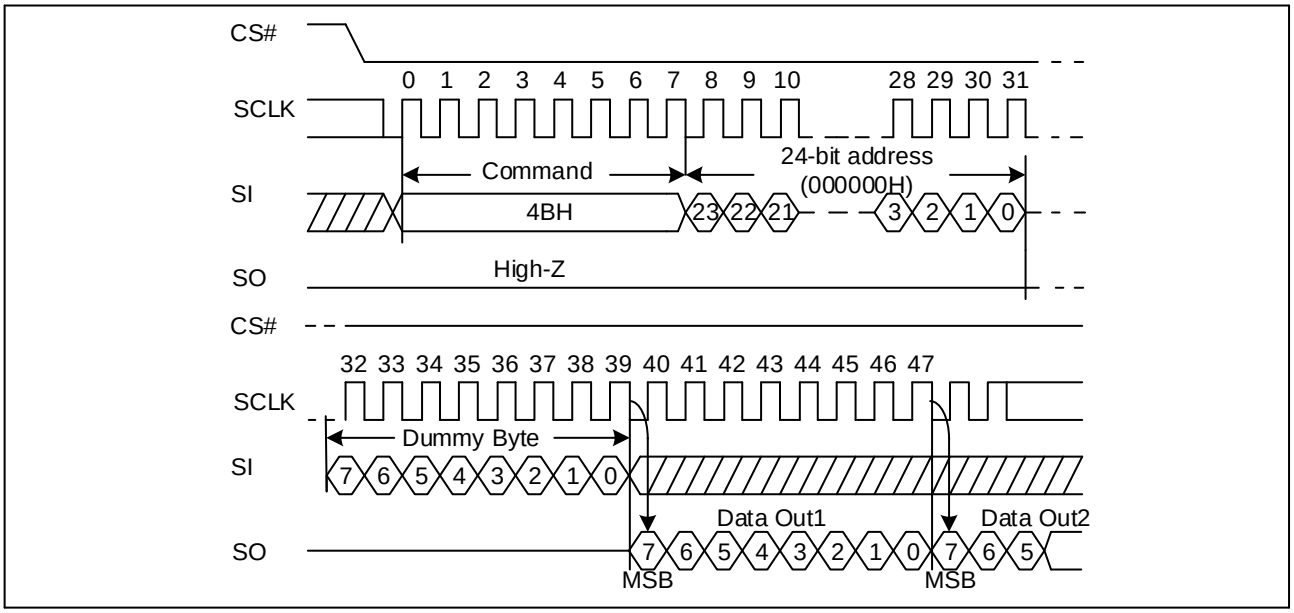


7.21 Read Unique ID (4BH)

The Read Unique ID command accesses a factory-set read-only 128bit number that is unique to each device. The Unique ID can be used in conjunction with user software methods to help prevent copying or cloning of a system.

The Read Unique ID command sequence: CS# goes low → sending Read Unique ID command → 3-Byte Address (000000H) →Dummy Byte→128bit Unique ID Out →CS# goes high.

Figure 24. Read Unique ID Sequence Diagram



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7.22 Erase Security Registers (44H)

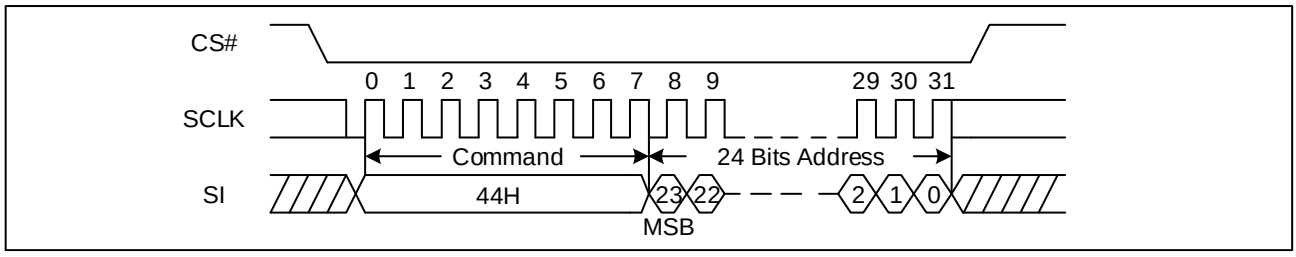
The GD25LQ40E/20E provides 3x512-Byte Security Registers which can be erased and programmed individually. These registers may be used by the system manufacturers to store security and other important information separately from the main memory array.

The Erase Security Registers command is similar to Sector/Block Erase command. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit.

The Erase Security Registers command sequence: CS# goes low → sending Erase Security Registers command → 3-byte address on SI → CS# goes high. The command sequence is shown below. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the Erase Security Registers command is not executed. As soon as CS# is driven high, the self-timed Erase Security Registers cycle (whose duration is t_{SE}) is initiated. While the Erase Security Registers cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Erase Security Registers cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. The Security Registers Lock Bit (LB1, LB2, LB3) in the Status Register can be used to OTP protect the security registers. Once the LB bit is set to 1, the Security Registers will be permanently locked; the Erase Security Registers command will be ignored.

Address	A23-16	A15-12	A11-9	A8-0
Security Register #1	00H	0001b	000b	Don't care
Security Register #2	00H	0010b	000b	Don't care
Security Register #3	00H	0011b	000b	Don't care

Figure 25. Erase Security Registers command Sequence Diagram



7.23 Program Security Registers (42H)

The Program Security Registers command is similar to the Page Program command. Each security register contains two pages content. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Program Security Registers command. The Program Security Registers command is entered by driving CS# Low, followed by the command code (42H), three address bytes and at least one data byte on SI. As soon as CS# is driven high, the self-timed Program Security Registers cycle (whose duration is t_{PP}) is initiated. While the Program Security Registers cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Program Security Registers cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

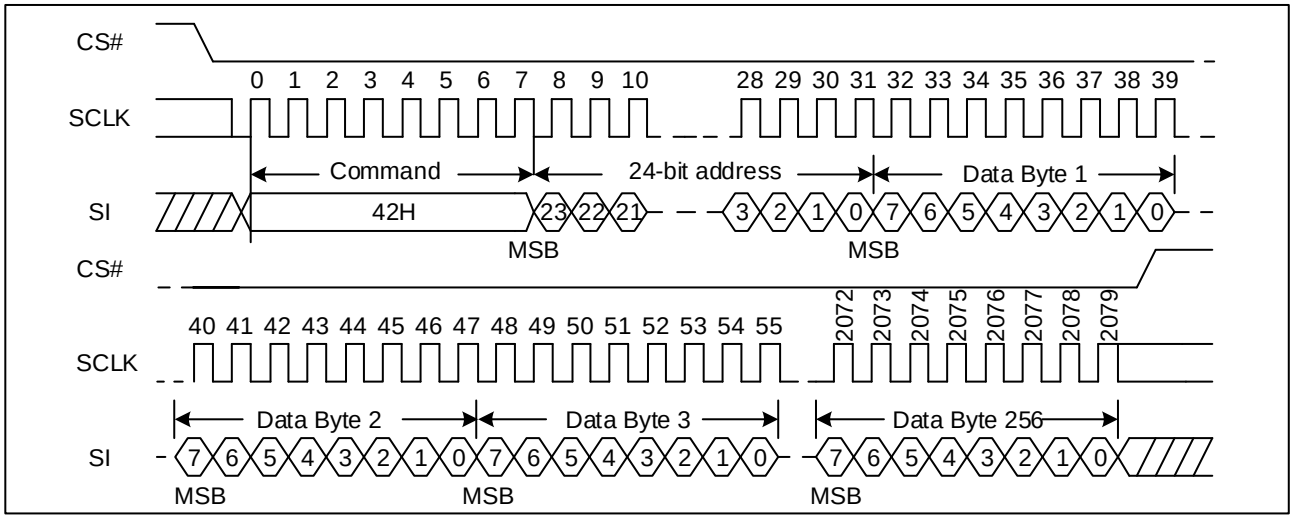
If the Security Registers Lock Bit (LB1, LB2, LB3) is set to 1, the Security Registers will be permanently locked. Program Security Registers command will be ignored.

Address	A23-16	A15-12	A11-9	A8-0
Security Register #1	00H	0001b	000b	Byte Address
Security Register #2	00H	0010b	000b	Byte Address

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Security Register #3	00H	0011b	000b	Byte Address

Figure 26. Program Security Registers command Sequence Diagram



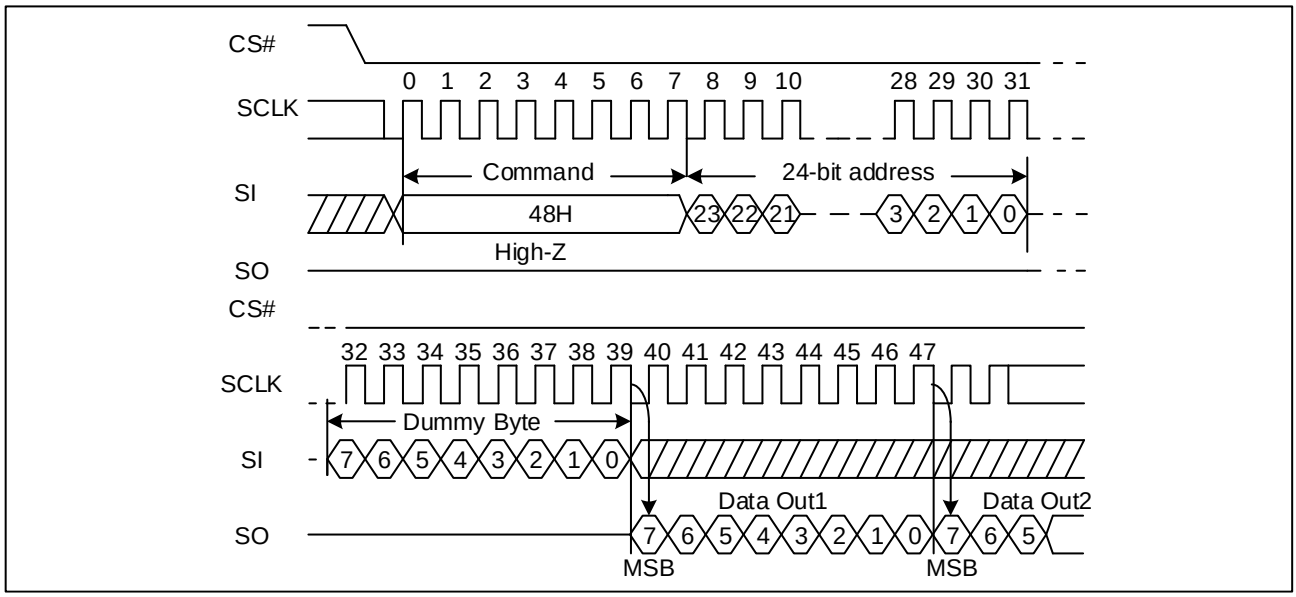
7.24 Read Security Registers (48H)

The Read Security Registers command is similar to Fast Read command. The command is followed by a 3-byte address (A23-A0) and a dummy byte, and each bit is latched-in on the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, and each bit is shifted out, at a Max frequency f_C, on the falling edge of SCLK. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. Once the A8-0 address reaches the last byte of the register (Byte 1FFH), it will reset to 000H, the command is completed by driving CS# high.

Address	A23-16	A15-12	A11-9	A8-0
Security Register #1	00H	0001b	000b	Byte Address
Security Register #2	00H	0010b	000b	Byte Address
Security Register #3	00H	0011b	000b	Byte Address

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Figure 27. Read Security Registers command Sequence Diagram

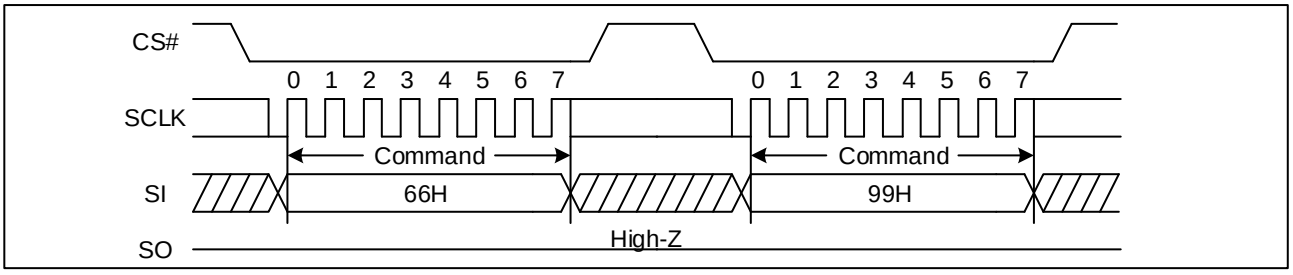


7.25 Enable Reset (66H) and Reset (99H)

If the Reset command is accepted, any on-going internal operation will be terminated and the device will return to its default power-on state and lose all the current volatile settings, such as Volatile Status Register bits, Write Enable Latch status (WEL), Program/Erase Suspend status, Read Parameter setting (P7-P0), Deep Power Down Mode, Continuous Read Mode bit setting (M7-M0) and Wrap Bit Setting (W6-W4).

The “Enable Reset (66H)” and “Reset (99H)” command sequence as follow: CS# goes low → Sending Enable Reset command → CS# goes high → CS# goes low → Sending Reset command → CS# goes high. Once the Reset command is accepted by the device, the device will take approximately t_{RST} / t_{RST_E} to reset. During this period, no command will be accepted. Data corruption may happen if there is an on-going or suspended internal Erase or Program operation when Reset command sequence is accepted by the device. It is recommended to check the WIP bit and the SUS1/SUS2 bit in Status Register before issuing the Reset command sequence.

Figure 28. Enable Reset and Reset command Sequence Diagram



7.26 Program/Erase Suspend (PES) (75H)

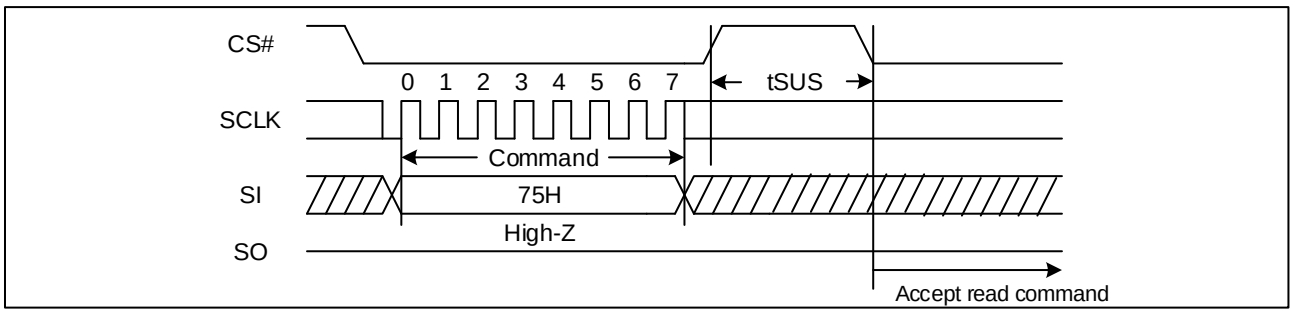
The Program/Erase Suspend command “75H”, allows the system to interrupt a page program or sector/block erase operation and then read data from any other sector or block. The Write Status Register command (01H) and Erase/Program Security Registers command (44H, 42H) and Erase commands (20H, 52H, D8H, C7H, 60H) and Page Program command (02H, 32H) are not allowed during Program suspend. The Write Status Register command (01H) and Erase Security Registers command (44H) and Erase commands (20H, 52H, D8H, C7H, 60H) are not allowed during Erase suspend.

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Program/Erase Suspend is valid only during the page program or sector/block erase operation. A maximum of time of “tsus” (See AC Characteristics) is required to suspend the program/erase operation.

The Program/Erase Suspend command will be accepted by the device only if the SUS1/SUS2 bit in the Status Register equal to 0 and WIP bit equal to 1 while a Page Program or a Sector or Block Erase operation is on-going. If the SUS1/SUS2 bit equal to 1 or WIP bit equal to 0, the Suspend command will be ignored by the device. The WIP bit will be cleared from 1 to 0 within “tsus” and the SUS1/SUS2 bit will be set from 0 to 1 immediately after Program/Erase Suspend. A power-off during the suspend period will reset the device and release the suspend state.

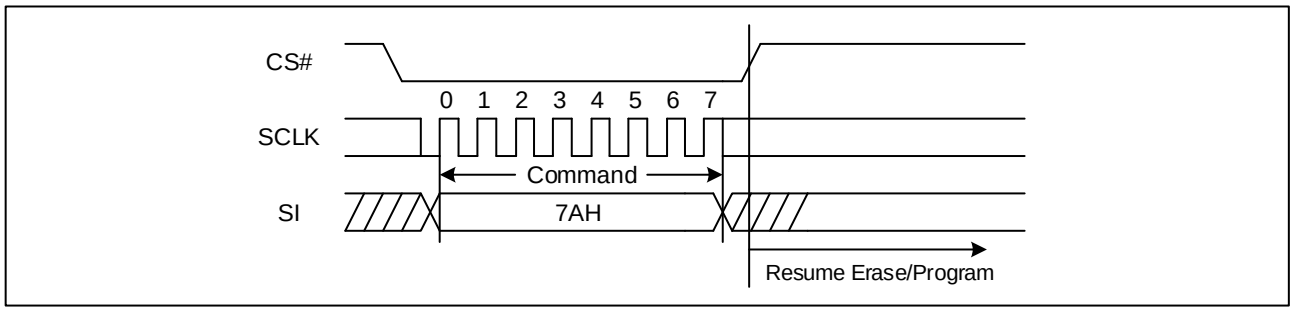
Figure 29. Program/Erase Suspend Sequence Diagram



7.27 Program/Erase Resume (PER) (7AH)

The Program/Erase Resume command must be written to resume the program or sector/block erase operation after a Program/Erase Suspend command. The Program/Erase Resume command will be accepted by the device only if the SUS1/SUS2 bit equal to 1 and the WIP bit equal to 0. After issued the SUS1/SUS2 bit in the status register will be cleared from 1 to 0 immediately, the WIP bit will be set from 0 to 1 within 200ns and the Sector or Block will complete the erase operation or the page will complete the program operation. The Program/Erase Resume command will be ignored unless a Program/Erase Suspend is active.

Figure 30. Program/Erase Resume Sequence Diagram



7.28 Deep Power-Down (DP) (B9H)

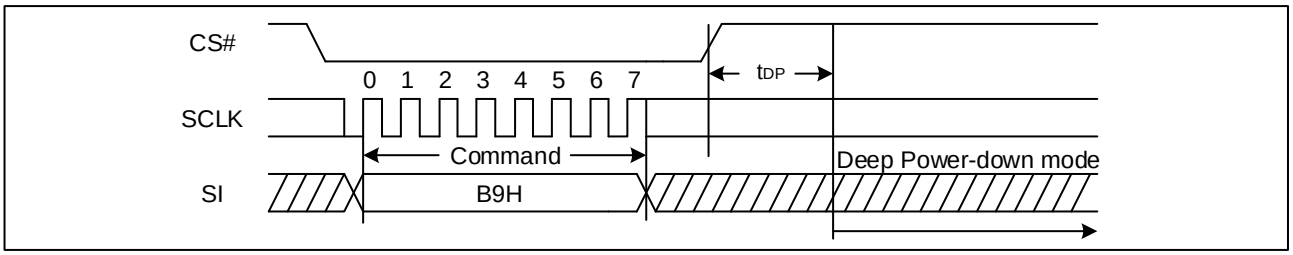
Executing the Deep Power-Down (DP) command is the only way to put the device in the lowest consumption mode (the Deep Power-Down Mode). It can also be used as an extra software protection mechanism, while the device is not in active use, since in this mode, the device ignores all Write, Program and Erase commands. Driving CS# high deselects the device, and puts the device in the Standby Mode (if there is no internal cycle currently in progress). But this mode is not the Deep Power-Down Mode. The Deep Power-Down Mode can only be entered by executing the Deep Power-Down (DP) command. Once the device has entered the Deep Power-Down Mode, all commands are ignored except the Release from Deep Power-Down and Read Device ID (RDI) command or software reset command. The Release from Deep Power-Down and Read Device ID (RDI) command releases the device from Deep Power-Down mode, also allows the Device ID of the device to be output on SO.

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The Deep Power-Down Mode automatically stops at Power-Down, and the device always in the Standby Mode after Power-Up.

The Deep Power-Down command sequence: CS# goes low → sending Deep Power-Down command → CS# goes high. CS# must be driven high after the eighth bit of the command code has been latched in; otherwise the Deep Power-Down (DP) command is not executed. As soon as CS# is driven high, it requires a delay of t_{DP} before the supply current is reduced to I_{CC2} and the Deep Power-Down Mode is entered. Any Deep Power-Down (DP) command, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 31. Deep Power-Down Sequence Diagram



7.29 Release from Deep Power-Down and Read Device ID (RDI) (ABH)

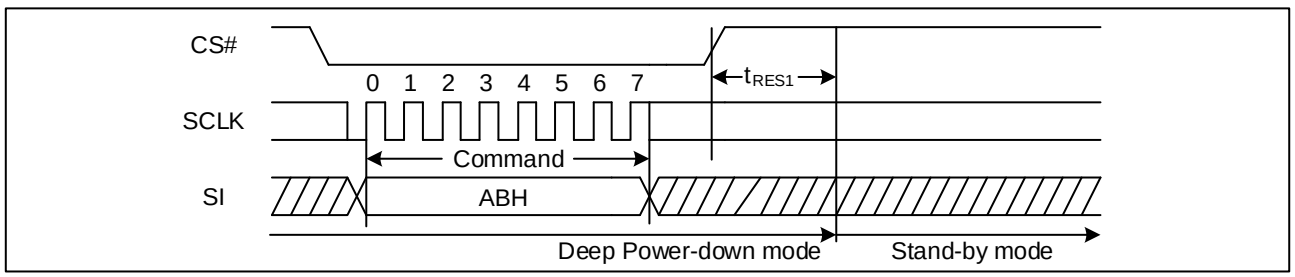
The Release from Power-Down and Read Device ID command is a multi-purpose command. It can be used to release the device from the Power-Down state or obtain the devices electronic identification (ID) number.

To release the device from the Power-Down state, the command is issued by driving the CS# pin low, shifting the instruction code "ABH" and driving CS# high. Release from Power-Down will take the time duration of t_{RES1} (See AC Characteristics) before the device will resume normal operation and other command are accepted. The CS# pin must remain high during the t_{RES1} time duration.

When used only to obtain the Device ID while not in the Power-Down state, the command is initiated by driving the CS# pin low and shifting the instruction code "ABH" followed by 3-dummy byte. The ID7~ID0 are then shifted out on the falling edge of SCLK with most significant bit (MSB) first. The Device ID value is listed in Manufacturer and Device Identification table. The Device ID can be read continuously. The command is completed by driving CS# high.

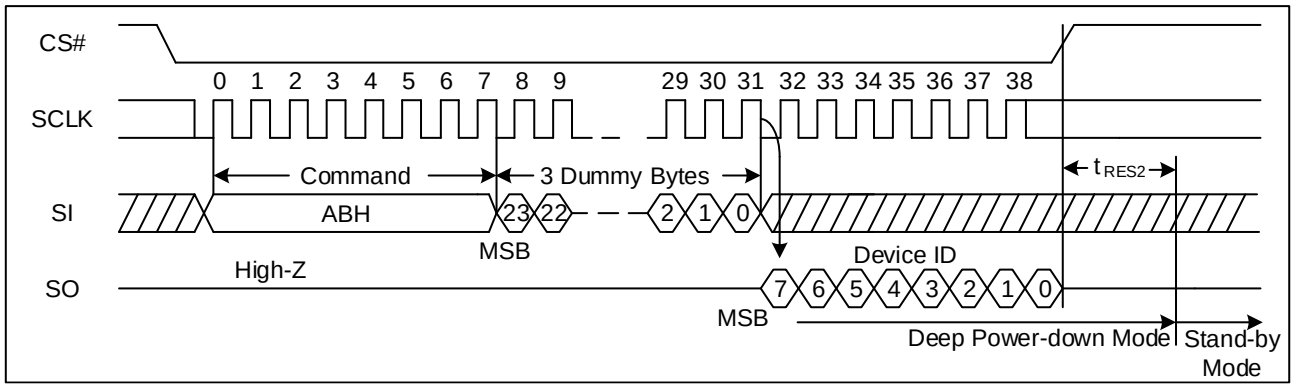
When used to release the device from the Power-Down state and obtain the ID7~ID0, the command is the same as previously described, except that after CS# is driven high it must remain high for a time duration of t_{RES2} (See AC Characteristics). After this time duration the device will resume normal operation and other command will be accepted. If the Release from Power-Down / Device ID command is issued while an Erase, Program or Write cycle is in process (when WIP equals 1) the command is ignored and will not have any effects on the current cycle.

Figure 32. Release Power-Down Sequence Diagram



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Figure 33. Release Power-Down/Read Device ID Sequence Diagram



7.30 Read Serial Flash Discoverable Parameter (5AH)

The Serial Flash Discoverable Parameter (SFDP) standard provides a consistent method of describing the functional and feature capabilities of serial flash devices in a standard set of internal parameter tables. These parameter tables can be interrogated by host system software to enable adjustments needed to accommodate divergent features from multiple vendors. The concept is similar to the one found in the Introduction of JEDEC Standard, JESD68 on CFI. SFDP is a standard of JEDEC Standard No.216B.

Figure 34. Read Serial Flash Discoverable Parameter command Sequence Diagram

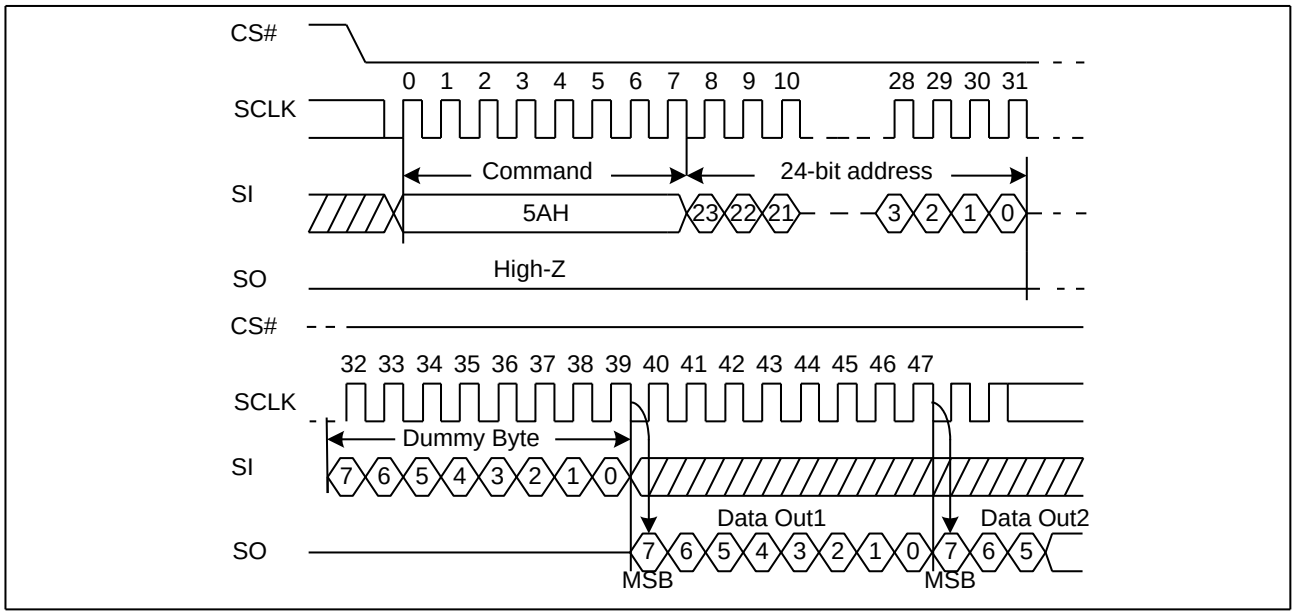


Table 9. Signature and Parameter Identification Data Values (Please contact GigaDevice for Details)

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8 ELECTRICAL CHARACTERISTICS

8.1 Power-On Timing

Figure 35. Power-On Timing Sequence Diagram

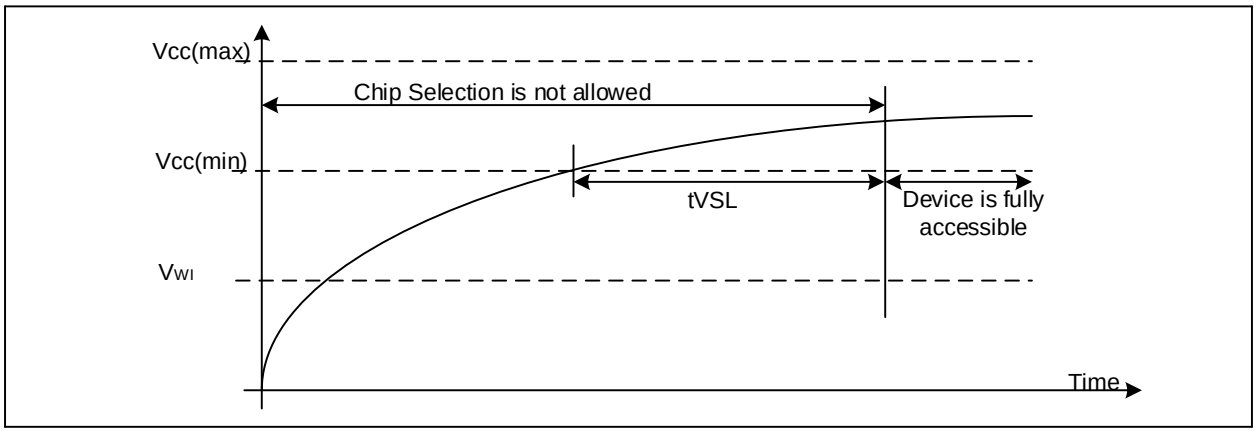


Table 10. Power-Up Timing and Write Inhibit Threshold

Symbol	Parameter	Min.	Max.	Unit
tVSL	VCC (min.) to device operation	700		μs
VWI	Write Inhibit Voltage	1	1.4	V

8.2 Initial Delivery State

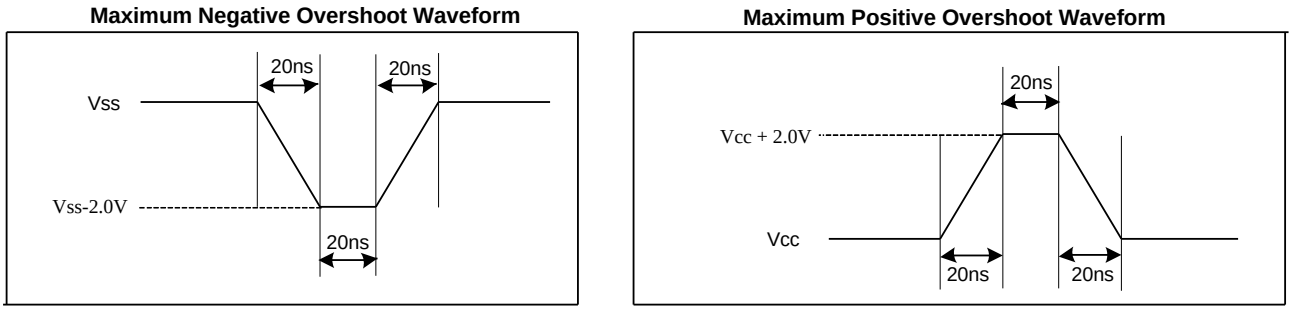
The device is delivered with the memory array erased: all bits are set to 1 (each Byte contains FFH). The Status Register contains 00H (all Status Register bits are 0).

8.3 Absolute Maximum Ratings

Parameter	Value	Unit
Ambient Operating Temperature (T_A)	-40 to 85	℃
Storage Temperature	-65 to 150	℃
Transient Input/Output Voltage (note: overshoot)	-2.0 to VCC+2.0	V
Applied Input/Output Voltage	-0.6 to VCC+0.4	V
VCC	-0.6 to 2.5	V

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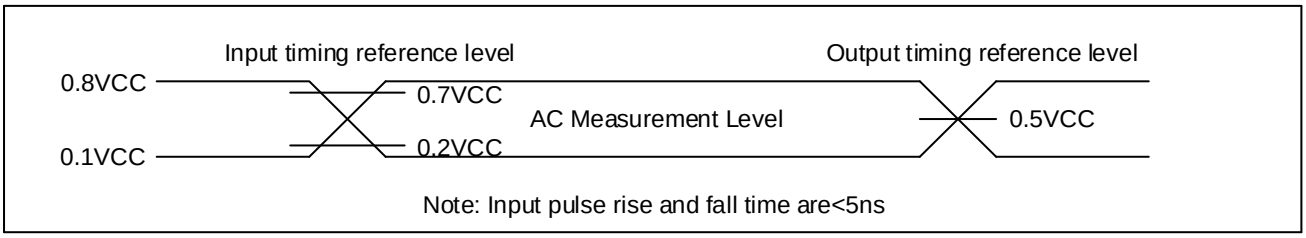
Figure 36. Input Test Waveform and Measurement Level



8.4 Capacitance Measurement Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
CIN	Input Capacitance			6	pF	VIN=0V
COUT	Output Capacitance			8	pF	VOUT=0V
C_L	Load Capacitance		30		pF	
	Input Rise And Fall time			5	ns	
	Input Pulse Voltage		0.1VCC to 0.8VCC		V	
	Input Timing Reference Voltage		0.2VCC to 0.7VCC		V	
	Output Timing Reference Voltage		0.5VCC		V	

Figure 37. Absolute Maximum Ratings Diagram



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8.5 DC Characteristics

(T_A = -40℃~85℃, VCC=1.65~2.0V)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit.
I_{LI}	Input Leakage Current				±2	μA
I_{LO}	Output Leakage Current				±2	μA
I_{CC1}	Standby Current	CS#=VCC, VIN=VCC or VSS		10	25	μA
I_{CC2}	Deep Power-Down Current	CS#=VCC, VIN=VCC or VSS		1	8	μA
I_{CC3}	Operating Current (Read)	CLK=0.1VCC / 0.9VCC at 133MHz, Q=Open(x4 I/O)		10	15	mA
		CLK=0.1VCC / 0.9VCC at 80MHz, Q=Open(x4 I/O)		8	12	mA
		CLK=0.1VCC / 0.9VCC at 80MHz, Q=Open(x1 I/O)		3	5	mA
I_{CC4}	Operating Current (PP)	CS#=VCC		8	15	mA
I_{CC5}	Operating Current (WRSR)	CS#=VCC		8	15	mA
I_{CC6}	Operating Current (SE)	CS#=VCC		8	15	mA
I_{CC7}	Operating Current (BE)	CS#=VCC		8	15	mA
I_{CC8}	Operating Current (CE)	CS#=VCC		8	15	mA
V_{IL}	Input Low Voltage				0.2VCC	V
V_{IH}	Input High Voltage		0.7VCC			V
V_{OL}	Output Low Voltage	I_{OL} = 100μA			0.2	V
V_{OH}	Output High Voltage	I_{OH} = -100μA	VCC-0.2			V

Note:

1. Typical value at T_A = 25℃, VCC = 1.8V.
2. Value guaranteed by design and/or characterization, not 100% tested in production.

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8.6 AC Characteristics

(T_A = -40℃~85℃, VCC=1.65~2.0V)

Symbol	Parameter	Min.	Typ.	Max.	Unit.
f_{C1}	Serial Clock Frequency For: all commands except 03H			133	MHz
f_R	Serial Clock Frequency For: Read (03H)			80	MHz
t_{CLH}	Serial Clock High Time	45% (1/Fc)			ns
t_{CLL}	Serial Clock Low Time	45% (1/Fc)			ns
t_{CLCH}	Serial Clock Rise Time (Slew Rate)	0.2			V/ns
t_{CHCL}	Serial Clock Fall Time (Slew Rate)	0.2			V/ns
t_{SLCH}	CS# Active Setup Time	5			ns
t_{CHSH}	CS# Active Hold Time	5			ns
t_{SHCH}	CS# Not Active Setup Time	5			ns
t_{CHSL}	CS# Not Active Hold Time	5			ns
t_{SHSL}	CS# High Time (Read/Write)	20			ns
t_{SHQZ}	Output Disable Time			6	ns
t_{CLQX}	Output Hold Time	1.2			ns
t_{DVCH}	Data In Setup Time	2			ns
t_{CHDX}	Data In Hold Time	2			ns
t_{HLCH}	HOLD# Low Setup Time (Relative To Clock)	5			ns
t_{HHCH}	HOLD# High Setup Time (Relative To Clock)	5			ns
t_{CHHH}	HOLD# Low Hold Time (Relative To Clock)	5			ns
t_{CHHL}	HOLD# High Hold Time (Relative To Clock)	5			ns
t_{HLQZ}	HOLD# Low To High-Z Output			6	ns
t_{HHQX}	HOLD# High To Low-Z Output			6	ns
t_{CLQV}	Clock Low To Output Valid (CL = 30pF)			7	ns
	Clock Low To Output Valid (CL = 15pF)			6	ns
t_{WHSL}	Write Protect Setup Time Before CS# Low	20			ns
t_{SHWL}	Write Protect Hold Time After CS# High	100			ns
t_{DP}	CS# High To Deep Power-Down Mode			3	μs
t_{RES1}	CS# High To Standby Mode Without Electronic Signature Read			20	μs
t_{RES2}	CS# High To Standby Mode With Electronic Signature Read			20	μs
t_{SUS}	CS# High To Next Command After Suspend			20	μs
t_{RS}	Latency Between Resume And Next Suspend	100			μs
t_{RST}	CS# High To Next Command After Reset (Except From Erase)			30	μs
t_{RST_E}	CS# High To Next Command After Reset (From Erase)			12	ms

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t_W	Write Status Register Cycle Time		2	25	ms
t_{BP1}	Byte Program Time (First Byte)		30	60	μs
t_{BP2}	Additional Byte Program Time (After First Byte)		2.5	5	μs
t_{PP}	Page Programming Time		0.4	2.4	ms
t_{SE}	Sector Erase Time		40	300	ms
t_{BE1}	Block Erase Time (32K Bytes)		0.15	0.8	s
t_{BE2}	Block Erase Time (64K Bytes)		0.2	1.2	s
t_{CE}	Chip Erase Time (GD25LQ40E)		1	3	s
	Chip Erase Time (GD25LQ20E)		0.5	1.5	s

Note:

1. Typical value at T_A = 25℃.
2. Value guaranteed by design and/or characterization, not 100% tested in production.

Figure 38. Input Timing

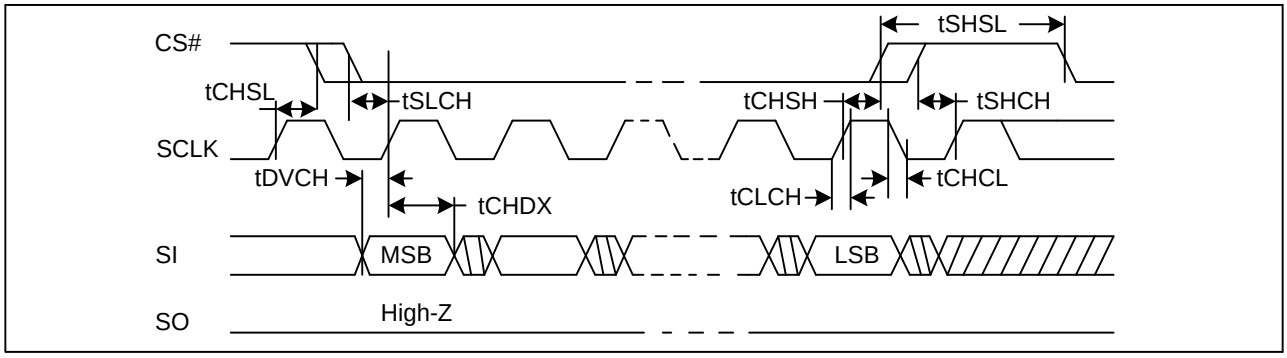
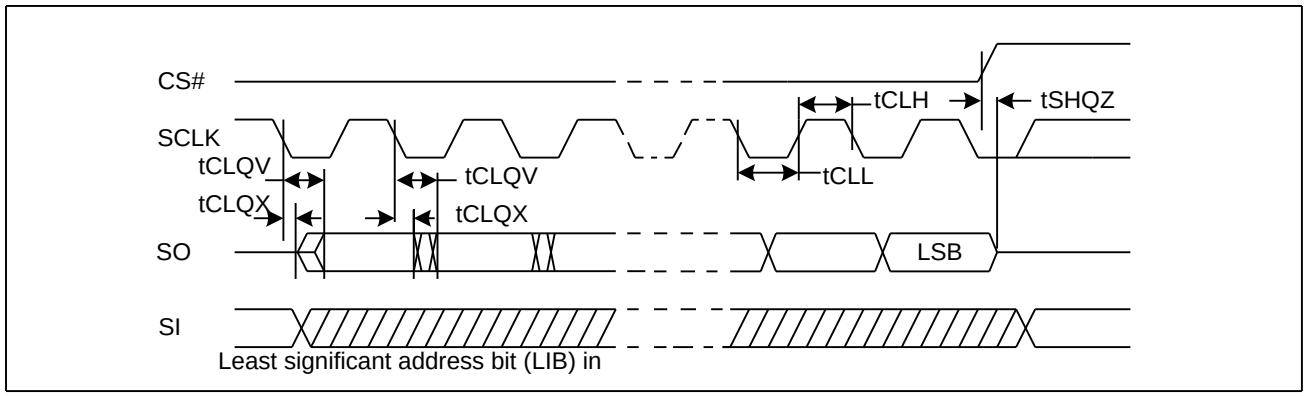


Figure 39. Output Timing



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Figure 40. Resume to Suspend Timing Diagram

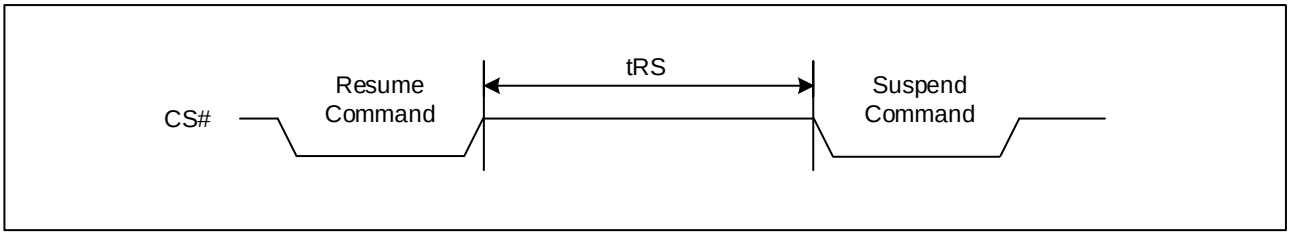


Figure 41. HOLD# Timing

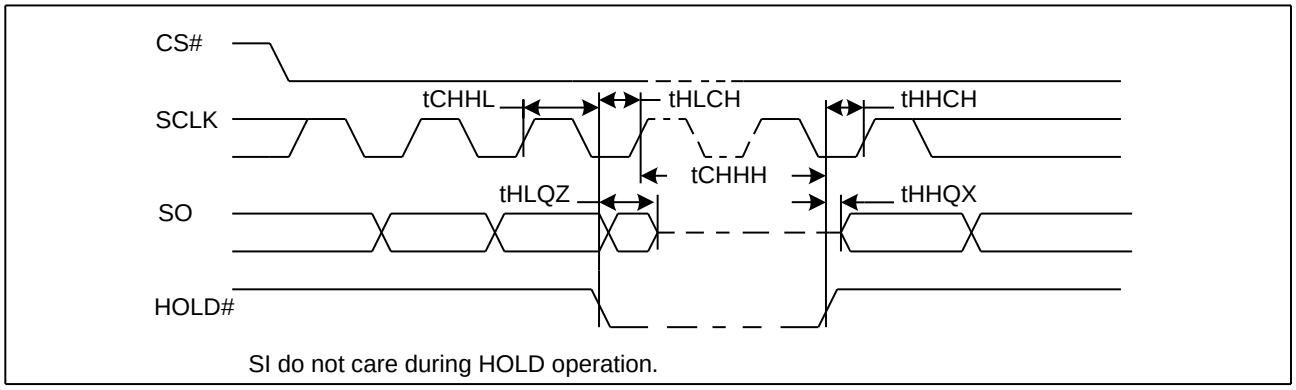
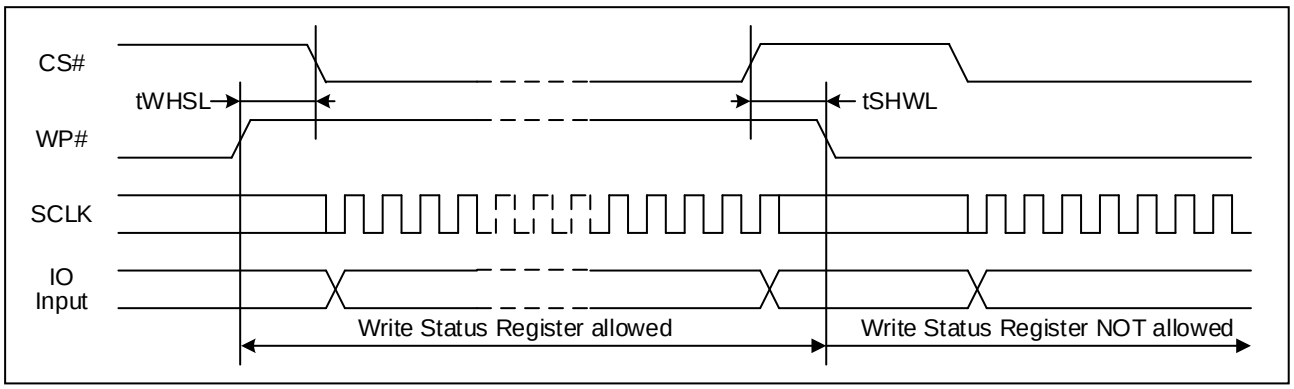
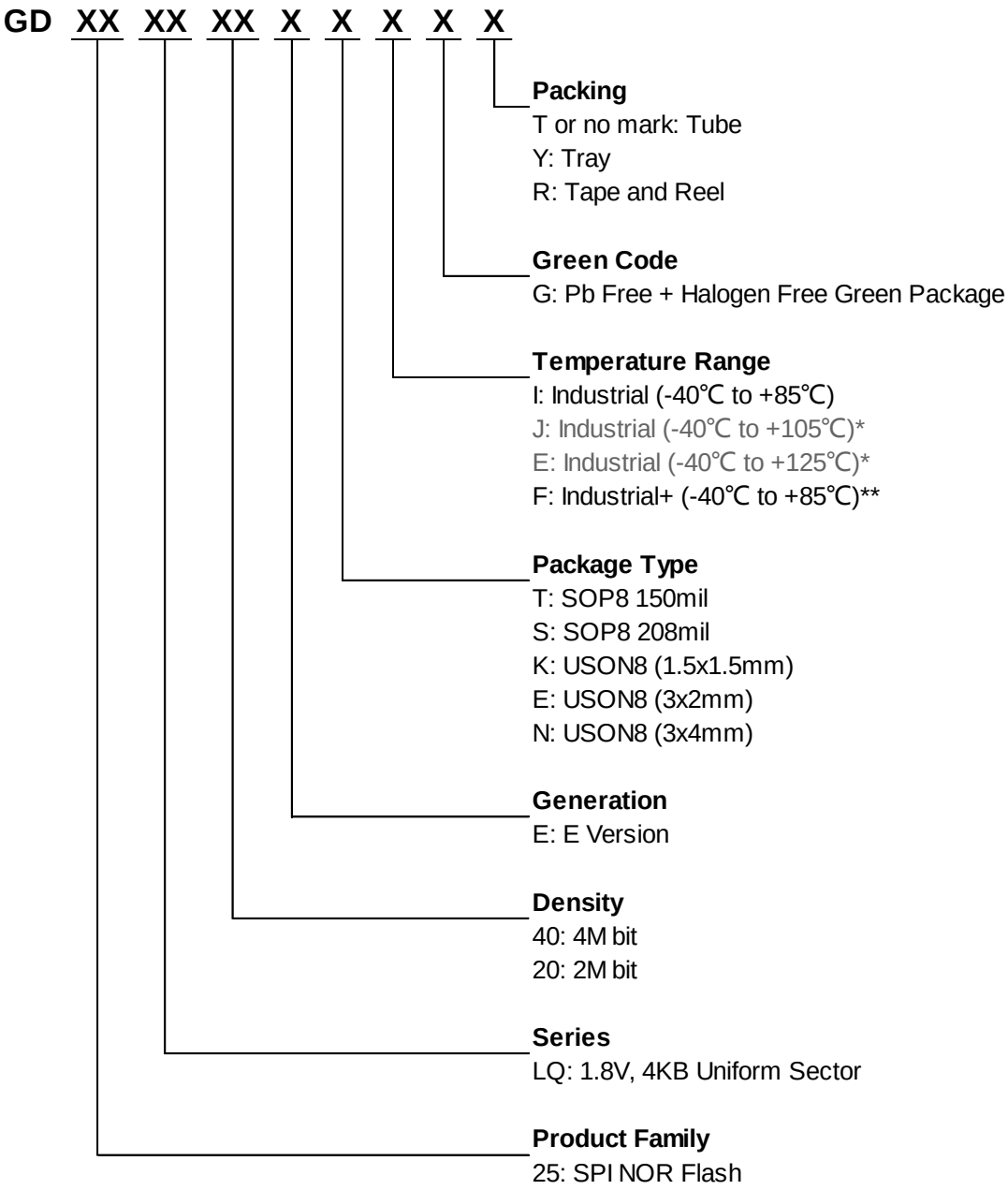


Figure 42. WP# Timing



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9 ORDERING INFORMATION



***This datasheet applies to temperature range I: Industrial (-40℃ to +85℃) and F: Industrial+ (-40℃ to +85℃) only. Please contact GigaDevice sales for extended temperature industrial products.**

****F grade has implemented additional test flows to ensure higher product quality than I grade.**

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9.1 Valid Part Numbers

Please contact GigaDevice regional sales for the latest product selection and available form factors.

Temperature Range I: Industrial (-40℃ to +85℃)

Product Number	Density	Package Type	Packing Options
GD25LQ40ETIG	4Mbit	SOP8 150mil	T/Y/R
GD25LQ20ETIG	2Mbit		
GD25LQ40ESIG	4Mbit	SOP8 208mil	T/Y/R
GD25LQ20ESIG	2Mbit		
GD25LQ40EKIG	4Mbit	USON8 (1.5x1.5mm)	R
GD25LQ20EKIG	2Mbit		
GD25LQ40EEIG	4Mbit	USON8 (3x2mm)	R
GD25LQ20EEIG	2Mbit		
GD25LQ40ENIG	4Mbit	USON8 (3x4mm)	R
GD25LQ20ENIG	2Mbit		

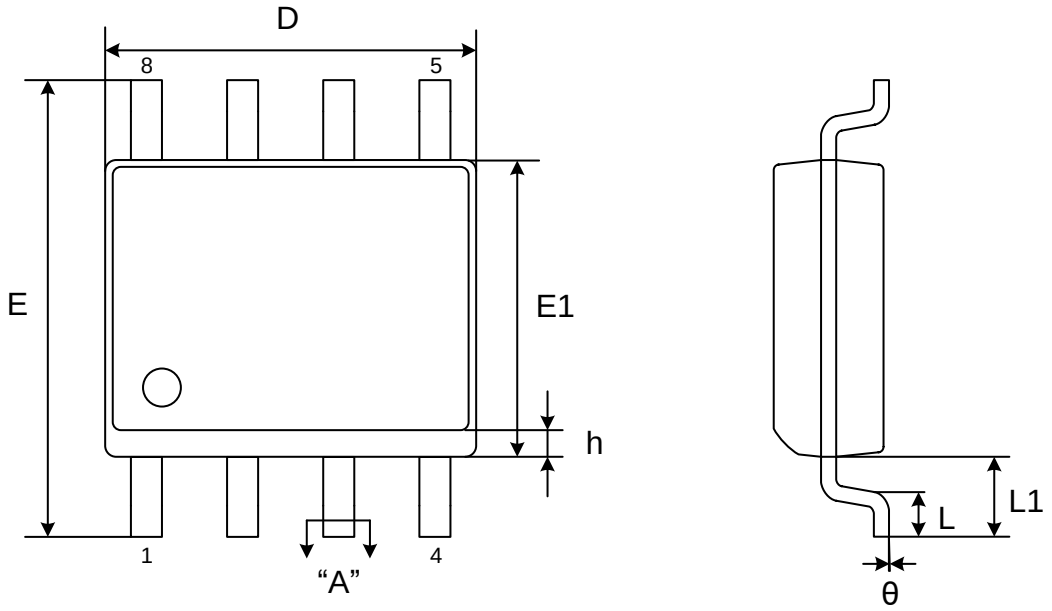
Temperature Range F: Industrial+ (-40℃ to +85℃)

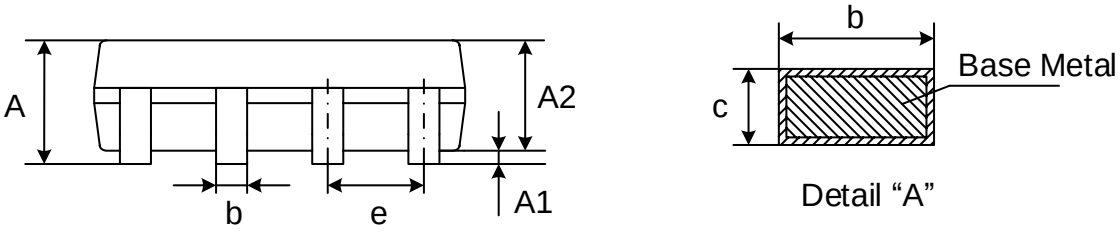
Product Number	Density	Package Type	Packing Options
GD25LQ40ETFG	4Mbit	SOP8 150mil	T/Y/R
GD25LQ20ETFG	2Mbit		
GD25LQ40ESFG	4Mbit	SOP8 208mil	T/Y/R
GD25LQ20ESFG	2Mbit		
GD25LQ40EKFG	4Mbit	USON8 (1.5x1.5mm)	R
GD25LQ20EKFG	2Mbit		
GD25LQ40EEFG	4Mbit	USON8 (3x2mm)	R
GD25LQ20EEFG	2Mbit		
GD25LQ40ENFG	4Mbit	USON8 (3x4mm)	R
GD25LQ20ENFG	2Mbit		

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10 PACKAGE INFORMATION

10.1 Package SOP8 150MIL





Dimensions

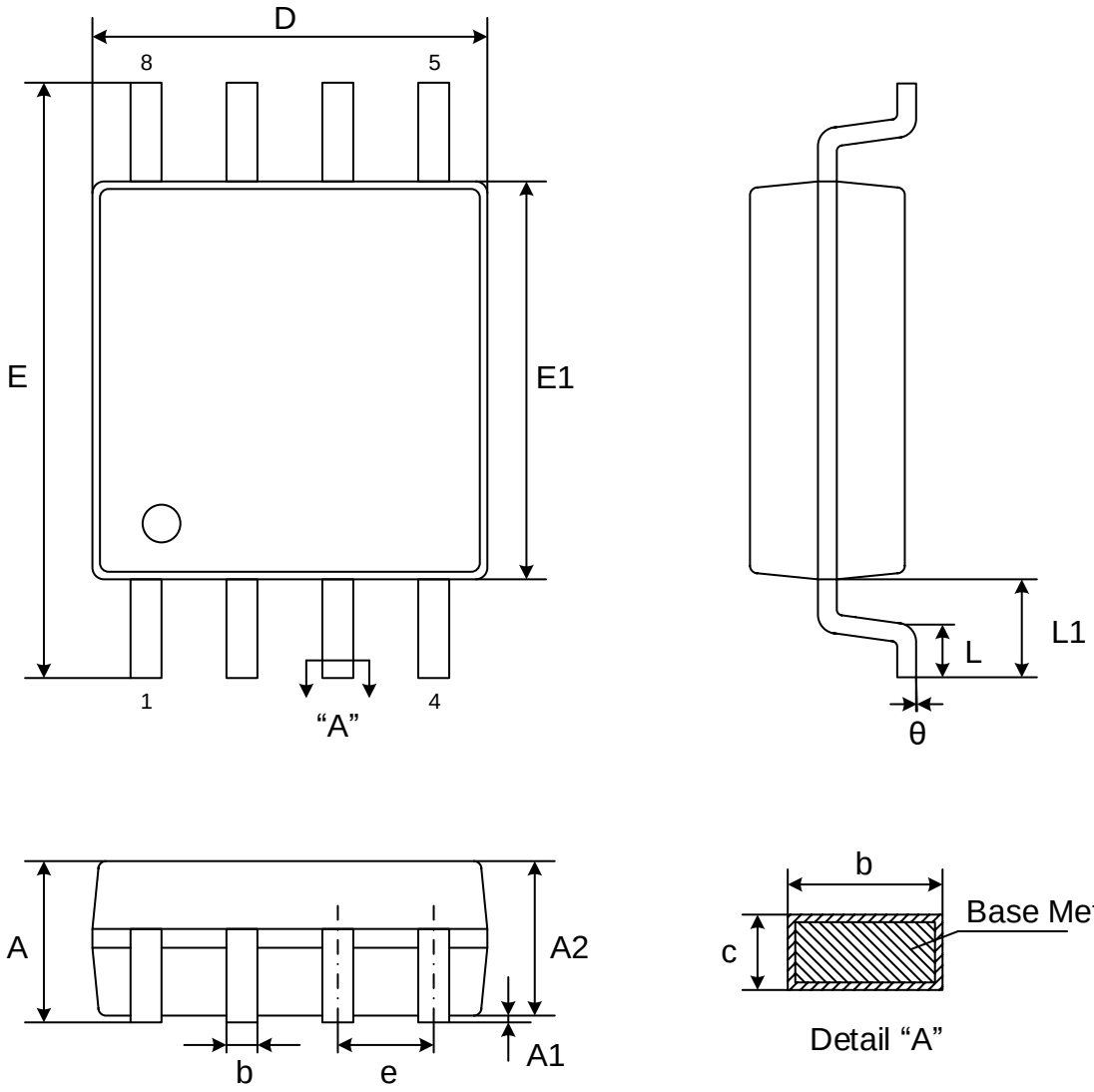
Symbol / Unit		A	A1	A2	b	c	D	E	E1	e	L	L1	h	θ
mm	Min	-	0.10	1.25	0.31	0.10	4.80	5.80	3.80	1.27	0.40	1.04	0.25	0°
	Nom	-	0.15	1.45	0.41	0.20	4.90	6.00	3.90		-		-	-
	Max	1.75	0.25	1.55	0.51	0.25	5.00	6.20	4.00		0.90		0.50	8°

Note:

1. Both the package length and width do not include the mold flash.
2. Seating plane: Max. 0.1mm.

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10.2 Package SOP8 208MIL



Dimensions

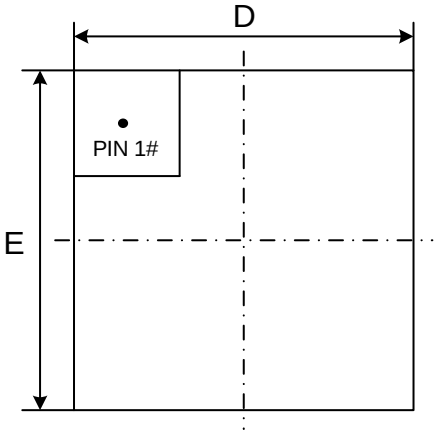
Symbol / Unit		A	A1	A2	b	c	D	E	E1	e	L	L1	θ
mm	Min	-	0.05	1.70	0.31	0.15	5.13	7.70	5.18	1.27	0.50	1.31	0°
	Nom	-	0.15	1.80	0.41	0.20	5.23	7.90	5.28		-		-
	Max	2.16	0.25	1.90	0.51	0.25	5.33	8.10	5.38		0.85		8°

Note:

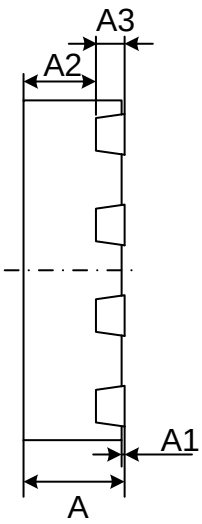
1. Both the package length and width do not include the mold flash.
2. Seating plane: Max. 0.1mm.

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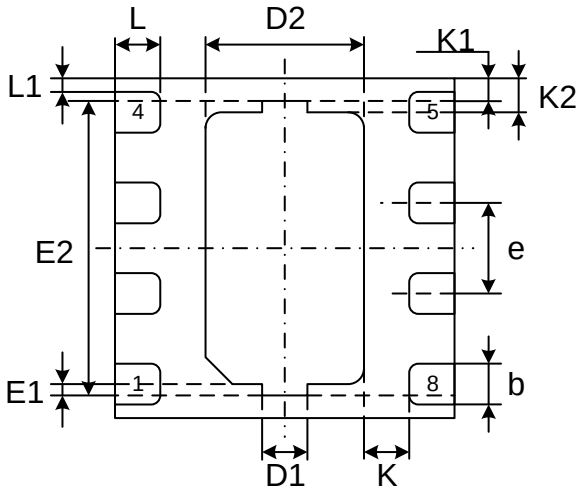
10.3 Package USON8 (1.5x1.5mm)



Top View



Side View



Bottom View

Dimensions

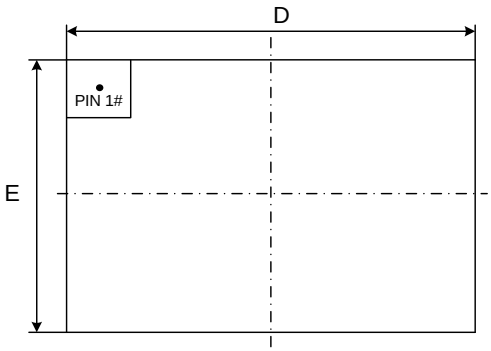
Symbol / Unit		A	A1	A2	A3	b	D	E	D1	E1	D2	E2	e	L	L1	K	K1	K2
mm	Min	0.40	0.00	0.33 REF	0.127 REF	0.13	1.40	1.40	0.20 REF	0.05 REF	0.60	1.20	0.40 REF	0.15	0.06 REF	0.20 REF	0.10 REF	0.15 REF
	Nom	0.45	0.02			0.18	1.50	1.50			0.70	1.30		0.20				
	Max	0.50	0.05			0.25	1.60	1.60			0.80	1.40		0.25				

Note:

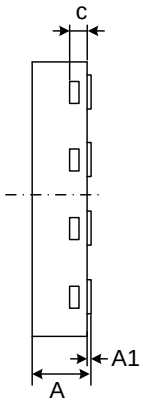
1. Both the package length and width do not include the mold flash.
2. The exposed metal pad area on the bottom of the package is floating.
3. Coplanarity ≤0.08mm. Package edge tolerance≤0.10mm.
4. The lead shape may be of little difference according to different package factories. These lead shapes are compatible with each other.

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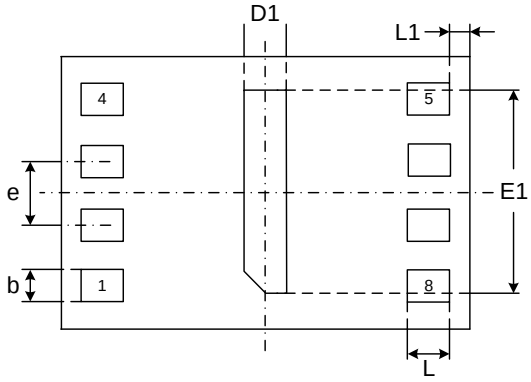
10.4 Package USON8 (3x2mm)



Top View



Side View



Bottom View

Dimensions

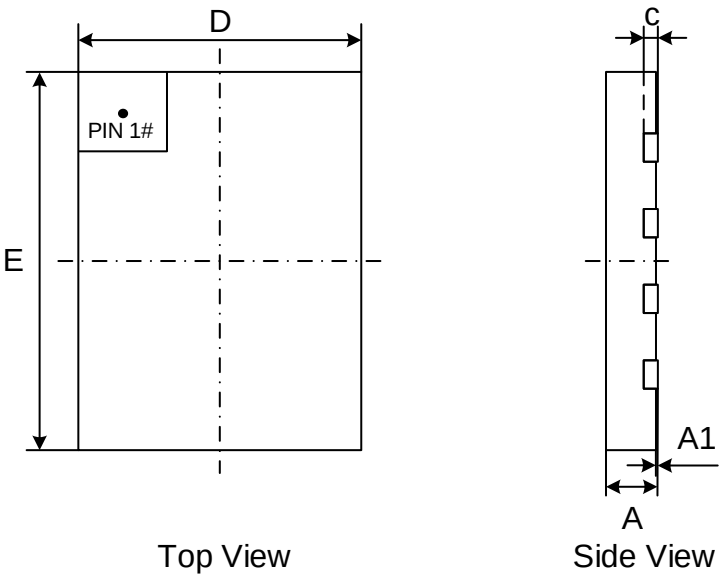
Symbol / Unit		A	A1	c	b	D	D1	E	E1	e	L	L1
mm	Min	0.40	0.00	0.10	0.20	2.90	0.15	1.90	1.55	0.50	0.30	0.10
	Nom	0.45	0.02	0.15	0.25	3.00	0.20	2.00	1.60		0.35	
	Max	0.50	0.05	0.20	0.30	3.10	0.25	2.10	1.65		0.40	

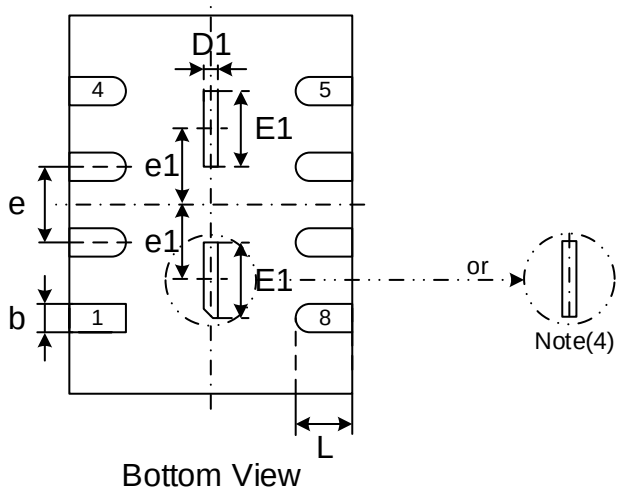
Note:

1. Both the package length and width do not include the mold flash.
2. The exposed metal pad area on the bottom of the package is floating.
3. Coplanarity ≤0.08mm. Package edge tolerance≤0.10mm.
4. The lead shape may be of little difference according to different package factories. These lead shapes are compatible with each other.

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10.5 Package USON8 (3x4mm)





Dimensions

Symbol / Unit		A	A1	c	b	D	D1	E	E1	e	e1	L
mm	Min	0.50	0.00	0.10	0.25	2.90	0.10	3.90	0.70	0.80 BSC	0.80 BSC	0.50
	Nom	0.55	0.02	0.15	0.30	3.00	0.20	4.00	0.80			0.60
	Max	0.60	0.05	0.20	0.35	3.10	0.30	4.10	0.90			0.70

Note:

1. Both the package length and width do not include the mold flash.
2. The exposed metal pad area on the bottom of the package is floating.
3. Coplanarity ≤0.08mm. Package edge tolerance≤0.10mm.
4. The lead shape may be of little difference according to different package factories. These lead shapes are compatible with each other.

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11 REVISION HISTORY

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