GD25D80E

DATASHEET

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1 FEATURES

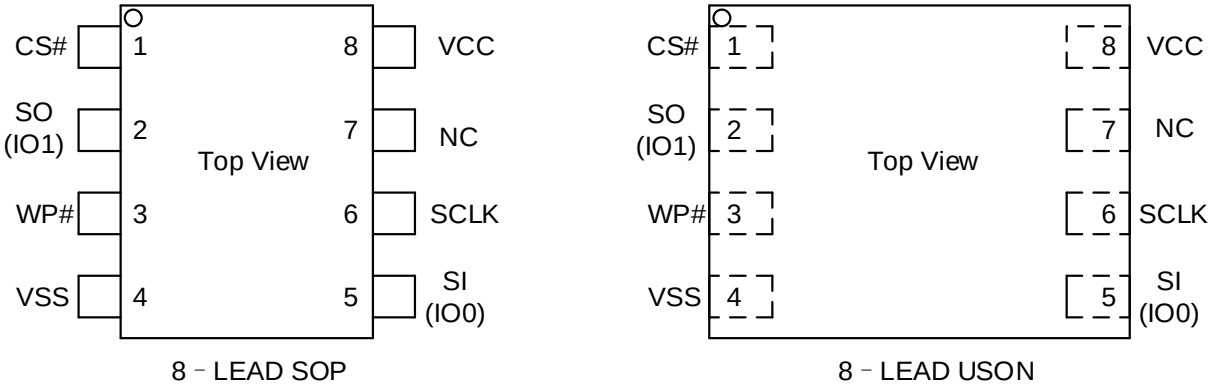
- 8M-bit Serial Flash
  - 1024K-Byte
  - 256 Bytes per programmable page
- Standard, Dual Output
  - Standard SPI: SCLK, CS#, SI, SO, WP#
  - Dual Output: SCLK, CS#, IO0, IO1, WP#
- High Speed Clock Frequency
  - 104MHz for fast read
  - Dual Output Data transfer up to 208Mbits/s
- Software/Hardware Write Protection
  - Write protect all/portion of memory via software
  - Enable/Disable protection with WP# Pin
  - Top/Bottom Block protection
- Endurance and Data Retention
  - Minimum 100,000 Program/Erase Cycles
  - 20-year data retention typical
- Fast Program/Erase Speed
  - Page Program time: 0.6ms typical
  - Sector Erase time: 60ms typical
  - Block Erase time: 0.2s/0.35s typical
  - Chip Erase time: 6s typical
- Flexible Architecture
  - Uniform Sector of 4K-Byte
  - Uniform Block of 32/64K-Byte
- Low Power Consumption
  - 0.1μA typical standby current
  - 0.1μA typical deep power down current
- Advanced Security Features
  - 128-bit Unique ID for each device
  - 512-Byte Security Registers With OTP Locks
- Single Power Supply Voltage
  - Full voltage range: 2.7-3.6V
- Package Information
  - USON8 (1.5x1.5mm)
  - USON8 (3x2mm)
  - SOP8 150mil

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2 GENERAL DESCRIPTIONS

The GD25D80E (8M-bit) Serial flash supports the standard Serial Peripheral Interface (SPI), and the Dual Output: Serial Clock, Chip Select, Serial Data I/O0 (SI) and I/O1 (SO). The Dual Output data is transferred with speed of 208Mbit/s.

CONNECTION DIAGRAM



PIN DESCRIPTION

Table 1. Pin Description for SOP8/USON8 Package

Pin No.	Pin Name	I/O	Description
1	CS#	I	Chip Select Input
2	SO (IO1)	O	Data Output (Data Input Output 1)
3	WP#	I	Write Protect Input
4	VSS		Ground
5	SI (IO0)	I/O	Data Input (Data Input Output 0)
6	SCLK	I	Serial Clock Input
7	NC		No Connection
8	VCC		Power Supply

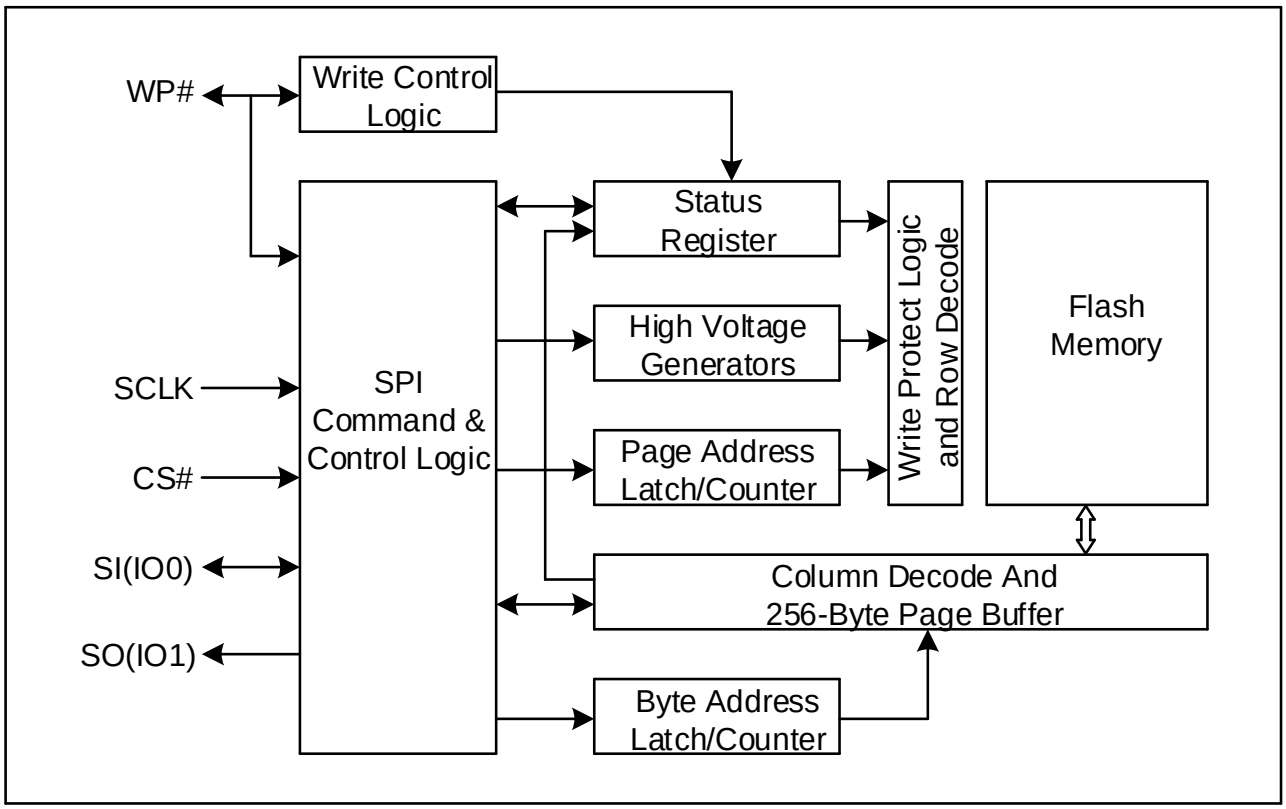
Note:

1.CS# must be driven high if chip is not selected. Please don't leave CS# floating any time after power is on.

2.If WP# is unused, it must be driven high by the host, or an external pull-up resistor must be placed on the PCB in order to avoid allowing the WP# input to float.

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BLOCK DIAGRAM



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3 MEMORY ORGANIZATION

GD25D80E

Each device has	Each block has	Each sector has	Each page has	
1M	64/32K	4K	256	Bytes
4K	256/128	16	-	pages
256	16/8	-	-	sectors
16/32	-	-	-	blocks

UNIFORM BLOCK SECTOR ARCHITECTURE

GD25D80E 64K Bytes Block Sector Architecture

Block	Sector	Address range	
15	255	0FF000H	0FFFFFH
	.....	.....	.....
	240	0F0000H	0F0FFFH
14	239	0EF000H	0EFFFFH
	.....	.....	.....
	224	0E0000H	0E0FFFH
.....	.....	.....	.....
	.....	.....	.....
	.....	.....	.....
.....	.....	.....	.....
	.....	.....	.....
	.....	.....	.....
2	47	02F000H	02FFFFH
	.....	.....	.....
	32	020000H	020FFFH
1	31	01F000H	01FFFFH
	.....	.....	.....
	16	010000H	010FFFH
0	15	00F000H	00FFFFH
	.....	.....	.....
	0	000000H	000FFFH

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4 DEVICE OPERATIONS

4.1 SPI Mode

Standard SPI

The GD25D80E features a serial peripheral interface on 4 signals bus: Serial Clock (SCLK), Chip Select (CS#), Serial Data Input (SI) and Serial Data Output (SO). Both SPI bus mode 0 and 3 are supported. Input data is latched on the rising edge of SCLK and data shifts out on the falling edge of SCLK.

Dual SPI

The GD25D80E supports Dual Output operation when using the “Dual Output Fast Read” (3BH) commands. These commands allow data to be transferred to or from the device at twice the rate of the standard SPI. When using the Dual Output command the SI pin becomes bidirectional I/O pins: IO0, and the SO pin becomes IO1.

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5 DATA PROTECTION

The GD25D80E provide the following data protection methods:

- Write Enable (WREN) command: The WREN command is set the Write Enable Latch bit (WEL). The WEL bit will return to reset by the following situation:
  -Power-Up
  -Write Disable (WRDI)
  -Write Status Register (WRSR)
  -Page Program (PP)
  -Sector Erase (SE) / Block Erase (BE) / Chip Erase (CE)
- Software Protection Mode: The Block Protect bits (BP2-BP0) define the section of the memory array that can be read but not changed.
- Hardware Protection Mode: WP# goes low to protect the Block Protect bits (BP2-BP0) and the SRP bit.
- Deep Power-Down Mode: In Deep Power-Down Mode, all commands are ignored except the Release from Deep Power-Down Mode command.
- Write Inhibit Voltage (VWI): Device would reset automatically when VCC is below a certain threshold VWI.

Table 2. GD25D80E Protected area size(8M, CMP=0)

Status Register Content			Memory Content			
BP2	BP1	BP0	Blocks	Addresses	Density	Portion
0	0	0	NONE	NONE	NONE	NONE
0	0	1	Sector 0 to 253	000000H-0FDFFFH	1016KB	Lower 254/256
0	1	0	Sector 0 to 251	000000H-0FBFFFH	1008KB	Lower 252/256
0	1	1	Sector 0 to 247	000000H-0F7FFFH	992KB	Lower 248/256
1	0	0	Sector 0 to 239	000000H-0EFFFFH	960KB	Lower 240/256
1	0	1	Sector 0 to 223	000000H-0DFFFFH	896KB	Lower 224/256
1	1	0	Sector 0 to 191	000000H-0BFFFFH	768KB	Lower 192/256
1	1	1	All	000000H-0FFFFFH	1024KB	ALL

Table 3. GD25D80E Protected area size (8M, CMP=1)

Status Register Content			Memory Content			
BP2	BP1	BP0	Blocks	Addresses	Density	Portion
0	0	0	ALL	000000H-0FFFFFH	1024KB	ALL
0	0	1	Sector 254 to 255	0FE000H-0FFFFFH	8KB	Upper 2/256
0	1	0	Sector 252 to 255	0FC000H-0FFFFFH	16KB	Upper 4/256
0	1	1	Sector 248 to 255	0F8000H-0FFFFFH	32KB	Upper 8/256
1	0	0	Sector 240 to 255	0F0000H-0FFFFFH	64KB	Upper 16/256
1	0	1	Sector 224 to 255	0E0000H-0FFFFFH	128KB	Upper 32/256
1	1	0	Sector 192 to 255	0C0000H-0FFFFFH	256KB	Upper 64/256
1	1	1	NONE	NONE	NONE	NONE

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6 STATUS REGISTER

Table 4. Status Register

No.	Name	Description	Note
S7	SRP	Status Register Protection Bit	Non-volatile writable
S6	LB	Security Register Lock Bit	Non-volatile writable (OTP)
S5	CMP	Complement Protect Bit	Non-volatile writable
S4	BP2	Block Protect Bit	Non-volatile writable
S3	BP1	Block Protect Bit	Non-volatile writable
S2	BP0	Block Protect Bit	Non-volatile writable
S1	WEL	Write Enable Latch	Volatile, read only
S0	WIP	Erase/Write In Progress	Volatile, read only

The status and control bits of the Status Register are as follows:

WIP bit

The Write in Progress (WIP) bit indicates whether the memory is busy in program/erase/write status register progress. When WIP bit sets to 1, means the device is busy in program/erase/write status register progress, when WIP bit sets 0, means the device is not in program/erase/write status register progress.

WEL bit

The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1 the internal Write Enable Latch is set, when set to 0 the internal Write Enable Latch is reset and no Write Status Register, Program or Erase command is accepted.

BP2, BP1, BP0 bits

The Block Protect (BP2, BP1, and BP0) bits are non-volatile. They define the size of the area to be software protected against Program and Erase commands. These bits are written with the Write Status Register (WRSR) command. When the Block Protect (BP2, BP1, BP0) bits are set to 1, the relevant memory area (as defined in Table2&3) becomes protected against Page Program (PP), Sector Erase (SE) and Block Erase (BE) commands. The Block Protect (BP2, BP1, and BP0) bits can be written provided that the Hardware Protected mode has not been set. The Chip Erase (CE) command is executed, if the Block Protect (BP2, BP1, and BP0) bits are 0 and CMP=0 or the Block Protect (BP2, BP1, and BP0) bits are 1 and CMP=1.

SRP bit

The Status Register Protect (SRP) bits are non-volatile Read/Write bits in the status register. The SRP bit controls the method of the write protection: software protected, hardware protected, or hardware unprotected.

Table 5. Status Register Protect (SRP) bit

SRP	WP#	Status Register	Description
0	X	Software Protected	The Status Register can be written to after a Write Enable command, WEL=1.(Default)
1	0	Hardware Protected	WP#=0, the Status Register locked and cannot be written to.

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1	1	Hardware Unprotected	WP#=1, the Status Register is unlocked and can be written to after a Write Enable command, WEL=1

CMP bit

The CMP bit is a non-volatile Read/Write bit in the Status Register (S5). It is used in conjunction with the BP2-BP0 bits to provide more flexibility for the array protection. Please see the Status registers Memory Protection table for details. The default setting is CMP=0.

LB bit

The LB bit is a non-volatile One Time Program (OTP) bit in Status Register (S6) that provide the write protect control and status to the Security Registers. The default state of LB is 0, the security registers are unlocked. LB can be set to 1 individually using the Write Register instruction. LB is One Time Programmable, once it is set to 1, the Security Registers will become read-only permanently.

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7 COMMAND DESCRIPTIONS

All commands, addresses and data are shifted in and out of the device, beginning with the most significant bit on the first rising edge of SCLK after CS# is driven low. Then, the one-byte command code must be shifted in to the device, with most significant bit first on SI, and each bit is latched on the rising edges of SCLK.

Every command sequence starts with a one-byte command code. Depending on the command, this might be followed by address bytes, or by data bytes, or by both or none. CS# must be driven high after the last bit of the command sequence has been completed. For the command of Read, Fast Read, Read Status Register or Release from Deep Power-Down, and Read Device ID, the shifted-in command sequence is followed by a data-out sequence. All read instruction can be completed after any bit of the data-out sequence is being shifted out, and then CS# must be driven high to return to deselected status.

For the command of Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Write Enable, Write Disable or Deep Power-Down command, CS# must be driven high exactly at a byte boundary, otherwise the command is rejected, and is not executed. That is CS# must be driven high when the number of clock pulses after CS# being driven low is an exact multiple of eight. For Page Program, if at any time the input byte is not a full byte, nothing will happen and WEL will not be reset.

Table 6. Commands

Command Name	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	Byte 8	Byte 9
Write Enable	06H								
Write Disable	04H								
Read Status Register	05H	(S7-S0)	(cont.)						
Write Status Register	01H	S7-S0							
Read Data	03H	A23-A16	A15-A8	A7-A0	(D7-D0)	(cont.)			
Fast Read	0BH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(cont.)		
Dual Output Fast Read	3BH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)(1)	(cont.)		
Page Program	02H	A23-A16	A15-A8	A7-A0	D7-D0	Next Byte			
Sector Erase	20H	A23-A16	A15-A8	A7-A0					
Block Erase (32K)	52H	A23-A16	A15-A8	A7-A0					
Block Erase (64K)	D8H	A23-A16	A15-A8	A7-A0					
Chip Erase	C7/60H								
Read Manufacturer/ Device ID	90H	00H	00H	00H	(MID7-MID0)	(ID7-ID0)	(cont.)		
Read Identification	9FH	(MID7-MID0)	(ID15-ID8)	(ID7-ID0)	(cont.)				
Read Unique ID	4BH	00H	00H	00H	dummy	(UID7-UID0)	(cont.)		
Erase Security Registers(2)	44H	A23-A16	A15-A8	A7-A0					

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Program Security Registers(2)	42H	A23-A16	A15-A8	A7-A0	D7-D0	Next Byte			
Read Security Registers(2)	48H	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(cont.)		
Deep Power-Down	B9H								
Release From Deep Power-Down	ABH								
Release From Deep Power-Down and Read Device ID	ABH	dummy	dummy	dummy	(ID7-ID0)	(cont.)			

Note:

1. Dual Output data

IO0 = (D6, D4, D2, D0)

IO1 = (D7, D5, D3, D1)

2. Security Registers Address

Security Register: A23-A16=00H, A15-A12=00H, A11-A9 = 000b, A8-A0= Byte Address;

TABLE OF ID DEFINITIONS

GD25D80E

Operation Code	MID7-MID0	ID15-ID8	ID7-ID0
9FH	C8	40	14
90H	C8		13
ABH			13

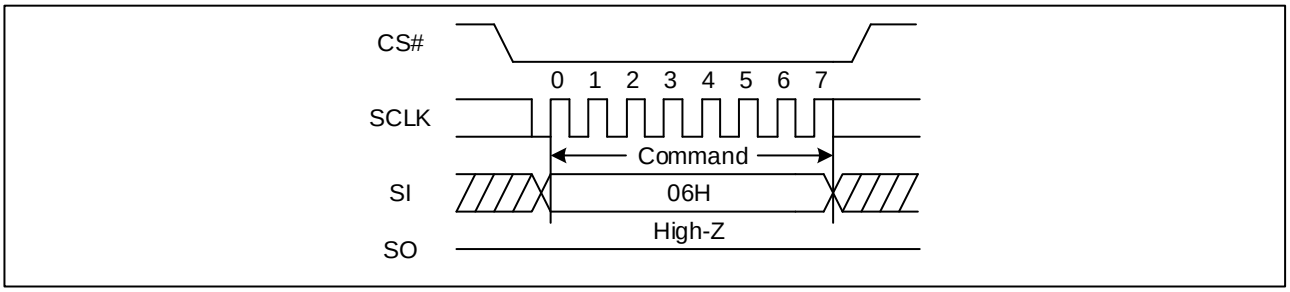
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7.1 Write Enable (WREN) (06H)

The Write Enable (WREN) command is for setting the Write Enable Latch (WEL) bit. The Write Enable Latch (WEL) bit must be set prior to every Page Program (PP), Sector Erase (SE), Block Erase (BE), Chip Erase (CE), Write Status Register (WRSR) and Erase/Program Security Registers command.

The Write Enable (WREN) command sequence: CS# goes low → sending the Write Enable command → CS# goes high.

Figure 1. Write Enable Sequence Diagram



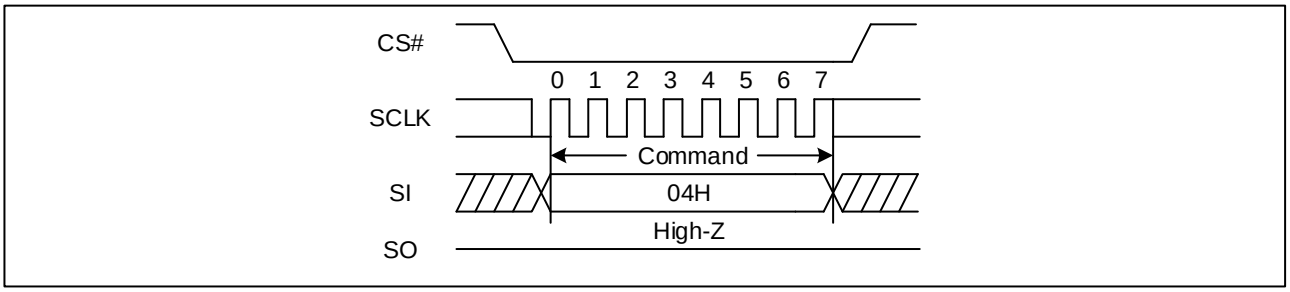
7.2 Write Disable (WRDI) (04H)

The Write Disable command is for resetting the Write Enable Latch (WEL) bit. The Write Enable Latch (WEL) bit may be set to 0 by issuing the Write Disable (WRDI) command to disable Page Program (PP), Sector Erase (SE), Block Erase (BE), Chip Erase (CE), Write Status Register (WRSR), that require WEL be set to 1 for execution. The WRDI command can be used by the user to protect memory areas against inadvertent writes that can possibly corrupt the contents of the memory. The WRDI command is ignored during an embedded operation while WIP bit =1.

The WEL bit is reset by following condition: Write Disable command (WRDI), Power-up, and upon completion of the Write Status Register, Page Program, Sector Erase, Block Erase and Chip Erase commands.

The Write Disable command sequence: CS# goes low →Sending the Write Disable command →CS# goes high.

Figure 2. Write Disable Sequence Diagram

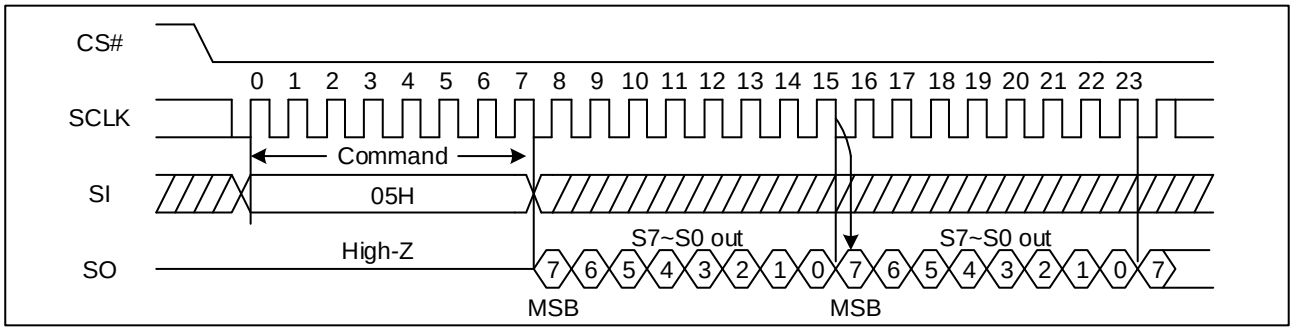


7.3 Read Status Register (RDSR) (05H)

The Read Status Register (RDSR) command is for reading the Status Register. The Status Register may be read at any time, even while a Program, Erase or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write in Progress (WIP) bit before sending a new command to the device. It is also possible to read the Status Register continuously. For command code “05H”, the SO will output Status Register bits S7~S0.

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Figure 3. Read Status Register Sequence Diagram



7.4 Write Status Register (WRSR) (01H)

The Write Status Register (WRSR) instruction allows new values to be written to the Status Register. A Write Enable (WREN) instruction must be executed previously to set the Write Enable Latch (WEL) bit, before it can be accepted.

The Write Status Register (WRSR) instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code and the data byte on Serial Data Input (SI).

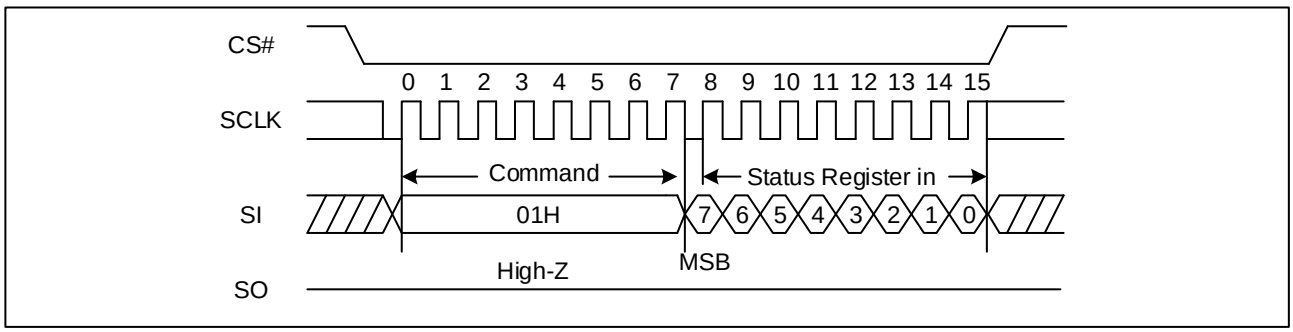
The Write Status Register (WRSR) instruction has no effect on S1 and S0 of the Status Register. S6 and S5 are always read as 0. Chip Select (CS#) must be driven High after the eighth bit of the data byte has been latched in. Otherwise, the Write Status Register (WRSR) instruction is not executed. As soon as Chip Select (CS#) is driven high, the self-timed Write Status Register cycle (the duration is tw) is initiated. While the Write Status Register cycle is in progress, reading Status Register to check the Write In Progress (WIP) bit is achievable.

The Write In Progress (WIP) bit is 1 during the self-timed Write Status Register cycle, and turn to 0 on the completion of the Write Status Register. When the cycle is completed, the Write Enable Latch (WEL) is reset to 0.

The Write Status Register (WRSR) instruction allows the user to change the values of the Block Protect (BP2, BP1, BP0) bits, which are utilized to define the size of the read-only area.

The Write Status Register (WRSR) instruction also allows the user to set or reset the Status Register Protect (SRP) bit in accordance with the Write Protect (WP#) signal, by setting which the device can enter into Hardware Protected Mode. The Write Status Register (WRSR) instruction is not executed once enter into the Hardware Protected Mode.

Figure 4. Write Status Register Sequence Diagram



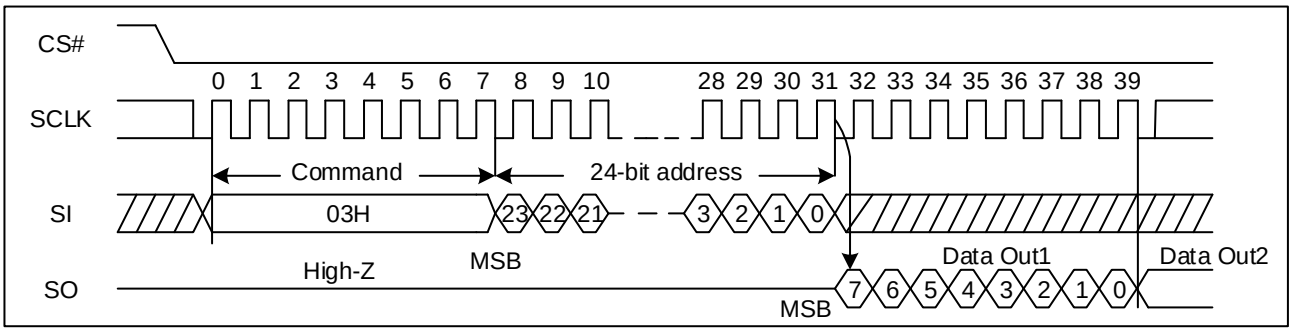
7.5 Read Data Bytes (READ) (03H)

The Read Data Bytes (READ) command is followed by a 3-byte address (A23-A0), and each bit is latched-in on the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, and each bit is shifted out, at a Max frequency f_R, on the falling edge of SCLK. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes (READ) command. Any Read Data Bytes (READ) command, while an Erase, Program or

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Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

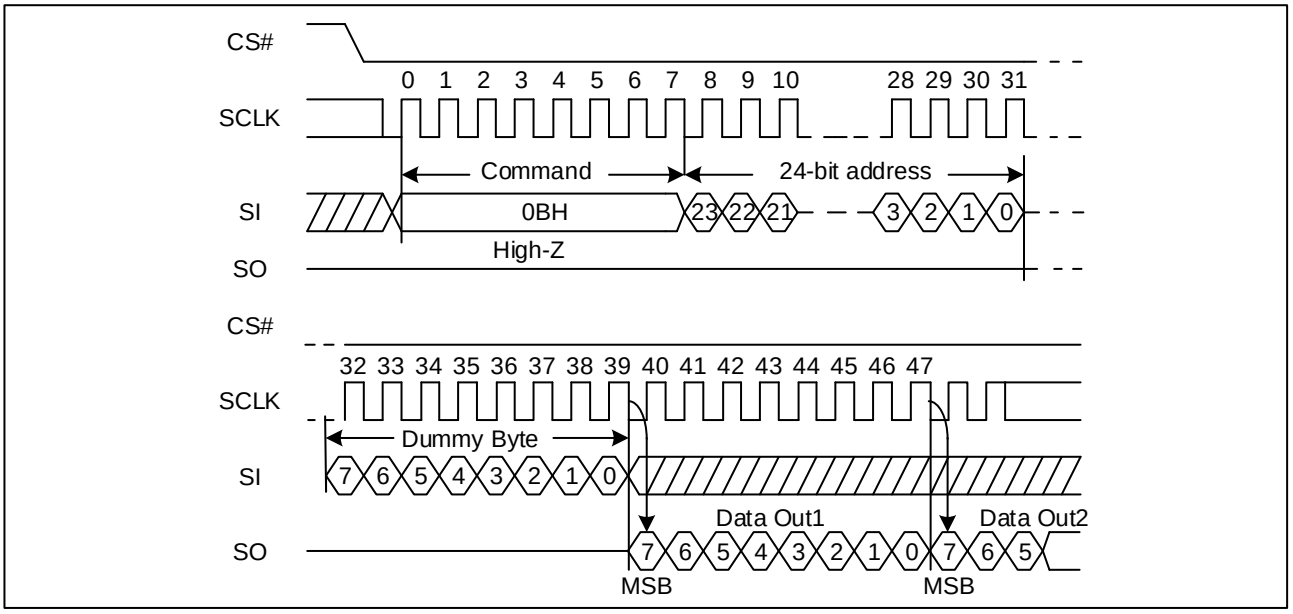
Figure 5. Read Data Bytes Sequence Diagram



7.6 Read Data Bytes at Higher Speed (Fast Read) (0BH)

The Read Data Bytes at Higher Speed (Fast Read) command is for quickly reading data out. It is followed by a 3-byte address (A23-A0) and a dummy byte, and each bit is latched-in on the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, and each bit is shifted out, at a Max frequency f_C, on the falling edge of SCLK. The first byte address can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out.

Figure 6. Read Data Bytes at Higher Speed Sequence Diagram



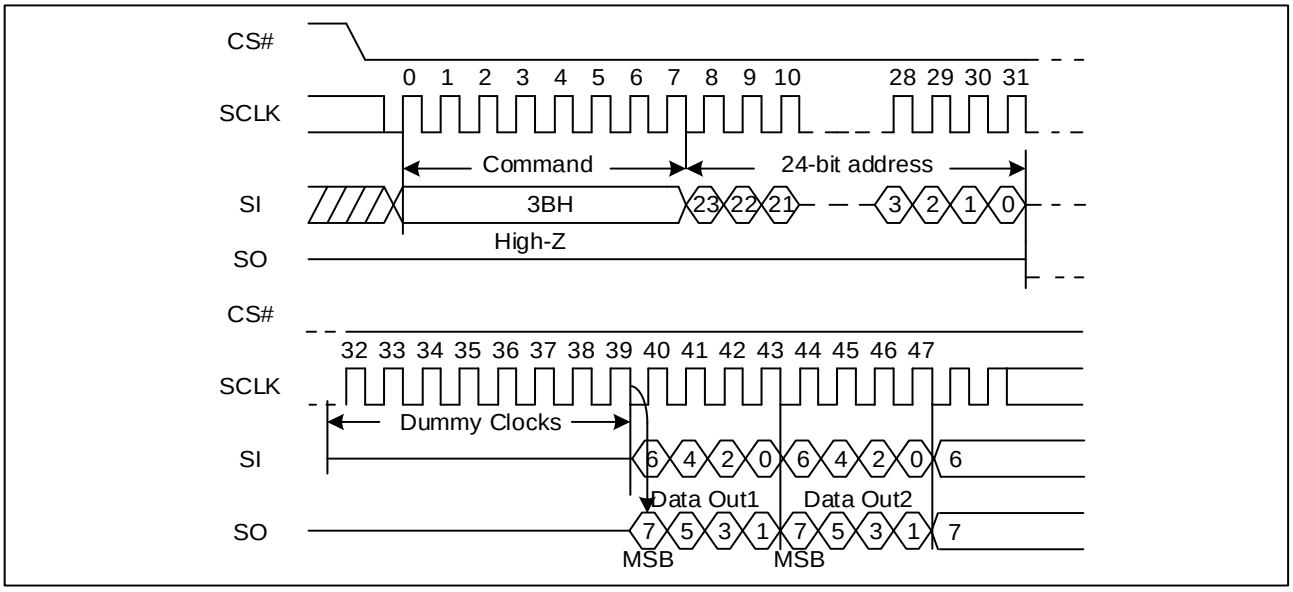
7.7 Dual Output Fast Read (3BH)

The Dual Output Fast Read command is followed by 3-byte address (A23-A0) and a dummy byte, and each bit is latched in on the rising edge of SCLK, then the memory contents are shifted out 2-bit per clock cycle from SI and SO.

The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out.

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Figure 7. Dual Output Fast Read Sequence Diagram



7.8 Page Program (PP) (02H)

The Page Program (PP) command is for programming the memory. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Page Program command.

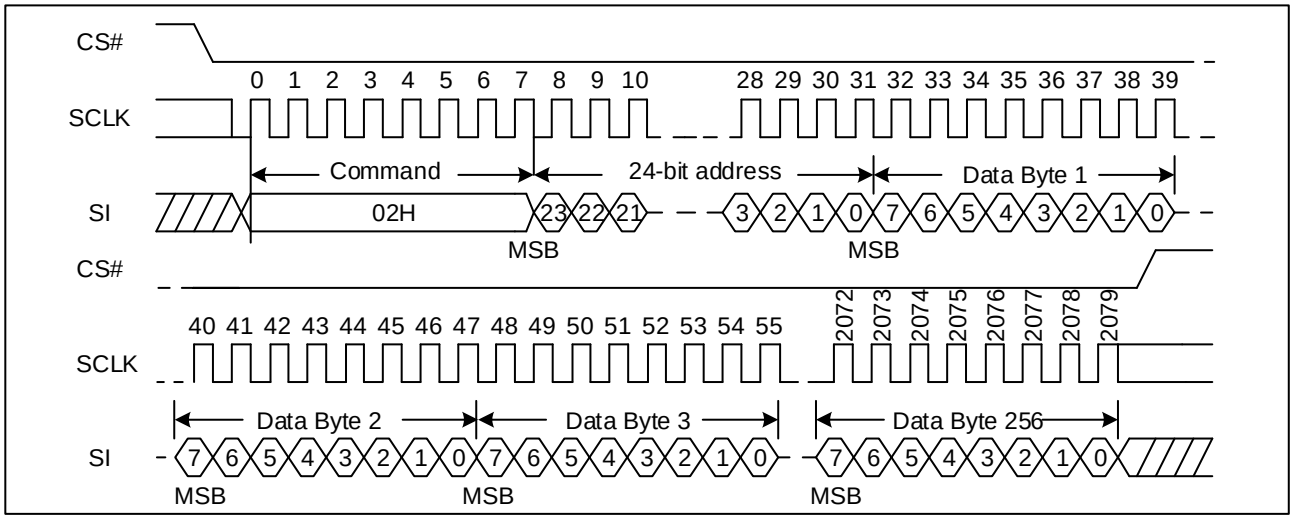
The Page Program (PP) command is entered by driving CS# Low, followed by the command code, three address bytes and at least one data byte on SI. If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 8 least significant bits (A7-A0) are all zero). CS# must be driven low for the entire duration of the sequence. The Page Program command sequence: CS# goes low → sending Page Program command → 3-byte address on SI → at least 1 byte data on SI → CS# goes high. If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page. CS# must be driven high after the eighth bit of the last data byte has been latched in; otherwise the Page Program (PP) command is not executed.

As soon as CS# is driven high, the self-timed Page Program cycle (whose duration is t_{PP}) is initiated. While the Page Program cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Page Program (PP) command applied to a page which is protected by the Block Protect (BP2, BP1, and BP0) is not executed.

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Figure 8. Page Program Sequence Diagram

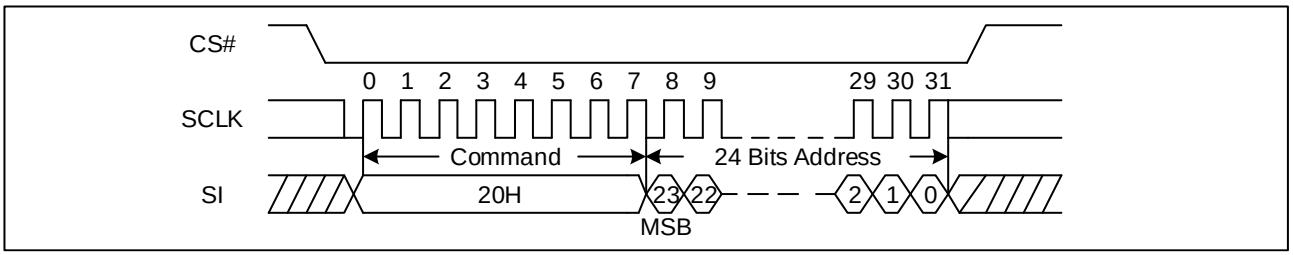


7.9 Sector Erase (SE) (20H)

The Sector Erase (SE) command is for erasing the all data of the chosen sector. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The Sector Erase (SE) command is entered by driving CS# low, followed by the command code, and 3-address byte on SI. Any address inside the sector is a valid address for the Sector Erase (SE) command. CS# must be driven low for the entire duration of the sequence.

The Sector Erase command sequence: CS# goes low → sending Sector Erase command → 3-byte address on SI → CS# goes high. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the Sector Erase (SE) command is not executed. As soon as CS# is driven high, the self-timed Sector Erase cycle (whose duration is t_{SE}) is initiated. While the Sector Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Sector Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A Sector Erase (SE) command applied to a sector which is protected by the Block Protect (BP2, BP1, and BP0) bit is not executed.

Figure 9. Sector Erase Sequence Diagram



7.10 32KB Block Erase (BE32) (52H)

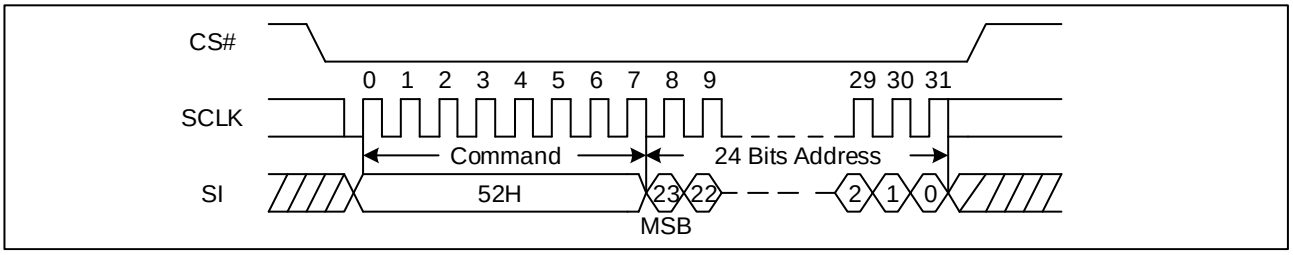
The 32KB Block Erase command is for erasing the all data of the chosen block. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The 32KB Block Erase command is entered by driving CS# low, followed by the command code, and three address bytes on SI. Any address inside the block is a valid address for the 32KB Block Erase command. CS# must be driven low for the entire duration of the sequence.

The 32KB Block Erase command sequence: CS# goes low → sending 32KB Block Erase command → 3-byte address on SI → CS# goes high. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the 32KB Block Erase command is not executed. As soon as CS# is driven high, the self-timed Block Erase cycle (whose

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duration is t_{BE1}) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A 32KB Block Erase command applied to a block which is protected by the Block Protect (BP2, BP1, and BP0) bits is not executed.

Figure 10. 32KB Block Erase Sequence Diagram

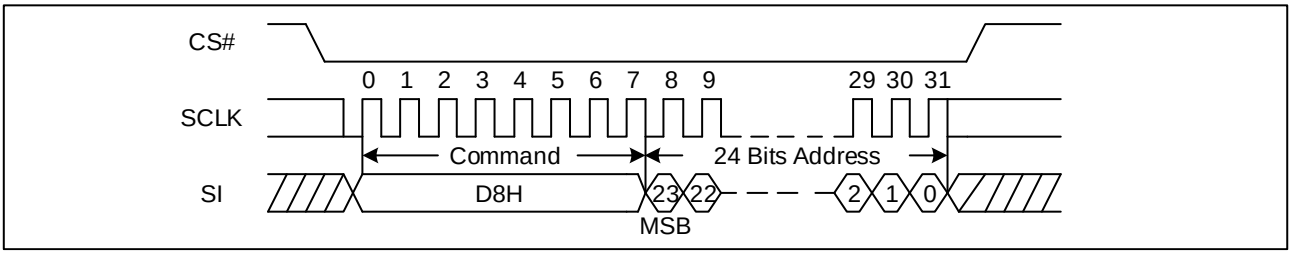


7.11 64KB Block Erase (BE64) (D8H)

The 64KB Block Erase command is for erasing the all data of the chosen block. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The 64KB Block Erase command is entered by driving CS# low, followed by the command code, and three address bytes on SI. Any address inside the block is a valid address for the 64KB Block Erase command. CS# must be driven low for the entire duration of the sequence.

The 64KB Block Erase command sequence: CS# goes low → sending 64KB Block Erase command → 3-byte address on SI → CS# goes high. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the 64KB Block Erase command is not executed. As soon as CS# is driven high, the self-timed Block Erase cycle (whose duration is t_{BE2}) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A 64KB Block Erase command applied to a block which is protected by the Block Protect (BP2, BP1, and BP0) bits is not executed.

Figure 11. 64KB Block Erase Sequence Diagram



7.12 Chip Erase (CE) (60H/C7H)

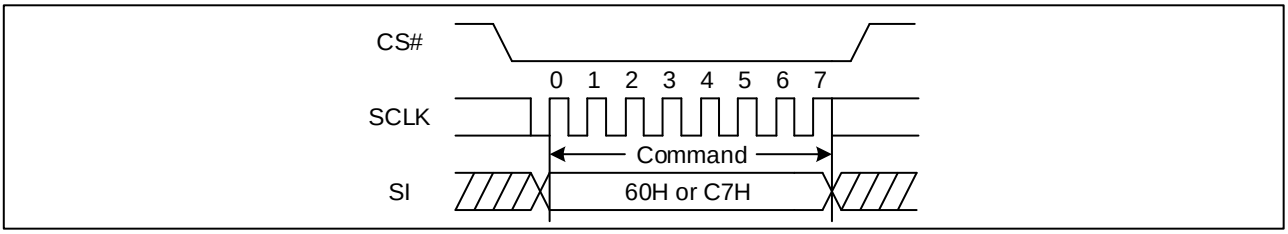
The Chip Erase (CE) command is for erasing the all data of the chip. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit .The Chip Erase (CE) command is entered by driving CS# Low, followed by the command code on Serial Data Input (SI). CS# must be driven Low for the entire duration of the sequence.

The Chip Erase command sequence: CS# goes low → sending Chip Erase command → CS# goes high. CS# must be driven high after the eighth bit of the command code has been latched in; otherwise the Chip Erase command is not executed. As soon as CS# is driven high, the self-timed Chip Erase cycle (whose duration is t_{CE}) is initiated. While the Chip Erase

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cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Chip Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. The Chip Erase (CE) command is executed, if the Block Protect (BP2, BP1, and BP0) bits are 0 and CMP=0 or the Block Protect (BP2, BP1, and BP0) bits are 1 and CMP=1. The Chip Erase (CE) command is ignored if one or more sectors are protected.

Figure 12. Chip Erase Sequence Diagram

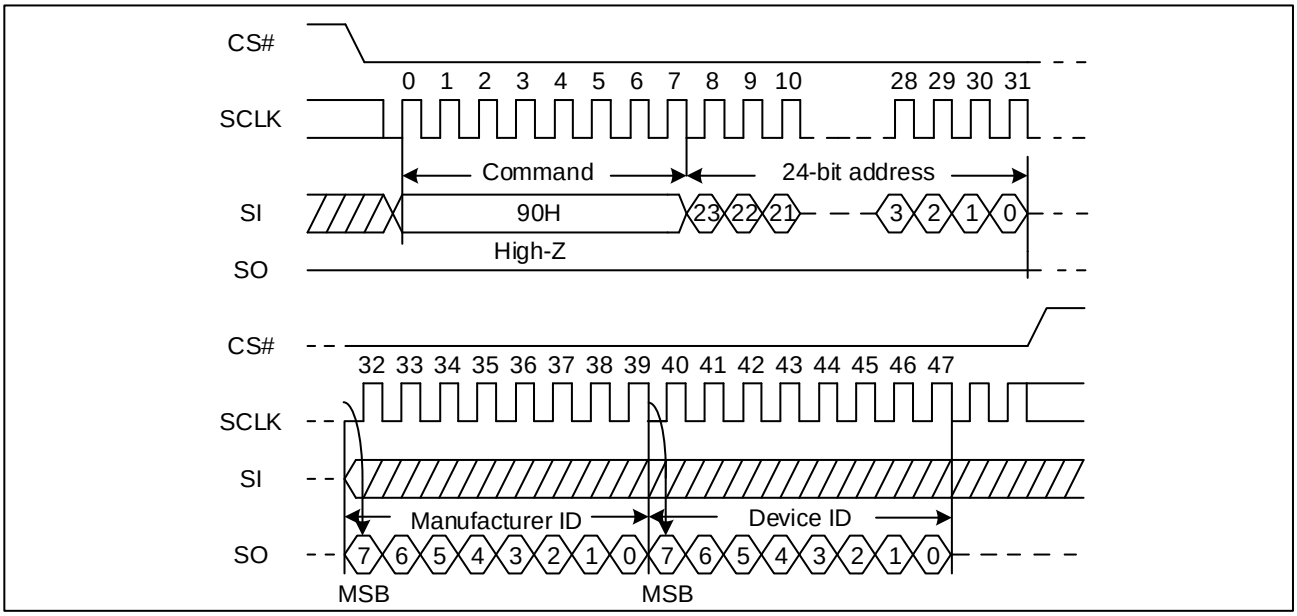


7.13 Read Manufacture ID/ Device ID (REMS) (90H)

The Read Manufacturer/Device ID command is an alternative to the Release from Power-Down / Device ID command that provides both the JEDEC assigned Manufacturer ID and the specific Device ID.

The command is initiated by driving the CS# pin low and shifting the command code “90H” followed by a 24-bit address (A23-A0) of 000000H. After which, the Manufacturer ID and the Device ID are shifted out on the falling edge of SCLK with most significant bit (MSB) first.

Figure 13. Read Manufacture ID/ Device ID Sequence Diagram



7.14 Read Identification (RDID) (9FH)

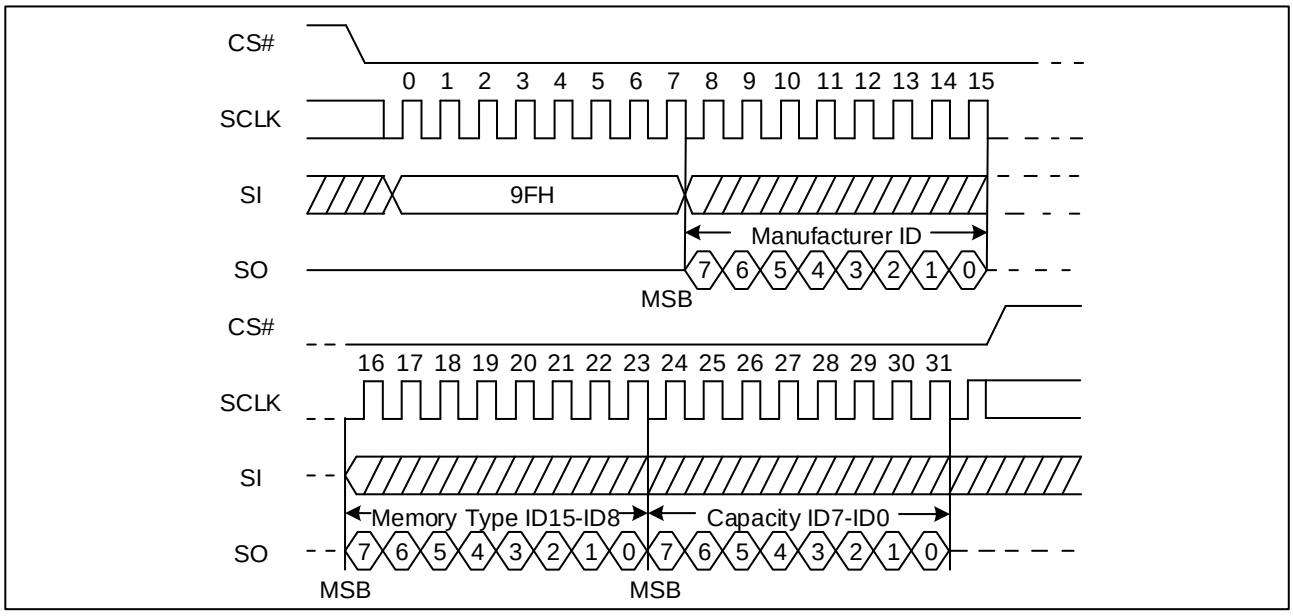
The Read Identification (RDID) command allows the 8-bit manufacturer identification to be read, followed by two bytes of device identification. The device identification indicates the memory type in the first byte, and the memory capacity of the device in the second byte. The Read Identification (RDID) command while an Erase or Program cycle is in progress, is not decoded, and has no effect on the cycle that is in progress. The Read Identification (RDID) command should not be issued while the device is in Deep Power-Down Mode.

The device is first selected by driving CS# low. Then, the 8-bit command code for the command is shifted in. This is followed

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by the 24-bit device identification, stored in the memory. Each bit is shifted out on the falling edge of Serial Clock. The Read Identification (RDID) command is terminated by driving CS# high at any time during data output. When CS# is driven high, the device is in the Standby Mode. Once in the Standby Mode, the device waits to be selected, so that it can receive, decode and execute commands.

Figure 14. Read Identification ID Sequence Diagram

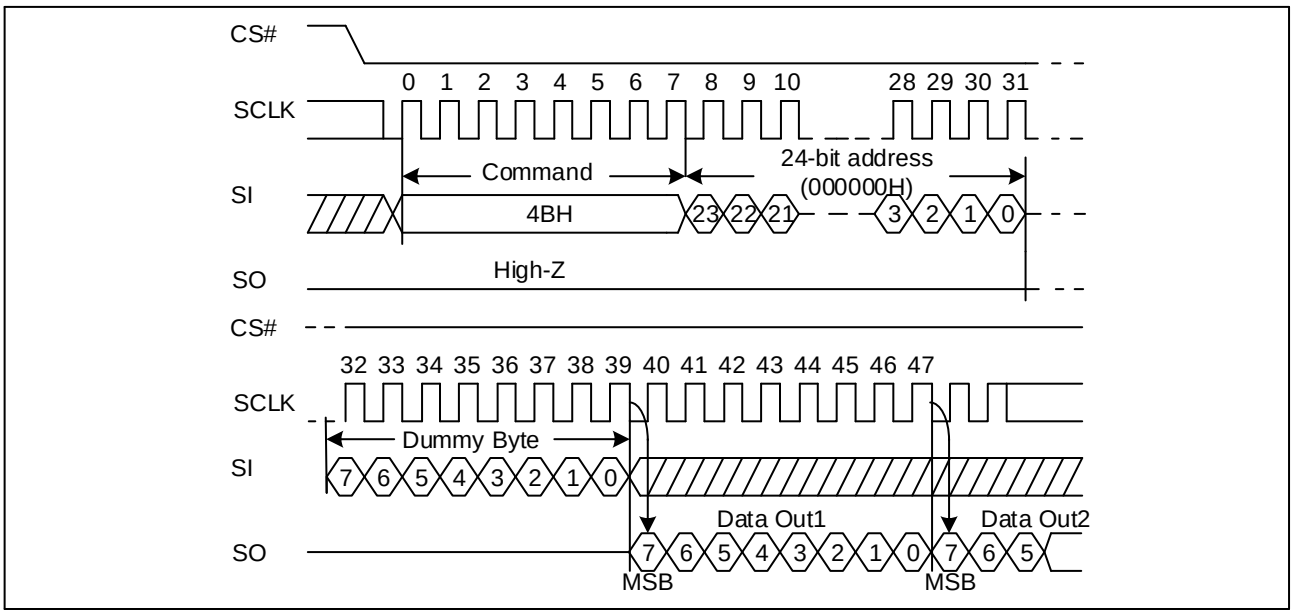


7.15 Read Unique ID (4BH)

The Read Unique ID command accesses a factory-set read-only 128bit number that is unique to each device. The Unique ID can be used in conjunction with user software methods to help prevent copying or cloning of a system.

The Read Unique ID command sequence: CS# goes low → sending Read Unique ID command → 3-Byte Address (000000H) →Dummy Byte→128bit Unique ID Out →CS# goes high.

Figure 15. Read Unique ID Sequence Diagram



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7.16 Erase Security Registers (44H)

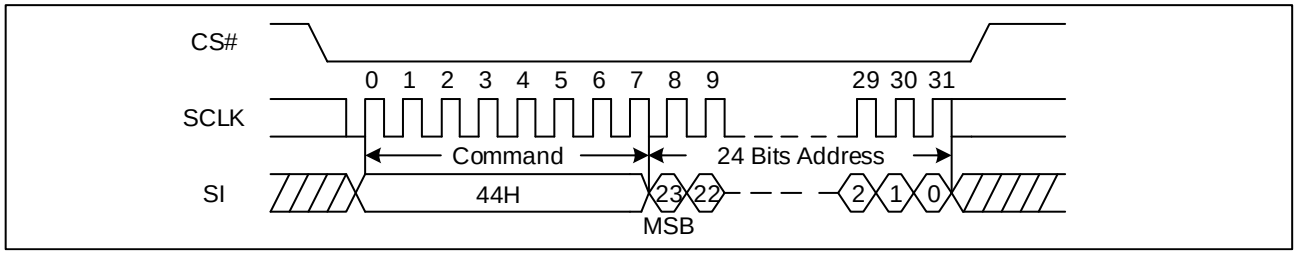
The GD25D80E provides 512-Byte Security Registers which can be erased and programmed individually. These registers may be used by the system manufacturers to store security and other important information separately from the main memory array.

The Erase Security Registers command is similar to Sector/Block Erase command. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit.

The Erase Security Registers command sequence: CS# goes low → sending Erase Security Registers command → 3-byte address on SI → CS# goes high. The command sequence is shown below. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the Erase Security Registers command is not executed. As soon as CS# is driven high, the self-timed Erase Security Registers cycle (whose duration is t_{SE}) is initiated. While the Erase Security Registers cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Erase Security Registers cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. The Security Registers Lock Bit (LB) in the Status Register can be used to OTP protect the security registers. Once the LB bit is set to 1, the Security Registers will be permanently locked; the Erase Security Registers command will be ignored.

Address	A23-16	A15-12	A11-9	A8-0
Security Register	00H	0000b	000b	Don't care

Figure 16. Erase Security Registers command Sequence Diagram



7.17 Program Security Registers (42H)

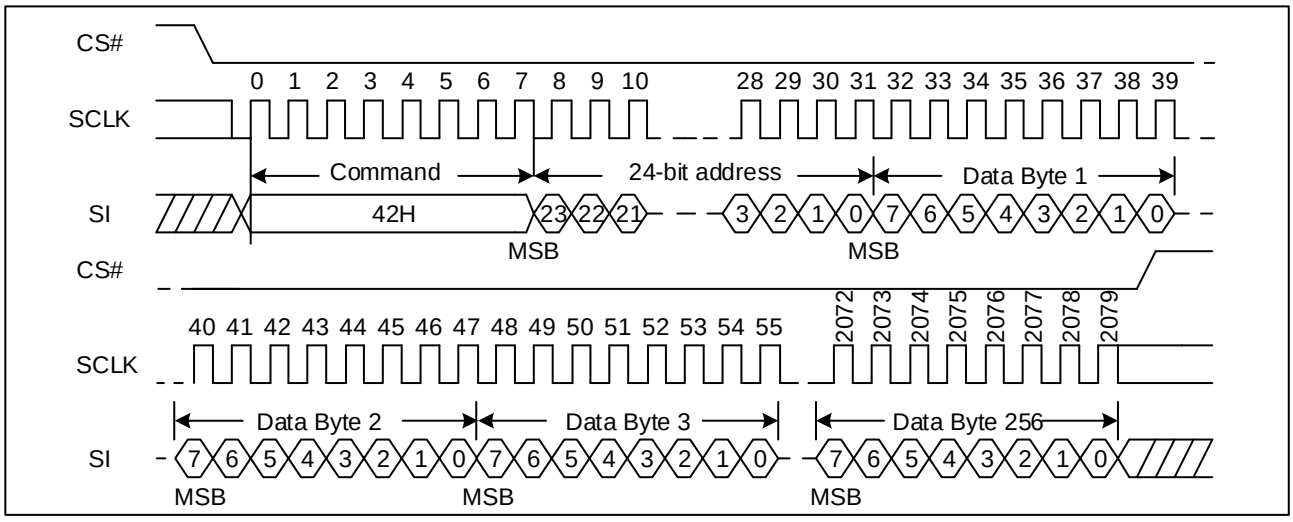
The Program Security Registers command is similar to the Page Program command. Each security register contains two pages content. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Program Security Registers command. The Program Security Registers command is entered by driving CS# Low, followed by the command code (42H), three address bytes and at least one data byte on SI. As soon as CS# is driven high, the self-timed Program Security Registers cycle (whose duration is t_{PP}) is initiated. While the Program Security Registers cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Program Security Registers cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

If the Security Registers Lock Bit (LB) is set to 1, the Security Registers will be permanently locked. Program Security Registers command will be ignored.

Address	A23-16	A15-12	A11-9	A8-0
Security Register	00H	0000b	000b	Byte Address

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Figure 17. Program Security Registers command Sequence Diagram

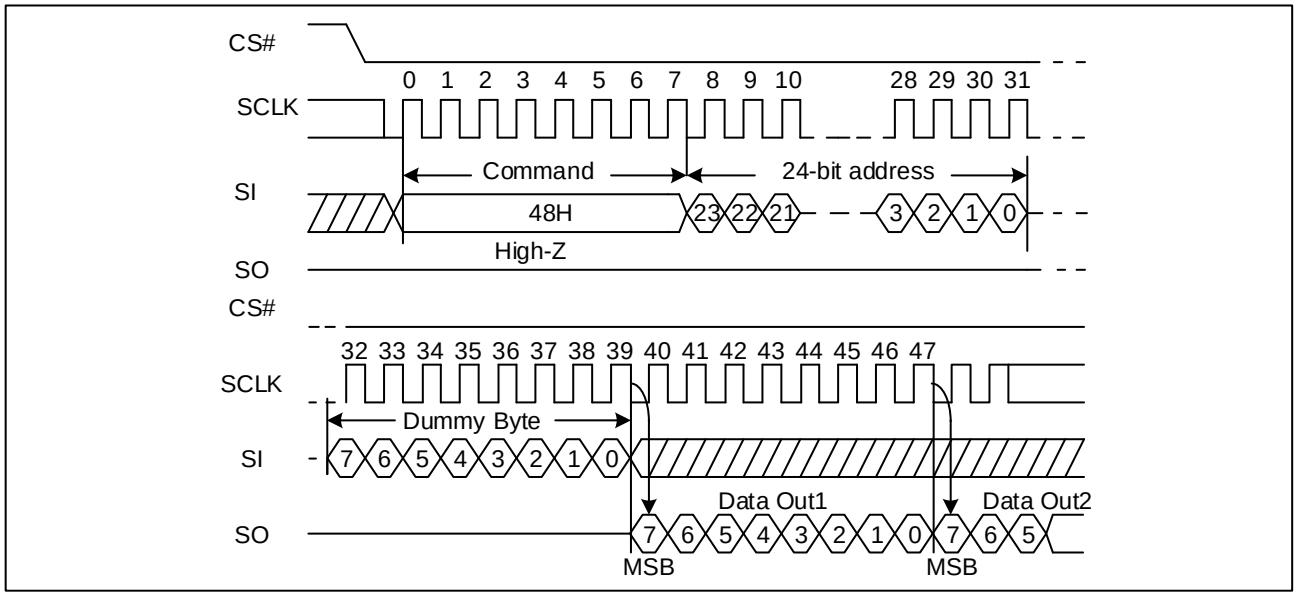


7.18 Read Security Registers (48H)

The Read Security Registers command is similar to Fast Read command. The command is followed by a 3-byte address (A23-A0) and a dummy byte, and each bit is latched-in on the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, and each bit is shifted out, at a Max frequency f_C, on the falling edge of SCLK. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. Once the A8-0 address reaches the last byte of the register (Byte 1FFH), it will reset to 000H, the command is completed by driving CS# high.

Address	A23-16	A15-12	A11-9	A8-0
Security Register	00H	0000b	000b	Byte Address

Figure 18. Read Security Registers command Sequence Diagram



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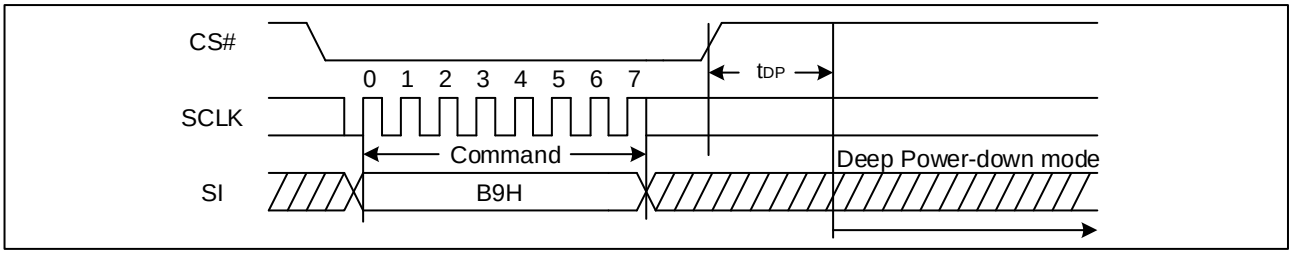
7.19 Deep Power-Down (DP) (B9H)

Executing the Deep Power-Down (DP) command is the only way to put the device in the lowest consumption mode (the Deep Power-Down Mode). It can also be used as an extra software protection mechanism, while the device is not in active use, since in this mode, the device ignores all Write, Program and Erase commands. Driving CS# high deselects the device, and puts the device in the Standby Mode (if there is no internal cycle currently in progress). But this mode is not the Deep Power-Down Mode. The Deep Power-Down Mode can only be entered by executing the Deep Power-Down (DP) command. Once the device has entered the Deep Power-Down Mode, all commands are ignored except the Release from Deep Power-Down and Read Device ID (RDI) command or software reset command. The Release from Deep Power-Down and Read Device ID (RDI) command releases the device from Deep Power-Down mode, also allows the Device ID of the device to be output on SO.

The Deep Power-Down Mode automatically stops at Power-Down, and the device always in the Standby Mode after Power-Up.

The Deep Power-Down command sequence: CS# goes low → sending Deep Power-Down command → CS# goes high. CS# must be driven high after the eighth bit of the command code has been latched in; otherwise the Deep Power-Down (DP) command is not executed. As soon as CS# is driven high, it requires a delay of t_{DP} before the supply current is reduced to I_{CC2} and the Deep Power-Down Mode is entered. Any Deep Power-Down (DP) command, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 19. Deep Power-Down Sequence Diagram



7.20 Release from Deep Power-Down and Read Device ID (RDI) (ABH)

The Release from Power-Down and Read Device ID command is a multi-purpose command. It can be used to release the device from the Power-Down state or obtain the devices electronic identification (ID) number.

To release the device from the Power-Down state, the command is issued by driving the CS# pin low, shifting the instruction code “ABH” and driving CS# high. Release from Power-Down will take the time duration of t_{RES1} (See AC Characteristics) before the device will resume normal operation and other command are accepted. The CS# pin must remain high during the t_{RES1} time duration.

When used only to obtain the Device ID while not in the Power-Down state, the command is initiated by driving the CS# pin low and shifting the instruction code “ABH” followed by 3-dummy byte. The ID7~ID0 are then shifted out on the falling edge of SCLK with most significant bit (MSB) first. The Device ID value is listed in Manufacturer and Device Identification table. The Device ID can be read continuously. The command is completed by driving CS# high.

When used to release the device from the Power-Down state and obtain the ID7~ID0, the command is the same as previously described, except that after CS# is driven high it must remain high for a time duration of t_{RES2} (See AC Characteristics). After this time duration the device will resume normal operation and other command will be accepted. If the Release from Power-Down / Device ID command is issued while an Erase, Program or Write cycle is in process (when WIP equals 1) the command is ignored and will not have any effects on the current cycle.

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Figure 20. Release Power-Down Sequence Diagram

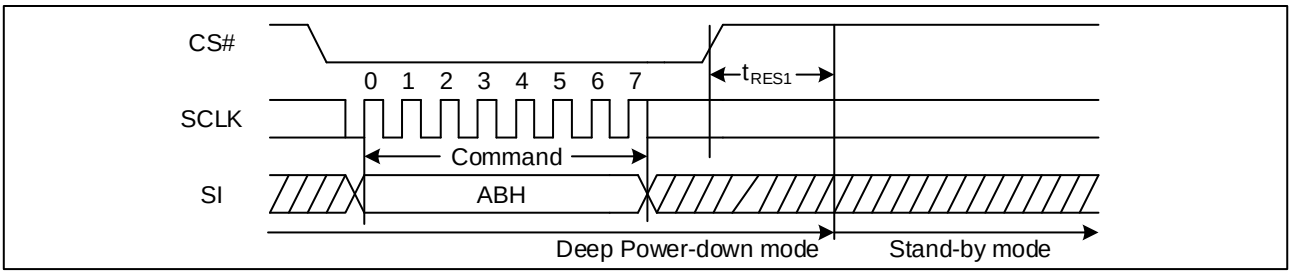
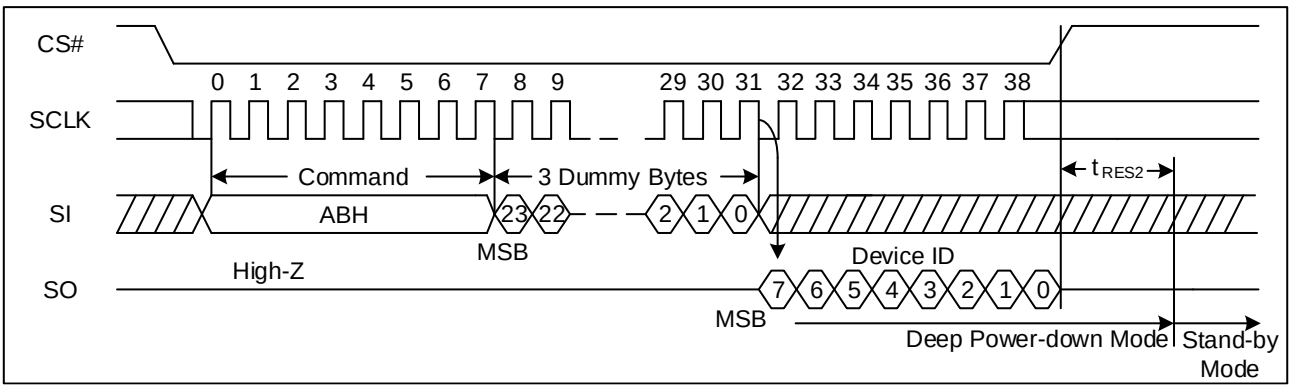


Figure 21. Release Power-Down/Read Device ID Sequence Diagram



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8 ELECTRICAL CHARACTERISTICS

8.1 Power-On Timing

Figure 22. Power-On Timing Sequence Diagram

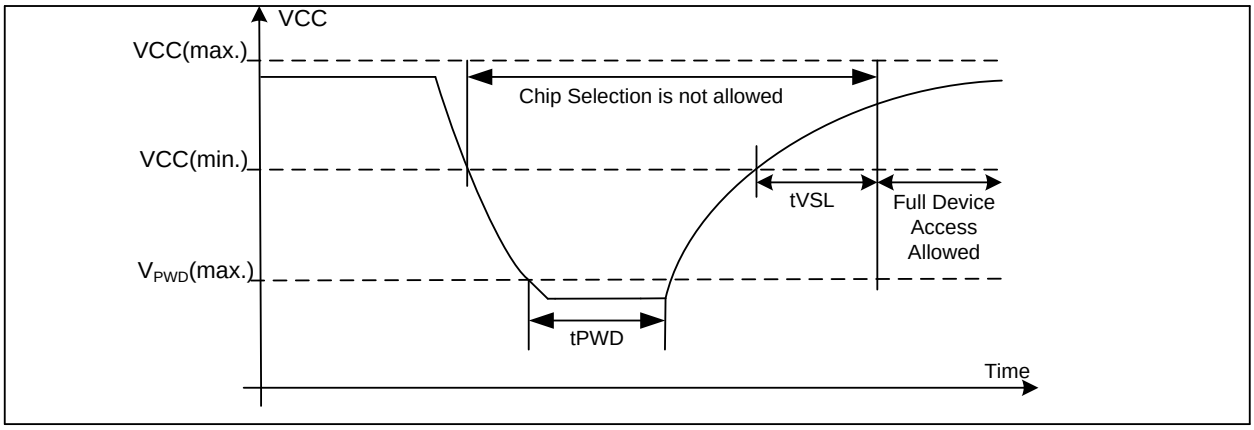


Table 7. Power-Up Timing and Write Inhibit Threshold

Symbol	Parameter	Min.	Max.	Unit
tVSL	VCC (min.) to device operation	0.9		ms
VWI	Write Inhibit Voltage	1.5	2.5	V
VPWD	VCC voltage needed to below VPWD for ensuring initialization will occur		0.5	V
tPWD	The minimum duration for ensuring initialization will occur	300		μs

8.2 Initial Delivery State

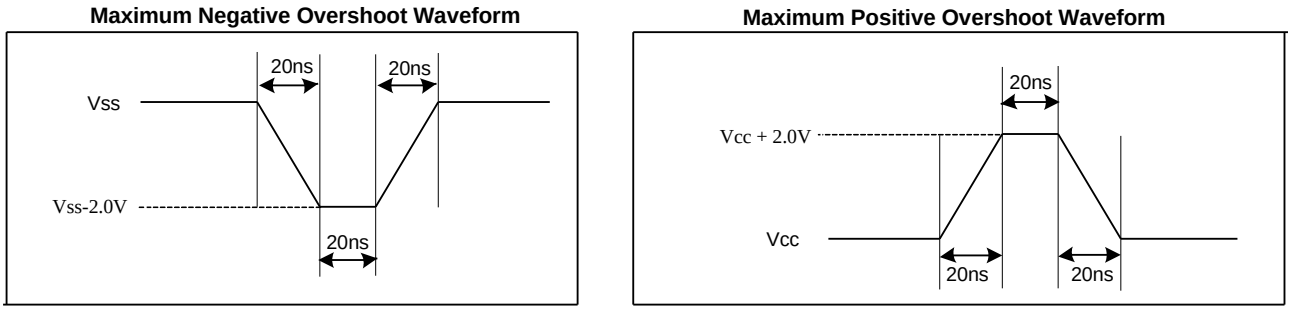
The device is delivered with the memory array erased: all bits are set to 1 (each Byte contains FFH). The Status Register contains 00H (all Status Register bits are 0).

8.3 Absolute Maximum Ratings

Parameter	Value	Unit
Ambient Operating Temperature (T_A)	-40 to 85 -40 to 105 -40 to 125	℃
Storage Temperature	-65 to 150	℃
Transient Input/Output Voltage (note: overshoot)	-2.0 to VCC+2.0	V
Applied Input/Output Voltage	-0.6 to VCC+0.4	V
VCC	-0.6 to 4.2	V

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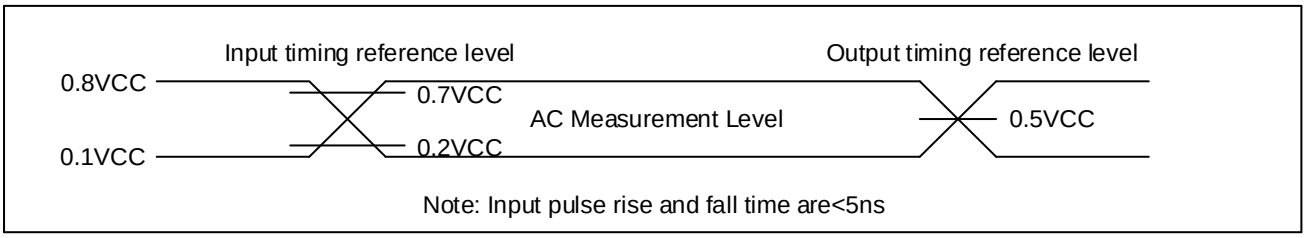
Figure 23. Input Test Waveform and Measurement Level



8.4 Capacitance Measurement Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
CIN	Input Capacitance			6	pF	VIN=0V
COUT	Output Capacitance			8	pF	VOUT=0V
C_L	Load Capacitance		30		pF	
	Input Rise And Fall time			5	ns	
	Input Pulse Voltage		0.1VCC to 0.8VCC		V	
	Input Timing Reference Voltage		0.2VCC to 0.7VCC		V	
	Output Timing Reference Voltage		0.5VCC		V	

Figure 24. Absolute Maximum Ratings Diagram



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8.5 DC Characteristics

(T_A = -40℃~85℃, VCC=2.7~3.6V)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit.
I_{LI}	Input Leakage Current				±2	μA
I_{LO}	Output Leakage Current				±2	μA
I_{CC1}	Standby Current	CS#=VCC, VIN=VCC or VSS		0.1	2	μA
I_{CC2}	Deep Power-Down Current	CS#=VCC, VIN=VCC or VSS		0.1	2	μA
I_{CC3}	Operating Current (Read)	CLK=0.1VCC/ 0.9VCC at 104MHz, Q=Open(x1 I/O)		3	6	mA
		CLK=0.1VCC/ 0.9VCC at 80MHz, Q=Open(x2 Output)		2.5	4.5	mA
		CLK=0.1VCC/ 0.9VCC at 50MHz, Q=Open(x1 I/O)		2	3.5	mA
I_{CC4}	Operating Current (PP)	CS#=VCC		10	20	mA
I_{CC5}	Operating Current (WRSR)	CS#=VCC		10	20	mA
I_{CC6}	Operating Current (SE)	CS#=VCC		10	20	mA
I_{CC7}	Operating Current (BE)	CS#=VCC		10	20	mA
I_{CC8}	Operating Current (CE)	CS#=VCC		10	20	mA
V_{IL}	Input Low Voltage		-0.5		0.2VCC	V
V_{IH}	Input High Voltage		0.7VCC		VCC+0.4	V
V_{OL}	Output Low Voltage	I_{OL} = 100μA			0.2	V
V_{OH}	Output High Voltage	I_{OH} = -100μA	VCC-0.2			V

Note:

1. Typical value at T_A = 25℃, VCC = 3.3V.
2. Value guaranteed by design and/or characterization, not 100% tested in production.

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(T_A = -40℃~105℃, VCC=2.7~3.6V)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit.
I_{LI}	Input Leakage Current				±2	μA
I_{LO}	Output Leakage Current				±2	μA
I_{CC1}	Standby Current	CS#=VCC, VIN=VCC or VSS		0.1	10	μA
I_{CC2}	Deep Power-Down Current	CS#=VCC, VIN=VCC or VSS		0.1	10	μA
I_{CC3}	Operating Current (Read)	CLK=0.1VCC/ 0.9VCC at 104MHz, Q=Open(x1 I/O)		3	22	mA
		CLK=0.1VCC/ 0.9VCC at 80MHz, Q=Open(x2 Output)		2.5	20	mA
		CLK=0.1VCC/ 0.9VCC at 50MHz, Q=Open(x1 I/O)		2	18	mA
I_{CC4}	Operating Current (PP)	CS#=VCC		10	30	mA
I_{CC5}	Operating Current (WRSR)	CS#=VCC		10	30	mA
I_{CC6}	Operating Current (SE)	CS#=VCC		10	30	mA
I_{CC7}	Operating Current (BE)	CS#=VCC		10	30	mA
I_{CC8}	Operating Current (CE)	CS#=VCC		10	30	mA
V_{IL}	Input Low Voltage		-0.5		0.2VCC	V
V_{IH}	Input High Voltage		0.7VCC		VCC+0.4	V
V_{OL}	Output Low Voltage	I_{OL} = 100μA			0.2	V
V_{OH}	Output High Voltage	I_{OH} = -100μA	VCC-0.2			V

Note:

1. Typical value at T_A = 25℃, VCC = 3.3V.
2. Value guaranteed by design and/or characterization, not 100% tested in production.

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(T_A = -40℃~125℃, VCC=2.7~3.6V)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit.
I_{LI}	Input Leakage Current				±2	μA
I_{LO}	Output Leakage Current				±2	μA
I_{CC1}	Standby Current	CS#=VCC, VIN=VCC or VSS		0.1	15	μA
I_{CC2}	Deep Power-Down Current	CS#=VCC, VIN=VCC or VSS		0.1	15	μA
I_{CC3}	Operating Current (Read)	CLK=0.1VCC/ 0.9VCC at 104MHz, Q=Open(x1 I/O)		3	25	mA
		CLK=0.1VCC/ 0.9VCC at 80MHz, Q=Open(x2 Output)		2.5	22	mA
		CLK=0.1VCC/ 0.9VCC at 50MHz, Q=Open(x1 I/O)		2	20	mA
I_{CC4}	Operating Current (PP)	CS#=VCC		10	30	mA
I_{CC5}	Operating Current (WRSR)	CS#=VCC		10	30	mA
I_{CC6}	Operating Current (SE)	CS#=VCC		10	30	mA
I_{CC7}	Operating Current (BE)	CS#=VCC		10	30	mA
I_{CC8}	Operating Current (CE)	CS#=VCC		10	30	mA
V_{IL}	Input Low Voltage		-0.5		0.2VCC	V
V_{IH}	Input High Voltage		0.7VCC		VCC+0.4	V
V_{OL}	Output Low Voltage	I_{OL} = 100μA			0.2	V
V_{OH}	Output High Voltage	I_{OH} = -100μA	VCC-0.2			V

Note:

1. Typical value at T_A = 25℃, VCC = 3.3V.
2. Value guaranteed by design and/or characterization, not 100% tested in production.

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8.6 AC Characteristics

(T_A = -40℃~85℃, VCC=2.7~3.6V)

Symbol	Parameter	Min.	Typ.	Max.	Unit.
f_{C1}	Serial Clock Frequency For: all commands except 03H and 3BH			104	MHz
f_{R1}	Serial Clock Frequency For: Read (03H) ,Dual Output (3BH)			80	MHz
t_{CLH}	Serial Clock High Time	45% (1/fc_{max})			ns
t_{CLL}	Serial Clock Low Time	45% (1/fc_{max})			ns
t_{CLCH}	Serial Clock Rise Time (Slew Rate)	0.2			V/ns
t_{CHCL}	Serial Clock Fall Time (Slew Rate)	0.2			V/ns
t_{SLCH}	CS# Active Setup Time	5			ns
t_{CHSH}	CS# Active Hold Time	5			ns
t_{SHCH}	CS# Not Active Setup Time	5			ns
t_{CHSL}	CS# Not Active Hold Time	5			ns
t_{SHSL}	CS# High Time (Read/Write)	40			ns
t_{SHQZ}	Output Disable Time			6	ns
t_{CLQX}	Output Hold Time	0			ns
t_{DVCH}	Data In Setup Time	2			ns
t_{CHDX}	Data In Hold Time	2			ns
t_{CLQV}	Clock Low To Output Valid			6	ns
t_{WHSL}	Write Protect Setup Time Before CS# Low	20			ns
t_{SHWL}	Write Protect Hold Time After CS# High	100			ns
t_{DP}	CS# High To Deep Power-Down Mode			0.1	μs
t_{RES1}	CS# High To Standby Mode Without Electronic Signature Read			0.1	μs
t_{RES2}	CS# High To Standby Mode With Electronic Signature Read			0.1	μs
t_W	Write Status Register Cycle Time		4	30	ms
t_{BP1}	Byte Program Time (First Byte)		30	50	μs
t_{BP2}	Additional Byte Program Time (After First Byte)		2.5	12	μs
t_{PP}	Page Programming Time		0.6	4.0	ms
t_{SE}	Sector Erase Time		60	400	ms
t_{BE1}	Block Erase Time (32K Bytes)		0.2	1.2	s
t_{BE2}	Block Erase Time (64K Bytes)		0.35	2.0	s
t_{CE}	Chip Erase Time		6	20	s

Note:

1. Typical value at T_A = 25℃, VCC = 3.3V.
2. Value guaranteed by design and/or characterization, not 100% tested in production.

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(T_A = -40℃~105℃, VCC=2.7~3.6V)

Symbol	Parameter	Min.	Typ.	Max.	Unit.
f_{C1}	Serial Clock Frequency For: all commands except 03H and 3BH			104	MHz
f_{R1}	Serial Clock Frequency For: Read (03H) ,Dual Output (3BH)			80	MHz
t_{CLH}	Serial Clock High Time	45% (1/fc_{max})			ns
t_{CLL}	Serial Clock Low Time	45% (1/fc_{max})			ns
t_{CLCH}	Serial Clock Rise Time (Slew Rate)	0.2			V/ns
t_{CHCL}	Serial Clock Fall Time (Slew Rate)	0.2			V/ns
t_{SLCH}	CS# Active Setup Time	5			ns
t_{CHSH}	CS# Active Hold Time	5			ns
t_{SHCH}	CS# Not Active Setup Time	5			ns
t_{CHSL}	CS# Not Active Hold Time	5			ns
t_{SHSL}	CS# High Time (Read/Write)	40			ns
t_{SHQZ}	Output Disable Time			6	ns
t_{CLQX}	Output Hold Time	0			ns
t_{DVCH}	Data In Setup Time	2			ns
t_{CHDX}	Data In Hold Time	2			ns
t_{CLQV}	Clock Low To Output Valid			6	ns
t_{WHSL}	Write Protect Setup Time Before CS# Low	20			ns
t_{SHWL}	Write Protect Hold Time After CS# High	100			ns
t_{DP}	CS# High To Deep Power-Down Mode			0.1	μs
t_{RES1}	CS# High To Standby Mode Without Electronic Signature Read			0.1	μs
t_{RES2}	CS# High To Standby Mode With Electronic Signature Read			0.1	μs
t_W	Write Status Register Cycle Time		4	30	ms
t_{BP1}	Byte Program Time (First Byte)		30	60	μs
t_{BP2}	Additional Byte Program Time (After First Byte)		2.5	15	μs
t_{PP}	Page Programming Time		0.6	4.0	ms
t_{SE}	Sector Erase Time		60	400	ms
t_{BE1}	Block Erase Time (32K Bytes)		0.2	1.2	s
t_{BE2}	Block Erase Time (64K Bytes)		0.35	2.0	s
t_{CE}	Chip Erase Time		6	20	s

Note:

1. Typical value at T_A = 25℃, VCC = 3.3V.
2. Value guaranteed by design and/or characterization, not 100% tested in production.

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(T_A = -40℃~125℃, VCC=2.7~3.6V)

Symbol	Parameter	Min.	Typ.	Max.	Unit.
f_{C1}	Serial Clock Frequency For: all commands except 03H and 3BH			104	MHz
f_{R1}	Serial Clock Frequency For: Read (03H) ,Dual Output (3BH)			80	MHz
t_{CLH}	Serial Clock High Time	45% (1/fc_{max})			ns
t_{CLL}	Serial Clock Low Time	45% (1/fc_{max})			ns
t_{CLCH}	Serial Clock Rise Time (Slew Rate)	0.2			V/ns
t_{CHCL}	Serial Clock Fall Time (Slew Rate)	0.2			V/ns
t_{SLCH}	CS# Active Setup Time	5			ns
t_{CHSH}	CS# Active Hold Time	5			ns
t_{SHCH}	CS# Not Active Setup Time	5			ns
t_{CHSL}	CS# Not Active Hold Time	5			ns
t_{SHSL}	CS# High Time (Read/Write)	40			ns
t_{SHQZ}	Output Disable Time			6	ns
t_{CLQX}	Output Hold Time	0			ns
t_{DVCH}	Data In Setup Time	2			ns
t_{CHDX}	Data In Hold Time	2			ns
t_{CLQV}	Clock Low To Output Valid			6	ns
t_{WHSL}	Write Protect Setup Time Before CS# Low	20			ns
t_{SHWL}	Write Protect Hold Time After CS# High	100			ns
t_{DP}	CS# High To Deep Power-Down Mode			0.1	μs
t_{RES1}	CS# High To Standby Mode Without Electronic Signature Read			0.1	μs
t_{RES2}	CS# High To Standby Mode With Electronic Signature Read			0.1	μs
t_W	Write Status Register Cycle Time		4	30	ms
t_{BP1}	Byte Program Time (First Byte)		30	80	μs
t_{BP2}	Additional Byte Program Time (After First Byte)		2.5	20	μs
t_{PP}	Page Programming Time		0.6	4.0	ms
t_{SE}	Sector Erase Time		60	400	ms
t_{BE1}	Block Erase Time (32K Bytes)		0.2	1.5	s
t_{BE2}	Block Erase Time (64K Bytes)		0.35	3.0	s
t_{CE}	Chip Erase Time		6	32	s

Note:

1. Typical value at T_A = 25℃, VCC = 3.3V.
2. Value guaranteed by design and/or characterization, not 100% tested in production.

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Figure 25. Input Timing

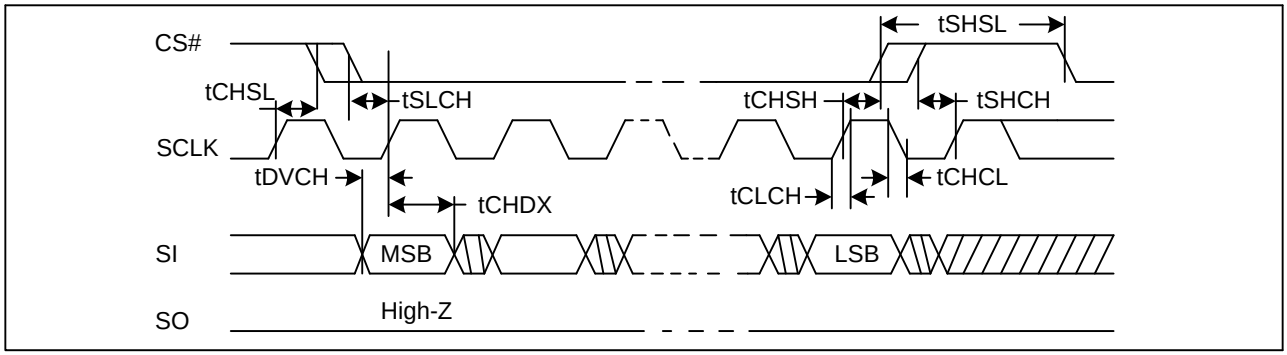


Figure 26. Output Timing

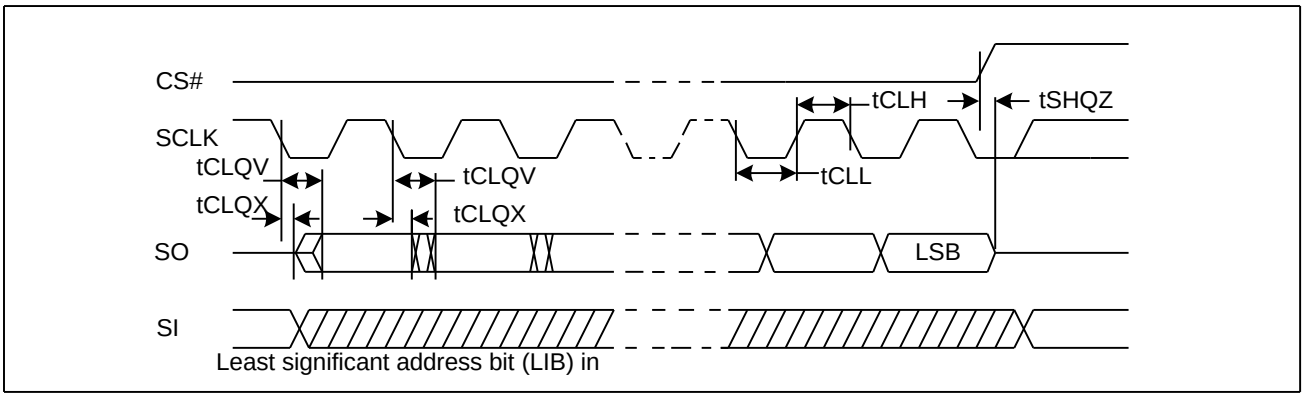
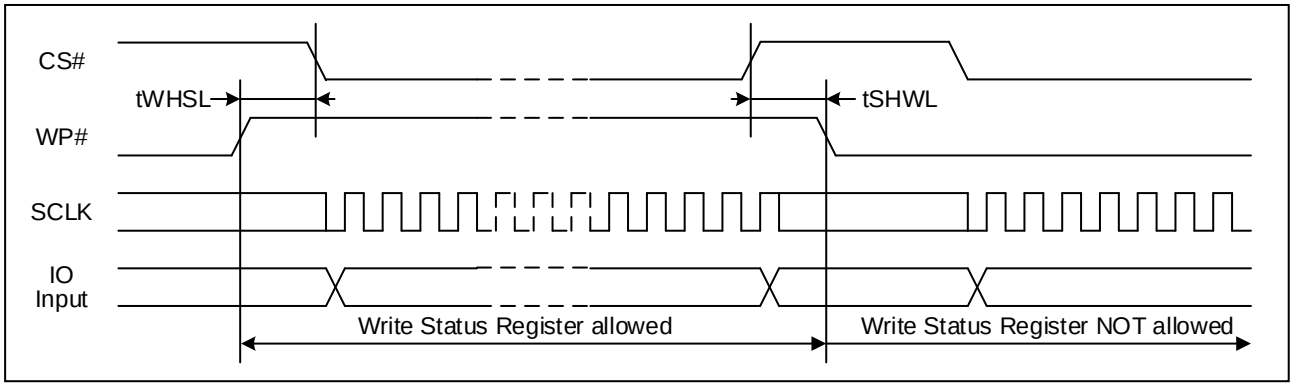
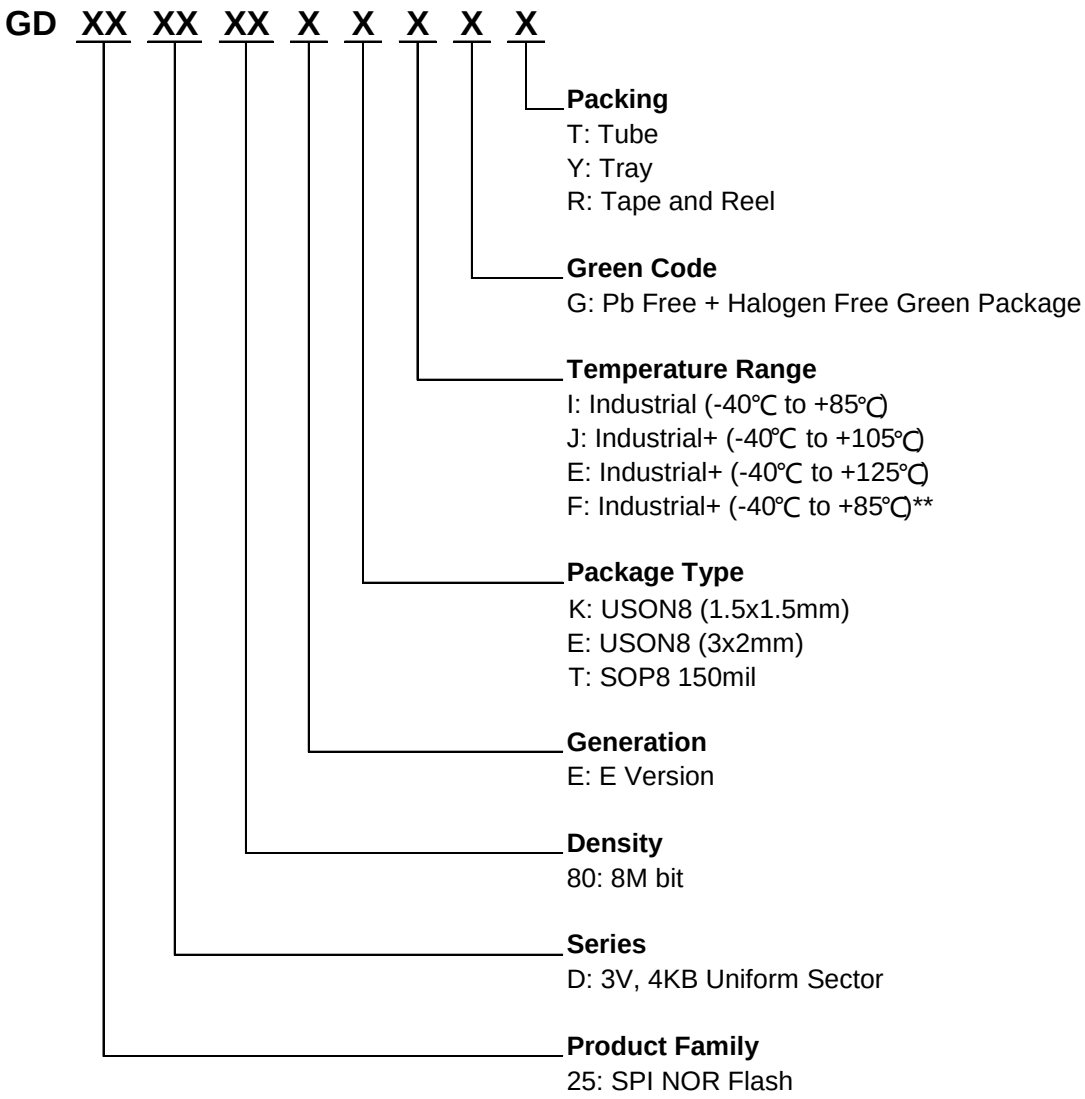


Figure 27. WP# Timing



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9 ORDERING INFORMATION



****F grade has implemented additional test flows to ensure higher product quality than I grade**

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9.1 Valid Part Numbers

Please contact GigaDevice regional sales for the latest product selection and available form factors.

Temperature Range I: Industrial (-40℃ to +85℃)

Product Number	Density	Package Type	Packing Options
GD25D80EKIG	8Mbit	USON8 (1.5x1.5mm)	R
GD25D80EEIG	8Mbit	USON8 (3x2mm)	R
GD25D80ETIG	8Mbit	SOP8 150mil	T/Y/R

Temperature Range J: Industrial+ (-40℃ to +105℃)

Product Number	Density	Package Type	Packing Options
GD25D80EKJG	8Mbit	USON8 (1.5x1.5mm)	R
GD25D80EEJG	8Mbit	USON8 (3x2mm)	R
GD25D80ETJG	8Mbit	SOP8 150mil	T/Y/R

Temperature Range E: Industrial+ (-40℃ to +125℃)

Product Number	Density	Package Type	Packing Options
GD25D80EKEG	8Mbit	USON8 (1.5x1.5mm)	R
GD25D80EEEG	8Mbit	USON8 (3x2mm)	R
GD25D80ETEG	8Mbit	SOP8 150mil	T/Y/R

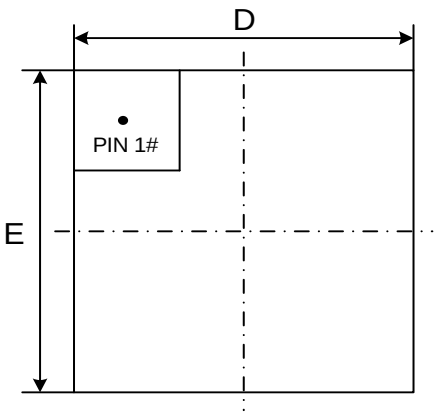
Temperature Range F: Industrial+ (-40℃ to +85℃)

Product Number	Density	Package Type	Packing Options
GD25D80EKFG	8Mbit	USON8 (1.5x1.5mm)	R
GD25D80EEFG	8Mbit	USON8 (3x2mm)	R
GD25D80ETFG	8Mbit	SOP8 150mil	T/Y/R

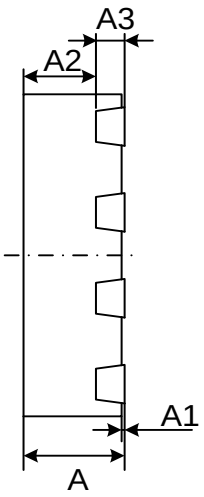
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10 PACKAGE INFORMATION

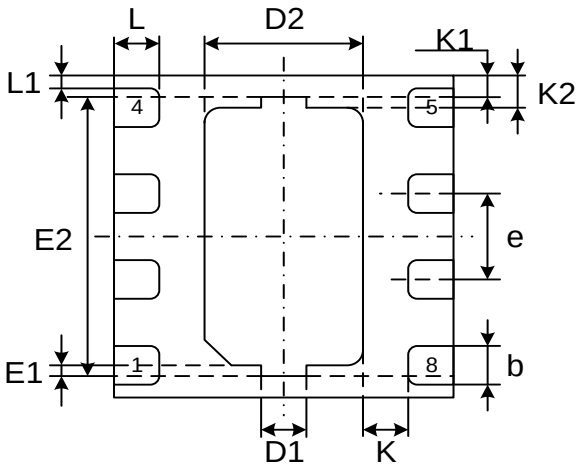
10.1 Package USON8 (1.5x1.5mm)



Top View



Side View



Bottom View

Dimensions

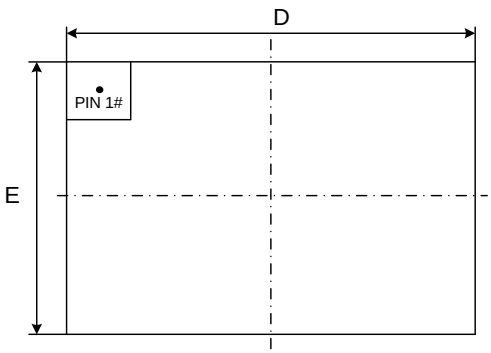
Symbol		A	A1	A2	A3	b	D	E	D1	E1	D2	E2	e	L	L1	K	K1	K2
Unit																		
mm	Min	0.40	0.00	0.33 REF	0.127 REF	0.13	1.40	1.40	0.20 REF	0.05 REF	0.60	1.20	0.40 REF	0.15	0.06 REF	0.20 REF	0.10 REF	0.15 REF
	Nom	0.45	0.02			0.18	1.50	1.50			0.70	1.30		0.20				
	Max	0.50	0.05			0.25	1.60	1.60			0.80	1.40		0.25				

Note:

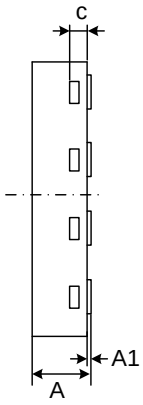
1. The exposed metal pad area on the bottom of the package is floating.
2. Coplanarity ≤0.08mm. Package edge tolerance≤0.10mm.
3. The lead shape may be of little difference according to different package factories. These lead shapes are compatible with each other.

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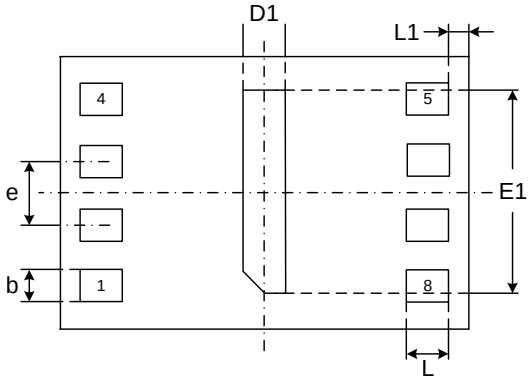
10.2 Package USON8 (3x2mm)



Top View



Side View



Bottom View

Dimensions

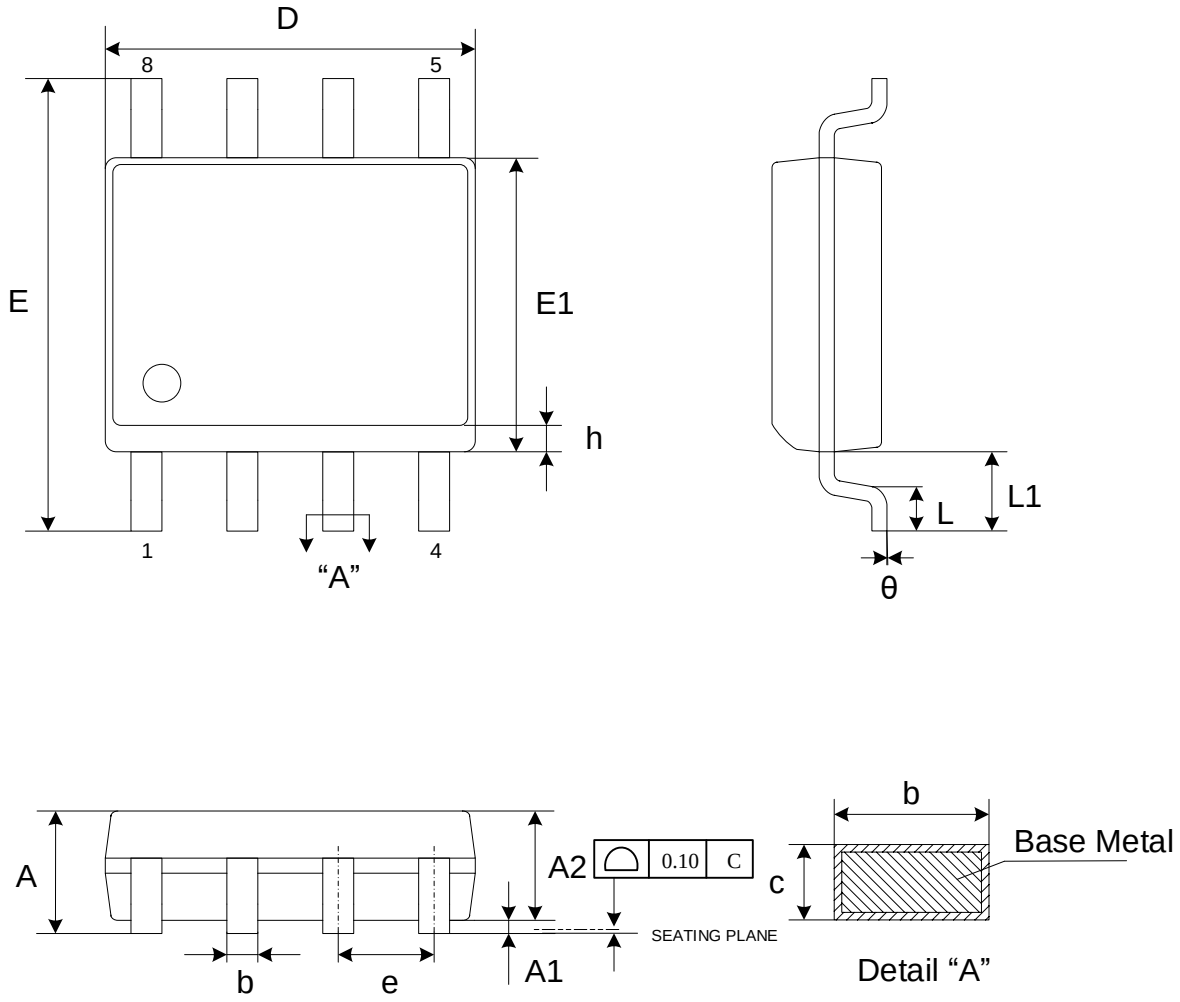
Symbol / Unit		A	A1	c	b	D	D1	E	E1	e	L	L1
mm	Min	0.40	0.00	0.10	0.20	2.90	0.15	1.90	1.55	0.50	0.30	0.10
	Nom	0.45	0.02	0.15	0.25	3.00	0.20	2.00	1.60		0.35	
	Max	0.50	0.05	0.20	0.30	3.10	0.25	2.10	1.65		0.40	

Note:

1. The exposed metal pad area on the bottom of the package is floating.
2. Coplanarity ≤0.08mm. Package edge tolerance≤0.10mm.
3. The lead shape may be of little difference according to different package factories. These lead shapes are compatible with each other.

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10.3 Package SOP8 150MIL



Dimensions

Symbol / Unit		A	A1	A2	b	c	D	E	E1	e	L	L1	h	θ
mm	Min	-	0.10	1.25	0.31	0.10	4.80	5.80	3.80	1.27	0.40	1.04	0.25	0°
	Nom	-	0.15	1.45	0.41	0.20	4.90	6.00	3.90		-		-	-
	Max	1.75	0.25	1.55	0.51	0.25	5.00	6.20	4.00		0.90		0.50	8°

Note:

1. Both the package length and width do not include the mold flash.

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11 REVISION HISTORY

Version No	Description	Page	Date
1.0	Initial release	All	2022-11-4

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