GD25D10B/05B

DATASHEET

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1. FEATURES

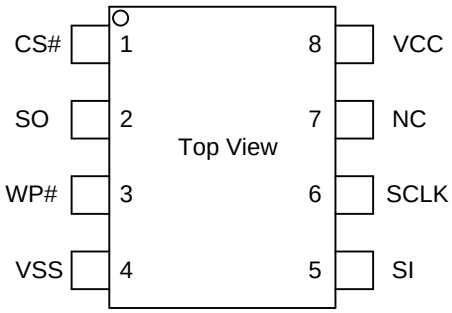
- 1M/512K-bit Serial Flash
  - -128K/64K-byte
  - -256 bytes per programmable page
- Standard, Dual Output
  - -Standard SPI: SCLK, CS#, SI, SO, WP#
  - -Dual Output: SCLK, CS#, IO0, O1, WP#
- Clock Frequency
  - -80MHz for fast read with 30PF load
  - -Dual Output Data transfer up to 160Mbits/s
- Software/Hardware Write Protection
  - -Write protect all/portion of memory via software
  - -Enable/Disable protection with WP# Pin
- Cycling endurance
  - -Minimum 100,000 Program/Erase Cycles
- Data retention
  - -20-year data retention typical
- Program/Erase Speed
  - -Page Program time: 0.7ms typical
  - -Sector Erase time: 40ms typical
  - -Block Erase time: 0.2/0.4s typical
  - -Chip Erase time:0.8/0.4s typical
- Flexible Architecture
  - -Sector of 4K-byte
  - -Block of 32/64k-byte
- Low Power Consumption
  - -18mA maximum active current
  - -5uA maximum power down current
- Single Power Supply Voltage
  - -Full voltage range:2.7~3.6V
- Package option
  - -SOP8 150MIL
  - -TSSOP8 173MIL
  - -USON8 2x3mm

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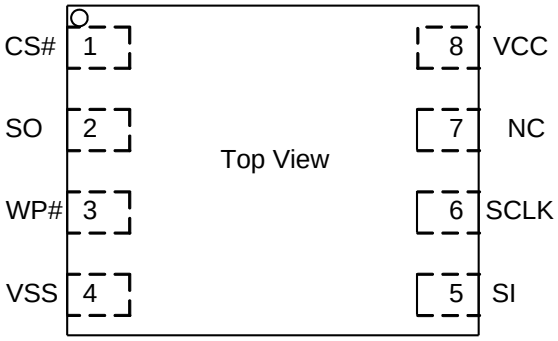
2. GENERAL DESCRIPTION

The GD25D10B/05B (1M/512K-bit) Serial flash supports the standard Serial Peripheral Interface (SPI), and supports the Dual Output: Serial Clock, Chip Select, Serial Data I/O0 (SI), O1 (SO). The Dual Output data is transferred with speed of 160Mbits/s.

CONNECTION DIAGRAM



8 – LEAD SOP/TSSOP



8 – LEAD USON

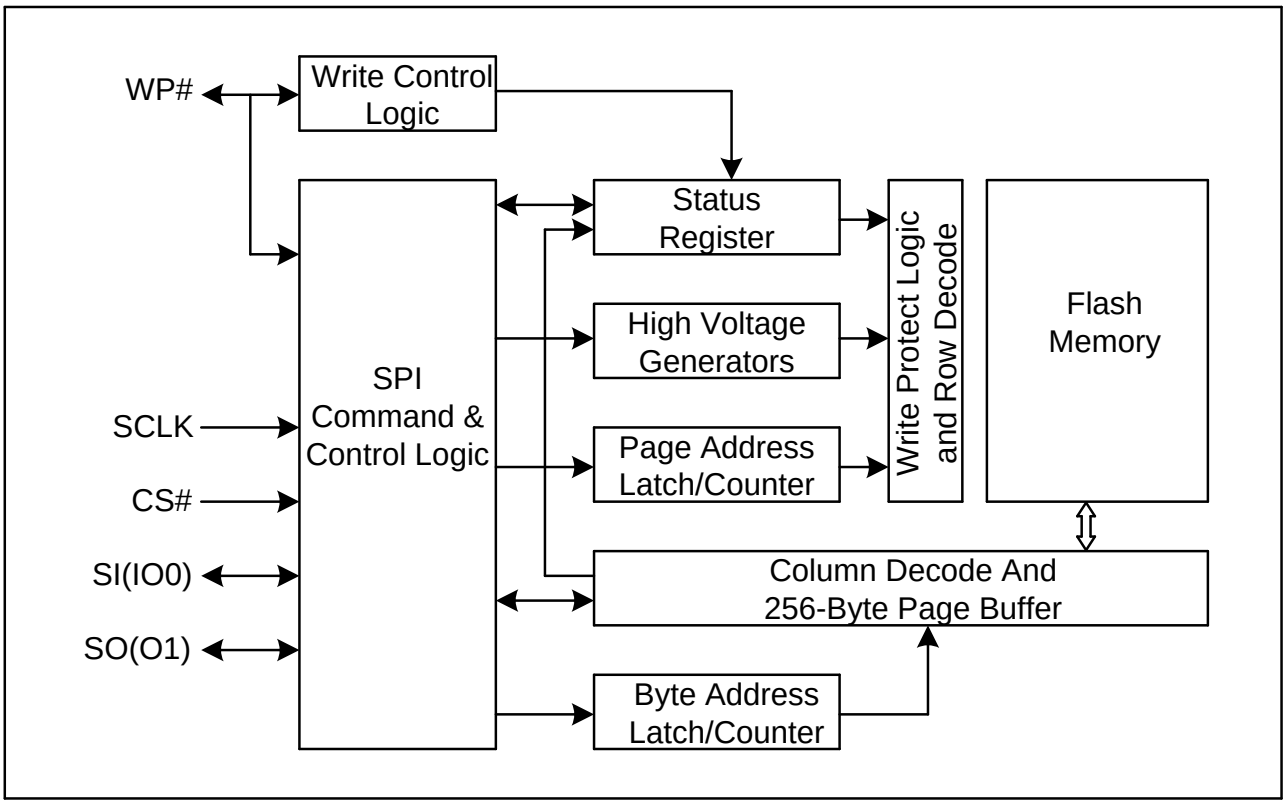
PIN DESCRIPTION

Pin Name	I/O	Description
CS#	**I**	Chip Select Input
SO (O1)	**O**	Data Output (Data Output 1)
WP#	**I**	Write Protect Input
VSS		Ground
SI (IO0)	**I/O**	Data Input (Data Input Output 0)
SCLK	**I**	Serial Clock Input
NC		No Connection
VCC		Power Supply

Note: CS# must be driven high if chip is not selected. Please don't leave CS# floating any time after power is on.

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BLOCK DIAGRAM



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3. MEMORY ORGANIZATION

GD25D10B

Each device has	Each block has	Each sector has	Each page has	
128K	64/32K	4K	256	bytes
512	256/128	16	-	pages
32	16/8	-	-	sectors
2/4	-	-	-	blocks

GD25D05B

Each device has	Each block has	Each sector has	Each page has	
64K	64/32K	4K	256	bytes
256	256/128	16	-	pages
16	16/8	-	-	sectors
1/2	-	-	-	blocks

UNIFORM BLOCK SECTOR ARCHITECTURE

GD25D10B 64K Bytes Block Sector Architecture

Block	Sector	Address range	
1	31	01F000H	01FFFFH
	……	……	……
	16	010000H	010FFFH
0	15	00F000H	00FFFFH
	……	……	……
	0	000000H	000FFFH

GD25D05 64K Bytes Block Sector Architecture

Block	Sector	Address range	
0	15	00F000H	00FFFFH
	……	……	……
	0	000000H	000FFFH

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4. DEVICE OPERATION

SPI Mode

Standard SPI

The GD25D10B/05B features a serial peripheral interface on 4 signals bus: Serial Clock (SCLK), Chip Select (CS#), Serial Data Input (SI) and Serial Data Output (SO). Both SPI bus mode 0 and 3 are supported. Input data is latched on the rising edge of SCLK and data shifts out on the falling edge of SCLK.

Dual SPI

The GD25D10B/05B supports Dual Output operation when using the “Dual Output Fast Read” (3BH) commands. These commands allow data to be transferred to or from the device at two times the rate of the standard SPI. When using the Dual Output command the SI and SO pins become bidirectional I/O pins: IO0 and O1.

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5. DATA PROTECTION

The GD25D10B/05B provides the following data protection methods:

- Write Enable (WREN) command: The WREN command is set the Write Enable Latch bit (WEL). The WEL bit will reset to 0 in the following situations:
  -Power-Up
  -Write Disable (WRDI)
  -Write Status Register (WRSR)
  -Page Program (PP)
  -Sector Erase (SE) / Block Erase (BE) / Chip Erase (CE)
- Software Protection Mode: The Block Protect (BP2, BP1, BP0) bits define the section of the protected memory area which is read-only and unalterable.
- Hardware Protection Mode: WP# going low to protected the BP0~BP2bits and SRP bits.
- Deep Power-Down Mode: In Deep Power-Down Mode, all commands are ignored except the Release from Deep Power-Down Mode command.
- Write Inhibit Voltage (VWI): Device would reset automatically when VCC is below a certain threshold VWI.

Table1.0(a) GD25D10B Protected area size

Status Register Content			Memory Content			
BP2	BP1	BP0	Blocks	Addresses	Density	Portion
0	0	0	NONE	NONE	NONE	NONE
0	0	1	Sector 0 to 29	000000H-01DFFFH	120KB	Lower 30/32
0	1	0	Sector 0 to 27	000000H-01BFFFH	112KB	Lower 28/32
0	1	1	Sector 0 to 23	000000H-017FFFH	96KB	Lower 24/32
1	0	0	Sector 0 to 15	000000H-00FFFFH	64KB	Lower 16/32
1	0	1	All	000000H-01FFFFH	128KB	ALL
1	1	X	All	000000H-01FFFFH	128KB	ALL

Table1.0(b) GD25D05B Protected area size

Status Register Content			Memory Content			
BP2	BP1	BP0	Blocks	Addresses	Density	Portion
0	0	0	NONE	NONE	NONE	NONE
0	0	1	Sector 0 to 29	000000H-00DFFFH	56KB	Lower 14/16
0	1	0	Sector 0 to 27	000000H-00BFFFH	48KB	Lower 12/16
0	1	1	Sector 0 to 23	000000H-007FFFH	32KB	Lower 8/16
1	X	X	All	000000H-00FFFFH	64KB	ALL

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6. STATUS REGISTER

S7	S6	S5	S4	S3	S2	S1	S0
SRP	Reserved	Reserved	BP2	BP1	BP0	WEL	WIP

The status and control bits of the Status Register are as follows:

WIP bit.

The Write In Progress (WIP) bit indicates whether the memory is busy in program/erase/write status register progress. When WIP bit is set to 1, it means the device is busy in program/erase/write status register progress. when WIP bit is cleared to 0, it means the device is not in program/erase/write status register progress. The default value of WIP is 0.

WEL bit.

The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1 the internal Write Enable Latch is set, when set to 0 the internal Write Enable Latch is reset and no Write Status Register, Program or Erase command is accepted. The default value of WEL is 0.

BP2, BP1, BP0 bits.

The Block Protect (BP2, BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against Program and Erase commands. These bits are written with the Write Status Register (WRSR) command. When the Block Protect (BP2, BP1, BP0) bits are set to 1, the relevant memory area (as defined in Table1).becomes protected against Page Program (PP), Sector Erase (SE) and Block Erase (BE) commands. The Block Protect (BP2, BP1, BP0) bits can be written provided that the Hardware Protected mode has not been set. The Chip Erase (CE) command is executed, if the Block Protect (BP2, BP1, BP0) bits are all 0. The default value of BP2:0 are 0s.

SRP bit

The Status Register Protect (SRP) bit operates in conjunction with the Write Protect (WP#) signal. The Status Register Write Protect (SRP) bit and Write Protect (WP#) signal set the device to the Hardware Protected mode. When the Status Register Protect (SRP) bit is set to 1, and Write Protect (WP#) is driven Low. In this mode, the non-volatile bits of the Status Register(SRP, BP2, BP1, BP0) become read-only bits and the Write Status Register (WRSR) instruction is not execution. The default value of SRP is 0.

SRP	#WP	Status Register	Description
0	X	Software Protected	The Status Register can be written to after a Write Enable command, WEL=1.(Default)
1	0	Hardware Protected	WP#=0, the Status Register locked and can not be written to.
1	1	Hardware Unprotected	WP#=1, the Status Register is unlocked and can be written to after a Write Enable command, WEL=1.

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7. COMMANDS DESCRIPTION

All commands, addresses and data are shifted in and out of the device by the host system, with the most significant bit first. On the first rising edge of SCLK after CS# is driven low, the one-byte command code must be shifted into the device, with the most significant bit first on SI, each bit being latched on the rising edges of SCLK.

See Table2, every command sequence starts with a one-byte command code. Depending on the command, this might be followed by address bytes, or data bytes, or dummy bytes. CS# must be driven high after the last bit of the command sequence has been shifted in.

For the command of Read, Fast Read, Read Status Register or Release from Deep Power-Down, and Read Device ID, the shifted-in command sequence is followed by a data-out sequence. CS# can be driven high after any bit of the data-out sequence is being shifted out.

For the command of Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Write Enable, Write Disable or Deep Power-Down command, CS# must be driven high exactly at a byte boundary, which means the clock pulse number should be an exact multiple of eight. Otherwise the command is rejected to executed. Especially for Page Program command, if at any time the input end is not a completed byte, nothing will be written into the memory array, neither would WEL bit be reset.

Table2. Commands

Command Name	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	n-Bytes
Write Enable	06H						
Write Disable	04H						
Read Status Register	05H	(S7-S0)					(continuous)
Write Status Register	01H	(S7-S0)					
Read Data	03H	A23-A16	A15-A8	A7-A0	(D7-D0)	(Next byte)	(continuous)
Fast Read	0BH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(continuous)
Dual Output Fast Read	3BH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)(1)	(continuous)
Page Program	02 H	A23-A16	A15-A8	A7-A0	(D7-D0)	Next byte	
Fast Page Program	F2 H	A23-A16	A15-A8	A7-A0	(D7-D0)	Next byte	
Sector Erase	20H	A23-A16	A15-A8	A7-A0			
Block Erase(32K)	52H	A23-A16	A15-A8	A7-A0			
Block Erase(64K)	D8H	A23-A16	A15-A8	A7-A0			
Chip Erase	C7/60 H						
Deep Power-Down	B9H						
Release From Deep Power-Down, And Read Device ID	ABH	dummy	dummy	dummy	(DID7-DID0)		(continuous)
Release From Deep Power-Down	ABH						
Manufacturer/ Device ID	90H	dummy	dummy	00H	(MID7-MID0)	(DID7-DID0)	(continuous)
Read Identification	9FH	(MID7-MID0)	(JDID15-JDID8)	(JDID7-JDID0)			(continuous)

NOTE:

1. Dual Output data

   IO0 = (D6, D4, D2, D0)

   O1 = (D7, D5, D3, D1)

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7.1. TABLE OF ID DEFINATION:

GD25D10B

Operation Code	M7-M0	ID15-ID8	ID7-ID0
9FH	C8	40	11
90H	C8		10
ABH			10

GD25D05B

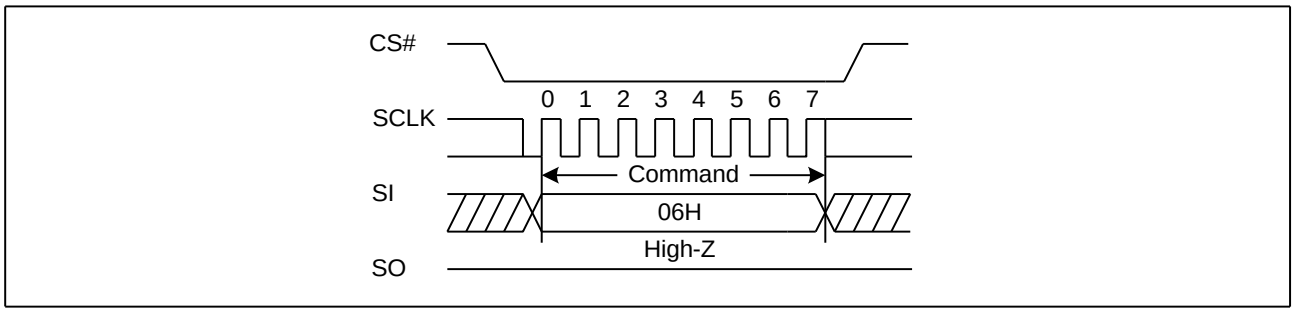
Operation Code	M7-M0	ID15-ID8	ID7-ID0
9FH	C8	40	10
90H	C8		05
ABH			05

7.2. Write Enable (WREN) (06H)

The Write Enable (WREN) command is for setting the Write Enable Latch (WEL) bit to 1. The Write Enable Latch (WEL) bit must be set prior to every Page Program (PP), Sector Erase (SE), Block Erase (BE), Chip Erase (CE) and Write Status Register (WRSR) command.

The Write Enable (WREN) command sequence: CS# goes low → sending the Write Enable command → CS# goes high.

Figure 1. Write Enable Sequence Diagram



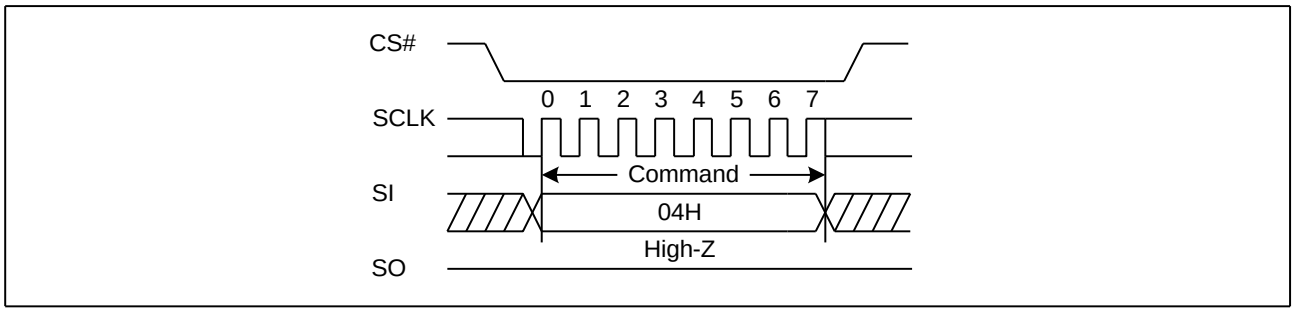
7.3. Write Disable (WRDI) (04H)

The Write Disable command is for resetting the Write Enable Latch (WEL) bit to 0. The WEL bit is reset by following condition: Power-up and upon completion of the Write Status Register, Page Program, Sector Erase, Block Erase and Chip Erase commands.

The Write Disable command sequence: CS# goes low→Sending the Write Disable command →CS# goes high.

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Figure 2. Write Disable Sequence Diagram

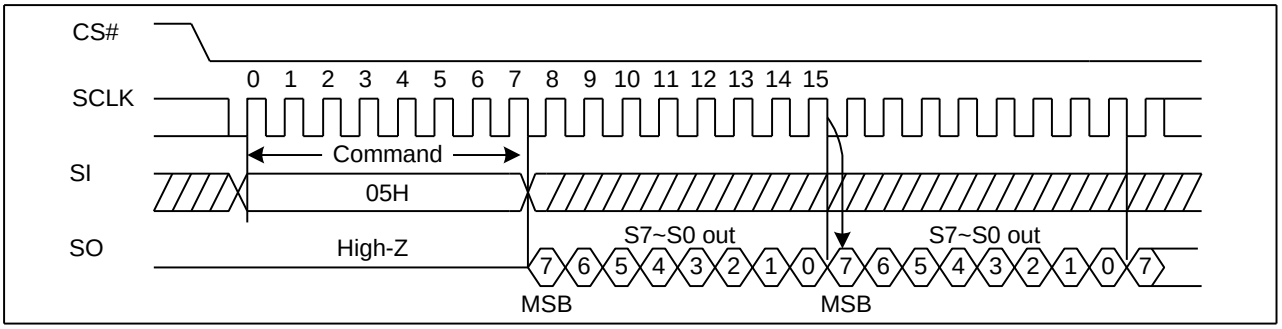


7.4. Read Status Register (RDSR) (05H)

The Read Status Register (RDSR) command is for reading the Status Register. The Status Register may be read at any time, even while a Program, Erase or Write Status Register cycle is in progress.

When one of these cycles is in progress, it is recommended to check the Write In Progress (WIP) bit before sending a new command to the device. It is also possible to read the Status Register continuously. For command code “05H”, the SO will output Status Register bits S7~S0.

Figure 3. Read Status Register Sequence Diagram



7.5. Write Status Register (WRSR) (01H)

The Write Status Register (WRSR) instruction allows new values to be written to the Status Register. A Write Enable (WREN) instruction must be executed previously to set the Write Enable Latch (WEL) bit, before it can be accepted.

The Write Status Register (WRSR) instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code and the data byte on Serial Data Input (DI).

The Write Status Register (WRSR) instruction has no effect on S6, S5, S1 and S0 of the Status Register. S6 and S5 are always read as 0. Chip Select (CS#) must be driven High after the eighth bit of the data byte has been latched in. Otherwise, the Write Status Register (WRSR) instruction is not executed. As soon as Chip Select (CS#) is driven High, the self-timed Write Status Register cycle (the duration is tW) is initiated. While the Write Status Register cycle is in progress, reading Status Register to check the Write In Progress (WIP) bit is achievable.

The Write In Progress (WIP) bit is 1 during the self-timed Write Status Register cycle, and turn to 0 on the completion of the Write Status Register. When the cycle is completed, the Write Enable Latch (WEL) is reset to 0.

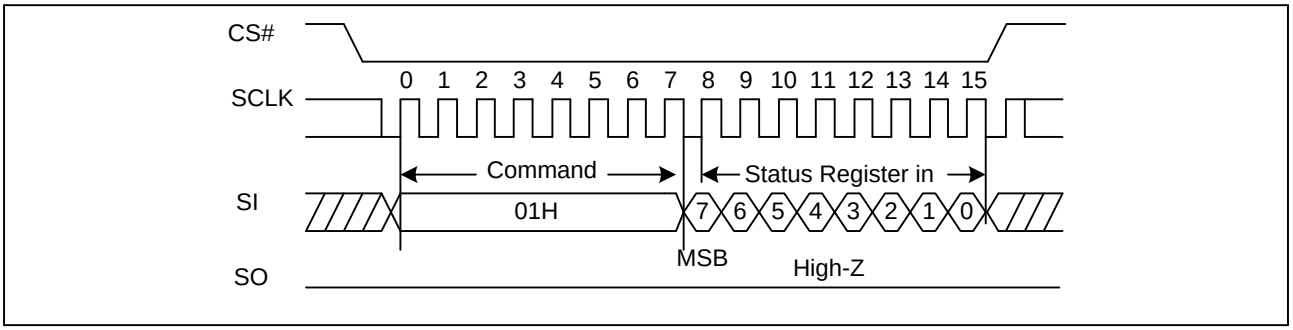
The Write Status Register (WRSR) instruction allows the user to change the values of the Block Protect (BP2, BP1,

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BP0) bits, which are utilized to define the size of the read-only area.

The Write Status Register (WRSR) instruction also allows the user to set or reset the Status Register Protect (SRP) bit in accordance with the Write Protect (WP#) signal, by setting which the device can enter into Hardware Protected Mode (HPM). The Write Status Register (WRSR) instruction is not executed once enter into the Hardware Protected Mode (HPM).

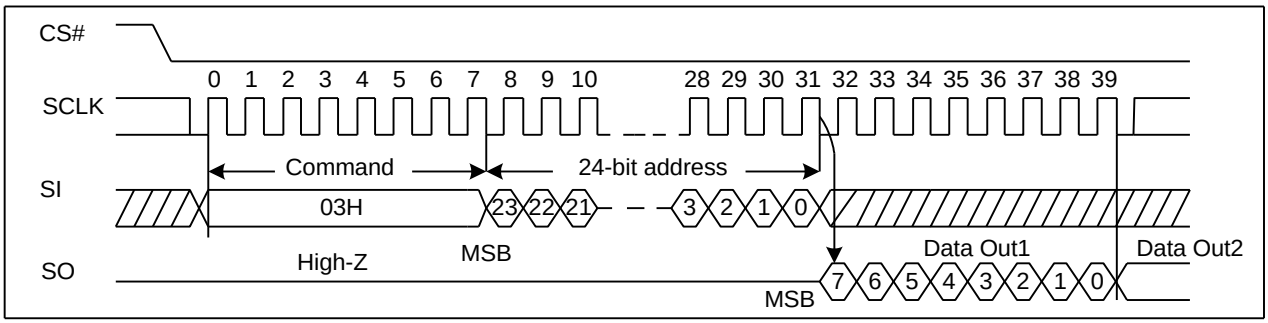
Figure 4. Write Status Register Sequence Diagram



7.6. Read Data Bytes (READ) (03H)

The Read Data Bytes (READ) command is followed by a 3-byte address (A23-A0), each bit being latched-in on the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency f_R, on the falling edge of SCLK. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes (READ) command. Any Read Data Bytes (READ) command, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 5. Read Data Bytes Sequence Diagram

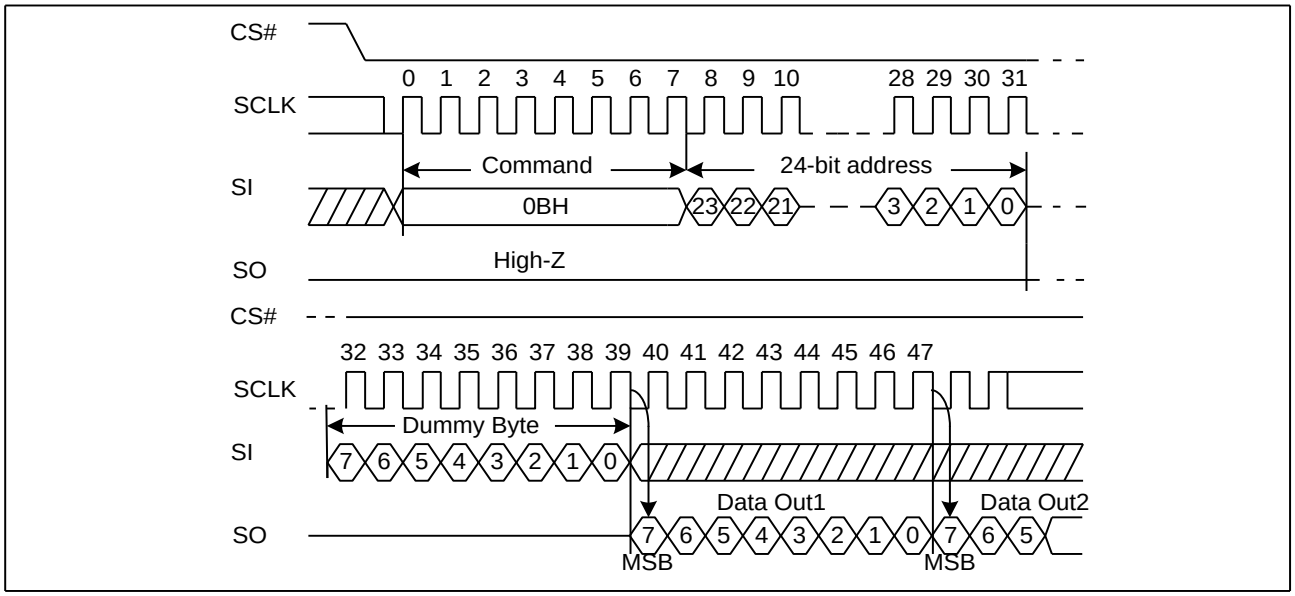


7.7. Read Data Bytes at Higher Speed (Fast Read) (0BH)

The Read Data Bytes at Higher Speed (Fast Read) command is for quickly reading data out. It is followed by a 3-byte address (A23-A0) and a dummy byte, each bit being latched-in on the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency f_C, on the falling edge of SCLK. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out.

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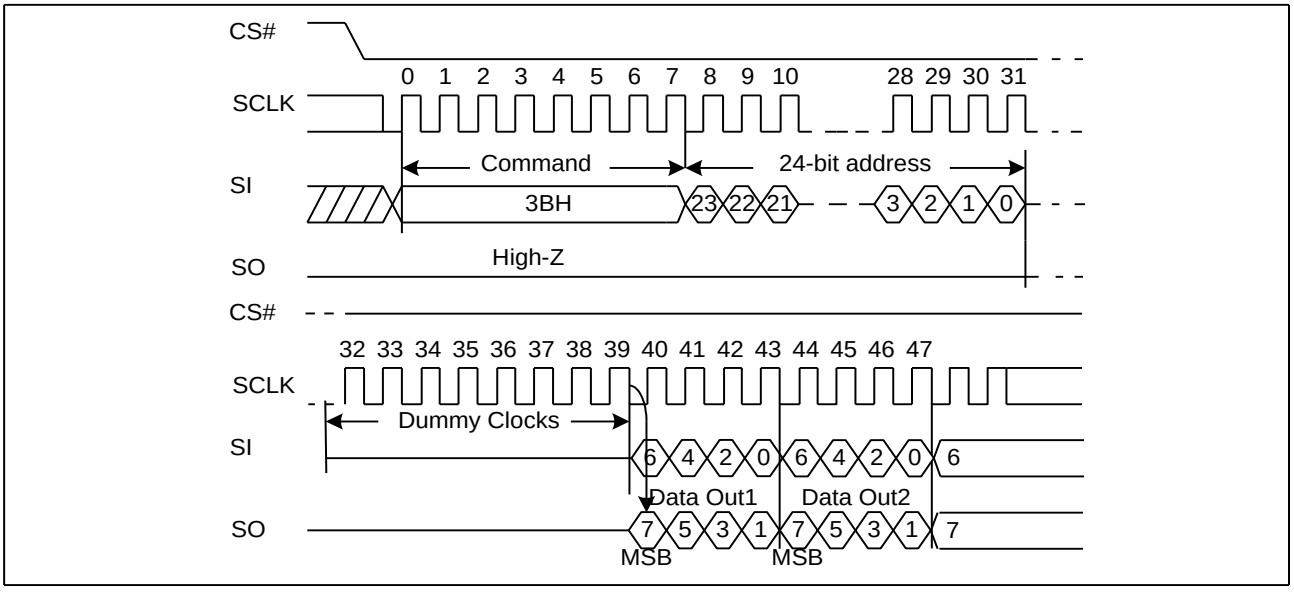
Figure 6. Read Data Bytes at Higher Speed Sequence Diagram



7.8. Dual Output Fast Read (3BH)

The Dual Output Fast Read command is followed by 3-byte address (A23-A0) and a dummy byte, each bit being latched in on the rising edge of SCLK, then the memory contents are shifted out 2-bit per clock cycle from SI and SO. The command sequence is shown in followed Figure7. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out.

Figure 7. Dual Output Fast Read Sequence Diagram



7.9. Page Program (PP) (02H)

The Page Program (PP) command is for programming the memory. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Page Program command.

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The Page Program (PP) command is entered by driving CS# Low, followed by the command code, three address bytes and at least one data byte on SI.

If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 8 least significant bits (A7-A0) are all zero). CS# must be driven low for the entire duration of the sequence.

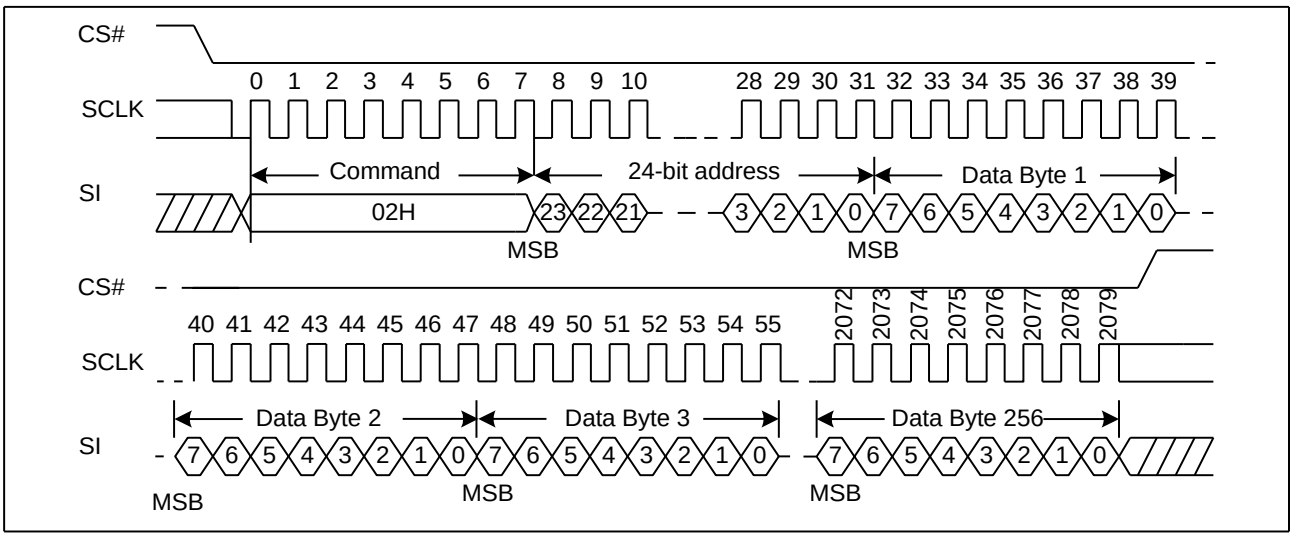
The Page Program command sequence: CS# goes low → sending Page Program command → 3-byte address on SI → at least 1 byte data on SI → CS# goes high. The command sequence is shown in Figure8.

If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page. CS# must be driven high after the eighth bit of the last data byte has been latched in; otherwise the Page Program (PP) command is not executed.

As soon as CS# is driven high, the self-timed Page Program cycle (whose duration is t_{PP}) is initiated. While the Page Program cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Page Program (PP) command is not executed when it is applied to a page protected by the Block Protect (BP2, BP1, BP0).

Figure 8. Page Program Sequence Diagram



7.10. Fast Page Program (FPP) (F2H)

The Fast Page Program (FPP) command is for programming the memory. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Page Program command.

The Fast Page Program (FPP) command is entered by driving CS# Low, followed by the command code, three address bytes and at least one data byte on SI. If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 8 least significant bits (A7-A0) are all zero). CS# must be driven low for the entire duration of the sequence.

The Page Program command sequence: CS# goes low → sending Page Program command → 3-byte address on SI → at least 1 byte data on SI → CS# goes high.

The command sequence is shown in Figure9. If more than 256 bytes are sent to the device, previously latched data

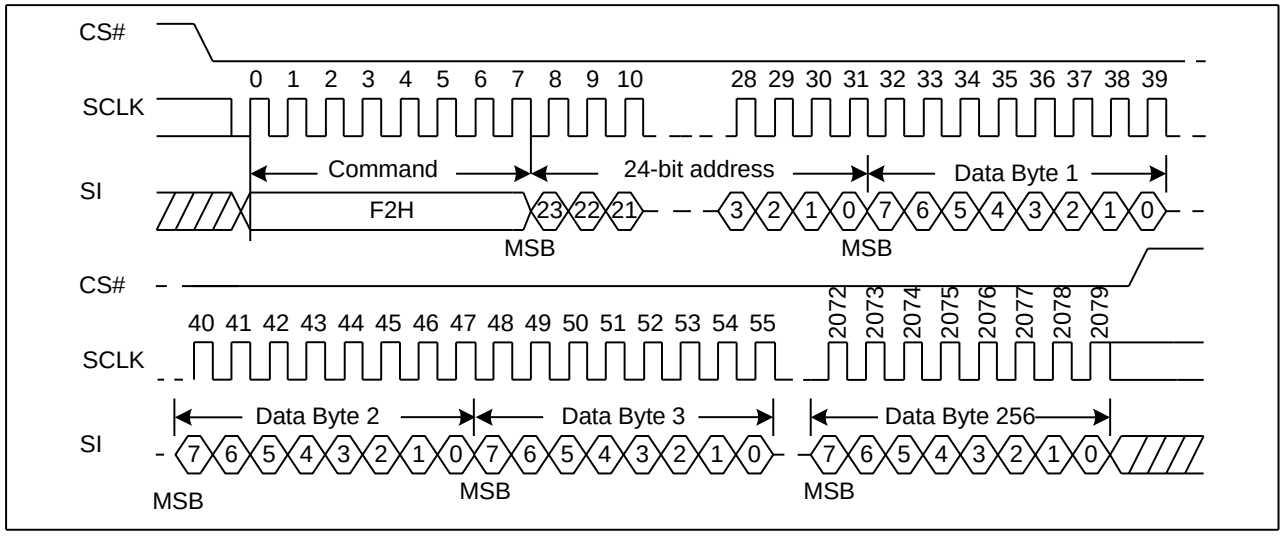
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are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page. CS# must be driven high after the eighth bit of the last data byte has been latched in; otherwise the Fast Page Program (FPP) command is not executed.

As soon as CS# is driven high, the self-timed Page Program cycle (whose duration is t_{PP}) is initiated. While the Page Program cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Fast Page Program (FPP) command is not executed when it is applied to a page protected by the Block Protect (BP2, BP1, BP0).

Figure 9. Fast Page Program Sequence Diagram



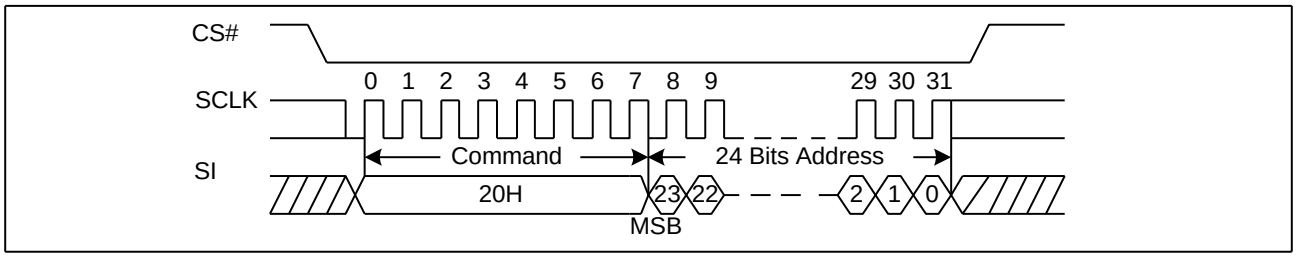
7.11. Sector Erase (SE) (20H)

The Sector Erase (SE) command is for erasing the all data of the specific sector. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The Sector Erase (SE) command is entered by driving CS# low, followed by the command code, and 3-address byte on SI. Any address inside the sector is a valid address for the Sector Erase (SE) command. CS# must be driven low for the entire duration of the sequence.

The Sector Erase command sequence: CS# goes low → sending Sector Erase command → 3-byte address on SI → CS# goes high. The command sequence is shown in Figure10. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the Sector Erase (SE) command is not executed. As soon as CS# is driven high, the self-timed Sector Erase cycle (whose duration is t_{SE}) is initiated. While the Sector Erase cycle is in progress, the Status Register is accessed to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Sector Erase cycle, and becomes 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A Sector Erase (SE) command applied to a sector which is protected by the Block Protect (BP2, BP1, BP0) bit (see Table1.0&1.1) is not executed.

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Figure 10. Sector Erase Sequence Diagram

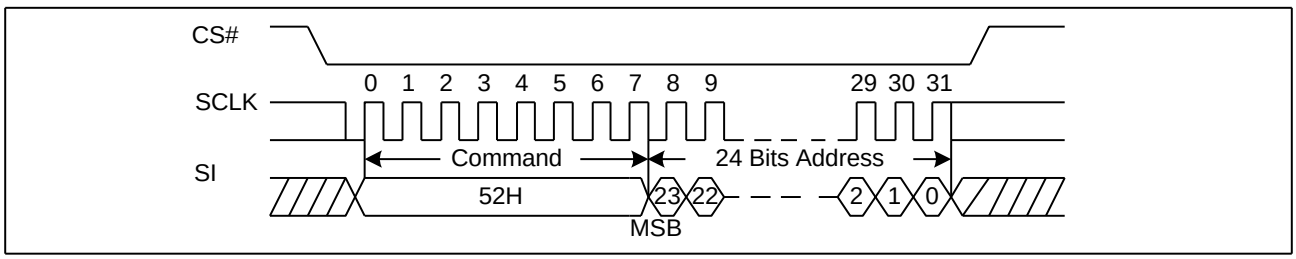


7.12. 32KB Block Erase (BE) (52H)

The 32KB Block Erase (BE) command is for erasing the all data of the chosen block. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The 32KB Block Erase (BE) command is entered by driving CS# low, followed by the command code, and three address bytes on SI. Any address inside the block is a valid address for the 32KB Block Erase (BE) command. CS# must be driven low for the entire duration of the sequence.

The 32KB Block Erase command sequence: CS# goes low → sending 32KB Block Erase command → 3-byte address on SI → CS# goes high. The command sequence is shown in Figure11. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the 32KB Block Erase (BE) command is not executed. As soon as CS# is driven high, the self-timed Block Erase cycle (whose duration is t_{BE}) is initiated. While the Block Erase cycle is in progress, the Status Register is accessed to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and becomes 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A 32KB Block Erase (BE) command applied to a block which is protected by the Block Protect (BP2, BP1, BP0) bits (see Table1.0&1.1) is not executed.

Figure 11. 32KB Block Erase Sequence Diagram



7.13. 64KB Block Erase (BE) (D8H)

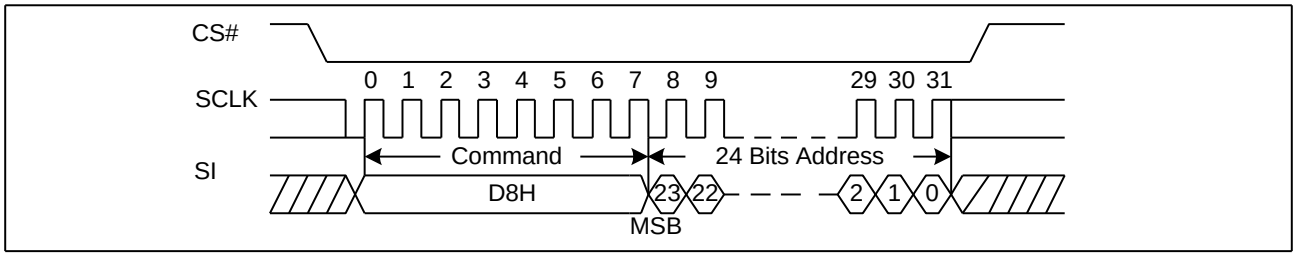
The 64KB Block Erase (BE) command is for erasing the all data of the chosen block. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The 64KB Block Erase (BE) command is entered by driving CS# low, followed by the command code, and three address bytes on SI. Any address inside the block is a valid address for the 64KB Block Erase (BE) command. CS# must be driven low for the entire duration of the sequence.

The 64KB Block Erase command sequence: CS# goes low → sending 64KB Block Erase command → 3-byte address on SI → CS# goes high. The command sequence is shown in Figure12. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the 64KB Block Erase (BE) command is not executed. As soon as CS# is driven high, the self-timed Block Erase cycle (whose duration is t_{BE}) is initiated. While the Block Erase cycle is in

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progress, the Status Register is accessed to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and becomes 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A 64KB Block Erase (BE) command applied to a block which is protected by the Block Protect (BP2, BP1, BP0) bits (see Table1.0&1.1) is not executed.

Figure 12. 64KB Block Erase Sequence Diagram

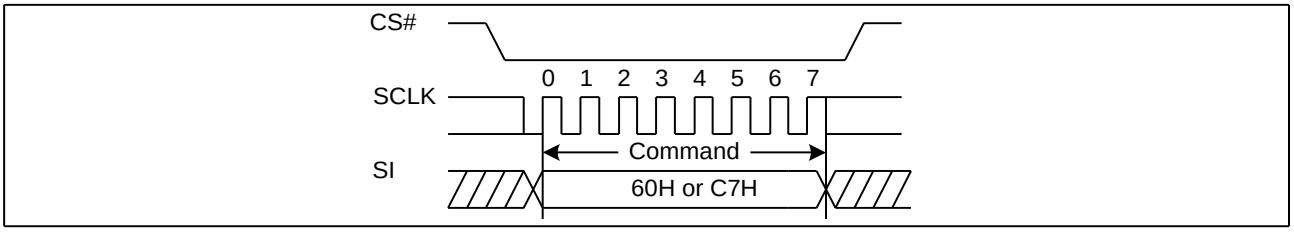


7.14. Chip Erase (CE) (60/C7H)

The Chip Erase (CE) command is for erasing the all data of the chip. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit .The Chip Erase (CE) command is entered by driving CS# Low, followed by the command code on Serial Data Input (SI). CS# must be driven Low for the entire duration of the sequence.

The Chip Erase command sequence: CS# goes low → sending Chip Erase command → CS# goes high. The command sequence is shown in Figure13. CS# must be driven high after the eighth bit of the command code has been latched in, otherwise the Chip Erase command is not executed. As soon as CS# is driven high, the self-timed Chip Erase cycle (whose duration is t_{CE}) is initiated. While the Chip Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Chip Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. The Chip Erase (CE) command is executed if the Block Protect (BP2, BP1, BP0) bits are all 0 or all 1. The Chip Erase (CE) command is not excuted if any sector is under protection.

Figure 13. Chip Erase Sequence Diagram



7.15. Deep Power-Down (DP) (B9H)

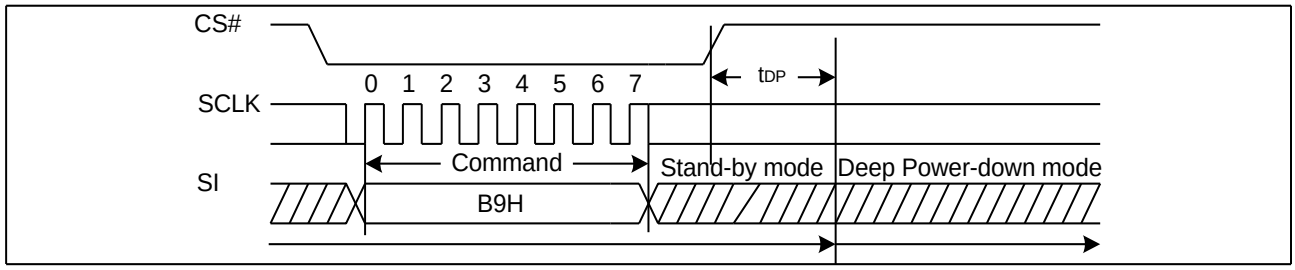
Executing the Deep Power-Down (DP) command is the only way to enter the lowest consumption mode (the Deep Power-Down Mode). Unlike deselecting the device by driving CS# high, or entering into the Standby Mode (if there is no internal cycle currently in progress), the Deep Power-Down Mode provides an extra software protection mechanism while the device is not in active use. The only access to this mode is by executing the Deep Power-Down (DP) command. Since in the Deep Power-Down mode, the device ignores all Write, Program and Erase commands. Once the device is in the Deep Power-Down Mode, all commands are ignored except the Release from Deep Power-Down and Read Device ID (RDI) command. This releases the device from this mode. The Release from Deep Power-Down and Read Device ID (RDI) command also allows the Device ID of the device to be output on SO.

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The Deep Power-Down Mode automatically stops at Power-Down, and the device always Power-Up in the Standby Mode. The Deep Power-Down (DP) command is entered by driving CS# low, followed by the command code on SI. CS# must be driven low for the entire duration of the sequence.

The Deep Power-Down command sequence: CS# goes low → sending Deep Power-Down command → CS# goes high. The command sequence is shown in Figure14. CS# must be driven high after the eighth bit of the command code has been latched in; otherwise the Deep Power-Down (DP) command is not executed. As soon as CS# is driven high, it requires a delay of t_{DP} before the supply current is reduced to I_{CC2} and the Deep Power-Down Mode is entered. Any Deep Power-Down (DP) command, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 14. Deep Power-Down Sequence Diagram



7.16. Release from Deep Power-Down / Read Device ID (ABH)

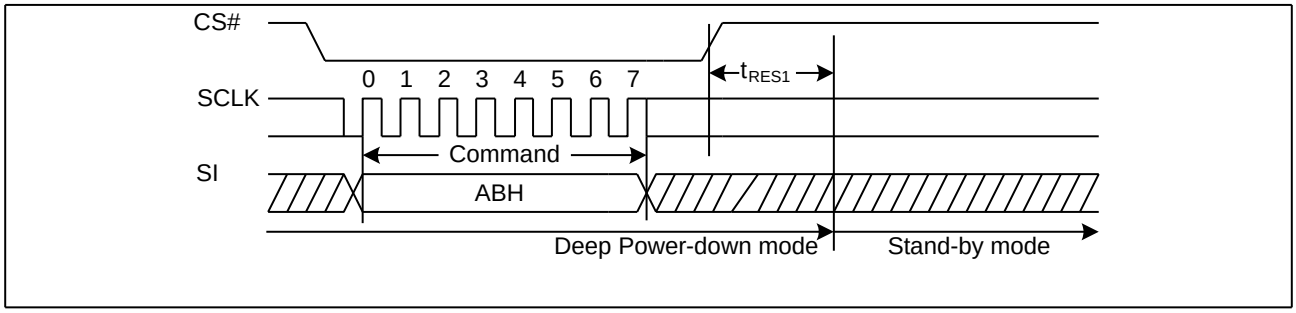
The Release from Power-Down and Read Device ID command is a multi-purpose command, which can be used to release the device from the Power-Down state or obtain the devices electronic identification (ID) number.

When used to release the device from the Power-Down state, the command is issued by driving the CS# pin low, shifting the instruction code “ABH” and driving CS# high as shown in Figure15. Release from Power-Down will take the time duration of t_{RES1} (See AC Characteristics) before the device will resume normal operation and other command are accepted. The CS# pin must keep high during the t_{RES1} time duration.

When used only to obtain the Device ID while not in the Power-Down state, the command is initiated by driving the CS# pin low and shifting the instruction code “ABH” followed by 3-dummy byte. The Device ID bits are then shifted out on the falling edge of SCLK with most significant bit (MSB) first as shown in Figure15. The Device ID value for the GD25D10B/05B is listed in Manufacturer and Device Identification table. The Device ID can be read continuously. The command is completed by driving CS# high.

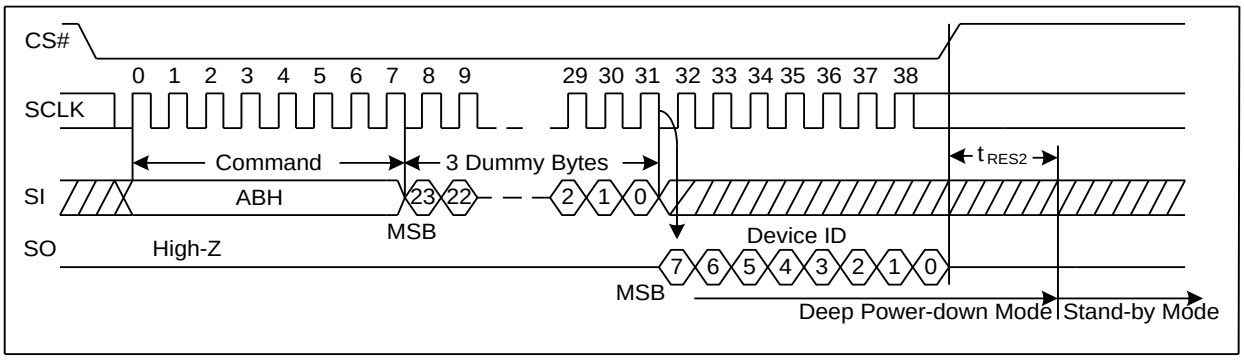
When used to release the device from the Power-Down state and obtain the Device ID, the command is the same as previously described, and shown in Figure16, except that after CS# is driven high it must remain high for a time duration of t_{RES2} (See AC Characteristics). After this time duration the device will resume normal operation and other command will be accepted. If the Release from Power-Down and Read Device ID command is issued while an Erase, Program or Write cycle is in process (when WIP equal 1) the command is ignored and will not have any effects on the current cycle.

Figure 15. Release Power-Down Sequence Diagram



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Figure 16. Release Power-Down and Read Device ID Sequence Diagram

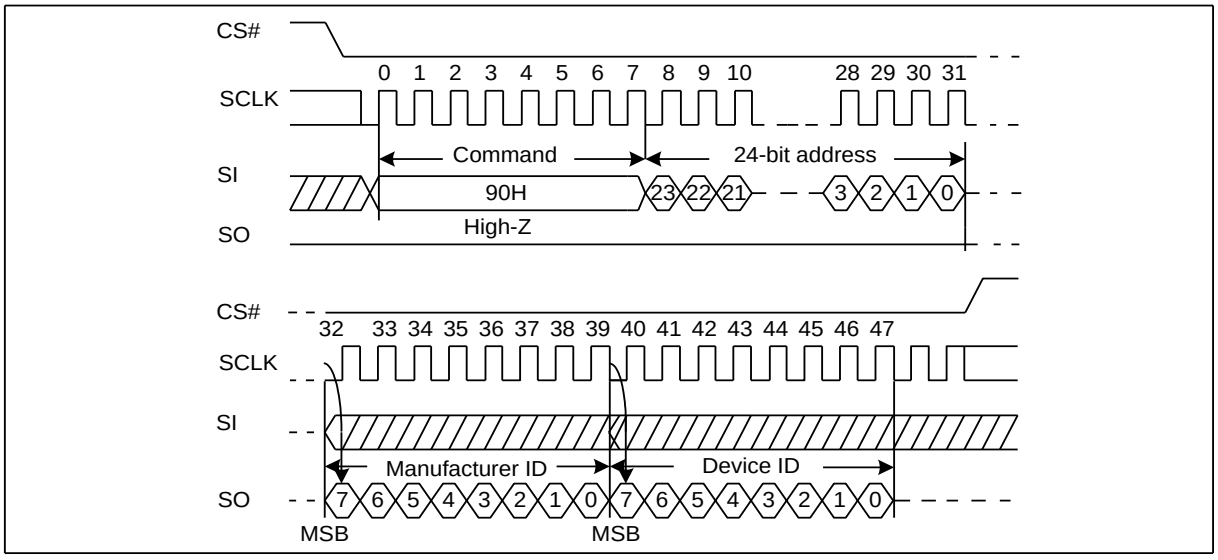


7.17. Read Manufacture ID/ Device ID (REMS) (90H)

The Read Manufacturer/Device ID command is an alternative to the Release from Power-Down / Device ID command that provides both the JEDEC assigned Manufacturer ID and the specific Device ID.

The command is initiated by driving the CS# pin low and shifting the command code “90H” followed by a 24-bit address (A23-A0) of 000000H. After that, the Manufacturer ID and the Device ID are shifted out on the falling edge of SCLK with most significant bit (MSB) first as shown in Figure17. If the 24-bit address is initially set to 000001H, the Device ID will be read first.

Figure 17. Read Manufacture ID/ Device ID Sequence Diagram



7.18. Read Identification (RDID) (9FH)

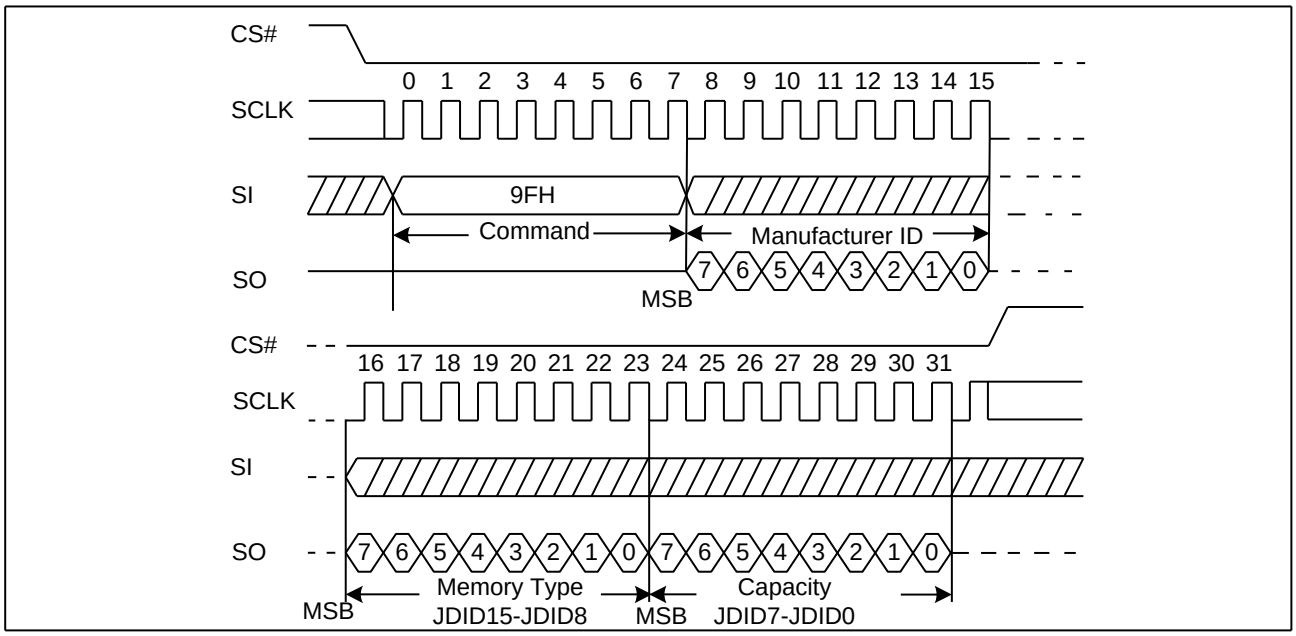
The Read Identification (RDID) command allows the 8-bit manufacturer identification to be read, followed by two bytes of device identification. The device identification indicates the memory type in the first byte, and the memory capacity of the device in the second byte. Any Read Identification (RDID) command while an Erase or Program cycle is in progress is not decoded, and has no effect on the cycle that is in progress. The Read Identification (RDID) command should not be issued while the device is in Deep Power-Down Mode.

The device is first selected by driving CS# to low. Then, the 8-bit command code for the command is shifted in. This is followed by the 24-bit device identification, stored in the memory, being shifted out on Serial Data Output, each bit being

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shifted out during the falling edge of Serial Clock. The command sequence is shown in Figure18. The Read Identification (RDID) command is terminated by driving CS# to high at any time during data output. When CS# is driven high, the device is put in the Standby Mode. Once in the Standby Mode, the device waits to be selected, so that it can receive, decode and execute commands.

Figure 18. Read Identification ID Sequence Diagram



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8. ELECTRICAL CHARACTERISTICS

8.1. POWER-ON TIMING

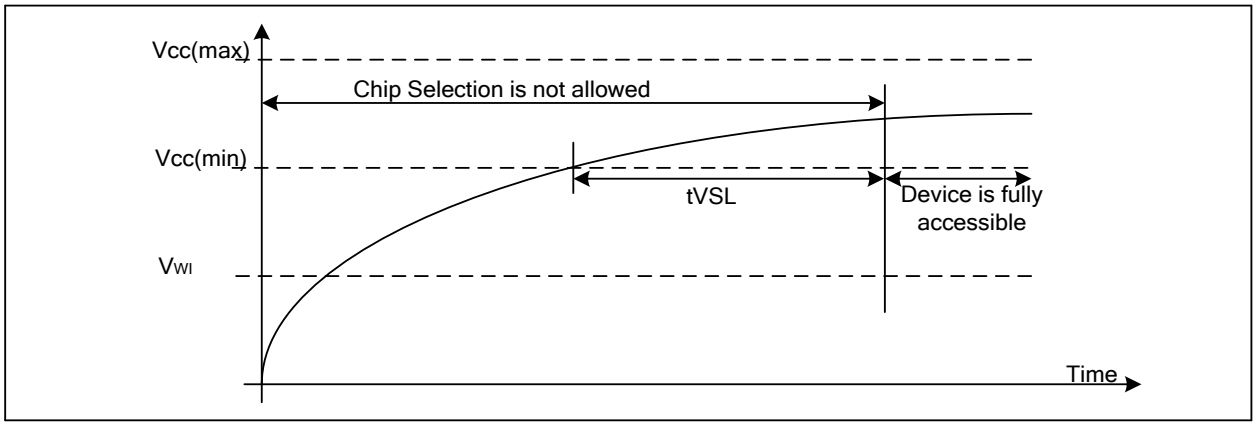


Table3. Power-Up Timing and Write Inhibit Threshold

Symbol	Parameter	Min	Max	Unit
tVSL	VCC(min) To CS# Low	5		ms
VWI	Write Inhibit Voltage	1.5	2.5	V

8.2. INITIAL DELIVERY STATE

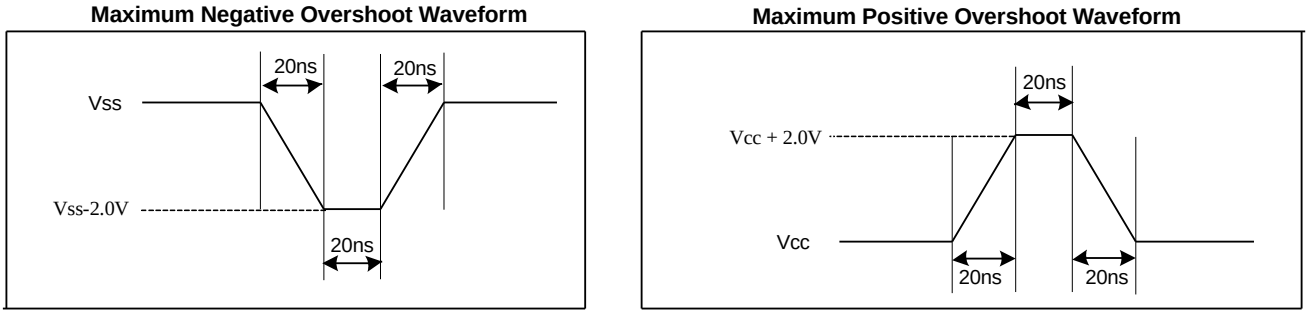
The device is delivered with the memory array erased: all bits are set to 1(each byte contains FFH).The Status Register contains 00H (all Status Register bits are 0).

8.3. ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Unit
Ambient Operating Temperature	-40 to 85	℃
Storage Temperature	-65 to 150c	℃
Applied Input/Output Voltage	-0.5 to 4.0	V
VCC	-0.5 to 4.0	V

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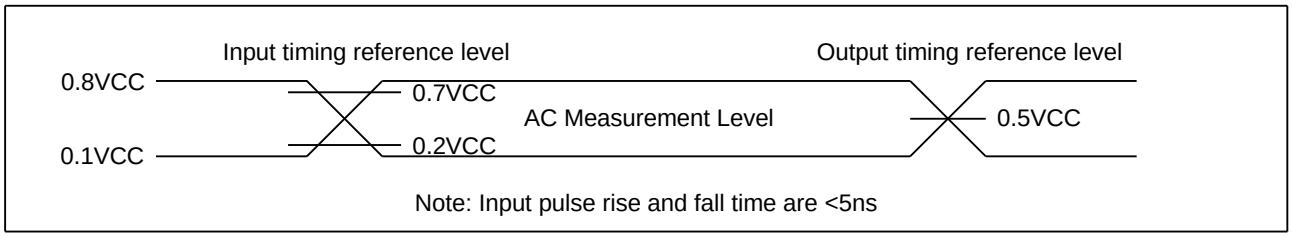
Figure 19. Maximum Negative/positive Overshoot Diagram



8.4. CAPACITANCE MEASUREMENT CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
CIN	Input Capacitance			6	pF	VIN=0V
COUT	Output Capacitance			8	pF	VOUT=0V
C_L	Load Capacitance		30		pF	
	Input Rise And Fall time			5	ns	
	Input Pulse Voltage	0.1VCC to 0.8VCC			V	
	Input Timing Reference Voltage	0.2VCC to 0.7VCC			V	
	Output Timing Reference Voltage	0.5VCC			V	

Figure 20. Input Test Waveform and Measurement Level



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8.5. DC CHARACTERISTICS

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Symbol	Parameter	Test Condition	Min.	Typ	Max.	Unit.
I_{LI}	Input Leakage Current				±2	μA
I_{LO}	Output Leakage Current				±2	μA
I_{CC1}	Standby Current	CS#=VCC, V_{IN}=VCC or VSS		1	5	μA
I_{CC2}	Deep Power-Down Current	CS#=VCC, V_{IN}=VCC or VSS		1	5	μA
I_{CC3}	Operating Current (Read)	CLK=0.1VCC / 0.9VCC at 80MHz, Q=Open(*1 I/O,*2 Output)		13	18	mA
I_{CC4}	Operating Current (PP)	CS#=VCC			10	mA
I_{CC5}	Operating Current(WRSR)	CS#=VCC			10	mA
I_{CC6}	Operating Current (SE)	CS#=VCC			10	mA
I_{CC7}	Operating Current (BE)	CS#=VCC			10	mA
V_{IL}	Input Low Voltage		-0.5		0.2VCC	V
V_{IH}	Input High Voltage		0.7VCC		VCC+0.4	V
V_{OL}	Output Low Voltage	I_{OL} =1.6mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} =-100μA	VCC-0.2			V

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8.6. AC CHARACTERISTICS

(T= -40℃~85℃, VCC=2.7~3.6V, C_L=30pf)

Symbol	Parameter	Min.	Typ.	Max.	Unit.
f_C	Serial Clock Frequency For: Dual Output(3BH)	DC.		80	MHz
f_R	Serial Clock Frequency For: Read(03H)	DC.		80	MHz
t_{CLH}	Serial Clock High Time	4			ns
t_{CLL}	Serial Clock Low Time	4			ns
t_{CLCH}	Serial Clock Rise Time (Slew Rate)	0.1			V/ns
t_{CHCL}	Serial Clock Fall Time (Slew Rate)	0.1			V/ns
t_{SLCH}	CS# Active Setup Time	5			ns
t_{CHSH}	CS# Active Hold Time	5			ns
t_{SHCH}	CS# Not Active Setup Time	5			ns
t_{CHSL}	CS# Not Active Hold Time	5			ns
t_{SHSL}	CS# High Time (Read/Write)	20			ns
t_{SHQZ}	Output Disable Time			6	ns
t_{CLQX}	Output Hold Time	0			ns
t_{DVCH}	Data In Setup Time	2			ns
t_{CHDX}	Data In Hold Time	2			ns
t_{CLQV}	Clock Low To Output Valid			6	ns
t_{WHSL}	Write Protect Setup Time Before CS# Low	20			ns
t_{SHWL}	Write Protect Hold Time After CS# High	100			ns
t_{DP}	CS# High To Deep Power-Down Mode			0.1	μs
t_{RES1}	CS# High To Standby Mode Without Electronic Signature Read			0.1	μs
t_{RES2}	CS# High To Standby Mode With Electronic Signature Read			0.1	μs
t_W	Write Status Register Cycle Time		2	15	ms
t_{PP}	Page Programming Time		0.7	4.0	ms
t_{FPP}	Fast Page Programming Time		0.5	4.0	ms
t_{SE}	Sector Erase Time		40	200	ms
t_{BE1}	Block Erase Time(32K Bytes)		0.2	0.6	s
t_{BE2}	Block Erase Time(64K Bytes)		0.4	1.0	s
t_{CE}	Chip Erase Time(GD25D10B/05B)		0.8/0.4	2.0/1.0	s

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Figure 21. Serial Input Timing

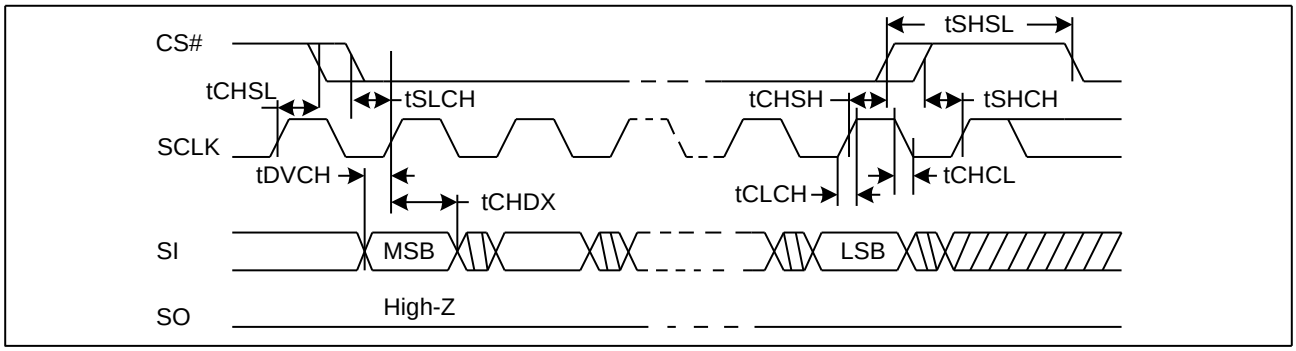
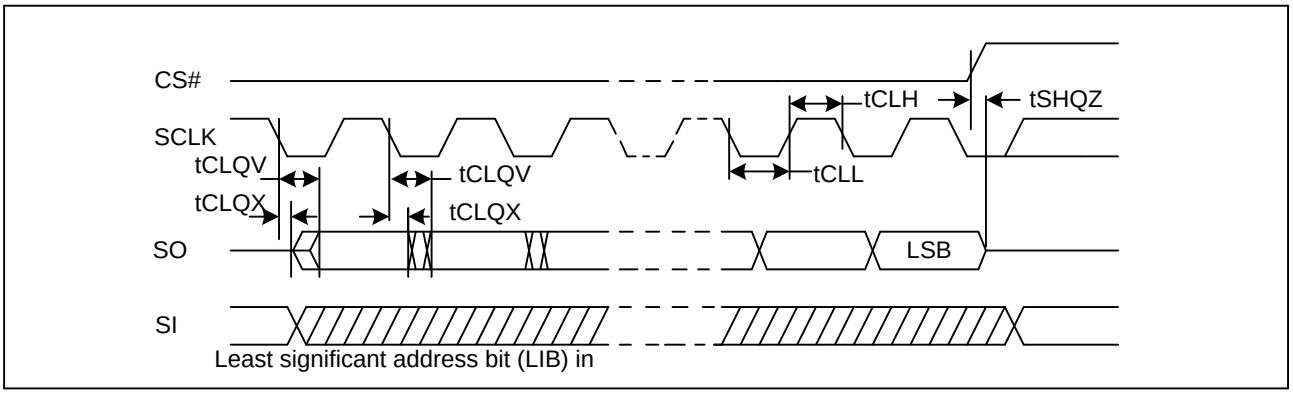
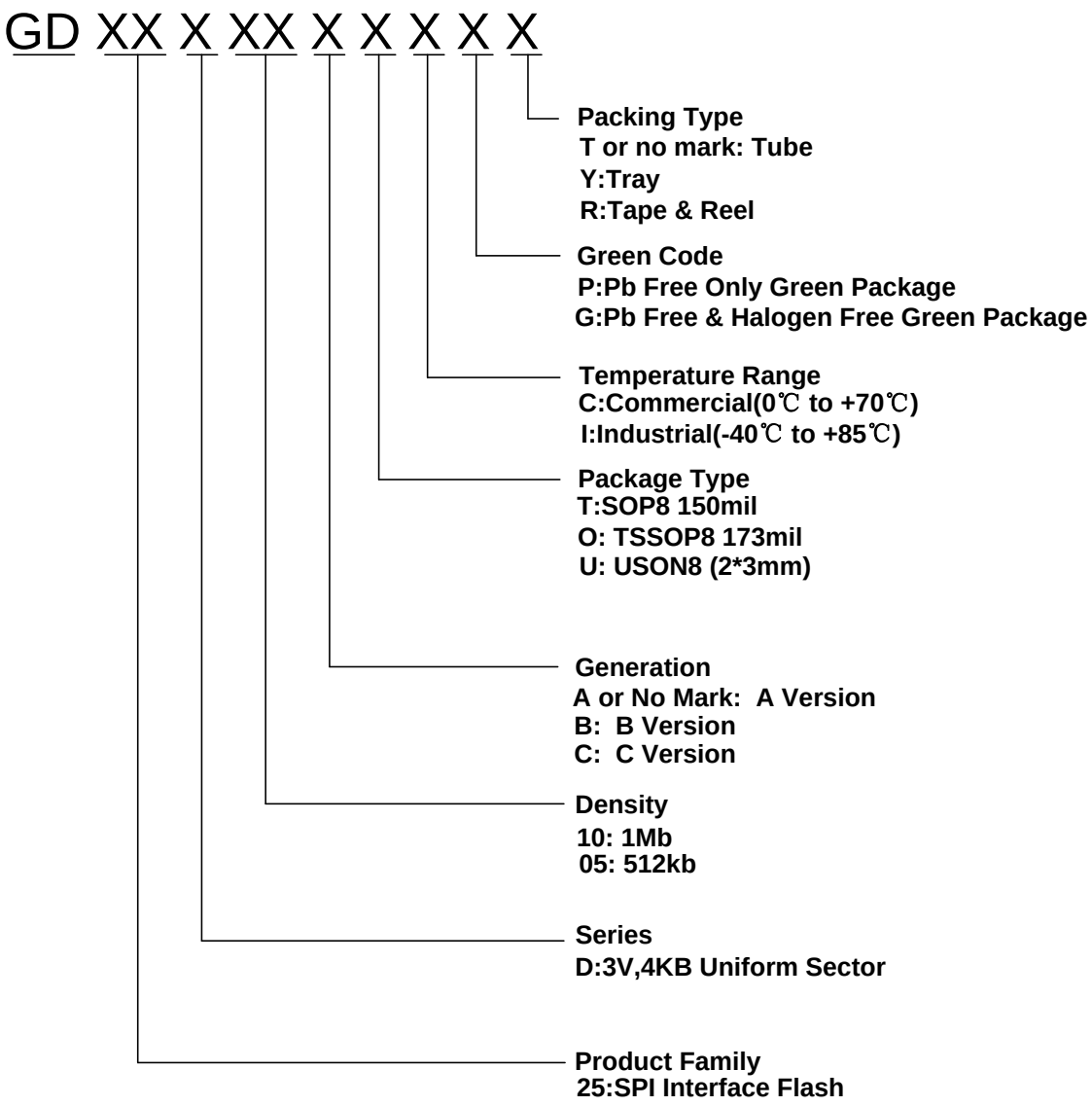


Figure 22. Output Timing



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9. ORDERING INFORMATION



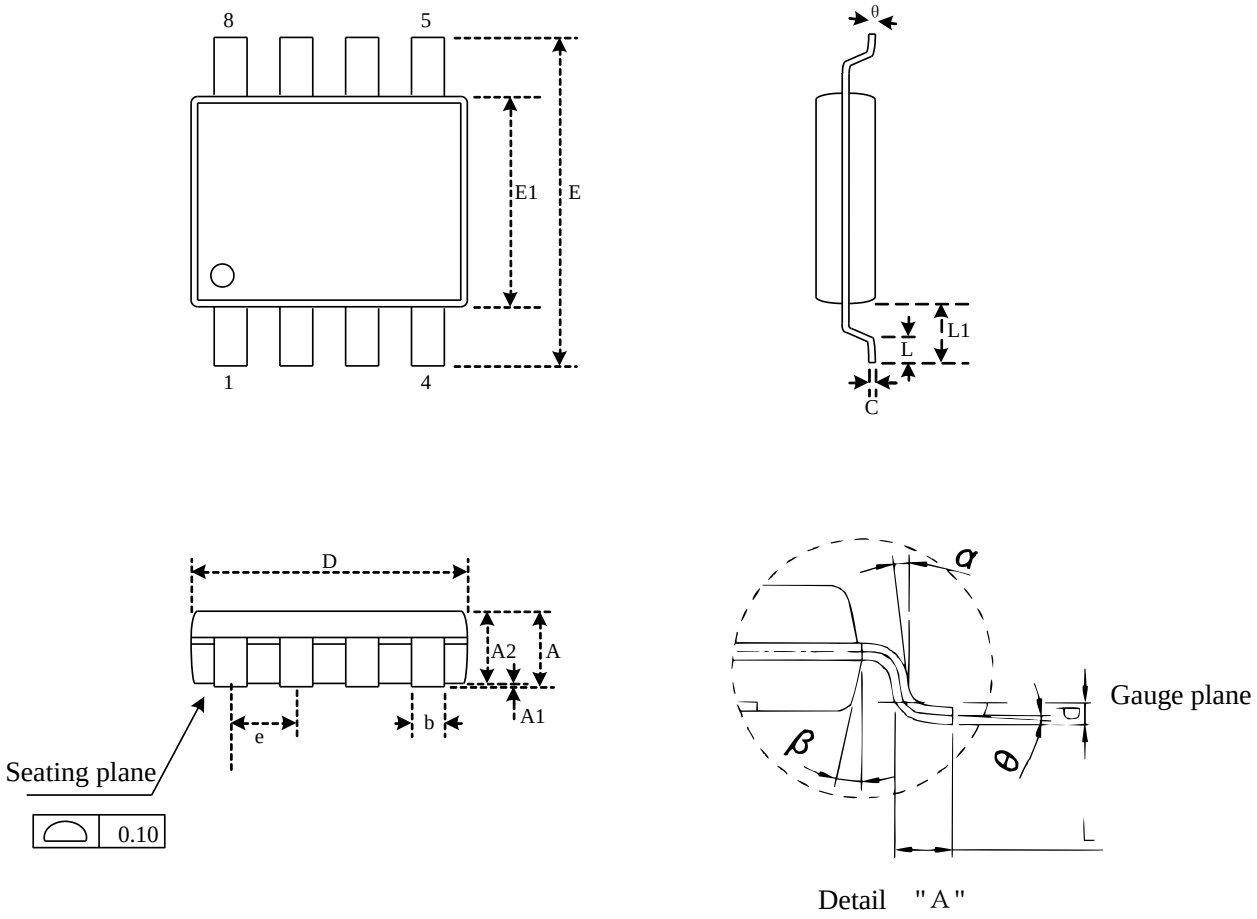
NOTE:

1. Standard bulk shipment is in Tube. Any alternation of packing method (for Tape, Reel and Tray etc.), please advise in advance.

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10. PACKAGE INFORMATION

10.1. Package SOP8 150MIL



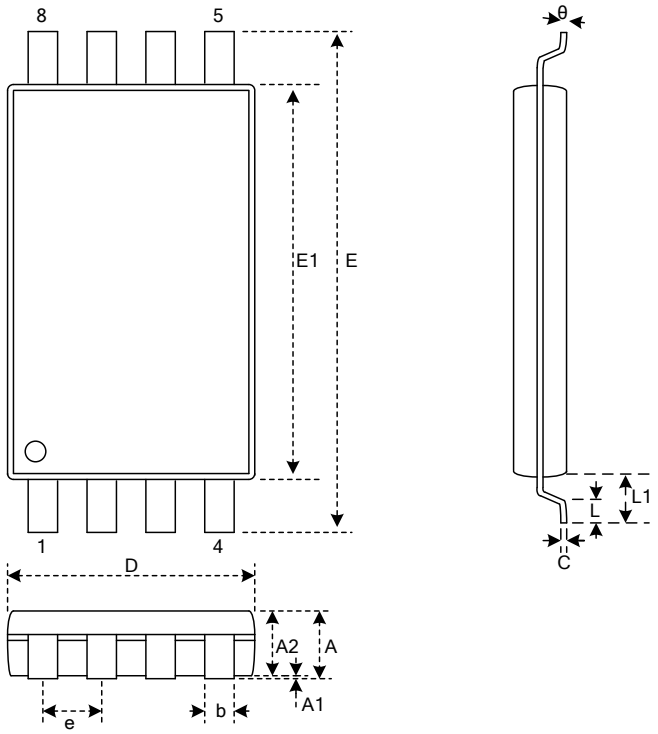
Dimensions

Symbol		A	A1	A2	b	C	D	E	E1	e	L	L1	θ	α	β
Unit															
mm	Min	-	0.05	1.35	0.31	0.15	4.77	5.80	3.80	-	0.40	0.85	0°	6°	11°
	Nom	-	-	-	-	-	4.90	6.00	3.90	1.27	-	1.06	-	7°	12°
	Max	1.75	0.25	1.55	0.51	0.25	5.03	6.20	4.00	-	0.90	1.27	8°	8°	13°
Inch	Min	-	0.002	0.053	0.012	0.006	0.188	-	0.149	-	0.016	0.033	0°	6°	11°
	Nom	-	-	-	0.016	-	0.193	0.236	0.154	0.050	-	0.042	-	7°	12°
	Max	0.069	0.010	0.061	0.020	0.010	0.198	-	0.158	-	0.035	0.050	8°	8°	13°

Note: Both package length and width do not include mold flash.

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10.2. Package TSSOP8 173MIL



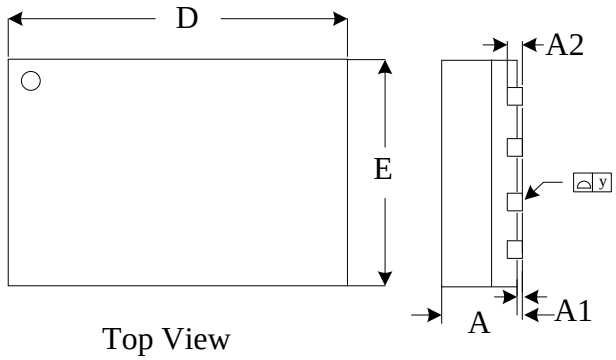
Dimensions

Symbol / Unit		A	A1	A2	b	C	D	E	E1	e	L	L1	θ
mm	Min	-	0.05	0.80	0.19	0.09	2.83	6.20	4.30	-	0.45	0.85	0
	Nom	-	0.10	0.92	0.24	0.14	2.96	6.40	4.40	0.65	0.60	1.00	4
	Max	1.20	0.15	1.05	0.30	0.20	3.10	6.60	4.50	-	0.75	1.15	8
Inch	Min	-	0.002	0.031	0.007	0.003	0.111	0.244	0.169	-	0.018	0.033	0
	Nom	-	0.004	0.036	0.010	0.006	0.116	0.252	0.173	0.026	0.024	0.039	4
	Max	0.047	0.006	0.041	0.012	0.008	0.122	0.260	0.177	-	0.030	0.045	8

Note:Both package length and width do not include mold flash.

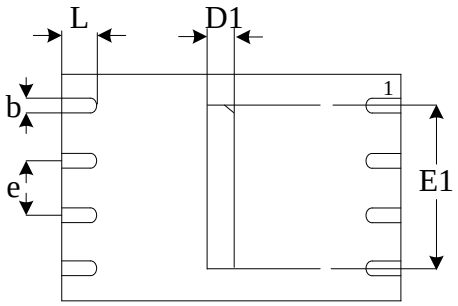
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10.3. Package USON8 (2*3mm)



Top View

Side View



Bottom View

Dimensions

Symbol / Unit		A	A1	A2	b	D	D1	E	E1	e	y	L
mm	Min	0.50		0.13	0.18	2.90	0.15	1.90	1.50		0.00	0.30
	Nom	0.55		0.15	0.25	3.00	0.20	2.00	1.60	0.50		0.35
	Max	0.60	0.05	0.18	0.30	3.10	0.30	2.10	1.70		0.05	0.45
Inch	Min	0.020		0.005	0.007	0.114	0.006	0.075	0.059		0.000	0.012
	Nom	0.022		0.006	0.010	0.118	0.008	0.079	0.063	0.020		0.014
	Max	0.024	0.002	0.007	0.012	0.122	0.012	0.083	0.067		0.002	0.018

Note:Both package length and width do not include mold flash.

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11. REVISION HISTORY

Version No	Description	Date
1.0	Initial Release:	2014-1-15
1.1	Update Package SOP8 150mil	2014-9-4
1.2	Update Status Register	2014-10-17
1.3	Update Package USON8 (3*2mm)	2015-6-11
1.4	Update Package TSSOP8 173MIL	2015-6-17
1.5	Update Package USON8 (3*2mm)	2015-6-18
1.6	Update Package TSSOP8 173MIL	2015-7-16
1.7	Modify AC CHARACTERISTICS: tCHCL Min.0.2 V/ns Change to 0.1 V/ns tCLCH Min.0.2 V/ns Change to 0.1 V/ns Modify Power-on Timing	2015-11-16
1.8	Modify POWER-ON TIMING: tVSL Min 10us Change to 5ms, VWI Min 1V Change to 1.5V. Modify Power-on Timing Sequence Diagram Modify Power-on Timing: Delete tPUW Modify General Description Modify Package USON8(2*3mm) Modify ORDERING INFORMATION Delete Data retention and endurance Delete Latch up characteristics	2016-7-11

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