Shanghai Fudan Microelectronics Group Company Limited

复旦微电子

# FM24C512D
# 2-Wire Serial EEPROM
## With Unique ID and Security Sector

**Data Sheet**

**Nov. 2013**



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## Description

The FM24C512D provides 524,288 bits of serial electrically erasable and programmable read-only memory (EEPROM) organized as 65,536 words of 8 bits each, with 128-bit UID and 128-byte Security Sector. The device's cascadable feature allows up to 8 devices to share a common 2-wire bus. The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operations are essential.

## Features

- **Low Operation Voltage: $V_{CC}$ = 1.7V to 5.5V**
- **Internally Organized: 65,536 x 8**
- **2-wire Serial Interface**
- **Schmitt Trigger, Filtered Inputs for Noise Suppression**
- **Bi-directional Data Transfer Protocol**
- **1MHz (2.5V~5.5V) and 400 kHz (1.7V) Compatibility**
- **Write Protect Pin for Hardware Data Protection**
- **128-Byte Page Write Modes (Partial Page Writes are Allowed)**
- **Lockable 128-Byte Security Sector**
- **128-Bit Unique ID for each device**
- **Self-timed Write Cycle (5 ms max)**
- **High-reliability**
  - **Endurance: 1,000,000 Write Cycles**
  - **Data Retention: 40 Years**
- **PDIP8, SOP8, TSSOP8 and TDFN8 Packages (RoHS Compliant and Halogen-free)**

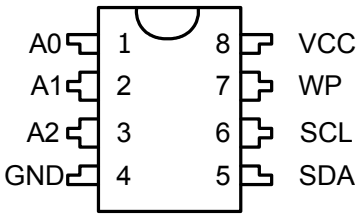
## Absolute Maximum Ratings

| | |
|---|---|
| Operating Temperature (Plastic Package) | -55°C to +125°C |
| Operating Temperature (Module Package) | -20°C to +60°C |
| Storage Temperature (Plastic Package) | -65°C to +150°C |
| Storage Temperature (Module Package) | -25°C to +70°C |
| Voltage on Any Pin with Respect to Ground | -1.0V to +7.0V |
| Maximum Operating Voltage | 6.25V |
| DC Output Current | 5.0 mA |

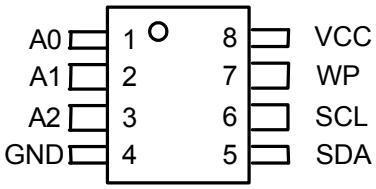
*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## Packaging Type

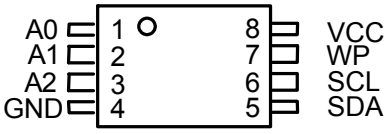
**PDIP 8**



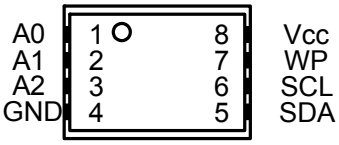

**SOP8**



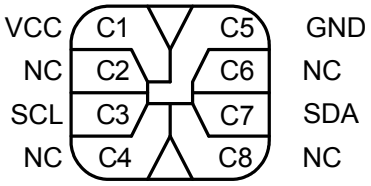

**TSSOP8**




**TDFN 8**




**Module package(8Pin)**



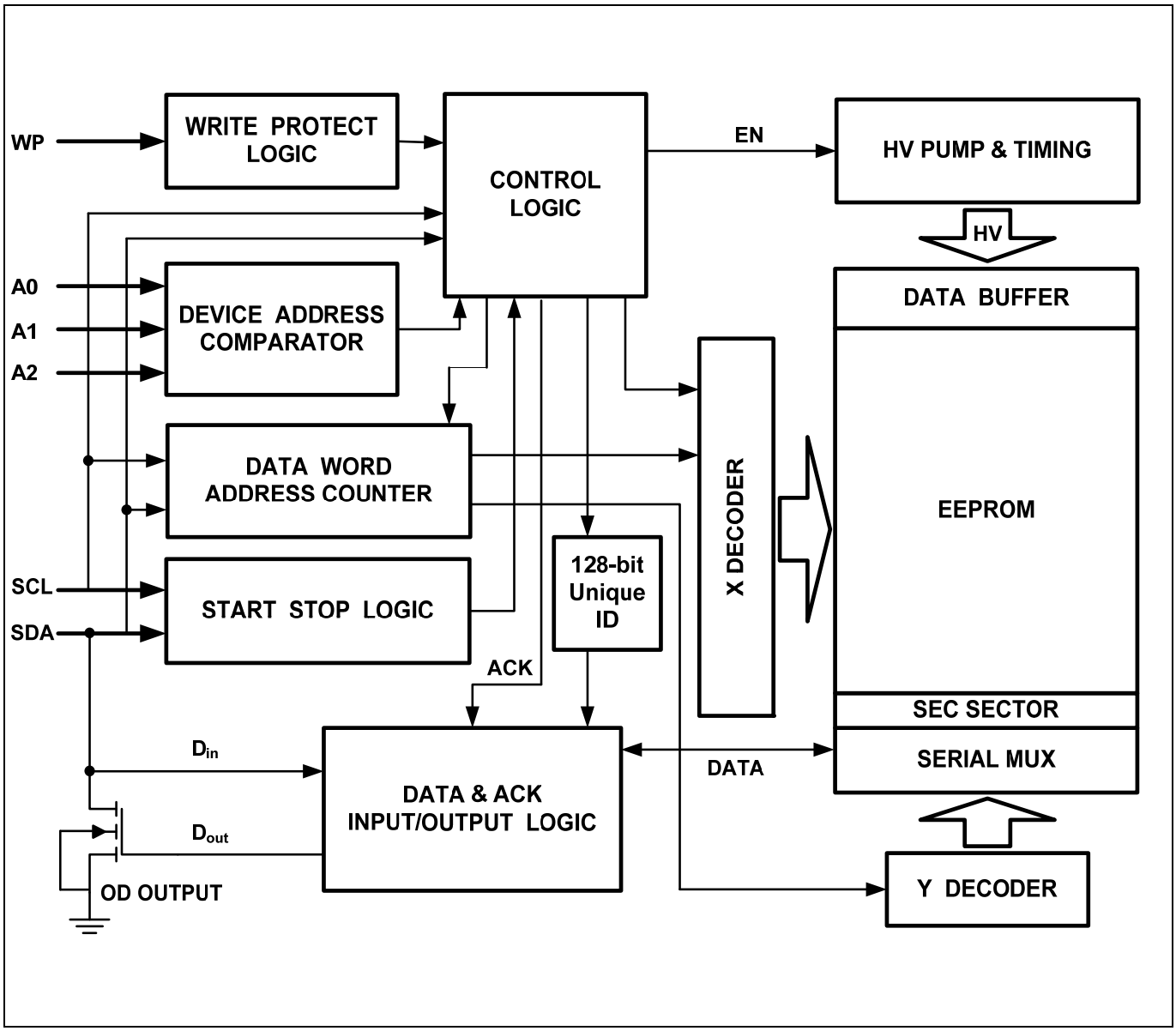

## Pin Configurations

| Pin Name | Function |
|---|---|
| A0~A2 | Device Address Inputs |
| SDA | Serial Data Input/Output |
| SCL | Serial Clock Input |
| WP | Write Protect |
| $V_{CC}$ | Power Supply |
| GND | Ground |
| NC | Not Connect |



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**Figure 1. Block Diagram**






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## Pin Description

**SERIAL CLOCK (SCL):** The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

**SERIAL DATA (SDA):** The SDA pin is bi-directional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open-collector devices.

**DEVICE/PAGE ADDRESSES (A2, A1, A0):** The A2, A1 and A0 pins are device address inputs that are hardwired or left not connected for hardware compatibility with other FM24CXX / FM24CXX devices. When the pins are hardwired, as many as eight 512K devices may be addressed on a single bus system (device addressing is discussed in detail under the Device Addressing section). If the pins are left floating, the A2, A1 and A0 pins will be internally pulled down to GND if the capacitive coupling to the circuit board $V_{CC}$ plane is <3pF, if coupling is >3pF, FMSH recommends connecting the address pins to GND.

**WRITE PROTECT (WP):** The FM24C512D has a Write Protect pin that provides hardware data protection. The WP pin allows normal write operations when connected to ground (GND). When the Write Protect pin is connected to VCC, all write operations to the memory are inhibited. If the pin is left floating, the WP pin will be internally pulled down to GND if the capacitive coupling to the circuit board Vcc plane is <3pF. If coupling is >3pF, FMSH recommends connecting the WP to GND. Switching WP to VCC prior to a write operation creates a software write protected function.

## Write Protect Description

| WP Pin Status | Part of the Memory Protected |
|---|---|
| | FM24C512D |
| WP=$V_{CC}$ | Full Memory |
| WP=GND | Normal Read/Write Operations |

## Memory Organization

**FM24C512D, 512K SERIAL EEPROM:** Internally organized with 512 pages of 128 bytes each, the 512K requires a 16-bit data word address for random word addressing.

**Security Sector:** The FM24C512D offers 128-byte Security Sectors which can be written and (later) permanently locked in Read-only mode. This memory may be used by the system manufacturers to store security and other important information separately from the main memory array.

**Unique ID:** The FM24C512D utilizes a separate memory block containing a factory programmed read-only 128-bit unique ID.

| Device ADDR | Page ADDR | Byte Number | | |
|---|---|---|---|---|
| | | 127 | ··· | 0 |
| 1010 | 0 | Data Memory (512P X 128B) | | |
| | 1 | | | |
| | 2 | | | |
| | ... | | | |
| | 511 | | | |
| 1011 | xxxx x00x xxxx xxxx[1] | Security Sector (128 Bytes) | | |
| 1011 | xxxx xx1x xxxx xxxx[2] | Unique ID（128 Bits） | | |

Note: 1. Address bits ADDR<10:9> must be 00, ADDR<6:0> define byte address, other bits are don't care
2. Address bits ADDR<10:9> must be x1, ADDR<3:0> define byte address, other bits are don't care



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## Pin Capacitance

| SYMBOL | PARAMETER | CONDITIONS | Max | Units |
|---|---|---|---|---|
| $C_{IN}$[1] | Input Capacitance | $V_{IN}$ = 0V, f = 1MHz | 6 | pF |
| $C_{OUT}$[1] | Output Capacitance | $V_{OUT}$ = 0V, f = 1MHz | 8 | pF |

Note: 1. This parameter is characterized and is not 100% tested.

## DC Characteristics

Applicable over recommended operating range from: $T_A$ = -40°C to +85°C, $V_{CC}$ = +1.7V to +5.5V, (unless otherwise noted).

| Symbol | Parameter | Test Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | | 1.7 | | 5.5 | V |
| $I_{CC1}$ | Supply Current | $V_{CC}$ = 5.0V, Read at 400KHz | | 0.4 | 1.0 | mA |
| $I_{CC2}$ | Supply Current | $V_{CC}$ = 5.0V, Write at 400KHz | | 2.0 | 3.0 | mA |
| $I_{SB1}$ | Standby Current | $V_{CC}$ = 1.7V, $V_{IN}$ = $V_{CC}$/ $V_{SS}$ | | | 1.0 | µA |
| $I_{SB2}$ | Standby Current | $V_{CC}$ = 5.5V, $V_{IN}$ = $V_{CC}$/ $V_{SS}$ | | | 6.0 | µA |
| $I_{LI}$ | Input Leakage Current | $V_{IN}$ = $V_{CC}$/$V_{SS}$ | | 0.1 | 3.0 | µA |
| $I_{LO}$ | Output Leakage Current | $V_{OUT}$ = $V_{CC}$/ $V_{SS}$ | | 0.05 | 3.0 | µA |
| $V_{IL}$[1] | Input Low Level | | -0.6 | | $V_{CC}$ x 0.3 | V |
| $V_{IH}$[1] | Input High Level | | $V_{CC}$ x 0.7 | | $V_{CC}$ + 0.5 | V |
| $V_{OL2}$ | Output Low Level 2 | $V_{CC}$ = 3.0V, $I_{OL}$ = 2.1 mA | | | 0.4 | V |
| $V_{OL1}$ | Output Low Level 1 | $V_{CC}$ =1.7V, $I_{OL}$ = 0.15 mA | | | 0.2 | V |

Note: 1. $V_{IL}$ min and $V_{IH}$ max are reference only and are not tested.



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# AC Characteristics

**400 kHz AC characteristics**

Recommended operating conditions: $T_A$ = -40°C to +85°C, $V_{CC}$ = +1.7V to +5.5V, CL = 100 pF (unless otherwise noted). Test conditions are listed in Note 2.

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $f_{SCL}$ | Clock Frequency, SCL | | 400 | kHz |
| $t_{LOW}$ | Clock Pulse Width Low | 1.3 | | µs |
| $t_{HIGH}$ | Clock Pulse Width High | 0.6 | | µs |
| $t_I$ [1] | Noise Suppression Time | | 80 | ns |
| $t_{AA}$ | Clock Low to Data Out Valid | 0.1 | 0.9 | µs |
| $t_{BUF}$ [1] | Time the bus must be free before a new transmission can Start | 1.3 | | µs |
| $t_{HD.STA}$ | Start Hold Time | 0.6 | | µs |
| $t_{SU.STA}$ | Start Setup Time | 0.6 | | µs |
| $t_{HD.DAT}$ | Data In Hold Time | 0 | | µs |
| $t_{SU.DAT}$ | Data In Setup Time | 100 | | ns |
| $t_R$ | Inputs Rise Time [1] | | 300 | ns |
| $t_F$ | Inputs Fall Time [1] | | 300 | ns |
| $t_{SU.STO}$ | Stop Setup Time | 0.6 | | µs |
| $t_{DH}$ | Data Out Hold Time | 100 | | ns |
| $t_{WR}$ | Write Cycle Time | | 5 | ms |
| Endurance [1] | 3.3V, 25°C, Page Mode | 1,000,000 | | Write Cycles |

**1 MHz AC characteristics**

Recommended operating conditions: $T_A$ = -40°C to +85°C, $V_{CC}$ = +2.5V to +5.5V, CL = 100 pF (unless otherwise noted). Test conditions are listed in Note 2.

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $f_{SCL}$ | Clock Frequency, SCL | | 1 | MHz |
| $t_{LOW}$ | Clock Pulse Width Low | 500 | | ns |
| $t_{HIGH}$ | Clock Pulse Width High | 320 | | ns |
| $t_I$ [1] | Noise Suppression Time | | 80 | ns |
| $t_{AA}$ | Clock Low to Data Out Valid | | 450 | ns |
| $t_{BUF}$ [1] | Time the bus must be free before a new transmission can Start | 500 | | ns |
| $t_{HD.STA}$ | Start Hold Time | 250 | | ns |
| $t_{SU.STA}$ | Start Setup Time | 250 | | ns |
| $t_{HD.DAT}$ | Data In Hold Time | 0 | | ns |
| $t_{SU.DAT}$ | Data In Setup Time | 50 | | ns |
| $t_R$ | Inputs Rise Time [1] | | 120 | ns |
| $t_F$ | Inputs Fall Time [1] | | 120 | ns |
| $t_{SU.STO}$ | Stop Setup Time | 250 | | ns |
| $t_{DH}$ | Data Out Hold Time | 100 | | ns |
| $t_{WR}$ | Write Cycle Time | | 5 | ms |
| Endurance [1] | 3.3V, 25°C, Page Mode | 1,000,000 | | Write Cycles |



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Notes: 1. This parameter is characterized and is not 100% tested.

2. AC measurement conditions:

RL (connects to $V_{CC}$): 1.3 kΩ

Input pulse voltages: 0.3 $V_{CC}$ to 0.7 $V_{CC}$

Input rise and fall times: ≤ 50 ns

Input and output timing reference voltages: 0.5 $V_{CC}$



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## Device Operation

**CLOCK and DATA TRANSITIONS:** The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (refer to Figure 4). Data changes during SCL high periods will indicate a start or stop condition as defined below.

**START CONDITION:** A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (refer to Figure 5).

**STOP CONDITION:** A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode (refer to Figure 5).

**ACKNOWLEDGE:** All address and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a zero during the ninth clock cycle to acknowledge that it has received each word.

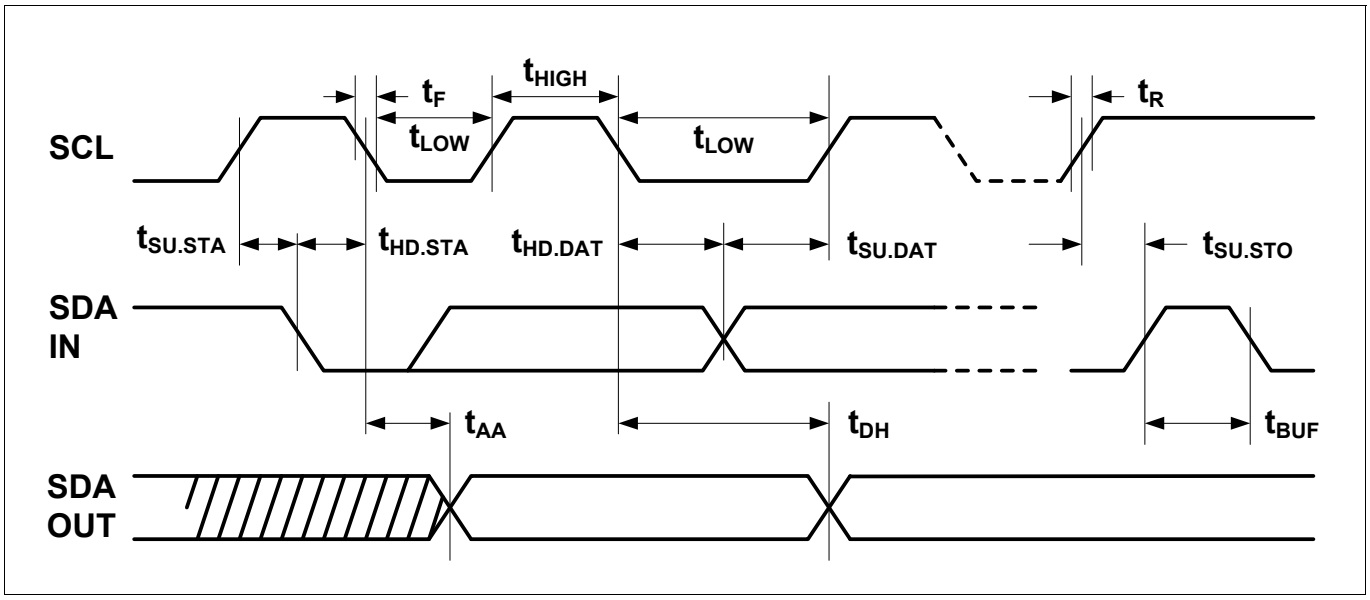
**STANDBY MODE:** The FM24C512D features a low-power standby mode which is enabled: (a) upon power-up and (b) after the receipt of the stop bit and the completion of any internal operations.

**Memory RESET:** After an interruption in protocol, power loss or system reset, any 2-wire part can be reset in following these steps:

1. Clock up to 9 Cycles,
2. Look for SDA high in each cycle while SCL is high and then,
3. Create a start condition as SDA is high.

## Bus Timing

### Figure 2. SCL: Serial Clock, SDA: Serial Data I/O

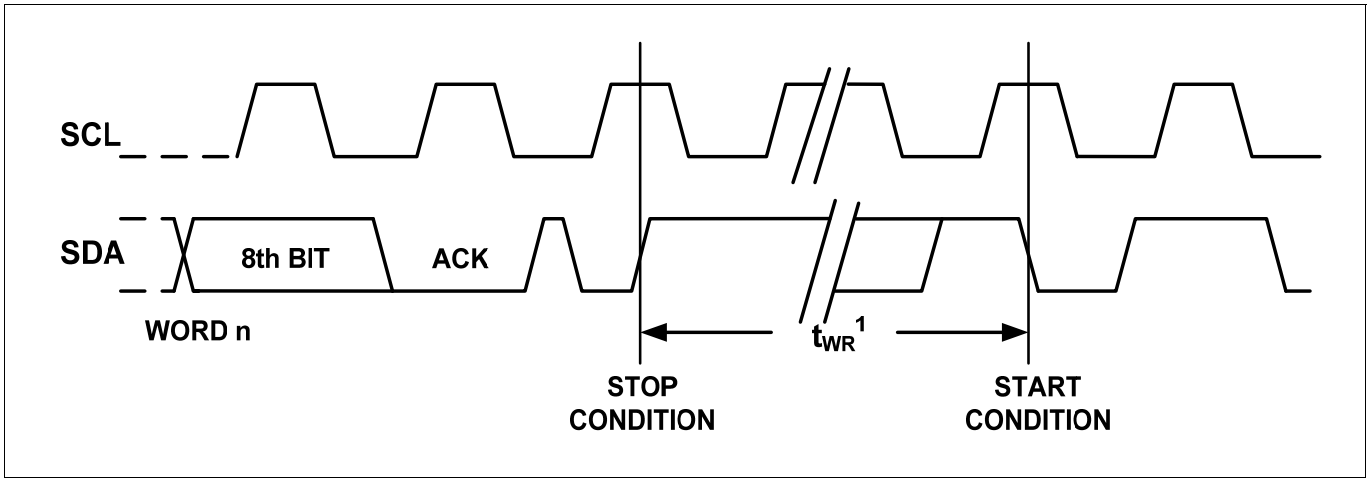





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## Write Cycle Timing

**Figure 3. SCL: Serial Clock, SDA: Serial Data I/O**




Note: 1. The write cycle time $t_{WR}$ is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

**Figure 4. Data Validity**

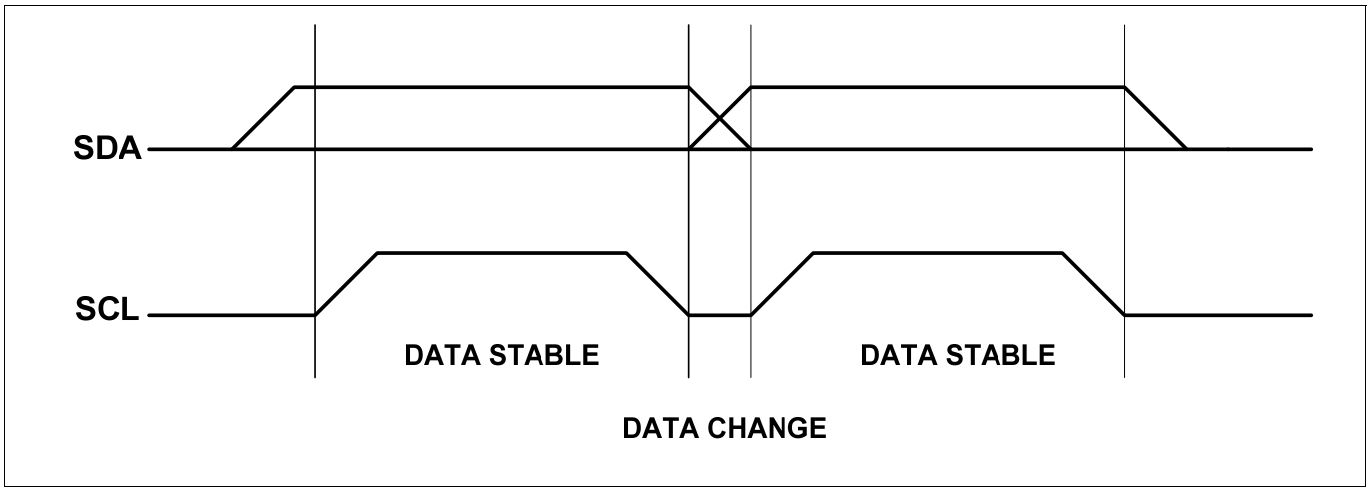
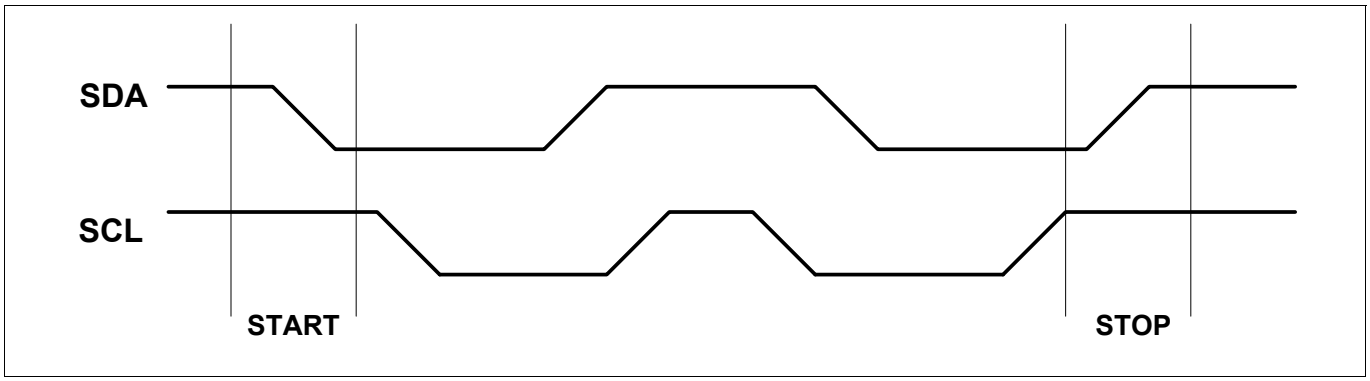


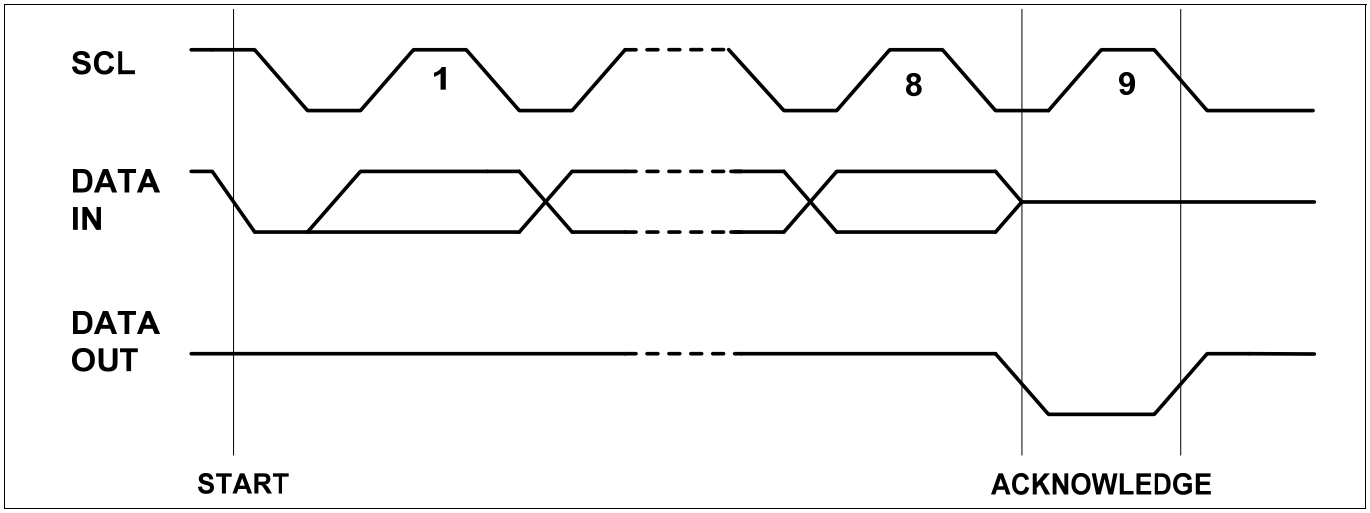

**Figure 5. Start and Stop Definition**






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**Figure 6. Output Acknowledge**




## Device Addressing

**Data Memory Access:** The 512K EEPROM device requires a 8-bit device address word following a start condition to enable the chip for a read or write operation (refer to Table 1).

The device address word consists of a mandatory '1010'(Ah) sequence for the first four most significant bits as shown in Table 1. This is common to all the EEPROM devices.

The 512K EEPROM uses the three device address bits A2, A1, A0 to allow as many as eight devices on the same bus. These bits must compare to their corresponding hard-wired input pins. The A2, A1 and A0 pins use an internal proprietary circuit that biases them to a logic low condition if the pins are allowed to float.

The Module package device address word also consists of a mandatory '1010'(Ah) sequence for the first four most significant bits. The next 3 bits are all zero.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

Upon a compare of the device address, the EEPROM will output a zero. If a compare is not made, the device will return to a standby state.

**Unique ID Access:** The FM24C512D utilizes a separate memory block containing a factory programmed 128-bit unique ID. Access to this memory location is obtained by beginning the device address word with a '1011'(Bh) sequence (refer to Table 1). The behavior of the next three bits (A2, A1 and A0) remains the same as during a standard memory addressing sequence.

The eighth bit of the device address needs be set to a one to read the Serial Number. Writing or altering the 128-bit unique ID is not possible.

For more details on accessing this special feature, See Read Operations on page 14.

**Security Sector Access:** The FM24C512D offers 128-byte Security Sector which can be written and (later) permanently locked in Read-only mode. Access to this memory location is obtained by beginning the device address word with a '1011'(Bh) sequence (refer to Table 1). The behavior of the next three bits (A2, A1 and A0) remains the same as during a standard memory addressing sequence.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

For more details on accessing this special feature, See Write Operations and Read Operations on page 13,14.

**NOISE PROTECTION:** Special internal circuitry placed on the SDA and SCL pins prevent small noise spikes from activating the device.

**DATA SECURITY:** The Device has a hardware data protection scheme that allows the user to write protect the entire memory when the WP pin is at $V_{CC}$.



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### Table 1-1. Device Address

| Access Area | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|---|
| Data Memory | 1 | 0 | 1 | 0 | A2 | A1 | A0 | R/W |
| Security Sector | 1 | 0 | 1 | 1 | A2 | A1 | A0 | R/W |
| Security Sector Lock Bit | 1 | 0 | 1 | 1 | A2 | A1 | A0 | R/W |
| Unique ID Number | 1 | 0 | 1 | 1 | A2 | A1 | A0 | 1 |
| | MSB | | | | | | | LSB |

### Table 1-2. First Word Address

| Access Area | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|---|
| Data Memory | A15 | A14 | A13 | A12 | A11 | A10 | A9 | A8 |
| Security Sector | x | x | x | x | x | 0 | 0 | x |
| Security Sector Lock Bit | x | x | x | x | x | 1 | 0 | X |
| Unique ID Number | x | x | x | x | x | x | 1 | x |
| | MSB | | | | | | | LSB |

**NOTE: x = Don`t care bit.**

### Table 1-3. Second Word Address

| Access Area | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|---|
| Data Memory | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
| Security Sector | x | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
| Security Sector Lock Bit | x | x | x | x | x | x | x | x |
| Unique ID Number | x | x | x | x | 0 | 0 | 0 | 0 |
| | MSB | | | | | | | LSB |

**NOTE: x = Don`t care bit.**



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# Write Operations

**BYTE WRITE:** A write operation requires two 8-bit data word address following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a zero and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a zero and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally-timed write cycle, $t_{WR,}$ to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (see **Figure 7** on page 15).

**PAGE WRITE:** The 512K EEPROM is capable of 128-byte page writes. A page write is initiated the same way as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to 127 more data words. The EEPROM will respond with a zero after each data word received. The microcontroller must terminate the page write sequence with a stop condition (see **Figure 8** on page 15).

The data word address lower seven bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than 128 data words are transmitted to the EEPROM, the data word address will “roll over” and previous data will be overwritten.

**ACKNOWLEDGE POLLING:** Once the internally timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a zero allowing the read or write sequence to continue.

**WRITE SECURITY SECTOR:** Write the Security Sector is similar to the page write but requires use of device address, and the special word address seen in Table 1 on page 12. The higher address bits ADDR<15:7> are don’t care except for address bits ADDR<10:9>，which must be equal to ‘00b’. Lower address bits ADDR<6:0> define the byte address inside the Security Sector (see **Figure 12** on page 16).

If the Security Sector is locked, the data bytes transferred during the Write Security Sector operation are not acknowledged (NoAck).

**LOCK SECURITY SECTOR:** Lock the Security Sector is similar to the byte write but requires use of device address, and special word address seen in Table 1 on page 12. The word address bits ADDR<10:9> must be ‘10b’, all other word address bits are don’t care. The data byte must be equal to the binary value xxxx xx1x, where x is don't care (see **Figure 14** on page 17).

If the Security Sector is locked, the data bytes transferred during the Lock Security Sector operation are not acknowledged (NoAck).



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# Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to one.

**CURRENT ADDRESS READ:** The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address "roll over" during read is from the last byte of the last memory page to the first byte of the first page. The address "roll over" during write is from the last byte of the current page to the first byte of the same page.

Once the device address with the read/write select bit set to one is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input zero but does generate a following stop condition (see **Figure 9** on page 15).

**RANDOM READ:** A random read requires a "dummy" byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a zero but does generate a following stop condition (see **Figure 10** on page 16).

**SEQUENTIAL READ:** Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will "roll over" and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a zero but does generate a following stop condition (see **Figure 11** on page 16)

**UNIQUE ID READ:** Reading the serial number is similar to the sequential read but requires use of the device address, a dummy write, and the use of specific word address seen in Table 1 on page 12. The higher address bits ADDR<15:4> are don't care except for address bits ADDR<10:9>，which must be equal to 'x1b'. Lower address bits ADDR<3:0> define the byte address inside the UID. If the application desires to read the first byte of the UID, the lower address bits ADDR<3:0> would need to be '0000b'.

When the end of the 128-bit UID number is reached (16 bytes of data), the data word address will roll-over back to the beginning of the 128-bit UID number. The Unique ID Read operation is terminated when the microcontroller does not respond with a zero (ACK) and instead issues a Stop condition (see **Figure 16** on page 18).

**READ SECURITY SECTOR**：Read the Security Sector is similar to the random read but requires use of device address, a dummy write, and the use of specific word address seen in Table 1 on page 12. The higher address bits ADDR<15:7> are don't care except for address bits ADDR<10:9>，which must be equal to '00b'. The lower address bits ADDR<6:0> define the byte address inside the Security Sector.

The internal byte address is automatically incremented to the next byte address after each byte of data is clocked out. When the last byte (7Fh) is reached, it will roll over to 00h, the first byte of the Security Sector, and continue to increment. (see **Figure 13** on page 17).

**READ LOCK STATUS**：There are two ways to check the lock status of the Security Sector.

1. The first way is initiated by a Security Sector Write, the EEPROM will acknowledge if the Security Sector is unlocked, while it will not acknowledge if the Security Sector is locked.

Once the acknowledge bit is read, it is recommended to generate a Start condition followed by a Stop condition, so that:

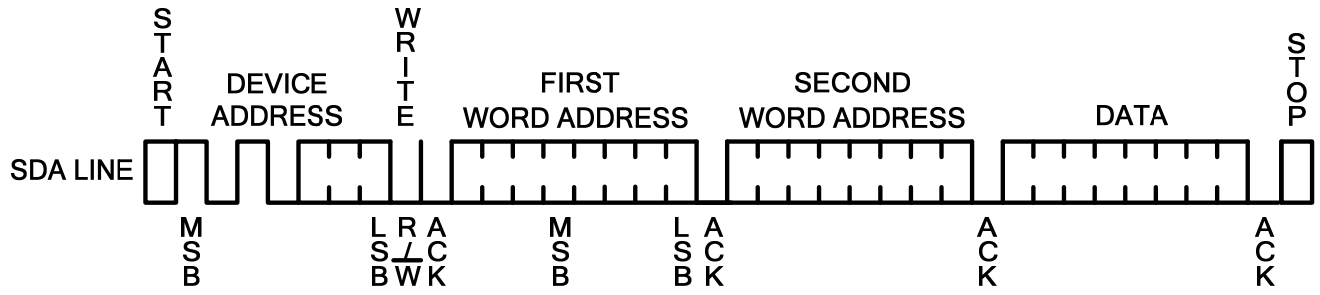
- Start: the truncated command is not executed because the Start condition resets the device internal logic
- Stop: the device is then set back into Standby mode by the Stop condition.

2. The second way is initiated by a Lock Status Read. Lock Status Read is similar to the random read but requires use of device address seen in Table 1 on page 12, a dummy write, and the use of specific word address. The address bits ADDR<10:9> must be '10b', all other address bits are Don't Care. The Lock bit is the BIT1 of the byte read on SDA. It is at "1" when the lock is active and at "0" when the lock is not active. The same data is shifted out repeatedly until the microcontroller does not respond with a zero but does generate a following stop condition (see **Figure 15** on page 18).



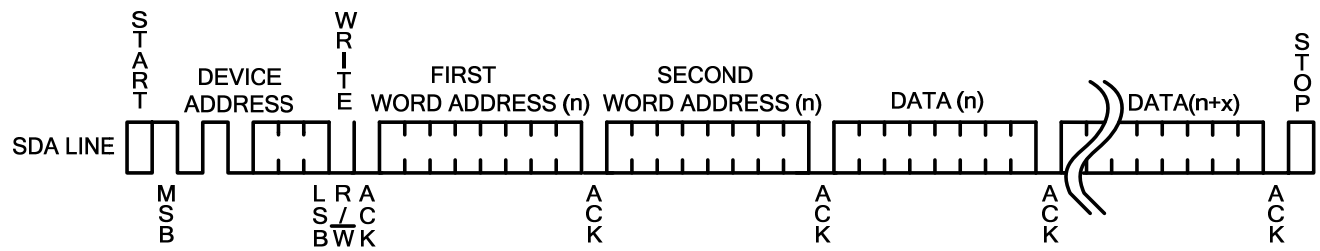
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**Figure 7. Byte Write**



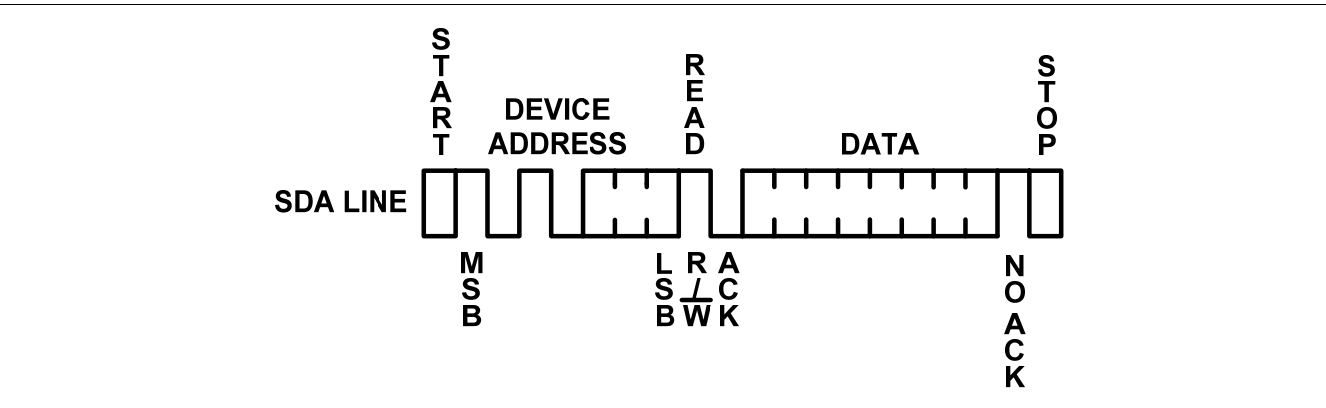

**Note: 1. * = *Don't CARE* bits**

**Figure 8. Page Write**




**Note: 1. * = *Don't CARE* bits**

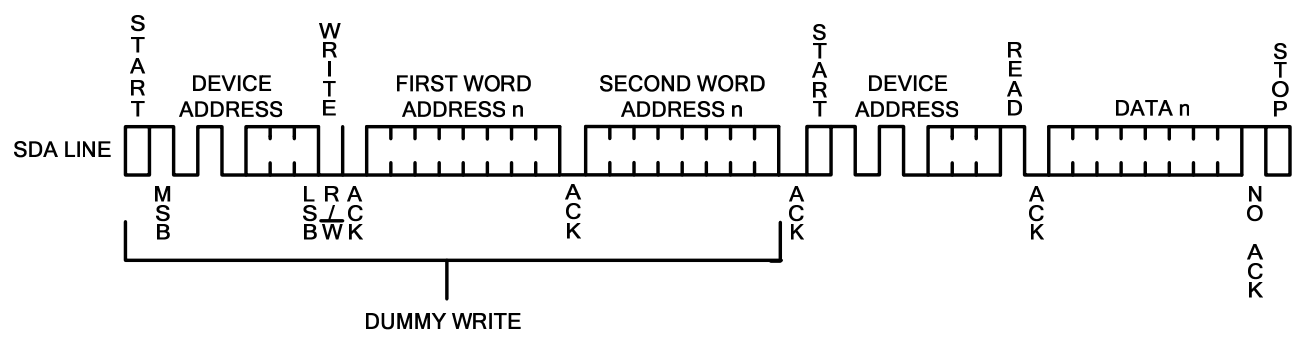
**Figure 9. Current Address Read**






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**Figure 10. Random Read**




Note: 1. * = *Don't CARE* bits.

**Figure 11. Sequential Read**

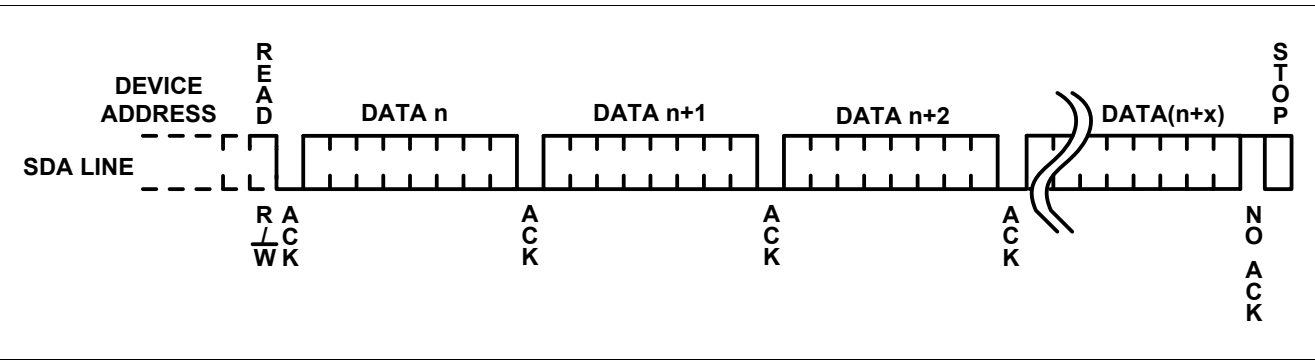
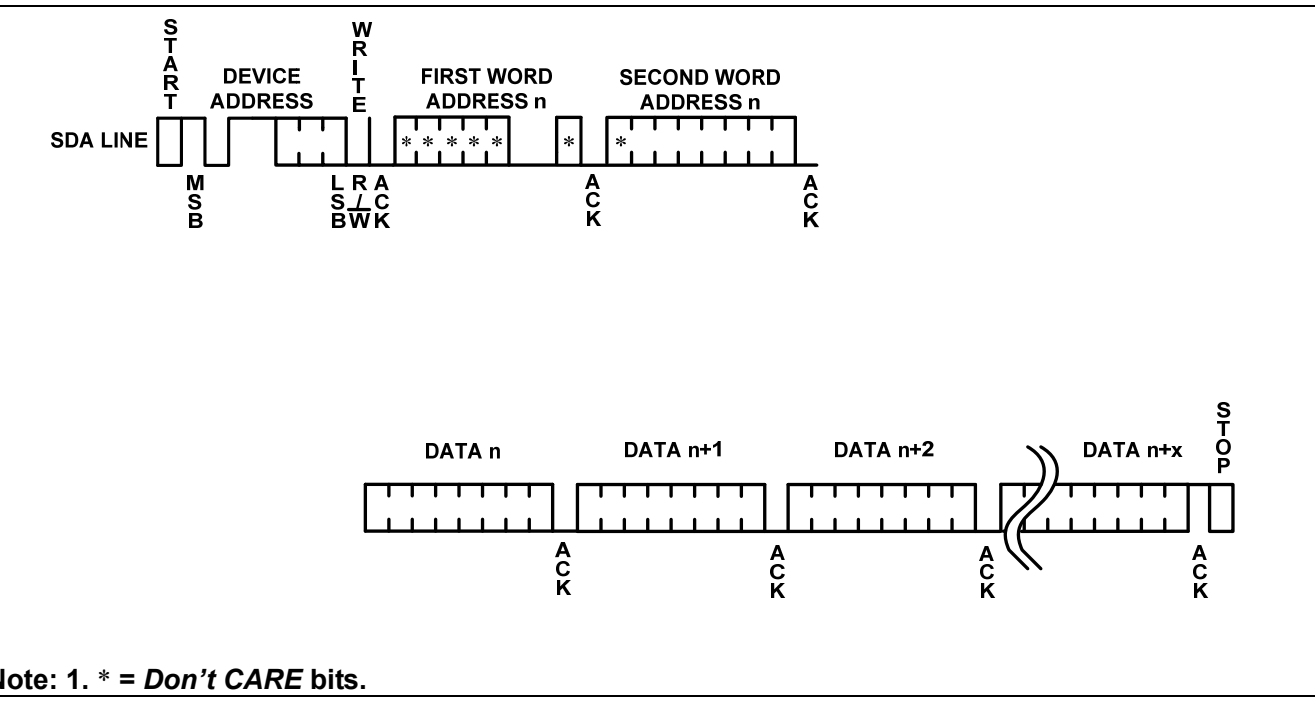



**Figure 12. Write Security Sector**

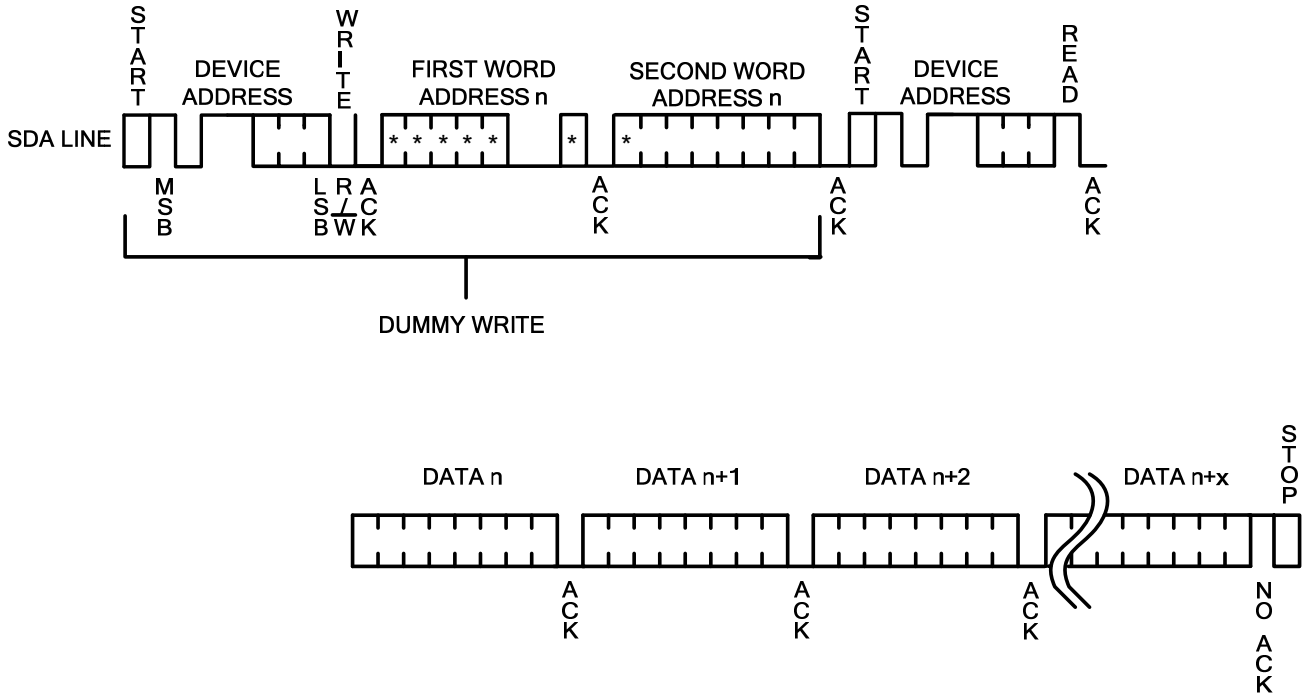



Note: 1. * = *Don't CARE* bits.



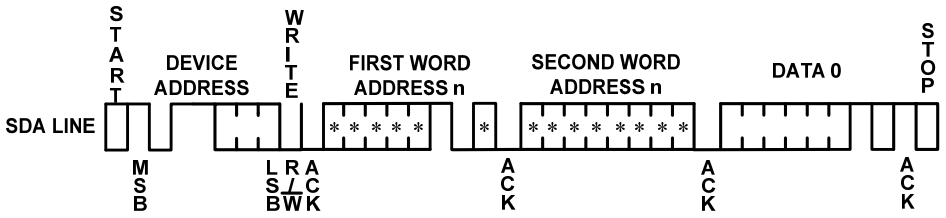
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**Figure 13. Read Security Sector**




**Note: 1. * = *Don't CARE* bits.**

**Figure 14. Lock Security Sector**

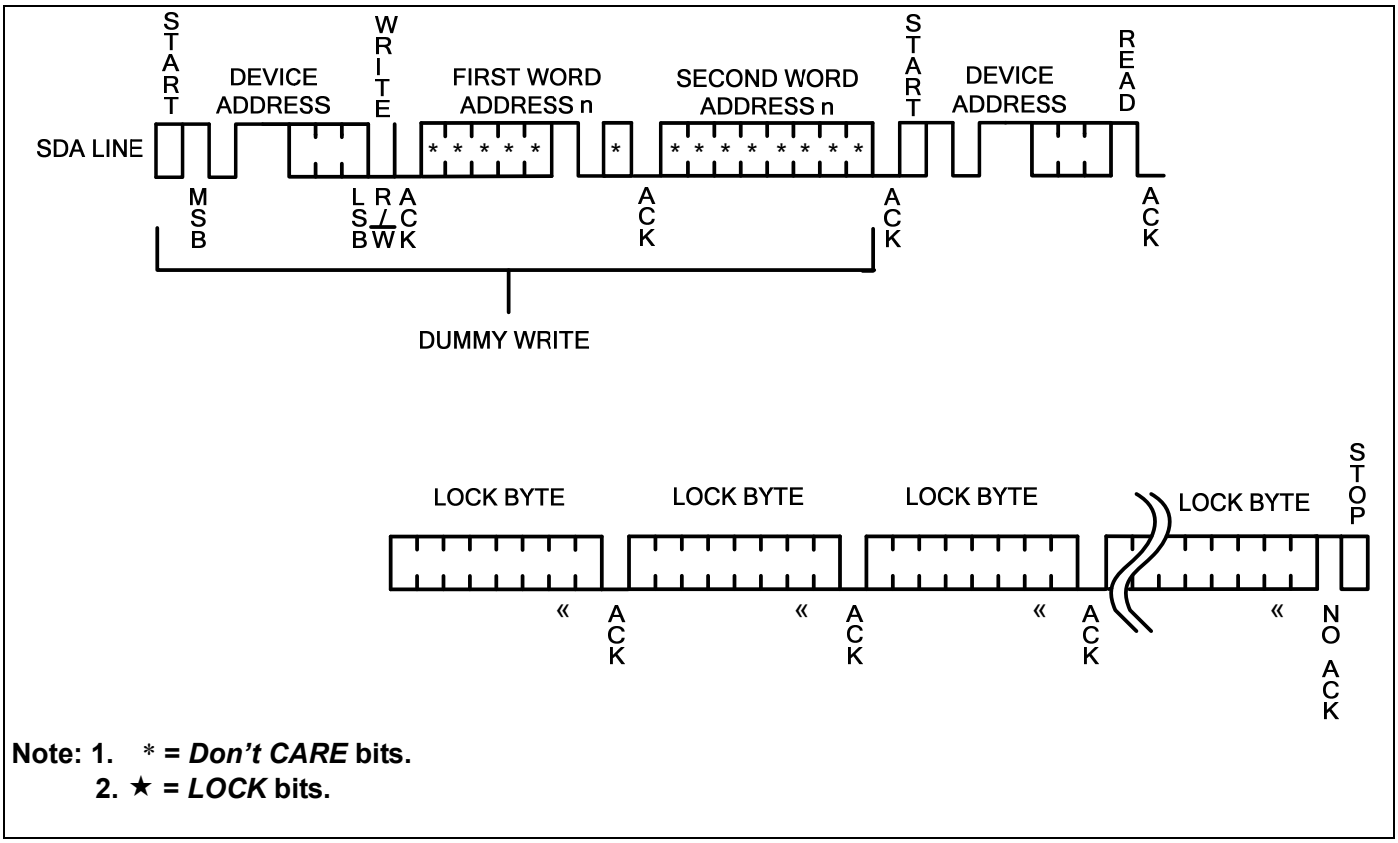



**Note: 1. * = *Don't CARE* bits.**



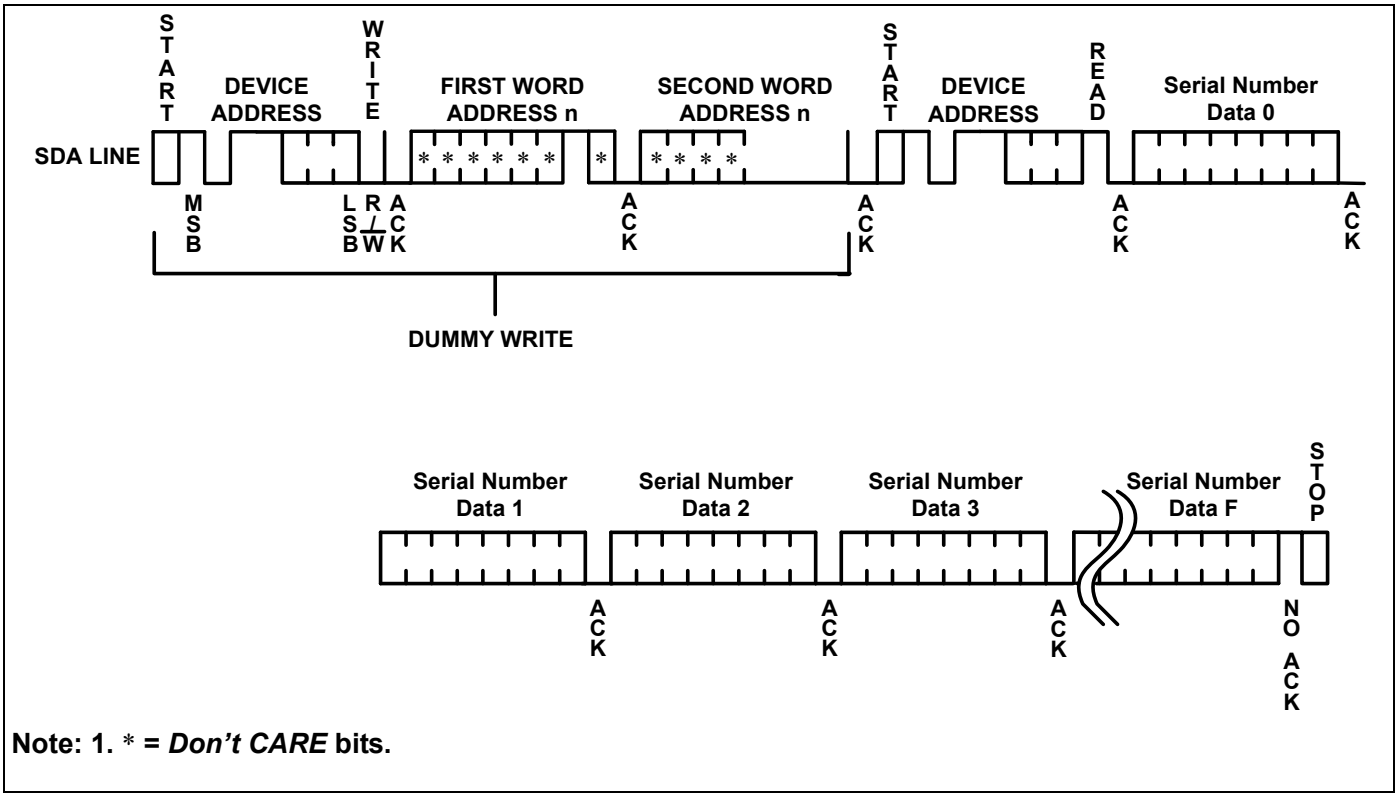
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**Figure 15. Read Lock Status**




**Note: 1. * = *Don't CARE* bits.**
**2. ★ = *LOCK* bits.**

**Figure 16. Read Unique ID**

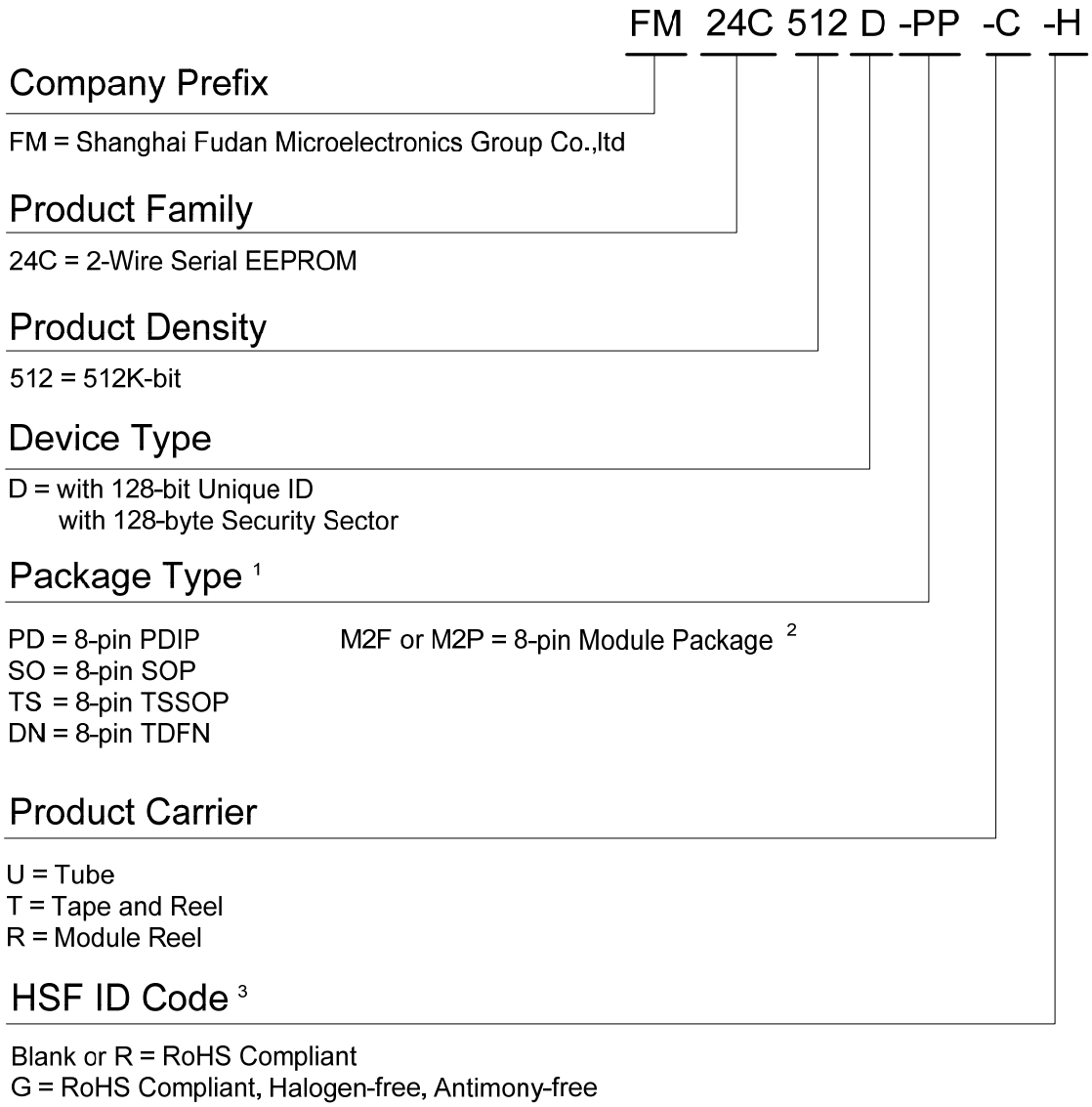



**Note: 1. * = *Don't CARE* bits.**



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# Ordering Information



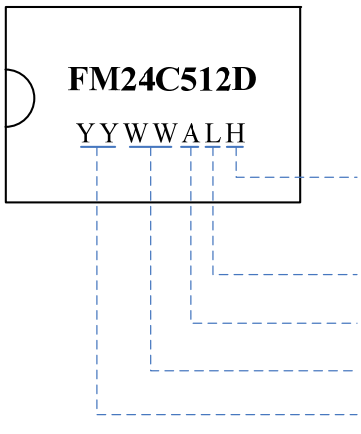

Note:
1. For SO, TS, DN package, MSL1 package are available, for detail please contact local sales office.
2. For the details of Module package please contact local sales office.
3. For PD package: R class only.
   For SO, TS and DN package: G class only.



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# Part Marking Scheme

## PDIP8




**HSF ID Code**
R = RoHS Compliant

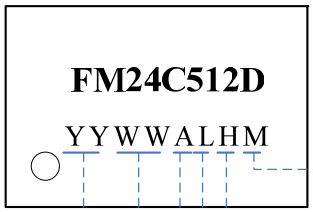
**Lot Number（just with 0~9、A~Z）**

**Assembly's Code**

**Work week during which the products was molded (eg..week 12)**

**The last two digits of the year In which the products was seal / molded.**

## SOP8




**Moisture Sensitivity Level**
1 = MSL1
Blank=MSL3

**HSF ID Code**
R = RoHS Compliant
G = RoHS Compliant, Halogen-free, Antimony-free

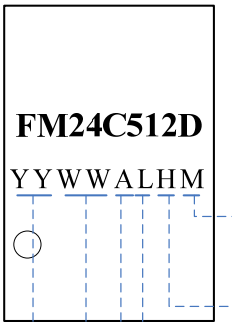
**Lot Number（just with 0~9、A~Z）**

**Assembly's Code**

**Work week during which the products was molded (eg..week 12)**

**The last two digits of the year In which the products was seal / molded.**

## TSSOP8




**Moisture Sensitivity Level**
1=MSL1
Blank=MSL3

**HSF ID Code**
R = RoHS Compliant
G = RoHS Compliant, Halogen-free, Antimony-free

**Lot Number（just with 0~9、A~Z）**

**Assembly's Code**

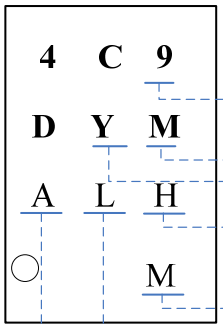
**Work week during which the products was molded (eg..week 12)**

**The last two digits of the year In which the products was seal / molded.**



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## TDFN8




**Product Density Code**

**The month (hexadecimal digit) in which the products was molded.**
**The last one digit of the year In which the products was seal / molded.**

**HSF ID Code**
G = RoHS Compliant, Halogen-free, Antimony-free

**Moisture Sensitivity Level**
1=MSL1

**Lot Number（just with 0~9、A~Z）**

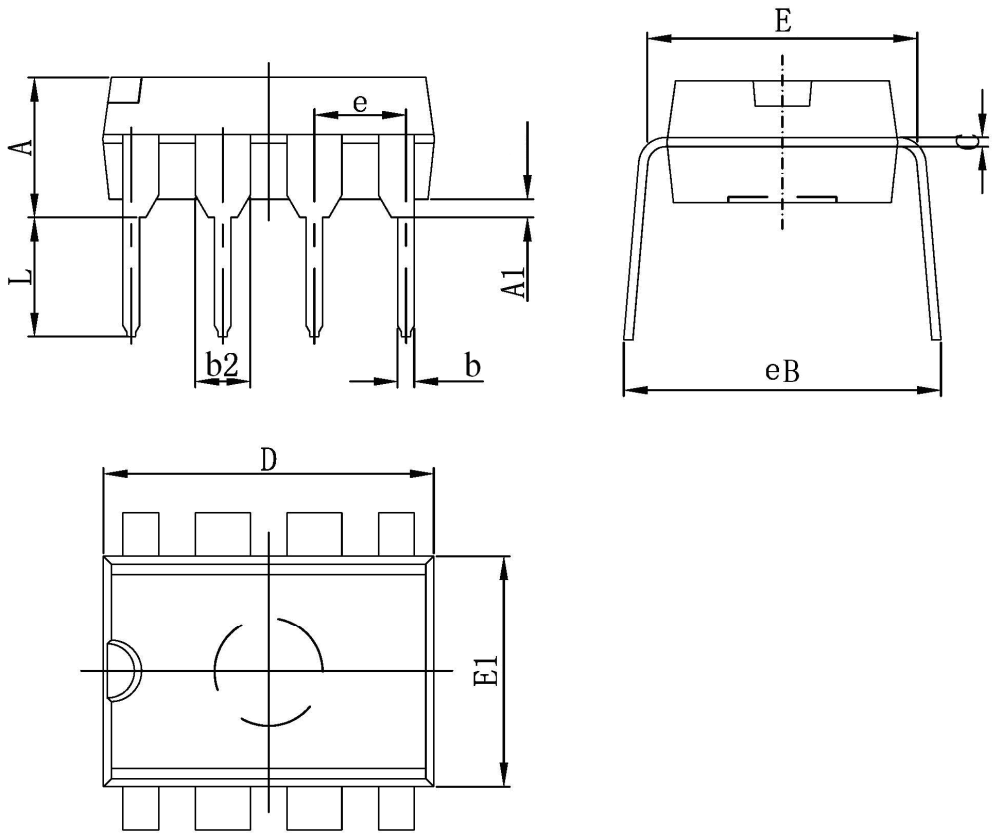
**Assembly’s Code**



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# Packaging Information

## PDIP 8




| Symbol | MIN | MAX |
|---|---|---|
| A | --- | 5.000 |
| A1 | 0.380 | --- |
| b | 0.380 | 0.570 |
| b2 | 1.300 | 1.700 |
| C | 0.200 | 0.360 |
| D | 9.000 | 10.000 |
| E1 | 6.100 | 7.000 |
| E | 7.320 | 8.250 |
| e | 2.540(BSC) | |
| L | 2.920 | 3.810 |
| eB | --- | 10.900 |

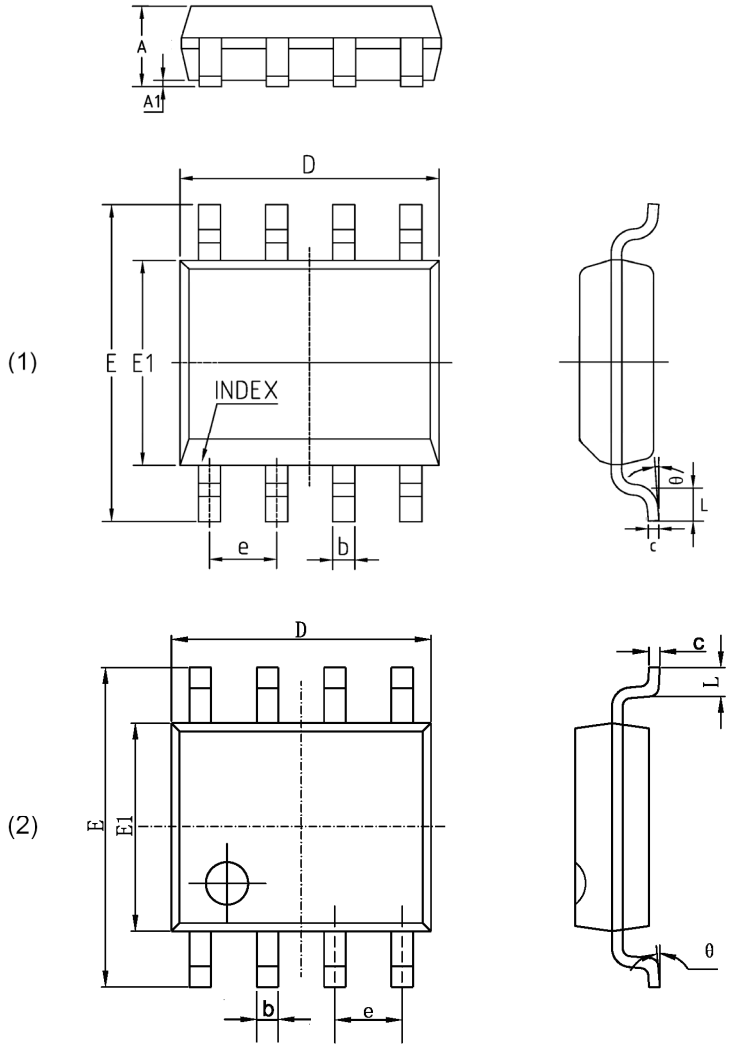
**NOTE:**

**1. Dimensions are in Millimeters.**



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# SOP 8




| Symbol | MIN | MAX |
|---|---|---|
| A | 1.350 | 1.750 |
| A1 | 0.050 | 0.250 |
| b | 0.330 | 0.510 |
| c | 0.150 | 0.250 |
| D | 4.700 | 5.150 |
| E1 | 3.800 | 4.000 |
| E | 5.800 | 6.200 |
| e | 1.270(BSC) | |
| L | 0.400 | 1.270 |
| θ | 0° | 8° |

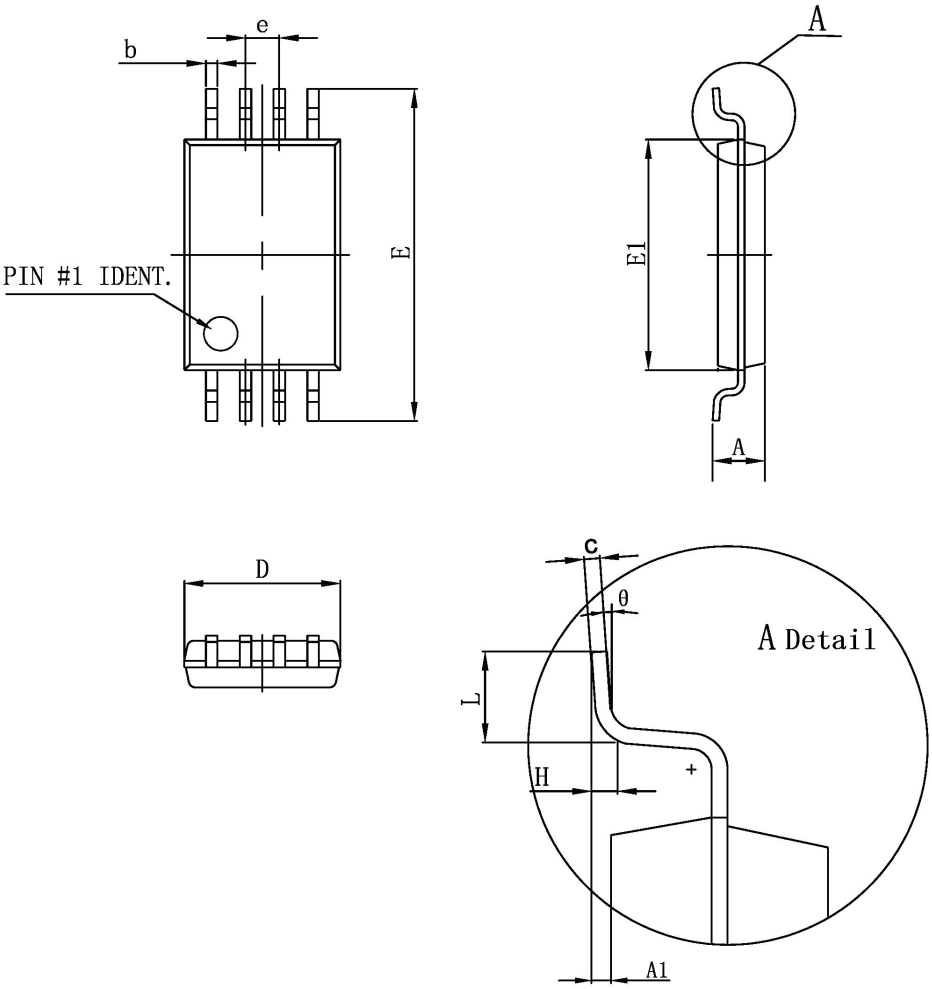
**NOTE:**

**1. Dimensions are in Millimeters.**



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# TSSOP8




| Symbol | MIN | MAX |
|---|---|---|
| D | 2.900 | 3.100 |
| E1 | 4.300 | 4.500 |
| b | 0.190 | 0.300 |
| c | 0.090 | 0.200 |
| E | 6.250 | 6.550 |
| A | | 1.200 |
| A1 | 0.050 | 0.150 |
| e | 0.650 (BSC) | |
| L | 0.450 | 0.750 |
| θ | 0° | 8° |

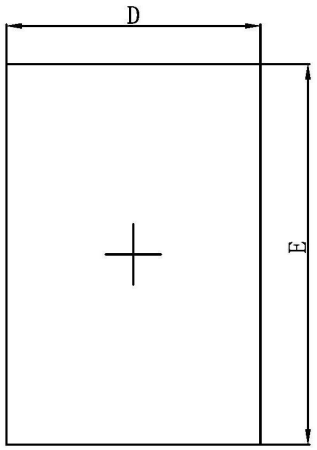
**NOTE:**

1. **Dimensions are in Millimeters.**

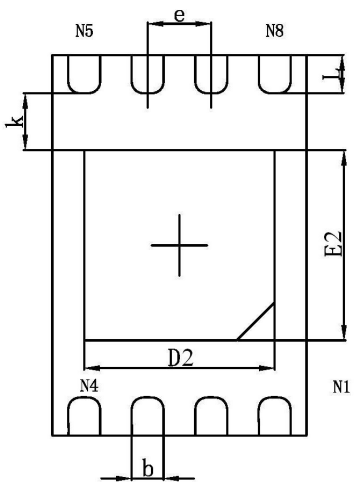


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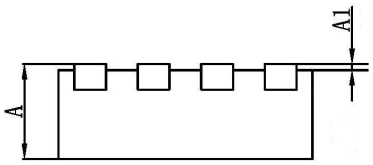
# TDFN8




**Top View**




**Bottom View**




**Side View**

| Symbol | MIN | MAX |
|---|---|---|
| A | 0.700 | 0.800 |
| A1 | 0.000 | 0.050 |
| D | 1.900 | 2.100 |
| E | 2.900 | 3.100 |
| D2 | 1.400 | 1.600 |
| E2 | 1.400 | 1.600 |
| k | 0.200(MIN) | |
| b | 0.200 | 0.300 |
| e | 0.500(TYP) | |
| L | 0.200 | 0.400 |

**NOTE:**

1. **Dimensions are in Millimeters.**



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# Revision History

| Version | Publication date | Pages | Paragraph or Illustration | Revise Description |
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| Preliminary | Nov 2013 | 27 | | Initial document Release. |
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| | | | | |



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