FORESEE eMMC Datasheet

E-01132

FEMDNN064G-C9A61

FEMDNN128G-C9A61

FEMDNN256G-C9A61

Version 0.1

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Key Features

eMMC 5.1 Specification Compatibility

- JEDEC Standard No. JESD84-B51A
- Backward compatible with eMMC4.41/4.5/5.0

Operating Voltage Range

- V_{CC} (NAND): 2.7 ~ 3.6V
- V_{CCQ} (Controller): 1.7 ~ 1.95V / 2.7 ~ 3.6V

Bus Mode

- Advanced 12-signal interfaces, including 8-line DATA, CLK, CMD, RSTN, DS
- Data bus width: 1 bit (default), 4 bits, 8 bits
- Data transfer rate: up to 400MB/s (HS400)
- eMMC I/F boot frequency: 0~52MHz
- eMMC I/F clock frequency: 0~200MHz

Temperature Range

- Operation: -25°C ~ +85°C
- Storage without operation: -40°C ~ +85°C

Supported Features

- HS400, HS200
- Partitioning, RPMB
- Boot feature, boot partition
- HW Reset / SW Reset
- Sleep Mode
- Discard, Trim, Erase
- High-Priority Interrupt (HPI)
- Field firmware update (FFU)
- Sudden-Power-Loss safeguard
- Hardware ECC engine
- Unique firmware backup mechanism
- Global-wear-leveling

Vendor Function

- Product Health Information
- Initial Data Acceleration (IDA)

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1 Introduction

1.1 General Description

FORESEE eMMC provides an embedded storage solution with NAND flash and eMMC controller in BGA package. The controller could manage the interface protocols, wear-leveling, bad blocks and ECC.

FORESEE eMMC has high performance at a competitive cost, high quality and low power consumption, and is compatible with the JEDEC standard of eMMC 5.1 specifications.

1.2 Part Number Decoder

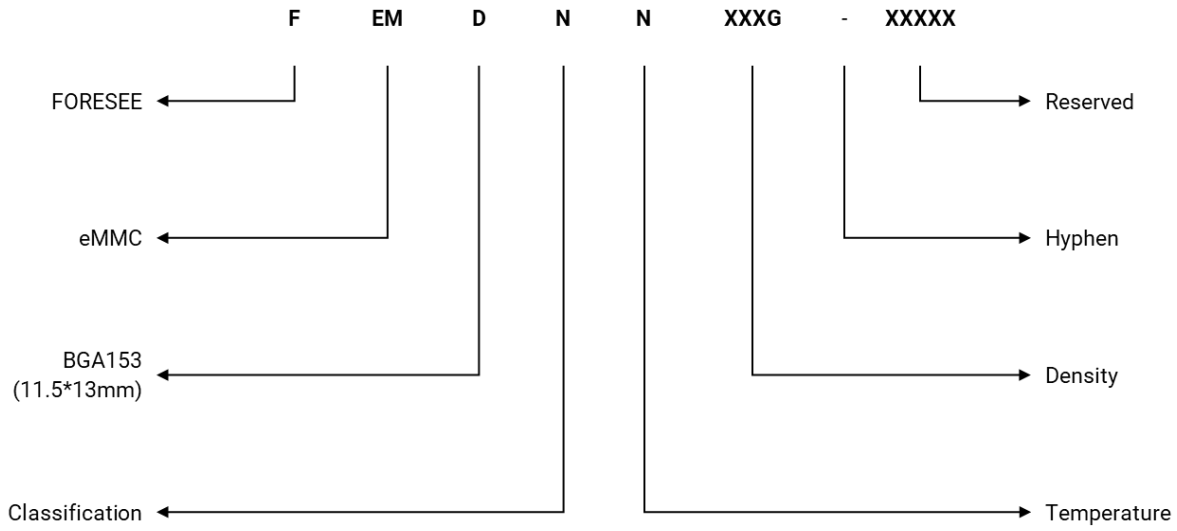


Figure 1 Part Number Decoder

1.3 Ordering Information

Table 1 Product Ordering Information

Part Number	Capacity	User Area	Package Size (mm)	Package Type	Shipping
FEMDNN064G-C9A61	64GB	58.28GB	11.5×13.0×1.0	153 FBGA	Tray
FEMDNN128G-C9A61	128GB	116.48GB	11.5×13.0×1.0	153 FBGA	Tray
FEMDNN256G-C9A61	256GB	232.96GB	11.5×13.0×1.0	153 FBGA	Tray

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2 Product Specifications

2.1 Temperature Specifications

Table 2 Temperature Specifications

Part Number	Temperature (Tc)	
FEMDNN064G-C9A61	Operation	-25 ~ +85°C
	Storage	-40~ +85°C
FEMDNN128G-C9A61	Operation	-25 ~ +85°C
	Storage	-40~ +85°C
FEMDNN256G-C9A61	Operation	-25 ~ +85°C
	Storage	-40~ +85°C

2.2 Power Consumption

2.2.1 Active Power Consumption During Operation

Table 3 Active Power Consumption during Operation

Part Number	I_{CC} (mA)	I_{CCQ} (mA)
FEMDNN064G-C9A61	60	100
FEMDNN128G-C9A61	60	100
FEMDNN256G-C9A61	65	105

Notes:
1. Power measurement conditions: Bus configuration =x8 @200MHz DDR, room temperature.
2. V_{CC} = 3.3V & V_{CCQ} = 1.8V.

2.2.2 Low Power Mode (Stand-by)

Table 4 Low Power Mode (Stand-by)

Part Number	I_{CC} (μA)	I_{CCQ} (μA)
FEMDNN064G-C9A61	50	500
FEMDNN128G-C9A61	50	500
FEMDNN256G-C9A61	50	500

Notes:
1. Power measurement conditions: Bus configuration =x8 @200MHz DDR, room temperature.
2. Standby: Entry of the Automatic Sleep Mode (See 3.6).

2.2.3 Low Power Mode (Sleep)

Table 5 Low Power Mode (Sleep)

Part Number	I_{CC} (μA)	I_{CCQ} (μA)
FEMDNN064G-C9A61	0	500
FEMDNN128G-C9A61	0	500
FEMDNN256G-C9A61	0	500

Notes:
1. Power measurement conditions: Bus configuration =x8 @200MHz DDR, room temperature.
2. Sleep: NAND Flash V_{CC} power supply is switched off (with Controller V_{CCQ} on).

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2.3 Performance

Table 6 Write/Read Performance

Part Number	Write	Read
FEMDNN064G-C9A61	Up to 300MB/s	Up to 320MB/s
FEMDNN128G-C9A61	Up to 300MB/s	Up to 320MB/s
FEMDNN256G-C9A61	Up to 300MB/s	Up to 320MB/s

Note:
1. Test Condition: Bus width x8, @200MHz DDR, room temperature,chunk size=1MB, CMDQ mode,QD=8.
2. Test platform: 3720 test board (HS400 ,without file system overhead).
3. The performance may vary depending on the condition and environment.

2.4 Ball Pin Configuration

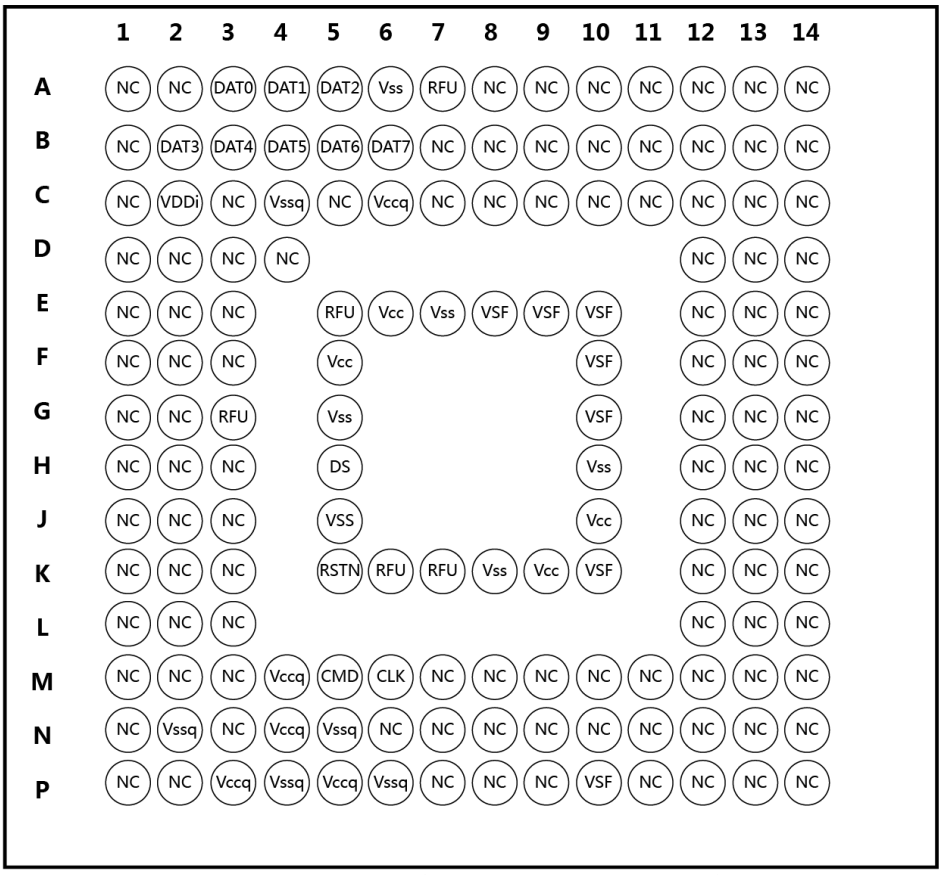


Figure 2 Ball Array (Top View Through Package)

Table 7 Ball Array Description

Pin Name	Description
DAT0	These are bidirectional data signals. The DAT signals operate in the push-pull mode. Only the device or the host is driving these signals at a time. By default, after power-up or reset, only DAT0 is used for data transfer. A wider data bus can be configured for data transfer, using either DAT0-DAT3 or DAT0-DAT7, by the eMMC host controller. The eMMC device includes internal pull-ups for data lines DAT1-DAT7. Immediately after entering the 4-bit mode, the device disconnects the internal pull-ups of lines DAT1, DAT2, and DAT3. Correspondingly, immediately after entering the 8-bit mode, the device disconnects the internal pull-ups of lines DAT1–DAT7.
DAT1	
DAT2	
DAT3	
DAT4	
DAT5	

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Pin Name	Description
DAT6	
DAT7	
RSTN	Hardware Reset Input.
V_{CCQ}	V_{CCQ} is the power supply line for host interface. It has two power modes: The high power mode is 2.7V~3.6V; the lower power mode is 1.7V~1.95V.
V_{CC}	V_{CC} is the power supply line for internal flash memory, and its power voltage range is 2.7V~3.6V.
VDDi	VDDi is the internal power node, not the power supply. Connect 1μF capacitor VDDi to the ground.
CMD	Command signal. This signal is a bidirectional command channel used for device initialization and command transfer. Commands are sent from the host to the device, and responses are sent from the device to the host. The CMD signal has 2 operation modes: open-drain for initialization, and push-pull for command transfer.
DS	Data Strobe signal. Newly assigned pin for the HS400 mode. Data Strobe is generated from eMMC to the host. In the HS400 mode, read data and CRC response are synchronized with Data Strobe.
CLK	Clock signal. Each cycle of this signal directs a one-bit transfer on the command and either a one-bit (1x) or two-bit (2x) transfer on all the data lines.
RFU	Reserved for future use.
VSF	Vendor specific function.
NC	Not connected.
V_{SS} /V_{SSQ}	Ground. V_{SS} and V_{SSQ} are internally connected.

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2.5 Package Dimension

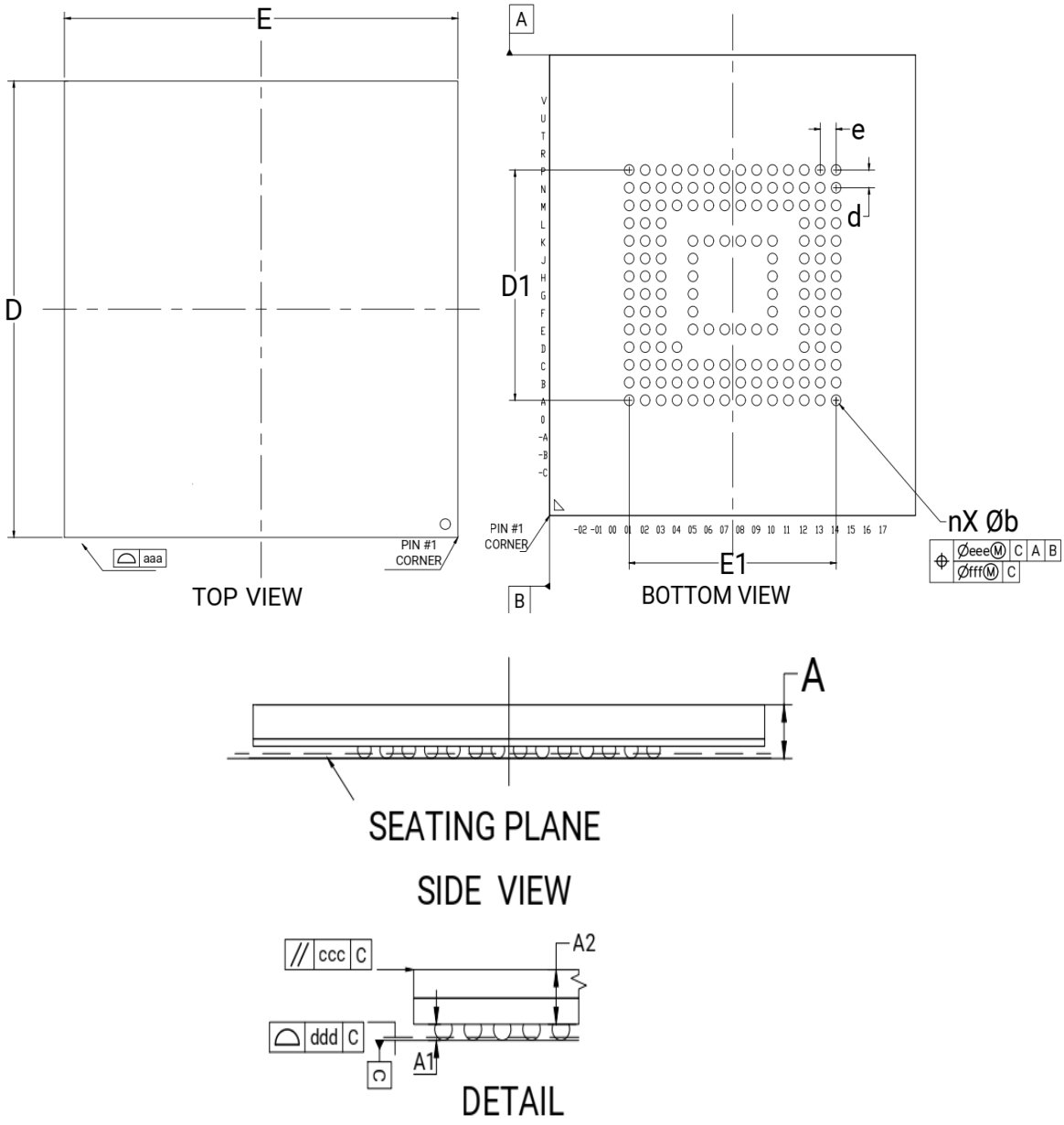


Figure 3 Package Dimension

Table 8 11.5mm x 13.0mm x 1.0mm Package Dimension

Symbol	Dimension in mm			Dimension in inch		
	Min	Normal	Max	Min	Normal	Max
A(1.0mm)	0.86	0.93	1.00	0.034	0.037	0.039
A1	0.18	0.21	0.24	0.007	0.008	0.009
A2(1.0mm)	0.67	0.72	0.77	0.026	0.028	0.030
Φb	0.25	0.30	0.35	0.010	0.012	0.014
d	0.50			0.020		
e	0.50			0.020		

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Symbol	Dimension in mm			Dimension in inch		
	Min	Normal	Max	Min	Normal	Max
n	153					
D	12.93	13.00	13.05	0.509	0.512	0.514
E	11.43	11.50	11.55	0.450	0.453	0.455
D1	6.40	6.50	6.60	0.252	0.256	0.260
E1	6.40	6.50	6.60	0.252	0.256	0.260
aaa	0.10			0.004		
ccc	0.10			0.004		
ddd	0.08			0.003		
eee	0.15			0.006		
fff	0.05			0.002		
JEDEC	MO-276(REF)					

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3 Technical Notes

3.1 System Architecture

The eMMC can be operated in 1-bit, 4-bit, or 8-bit mode. NAND flash memory is managed by a controller inside. The controller has ECC, wear leveling and bad block management functions. All flash management hassles are invisible to the host.

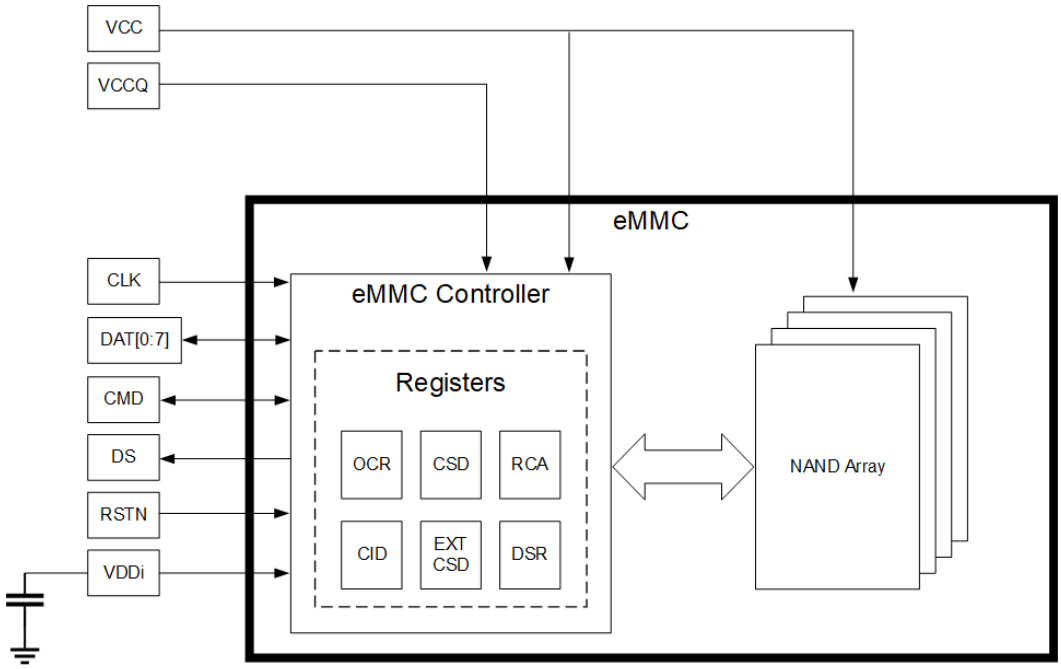


Figure 4 eMMC System Architecture

3.2 Functional Description

FORESEE eMMC with the powerful L2P (Logical to Physical) NAND Flash management algorithm provides the following unique functions.

3.2.1 Host Not Required to Operate NAND Flash

As the eMMC controller manages flash operation, such as data storage and retrieval, defect diagnostics and handling, and power management, the host is not required to handle NAND flash data.

3.2.2 Internal ECC to Correct Defects in NAND Flash

The hardware error correction code (ECC) function can prevent data corruption.

3.2.3 Sudden-Power-Loss Safeguard

To prevent data loss, a mechanism named Sudden-Power-Loss Safeguard is introduced in the eMMC. In case of sudden power failure, the eMMC could work properly after power cycling.

3.2.4 Global-wear-leveling

To achieve the best stability and device endurance, this eMMC is equipped with the Global Wear Leveling

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algorithm. It ensures that not only the normal area, but also the frequently accessed area, such as FAT, would be programmed and erased evenly.

3.2.5 Cache

The eMMC has enhanced the data writing performance with Cache, which also highly increases the endurance and reliability of the product.

3.3 Interface Timing Mode

FORESEE eMMC supports a high-speed DDR interface timing mode up to 400MB/s at 200MHz with 1.8V I/O supply.

Table 9 Device Type Value (EXT_CSD register: DEVICE_TYPE [196])

Bit	Device Type	Supported or Not
7	HS400 Dual Data Rate eMMC at 200 MHz – 1.2 V I/O	Not supported
6	HS400 Dual Data Rate eMMC at 200 MHz – 1.8 V I/O	Supported
5	HS200 Single Data Rate eMMC at 200 MHz - 1.2 V I/O	Not supported
4	HS200 Single Data Rate eMMC at 200 MHz - 1.8 V I/O	Supported
3	High-Speed Dual Data Rate eMMC at 52 MHz - 1.2 V I/O	Not supported
2	High-Speed Dual Data Rate eMMC at 52 MHz - 1.8 V or 3.3 V I/O	Supported
1	High-Speed eMMC at 52 MHz - at rated device voltage(s)	Supported
0	High-Speed eMMC at 26 MHz - at rated device voltage(s)	Supported

3.4 Partition Management

The embedded device also offers the possibility to configure the host's additionally split local memory partitions with independent addressable space, starting from logical address 0x00000000 for different usage models. The default size of each Boot Area Partition is 4096 KB. The size of a Boot Area Partition is calculated as (128KB × BOOT_SIZE_MULT). The sizes of Boot Area Partitions 1 and 2 cannot be set independently, and should be set to the same value. These two Boot Area Partitions are enhanced partitions. Therefore, memory block area can be classified as follows:

- Boot partitions are default.
- The host is free to configure one segment in the User Data Area as enhanced storage media, and to specify its starting location and size in terms of Write Protect Groups. The attributes of this enhanced User Data Area can be programmed only once during the device life-cycle (one-time programmable).
- Up to four General Purpose Area Partitions can be configured to store user data or sensitive data, or for other host usage models. The size of these partitions is a multiple of the write protect group. Size and attributes can be programmed once in device life-cycle (one-time programmable). Each of the General Purpose Area Partitions can be configured with enhanced technological features.

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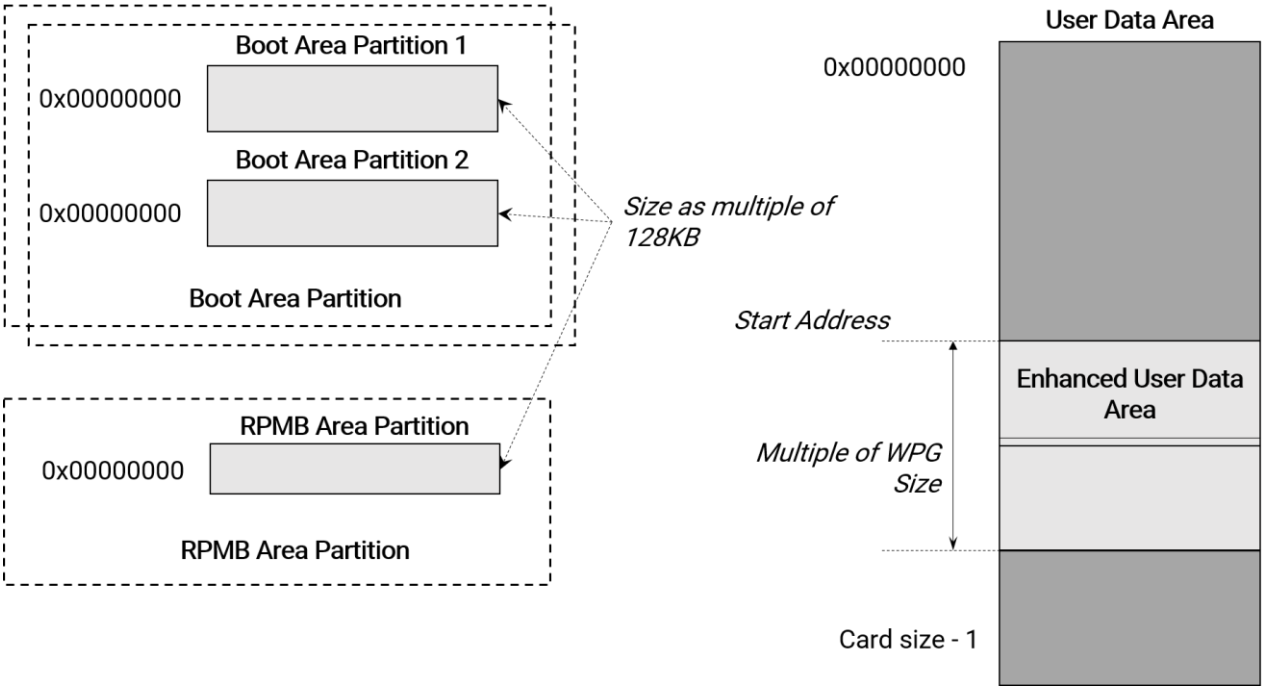


Figure 5 Partitions and User Data Area Configuration

In the boot operation mode, the master can read boot data from the slave (device) by keeping the CMD line low or sending CMD0 with argument + 0xFFFFFFFA, before issuing CMD1. The data can be read from either the boot area or the user area depending on register setting.

Table 10 Boot ACK, Boot Data and Initialization Time

Timing Factor	Value
Boot ACK Time	< 50 ms
Boot Data Time	< 1 s
Initialization Time	< 1 s

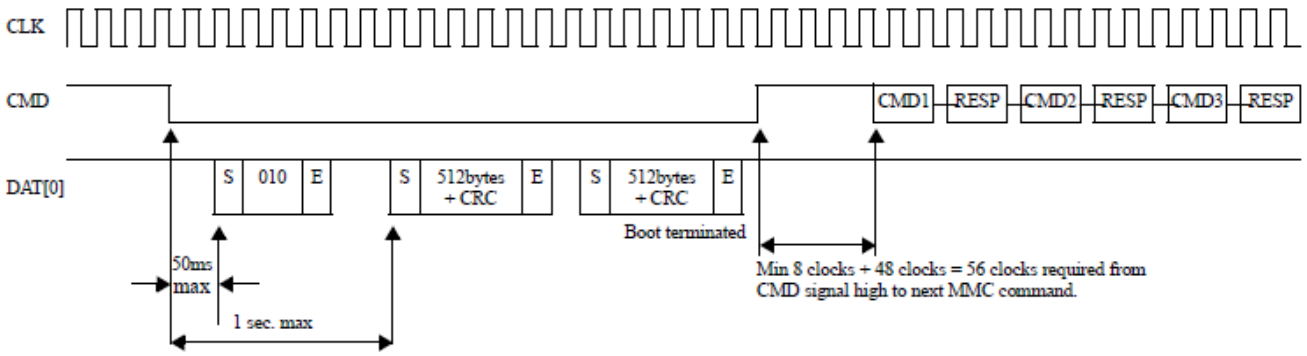


Figure 6 State Diagram (Boot Mode)

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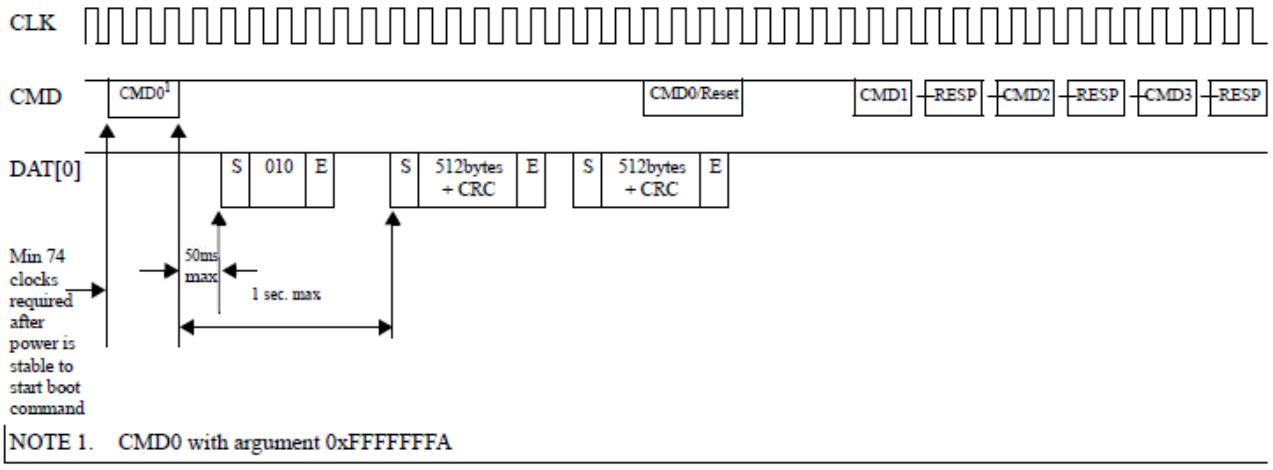


Figure 7 State Diagram (Alternative Boot Mode)

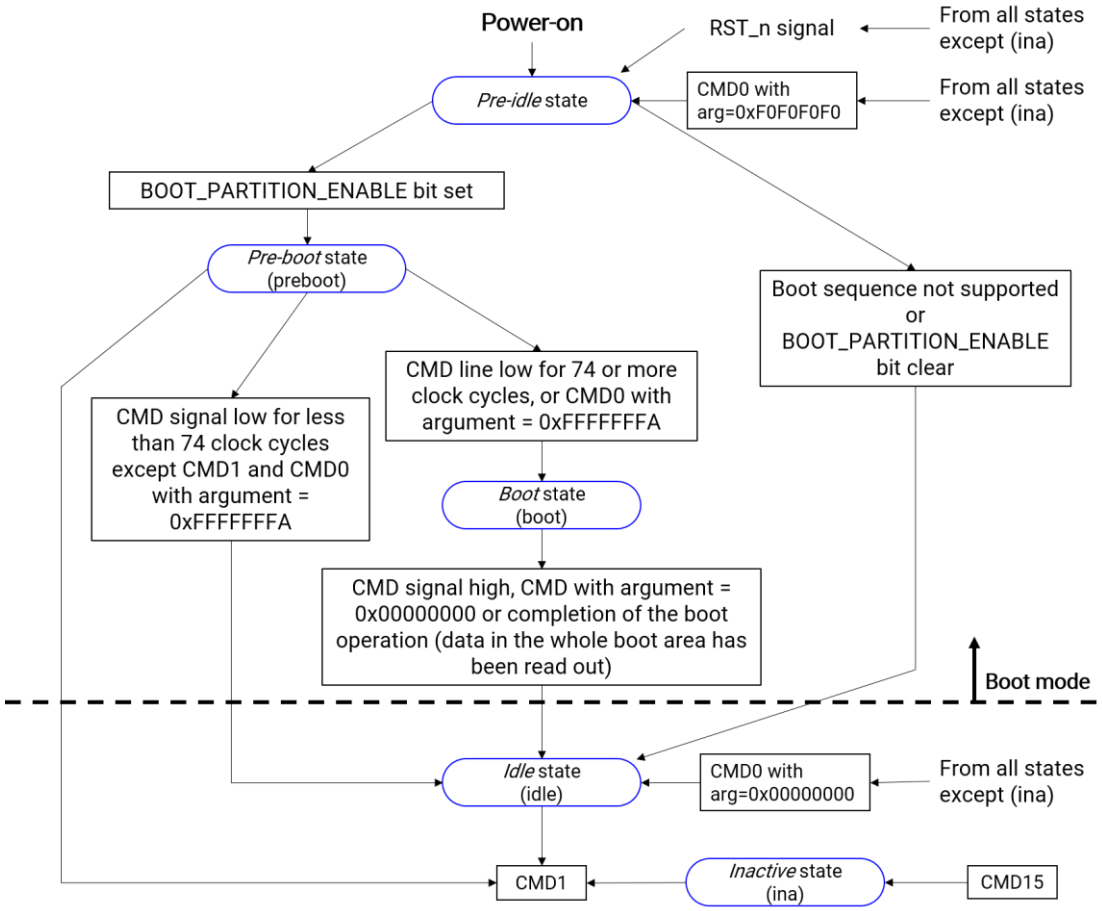


Figure 8 State Diagram (Boot Mode)

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3.5 Partition Configuration

Table 11 Partition Configuration

Part Number	Area/Partition	Size (GB)	Size (MB)	Size (Sector)	Size (Byte)	Size (Hex, Byte)
FEMDNN064G-C9A61	User	58.28	59680	122224640	62579015680	E92000000
	Boot Partition 1	-	4	8192	4194304	400000
	Boot Partition 2	-	4	8192	4194304	400000
	RPMB	-	16	32768	16777216	1000000
FEMDNN128G-C9A61	User	116.48	119276	244277248	125069950976	1d1ec00000
	Boot Partition 1	-	4	8192	4194304	400000
	Boot Partition 2	-	4	8192	4194304	400000
	RPMB	-	16	32768	16777216	1000000
FEMDNN256G-C9A61	User	232.96	238552	488554496	250139901952	3A3D800000
	Boot Partition 1	-	4	8192	4194304	400000
	Boot Partition 2	-	4	8192	4194304	400000
	RPMB	-	16	32768	16777216	1000000

3.6 Sleep (CMD5)

The eMMC can be switched between a sleep state and a standby state by SLEEP/AWAKE (CMD5). In the sleep state, the power consumption of the memory device is minimized. The memory device reacts only to the commands RESET (CMD0 with argument of either 0x00000000 or 0xF0F0F0F0 or H/W reset) and SLEEP/AWAKE (CMD5). All the other commands are ignored by the memory device. The timeout for state transitions between the standby state and the sleep state is defined in the EXT_CSD register S_A_TIMEOUT. The maximum current consumptions during the sleep state are defined in the EXT_CSD registers S_A_VCC and S_A_VCCQ. Sleep command: The bit 15 is set to 1 in SLEEP/AWAKE (CMD5) argument. Awake command: The bit 15 is set to 0 in SLEEP/AWAKE (CMD5) argument.

3.7 High-speed Mode Selection

After the host verifies that the card complies with the version 4.0, or higher of JEDEC standard, it must enable the high-speed mode timing in the card before changing the clock frequency to a frequency higher than 20MHz. To switch to a higher clock frequency, the host has to enable the high-speed interface timing. The host uses the SWITCH command to write 0x01 to the HS_TIMING byte, in the Modes segment of the EXT_CSD register.

3.8 Bus Width Selection

After the host verifies the functional pins on the bus, it should change the bus width configuration accordingly, using the SWITCH command. The bus width configuration is changed by writing to the BUS_WIDTH byte in the Modes Segment of the EXT_CSD register (using the SWITCH command to do so). After power-on or software reset, the content of the BUS_WIDTH byte is 0x00.

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3.9 Field Firmware Update (FFU)

To download a new firmware, the controller requires instruction sequence following JEDEC standards.

Longsys eMMC only supports the Manual Mode (MODE_OPERATION_CODES is not supported). For more details, refer to the App note.

3.9.1 Field FW Update Flow - CMD Sequence

Table 12 FFU Command Sequence

Step	Operation	State	CMD	Argument	Remark
1	Go to Transfer	--	CMD0	0X00000000	
		Idle	CMD1	0X40FF8080	Repeat sending CMD1 till OCR bit31 =1
		Ready	CMD2	0X00000000	
		Ident	CMD3	0X00010000	
		Standby	CMD10	0X00010000	Check Product Name of CID to make sure the eMMC is updated (Not Necessary)
		Standby	CMD7	0X00010000	
2	Get EXT_CSD	Transfer	CMD8	0X00000000	Check if FFU is supported by the device by reading SUPPORTED_MODES (EXT_CSD [493]). Check if the FW update is supported by reading FW_CONFIG (EXT_CSD [169]). Save the FIRMWARE_VERSION (EXT_CSD [254:261]), and the FFU_ARG (EXT_CSD [490:487]).
3	Enter FFU mode	Transfer	CMD6	0X031E0100	
4	Send FW to device (Download)	Transfer	CMD24/ CMD25	FFU_ARG	Send the whole FW data after CMD24/ CMD25. Argument must be FFU_ARG.
		Receive	CMD12	0X00000000	If CMD24 is sent, this step is not needed.
5	Exit FFU mode	Transfer	CMD13	0X00010000	
		Transfer	CMD6	0X031E0000	
6	Get EXT_CSD	Transfer	CMD8	0X00000000	Check FFU_STATUS (EXT_CSD [26]). If FFU_STATUS is not 0, then FFU failed.
7	Reset	--	CMD0 or HW Reset or Power Cycle	--	Reset to change the FW.
8	Check FW Version	Transfer	CMD8	0X00000000	Check the FIRMWARE_VERSION (EXT_CSD [254:261]) to judge whether FW is updated or not.

3.9.2 SUPPORTED_MODE [493] (Read Only)

BIT [0]: '0' FFU is not supported by the device.

'1' FFU is supported by the device.

BIT [1]: '0' Vendor specific mode (VSM) is not supported by the device.

'1' Vendor specific mode is supported by the device.

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Table 13 FFU Supported Mode Register

Bit	Field	Supported or Not
BIT [7:2]	Reserved	-
BIT [1]	VSM	Supported
BIT [0]	FFU	Supported

3.9.3 FFU_FEATURE [492] (Read Only)

BIT [0]: '0' Device does not support MODE_OPERATION_CODES field (Manual Mode).

'1' Device supports MODE_OPERATION_CODES field (Auto Mode).

Table 14 FFU Feature Register

Bit	Field	Supported or Not
BIT [7:1]	Reserved	-
BIT [0]	SUPPORTED_MODE_OPERATION_CODES	Not supported

3.9.4 FFU_ARG [490-487] (Read Only)

Using this field, the device reports to the host the value which the host should set as an argument for read and write commands in the FFU mode.

3.9.5 FW_CONFIG [169] (R/W)

BIT [0]: '0' FW update enabled.

'1' FW update disabled permanently

Table 15 FFU FW Config Register

Bit	Field	Supported or Not
BIT [7:1]	Reserved	-
BIT [0]	Update disabled	Supported

3.9.6 MODE_CONFIG [30] (R/W/E_P)

Using this field, the host can change the mode of the device.

Table 16 FFU FW Config Register

Bit	Field	Supported or Not
0x00	Normal Mode	To keep the compatibility
0x01	FFU Mode	-
0x10	Vendor Specific Mode	-
Others	Reserved	-

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3.9.7 FFU_STATUS [26] (Read Only)

Using this field, the device reports to the host the state of FFU process.

Table 17 FFU Status Register

Value	Description
0x13 ~ 0Xff	Reserved
0x12	Error in downloading Firmware
0x11	Firmware installation error
0x10	General error
0x01 ~ 0x0F	Reserved
0x00	Success

3.9.8 OPERATION_CODES_TIMEOUT [491] (Read Only)

Maximum timeout for the SWITCH command is the value set in the MODE_OPERATION_CODES field.

The register is set to '0', because the controller doesn't support MODE_OPERATION_CODES.

Table 18 FFU Operation Codes Timeout Register

Value	Description	Timeout value
0x01 ~ 0x17	MODE_OPERATION_CODES_TIMEOUT = 100us x 2OPERATION_CODES_TIMEOUT	(Not defined)
0x18 ~ 0Xff	Reserved	-

3.9.9 MODE_OPERATION_CODES [29] (W/E_P)

The host sets the operation to be performed in the selected mode. In case MODE_CONFIGS is set to FFU_MODE, MODE_OPERATION_CODES could have the following values:

Table 19 FFU Mode Operation Codes Register

Value	Description
0x01	FFU_INSTALL
0x02	FFU_ABORT
0x00, others	Reserved

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3.10 Vendor Function

3.10.1 Automatic Sleep Mode

If the host does not issue any command during a certain period of time after the previously issued command is completed, the device enters the “Power Saving mode” to reduce power consumption. At this time, commands arriving at the device while it is in the power saving mode will be serviced in normal fashion.

3.10.2 Product Health Information Health Report

Product Health Information is a monitoring system that reports indicators of eMMC reliability, including original bad blocks, increased bad blocks, power-up number, power-loss counts etc. It could predict product failures. We could use recorded Product Health Information data to find where the failures lie, help solve failures and avoid them in future eMMC designs. For more details, please refer to the App Note.

3.10.3 Initial Data Acceleration (IDA)

The eMMC prevents pre-written data loss with IDA in case that our customers need to write data into eMMC before SMT. Please contact your agency for more information.

The amount of pre-written data should be managed properly. It is recommended to limit the size of pre-written data.

For FEMDNN064G-C9A61& FEMDNN128G-C9A61& FEMDNN256G-C9A61, pre-written data is not allowed,which can cause data lost after SMT!

Table 20 IDA Maximum Size

Part Number	Size Limited for Pre-written Data
FEMDNN064G-C9A61	19GB
FEMDNN128G-C9A61	38GB
FEMDNN256G-C9A61	76GB

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4 Register Value

4.1 OCR Register

The 32-bit operation conditions register stores the V_{CCQ} voltage profile of the eMMC. In addition, this register includes a status information bit. This status bit is set if the eMMC power-up procedure has been finished. The OCR register shall be implemented by the eMMC.

Table 21 OCR Register

OCR Bit	V_{CCQ} Voltage Window	eMMC
[6:0]	Reserved	000 0000b
[7]	1.7–1.95	1b
[14:8]	2.0–2.6	000 0000b
[23:15]	2.7–3.6	1 1111 1111b
[28:24]	Reserved	000 0000b
[30:29]	Access Mode	00b (byte mode)/10b (sector mode)
[31]	Power up status bit (busy)*	

Note:
1. This bit is set to LOW if the eMMC has not finished the power-up routine. The supported voltage range is coded as shown in the table.

4.2 CID Register

The Card Identification (CID) register is 128 bits wide. It contains the card identification information used during the card identification phase. Every individual flash or I/O card shall have a unique identification number. Every type of ROM card (defined by content) shall have a unique identification number. The structure of the CID register is defined in the following table.

Table 22 CID Register

Name		Field	Width	CID-slice	CID Value	Remark
Manufacturer ID		MID	8	[127:120]	D6h	
Bank index number		BIN	6	[119:114]	Ah	
Card/BGA		CBX	2	[113:112]	01h	BGA
OEM/Application ID		OID	8	[111:104]	03h	
Product name	FEMDNN064G-C9A61	PNM	48	[103:56]	43 39 41 36 31 31h	C9A611
	FEMDNN128G-C9A61	PNM	48	[103:56]	43 39 41 36 31 32h	C9A612
	FEMDNN256G-C9A61	PNM	48	[103:56]	43 39 41 36 31 34h	C9A614
Product revision		PRV	8	[55:48]	--	
Product serial number		PSN	32	[47:16]	--	Not fixed
Manufacturing date		MDT	8	[15:8]	--	Not fixed
CRC7 checksum		CRC	7	[7:1]	--	Not fixed
Not used, always '1'		-	1	[0:0]	--	

4.3 CSD Register

The Card-Specific Data (CSD) register provides information on how to access the card contents. The CSD defines the data format, error correction type, maximum data access time, data transfer speed,

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whether the DSR register can be used, etc. The programmable part of the register (entries marked by W or E, as shown below) can be changed by CMD27. The types of the CSD Registry entries are coded as follows:

Table 23 CSD Register

Name	Field	Width	Cell Type	CSD-slice	Value
CSD structure	CSD_STRUCTURE	2	R	[127:126]	3h
System specification version	SPEC_VERS	4	R	[125:122]	4h
Reserved	-	2	R	[121:120]	--
Data read access-time 1	TAAC	8	R	[119:112]	FFh
Data read access-time 2 in CLK cycles (NSAC*100)	NSAC	8	R	[111:104]	FFh
Max. bus clock frequency	TRAN_SPEED	8	R	[103:96]	32h
Card command classes	CCC	12	R	[95:84]	9F5h
Max. read data block length	READ_BL_LEN	4	R	[83:80]	9h
Partial blocks for read allowed	READ_BL_PARTIAL	1	R	[79:79]	0h
Write block misalignment	WRITE_BLK_MISALIGN	1	R	[78:78]	0h
Read block misalignment	READ_BLK_MISALIGN	1	R	[77:77]	0h
DSR implemented	DSR_IMP	1	R	[76:76]	0h
Reserved	-	2	R	[75:74]	--
Device size	C_SIZE	12	R	[73:62]	FFFh
Max. read current @V_{DD} min	VDD_R_CURR_MIN	3	R	[61:59]	7h
Max. read current @V_{DD} max	VDD_R_CURR_MAX	3	R	[58:56]	7h
Max. write current @V_{DD} min	VDD_W_CURR_MIN	3	R	[55:53]	7h
Max. write current @V_{DD} max	VDD_W_CURR_MAX	3	R	[52:50]	7h
Device size multiplier	C_SIZE_MULT	3	R	[49:47]	7h
Erase group size	ERASE_GRP_SIZE	5	R	[46:42]	1Fh
Erase group size multiplier	ERASE_GRP_MULT	5	R	[41:37]	1Fh
Write protect group size	WP_GRP_SIZE	5	R	[36:32]	0Fh
Write protect group enable	WP_GRP_ENABLE	1	R	[31:31]	1h
Manufacturer default ECC	DEFAULT_ECC	2	R	[30:29]	0h
Write speed factor	R2W_FACTOR	3	R	[28:26]	5h
Max. write data block length	WRITE_BL_LEN	4	R	[25:22]	9h
Partial blocks for write allowed	WRITE_BL_PARTIAL	1	R	[21:21]	0h
Reserved	-	4	R	[20:17]	--
Content protection application	CONTENT_PROT_APP	1	R	[16:16]	0h
File format group	FILE_FORMAT_GRP	1	R/W	[15:15]	0h
Copy flag (OTP)	COPY	1	R/W	[14:14]	0h
Permanent write protection	PERM_WRITE_PROTECT	1	R/W	[13:13]	0h
Temporary write protection	TMP_WRITE_PROTECT	1	R/W/E	[12:12]	0h
File format	FILE_FORMAT	2	R/W	[11:10]	0h
ECC code	ECC	2	R/W/E	[9:8]	0h

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Name	Field	Width	Cell Type	CSD-slice	Value
CRC	CRC	7	R/W/E	[7:1]	--
Not used, always '1'	-	1	-	[0:0]	--

4.4 Extended CSD Register

The Extended CSD register defines the card properties and selected modes. It is 512 bytes long. The most significant 320 bytes are the Properties segment, which defines the card capabilities and cannot be modified by the host. The lower 192 bytes are the Modes segment, which defines the configuration the card is working in. These modes can be changed by the host by means of the SWITCH command.

Table 24 Extended CSD Register

Name	Field	Size	Type	Slice [Byte]	Value
Reserved*	/	6	/	[511:506]	/
Extended Security Commands Error	EXT_SECURITY_ERR	1	R	[505]	0h
Supported Command Sets	S_CMD_SET	1	R	[504]	1h
HPI Features	HPI_FEATURES	1	R	[503]	1h
Background Operations Support[1]	BKOPS_SUPPORT	1	R	[502]	1h
Max Packed Read Commands	MAX_PACKED_READS	1	R	[501]	3Fh
Max Packed Write Commands	MAX_PACKED_WRITES	1	R	[500]	3Fh
Data Tag Support	DATA_TAG_SUPPORT	1	R	[499]	1h
Tag Unit Size	TAG_UNIT_SIZE	1	R	[498]	3h
Tag Resources Size	TAG_RES_SIZE	1	R	[497]	0h
Context Management Capabilities	CONTEXT_CAPABILITIES	1	R	[496]	5h
Large Unit Size[2]	LARGE_UNIT_SIZE_M1	1	R	[495]	7h
Extended Partitions Attribute Support	EXT_SUPPORT	1	R	[494]	3h
Supported Modes	SUPPORTED_MODES	1	R	[493]	3h
FFU Features	FFU_FEATURES	1	R	[492]	0h
Operation Codes Timeout	OPERATION_CODE_TIMEOUT	1	R	[491]	0h
FFU Argument	FFU_ARG	4	R	[490:487]	0h
Barrier Support	BARRIER_SUPPORT	1	R	[486]	0h
Reserved*	/	177	/	[485:309]	/
CMD Queuing Support	CMDQ_SUPPORT	1	R	[308]	1h
CMD Queuing Depth	CMDQ_DEPTH	1	R	[307]	1Fh
Reserved*	/	1	/	[306]	/
Number Of FW Sectors Correctly Programmed	NUMBER_OF_FW_SECTORS_CORRECTLY_PROGRAMMED	4	R	[305:302]	0h
Vendor Proprietary Health Report	VENDOR_PROPRIETARY_HEALTH_REPORT	1	R	[301:270]	/

1 BKOPS supported.

2 Large Unit Size = 1MB × (LARGE_UNIT_SIZE_M1 + 1).

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Name	Field	Size	Type	Slice [Byte]	Value
Device Life Time Estimation Type B[3]	DEVICE_LIFE_TIME_EST_TYP_B	1	R	[269]	1h
Device Life Time Estimation Type A[4]	DEVICE_LIFE_TIME_EST_TYP_A	1	R	[268]	1h
Pre EOL Information	PRE_EOL_INFO	1	R	[267]	1h
Optimal Read Size	OPTIMAL_READ_SIZE	1	R	[266]	0h
Optimal Write Size	OPTIMAL_WRITE _SIZE	1	R	[265]	20h
Optimal Trim Unit Size	OPTIMAL_TRIM_UNIT_SIZE	1	R	[264]	1h
Device Version	DEVICE_VERSION	2	R	[263:262]	0h
Firmware Version[5]	FIRMWARE_VERSION	8	R	[261:254]	/
Power Class for 200mhz, DDR at VCC=3.6V	PWR_CL_DDR_200_360	1	R	[253]	0h
Cache Size	CACHE_SIZE	4	R	[252:249]	10000h
Generic CMD6 Timeout[6]	GENERIC_CMD6_TIME	1	R	[248]	Ah
Power-off Notification (Long) Timeout[7]	POWER_OFF_LONG_TIME	1	R	[247]	3Ch
Background Operations Status[8]	BKOPS_STATUS	1	R	[246]	0h
Number of Correctly Programmed Sectors	CORRECTLY_PRG_SECTORS_NUM	4	R	[245:242]	/
1st Initialization Time after Partitioning[9]	INI_TIMEOUT_AP	1	R	[241]	1Eh
Cache Flushing Policy	CACHE_FLUSH_POLICY	1	R	[240]	0h
Power Class for 52Mhz, DDR at V_{CC}=3.6V[10]	PWR_CL_DDR_52_360	1	R	[239]	0h
Power Class for 52Mhz, DDR at V_{CC}=1.95V[11]	PWR_CL_DDR_52_195	1	R	[238]	0h
Power Class for 200Mhz at V_{CCQ}=1.95V, VCC=3.6V	PWR_CL_200_195	1	R	[237]	0h
Power Class for 200Mhz at V_{CCQ}=1.3V, VCC=3.6V	PWR_CL_200_130	1	R	[236]	0h
Minimum Write Performance for 8bit @52mhz in DDR Mode[12]	MIN_PERF_DDR_W_8_52	1	R	[235]	0h
Minimum Read Performance for 8bit @52mhz in DDR Mode[13]	MIN_PERF_DDR_R_8_52	1	R	[234]	0h
Reserved*	/	1	/	[233]	/
Trim Multiplier[14]	TRIM_MULT	1	R	[232]	5h
Secure Feature Support[15]	SEC_FEATURE_SUPPORT	1	R	[231]	55h

3 For Enhanced Partition lifetime.
4 For Partition User Area lifetime.
5 FW Patch Ver.
6 Generic CMD6 Timeout = 10ms × GENERIC_CMD6_TIME.
7 Power off Notification (Long) Timeout = 10ms × POWER_OFF_LONG_TIME.
8 No operations required.
9 Initial Timeout = 100ms × INI_TIMEOUT_AP.
10 RMS 100 mA, peak 200 mA.
11 RMS 65 mA, peak 130 mA.
12 For cards not reaching the 4.8MB/s value. Only support SDR.
13 For cards not reaching the 4.8MB/s value.
14 TRIM Timeout = 300ms × TRIM_MULT.
15 a) Support the secure and insecure trim operations. Only support insecure trim operation.

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Name	Field	Size	Type	Slice [Byte]	Value
Secure Erase Multiplier[16]	SEC_ERASE_MULT	1	R	[230]	1Bh
Secure Trim Multiplier[17]	SEC_TRIM_MULT	1	R	[229]	11h
Boot Information[18]	BOOT_INFO	1	R	[228]	7h
Reserved*	/	1	/	[227]	/
Boot Partition Size[19]	BOOT_SIZE_MULT	1	R	[226]	20h
Access Size[20]	ACC_SIZE	1	R	[225]	6h
High-Capacity Erase Unit Size[21]	HC_ERASE_GRP_SIZE	1	R	[224]	1h
High-Capacity Erase Timeout[22]	ERASE_TIMEOUT_MULT	1	R	[223]	5h
Reliable Write Sector Count[23]	REL_WR_SEC_C	1	R	[222]	1h
High-Capacity Write Protect Group Size[24]	HC_WP_GRP_SIZE	1	R	[221]	10h
Sleep Current (V_{CC})[25]	S_C_VCC	1	R	[220]	7h
Sleep Current (V_{CCQ})[26]	S_C_VCCQ	1	R	[219]	9h
Production State Awareness Timeout[27]	PRODUCTION_STATE_AWARENESS_TIMEOUT	1	R	[218]	0h
Sleep/Awake Timeout[28]	S_A_TIMEOUT	1	R	[217]	16h
Sleep Notification Timeout[29]	SLEEP_NOTIFICATION_TIME	1	R	[216]	10h
Sector Count[30]	SEC_COUNT	4	R	[215:212]	X[31]
Secure Write Protection Mode	SECURE_WP_INFO	1	R	[211]	1h
Minimum Write Performance for 8bit @52mhz	MIN_PERF_W_8_52	1	R	[210]	0h
Minimum Read Performance for 8bit @52mhz	MIN_PERF_R_8_52	1	R	[209]	0h
Minimum Write Performance for 4bit @52mhz or 8bit @26mhz	MIN_PERF_W_8_26_4_52	1	R	[208]	0h
Minimum Read Performance for 4bit @52mhz or 8bit @26mhz	MIN_PERF_R_8_26_4_52	1	R	[207]	0h

b) Support the automatic secure purge operation on retired defective portions of the array.
c) Secure purge operations are supported. But physical removal of data is not immediately.
d) Support the sanitize operation.But physical removal of data is not immediately.

16 Secure Erase Timeout = 300ms × ERASE_TIMEOUT_MULT × SEC_ERASE_MULT.
17 Secure TRIM Timeout = 300ms × ERASE_TIMEOUT_MULT × SEC_TRIM_MULT.
18 a) Support high speed timing boot.
b) Support dual data rate during boot.
c) Support alternative boot method.
19 Boot Partition Size = 128Kbytes × BOOT_SIZE_MULT.
20 Super page 16KB.
21 Erase Unit Size = 512Kbyte × HC_ERASE_GRP_SIZE.
22 Erase Timeout = 300 ms × ERASE_TIMEOUT_MULT.
23 1 sector.
24 Write Protect Group Size = 512KB × HC_ERASE_GRP_SIZE × HC_WP_GRP_SIZE.
25 Sleep Current = 1μA × 2^X: register value = X >0.
26 Sleep Current = 1μA × 2^X: register value = X >0.
27 0: Not defined. Production State Timeout = 100us × 2^ PRODUCTION_STATE_AWARENESS_TIMEOUT.
28 Sleep/Awake Timeout = 100ns × 2^S_A_TIMEOUT.
29 Sleep Notification Timeout = 10us × 2^SLEEP_NOTIFICATION_TIME.
30 Depend on density. Device density = SEC_COUNT × 512B.
31 Sector count in hex. See Size (Sector) in Chapter 3.5 Partition Configuration.

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Name	Field	Size	Type	Slice [Byte]	Value
Minimum Write Performance for 4bit @26mhz	MIN_PERF_W_4_26	1	R	[206]	0h
Minimum Read Performance for 4bit @26mhz	MIN_PERF_R_4_26	1	R	[205]	0h
Reserved*	/	1	/	[204]	/
Power Class for 26mhz @3.6V 1R[32]	PWR_CL_26_360	1	R	[203]	0h
Power Class for 52mhz @3.6V 1R [33]	PWR_CL_52_360	1	R	[202]	0h
Power Class for 26mhz @1.95V 1R[34]	PWR_CL_26_195	1	R	[201]	0h
Power Class for 52mhz @1.95V 1R[35]	PWR_CL_52_195	1	R	[200]	0h
Partition Switching Timing[36]	PARTITION_SWITCH_TIME	1	R	[199]	Ah
Out-of-Interrupt Busy Timing[37]	OUT_OF_INTERRUPT_TIME	1	R	[198]	Ah
I/O Driver Strength	DRIVER_STRENGTH	1	R	[197]	1Fh
Device Type [38]	DEVICE_TYPE	1	R	[196]	57h
Reserved*	/	1	/	[195]	/
CSD Structure Version[39]	CSD_STRUCTURE	1	R	[194]	2h
Reserved*	/	1	/	[193]	/
Extended CSD Revision[40]	EXT_CSD_REV	1	R	[192]	8h
Command Set	CMD_SET	1	R/W/E_P	[191]	0h
Reserved*	/	1	/	[190]	/
Command Set Revision	CMD_SET_REV	1	R	[189]	0h
Reserved*	/	1	/	[188]	/
Power Class	POWER_CLASS	1	R/W/E_P	[187]	0h
Reserved*	/	1	/	[186]	/
High Speed Interface Timing	HS_TIMING	1	R/W/E_P	[185]	0h
Strobe Support	STROBE_SUPPORT	1	R	[184]	1h
Bus Width Mode	BUS_WIDTH	1	W/E_P	[183]	0h
Reserved*	/	1	/	[182]	/
Erased Memory Content	ERASED_MEM_CONT	1	R	[181]	0h
Reserved*	/	1	/	[180]	/
Partition Configuration	PARTITION_CONFIG	1	R/W/E, R/W/E_P	[179]	0h
Boot Config Protection	BOOT_CONFIG_PROT	1	R/W, R/W/C_P	[178]	0h
Boot Bus Conditions	BOOT_BUS_CONDITIONS	1	R/W/E	[177]	0h

32 RMS 100 mA, peak 200 mA.
33 RMS 100 mA, peak 200 mA.
34 RMS 65 mA, peak 130 mA.
35 RMS 65 mA, peak 130 mA.
36 Partition Switch Timeout = 10ms × PARTITION_SWITCH_TIME.
37 HPI Timeout = 10ms × OUT_OF_INTERRUPT_TIME.
38 HS400 DDR eMMC@200Mhz-1.8V I/O.
39 CSD version 1.2.
40 Revision 1.8 (for MMC v5.1).

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Name	Field	Size	Type	Slice [Byte]	Value
Reserved*	/	1	/	[176]	/
High-Density Erase Group Definition	ERASE_GROUP_DEF	1	R/W/E_P	[175]	0h
Boot Write Protection Status Registers	BOOT_WP_STATUS	1	R	[174]	0h
Boot Area Write Protection Register	BOOT_WP	1	R/W, R/W/C_P	[173]	0h
Reserved*	/	1	/	[172]	/
User Area Write Protection Register	USER_WP	1	R/W, R/W/C_P, R/W/E_P	[171]	0h
Reserved*	/	1	/	[170]	/
FW Configuration	FW_CONFIG	1	R/W	[169]	0h
RPMB Size[41]	RPMB_SIZE_MULT	1	R	[168]	80h
Write Reliability Setting Register	WR_REL_SET	1	R/W	[167]	1Fh
Write Reliability Parameter Register[42]	WR_REL_PARAM	1	R	[166]	15h
Start Sanitize Operation	SANITIZE_START	1	W/E_P	[165]	0h
Manually Start Background Operations	BKOPS_START	1	W/E_P	[164]	0h
Enable Background Operations Handshake[43]	BKOPS_EN	1	R/W	[163]	0h
H/W Reset Function	RST_n_FUNCTION	1	R/W	[162]	0h
HPI Management	HPI_MGMT	1	R/W/E_P	[161]	0h
Partitioning Support[44]	PARTITIONING_SUPPORT	1	R	[160]	7h
Max Enhanced Area Size	MAX_ENH_SIZE_MULT	3	R	[159:157]	/
Partitions Attribute[45]	PARTITIONS_ATTRIBUTE	1	R/W	[156]	0h
Partitions Setting	PARTITIONS_SETTING_COMPLETED	1	R/W	[155]	0h
General Purpose Partition Size	GP_SIZE_MULT	12	R/W	[154:143]	0h
Enhanced User Data Area Size	ENH_SIZE_MULT	3	R/W	[142:140]	0h
Enhanced User Data Start Address	ENH_START_ADDR	4	R/W	[139:136]	0h
Reserved*	/	1	/	[135]	/
Bad Block Management Mode[46]	SEC_BAD_BLK_MGMNT	1	R/W	[134]	0h
Production State Awareness	PRODUCTION_STATE_AWARENESS	1	R/W/E	[133]	0h
Package Case Temperature is Controlled	TCASE_SUPPORT	1	W/E_P	[132]	0h
Periodic Wake-up	PERIODIC_WAKEUP	1	R/W/E	[131]	0h

41 RPMB Partition Size = 128kB × RPMB_SIZE_MULT.
42 Support the enhanced definition of reliable write.
43 Although these fields can be re-written by host, auto background cannot be closed.
44 Although these fields can be re-written by host, auto background cannot be closed.
44 a) Enhanced technological features in partitions and user data area.
b) Device supports partitioning features.
c) Device can have extended partition attributes.
45 Although these fields can be re-written by host, this function is not supported.
46 Although these fields can be re-written by host, this function is not supported.

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Name	Field	Size	Type	Slice [Byte]	Value
Program CID/CSD in DDR Mode Support	PROGRAM_CID_CSD_DDR_SUPPORT	1	R	[130]	1h
Reserved*	/	2	/	[129:128]	/
Vendor Specific Fields	VENDOR_SPECIFIC_FIELD	64	vendor specific	[127:64]	/
Native Sector Size	NATIVE_SECTOR_SIZE	1	R	[63]	0h
Sector Size Emulation	USE_NATIVE_SECTOR	1	R/W	[62]	0h
Sector Size	DATA_SECTOR_SIZE	1	R	[61]	0h
1st Initialization after Disabling Sector Size Emulation	INI_TIMEOUT_EMU	1	R	[60]	0h
Class 6 Commands Control[47]	CLASS_6_CTRL	1	R/W/E_P	[59]	0h
Number of Addressed Groups to be Released	DYNCAP_NEEDED	1	R	[58]	0h
Exception Events Control	EXCEPTION_EVENTS_CTRL	2	R/W/E_P	[57:56]	0h
Exception Events Status	EXCEPTION_EVENTS_STATUS	2	R	[55:54]	0h
Extended Partitions Attribute[48]	EXT_PARTITIONS_ATTRIBUTE	2	R/W	[53:52]	0h
Context Configuration[49]	CONTEXT_CONF	15	R/W/E_P	[51:37]	0h
Packed Command Status	PACKED_COMMAND_STATUS	1	R	[36]	0h
Packed Command Failure Index	PACKED_FAILURE_INDEX	1	R	[35]	0h
Power off Notification	POWER_OFF_NOTIFICATION	1	R/W/E_P	[34]	0h
Control to Turn the Cache ON/OFF	ON/OFF CACHE_CTRL	1	R/W/E_P	[33]	0h
Flushing of the Cache	FLUSH_CACHE	1	W/E_P	[32]	0h
Control to Turn the Barrier ON/OFF	ON/OFF BARRIER_CTRL	1	R/W	[31]	0h
Mode Config	MODE_CONFIG	1	R/W/E_P	[30]	0h
Mode Operation Codes	MODE_OPERATION_CODES	1	W/E_P	[29]	0h
Reserved*	/	2	/	[28:27]	/
FFU Status	FFU_STATUS	1	R	[26]	0h
Pre Loading Data Size	PRE_LOADING_DATA_SIZE	4	R/W/E_P	[25:22]	0h
Max Pre Loading Data Size	MAX_PRE_LOADING_DATA_SIZE	4	R	[21:18]	/
Product State Awareness Enablement	PRODUCT_STATE_AWARENESS_ENABLEMENT	1	R/W/E, R	[17]	0h
Secure Removal Type	SECURE_REMOVAL_TYPE	1	R/W, R	[16]	39h
Command Queue Mode Enable	CMDQ_MODE_EN	1	R/W/E_P	[15]	0h
Reserved*	/	15	/	[14:0]	/

Notes:
1. Type:
R: Read only
W: One-time programmable and NOT readable.
R/W: One-time programmable and readable.

[47] Although these fields can be re-written by host, this function is not supported.
[48] Although these fields can be re-written by host, this function is not supported.
[49] Although these fields can be re-written by host, this function is not supported.

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R/W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and readable.
R/W/C_P: Writable after value cleared by power failure and HW/ rest assertion (the value not cleared by CMD0 reset) and readable.
R/W/E_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and readable.
2. Reserved*: Reserved bits should be read as 0.

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5 DC Parameters

5.1 Reference Schematics

V_{CC} is used for the NAND flash device; V_{CCQ} is used for the controller and for the eMMC and NAND interface voltage. For more details, please refer to application note.

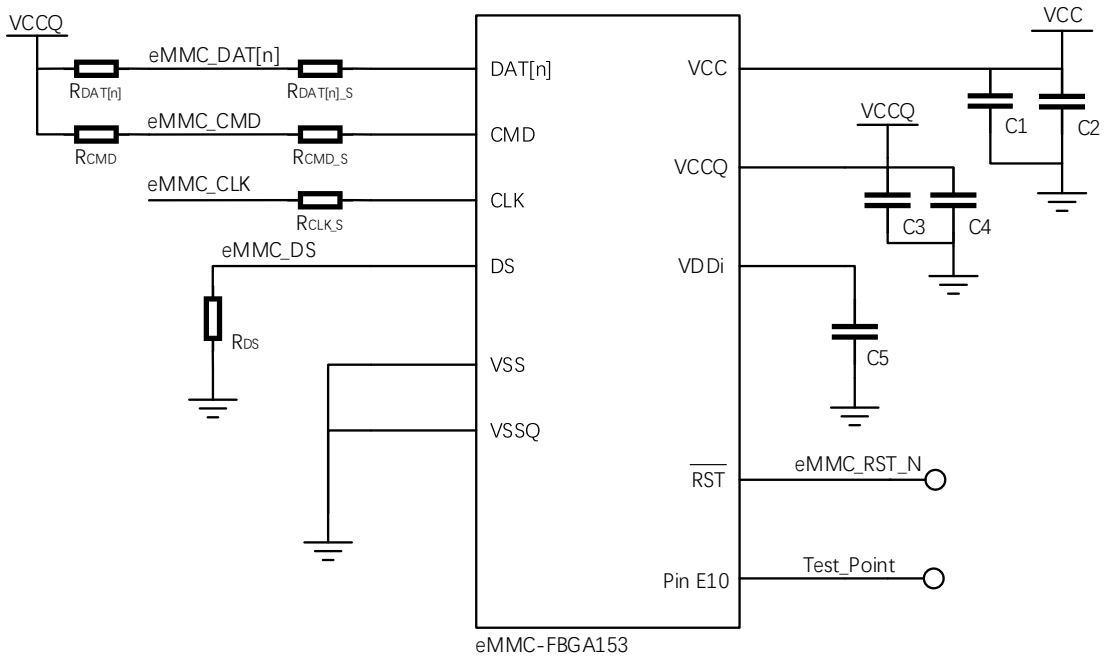


Figure 9 eMMC Reference Schematics

Table 25 Reference Component Parameters

Parameter	Symbol	Min	Typical	Max	Remark
Power of V_{CC}	V_{CC}	2.7V	3.3V	3.6V	Should be separated from V_{CCQ}
Power of V_{CCQ} (High Perf.)	V_{CCQ}	1.7V	1.8V	1.95V	HS200/HS400
Power of V_{CCQ} (Low Perf.)	V_{CCQ}	2.7V	3.3V	3.6V	52MHz CLK SDR/DDR
DAT[n] Pull-Up Resistance	RDAT[n]	10kΩ	--	100kΩ	DAT[n], n=0~7
CMD Pull-Up Resistance	RCMD	4.7kΩ	--	100kΩ	
DS Pull-Down Resistance	RDS	10kΩ	--	100kΩ	HS400
DAT[n] Serial Resistance	RDAT[n]_S	--	0Ω	33Ω	Reserving for EVT
CMD Serial Resistance	RCMD_S	--	0Ω	33Ω	Reserving for EVT
CLK Serial Resistance	RCLK_S	--	0Ω	33Ω	Reserving for EVT
Power Coupling Capacitor 1	C1, C3	2.2μF	--	4.7μF	6.3V, X5R or higher classification
Power Coupling Capacitor 2	C2, C4	--	0.1μF	--	6.3V, X5R or higher classification
VDDi Coupling Capacitor	C5	0.1μF	1μF	--	6.3V, X5R or higher classification

Notes:
1. Coupling capacitor should be connected with V_{CC}/V_{CCQ} and V_{SS} as closely as possible.
2. The V_{CC} and V_{CCQ} power should be separated.
3. It is recommended that the V_{SS} be laid between the CLK and the Data lines.

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5.2 Supply Voltage

Table 26 Supply Voltage

Item	Min	Max	Unit
V_{CCQ}	1.70 (2.7)	1.95 (3.6)	V
V_{CC}	2.7	3.6	V
V_{SS}	-0.5	0.5	V

Note:
1. Once the power supply V_{CC} or V_{CCQ} falls below the minimum guaranteed voltage (for example, upon sudden power failure), the voltage level of V_{CC} or V_{CCQ} shall be kept less than 0.5V for at least 1ms before it goes beyond 0.5V again.

5.3 Absolute Maximum Ratings

Table 27 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Voltage input	V_{IN}	-0.3	4.0	V
V_{CC} supply	V_{CC}	-0.3	4.0	V
V_{CCQ} supply	V_{CCQ}	-0.3	4.0	V

Note:
1. Voltage on any pin relative to V_{SS}.

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6 AC Parameters

6.1 Timing Parameters

Table 28 Timing Parameters

Timing Parameter		Max. Value	Unit
Initialization Time (t_{INIT})	Normal[a]	1	s
	After Partition Setting[b]	3	s
Read Timeout		100	ms
Write Timeout		350	ms
Erase Timeout		1.5	s
Force Erase Timeout		3	min
Secure Erase Timeout		40.5	s
Trim Timeout		1.5	s
Partition Switching Timeout (After Init)		100	ms
Power Off Notification (Short) Timeout		100	ms
Power Off Notification (Long) Timeout		600	ms
Sleep Mode[c]		419.43	ms

It is advised that the timeout values specified in the table above are for testing under Longsys test pattern only.
EXCEPTION_EVENT may occur and the actual timeout situation may vary due to user environment.
a Normal initialization time without initial partition setting.
b Initialization Time after Partition Setting, refer to INI_TIMEOUT_AP in EXT_CSD register.
This Initialization Time for Partition Setting only operates once in the first place during lifetime.
c To access sleep mode, host should issue CMD5. It takes less than 419.43 ms to go to sleep mode in device after issuing CMD5. NAND will be idle during sleep mode.

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6.2 Bus Signal Levels

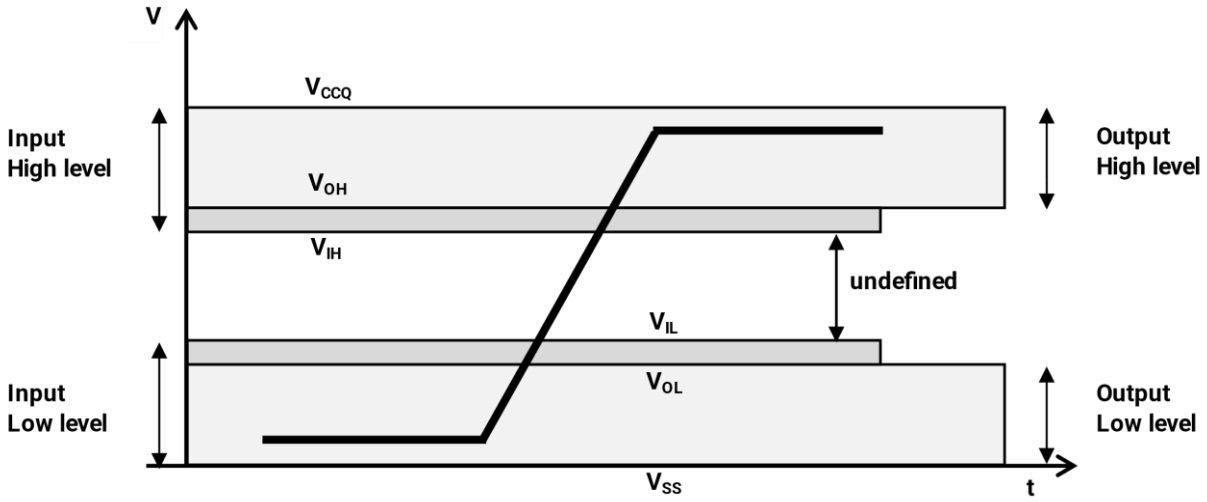


Figure 10 Bus Signal Levels

Table 29 Open-Drain Mode Bus Signal Level

Parameter	Symbol	Min	Max	Unit	Conditions
Output HIGH voltage	V_{OH}	V_{CCQ} - 0.2	-	V	Note 1
Output LOW voltage	V_{OL}	-	0.3	V	I_{OL} = 2mA

Note:
1. Because V_{OH} depends on external resistance value (including value outside the package), this value does not apply as device specification. Host is responsible to choose the external pull-up and open-drain resistance value to meet V_{OH} Min value.

Table 30 Push-Pull Mode Bus Signal Level @V_{CCQ} = 1.8V

Parameter	Symbol	Min	Max	Unit	Conditions
Output HIGH voltage	V_{OH}	V_{CCQ} - 0.45	-	V	I_{OH} = - 2mA
Output LOW voltage	V_{OL}	-	0.45	V	I_{OL} = 2mA
Input HIGH voltage	V_{IH}	0.65 x V_{CCQ}	V_{CCQ} + 0.3	V	
Input LOW voltage	V_{IL}	V_{SS} - 0.3	0.35 x V_{CCQ}	V	

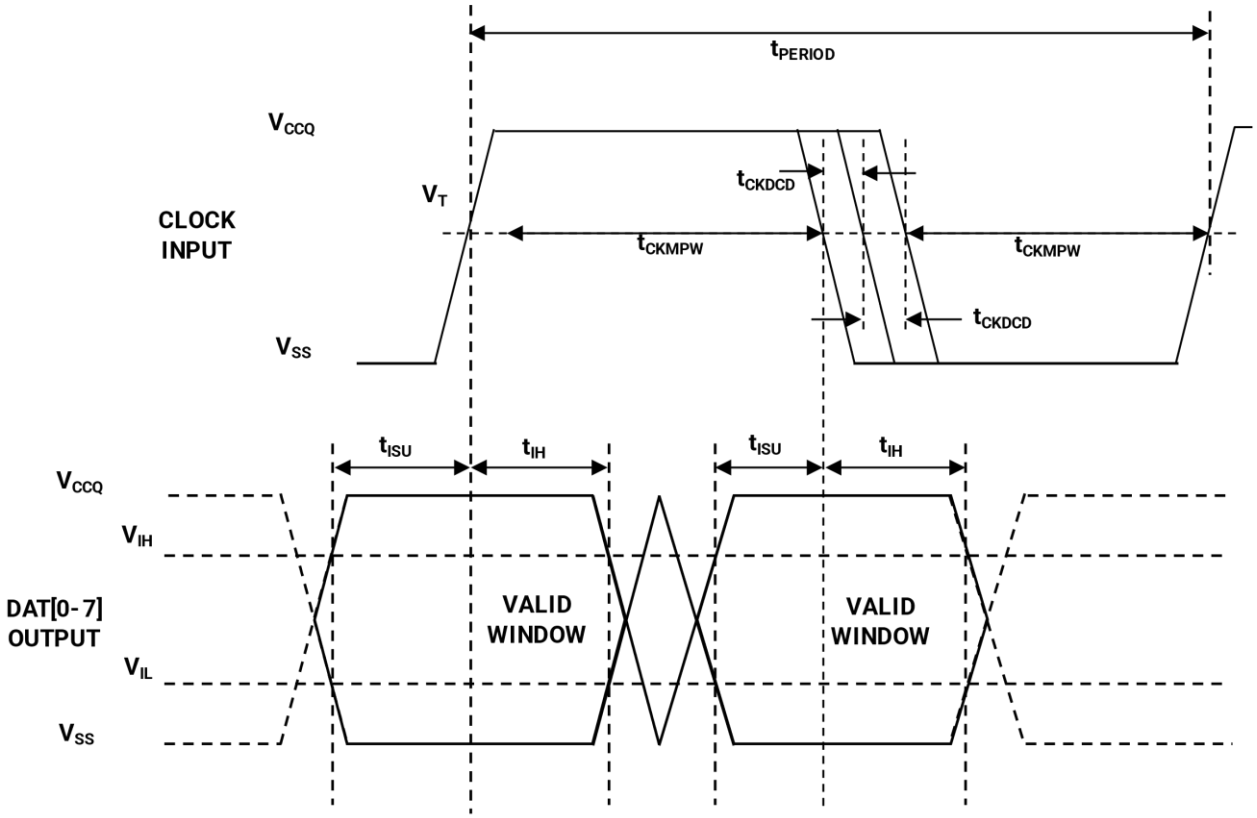
Table 31 Push-Pull Mode Bus Signal Level @V_{CCQ} = 3.3V

Parameter	Symbol	Min	Max	Unit	Conditions
Output HIGH voltage	V_{OH}	0.75 x V_{CCQ}	-	V	I_{OH} = - 100μA @ V_{CCQ} min
Output LOW voltage	V_{OL}	-	0.125 x V_{CCQ}	V	I_{OL} = 100μA @ V_{CCQ} min
Input HIGH voltage	V_{IH}	0.625 x V_{CCQ}	V_{CCQ} + 0.3	V	
Input LOW voltage	V_{IL}	V_{SS} - 0.3	0.25 x V_{CCQ}	V	

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6.3 Bus Timing Specification

6.3.1 HS400 Device Input Timing



Note 1: V_T=50% of V_{CCQ}, indictates clock reference point for timing measurements

Figure 11 HS400 Device Input Timing

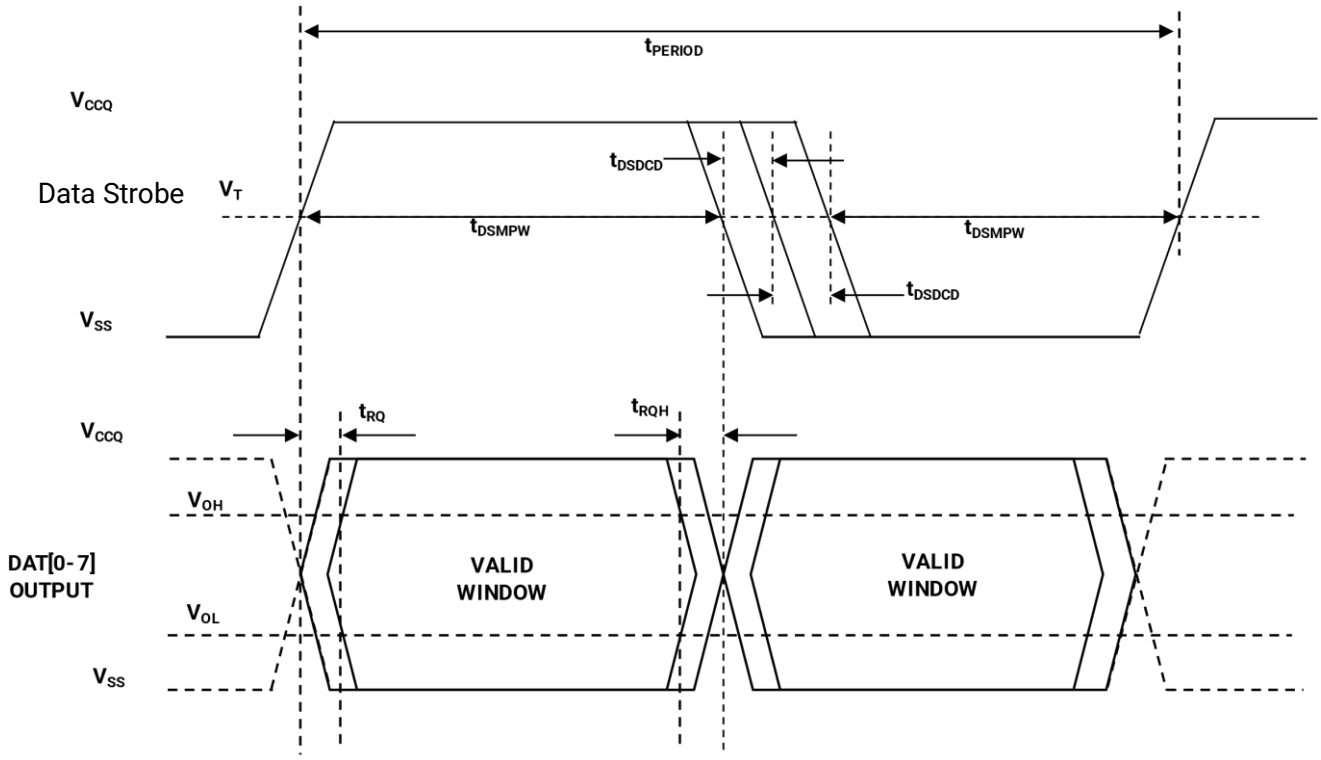
Table 32 HS400 Device Input Timing

Parameter	Symbol	Min	Max	Unit	Remark
Input CLK					
Cycle time data transfer mode	t_{PERIOD}	5	-	ns	200MHz (max), between rising edges with respect to V_T
Slew rate	SR	1.125	-	V/ns	With respect to V_{IN}/V_{IL}
Duty cycle distortion	t_{CKDCD}	0.0	0.3	ns	Allowable deviation from an ideal 50% duty cycle With respect to V_T. Including jitter, phase noise
Minimum pulse width	t_{CKMPW}	2.2	-	ns	With respect to V_T
Input DAT (referenced to CLK)					
Input setup time	t_{ISUddr}	0.4	-	ns	$C_{DEVICE} \leq 6pF$ With respect to V_{IH}/V_{IL}
Input hold time	t_{IHddr}	0.4	-	ns	$C_{DEVICE} \leq 6pF$ With respect to V_{IH}/V_{IL}
Slew rate	SR	1.125	-	V/ns	With respect to V_{IH}/V_{IL}

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6.3.2 HS400 Device Output Timing

The Data Strobe is used to read data in HS400 mode. The Data Strobe is toggled only during data read or CRC status response.



Note 1: V_T=50% of V_{CCQ}, indictates clock reference point for timing measurements

Figure 12 HS400 Device Output Timing

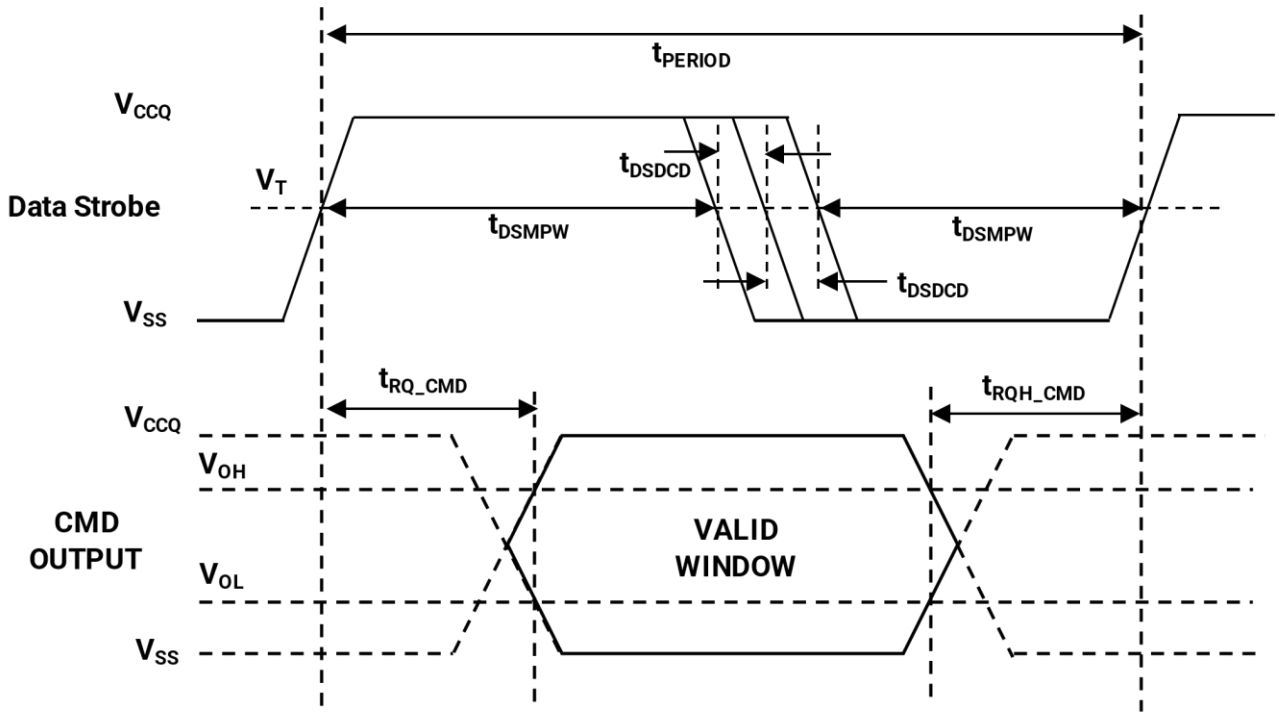
Table 33 HS400 Device Output Timing

Parameter	Symbol	Min	Max	Unit	Remark
Data Strobe					
Cycle time data transfer mode	t_{PERIOD}	5	-	ns	200MHz (max), between rising edges with respect to V_T
Slew rate	SR	1.125	-	V/ns	With respect to V_{OH}/V_{OL} and HS400 reference load
Duty cycle distortion	t_{DSDCD}	0.0	0.2	ns	Allowable deviation from input CLK duty cycle distortion (t_{CKDCD}). With respect to V_T. Including jitter, phase noise
Minimum pulse width	t_{DSMPW}	2.0	-	ns	With respect to V_T
Output DAT (referenced to Data Strobe)					
Output skew	t_{RQ}	-	0.4	ns	With respect to V_{OH}/V_{OL} and HS400 reference load
Output hold skew	t_{RQH}	-	0.4	ns	With respect to V_{OH}/V_{OL} and HS400 reference load
Slew rate	SR	1.125	-	V/ns	With respect to V_{OH}/V_{OL} and HS400 reference load

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6.3.3 HS400 Device Command Output Timing

Data strobe signal is toggled only for Data out, CRC response and CMD Response in HS400 mode.



Note 1: V_T=50% of V_{CCQ}, indictates clock reference point for timing measurements

Figure 13 HS400 Device Command Output Timing

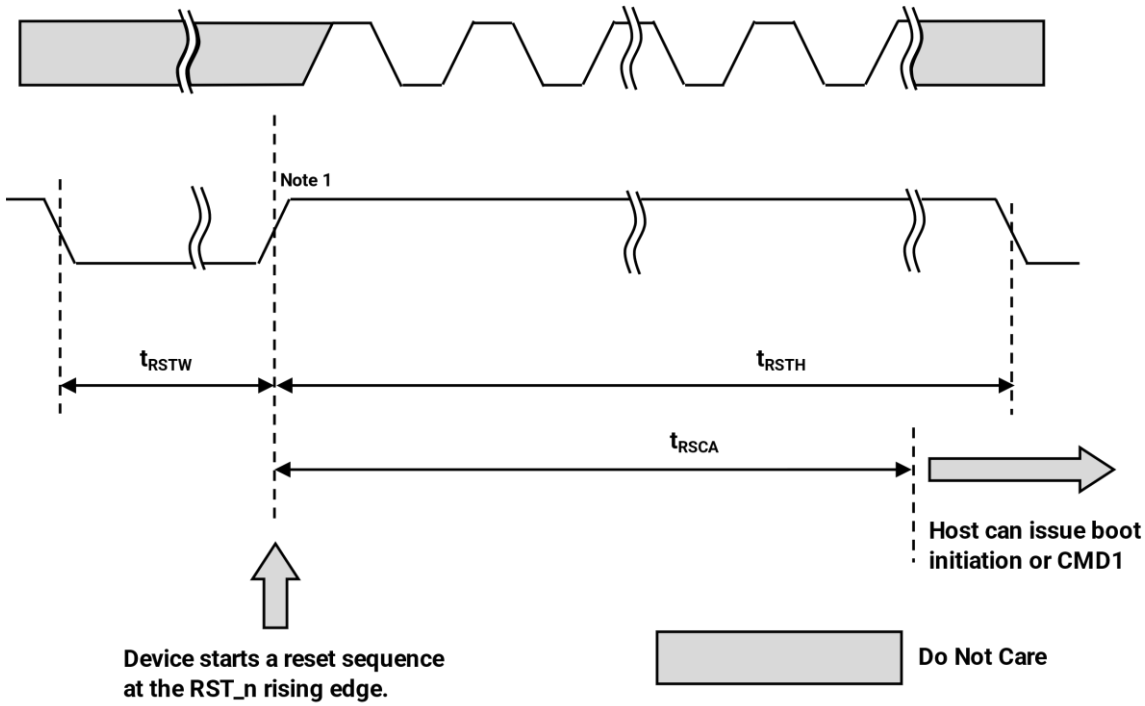
Table 34 HS400 Device Command Output Timing

Parameter	Symbol	Min	Max	Unit	Remark
Data Strobe					
Cycle time data transfer mode	t_{PERIOD}	5	-	ns	200MHz (max), between rising edges with respect to V_T
Slew rate	SR	1.125	-	V/ns	With respect to V_{OH}/V_{OL} and HS400 reference load
Duty cycle distortion	t_{DSDCD}	0.0	0.2	ns	Allowable deviation from input CLK duty cycle distortion (t_{CKDCD}) With respect to V_T. Including jitter, phase noise
Minimum pulse width	t_{DSMPW}	2.0	-	ns	With respect to V_T
CMD Response (referenced to Data Strobe)					
Output skew (CMD)	t_{RQ_CMD}	-	0.4	ns	With respect to V_{OH}/V_{OL} and HS400 reference load
Output hold skew (CMD)	t_{RQH_CMD}	-	0.4	ns	With respect to V_{OH}/V_{OL} and HS400 reference load
Slew rate	SR	1.125	-	V/ns	With respect to V_{OH}/V_{OL} and HS400 reference load

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6.4 H/W Reset Operation

The device will detect the rising edge of the RST_n signal to trigger the internal reset sequence.



Note 1: Device will detect the rising edge of RST_n signal to trigger internal reset sequence.

Figure 14 H/W Reset Operation

Table 35 H/W Reset Timings

Symbol	Parameter	Min	Max	Unit
t_{RSTW}	RST_n pulse width	3	-	μs
t_{RSCA}	RST_n to Command time	200	-	μs
t_{RSTH}	RST_n high period (interval time)	1	-	μs

Notes:
1. 74 cycles of clock signal required before issuing CMD1 or CMD0 with argument 0xFFFFFFFA.
2. During the device's internal initialization sequence right after power-on, the device may not be able to detect RST_n signal, because the device may not complete loading RST_n_ENABLE bits of the extended CSD register into the controller yet.

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6.5 Power On

An eMMC bus power-up is handled locally in each device and in the bus master. Figure 15 shows the power-on sequence.

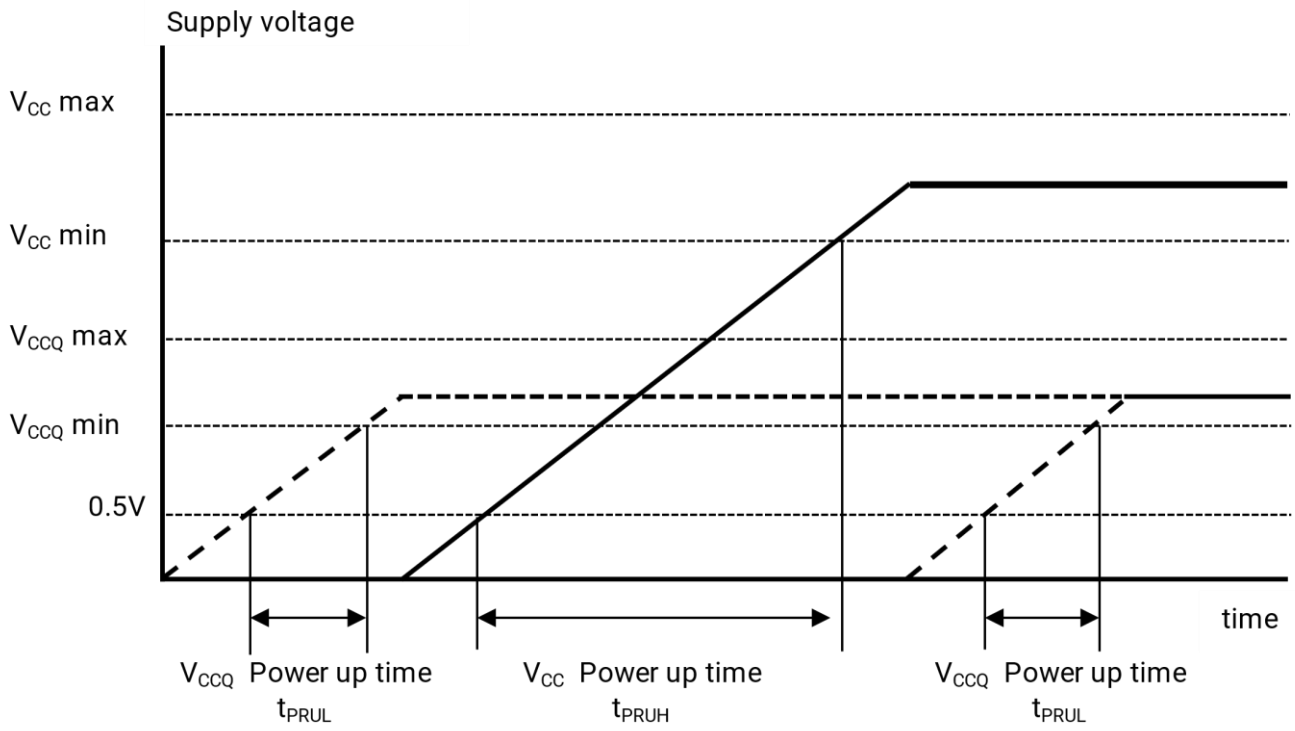


Figure 15 Power-on Sequence

Table 36 Power-on Parameters

Parameter	Symbol	Min	Max
Supply power-up 3.3V	t_{PRUH}	10 µs	35 ms
Supply power-up 1.8V	t_{PRUL}	10 µs	25 ms

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Revision History

Version	Date	Description
0.1	2025/01/03	Draft for ES sample

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