CSNP1GCR01-BOW

Version：V1.1

JAN20, 2021

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

扫码查规格书

Revision History

Version	Date	Description
V1.0	16/03/2020	Origin Draft
V1.1	20/01/2021	Updated operating temperature

Contents

REVISION HISTORY I

1. INTRODUCTION 1

1.1 OVERVIEW 1
1.2 FEATURES 1
1.3 BLOCK DIAGRAM 1

2. PRODUCT SPECIFICATIONS 2

2.1 PIN ASSIGNMENTS (TOP VIEW) 2
2.2 PACKAGE DIMENSIONS 2

3. PERFORMANCE 4

4. DC CHARACTERISTICS 5

5. AC CHARACTERISTICS 6

5.1 BUS TIMING (DEFAULT MODE) 6
5.2 BUS TIMING (HIGH-SPEED MODE) 6

6. REFERENCE DESIGN 8

1. Introduction

1.1 Overview

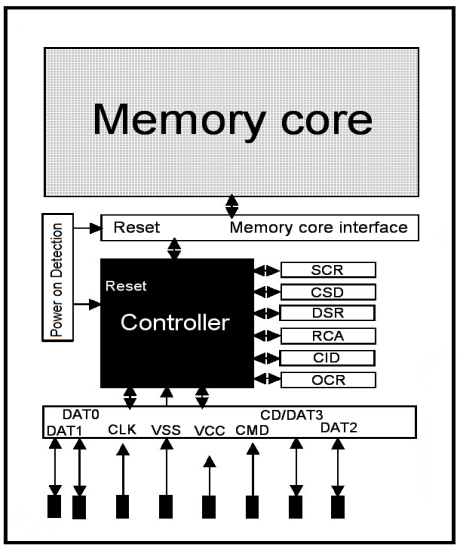
CSNP1GCR01-BOW is an 1Gb density of embedded storage based on NAND Flash and SD controller. This product has many advantages comparing to raw NAND, it has embedded bad block management, and stronger embedded ECC.

CSNP1GCR01-BOW is LGA-8 package. The size is 8mm x 6mm x0.75mm.

1.2 Features

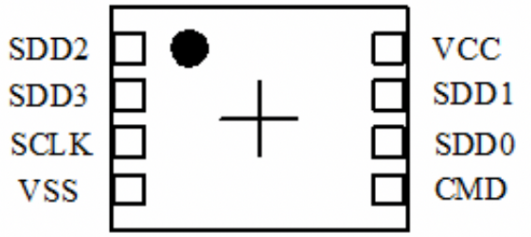
- Interface: Standard SD Specification Version 2.0 with 1-I/O and 4-I/O.
- Power supply: Vcc = 2.7V - 3.6V
- Default mode: Variable clock rate 0 - 25 MHz, up to 12.5 MB/sec interface speed (using 4 parallel data lines)
- High-Speed mode: Variable clock rate 0 - 50 MHz, up to 25 MB/sec interface speed (using 4 parallel data lines)
- Operating Temperature: -30°C to +85°C
- Storage Temperature: -40°C to +85°C
- Standby Current：< 200uA

1.3 Block Diagram



2. Product Specifications

2.1 Pin Assignments (Top View)

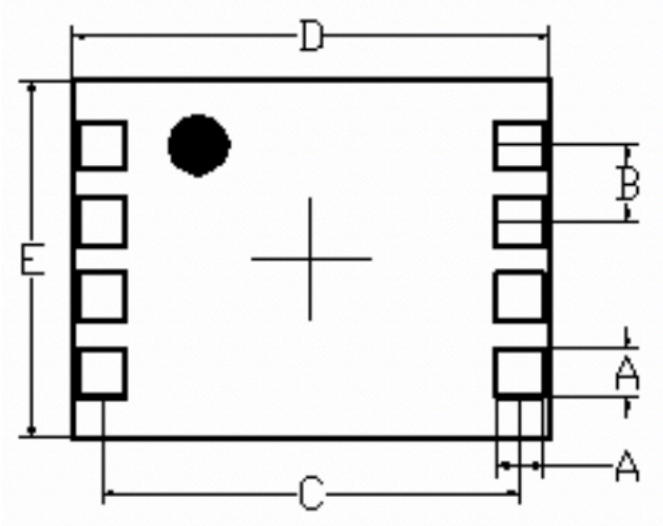


PIN#	SD MODE			SPI MODE		
	NAME	TYPE[1]	DESCRIPTION	NAME	TYPE	DESCRIPTION
1	SDD2	I/O/PP	Data Line [Bit2]	RSV		Reserved
2	CD/SDD3[2]	I/O/PP[3]	SDNAND Detect/ Data Line [Bit3]	CS	I[3]	Chip Select (Neg True)
3	SCLK	I	Clock	SCLK	I	Clock
4	VSS	S	Supply Voltage Ground	VSS	S	Supply Voltage Ground
5	CMD	PP	Command/Response	DI	I	Data In
6	SDD0	I/O/PP	Data Line [Bit0]	DO	O/PP	Data Out
7	SDD1	I/O/PP	Data Line [Bit1]	RSV		Reserved
8	VCC	S	Supply Voltage	VCC	S	Supply Voltage

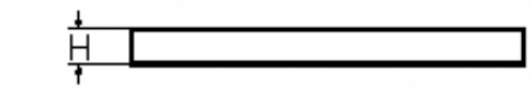
1) S: power supply; I: input; O: output using push-pull drivers; PP: I/O using push-pull drivers;

2) The extended SDD lines (SDD1-SDD3) are input on power up. They start to operate as SDD lines after SET_BUS_WIDTH command. The Host shall keep its own SDD1-SDD3 lines in input mode, as well, while they are not used. It is defined so, in order to keep compatibility to SDNAND.

2.2 Package Dimensions



TOP VIEW



SIDE VIEW

	Common Dimensions			
Symbol	**Min**	**Nom**	**Max**	**Note**
A	0.65	0.75	0.85	
B	1.17	1.27	1.37	
C	6.90	7	7.10	
D	7.90	8	8.10	
E	5.90	6	6.10	
F	10.90	11	11.1	
H	0.75	0.85	0.95	

SDNAND Package Dimensions (unit: mm)

3. Performance

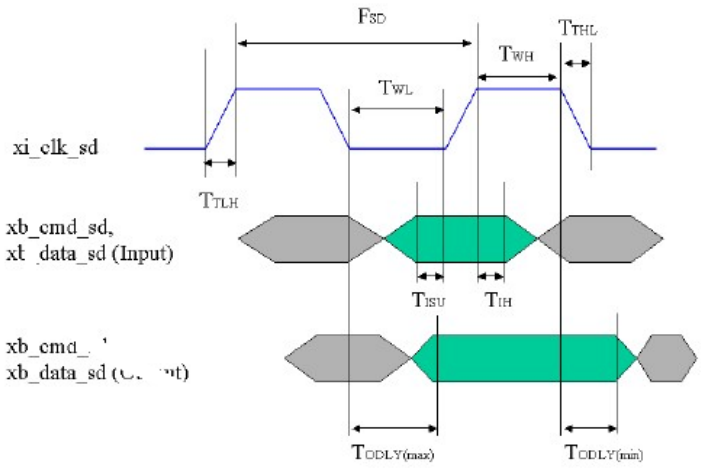
Parameter	Range	
Temperature	Work Model	-30° ~ 85℃
	Storage Model	- 40° ~ 85℃
Humidity	Work Model	8% to 95%, Non-condensing
	Storage Model	8% to 95%, Non-condensing

4. DC Characteristics

Symbol	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IL}	Input low voltage		VSS-0.3		0.25VCC	V
V_{IH}	Input high voltage		0.625VCC		VCC+0.3	V
V_{OL}	Output low voltage	IOL=100μA @VCC_min			0.125VCC	V
V_{OH}	Output high voltage	IOH=100μA @VCC_min	0.75VCC			V
I_{IN}	Input leakage current	VIN=VCC or 0	-10	+/-1	10	μA
I_{OUT}	Tri-state output leakage current		-10	+/-1	10	μA
I_{STBY}	Standby current	3.3V@clock stop		150	200	μA
I_{OP}	Operation current	3.3v@50MHz (Write)		15	25	mA
		3.3v@50MHz (Read)		15	25	mA

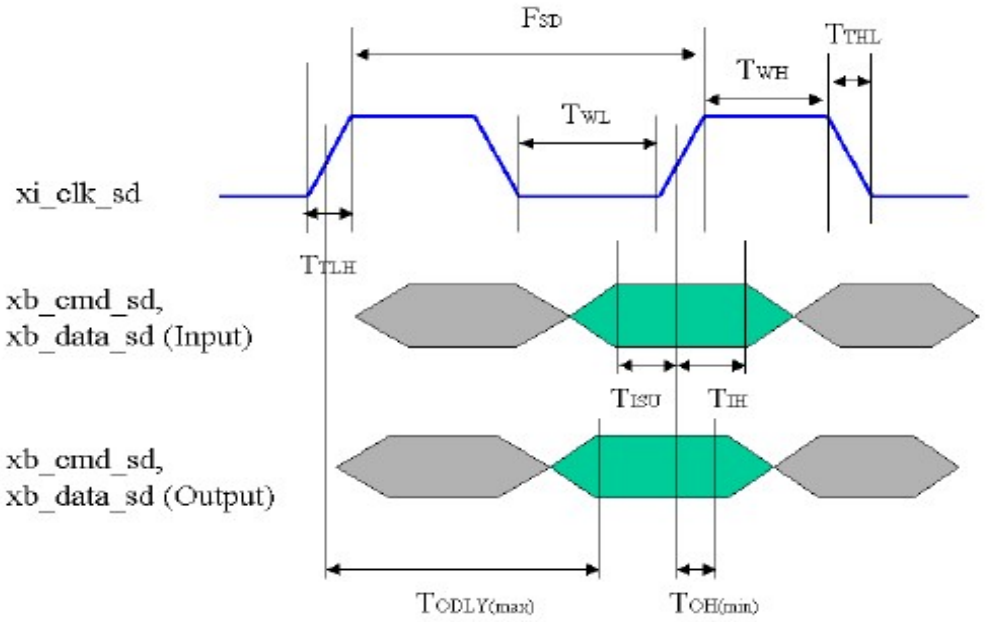
5. AC Characteristics

5.1 Bus Timing (Default Mode)



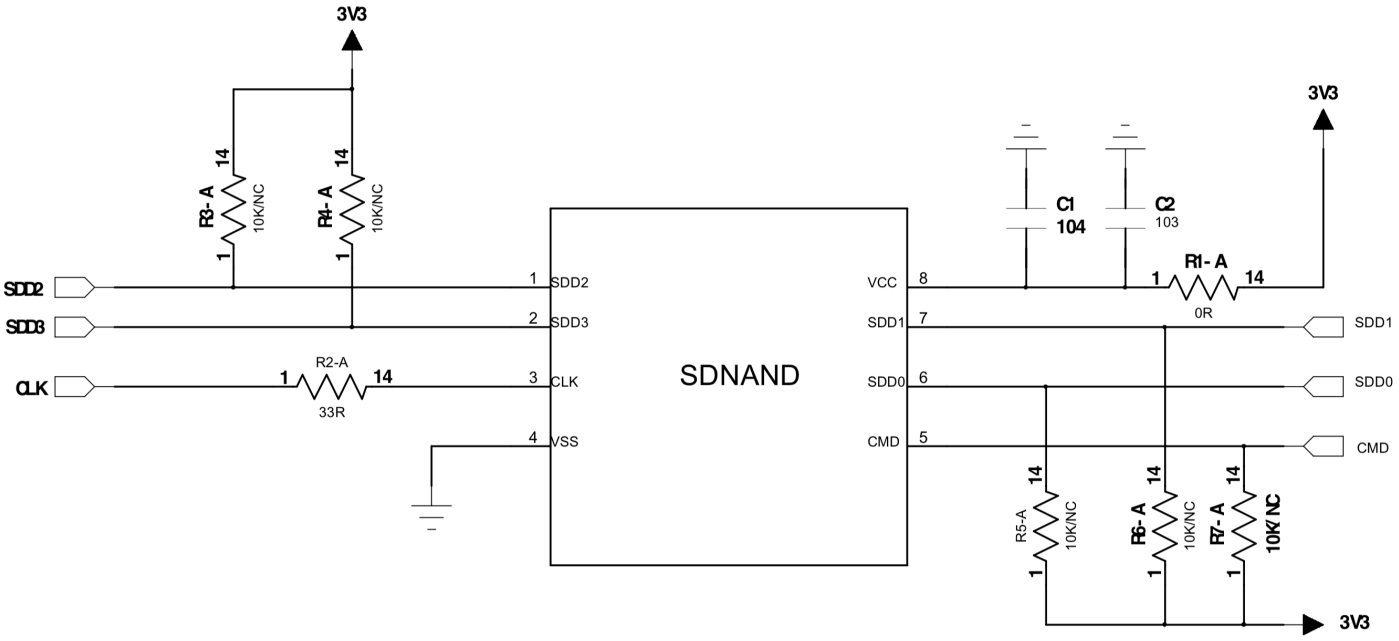
SYMBOL	PARAMETER	MIN	MAX	UNIT	NOTE
F_{SD}	SD clock frequency	0	25	MHz	
T_{WL}	Clock low time	10		ns	
T_{WH}	Clock high time	10		ns	
T_{TLH}	Clock rise time		10	ns	
T_{THL}	Clock fall time		10	ns	
T_{ISU}	Input setup time	5		ns	
T_{IH}	Input hold time	5		ns	
T_{ODLY}	Output delay time	0	14	ns	

5.2 Bus Timing (High-speed Mode)



SYMBOL	PARAMETER	MIN	MAX	UNIT	NOTE
F_{SD}	SD clock frequency	0	25	MHz	
T_{WL}	Clock low time	10		ns	
T_{WH}	Clock high time	10		ns	
T_{TLH}	Clock rise time		10	ns	
T_{THL}	Clock fall time		10	ns	
T_{ISU}	Input setup time	5		ns	
T_{IH}	Input hold time	5		ns	
T_{ODLY}	Output delay time	0	14	ns	
T_{OH}	Output hold time	2.5		ns	

6. Reference Design



Note：

R_{DAT} and R_{CMD} (10K~100 kΩ) are pull-up resistors protecting the CMD and the DAT lines against bus floating when SDNAND is in a high-impedance mode.

The host shall pull-up all DAT0-3 lines by R_{DAT}, even if the host uses the SDNAND as 1-bit mode only in SD mode. It is recommended to have 2.2uF capacitance on VCC.

R_{CLK} reference 0~120 Ω.