AT25128B and AT25256B

SPI Serial EEPROM

128K (16,384 x 8), 256K (32,768 x 8)

DATASHEET

Features

- Serial Peripheral Interface (SPI) Compatible
- Supports SPI Modes 0 (0,0) and 3 (1,1)
  - Data Sheet Describes Mode 0 Operation
- Low-voltage and Standard-voltage Operation
  - V_{CC} = 1.8V to 5.5V
- 20MHz Clock Rate (5V)
- 64-byte Page Mode and Byte Write Operation
- Block Write Protection
  - Protect 1/4, 1/2, or Entire Array
- Write Protect ($\overline{WP}$) Pin and Write Disable Instructions for Both Hardware and Software Data Protection
- Self-timed Write Cycle (5ms max)
- High Reliability
  - Endurance: 1,000,000 Write Cycles
  - Data Retention: 100 Years
- Green (Pb/Halogen-free/RoHS Compliant) Packaging Options
- Die Sales: Wafer Form, Waffle Pack, and Bumped Wafers

Description

The Atmel® AT25128B/256B provides 131,072/262,144 bits of Serial Electrically Erasable Programmable Read-Only Memory (EEPROM) organized as 16,384/32,768 words of 8 bits each. The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operation are essential. The AT25128B/256B is available in space saving JEDEC SOIC, TSSOP, UDFN, and VFBGA packages.

The AT25128B/256B is enabled through the Chip Select pin ($\overline{CS}$) and accessed via a 3-Wire interface consisting of Serial Data Input (SI), Serial Data Output (SO), and Serial Clock (SCK). All programming cycles are completely self-timed, and no separate erase cycle is required before write.

Block Write protection is enabled by programming the status register with one of four blocks of Write Protection. Separate Program Enable and Program Disable instructions are provided for additional data protection. Hardware Data Protection is provided via the $\overline{WP}$ pin to protect against inadvertent write attempts. The $\overline{HOLD}$ pin may be used to suspend any serial communication without resetting the serial sequence.

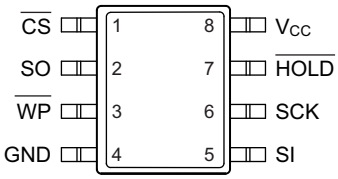
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1. Pin Configurations

Table 1-1. Pin Configurations

Pin Name	Function
$\overline{CS}$	Chip Select
GND	Ground
$\overline{HOLD}$	Suspends Serial Input
SCK	Serial Data Clock
SI	Serial Data Input
SO	Serial Data Output
V_{CC}	Power Supply
$\overline{WP}$	Write Protect

8-lead SOIC



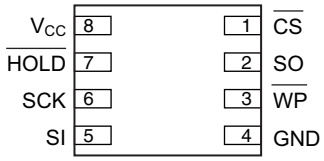
Top View

8-lead TSSOP



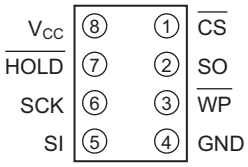
Top View

8-pad UDFN



Bottom View

8-ball VFBGA



Bottom View

Note: Drawings are not to scale.

2. Absolute Maximum Ratings*

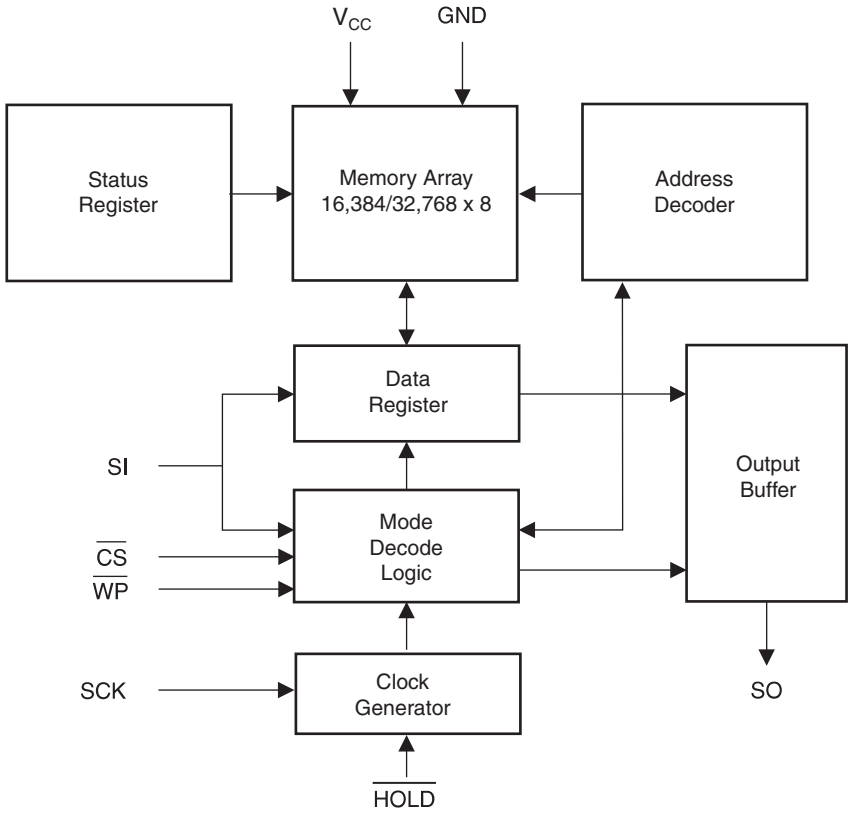
Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on any pin with respect to ground	-1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0mA

*Notice: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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3. Block Diagram

Figure 3-1. Block Diagram



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4. Electrical Characteristics

4.1 Pin Capacitance[1]

Table 4-1. Pin Capacitance

Applicable over recommended operating range from T_A = 25°C, f = 1MHz, V_{CC} = +5V (unless otherwise noted).

Symbol	Test Conditions	Max	Units	Conditions
C_{OUT}	Output Capacitance (SO)	8	pF	V_{OUT} = 0V
C_{IN}	Input Capacitance ($\overline{CS}$, SCK, SI, $\overline{WP}$, $\overline{HOLD}$)	6	pF	V_{IN} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

4.2 DC Characteristics

Table 4-2. DC Characteristics

Applicable over recommended operating range from: T_{AI} = -40°C to +85°C, V_{CC} = +1.8V to +5.5V, (unless otherwise noted).

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
V_{CC1}	Supply Voltage			1.8		5.5	V
V_{CC2}	Supply Voltage			2.5		5.5	V
V_{CC3}	Supply Voltage			4.5		5.5	V
I_{CC1}	Supply Current	V_{CC} = 5V at 20MHz SO = Open, Read			9	10	mA
I_{CC2}	Supply Current	V_{CC} = 5V at 10MHz SO = Open, Read, Write			5	7	mA
I_{CC3}	Supply Current	V_{CC} = 5V at 1MHz SO = Open, Read, Write			2.2	3.5	mA
I_{SB1}	Standby Current	V_{CC} = 1.8V, $\overline{CS}$ = V_{CC}			0.2	3	µA
I_{SB2}	Standby Current	V_{CC} = 2.5V, $\overline{CS}$ = V_{CC}			0.5	3	µA
I_{SB3}	Standby Current	V_{CC} = 5.0V, $\overline{CS}$ = V_{CC}			2	5	µA
I_{IL}	Input Leakage	V_{IN} = 0V to V_{CC}		-3		3	µA
I_{OL}	Output Leakage	V_{IN} = 0V to V_{CC} T_{AC} = 0°C to 70°C		-3		3	µA
V_{IL}[1]	Input Low-voltage			-1		V_{CC} x 0.3	V
V_{IH}[1]	Input High-voltage			V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL1}	Output Low-voltage	3.6V ≤ V_{CC} ≤ 5.5V	I_{OL} = 3.00mA			0.4	V
V_{OH1}	Output High-voltage	3.6V ≤ V_{CC} ≤ 5.5V	I_{OH} = -1.60mA	V_{CC} – 0.8			V
V_{OL2}	Output Low-voltage	1.8V ≤ V_{CC} ≤ 3.6V	I_{OL} = 0.15mA			0.2	V
V_{OH2}	Output High-voltage	1.8V ≤ V_{CC} ≤ 3.6V	I_{OH} = -100µA	V_{CC} – 0.2			V

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

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4.3 AC Characteristics

Table 4-3. AC Characteristics

Applicable over recommended operating range from T_{AI} = -40 to +85°C, V_{CC} = As Specified, CL = 1 TTL Gate and 30pF (unless otherwise noted).

Symbol	Parameter	Voltage	Min	Max	Units
f_{SCK}	SCK Clock Frequency	4.5 – 5.5 2.5 – 5.5 1.8 – 5.5	0 0 0	20 10 5	MHz
t_{RI}	Input Rise Time	4.5 – 5.5 2.5 – 5.5 1.8 – 5.5		2 2 2	µs
t_{FI}	Input Fall Time	4.5 – 5.5 2.5 – 5.5 1.8 – 5.5		2 2 2	µs
t_{WH}	SCK High Time	4.5 – 5.5 2.5 – 5.5 1.8 – 5.5	20 40 80		ns
t_{WL}	SCK Low Time	4.5 – 5.5 2.5 – 5.5 1.8 – 5.5	20 40 80		ns
t_{CS}	$\overline{CS}$ High Time	4.5 – 5.5 2.5 – 5.5 1.8 – 5.5	100 100 200		ns
t_{CSS}	$\overline{CS}$ Setup Time	4.5 – 5.5 2.5 – 5.5 1.8 – 5.5	100 100 200		ns
t_{CSH}	$\overline{CS}$ Hold Time	4.5 – 5.5 2.5 – 5.5 1.8 – 5.5	100 100 200		ns
t_{SU}	Data In Setup Time	4.5 – 5.5 2.5 – 5.5 1.8 – 5.5	5 10 20		ns
t_H	Data In Hold Time	4.5 – 5.5 2.5 – 5.5 1.8 – 5.5	5 10 20		ns
t_{HD}	$\overline{Hold}$ Setup Time	4.5 – 5.5 2.5 – 5.5 1.8 – 5.5	5 10 20		ns
t_{CD}	$\overline{Hold}$ Hold Time	4.5 – 5.5 2.5 – 5.5 1.8 – 5.5	5 10 20		ns
t_V	Output Valid	4.5 – 5.5 2.5 – 5.5 1.8 – 5.5	0 0 0	20 40 80	ns
t_{HO}	Output Hold Time	4.5 – 5.5 2.5 – 5.5 1.8 – 5.5	0 0 0		ns

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Table 4-3. AC Characteristics (Continued)

Applicable over recommended operating range from T_{AI} = -40 to +85°C, V_{CC} = As Specified, CL = 1 TTL Gate and 30pF (unless otherwise noted).

Symbol	Parameter	Voltage	Min	Max	Units
t_{LZ}	$\overline{\text{Hold}}$ to Output Low Z	4.5 – 5.5 2.5 – 5.5 1.8 – 5.5	0 0 0	25 50 100	ns
t_{HZ}	$\overline{\text{Hold}}$ to Output High Z	4.5 – 5.5 2.5 – 5.5 1.8 – 5.5		25 50 100	ns
t_{DIS}	Output Disable Time	4.5 – 5.5 2.5 – 5.5 1.8 – 5.5		25 50 100	ns
t_{WC}	Write Cycle Time	4.5 – 5.5 2.5 – 5.5 1.8 – 5.5		5 5 5	ms
Endurance(1)	3.3V, 25°C, Page Mode		1,000,000		Write Cycles

Note: 1. This parameter is characterized and is not 100% tested.

5. Serial Interface Description

Master: The device that generates the serial clock.

Slave: Because the Serial Clock pin (SCK) is always an input, the AT25128B/256B always operates as a slave.

Transmitter/Receiver: The AT25128B/256B has separate pins designated for data transmission (SO) and reception (SI).

MSB: The Most Significant Bit (MSB) is the first bit transmitted and received.

Serial Opcode: After the device is selected with $\overline{\text{CS}}$ going low, the first byte will be received. This byte contains the opcode which defines the operations to be performed.

Invalid Opcode: If an invalid opcode is received, no data will be shifted into the AT25128B/256B, and the serial output pin (SO) will remain in a high-impedance state until the falling edge of $\overline{\text{CS}}$ is detected again. This will reinitialize the serial communication.

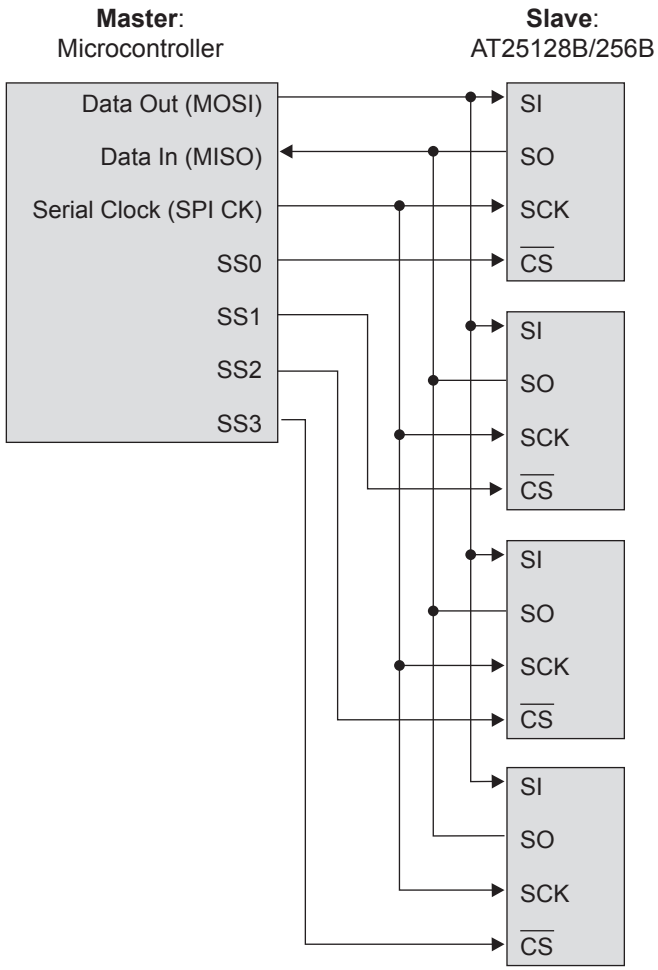
Chip Select: The AT25128B/256B is selected when the $\overline{\text{CS}}$ pin is low. When the device is not selected, data will not be accepted via the SI pin, and the SO pin will remain in a high-impedance state.

Hold: The $\overline{\text{HOLD}}$ pin is used in conjunction with the $\overline{\text{CS}}$ pin to select the AT25128B/256B. When the device is selected and a serial sequence is underway, $\overline{\text{HOLD}}$ can be used to pause the serial communication with the master device without resetting the serial sequence. To pause, the $\overline{\text{HOLD}}$ pin must be brought low while the SCK pin is low. To resume serial communication, the $\overline{\text{HOLD}}$ pin is brought high while the SCK pin is low (SCK may still toggle during $\overline{\text{HOLD}}$). Inputs to the SI pin will be ignored while the SO pin is in the high-impedance state.

Write Protect: The Write Protect pin ($\overline{\text{WP}}$) will allow normal read/write operations when held high. When the $\overline{\text{WP}}$ pin is brought low and WPEN bit is one, all write operations to the status register are inhibited. $\overline{\text{WP}}$ going low while CS is still low will interrupt a write to the status register. If the internal write cycle has already been initiated, $\overline{\text{WP}}$ going low will have no effect on any write operation to the status register. The $\overline{\text{WP}}$ pin function is blocked when the WPEN bit in the status register is zero. This will allow the user to install the AT25128B/256B in a system with the $\overline{\text{WP}}$ pin tied to ground and still be able to write to the status register. All $\overline{\text{WP}}$ pin functions are enabled when the WPEN bit is set to one.

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Figure 5-1. SPI Serial Interface



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6. Functional Description

The AT25128B/256B is designed to interface directly with the synchronous Serial Peripheral Interface (SPI) of the 6800 series of microcontrollers.

The AT25128B/256B utilizes an 8-bit instruction register. The list of instructions and their operation codes are contained in Figure 6-1. All instructions, addresses, and data are transferred with the MSB first and start with a high-to-low $\overline{CS}$ transition.

Table 6-1. Instruction Set for the AT25010B/020B/040B

Instruction Name	Instruction Format	Operation
WREN	0000 X110	Set Write Enable Latch
WRDI	0000 X100	Reset Write Enable Latch
RDSR	0000 X101	Read Status Register
WRSR	0000 X001	Write Status Register
READ	0000 X011	Read Data from Memory Array
WRITE	0000 X010	Write Data to Memory Array

Write Enable (WREN): The device will power-up in the Write Disable state when V_{CC} is applied. All programming instructions must therefore be preceded by a Write Enable instruction. The $\overline{WP}$ pin must be held high during a WREN instruction.

Write Disable (WRDI): To protect the device against inadvertent writes, the Write Disable instruction disables all programming modes. The WRDI instruction is independent of the status of the $\overline{WP}$ pin.

Read Status Register (RDSR): The Read Status Register instruction provides access to the status register. The Read/Busy and Write Enable status of the device can be determined by the RDSR instruction. Similarly, the Block Write Protection bits indicate the extent of protection employed. These bits are set by using the WRSR instruction.

Table 6-2. Status Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WPEN	X	X	X	BP1	BP0	WEN	$\overline{RDY}$

Table 6-3. Read Status Register Bit Definition

Bit	Definition
Bit 0 ($\overline{RDY}$)	Bit 0 = 0 ($\overline{RDY}$) indicates the device is ready. Bit 0 = 1 indicates the write cycle is in progress.
Bit 1 (WEN)	Bit 1 = 0 indicates the device *is not* write enabled. Bit 1 = 1 indicates the device is write enabled.
Bit 2 (BP0)	See Table 6-4.
Bit 3 (BP1)	See Table 6-4.
Bits 4 to 6 are zeros when the device is not in an internal write cycle.	
Bit 7 (WPEN)	See Table 6-5.
Bits 0 to 7 are ones during an internal write cycle.	

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Write Status Register (WRSR): The WRSR instruction allows the user to select one of four levels of protection. The AT25128B/256B is divided into four array segments. None, one-quarter (¼), one-half (½), or all of the memory segments can be protected. Any of the data within any selected segment will therefore be read-only. The block write protection levels and corresponding status register control bits are shown in Table 6-4.

Bits BP1, BP0, and WPEN are nonvolatile cells that have the same properties and functions as the regular memory cells (e.g., WREN, t_{WC}, RDSR).

Table 6-4. Block Write Protect Bits

Level	Status Register Bits		Array Addresses Protected	
	BP1	BP0	AT25128B	AT25256B
0	0	0	None	None
1 (¼)	0	1	3000 – 3FFF	6000 – 7FFF
2 (½)	1	0	2000 – 3FFF	4000 – 7FFF
3 (All)	1	1	0000 – 3FFF	0000 – 7FFF

The WRSR instruction also allows the user to enable or disable the write protect ($\overline{WP}$) pin through the use of the Write Protect Enable (WPEN) bit. Hardware write protection is enabled when the $\overline{WP}$ pin is low and the WPEN bit is one. The hardware write protection is disabled when either the $\overline{WP}$ pin is high or the WPEN bit is zero. When the device is hardware write protected, writes to the Status Register including the Block Protect bits, the WPEN bit, and the block protected sections in the memory array are disabled. Writes are only allowed to sections of the memory which are not block-protected.

Note: When the WPEN bit is hardware write protected, it cannot be changed back to zero as long as the $\overline{WP}$ pin is held low.

Table 6-5. WPEN Operation

WPEN	$\overline{WP}$	WEN	Protected Blocks	Unprotected Blocks	Status Register
0	X	0	Protected	Protected	Protected
0	X	1	Protected	Writable	Writable
1	Low	0	Protected	Protected	Protected
1	Low	1	Protected	Writable	Protected
X	High	0	Protected	Protected	Protected
X	High	1	Protected	Writable	Writable

Read Sequence (READ): Reading the AT25128B/256B via the SO pin requires the following sequence. After the $\overline{CS}$ line is pulled low to select a device, the Read opcode is transmitted via the SI line followed by the byte address to be read (Table 6-6). Upon completion, any data on the SI line will be ignored. The data (D7 – D0) at the specified address is then shifted out onto the SO line. If only one byte is to be read, the $\overline{CS}$ line should be driven high after the data comes out. The Read Sequence can be continued since the byte address is automatically incremented and data will continue to be shifted out. When the highest address is reached, the address counter will roll-over to the lowest address allowing the entire memory to be read in one continuous read cycle.

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Write Sequence (WRITE): In order to program the AT25128B/256B, the Write Protect pin ($\overline{WP}$) must be held high and two separate instructions must be executed. First, the device *must be write enabled* via the WREN instruction. Then a Write (WRITE) instruction may be executed. Also, the address of the memory location(s) to be programmed must be outside the protected address field location selected by the Block Write Protection level. During an internal write cycle, all commands will be ignored except the RDSR instruction.

A Write instruction requires the following sequence. After the $\overline{CS}$ line is pulled low to select the device, the Write opcode is transmitted via the SI line followed by the byte address and the data (D7 – D0) to be programmed (see Table 6-6 for the address key). Programming will start after the $\overline{CS}$ pin is brought high. The low-to-high transition of the $\overline{CS}$ pin must occur during the SCK low time immediately after clocking in the D0 (LSB) data bit.

The Ready/Busy status of the device can be determined by initiating a Read Status Register (RDSR) instruction. If Bit 0 is one, the write cycle is still in progress. If Bit 0 is zero, the write cycle has ended. Only the RDSR instruction is enabled during the write programming cycle.

The AT25128B/256B is capable of an 64-byte Page Write operation. After each byte of data is received, the six low-order address bits are internally incremented by one; the high-order bits of the address will remain constant. If more than 64 bytes of data are transmitted, the address counter will roll-over, and the previously written data will be overwritten. The AT25128B/256B is automatically returned to the Write Disable state at the completion of a write cycle.

Note: If the $\overline{WP}$ pin is brought low or if the device is not Write Enabled (WREN), the device will ignore the Write instruction and will return to the standby state, when $\overline{CS}$ is brought high. A new CS falling edge is required to reinitiate the serial communication.

Table 6-6. Address Key

Address	AT25128B	AT25256B
A_N	$A_{13} – A_0$	$A_{14} – A_0$
Don’t Care Bits	$A_{15} – A_{14}$	A_{15}

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7. Timing Diagrams — SPI Mode 0 (0,0)

Figure 7-1. Synchronous Data Timing (for Mode 0)

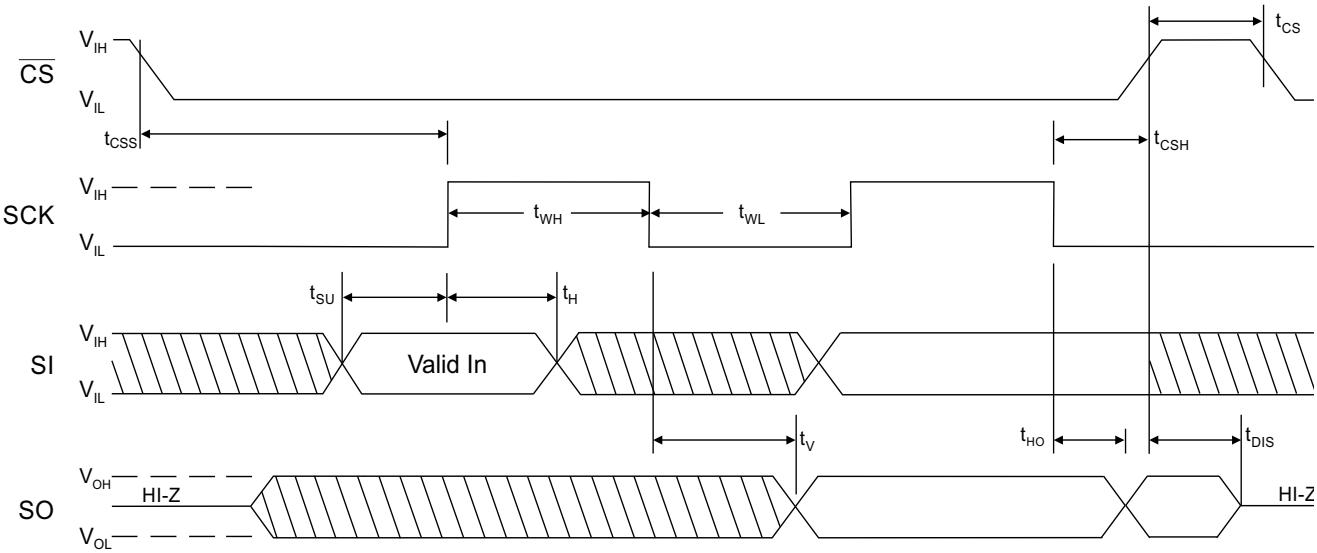


Figure 7-2. WREN Timing

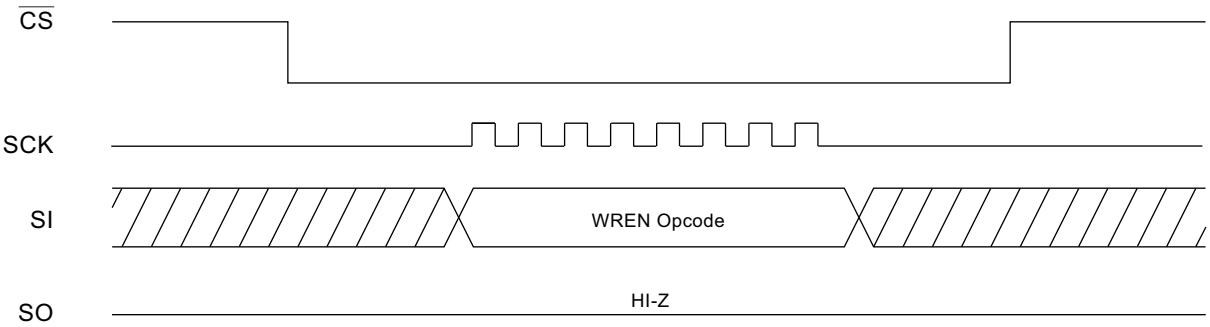
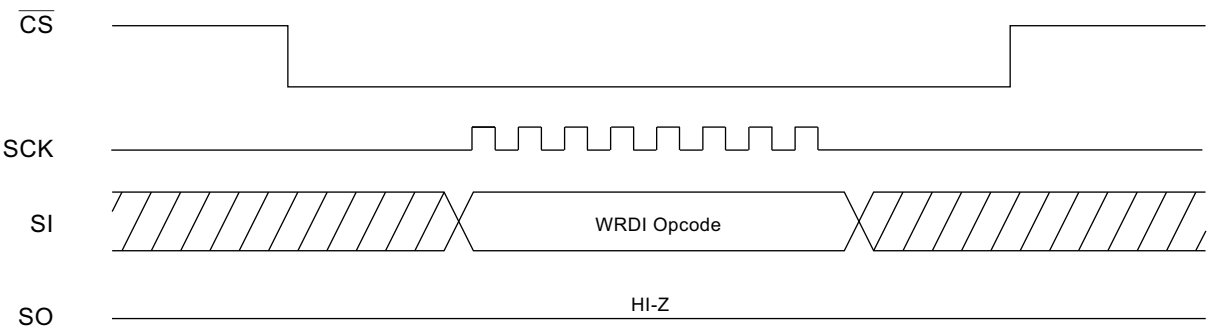


Figure 7-3. WRDI Timing



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Figure 7-4. RDSR Timing

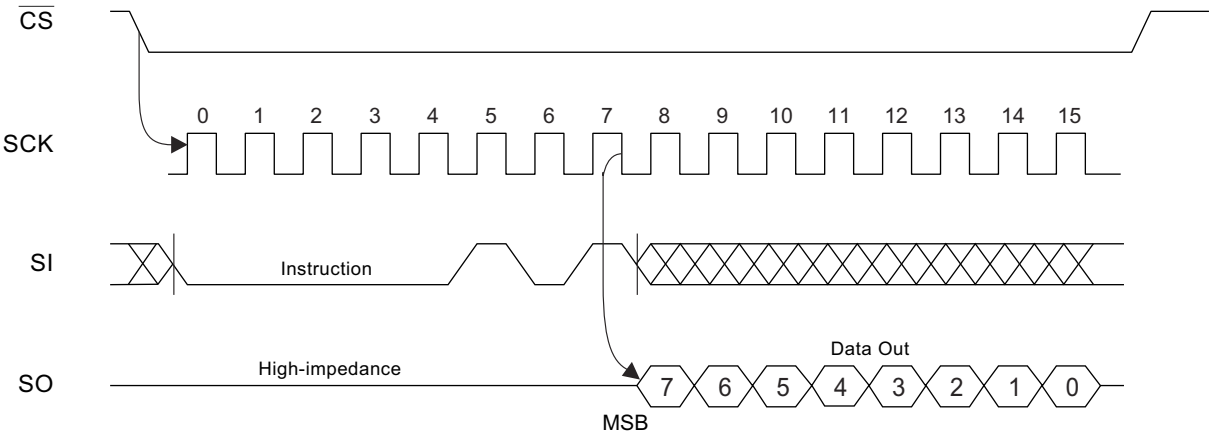


Figure 7-5. WRSR Timing

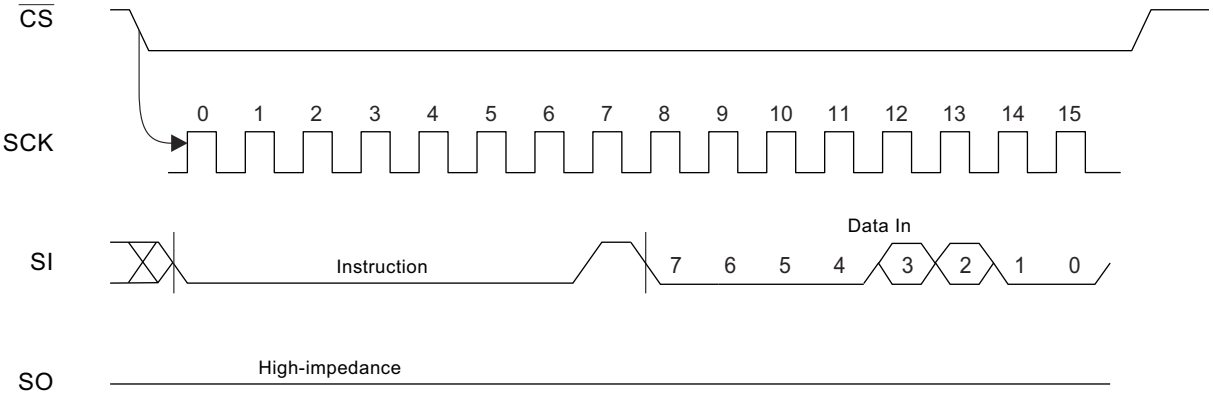
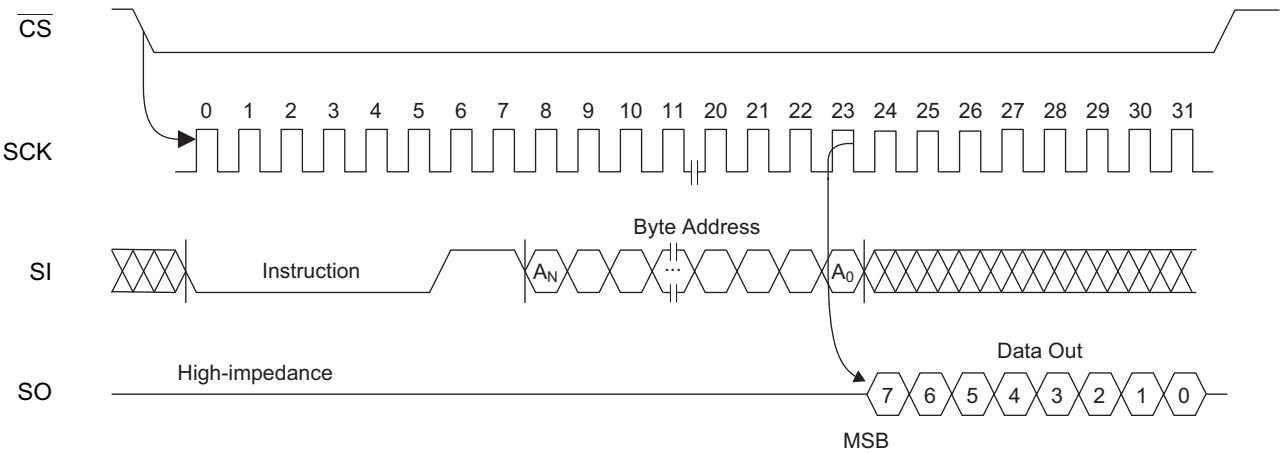


Figure 7-6. READ Timing



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Figure 7-7. WRITE Timing

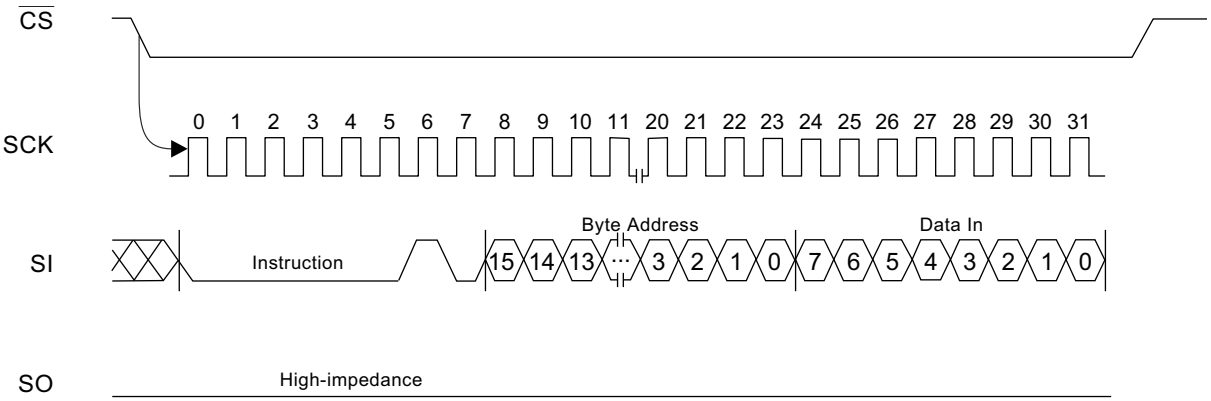
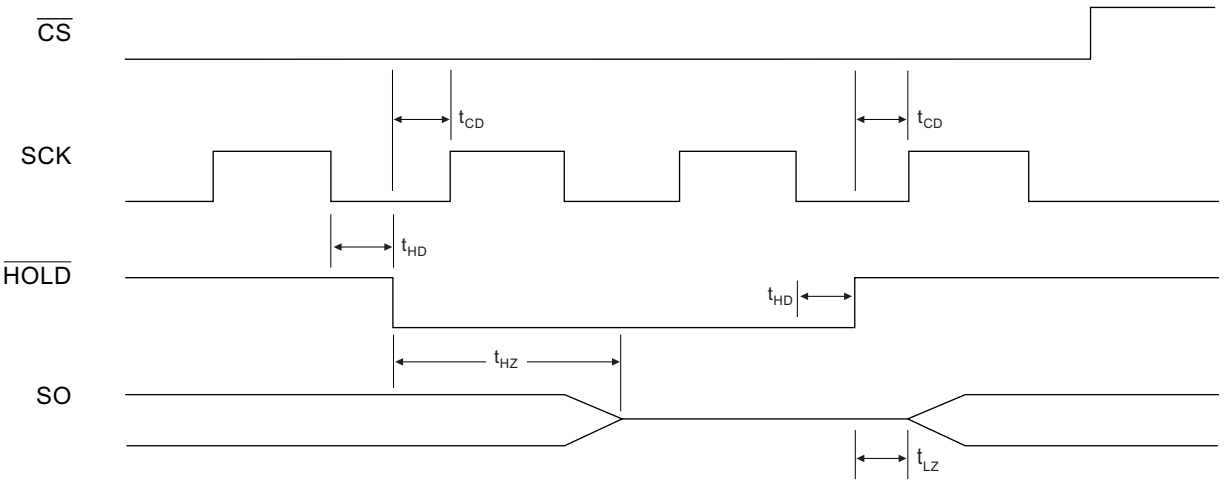
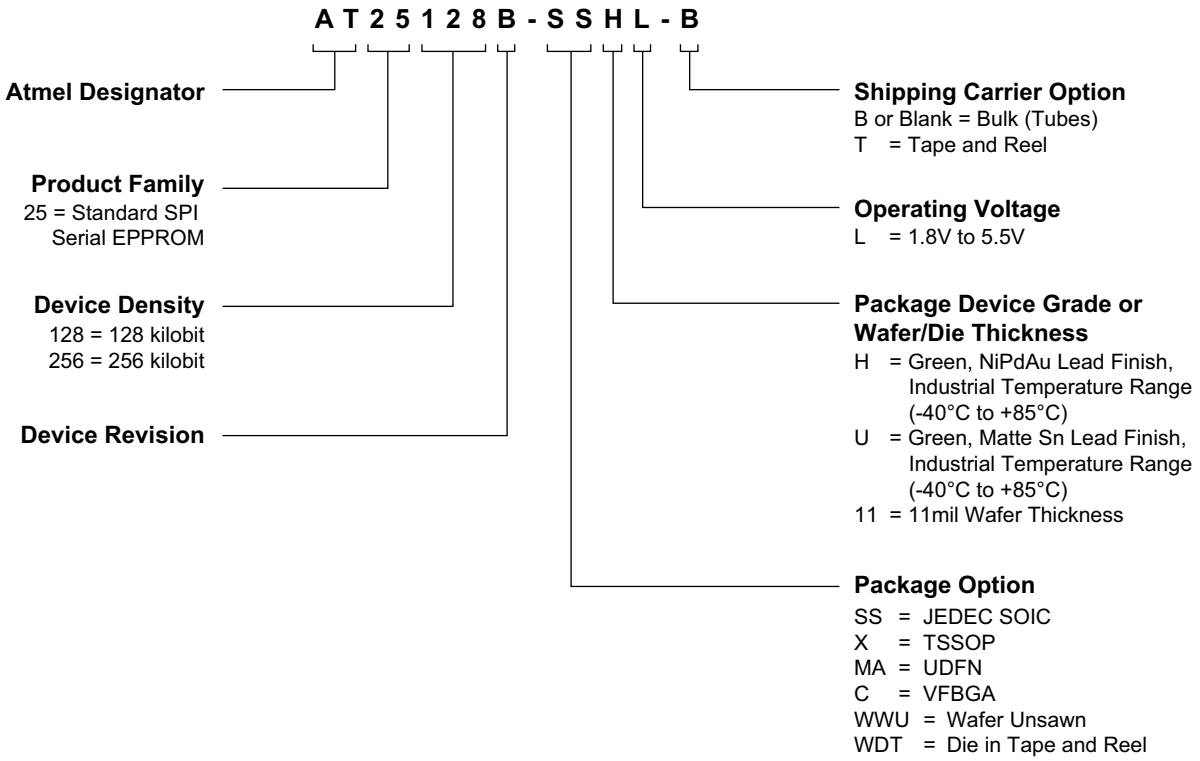


Figure 7-8. $\overline{\text{HOLD}}$ Timing



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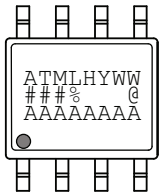
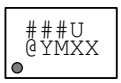
8. Ordering Code Detail



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9. Part Markings

AT25128B and AT25256B: Package Marking Information

8-lead SOIC	8-lead TSSOP
	
8-pad UDFN	**8-ball VFBGA**
2.0 x 3.0 mm Body	2.35 x 3.73 mm Body
	

Note 1: ● designates pin 1

Note 2: Package drawings are not to scale

Catalog Number Truncation			
AT25128B		Truncation Code ###: 5DB	
AT25256B		Truncation Code ###: 5EB	
Date Codes			**Voltages**
Y = Year		M = Month	WW = Work Week of Assembly	% = Minimum Voltage
4: 2014	8: 2018	A: January	02: Week 2	L: 1.8V min
5: 2015	9: 2019	B: February	04: Week 4	
6: 2016	0: 2020	...	...	
7: 2017	1: 2021	L: December	52: Week 52	
Country of Assembly	**Lot Number**		**Grade/Lead Finish Material**
@ = Country of Assembly	AAA...A = Atmel Wafer Lot Number		U: Industrial/Matte Tin/SnAgCu H: Industrial/NiPdAu
Trace Code			**Atmel Truncation**
XX = Trace Code (Atmel Lot Numbers Correspond to Code) Example: AA, AB.... YZ, ZZ			AT: Atmel ATM: Atmel ATML: Atmel

3/11/14

Atmel Package Mark Contact: DL-CSO-Assy_eng@atmel.com	**TITLE** **25128-256BSM**, AT25128B and AT25256B Package Marking Information	**DRAWING NO.** 25128-256BSM	**REV.** A

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10. Ordering Information

Atmel Ordering Code	Lead Finish	Package	Voltage	Operation Range
AT25128B-SSHL-B (1)	NiPdAu (Lead-free/Halogen-free)	8S1	1.8V to 5.5V	Industrial Temperature (-40 to +85°C)
AT25128B-SSHL-T (2)				
AT25128B-XHL-B (1)		8X		
AT25128B-XHL-T (2)				
AT25128B-MAHL-T (2)		8MA2		
AT25128B-CUL-T (2)	SnAgCu (Lead-free/Halogen-free)	8U2-1		
AT25128B-WWU11L (3)	—	Wafer		
AT25256B-SSHL-B (1)	NiPdAu (Lead-free/Halogen-free)	8S1	1.8V to 5.5V	Industrial Temperature (-40 to +85°C)
AT25256B-SSHL-T (2)				
AT25256B-XHL-B (1)		8X		
AT25256B-XHL-T (2)				
AT25256B-MAHL-T (2)		8MA2		
AT25256B-CUL-T (2)	SnAgCu (Lead-free/Halogen-free)	8U2-1		
AT25256B-WWU11L (3)	—	Wafer		

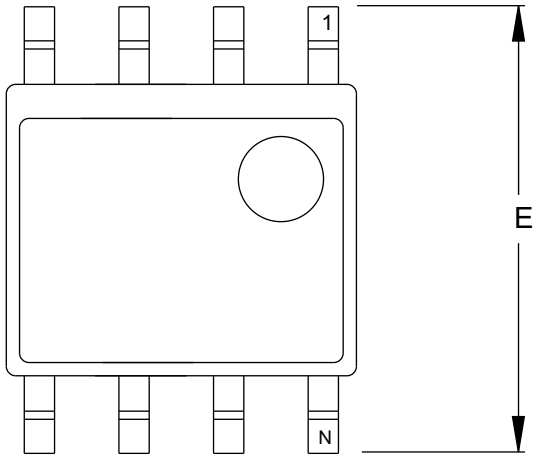
Notes:
1. B = Bulk delivery in tubes.
   - SOIC and TSSOP = 100 per tube
2. T = Tape and Reel
   - SOIC = 4,000 per reel
   - TSSOP, UDFN, and VFBGA = 5,000 per reel
3. Contact Atmel Sales for Wafer sales.

Package Type	
8S1	8-lead, 0.15" wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8X	8-lead, 4.40mm body, Plastic Thin Shrink Small Outline Package (TSSOP)
8MA2	8-pad, 2.00mm x 3.00mm body, 0.50mm pitch, Plastic Ultra Thin Dual Flat No Lead (UDFN)
8U2-1	8-ball, 2.35mm x 3.73mm body, 0.75mm pitch, Very Thin, Fine-Pitch Ball Grid Array (VFBGA)

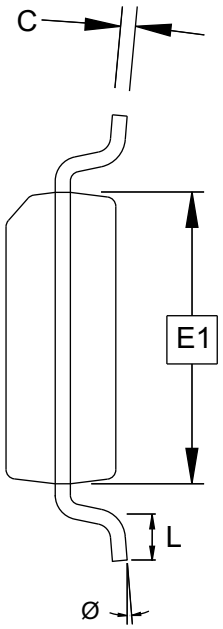
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11. Packaging Information

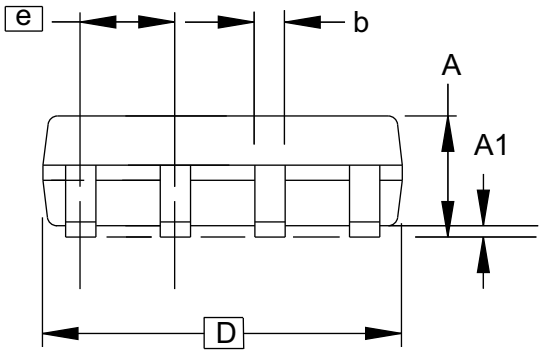
11.1 8S1 — 8-lead JEDEC SOIC



TOP VIEW



END VIEW



SIDE VIEW

Notes: This drawing is for general information only.
Refer to JEDEC Drawing MS-012, Variation AA
for proper dimensions, tolerances, datums, etc.

COMMON DIMENSIONS
(Unit of Measure = mm)

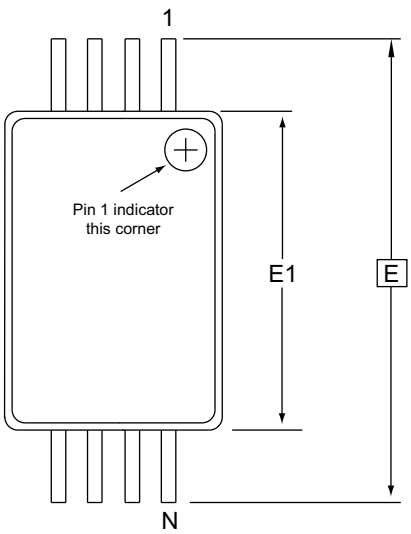
SYMBOL	MIN	NOM	MAX	NOTE
A	1.35	–	1.75	
A1	0.10	–	0.25	
b	0.31	–	0.51	
C	0.17	–	0.25	
D	4.80	–	5.05	
E1	3.81	–	3.99	
E	5.79	–	6.20	
e	1.27 BSC			
L	0.40	–	1.27	
Ø	0°	–	8°	

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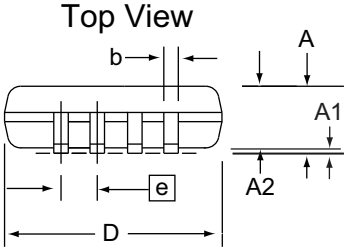
Atmel Package Drawing Contact: packagedrawings@atmel.com	**TITLE** 8S1, 8-lead (0.150” Wide Body), Plastic Gull Wing Small Outline (JEDEC SOIC)	**GPC** SWB	**DRAWING NO.** 8S1	**REV.** G

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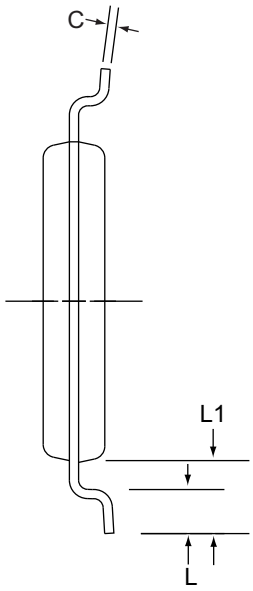
11.2 8X — 8-lead TSSOP



Top View



Side View



End View

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-153, Variation AA, for proper dimensions, tolerances, datums, etc.
2. Dimension D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15mm (0.006in) per side.
3. Dimension E1 does not include inter-lead Flash or protrusions. Inter-lead Flash and protrusions shall not exceed 0.25mm (0.010in) per side.
4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07mm.
5. Dimension D and E1 to be determined at Datum Plane H.

COMMON DIMENSIONS
(Unit of Measure = mm)

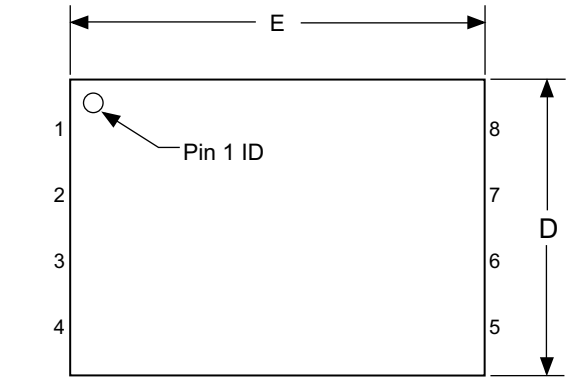
SYMBOL	MIN	NOM	MAX	NOTE
A	-	-	1.20	
A1	0.05	-	0.15	
A2	0.80	1.00	1.05	
D	2.90	3.00	3.10	2, 5
E		6.40 BSC		
E1	4.30	4.40	4.50	3, 5
b	0.19	0.25	0.30	4
e		0.65 BSC		
L	0.45	0.60	0.75	
L1		1.00 REF		
C	0.09	-	0.20	

2/27/14

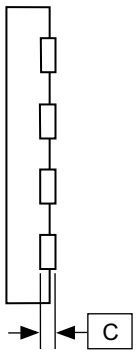
Atmel Package Drawing Contact: packagedrawings@atmel.com	TITLE 8X, 8-lead 4.4mm Body, Plastic Thin Shrink Small Outline Package (TSSOP)	GPC TNR	DRAWING NO. 8X	REV. E

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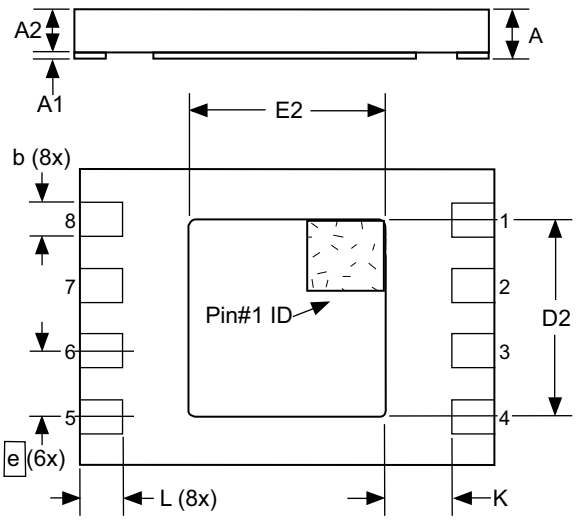
11.3 8MA2 — 8-pad UDFN



TOP VIEW



SIDE VIEW



BOTTOM VIEW

Notes:
1. This drawing is for general information only. Refer to Drawing MO-229, for proper dimensions, tolerances, datums, etc.
2. The Pin #1 ID is a laser-marked feature on Top View.
3. Dimensions b applies to metallized terminal and is measured between 0.15 mm and 0.30 mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension should not be measured in that radius area.
4. The Pin #1 ID on the Bottom View is an orientation feature on the thermal pad.

COMMON DIMENSIONS
(Unit of Measure = mm)

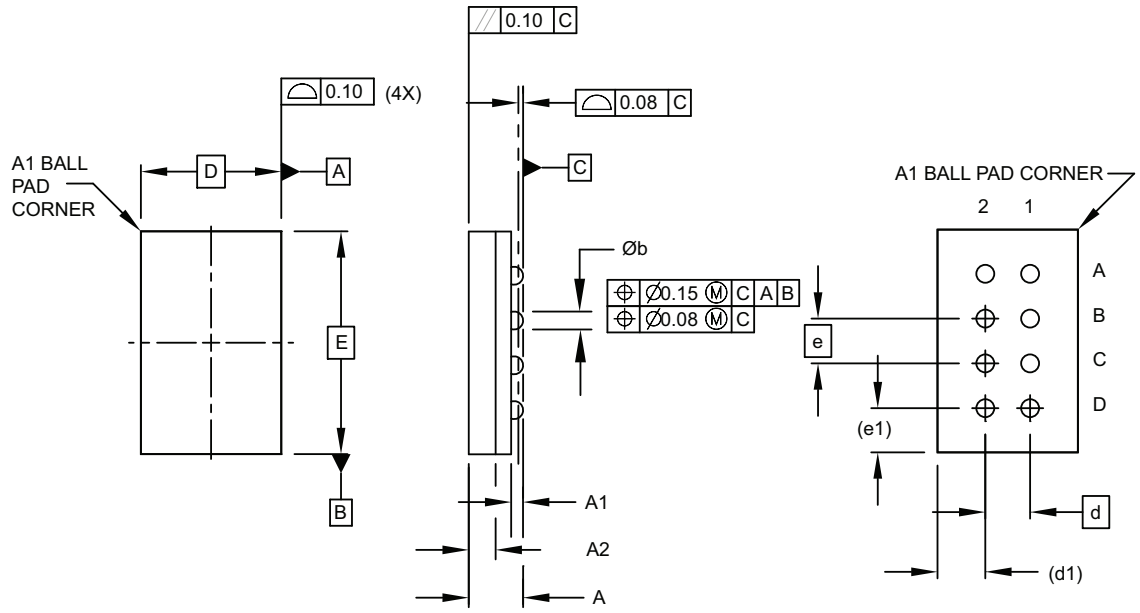
SYMBOL	MIN	NOM	MAX	NOTE
A	0.50	0.55	0.60	
A1	0.0	0.02	0.05	
A2	-	-	0.55	
D	1.90	2.00	2.10	
D2	1.20	-	1.60	
E	2.90	3.00	3.10	
E2	1.20	-	1.60	
b	0.18	0.25	0.30	3
C	1.52 REF			
L	0.30	0.35	0.40	
e	0.50 BSC			
K	0.20	-	-	

6/6/14

Atmel Package Drawing Contact: packagedrawings@atmel.com	**TITLE** 8MA2, 8-pad 2 x 3 x 0.6mm Body, Thermally Enhanced Plastic Ultra Thin Dual Flat No-Lead Package (UDFN)	**GPC** YNZ	**DRAWING NO.** 8MA2	**REV.** F

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11.4 8U2-1 — 8-ball VFBGA



TOP VIEW SIDE VIEW BOTTOM VIEW

8 SOLDER BALLS

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.81	0.91	1.00	
A1	0.15	0.20	0.25	
A2	0.40	0.45	0.50	
b	0.25	0.30	0.35	
D	2.35 BSC			
E	3.73 BSC			
e	0.75 BSC			
e1	0.74 REF			
d	0.75 BSC			
d1	0.80 REF			

Notes:

1. This drawing is for general
2. Dimension 'b' is measured at the maximum solder ball diameter.
3. Solder ball composition shall be 95.5Sn-4.0Ag-.5Cu.

6/11/13

Atmel Package Drawing Contact: packagedrawings@atmel.com	TITLE 8U2-1, 8-ball, 2.35 x 3.73 mm Body, 0.75 mm pitch, Very Thin, Fine-Pitch Ball Grid Array Package (VFBGA)	GPC GWW	DRAWING NO. 8U2-1	REV. G

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12. Revision History

Doc. Rev.	Date	Comments
8698D	07/2014	Update part markings, 8MA2 and 8U2-1 package drawings, package 8A2 to 8X, template, logos, and disclaimer page. No change to functional specification.
8698C	08/2011	Update 8A2 and 8S1 package drawings. Correct page 13, Device Density from 156K to 256K. Correct page 9, table headings. Correct cross references on pages 7, 8, and 9.
8698B	03/2010	Update Catalog Numbering Scheme. Update Ordering Information and package types.
8698A	12/2009	Initial document release.

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