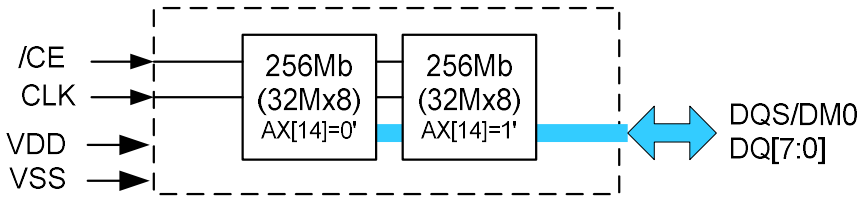
# Double-Data-Rate OPI/HPI Xccela PSRAM

## Specifications

- **Single Supply Voltage:**
  - $V_{DD}$ =1.62 to 1.98V
  - $V_{DDQ}$ =1.62 to 1.98V
- **Interface:** Octal Peripheral interface (OPI) and Hexadecimal Peripheral interface (HPI) with Xccela mode:
  - Two bytes transfer per clock –X8
  - Two words transfer per clock – X16
  - Mode register configurable X8(default)/X16
  - Note: 1 Word = 2 Bytes in this document.
- **Performance:** Clock rate up to 250MHz, 500MBps read/write throughput – X8 1000MBps read/write throughput – X16
- **Organization:** 512Mb in X8 mode (default)
  - 64M x 8bits with 2048 bytes per page
  - Column address: AY0 to AY10
  - Row address: AX0 to AX14
- **Organization:** 512Mb in X16 mode
  - 32M x 16bits with 1024 Words per page
  - Column address: AY0 to AY9
  - Row address: AX0 to AX14
- **Refresh:** Self-managed
- **Operating temperature range**
  - $T_{OPER}$ = -40°C to +85°C (standard range)
  - $T_{OPER}$ = -40°C to +105°C (extended range)
- **Typical Standby Current:**
  - 80µA @ 25°C (Halfsleep™ Mode with data retained)
- **Maximum Standby Current:**
  - 2200µA @ 105°C
  - 1360µA @ 85°C

## Features

- **Low Power Features:**
  - Partial Array Self-Refresh (PASR)
  - Auto Temperature Compensated Self-Refresh (ATCSR) self-managed by a built-in temperature sensor
  - Ultra Low Power Halfsleep™ mode with data retention.
- **Software reset**
- **Output driver LVCMOS** with programmable drive strength
- **Data mask (DM)** for write operation
- **Data strobe (DQS)** for high speed read operation
- Register configurable write and read latencies
- **Write burst length**
  - max 2048 Bytes in X8/1024 Words in X16
  - min 2 Bytes in X8 /2 Words in X16
- **Wrap & hybrid burst in**
  - 16/32/64/128/2K Bytes length in X8 mode.
  - 16/32/64/128/1K Words length in X16 mode.
- **Linear Burst Commands**
- **Row Boundary Crossing (RBX)** read operations enabled via Mode Register
- X16 mode can be configured by setting MR8[6]=1 (default is X8 mode and MR8[6]=0)




Block Diagram


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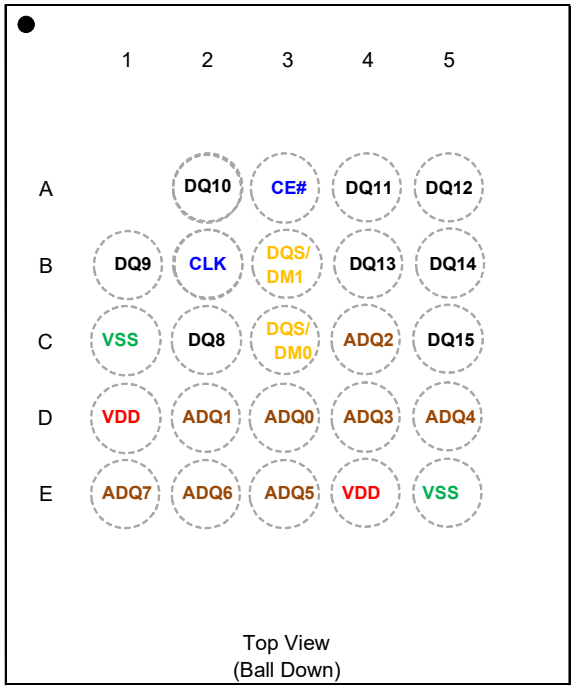
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# 2 Package Information

## 2.1 Package Types : BGA 24B X8/X16 (BG)

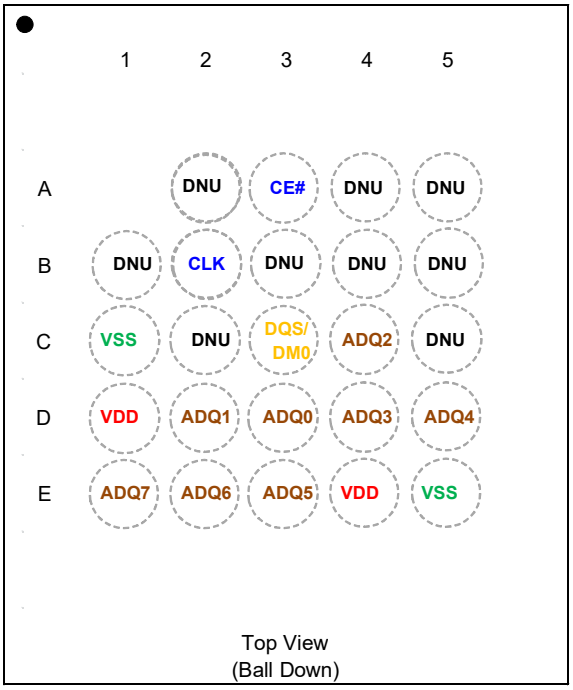
The APS512XXN-OB9 is available in mini-BGA 24B package 6 x 8 x 1.2mm, ball pitch 1.0mm, ball size 0.4mm, package code “BG”.

- Ball Assignment for MINI-BGA 24B




(6x8x1.2mm)(P1.0)(B0.4)

Note: Part Number APS512XXN-OB9-BG for 512Mb




(6x8x1.2mm)(P1.0)(B0.4)

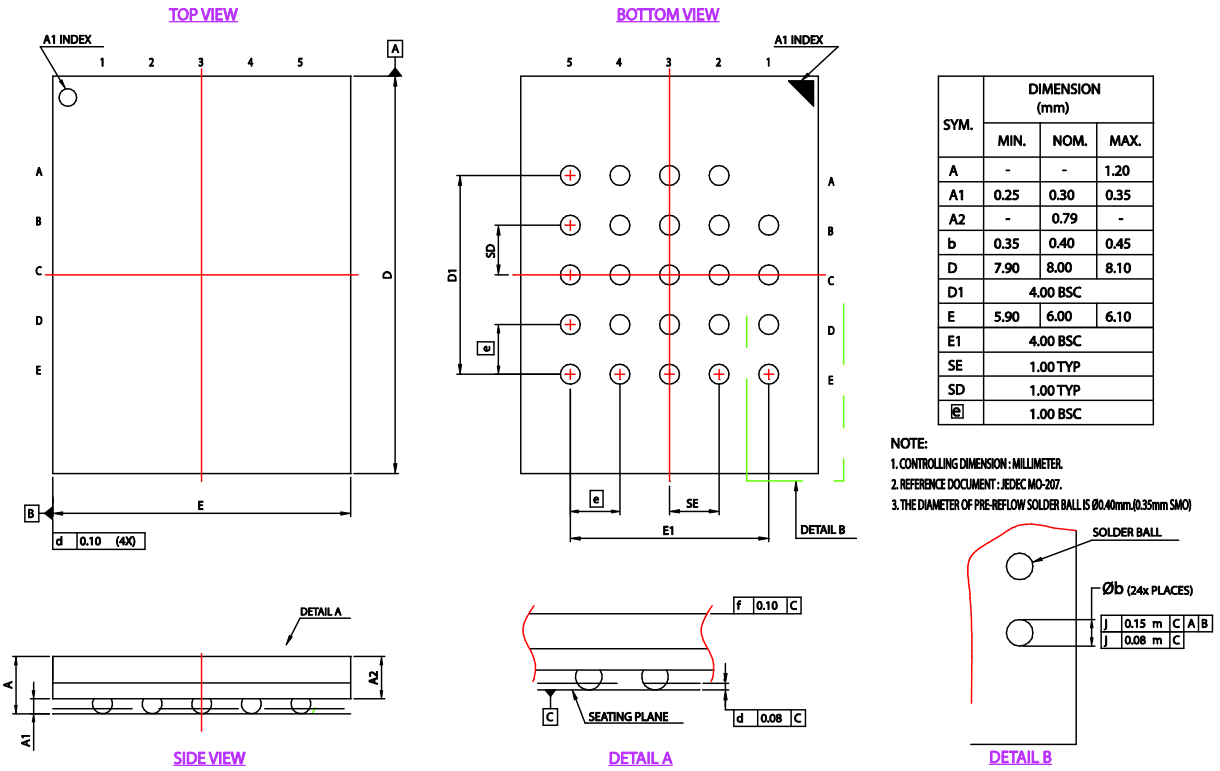
Note: Ball out of X8 mode only in Part Number APS512XXN-OB9-BG for 512Mb
DNU: Do Not Use for X8 mode only


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## 2.2 Package Outline Drawing

### 2.2.1 BGA 24B , package code BG




| SYM. | DIMENSION (mm) | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | - | - | 1.20 |
| A1 | 0.25 | 0.30 | 0.35 |
| A2 | - | 0.79 | - |
| b | 0.35 | 0.40 | 0.45 |
| D | 7.90 | 8.00 | 8.10 |
| D1 | | 4.00 BSC | |
| E | 5.90 | 6.00 | 6.10 |
| E1 | | 4.00 BSC | |
| SE | | 1.00 TYP | |
| SD | | 1.00 TYP | |
| e | | 1.00 BSC | |

NOTE:
1. CONTROLLING DIMENSION : MILLIMETER.
2. REFERENCE DOCUMENT : JEDEC MO-207.
3. THE DIAMETER OF PRE-REFLOW SOLDER BALL IS Ø0.40mm.(0.35mm SMO)


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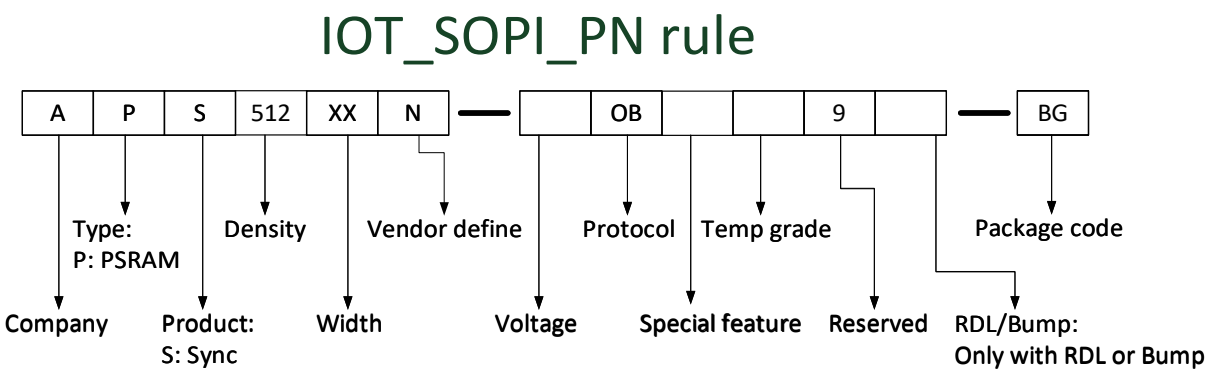
# 3 Ordering Information

**Table 1: Ordering Information**

| *Part Number* | *IO* | *Temperature Range* | *Max Frequency* | *Note* |
|---|---|---|---|---|
| APS512XXN-OB9-BG | X8/X16 | Tc=-40°C to +85°C | 250 MHz | BGA 24B |
| APS512XXN-OBX9-BG | X8/X16 | Tc=-40°C to +105°C | 250 MHz | BGA 24B |

Note for "x"

- -OB9 is standard part for normal temperature grade





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# 4 Signal Table

All signals are listed in Table 2.

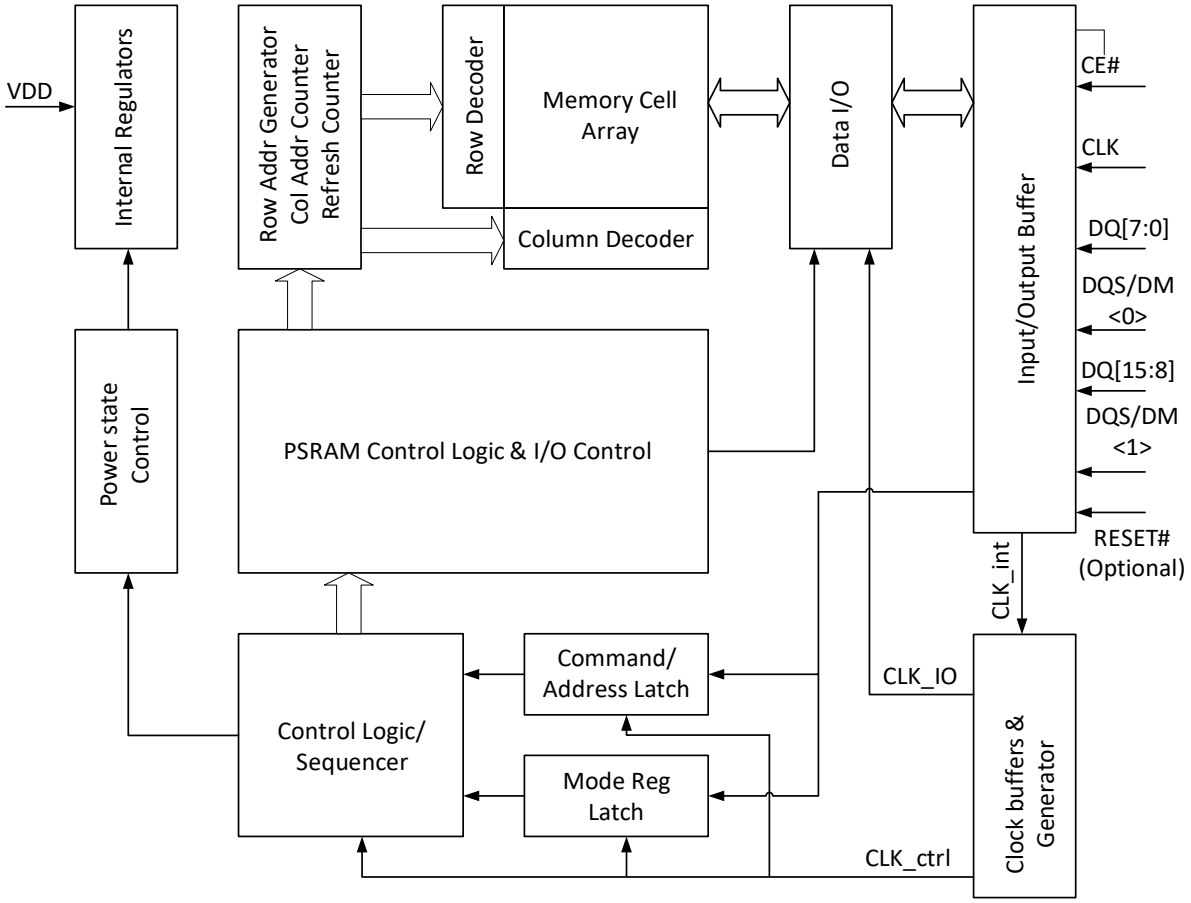
**Table 2: Signals Table**

| *Symbol* | *Type* | *Description* | *Comments* |
|---|---|---|---|
| $V_{DD}$ | Power | Core & IO supply 1.8V | $V_{DDQ}$ short to $V_{DD}$ internally. |
| $V_{SS}$ | Ground | Core& IO supply ground | |
| A/DQ[7:0] | IO | Address/Data bus [7:0] | Used in X8 and X16 |
| DQ[15:8] | IO | Data bus [15:8] | Used in X16 only |
| DQS/DM<0> | IO | DQ strobe clock for DQ[7:0] during all reads, Data mask for DQ[7:0] during memory writes. DM is active high. DM=1 means “do not write”. | Used in X8 and X16 |
| DQS/DM<1> | IO | DQ strobe clock for DQ[15:8] during memory reads, Data mask for DQ[15:8] during memory writes. DM is active high. DM=1 | Used in X16 only |
| CE# | Input | Chip select, active low. When CE#=1, chip is in standby state. | |
| CLK | Input | Input clock | |


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# 5 Block diagram





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# 6 Power-Up Initialization

Octal DDR products include an on-chip voltage sensor used to start the self-initialization process. $V_{DD}$ and $V_{DDQ}$ must be applied simultaneously. When they reach a stable level at or above minimum $V_{DD}$, the device is in Phase 1 and it requires 150µs to complete its self-initialization process. System host can then proceed to Phase 2 of the initialization described in section 6.1.

During Phase 1 CE# should remain HIGH (track $V_{DD}$ within 200mV); CLK should remain LOW.

After Phase 2 is complete the device is ready for operation, however Halfsleep™ entry and Deep Power Down (DPD) entry are not available until Halfsleep™ Power Up (tHSPU) or DPD Power Up (tDPDp) durations are observed.

## *6.1 Power-Up Initialization Method (via. Global Reset)*

As an alternate power-up initialization method, after the Phase 1 150µs period the Global Reset command can also be used to reset the device in Phase 2 as follows:

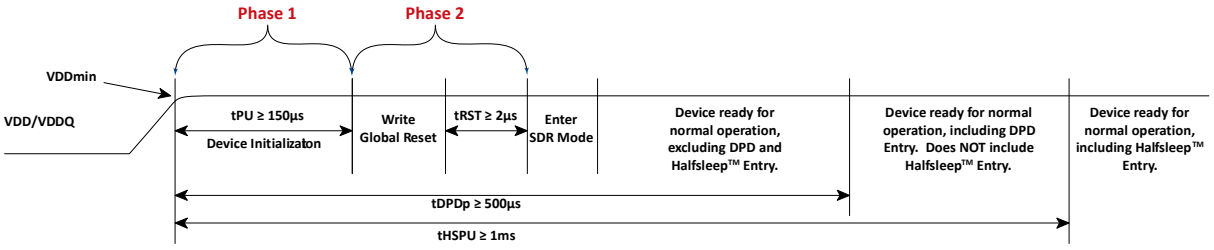



**Figure 1. Power-Up Initialization Method Timing with Global Reset**

The Global Reset command resets all register contents. Memory content is not guaranteed. The command frame is made of 4 clocked CE# lows. Clocking is optional during tRST. The Global Reset command sequence is shown below.

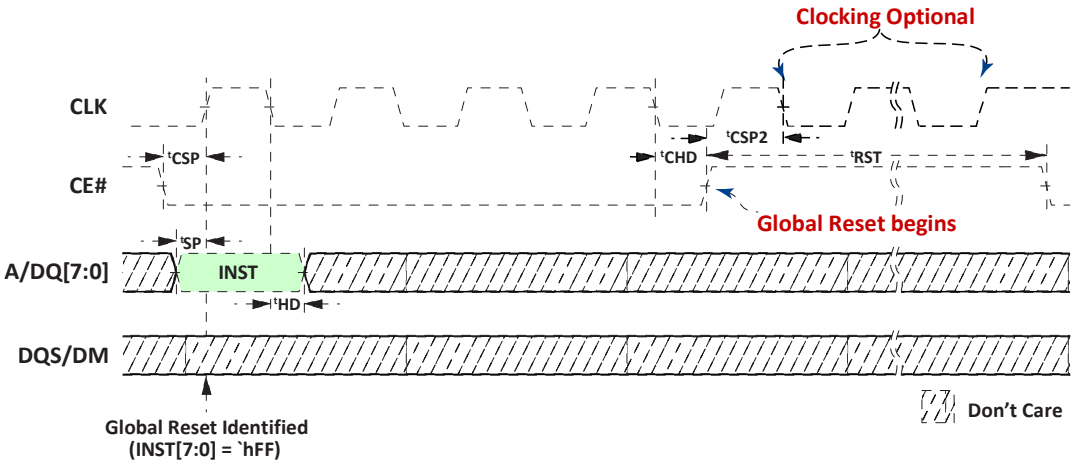



**Figure 2: Global Reset**


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# 7 Interface Description

## 7.1 Address Space

Octal DDR PSRAM device is byte-addressable(X8)/word-addressable(X16). Memory accesses must start on even addresses (A[0]='0). Mode Register accesses can start on even or odd address.

## 7.2 Burst Type & Length

Read and write operations are default Hybrid Wrap 32 mode. Other burst lengths of 16, 32, 64 or 2K bytes in standard or Hybrid wrap modes are register configurable (16, 32, 64 and 1K words configurable in X16 mode). The device also includes command burst options for Linear Bursting (see Table 20). Bursts can start on any even address. Write burst length requires a minimum of 2 bytes(X8)/2 words (X16). Read has no minimum length. Both write and read have no restriction on maximum burst length as long as tCEM is met.

## 7.3 Command/Address Latching

After CE# goes LOW, instruction code is latched on 1st CLK rising edge. Access address is latched on the 3rd, 4th, 5th & 6th CLK edges (2nd CLK rising edge, 2nd CLK falling edge, 3rd CLK rising edge, 3rd CLK falling edge).

## 7.4 Command Truth Table

The Octal DDR PSRAM recognizes commands listed in the following table. Instruction and address are input through A/DQ[7:0] pins. Host must send correct instruction and address format according to the following table.

Note that CA[10] is only used in X8 mode and it is ignored in X16 mode.
Note that Linear Burst commands, 20h and A0h, ignore burst setting defined by MR8[2:0].
Note that only Linear Burst Read command is capable of performing row boundary crossing (RBX) read function.

| | 1st CLK | | 2nd CLK | | 3rd CLK | |
|---|---|---|---|---|---|---|
| **Command** | | | | | | |
| Sync Read | 00h | | A3 | A2 | A1 | A0 |
| Sync Write | 80h | | A3 | A2 | A1 | A0 |
| Linear Burst Read | 20h | | A3 | A2 | A1 | A0 |
| Linear Burst Write | A0h | | A3 | A2 | A1 | A0 |
| Mode Register Read | 40h | | × | | | MA |
| Mode Register Write | C0h | | × | | | MA |
| Global Reset | FFh | | × | | | |

Remarks:
× = don't care ($V_{IH}$/$V_{IL}$)
A3 = 7'bx, RA[13] {unused address bits are reserved}
A2 = RA[12:5]
A1 = RA[4:0],CA[10:8] { CA[10] is used only in X8 mode}
A0 = CA[7:0]
MA = Mode Register Address


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## 7.5 Read Operation

After address latching, the device initializes DQS/DM to '0 from CLK rising edge of the 3rd clock cycle (A1). See Figure 3 below.

Output data is available after LC latency cycles, as shown in Figure 5 & Figure 6. LC is latency configuration code defined in Table 5 and Table 6. When data is valid, A/DQ[7:0] and DQS/DM follow the timing specified in Figure 7. Synchronous timing parameters are shown in Table 30 & Table 31. CE# should be kept low until the last byte of data has been received by the host.

In case of internal refresh insertion, variable latency output data may be delayed by **up to** (LCx2) latency cycles as shown in Figure 5. True variable refresh pushout latency can be anywhere **between** LC to LCx2. The 1st DQS/DM rising edge after read pre-amble indicates the beginning of valid data.

In X16 mode DQ [15:8] will not receive INST/ADD, instead they will remain Hi-Z until read latency and then start pumping out data, similar to DQ [7:0].

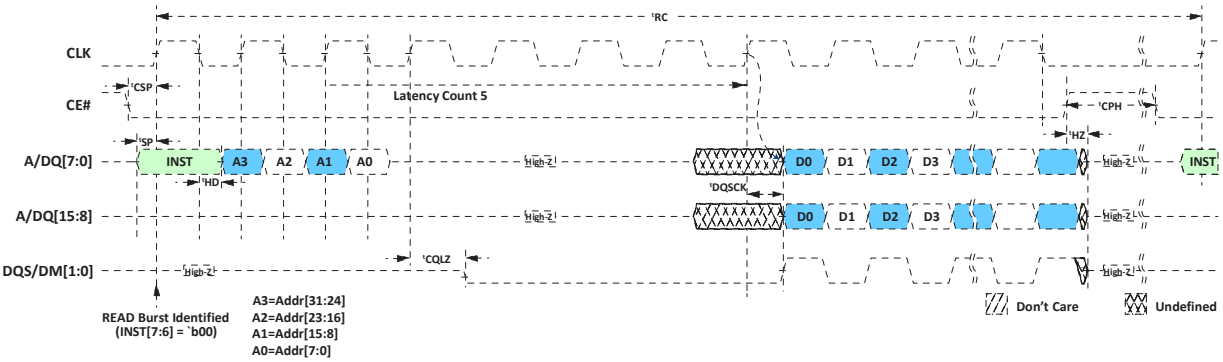



**Figure 3: Synchronous Read**

If RBX is enabled (MR8[3] written to 1) and a Linear Burst Read Command ('h20) is issued, read operation may cross row boundaries as shown in Figure 4.

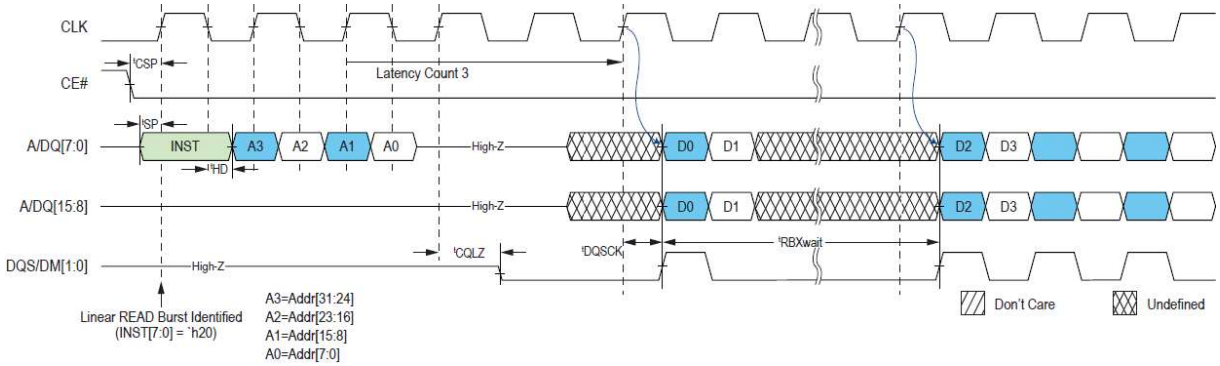



**Figure 4: Linear Burst Read with RBX (Starting address '7FE in X8 mode and '3FE in X16 mode)**


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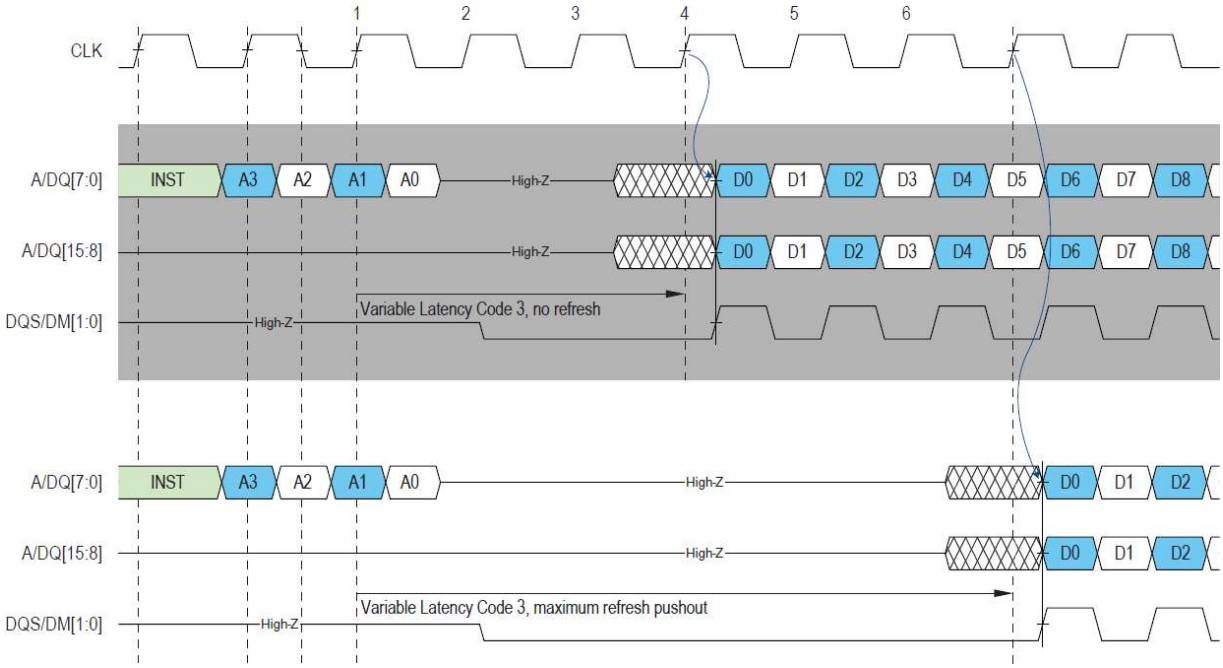



**Figure 5: Variable Read Latency Refresh Pushout**

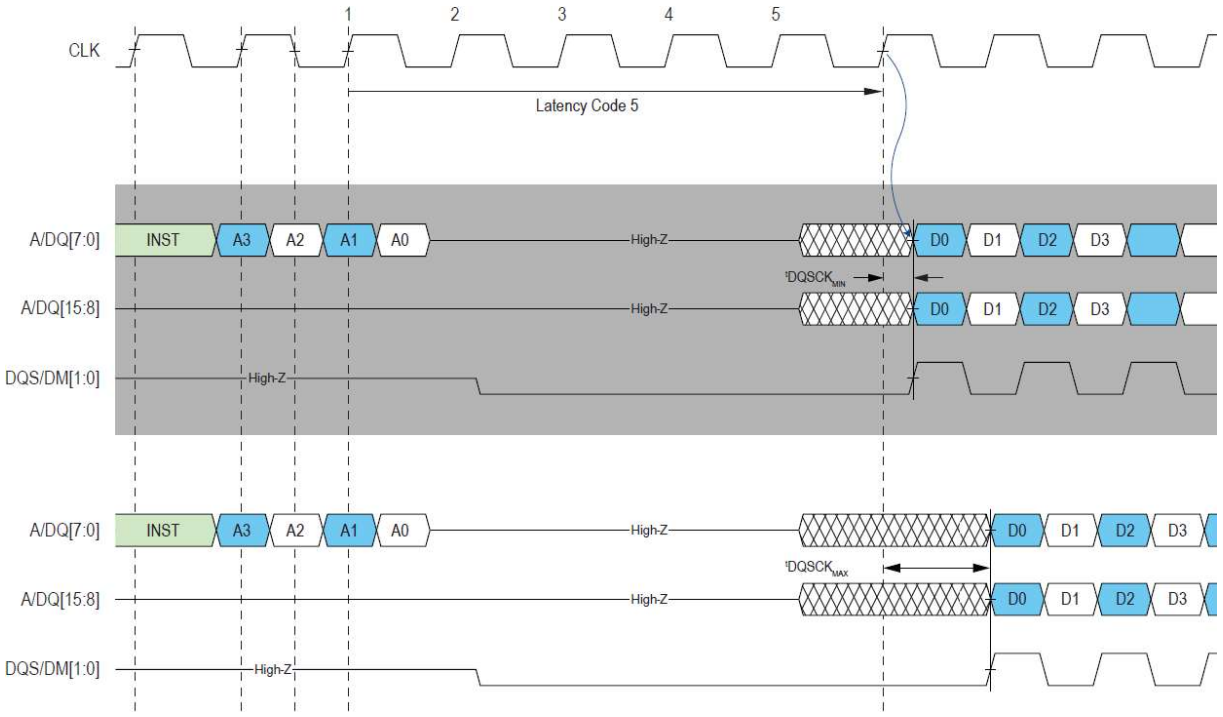



**Figure 6: Read Latency & tDQSCK**


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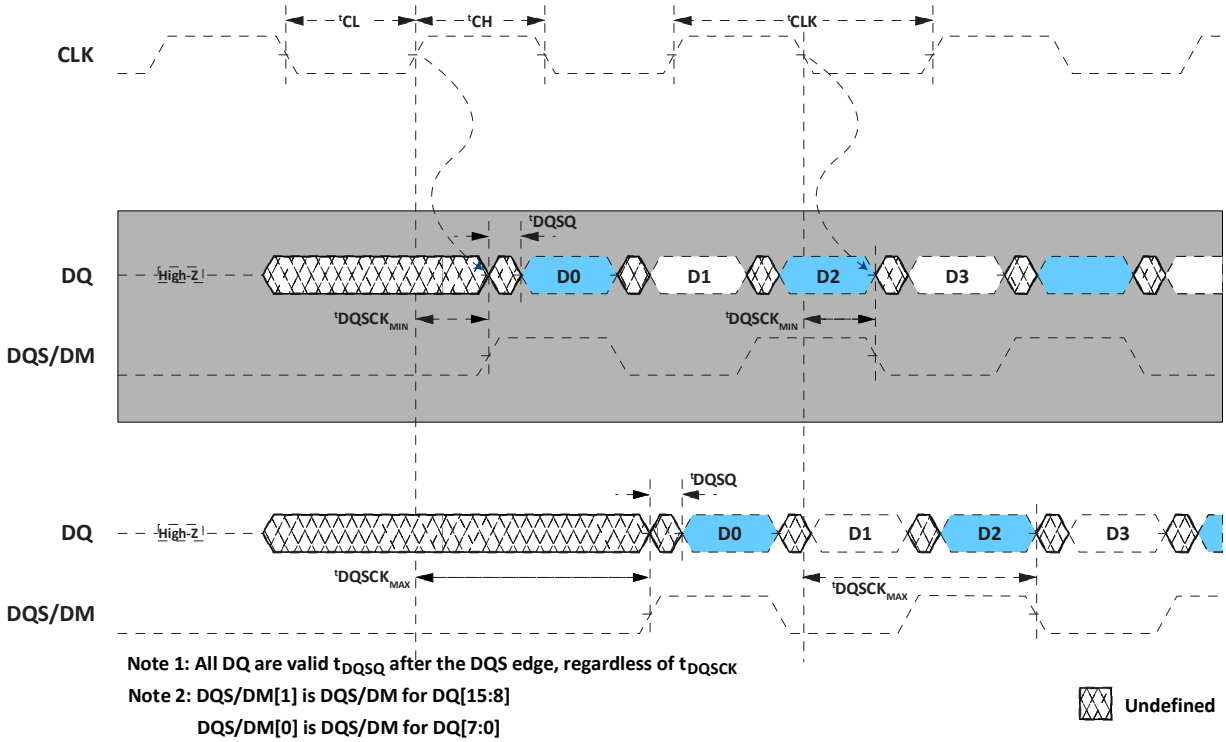



**Figure 7: Read DQS/DM & DQ timing**


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## 7.6 Write Operation

A minimum of 2 bytes (in X8 mode) / 2words (in X16 mode) of data must be input in a write operation. In the case of consecutive short burst writes, tRC must be met by issuing additional CE# high time between operations. Single-byte write operations can be done by masking through DQS/DM pin as shown in Figure 8.

In X16 mode DQ[15:8] are ignored during INST/ADDR cycles. Instead, DQ[15:8] are only used after write latency to receive the data, similar to DQ[7:0]. During write data cycles the DQ[15:8] and DQ[7:0] can be independently masked via DM[1] and DM[0].

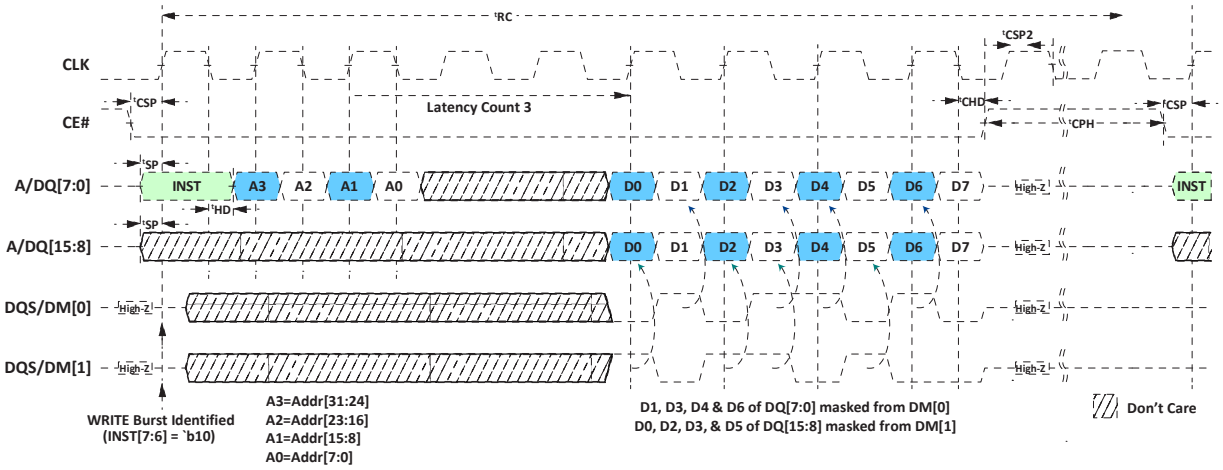



**Figure 8: Synchronous Write followed by any Operation**

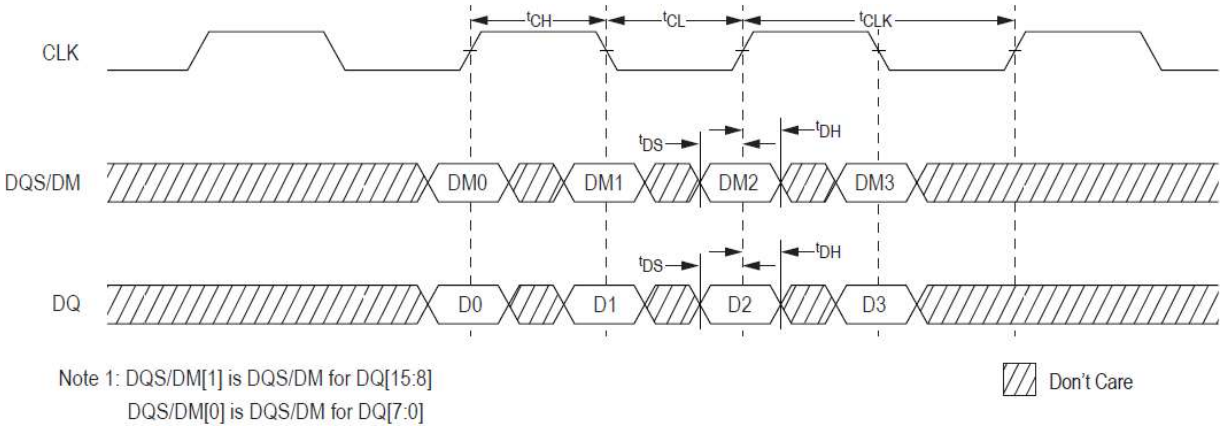


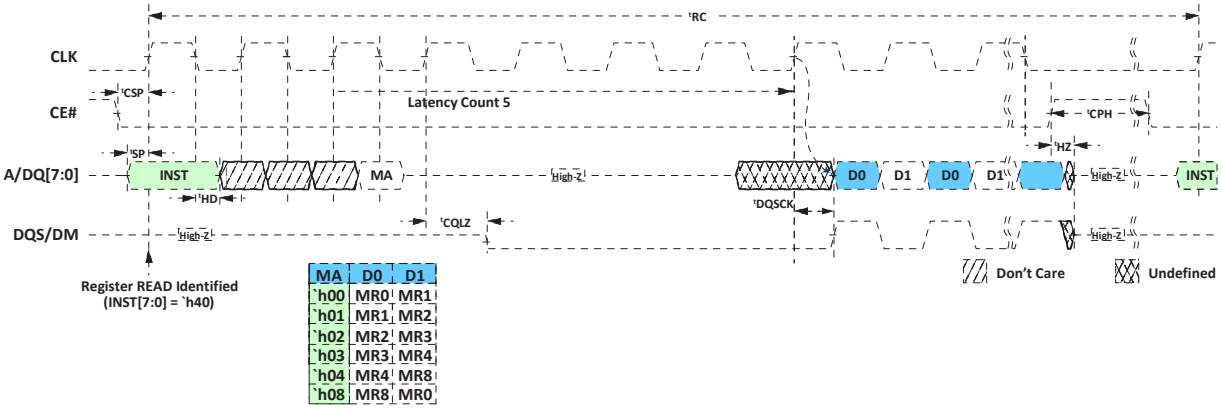

**Figure 9: Write DQS/DM & DQ Timing**


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## 7.7 Control Registers

Register Read is shown below. Mode Address in command determines which Mode Register is read from as Data0 (see chart in the Figure below). All Mode Registers are 8-bit wide, Mode register write and read uses only A/DQ[7:0] even in X16 mode.




| MA | D0 | D1 |
|---|---|---|
| `h00 | MR0 | MR1 |
| `h01 | MR1 | MR2 |
| `h02 | MR2 | MR3 |
| `h03 | MR3 | MR4 |
| `h04 | MR4 | MR8 |
| `h08 | MR8 | MR0 |

**Figure 10: Register Read**

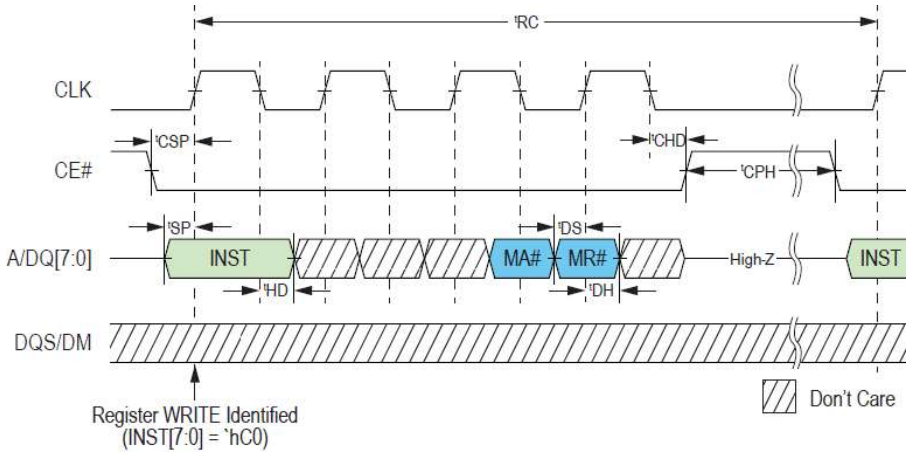



**Figure 11: Register Write**

Register Writes are always latency 1. Write Latency Code, MR4[7:5] does not apply to Register writes. Register Reads follow the same read latency settings, defined in MR0[4:2] (see Table 6).

Registers 0, 4 & 8 are read and writable. Registers 1, 2 and 3 are read-only. Register 6 is write-only.

Register mapping is shown in Table 3. All MR0 or MR8 writes must have MR0[7:6] or MR8[7] written to `0(s).


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**Table 3: Mode Register Table**

| MR No. | MA[7:0] | Access | OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | `h00 | R/W | '00' | | LT | Read Latency Code | | | Drive Str. | |
| 1 | `h01 | R | ULP | rsvd. | | Vendor ID | | | | |
| 2 | `h02 | R | KGD | | | Dev ID | | Density | | |
| 3 | `h03 | R | RBXen | 0 | SRF | | rsvd. | | | |
| 4 | `h04 | R/W | Write Latency Code | | | RF rate | | PASR | | |
| 6 | `h06 | W | Halfsleep™ | | | | rsvd. | | | |
| 8 | `h08 | R/W | '0' | x8/x16 | rsvd | | RBX | BT | BL | |

**Table 4: Read Latency Type MR0[5]**

| Latency Type | |
|---|---|
| MR0[5] | LT |
| 0 | Variable (default) |
| 1 | Fixed |

**Table 5: Read Latency Codes MR0[5:2]**

| | VL Codes (MR0[5]=0) | | FL Codes (MR0[5]=1) | Max Input CLK Freq (MHz) | | Note |
|---|---|---|---|---|---|---|
| MR0[4:2] | Latency | Max push out | Latency | Standard | Extended | |
| 001 | 4 | 8 | 8 | 66 | 66 | |
| 010 | 5 (default) | 10 | 10 | 109 | 109 | |
| 011 | 6 | 12 | 12 | 133 | 133 | |
| 100 | 7 | 14 | 14 | 166 | 166 | |
| 101 | 9 | 16 | 16 | 200 | 200 | |
| 110 | 10 | 18 | 18 | 225 | 225 | 1 |
| 111 | 11 | 19 | 19 | 250 | 250 | 1 |

Note 1: The RBX function cannot be used when MR0[4:2] is set to 101 or 110

**Table 6: Operation Latency Code Table**

| Type | Operation | VL (default) | | FL |
|---|---|---|---|---|
| | | No Refresh | Refresh | |
| Memory | Read | LC | Max push out | FLC |
| | Write | WLC | | WLC |
| Register | Read | LC | | LC |
| | Write | 1 | | 1 |

*Note: see Table 15 for WLC settings.


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**Table 7: Drive Strength Codes MR0[1:0]**

| *Codes* | *Drive Strength* |
|---|---|
| ‘00 | Full (25Ω default) |
| ‘01 | Half (50Ω) |
| ‘10 | 1/4 (100Ω) |
| ‘11 | 1/8 (200Ω) |

**Table 8: Ultra Low Power Device mapping MR1[7]**

| *ULP* | |
|---|---|
| ‘0 | Non-ULP (no Halfsleep™) |
| ‘1 | ULP (Halfsleep™ supported) |

**Table 9: Vendor ID mapping MR1[4:0]**

| *Vendor ID* |
|---|
| 01101: APM |

**Table 10: Good-Die Bit MR2[7:5]***

| *Codes* | *Good Die ID* |
|---|---|
| ‘110 | PASS |
| others | FAIL |

*Note: Default is FAIL die, and only mark PASS after all tests passed.

**Table 11: Device ID MR2[4:3]**

| *Codes* | *Device ID* |
|---|---|
| ‘00 | Generation 1 |
| ‘01 | Generation 2 |
| ‘10 | Generation 3 |
| ‘11 | Generation 4 (default) |

**Table 12: Device Density mapping MR2[2:0]**

| *MR2[2:0]* | *Density* |
|---|---|
| ‘001 | 32Mb |
| ‘011 | 64Mb |
| ‘101 | 128Mb |
| ‘111 | 256Mb (default) |
| ‘110 | 512Mb |
| others | reserved |


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**Table 13: Row Boundary Crossing Enable MR3[7]**

| *MR3[7] (read-only)* | *RBXen* |
|---|---|
| 0 | RBX not supported |
| 1 | RBX supported via MR8[3]=1 |

**Table 14: Self Refresh Flag MR3[5:4]**

MR3[5:4] indicates current device refresh rate. Refresh rate depends on temperature and refresh frequency configuration, set by MR4[4:3].

| *MR3[5:4] (read-only)* | *Self Refresh Flag* |
|---|---|
| 01 | 0.5x Refresh |
| 00 | 1x Refresh |
| 10 | 4x Refresh |
| 11 | reserved |

**Table 15: Write Latency MR4[7:5]**

Write latency, WLC, is default to 5 after power up. Use MR Write to set write latencies according to write latency table. When operating frequency exceeding Fmax listed in the table will result in write data corruption.

| *MR4[7:5]* | *Write Latency Codes (WLC)* | *Fmax (MHz)* |
|---|---|---|
| 000 | 3 | 66 |
| 100 | 4 | 109 |
| 010 | 5 (default) | 133 |
| 110 | 6 | 166 |
| 001 | 7 | 200 |
| 101 | 8 | 225 |
| 011 | 9 | 250 |

**Table 16: Refresh Frequency setting MR4[4:3]**

| *MR4[4:3]* | *Refresh Frequency* |
|---|---|
| x0 | Always 4x Refresh (default) |
| 01 | Enables 1x Refresh when temperature allows |
| 11 | Enable 0.5x Refresh when temperature allows |

Note: x= don't care


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**Table 17: PASR MR4[2:0]**

The PASR bits restrict refresh operation to a portion of the total memory array. This feature allows the device to reduce standby current by refreshing only that part of the memory array required by the host system. The refresh options are full array, one-half array, one-quarter array, one-eighth array, or none of the array. The mapping of these partitions can start at either the beginning or the end of the address map.

Address Space: RA [13:0], CA [10:0] note: CA [10] is ignored in X16 mode.

| *512Mb X8* | | | | |
|---|---|---|---|---|
| ***Codes*** | ***Refresh Coverage*** | ***Address Space*** | ***Size*** | ***Density*** |
| ‘000 | Full array (default) | 0000000h-3FFFFFFh | 64M X8 | 512Mb |
| ‘001 | Bottom 1/2 array | 0000000h-1FFFFFFh | 32M X8 | 256Mb |
| ‘010 | Bottom 1/4 array | 0000000h-0FFFFFFh | 16M X8 | 128Mb |
| ‘011 | Bottom 1/8 array | 0000000h-07FFFFFh | 8M X8 | 64Mb |
| ‘100 | None | 0 | 0M | 0Mb |
| ‘101 | Top 1/2 array | 2000000h-3FFFFFFh | 32M X8 | 256Mb |
| ‘110 | Top 1/4 array | 3000000h-3FFFFFFh | 16M X8 | 128Mb |
| ‘111 | Top 1/8 array | 3800000h-3FFFFFFh | 8M X8 | 64Mb |

| *512Mb X16* | | | | |
|---|---|---|---|---|
| ***Codes*** | ***Refresh Coverage*** | ***Address Space*** | ***Size*** | ***Density*** |
| ‘000 | Full array (default) | 0000000h-1FFFFFFh | 32M X16 | 512Mb |
| ‘001 | Bottom 1/2 array | 0000000h-0FFFFFFh | 16M X16 | 256Mb |
| ‘010 | Bottom 1/4 array | 0000000h-07FFFFFh | 8M X16 | 128Mb |
| ‘011 | Bottom 1/8 array | 0000000h-03FFFFFh | 4M X16 | 64Mb |
| ‘100 | None | 0 | 0M | 0Mb |
| ‘101 | Top 1/2 array | 1000000h-1FFFFFFh | 16M X16 | 256Mb |
| ‘110 | Top 1/4 array | 1800000h-1FFFFFFh | 8M X16 | 128Mb |
| ‘111 | Top 1/8 array | 1C00000h-1FFFFFFh | 4M X16 | 64Mb |


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**Table 18: Halfsleep™ MR6[7:0]**

| *MR6[7:0]* | *ULP Modes* |
|---|---|
| 'hF0 | Halfsleep™ |
| 'hC0 | Deep Power Down |
| others | reserved |

Note: see 7.8 **HalfsleepTM** Mode; 7.9 Deep Power Down Mode for more information.

**Table 19: IO X8/X16 Mode MR8 [6]**

Device powers up in X8 mode, MR8[6]=0. After power up device can be configured to X16 mode by setting MR8[6]=1 via mode register write command. Host can switch in and out of X16 mode any time after power up.

| *MR8[6]* | *X8/X16 Mode* |
|---|---|
| 0 | X8 (default) |
| 1 | X16 |


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**Table 20: Burst Type MR8[2], Burst Length MR8[1:0]**

By default the device powers up in 32 Byte Hybrid Wrap. In non-Hybrid burst (MR8[2]=0), MR8[1:0] sets the burst address space in which the device will continually wrap within. If Hybrid burst wrap is selected (MR8[2]=1), the device will burst through the initial wrapped burst length once, then continue to burst incrementally up to maximum column address (2K in X8 mode/1K in X16 mode) before wrapping around within the entire column address space. Burst length (MR8[1:0]) can be set to 16,32,64 & 2K in X8 mode (1K in X16 mode) Lengths.

| *MR8[2]* | *MR8[1:0]* | *Burst Length X8/X16 Mode* | *Example of Sequence of Bytes During Wrap* | |
|---|---|---|---|---|
| | | | *Starting* | *Burst Address Sequence in X8 mode* |
| '0 | '00 | 16 Byte/Word Wrap | 4 | [4,5,6,…15,0,1,2,…] |
| '0 | '01 | 32 Byte/Word Wrap | 4 | [4,5,6,…31,0,1,2,…] |
| '0 | '10 | 64 Byte/Word Wrap | 4 | [4,5,6,…63,0,1,2,…] |
| '0 | '11 | 2K Byte/1K Word Wrap | 4 | [4,5,6,…2047,0,1,2,…] |
| '1 | '00 | 16 Byte/Word Hybrid Wrap | 2 | [2,3,4,…15,0,1],16,17,18,…2047,0,1,… |
| '1 | '01 | 32 Byte/Word Hybrid Wrap | 2 | [2,3,4,…31,0,1],32,33,34,…2047,0,1,… |
| '1 | '10 | 64 Byte/Word Hybrid Wrap | 2 | [2,3,4,…63,0,1],64,65,66,…2047,0,1,… |
| '1 | '11 | 2K Byte/1K Word Wrap | 2 | [2,3,4,…2047,0,1,2,…] |

The Linear Burst Commands (INST[5:0]=6'b10_0000) forces the current array read or write command to do 2K Byte Wrap(X8)/1K Word(X16) (equivalent to having MR8[1:0] set to 2'b11). For non-RBX Enabled devices the burst command read/writes linearly from the starting address and wraps back to the beginning of the page upon reaching the end of the page. To access a different page, host must issue a new command.

**Table 21: Row Boundary Crossing Read Enable MR8[3]**

This register setting applies to Linear Burst reads only on RBX enabled devices (MR3[7]=1). Default write and read burst behavior is limited within page (row) address space. In X8 mode column address range is 2K (CA='h000 -> 'h7FF) and it is 1K (CA='h000 -> 'h3FF) in X16 mode. Setting this bit high will allow Linear Burst Read command to cross over into the next Row (RA+1).

| *MR8[3]* | *RBX Read* |
|---|---|
| 0 | Reads stay within page (row) boundary |
| 1 | Allow reads cross page (row) boundary |


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## 7.8 Halfsleep™ Mode

Halfsleep™ Mode puts the device in an ultra-low power state, while the stored data is retained. Halfsleep™ Mode Entry is entered by writing 8'hF0 into MR6. CE# going high initiates the Halfsleep™ mode and must be maintained for the minimum duration of Halfsleep™ time, tHS. The Halfsleep™ Entry command sequence is shown below.

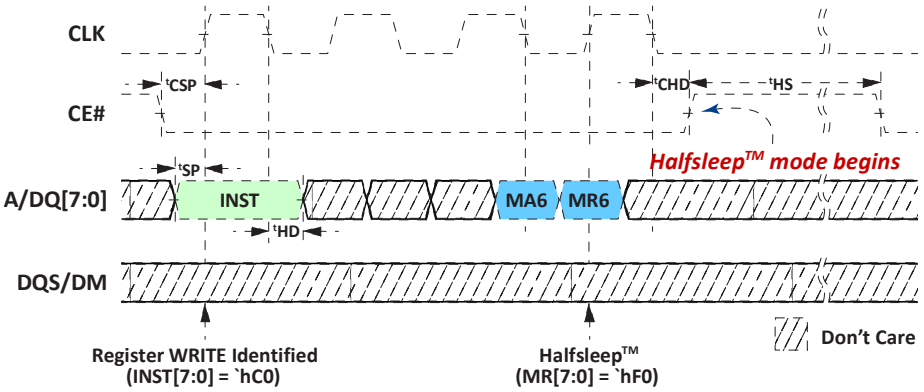



**Figure 12: Halfsleep™ Entry Write (latency same as Register Writes, WL1)**

Halfsleep™ Exit is initiated by a low pulsed CE#. Afterwards, CE# can be held high with or without clock toggling until the first operation begins (observing minimum Halfsleep™ Exit time, tXHS).

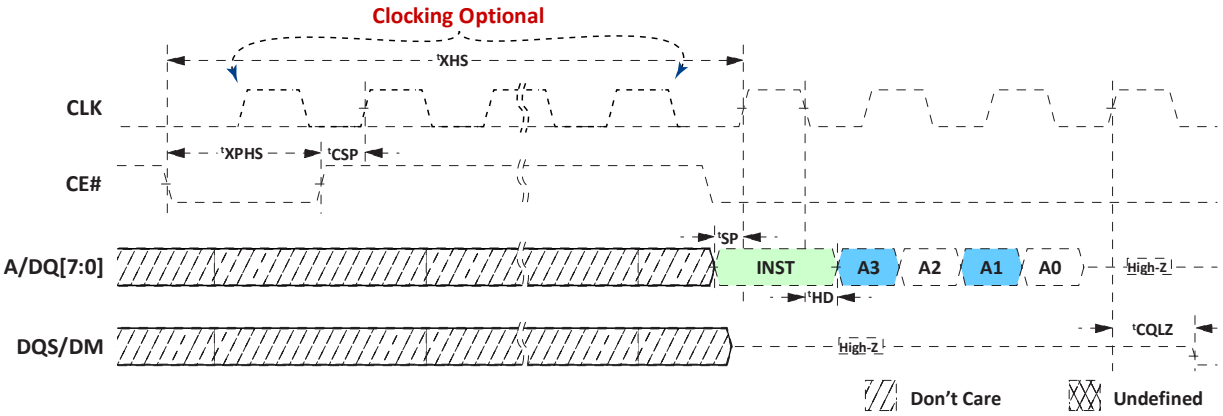



**Figure 13: Halfsleep™ Exit (Read Operation shown as example)**


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## 7.9 Deep Power Down Mode

Deep Power Down Mode (DPD) puts the device into power down state. DPD Mode Entry is entered by writing 8'hC0 into MR6. CE# going high initiates the DPD Mode and must be maintained for the minimum duration of Deep Power Down time, tDPD. The Deep Power Down Entry command sequence is shown below.

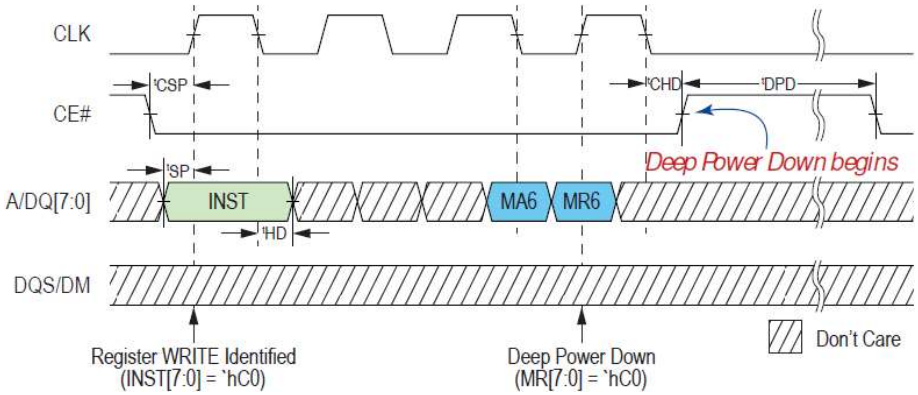



**Figure 14: Deep Power Down Entry**

Deep Power Down Exit is initiated by a low pulsed CE#. After a CE# DPD exit, CE# must be held high with or without clock toggling until the first operation begins (observing minimum Deep Power Down Exit time, tXDPD).

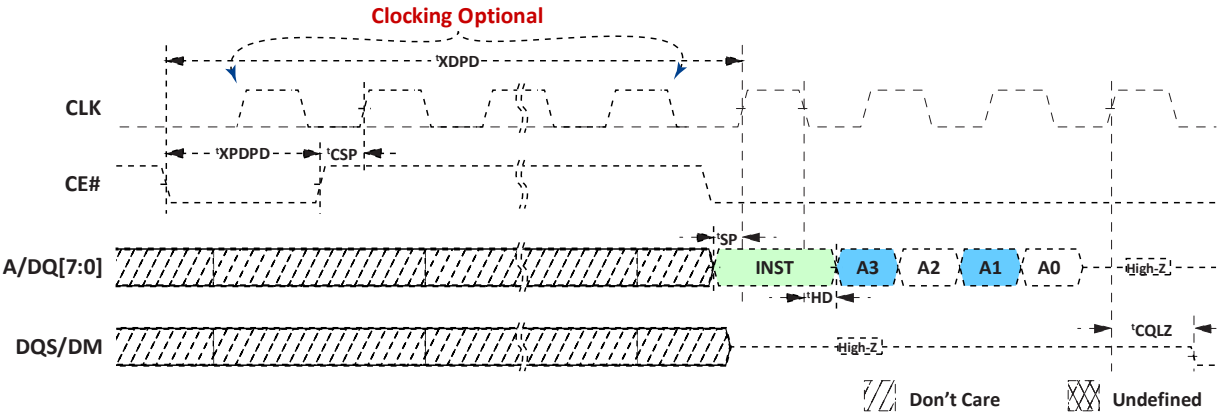



**Figure 15: Deep Power Down Exit (Read Operation shown as example)**

Register values and memory content are not retained in DPD Mode. After DPD mode register values will reset to defaults. tDPDp is minimum period between two DPD Modes (measured from DPD exit to the next DPD entry) as well as from the initial power up to the first DPD entry.


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# 8 Electrical Specifications:

## 8.1 Absolute Maximum Ratings

**Table 22: Absolute Maximum Ratings**

| Parameter | Symbol | Rating | Unit | Notes |
|---|---|---|---|---|
| Voltage to any ball except $V_{DD}$, $V_{DDQ}$ relative to $V_{SS}$ | VT | -0.4 to $V_{DD}$/$V_{DDQ}$+0.4 | V | |
| Voltage on $V_{DD}$ supply relative to $V_{SS}$ | $V_{DD}$ | -0.4 to +2.45 | V | |
| Voltage on $V_{DDQ}$ supply relative to $V_{SS}$ | $V_{DDQ}$ | -0.4 to +2.45 | V | |
| Storage Temperature | $T_{STG}$ | -55 to +150 | °C | 1 |

Notes 1: Storage temperature refers to the case surface temperature on the center/top side of the PSRAM.

Caution:
Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

## 8.2 Pin Capacitance

**Table 23: Bare Die Pin Capacitance**

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Input Pin Capacitance | CIN | | 1 | pF | VIN=0V |
| Output Pin Capacitance | COUT | | 2 | pF | VOUT=0V |

Note: spec'd at 25°C.

**Table 24: Package Pin Capacitance**

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Input Pin Capacitance | CIN | | 5 | pF | VIN=0V |
| Output Pin Capacitance | COUT | | 6 | pF | VOUT=0V |

Note: spec'd at 25°C.

**Table 25: Load Capacitance**

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Load Capacitance | $C_L$ | | 15 | pF | |

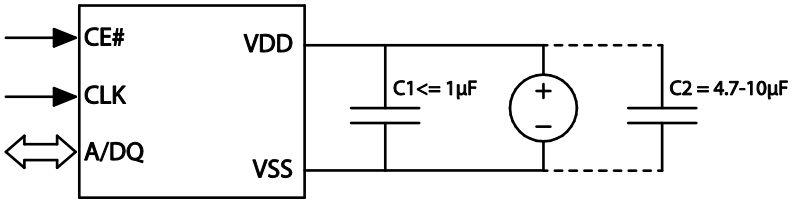
Note: System $C_L$ for the use of package


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## 8.3 Decoupling Capacitor Requirement

System designers need to take care of power integrity considering voltage regulator response and the memory peak currents/usage modes.




### 8.3.1 Low ESR cap C1:

It is recommended to place a low ESR decoupling capacitor of <=1µF close to the device to absorb transient peaks.

### 8.3.2 Large cap C2:

Though Halfsleep™ average current is small (less than 100µA), its peak current from internal periodical burst refresh can reach up to the level of 25mA. The peak current duration can last for few tens of microseconds. During this period if the system regulator cannot supply such large peaks, it is important to place a 4.7µF-10µF cap to cover the burst refresh current demand and replenish the cap before the next burst of refresh.

If needed, contact AP Memory for further decoupling solution assistance.

## 8.4 Operating Conditions

**Table 26: Operating Characteristics**

| Parameter | Min | Max | Unit | Notes |
|---|---|---|---|---|
| Operating Temperature (extended) | -40 | 105 | °C | |
| Operating Temperature (standard) | -40 | 85 | °C | |


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## 8.5 DC Characteristics

**Table 27: DC Characteristics**

| Symbol | Parameter | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage | 1.62 | 1.98 | V | |
| $V_{DDQ}$ | I/O Supply Voltage | 1.62 | 1.98 | V | |
| $V_{IH}$ | Input high voltage | $V_{DDQ}$-0.4 | $V_{DDQ}$+0.3 | V | |
| $V_{IL}$ | Input low voltage | -0.3 | 0.4 | V | |
| $V_{OH}$ | Output high voltage ($I_{OH}$=-0.2mA) | 0.8 $V_{DDQ}$ | | V | |
| $V_{OL}$ | Output low voltage ($I_{OL}$=+0.2mA) | | 0.2 $V_{DDQ}$ | V | |
| $I_{LI}$ | Input Pin leakage current | | 1 | µA | |
| $I_{LO}$ | Output Pin leakage current | | 1 | µA | |
| ICC | Read/Write @13MHz (X8/X16) | | 7.5/9 | mA | 1 |
| | Read/Write @133MHz (X8/X16) | | 28.5/34.5 | mA | 1 |
| | Read/Write @166MHz (X8/X16) | | 33/42 | mA | 1 |
| | Read/Write @200MHz (X8/X16) | | 39/49.5 | mA | 1 |
| | Read/Write @225MHz (X8/X16) | | 43.5/55.5 | mA | 1 |
| | Read/Write @250MHz (X8/X16) | | 48/60 | mA | 1 |
| $ISB_{EXT}$ | Standby current (105C) | | 2200 | µA | 2 |
| $ISB_{STD}$ | Standby current (85C) | | 1360 | µA | 2 |
| $ISB_{STDDPD}$ | Standby current (Deep Power Down - 40°C to 85°C) | | 40 | µA | 3 |

Note 1: Current is only characterized.

Note 2: Without CLK toggling. ISB will be higher if CLK is toggling.

Note 3: Typical mean $ISB_{STDDPD}$ 8uA at 25°C


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## 8.6 ISB Partial Array Refresh Current

**Table 28: Typical-mean PASR Current @ 25°C**

| ***Standby Current @ 25°C*** | | | |
|---|---|---|---|
| ***PASR*** | ***ISB –typical mean*** | ***Unit*** | ***Notes*** |
| Full | 180 | µA | 1, 2 |
| 1/2 | 160 | µA | 1, 2 |
| 1/4 | 150 | µA | 1, 2 |
| 1/8 | 145 | µA | 1, 2 |
| ***Halfsleep™ Current @ 25°C*** | | | |
| ***PASR*** | ***I Halfsleep™ -typical mean*** | ***Unit*** | ***Notes*** |
| Full | 80 | µA | 1,2,3 |
| 1/2 | 60 | µA | 1,2,3 |
| 1/4 | 50 | µA | 1,2,3 |
| 1/8 | 44 | µA | 1,2,3 |

**Table 29: Typical-mean PASR Current @ 105°C /85°C**

| ***Standby Current @ 105°C*** | | | |
|---|---|---|---|
| ***PASR*** | ***ISB –typical mean*** | ***Unit*** | ***Notes*** |
| Full | 1050 | µA | 2 |
| 1/2 | 725 | µA | 2 |
| 1/4 | 565 | µA | 2 |
| 1/8 | 485 | µA | 2 |
| ***Halfsleep™ Current @ 85°C*** | | | |
| ***PASR*** | ***I Halfsleep™ -typical mean*** | ***Unit*** | ***Notes*** |
| Full | 880 | µA | 2, 3 |
| 1/2 | 600 | µA | 2, 3 |
| 1/4 | 460 | µA | 2, 3 |
| 1/8 | 380 | µA | 2, 3 |

Note1: Current at 25°C is only attainable by enabling 0.5x Refresh Frequency (see Table 17)
Note2: PASR Current is only characterized without CLK toggling.
Note3: Spec'd Halfsleep™ current is only guaranteed after 150ms into Halfsleep™ mode.


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## 8.7 AC Characteristics

**Table 30: READ/WRITE Timing**

| | | KGD/BGA 1.8V Only | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 133MHz | | 166MHz | | 200MHz | | 225MHz | | 250MHz | | | |
| Symbol | Parameter | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Unit | Notes |
| tCLK | CLK period | 7.5 | | 6 | | 5 | | 4.4 | | 4 | | ns | |
| tCH/tCL | Clock high/low width | 0.45 | 0.55 | 0.45 | 0.55 | 0.45 | 0.55 | 0.45 | 0.55 | 0.45 | 0.55 | tCLK | |
| tKHKL | CLK rise or fall time | | 1.2 | | 1 | | 0.8 | | 0.7 | | 0.6 | ns | |
| tCPH | CE# HIGH between subsequent burst operations | 15 | | 18 | | 24 | | 26 | | 28 | | ns | |
| tCEM | CE# low pulse width (excluding Halfsleep™ exit) | | 4 | | 4 | | 4 | | 4 | | 4 | µs | Standard temp |
| | | | 1 | | 1 | | 1 | | 1 | | 1 | µs | Extended temp |
| tCEM | CE# low pulse width | 3 | | 3 | | 3 | | 3 | | 3 | | tCLK | Minimum 3 clocks |
| tCSP | CE# setup time to CLK rising edge | 2 | | 2 | | 2 | | 2 | | 1.6 | | ns | |
| tCSP2 | CE# rising edge to next CLK falling edge | 1.5 | | 1.5 | | 1.5 | | 1.5 | | 1.5 | | ns | |
| tCHD | CE# hold time from CLK falling edge | 2 | | 2 | | 2 | | 2 | | 1.6 | | ns | |
| tSP | Setup time to active CLK edge | 0.8 | | 0.6 | | 0.5 | | 0.5 | | 0.5 | | ns | |
| tHD | Hold time from active CLK edge | 0.8 | | 0.6 | | 0.5 | | 0.5 | | 0.5 | | ns | Max 0.75*tCLK |
| tHZ | Chip disable to DQ/DQS output high-Z | | 6 | | 6 | | 6 | | 6 | | 6 | ns | |
| tRBXwait | Row Boundary Crossing Wait Time | 30 | 65 | 30 | 65 | 30 | 65 | NA | NA | NA | NA | ns | |
| tRC | Write Cycle | 60 | | 60 | | 60 | | 60 | | 60 | | ns | |
| tRC | Read Cycle | 60 | | 60 | | 60 | | 60 | | 60 | | ns | |
| tHS | Minimum Halfsleep™ duration | 150 | | 150 | | 150 | | 150 | | 150 | | µs | |
| tXHS | Halfsleep™ Exit CE# low to CLK setup time | 150 | | 150 | | 150 | | 150 | | 150 | | µs | |
| tXPHS | Halfsleep™ Exit CE# low pulse width | 60 | | 60 | | 60 | | 60 | | 60 | | ns | |
| | | | tCEM | | tCEM | | tCEM | | tCEM | | tCEM | µs | Standard temp |
| | | | | | | | | | | | | µs | Extended temp |
| tDPD | Minimum DPD | 500 | | 500 | | 500 | | 500 | | 500 | | µs | |
| tDPDp | Minimum period between DPD Modes | 500 | | 500 | | 500 | | 500 | | 500 | | µs | |
| tXDPD | DPD CE# low to CLK setup time | 150 | | 150 | | 150 | | 150 | | 150 | | µs | |
| tXPDPD | DPD Exit CE# low pulse width | 60 | | 60 | | 60 | | 60 | | 60 | | ns | |
| tPU | Device Initialization | 150 | | 150 | | 150 | | 150 | | 150 | | µs | |
| tRP | RESET# low pulse width | 1 | | 1 | | 1 | | 1 | | 1 | | µs | |
| tRST | Reset to CMD valid | 2 | | 2 | | 2 | | 2 | | 2 | | µs | |


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**Table 31: DDR timing parameters**

| | | KGD/BGA 1.8V Only | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 133MHz | | 166MHz | | 200MHz | | 225MHz | | 250MHz | | | |
| **Symbol** | **Parameter** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Unit** | **Notes** |
| tCQLZ | Clock rising edge to DQS low | 1 | 6 | 1 | 6 | 1 | 6 | 1 | 6 | 1 | 6 | ns | |
| tDQSCK | DQS output access time from CLK | 2 | 6.5 | 2 | 6.5 | 2 | 6.5 | 2 | 6.5 | 2 | 6.5 | ns | |
| tDQSQ | DQS – DQ skew | | 0.6 | | 0.5 | | 0.4 | | 0.4 | | 0.4 | ns | |
| tDS | DQ and DM input setup time | 0.8 | | 0.6 | | 0.5 | | 0.5 | | 0.5 | | ns | |
| tDH | DQ and DM input hold time | 0.8 | | 0.6 | | 0.5 | | 0.5 | | 0.5 | | ns | |


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# 9 Change Log

| Version | Who | Date | Description |
|---|---|---|---|
| 0.1 | Boray | Apr. 18, 2023 | Initial Version |
| 0.2 | Boray | Apr. 24, 2023 | Adjust AC data and PN |
| 0.3 | Boray | Jul.18, 2023 | 1. Update Read/write latency table<br>2. Update Figure 7<br>3. Modify protocol description |
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