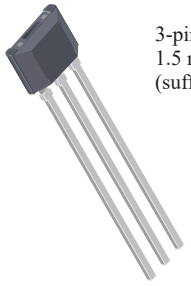
# ALS31001LUAA

## Linear Hall-Effect Sensor IC with Analog Output, in Ultramini Through-Hole Package

### FEATURES AND BENEFITS

- 3.3 or 5.0 V supply operation
- QVO temperature coefficient programmed at Allegro™ for improved accuracy
- High-bandwidth, low-noise analog output
- High-speed chopping scheme minimizes QVO drift across operating temperature range
- Temperature-stable quiescent voltage output and sensitivity
- Precise recoverability after temperature cycling
- Output voltage clamps provide short-circuit diagnostic capabilities
- Undervoltage lockout (UVLO)
- Wide ambient temperature range: –40°C to 150°C
- Immune to mechanical stress
- Enhanced EMC performance for stringent automotive applications
- Small package size

### PACKAGE:



3-pin ultramini SIP
1.5 mm × 4 mm × 3 mm
(suffix UA)

*Not to scale*

### DESCRIPTION

New applications for linear output Hall-effect sensors, such as displacement and angular position, require higher accuracy and smaller package sizes. The Allegro ALS31001LUAA linear Hall-effect sensor IC has been designed specifically to meet both requirements.

The accuracy of this device is enhanced via end-of-line optimization. The ALS31001LUAA features non-volatile memory to optimize device sensitivity and the quiescent voltage output (QVO: output in the absence of a magnetic field) for a given application or circuit. Optimized performance is sustained across the full operating temperature range by programming the temperature coefficient for both sensitivity and QVO at Allegro end-of-line test.

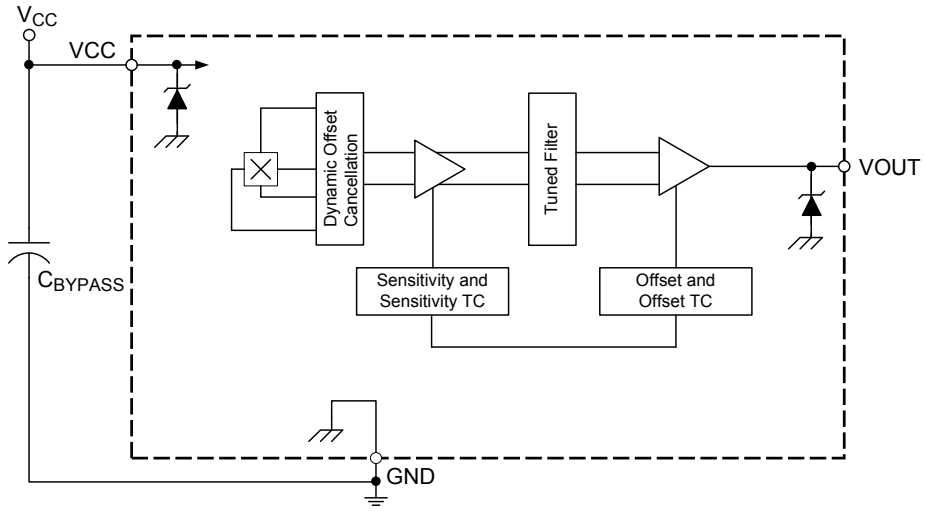
This ratiometric Hall-effect sensor IC provides a voltage output proportional to the applied magnetic field. The quiescent voltage output is adjusted around 50% of the supply voltage.

The features of this linear device make it ideal for use in automotive and industrial applications requiring high accuracy and operation across an extended temperature range, –40°C to 150°C.

Each BiCMOS monolithic circuit integrates: a Hall element, temperature-compensating circuitry to reduce the intrinsic sensitivity drift of the Hall element, a small-signal high-gain amplifier, a clamped low-impedance output stage, and a proprietary dynamic offset cancellation technique.

*Continued on the next page…*

### Functional Block Diagram




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## DESCRIPTION (CONTINUED)

The ALS31001LUAA sensor IC is offered in the UA package style: a 3-pin ultramini single inline package (SIP) for through-hole mounting. The package is lead (Pb) free, with 100% matte-tin leadframe plating.

## SELECTION GUIDE

| Part Number | Output Polarity | Nominal Supply Voltage (V) | Sensitivity (typ) (mV/G) | Packing* | Package |
|---|---|---|---|---|---|
| ALS31001LUAATN | Forward | 3.3 | 1.8 | 4000 pieces per 13-inch reel | 3-pin SIP through-hole |
| ALS31001LUAATN-5V | Forward | 5.0 | 2.5 | | |

*Contact Allegro™ for additional packing options

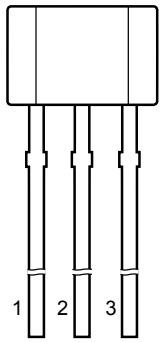
## ABSOLUTE MAXIMUM RATINGS

| Characteristic | Symbol | Notes | Rating | Unit |
|---|---|---|---|---|
| Forward Supply Voltage | $V_{CC}$ | | 8 | V |
| Reverse Supply Voltage | $V_{RCC}$ | | –0.1 | V |
| Forward Output Voltage | $V_{OUT}$ | | 7 | V |
| Reverse Output Voltage | $V_{ROUT}$ | | –0.1 | V |
| Output Source Current | $I_{OUT(SOURCE)}$ | VOUT to GND | 2 | mA |
| Output Sink Current | $I_{OUT(SINK)}$ | VCC to VOUT | 10 | mA |
| Operating Ambient Temperature | $T_A$ | Range L | –40 to 150 | °C |
| Maximum Junction Temperature | $T_J$(max) | | 165 | °C |
| Storage Temperature | $T_{stg}$ | | –65 to 170 | °C |

## THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

| Characteristic | Symbol | Test Conditions | Value | Units |
|---|---|---|---|---|
| Package Thermal Resistance | $R_{\theta JA}$ | Package UA, 1-layer PCB with copper limited to solder pads | 165 | °C/W |

### Pinout Diagram




UA Package

### Terminal List Table

| Name | Number | Description |
|---|---|---|
| VCC | 1 | Input power supply; tie to GND with bypass capacitor |
| GND | 2 | Ground |
| VOUT | 3 | Output signal |



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**OPERATING CHARACTERISTICS:** Valid over $T_A$ , $C_{BYPASS}$ = 0.1 µF, and nominal $V_{CC}$, unless otherwise noted

| Characteristic | Symbol | Test Conditions | Min. | Typ. | Max. | Unit[1] |
|---|---|---|---|---|---|---|
| **ELECTRICAL CHARACTERISTICS** | | | | | | |
| Supply Voltage | $V_{CC}$ | ALS31001LUAA-TN | 3.0 | 3.3 | 3.6 | V |
| | | ALS31001LUAATN-5V | 4.5 | 5.0 | 5.5 | V |
| Undervoltage Threshold[2] | $V_{UVLOHI}$ | Tested at $T_A$ = 25°C and $T_A$ = 150°C (device powers-on) | – | – | 3 | V |
| | $V_{UVLOLO}$ | Tested at $T_A$ = 25°C and $T_A$ = 150°C (device powers-off) | 2.5 | – | – | V |
| Supply Current | $I_{CC}$ | ALS31001LUAATN | – | 4.2 | 5.5 | mA |
| | | ALS31001LUAATN-5V | – | – | 8 | mA |
| Power-On Time[3][4] | $t_{PO}$ | $T_A$ = 25°C, $C_{L(PROBE)}$ = 10 pF | – | 50 | – | µs |
| $V_{CC}$ Ramp Time[3][4] | $t_{VCC}$ | $T_A$ = 25°C | 0.005 | – | 100 | ms |
| $V_{CC}$ Off Level[3][4] | $V_{CCOFF}$ | $T_A$ = 25°C | 0 | – | 0.33 | V |
| Delay to Clamp[3][4] | $t_{CLP}$ | $T_A$ = 25°C, $C_L$ = 0.22 nF | – | 30 | – | µs |
| Supply Zener Clamp Voltage | $V_Z$ | $T_A$ = 25°C, $I_{CC}$ = 13 mA | 6 | 7.3 | – | V |
| Internal Bandwidth[4] | $BW_i$ | Small signal –3 dB | – | 20 | – | kHz |
| Chopping Frequency[5] | $f_C$ | $T_A$ = 25°C | – | 400 | – | kHz |
| **OUTPUT CHARACTERISTICS** | | | | | | |
| Output Referred Noise[4] | $V_N$ | $V_{CC}$ = 3.3 V, $T_A$ = 25°C, $C_L$ = open, Sens = 1.8 mV/G, no load on VOUT | – | 4.9 | – | $mV_{(p-p)}$ |
| Input Referred RMS Noise Density[4] | $V_{NRMS}$ | $V_{CC}$ = 3.3 V, $T_A$ = 25°C, $C_L$ = open, Sens = 1.8 mV/G, no load on VOUT, $f_{measured}$ << 1 … 10 kHz | – | 3.0 | – | mG/√Hz |
| DC Output Resistance[4] | $R_{OUT}$ | | – | 3 | – | Ω |
| Output Load Resistance[4] | $R_L$ | VOUT to GND | 10 | – | – | kΩ |
| Output Load Capacitance[4] | $C_L$ | VOUT to GND | – | – | 0.22 | nF |
| Output Voltage Clamps[6][11] | $V_{CLPHIGH}$ | ALS31001LUAATN; $T_A$ = 25°C, B = +1000 G, $R_L$ = 10 kΩ (VOUT to GND) | 2.842 | 2.97 | 3.069 | V |
| | | ALS31001LUAATN-5V; $T_A$ = 25°C, B = +1000 G, $R_L$ = 10 kΩ (VOUT to GND) | 4.30 | 4.5 | 4.70 | V |
| | $V_{CLPLOW}$ | ALS31001LUAATN; $T_A$ = 25°C, B = –1000 G, $R_L$ = 10 kΩ (VOUT to GND) | 0.264 | 0.33 | 0.462 | V |
| | | ALS31001LUAATN-5V; $T_A$ = 25°C, B = –1000 G, $R_L$ = 10 kΩ (VOUT to GND) | 0.35 | 0.55 | 0.75 | V |
| Sensitivity[7] | Sens | $T_A$ = 25°C, ALS31001LUAATN | 1.71 | 1.80 | 1.89 | mV/G |
| | | $T_A$ = 25°C, ALS31001LUAATN-5V | 2.42 | 2.5 | 2.58 | mV/G |
| Quiescent Voltage Output (QVO) | $V_{OUT(Q)}$ | $T_A$ = 25°C, ALS31001LUAATN | 1.61 | 1.65 | 1.69 | V |
| | | $T_A$ = 25°C, ALS31001LUAATN-5V | 2.368 | 2.4 | 2.432 | V |
| Sensitivity Temperature Coefficient | $TC_{Sens}$ | Programmed at $T_A$ = 150°C, calculated relative to Sens at 25°C; ALS31001LUAATN | 0.08 | 0.12 | 0.16 | %/°C |
| | | Programmed at $T_A$ = 150°C, calculated relative to Sens at 25°C; ALS31001LUAATN-5V | 0.10 | 0.13 | 0.16 | %/°C |

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**OPERATING CHARACTERISTICS (continued):** Valid over $T_A$ , $C_{BYPASS}$ = 0.1 µF, and nominal $V_{CC}$, unless otherwise noted

| Characteristic | Symbol | Test Conditions | Min. | Typ. | Max. | Unit [1] |
|---|---|---|---|---|---|---|
| **ERROR COMPONENTS** | | | | | | |
| Linearity Sensitivity Error | $Lin_{ERR}$ | | – | ±1.5 | – | % |
| Symmetry Sensitivity Error | $Sym_{ERR}$ | | – | ±1.5 | – | % |
| Ratiometry Quiescent Voltage Output Error [8] | $Rat_{VOUT(Q)}$ | Across supply voltage range (relative to nominal $V_{CC}$) | – | ±1.5 | – | % |
| Ratiometry Sensitivity Error [8][9] | $Rat_{Sens}$ | Across supply voltage range (relative to nominal $V_{CC}$) | – | ±1.5 | – | % |
| Ratiometry Clamp Error [10] | $Rat_{VOUTCLP}$ | $T_A$ = 25°C, across supply voltage range (relative to nominal $V_{CC}$) | – | ±1.5 | – | % |
| **DRIFT CHARACTERISTICS** | | | | | | |
| Typical Quiescent Voltage Output Drift Across Temperature Range | $\Delta V_{OUT(Q)}$ | $T_A$ = 150°C | –23 | 0 | 23 | mV |
| Sensitivity Drift Due to Package Hysteresis | $\Delta Sens_{PKG}$ | $T_A$ = 25°C, after temperature cycling | – | ±2 | – | % |

[1] 1 G (gauss) = 0.1 mT (millitesla),
[2] On power-up, the output of the device is held low until $V_{CC}$ exceeds $V_{UVLOHI}$. After the device is powered, the output remains valid until $V_{CC}$ drops below $V_{UVLOLO}$, when the output is pulled low.
[3] See the Characteristic Definitions section.
[4] Determined by design and characterization, not evaluated at final test.
[5] $f_C$ varies as much as approximately ±20% across the full operating ambient temperature range and process.
[6] $V_{CLPLOW}$ and $V_{CLPHIGH}$ scale with $V_{CC}$ due to ratiometry.
[7] Sensitivity drift through the life of the part, $\Delta Sens_{LIFE}$, can have a typical error value ±3% in addition to package hysteresis effects.
[8] Percent change from actual value at nominal $V_{CC}$, for a given temperature.
[9] Cold temperature may exhibit up to 8% Ratiometry Sensitivity Error.
[10] Percent change from actual value at nominal $V_{CC}$, $T_A$ = 25°C.
[11] Tested at wafer probe.



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## CHARACTERISTIC DEFINITIONS

**Power-On Time.** When the supply is ramped to its operating voltage, the device output requires a finite time to react to an input magnetic field. Power-On Time, $t_{PO}$, is defined as the time it takes for the output voltage to begin responding to an applied magnetic field after the power supply has reached its minimum specified operating voltage, $V_{CC}$ (min), as shown in figure 1.

**Delay to Clamp.** A large magnetic input step may cause the clamp to overshoot its steady-state value. The Delay to Clamp, $t_{CLP}$, is defined as the time it takes for the output voltage to settle within 1% of its steady-state value, after initially passing through its steady-state voltage, as shown in figure 2.

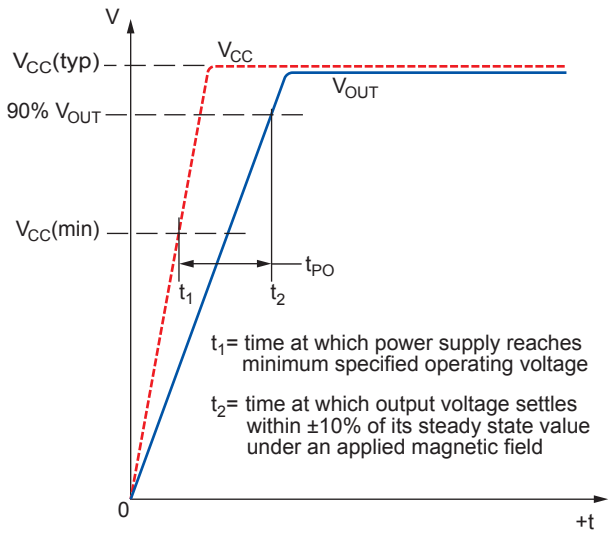



Figure 1. Definition of Power On Time, $t_{PO}$

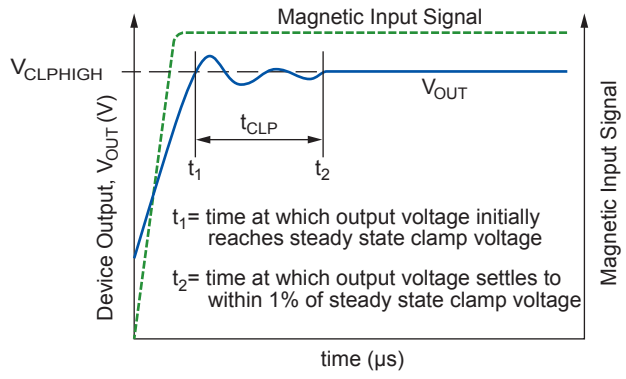



Figure 2. Definition of Delay to Clamp, $t_{CLP}$

**Quiescent Voltage Output.** In the quiescent state (no significant magnetic field: B = 0 G), the output, $V_{OUT(Q)}$, is at a constant ratio to the supply voltage, $V_{CC}$, across the entire operating ranges of $V_{CC}$ and Operating Ambient Temperature, $T_A$.

**Quiescent Voltage Output Drift Across Temperature Range.** Due to internal component tolerances and thermal considerations, the Quiescent Voltage Output, $V_{OUT(Q)}$, may drift due to temperature changes within the Operating Ambient Temperature, $T_A$. For purposes of specification, the Quiescent Voltage Output Drift Across Temperature Range, $\Delta V_{OUT(Q)}$ (mV), is defined as:

$$\Delta V_{OUT(Q)} = V_{OUT(Q)(TA)} - V_{OUT(Q)(25°C)} \quad (1)$$

**Sensitivity.** The amount of the output voltage change is proportional to the magnitude and polarity of the magnetic field applied. This proportionality is specified as the magnetic sensitivity, Sens (mV/G), of the device and is defined as:

$$\text{Sens} = \frac{V_{OUT(B+)} - V_{OUT(B-)}}{(B+) - (B-)} \quad (2)$$

where B+ is the magnetic flux density in a positive field (south polarity) and B– is the magnetic flux density in a negative field (north polarity).

**Sensitivity Temperature Coefficient.** The device sensitivity changes as temperature changes, with respect to its Sensitivity Temperature Coefficient, $TC_{SENS}$. $TC_{SENS}$ is programmed at 150°C, and calculated relative to the baseline sensitivity programming temperature of 25°C. $TC_{SENS}$ is defined as:

$$TC_{Sens} = \left(\frac{Sens_{T2} - Sens_{T1}}{Sens_{T1}} \times 100\right)\left(\frac{1}{T2 - T1}\right) \quad (\%/°C) \quad (3)$$

where T1 is the baseline Sens programming temperature of 25°C, and T2 is the $TC_{SENS}$ programming temperature of 150°C.

The ideal value of Sens across the full ambient temperature range, $Sens_{IDEAL(TA)}$, is defined as:

$$Sens_{IDEAL(TA)} = Sens_{T1} \times [100\ (\%) + TC_{SENS}\ (T_A - T1)] \quad (4)$$

**Sensitivity Drift Across Temperature Range.** Second order sensitivity temperature coefficient effects cause the magnetic sensitivity, Sens, to drift from its ideal value across the operating ambient temperature range, $T_A$. For purposes of specification,



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the Sensitivity Drift Across Temperature Range, $\Delta Sens_{TC}$, is defined as:

$$\Delta Sens_{TC} = \frac{Sens_{TA} - Sens_{IDEAL(TA)}}{Sens_{IDEAL(TA)}} \times 100 \quad (\%) \qquad (5)$$

**Sensitivity Drift Due to Package Hysteresis.** Package stress and relaxation can cause the device sensitivity at $T_A = 25°C$ to change during and after temperature cycling. This change in sensitivity follows a hysteresis curve. For purposes of specification, the Sensitivity Drift Due to Package Hysteresis, $\Delta Sens_{PKG}$, is defined as:

$$\Delta Sens_{PKG} = \frac{Sens_{(25°C)(2)} - Sens_{(25°C)(1)}}{Sens_{(25°C)(1)}} \times 100 \quad (\%) \qquad (6)$$

where $Sens_{(25°C)(1)}$ is the programmed value of sensitivity at $T_A = 25°C$, and $Sens_{(25°C)(2)}$ is the value of sensitivity at $T_A = 25°C$ after temperature cycling $T_A$ up to 150°C, down to –40°C, and back to up 25°C.

**Linearity Sensitivity Error.** The ALS31001LUAA is designed to provide linear output in response to a ramping applied magnetic field. Consider two magnetic fields, B1 and B2. Ideally, the sensitivity of a device is the same for both fields, for a given supply voltage and temperature. Linearity error is present when there is a difference between the sensitivities measured at B1 and B2.

Linearity Sensitivity Error, $LIN_{ERR}$, is calculated separately for positive ($Lin_{ERR+}$) and negative ($Lin_{ERR–}$) applied magnetic fields. $LIN_{ERR}$ (%) is measured and defined as:

$$Lin_{ERR+} = \left(1 - \frac{Sens_{(B+)(2)}}{Sens_{(B+)(1)}}\right) \times 100 \quad (\%) \qquad (7)$$

$$Lin_{ERR–} = \left(1 - \frac{Sens_{(B–)(2)}}{Sens_{(B–)(1)}}\right) \times 100 \quad (\%)$$

where:

$$Sens_{Bx} = \frac{|V_{OUT(Bx)} - V_{OUT(Q)}|}{B_x} \qquad (8)$$

and Bx are positive and negative magnetic fields, with respect to the quiescent voltage output, such that

$$|B_{(+)(2)}| > |B_{(+)(1)}| \text{ and } |B_{(–)(2)}| > |B_{(–)(1)}|$$

The effective linearity error is:

$$Lin_{ERR} = \max(|Lin_{ERR+}|, |Lin_{ERR–}|) \qquad (9)$$

The output voltage clamps, $V_{CLPHIGH}$ and $V_{CLPLOW}$, limit the operating magnetic range of the applied field in which the device provides a linear output. The maximum positive and negative applied magnetic fields in the operating range can be calculated:

$$|B_{MAX(+)}| = \frac{V_{CLPHIGH} - V_{OUT(Q)}}{Sens} \qquad (10)$$

$$|B_{MAX(–)}| = \frac{V_{OUT(Q)} - V_{CLPLOW}}{Sens}$$

**Symmetry Sensitivity Error.** The magnetic sensitivity of the device is constant for any two applied magnetic fields of equal magnitude and opposite polarities. Symmetry error, $Sym_{ERR}$ (%), is measured and defined as:

$$Sym_{ERR} = \left(1 - \frac{Sens_{(B+)}}{Sens_{(B–)}}\right) \times 100 \quad (\%) \qquad (11)$$

where $Sens_{Bx}$ is as defined in equation 10, and B+ and B– are positive and negative magnetic fields such that |B+| = |B–|.

**Ratiometry Error.** The ALS31001LUAA provides ratiometric output. This means that the Quiescent Voltage Output, $V_{OUT(Q)}$, magnetic sensitivity, Sens, and clamp voltages, $V_{CLPHIGH}$ and $V_{CLPLOW}$, are proportional to the supply voltage, $V_{CC}$. In other words, when the supply voltage increases or decreases by a certain percentage, each characteristic also increases or decreases by the same percentage. Error is the difference between the measured change in the supply voltage relative to the nominal $V_{CC}$ level (3.3 V or 5.0 V), and the measured change in each characteristic. Equations below show examples for a 3.3 V supply device.

The ratiometric error in quiescent voltage output, $Rat_{VOUT(Q)}$ (%), for a given supply voltage, $V_{CC}$, is defined as:

$$Rat_{VOUT(Q)} = \left(1 - \frac{V_{OUT(Q)(VCC)} / V_{OUT(Q)(3.3V)}}{V_{CC} / 3.3\ (V)}\right) \times 100 \quad (\%) \qquad (12)$$

The ratiometric error in magnetic sensitivity, $Rat_{Sens}$ (%), for a given supply voltage, $V_{CC}$, is defined as:

$$Rat_{Sens} = \left(1 - \frac{Sens_{(VCC)} / Sens_{(3.3V)}}{V_{CC} / 3.3\ (V)}\right) \times 100 \quad (\%) \qquad (13)$$

The ratiometric error in the clamp voltages, $Rat_{VOUTCLP}$ (%), for a given supply voltage, $V_{CC}$, is defined as:

$$Rat_{VOUTCLP} = \left(1 - \frac{V_{CLP(VCC)} / V_{CLP(3.3V)}}{V_{CC} / 3.3\ (V)}\right) \times 100 \quad (\%) \qquad (14)$$

where $V_{CLP}$ is either $V_{CLPHIGH}$ or $V_{CLPLOW}$.



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**Undervoltage Lockout.** The ALS31001LUAA provides an undervoltage lockout feature which ensures that the device outputs a VOUT signal only when $V_{CC}$ is above certain thresholds. The undervoltage lockout feature provides a hysteresis of operation to eliminate indeterminate output states.

The output of the ALS31001LUAA is held low (GND) until $V_{CC}$ exceeds $V_{UVLOHI}$. After $V_{CC}$ exceeds $V_{UVLOHI}$, the device VOUT output is enabled, providing a ratiometric output voltage that is proportional to the input magnetic signal and $V_{CC}$. If $V_{CC}$ should drop back down below $V_{UVLOLO}$ for longer than $t_{UVLO}$ after the device is powered up, the output would be pulled low (see figure 3) until $V_{UVLOHI}$ is reached again and VOUT would be reenabled.

**$V_{CC}$ Ramp Time.** The time taken for $V_{CC}$ to ramp from 0 V to $V_{CC}$(typ) (see figure 4).

**$V_{CC}$ Off Level.** For applications in which the VCC pin of the ALS31001LUAA is being power-cycled (for example using a multiplexer to toggle the part on and off), the specification of $V_{CC}$ Off Level, $V_{CCOFF}$, determines how high a $V_{CC}$ off voltage can be tolerated while still ensuring proper operation and startup of the device (see figure 4).

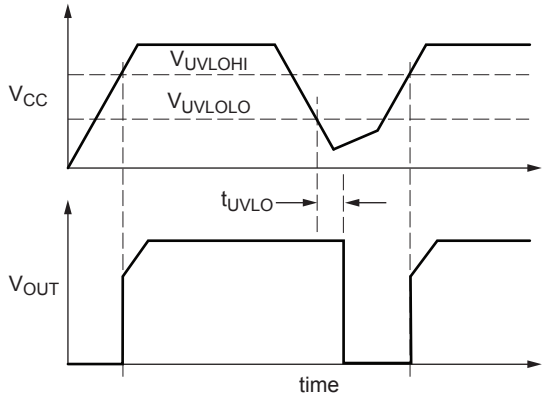



Figure 3. Definition of Undervoltage Lockout

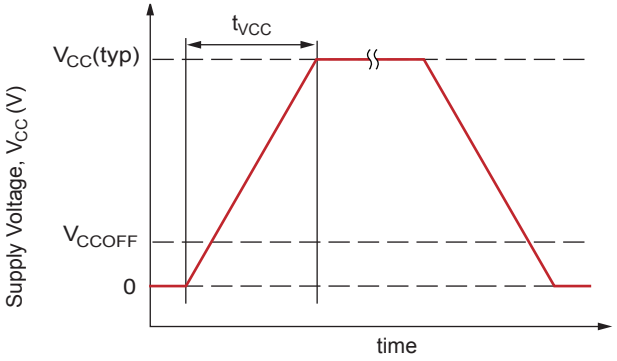



Figure 4. Definition of $V_{CC}$ Ramp Time, $t_{VCC}$



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## APPLICATION INFORMATION

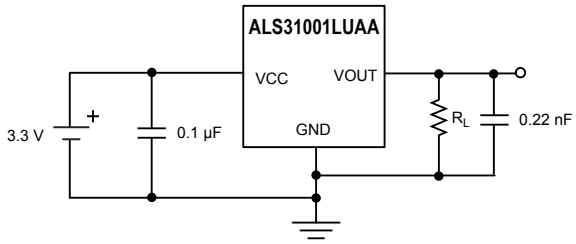



Figure 5. Typical Application Circuit

### CHOPPER STABILIZATION TECHNIQUE

When using Hall-effect technology, a limiting factor for switchpoint accuracy is the small-signal voltage developed across the Hall element. This voltage is disproportionally small relative to the offset that can be produced at the output of the Hall sensor IC. This makes it difficult to process the signal while maintaining an accurate, reliable output over the specified operating temperature and voltage ranges. Chopper stabilization is a unique approach used to minimize Hall offset on the chip. Allegro employs a technique to remove key sources of the output drift induced by thermal and mechanical stresses. This offset reduction technique is based on a signal modulation-demodulation process. The undesired offset signal is separated from the magnetic field-induced signal in the frequency domain, through modulation. The subsequent demodulation acts as a modulation process for the offset, causing the magnetic field-induced signal to recover its original spectrum at base band, while the DC offset becomes a high-frequency signal. The magnetic-sourced signal then can pass through a low-pass filter, while the modulated DC offset is suppressed. In addition to the removal of the thermal and mechanical stress related offset, this novel technique also reduces the amount of thermal noise in the Hall sensor IC while completely removing the modulated residue resulting from the chopper operation. The chopper stabilization technique uses a high-frequency sampling clock. For demodulation process, a sample-and-hold technique is used. This high-frequency operation allows a greater sampling rate, which results in higher accuracy and faster signal-processing capability. This approach desensitizes the chip to the effects of thermal and mechanical stresses, and produces devices that have extremely stable quiescent Hall output voltages and precise recoverability after temperature cycling. This technique is made possible through the use of a BiCMOS process, which allows the use of low-offset, low-noise amplifiers in combination with high-density logic integration and sample-and-hold circuits.

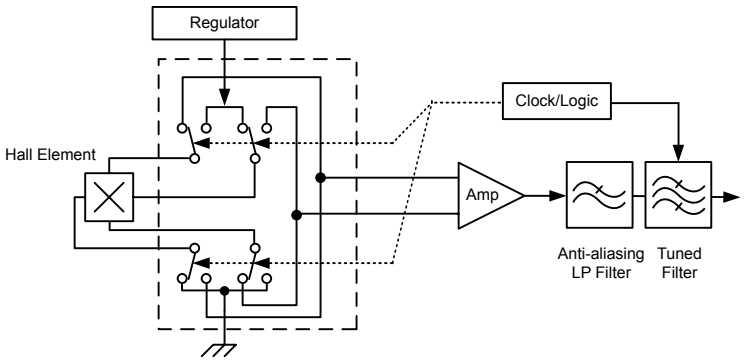



Figure 6. Chopper Stabilization Technique



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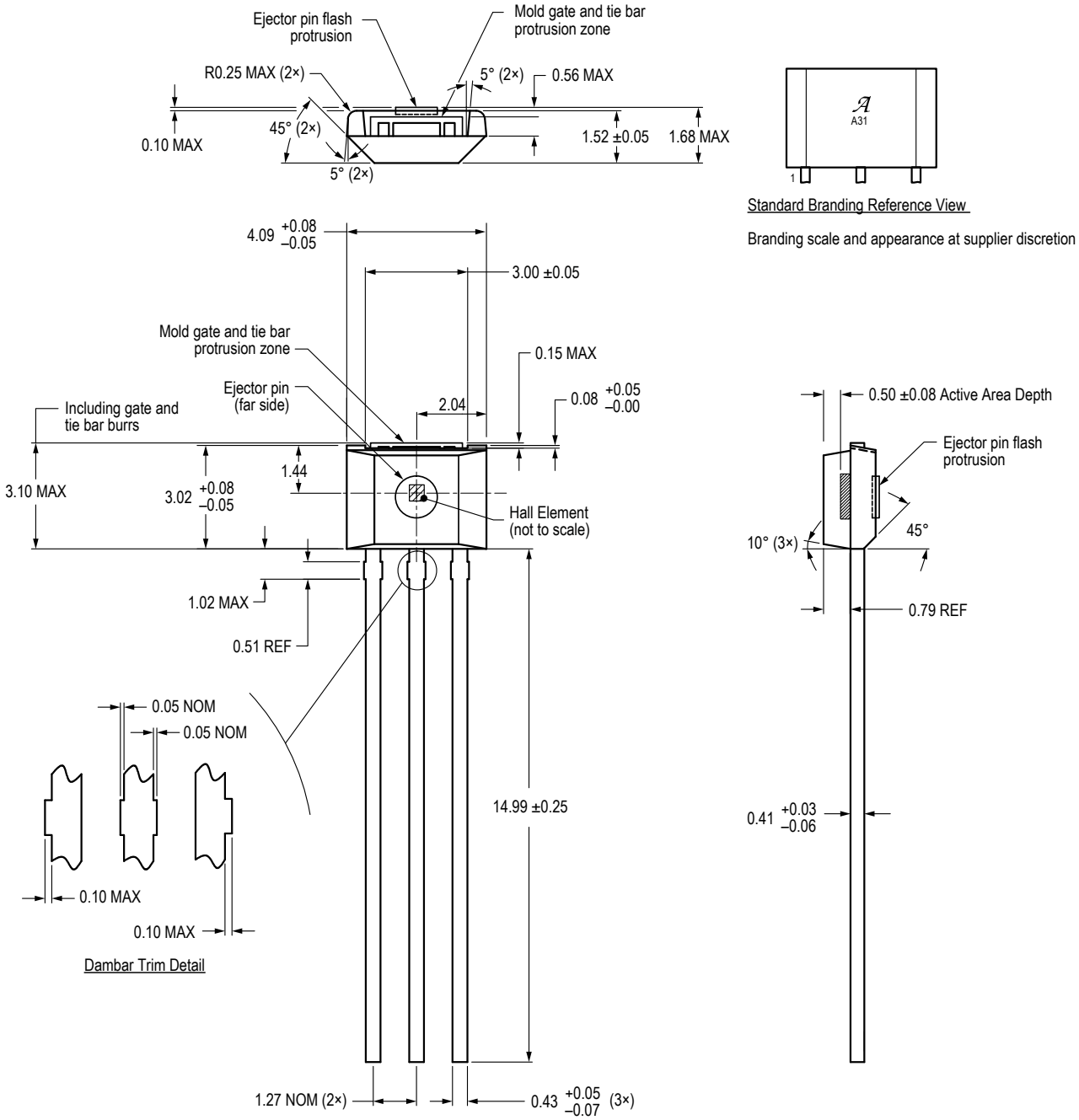
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## Package UA, 3-Pin SIP

**For Reference Only – Not For Tooling Use**

(Reference DWG-0000404, Rev. 1)
NOT TO SCALE
Dimensions in millimeters
Exact case and lead configuration at supplier discretion within limits shown






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## Revision History

| Number | Date | Description |
|---|---|---|
| – | November 28, 2017 | Initial release |
| 1 | January 11, 2019 | Minor editorial updates |
| 2 | January 20, 2020 | Minor editorial updates |
| 3 | March 24, 2020 | Added 5 V supply voltage variant |
| 4 | March 31, 2020 | Updated Output Voltage Clamps characteristic (page 3) |
| 5 | April 20, 2020 | Updated Output Voltage Clamps characteristic (page 3) |
| 6 | April 23, 2020 | Updated part numbers (pages 2-3) |
| 7 | May 4, 2021 | Updated Package Outline Drawing reference number and active area depth (page 9) |
| 8 | May 13, 2022 | Updated Package Outline Drawing (page 9) |

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