# A31316

# 3D Magnetic Position Sensor IC

## FEATURES AND BENEFITS

- 3D magnetic sensor enables flexible mechanical integration for contactless linear and rotary position applications
- Configurable signal path processing and on-chip angle calculation for accurate 360° and short stroke (<360°) rotary applications
- Multiple programmable linearization options for maximum measurement accuracy:
  - □ Piecewise-linear and binning modes
  - □ Up to 33-point fixed position
  - □ Up to 22-point programmable positions
- PWM and SENT (SAE J2716) output formats
- Integrated IC diagnostics for high reliability
- Developed in accordance with ISO 26262 requirements for hardware product development for use in safety-critical applications targeting ASIL B compatibility (pending assessment)
- Broken wire detection
- 5 V operation with Undervoltage Detection (UVD)
- Built-In Self-Test (BIST) Diagnostic Capability
- Wide operating temperature range: –40°C to 150°C
- In package passives remove the need for external support circuitry.

## PACKAGE



**Figure 1: 3-PIN SIP (Suffix UC)**

*Not to scale*

## DESCRIPTION

The A31316 is a robust 3D Hall-effect magnetic position sensor designed for on-axis and off-axis rotary as well as linear stroke position measurement in automotive, industrial, and consumer applications.

This sensor integrates vertical and planar Hall-effect elements with precision temperature-compensation circuitry to detect two out of three magnetic field components (X, Y, and Z). Configurable signal processing, linearization, and angle calculation allows the A31316 to accurately resolve the absolute rotary (full 360° and short stroke <360°) or linear position of a moving magnetic target.

The A31316 features PWM or SENT (SAE J2716) interface options to output the angle between the two factory-selected axes or the field form a single axis. In addition, the SENT interface provides the option to output the field measurement from both channels.

On-chip EEPROM technology, capable of supporting up to 100 write cycles, is integrated for flexible programming of configuration and calibration parameters and includes bits provided for customer device identification purposes.

The A31316 contains on-chip diagnostic features required for high reliability automotive applications, including monitors of both internal and external fault conditions.

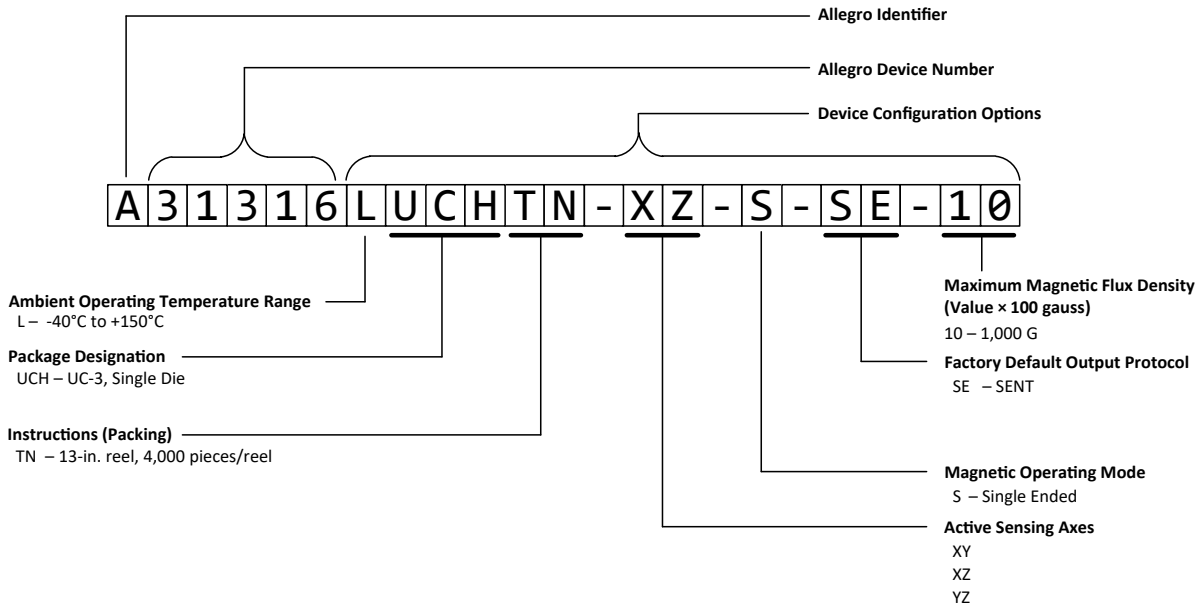
Developed in accordance with ISO 26262 as a hardware safety element out of context (SEooC) with ASIL B capability for use in automotive safety-related systems when integrated and used in the manner prescribed in the applicable safety manual and datasheet.

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## SELECTION GUIDE

| Part Number | Temperature Trim Range | Optimized Field Range | Channel A | Channel B | Packing |
|---|---|---|---|---|---|
| A31316LUCHTN-XZ-S-SE-10 | –40°C to 150°C | 300 to 1000 gauss | X | Z | 4,000 pieces per 13-in reel |
| A31316LUCHTN-XY-S-SE-10 | –40°C to 150°C | 300 to 1000 gauss | X | Y | 4,000 pieces per 13-in reel |
| A31316LUCHTN-YZ-S-SE-10 | –40°C to 150°C | 300 to 1000 gauss | Z | Y | 4,000 pieces per 13-in reel |

## PART NUMBER GUIDE






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## ABSOLUTE MAXIMUM RATINGS

| Characteristic | Symbol | Notes | Rating | Unit |
|---|---|---|---|---|
| Forward Supply Voltage | $V_{CC(absmax)}$ | Supply is clamped with 20 V limit to GND | 18 | V |
| Reverse Supply Voltage | $V_{RCC(absmax)}$ | Supply is clamped with –20 V limit to GND | –18 | V |
| Forward $V_{OUT}$-$V_{CC}$ Voltage | $V_{OUT-CC(absmax)}$ | $V_{OUT}$ is clamped with 20 V limit to $V_{CC}$; Note: There is no reverse $V_{OUT}$-$V_{CC}$ clamp | 18 | V |
| Forward Output Voltage | $V_{OUT(absmax)}$ | Output is clamped with 20 V limit to GND | 18 | V |
| Reverse Output Voltage | $V_{ROUT(absmax)}$ | Output is clamped with –10 V limit to GND | –6 | V |
| Forward Supply Current | $I_{CC}$ | | 40 | mA |
| Reverse Supply Current | $I_{RCC}$ | | –30 | mA |
| Output Current Limit | $I_{OUT(SOURCE)}$ | VOUT shorted to GND | 30 | mA |
| | $I_{OUT(SINK)}$ | VCC shorted to VOUT | –30 | mA |
| Extended Operating Ambient Temperature | $T_{A(EXT)}$ | Device will work within this temperature range, but performance is not specified | –45 to 165 | °C |
| Maximum Junction Temperature | $T_{J(MAX)}$ | | 165 | °C |
| Storage Temperature | $T_{stg}$ | | –65 to 165 | °C |

**THERMAL CHARACTERISTICS:** May require derating at maximum conditions; see application information

| Characteristic | Symbol | Test Conditions* | Value | Unit |
|---|---|---|---|---|
| Package Thermal Resistance | $R_{\Theta JA}$ | | 270 | °C/W |

*Additional thermal information available on the Allegro website.



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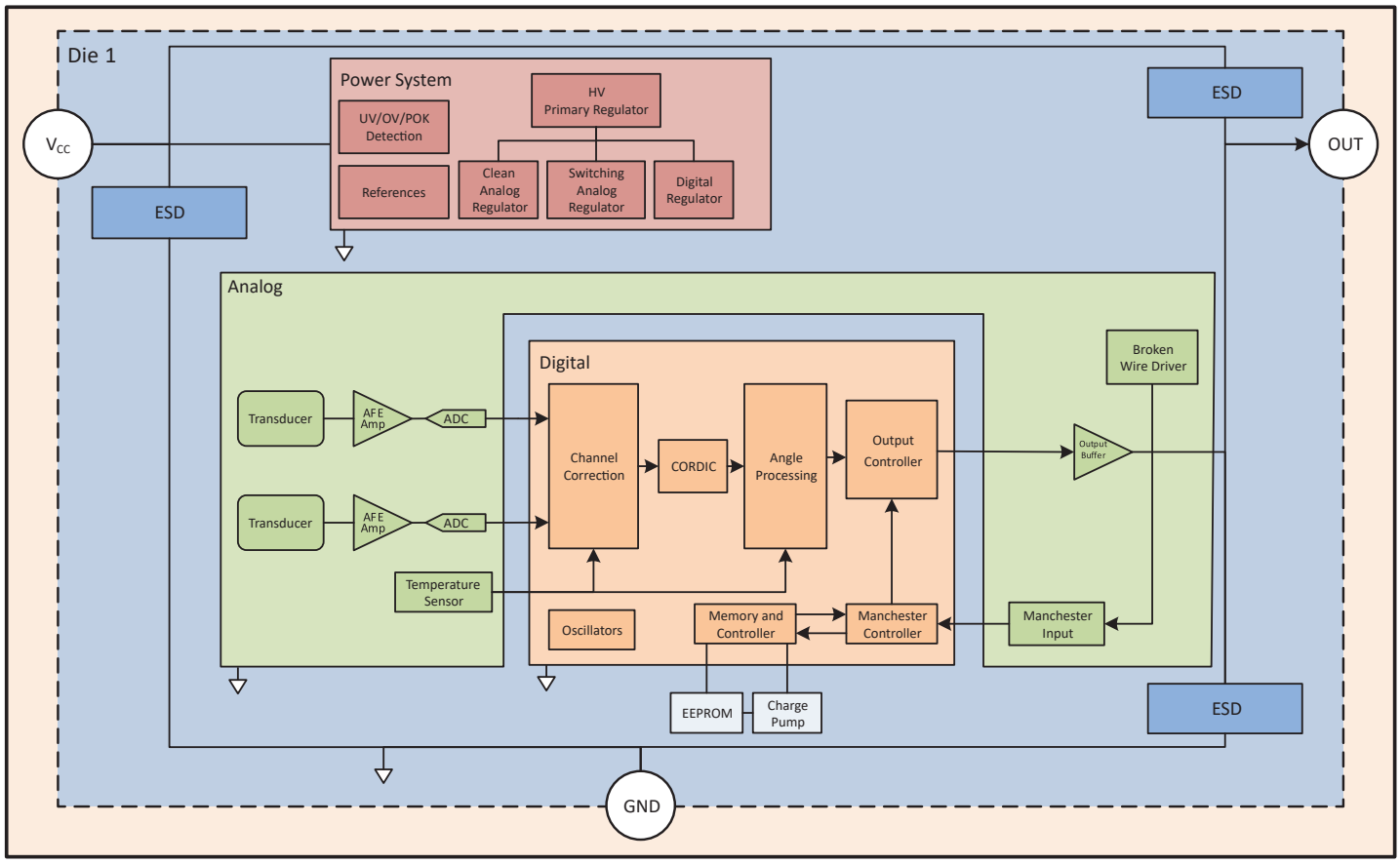



**Figure 2: Functional Block Diagram**



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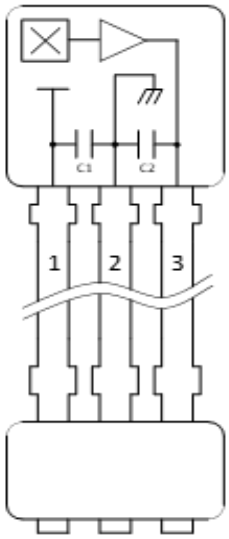
## PINOUT DIAGRAM, TERMINAL AND CAPACITOR LIST

**Terminal List**

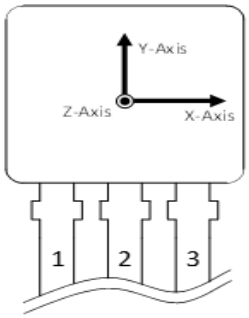
| Pin | Name | Function |
|---|---|---|
| 1 | VCC | Supply voltage |
| 2 | GND | Ground |
| 3 | OUT | Device output |

**Capacitor List**

| Capacitor | Value |
|---|---|
| C1 | 100 nF |
| C2 | 4.7 nF |



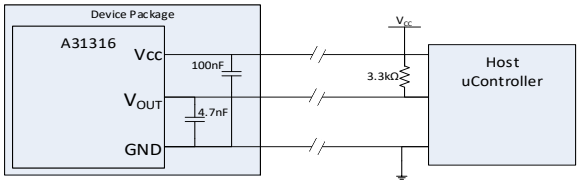

## AXIS DEFINITIONS




Note: Arrows show the default polarity of each axis. Polarity can be changed with internal settings.

## APPLICATION CIRCUIT

The A31316 contains all internal components required for use in default configurations (Push-pull mode). It is still recommended to provide a pull-up resistor in the event of a line break, or an error condition causes the devices to enter a High-Z state, so that there is a known output voltage.






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**OPERATING CHARACTERISTICS**: Valid at $T_A$ = –40°C to 150°C, $V_{CC}$ = 4.5 to 5.5 V, unless otherwise noted.

| Characteristics | Symbol | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **ELECTRICAL REQUIREMENTS** | | | | | | |
| Supply Voltage | $V_{CC}$ | | 4.5 | 5 | 6 | V |
| Supply Buffer Capacitor | $C_{SUP}$ | External capacitance in addition | 0 | – | 500 | nF |
| Supply Current | $I_{CC}$ | | 5 | 8.5 | 10 | mA |
| **DEVICE REQUIREMENTS** | | | | | | |
| Ambient Operating Temperature | $T_A$ | | –40 | – | 150 | °C |
| Number of EEPROM Writes [1] | $N_{EEPROM}$ | $T_A$ = 25°C | – | – | 100 | writes |
| **MAGNETIC REQUIREMENTS** | | | | | | |
| Magnetic Flux Density | $\|B_{IN}\|$ | For xxx-10 parts, devices tested at $\|B_{IN}\|$ = 300 G, operation below this value is characterized, but not specified | – | ±300 | ±1000 | G |

[1] EEPROM writes are not supported at temperatures above 85°C.



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**PERFORMANCE CHARACTERISTICS:** Valid for all electrical and device requirements ranges and $|B_{IN}| \geq 300$ G, unless otherwise noted

| Characteristics | Symbol | Test Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| **DEVICE SPECIFICATIONS** | | | | | | | |
| Undervoltage Detection Threshold | $V_{UVD\ (LOW,\ FALL)}$ | $V_{CC}$ falling, uvd_sel = '0' | | 3.60 | – | 4.10 | V |
| | $V_{UVD\ (LOW,\ RISE)}$ | $V_{CC}$ rising, uvd_sel = '0' | | 3.70 | – | 4.20 | V |
| | $V_{UVD\ (HIGH,\ FALL)}$ | $V_{CC}$ falling, uvd_sel = '1' | | 4.10 | – | 4.40 | V |
| | $V_{UVD\ (HIGH,\ RISE)}$ | $V_{CC}$ rising, uvd_sel = '1' | | 4.20 | – | 4.50 | V |
| Overvoltage Detection Threshold | $V_{OVD\ (LOW,\ FALL)}$ | $V_{CC}$ falling, ovd_sel = '1' | | 5.60 | – | 6.00 | V |
| | $V_{OVD\ (LOW,\ RISE)}$ | $V_{CC}$ rising, ovd_sel = '1' | | 5.65 | – | 6.05 | V |
| | $V_{OVD\ (HIGH,\ FALL)}$ | $V_{CC}$ falling, ovd_sel = '0' | | 8.40 | – | 10.20 | V |
| | $V_{OVD\ (HIGH,\ RISE)}$ | $V_{CC}$ rising, ovd_sel = '0' | | 8.60 | – | 10.40 | V |
| Power-On Reset Voltage | $V_{POR(FALL)}$ | $V_{CC}$ falling | | 2.60 | – | 2.90 | V |
| | $V_{POR(RISE)}$ | $V_{CC}$ rising | | 2.80 | – | 3.10 | V |
| Power-On Time | $t_{PO}$ | Time from $V_{CC} > V_{CC(MIN)}$ until unfiltered output is settled | | – | 1 | 1.70 | ms |
| Oscillator Frequency | $f_{OSC}$ | | | 7.36 | 8 | 8.64 | MHz |
| Output Current Limit | $I_{LIMIT}$ | Output FET on, $T_A$ = 25°C | | 19 | – | 30 | mA |
| **ABSOLUTE ANGLE SPECIFICATIONS** | | | | | | | |
| Angle Error (XY) | $ERR_{ANG(XY)}$ | $T_A$ = 25°C[1] | | –1 | – | 1 | degrees |
| | | –40°C ≤ $T_A$ ≤ 150°C | | –1.2 | – | 1.2 | degrees |
| Angle Error (XZ) | $ERR_{ANG(XZ)}$ | $T_A$ = 25°C [1] | | –1 | – | 1 | degrees |
| | | –40°C ≤ $T_A$ ≤ 150°C | | –1.2 | – | 1.2 | degrees |
| Angle Error (YZ) | $ERR_{ANG(YZ)}$ | $T_A$ = 25°C [1] | | –1 | – | 1 | degrees |
| | | –40°C ≤ $T_A$ ≤ 150°C | | –1.2 | – | 1.2 | degrees |
| Input-Referred Angle Noise [2] | $N_{ANG(IN)}$ | $\|B_{IN}\|$ = ± 300 G input field | bw_sel = 0, 329.1 Hz | – | 0.0291 | – | $degree_{RMS}$ |
| | | | bw_sel = 1, 465.8 Hz | – | 0.0291 | – | $degree_{RMS}$ |
| | | | bw_sel = 2, 556 Hz | – | 0.0326 | – | $degree_{RMS}$ |
| | | | bw_sel = 3, 700 Hz | – | 0.0381 | – | $degree_{RMS}$ |
| | | | bw_sel = 4, 1000 Hz | – | 0.0468 | – | $degree_{RMS}$ |
| | | | bw_sel = 5, 1482 Hz | – | 0.0575 | – | $degree_{RMS}$ |
| | | | bw_sel = 6, 2024 Hz | – | 0.0673 | – | $degree_{RMS}$ |
| **ANGLE DRIFT SPECIFICATIONS** | | | | | | | |
| Angle Drift (XY) | $DRIFT_{Ang,Temp(XY)}$ | Change in angle relative to $T_A$ = 25°C | | –1.2 | – | 1.2 | degrees |
| | $DRIFT_{Ang,Life(XY)}$ | Change in angle relative to pre-stress conditions[3] | | –0.9 | ±0.16 | 0.9 | degrees |
| Angle Drift (XZ) | $DRIFT_{Ang,Temp(XZ)}$ | Change in angle relative to $T_A$ = 25°C | | –1.2 | – | 1.2 | degrees |
| | $DRIFT_{Ang,Life(XZ)}$ | Change in angle relative to pre-stress conditions[3] | | –1.1 | ±0.65 | 1.1 | degrees |
| Angle Drift (YZ) | $DRIFT_{Ang,Temp(YZ)}$ | Change in angle relative to $T_A$ = 25°C | | –1.2 | – | 1.2 | degrees |
| | $DRIFT_{Ang,Life(YZ)}$ | Change in angle relative to pre-stress conditions[3] | | –1.0 | ±0.69 | 1.0 | degrees |

*Continued on next page...*



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**PERFORMANCE CHARACTERISTICS (continued):** Valid for all electrical and device requirements ranges and $|B_{IN}| \geq 300$ G, unless otherwise noted

| Characteristics | Symbol | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **ABSOLUTE CHANNEL SPECIFICATIONS** | | | | | | |
| Default Channel Sensitivity | $SENS_{Target}$ | Selection Guide Part Number: XXX-10 | – | 32.125 | – | LSB / G |
| Channel Sensitivity Error (X,Y) | $ERR_{Sens(X,Y)}$ | $T_A$ = 25°C [1] | –1.5 | – | 1.5 | % |
| | | –40°C ≤ $T_A$ ≤ 150°C | –3 | – | 3 | % |
| Channel Sensitivity Error (Z) | $ERR_{Sens(Z)}$ | $T_A$ = 25°C [1] | –1.5 | – | 1.5 | % |
| | | –40°C ≤ $T_A$ ≤ 150°C | –4 | – | 4 | % |
| Channel Offset Error (X,Y) | $ERR_{Off(X,Y)}$ | $T_A$ = 25°C [1] | –1.5 | – | 1.5 | G |
| | | –40°C ≤ $T_A$ ≤ 150°C | –4 | – | 4 | G |
| Channel Offset Error (Z) | $ERR_{Off(Z)}$ | $T_A$ = 25°C [1] | –1.5 | – | 1.5 | G |
| | | –40°C ≤ $T_A$ ≤ 150°C | –2.5 | – | 2.5 | G |
| Channel Linearity Error [2] | $ERR_{LIN}$ | 100 G ≤ $B_{IN}$ ≤ 1000 G | –0.3 | – | 0.3 | % |
| Input-Referred Channel Noise (X,Y) [2] | $N_{CHAN(X,Y)}$ | $T_A$ = 25°C[1] | – | 5.245 | – | mG (RMS/√Hz) |
| | | –40°C ≤ $T_A$ ≤ 150°C | – | 7.821 | – | mG (RMS/√Hz) |
| Input-Referred Channel Noise (Z) [2] | $N_{CHAN(Z)}$ | $T_A$ = 25°C[1] | – | 2.083 | – | mG (RMS/√Hz) |
| | | –40°C ≤ $T_A$ ≤ 150°C | – | 3.104 | – | mG (RMS/√Hz) |
| **CHANNEL DRIFT SPECIFICATIONS** | | | | | | |
| Channel Sensitivity Error Drift (X,Y) | $DRIFT_{Sens,Temp(X,Y)}$ | Change in sensitivity relative to $T_A$ = 25°C [1] | –2 | – | 2 | % |
| | $DRIFT_{Sens,Life(X,Y)}$ | Change in sensitivity relative to pre-stress conditions [3] | –1.4 | ±0.31 | 1.4 | % |
| Channel Sensitivity Error Drift (Z) | $DRIFT_{Sens,Temp(Z)}$ | Change in sensitivity relative to $T_A$ = 25°C [1] | –3 | – | 3 | % |
| | $DRIFT_{Sens,Life(Z)}$ | Change in sensitivity relative to pre-stress conditions [3] | –4.7 | ±2.30 | 4.7 | % |
| Channel Offset Drift (X,Y) | $DRIFT_{Off,Temp(X,Y)}$ | Change in offset relative to $T_A$ = 25°C [1] | –3.5 | – | 3.5 | G |
| | $DRIFT_{Off,Life(X,Y)}$ | Change in sensitivity relative to pre-stress conditions [3] | –0.97 | ±0.33 | 0.97 | G |
| Channel Offset Drift (Z) | $DRIFT_{Off,Temp(Z)}$ | Change in offset relative to $T_A$ = 25°C [1] | –1.5 | – | 1.5 | G |
| | $DRIFT_{Off,Life(Z)}$ | Change in sensitivity relative to pre-stress conditions[3] | –0.6 | ±0.15 | 0.6 | G |

[1] 25°C measurements taken after 48-72 hour wait at 40-55% relative humidity.
[2] Parameter not measured at final test. Determined by design and characterization.
[3] Min and Max values based on worst case drift seen during Q100 qual.



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**INTERFACE CHARACTERISTICS:** Valid for all electrical and device requirements ranges and $|B_{IN}| \geq 300$ G, unless otherwise noted

| Characteristics | Symbol | | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Broken Wire Response Time | $t_{BW}$ | | Time after $V_{CC}$ – GND = 0.2 V, either $V_{CC}$ or GND wire broken | – | – | 500 | µs |
| Diagnostic Voltage Ranges | $V_{SATDIAG(HIGH)}$ | $V_{CC}$ = 5 V | $R_L$ = 3.3 kΩ | 94 | 98 | 100 | $\%V_{CC}$ |
| | | | $R_L$ = 5 kΩ | 96 | 98 | 100 | $\%V_{CC}$ |
| | | | $R_L$ = 10 kΩ | 97 | 98 | 100 | $\%V_{CC}$ |
| | $V_{SATDIAG(LOW)}$ | $V_{CC}$ = 5 V | $R_L$ = 3.3 kΩ | 0 | 2 | 6 | $\%V_{CC}$ |
| | | | $R_L$ = 5 kΩ | 0 | 2 | 4 | $\%V_{CC}$ |
| | | | $R_L$ = 10 kΩ | 0 | 2 | 3 | $\%V_{CC}$ |
| High-Z Leakage | $I_{leak(Hi-Z)}$ | | Device in High-Z mode, output shorted to GND or VCC | –10 | – | 10 | µA |
| Filter Step Response Time | $t_{RESP}$ | | bw_sel = 5, time to 90% response to step | – | 396 | 450 | µs |
| Angle Update Rate | $t_{UPDATE}$ | | Valid for all bandwidth settings | 14.72 | 16 | 17.28 | µs |
| **MANCHESTER INTERFACE SPECIFICATIONS** | | | | | | | |
| Manchester Input Thresholds [3] | $V_{trig(H)}$ | | $V_{OUT}$ rising, dig_comm_input_high = '0' | 1.800 | 1.980 | 2.160 | V |
| | | | $V_{OUT}$ rising, dig_comm_input_high = '1' | 2.185 | 2.365 | 2.540 | V |
| | $V_{trig(L)}$ | | $V_{OUT}$ falling, dig_comm_input_low = '0' | 0.830 | 0.990 | 1.155 | V |
| | | | $V_{OUT}$ falling, dig_comm_input_low = '1' | 1.385 | 1.640 | 1.905 | V |
| | $V_{trig(hys)}$ | | dig_comm_input_high = '0', dig_comm_input_low = '0' | 0.815 | 0.985 | 1.150 | V |
| | | | dig_comm_input_high = '0', dig_comm_input_low = '1' | 0.160 | 0.335 | 0.525 | V |
| | | | dig_comm_input_high = '1', dig_comm_input_low = '0' | 1.155 | 1.380 | 1.605 | V |
| | | | dig_comm_input_high = '1', dig_comm_input_low = '1' | 0.495 | 0.725 | 0.995 | V |
| Manchester Communication Speed [3] | $f_{MAN}$ | | Manchester input bit rate (from host to sensor) | 4.0 | – | 100 | kbps |
| | | | Manchester output bit rate with 100 nF load (device responds at the input bit rate) | 4.0 | – | 8 [1] | kbps |
| **SENT INTERFACE SPECIFICATIONS** | | | | | | | |
| SENT Tick Time | $t_{TICK}$ | | Valid for all SENT Modes, dig_out_data_rate = '0' | 2.76 | 3 | 3.24 | µs |
| | | | Valid for all SENT Modes, range of selectable tick times [2] | 0.25 | – | 10 | µs |
| SENT Tick Time Tolerance | $TOL_{TICK}$ | | Valid for all selectable tick times | –8 | – | 8 | % |
| SENT Output Resolution | | | Based on sent_data_sel | 12 | – | 16 | bits |
| SENT Output Saturation Voltage | $V_{SAT(LOW)}$ | | Output current = –4.7 mA, $V_{CC}$ = 5 V, output FET on | – | – | 0.55 | V |
| SENT Output Load Capacitance | $C_L$ | | | 0 | – | 1 | nF |
| SENT Output Load Resistance | $R_{L(PULLUP)}$ | | Output Current ≥ –10 mA | 3.3 | – | – | kΩ |
| SENT Output Low Voltage [3] | $V_{OL}$ | | Low state voltage with 0.52 mA DC load current | – | – | 0.5 | V |
| SENT Output High Voltage [3] | $V_{OH}$ | | High state voltage with 0.1 mA DC load current | 4.1 | – | – | V |

*Continued on next page...*



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**INTERFACE CHARACTERISTICS:** Valid for all electrical and device requirements ranges and $|B_{IN}| \geq 300$ G, unless otherwise noted

| Characteristics | Symbol | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| SENT Ground Current [3] | $I_{GND}$ | Average current through (signal) ground line over one message | – | – | 50 | mA |
| SENT Supply Ripple Current [3] | $I_{SUP-RIPPLE}$ | Peak-to-peak variation in supply current consumption over one message at frequencies up to $f_C$ = 30 kHz measured as described for IGND | – | – | 9 | mA |
| SENT Fall Time [3] | $t_{FALL}$ | From $V_{OUT}$ = 3.8 V to $V_{OUT}$ = 1.1 V, $I_{GND} \leq 20$ mA, 3 µs tick time | – | – | 6.5 | µs |
| | | From $V_{OUT}$ = 3.8 V to $V_{OUT}$ = 1.1 V, 20 mA ≤ $I_{GND}$ ≤ 50 mA, 3 µs tick time | – | – | 5 | µs |
| SENT Rise Time [3] | $t_{RISE}$ | From $V_{OUT}$ = 1.1 V to $V_{OUT}$ = 3.8 V, 3 µs tick time | – | – | 18 | µs |
| SENT Edge Jitter [3] | $\Delta t_{FALL}$ | Edge to edge jitter with static environment for any pulse prior, 3 µs tick time | – | – | 0.1 | µs |
| SENT Nibble Jitter [3] | $\Delta t_{NIBBLE}$ | Variation of maximum nibble time compared to the expected time derived from the calibration pulse, 3 µs tick time | – | – | 0.3 | µs |
| **PWM INTERFACE SPECIFICATION** | | | | | | |
| PWM Carrier Frequency | $f_{PWM}$ | See Table 10 | 125 | – | 160000 | Hz |
| PWM Carrier Frequency Tolerance | $TOL(f_{PWM})$ | | –8 | – | 8 | % |
| PWM Resolution | $res_{PWM}$ | Based of $f_{PWM}$ | 8 | – | 15 | bit |
| Output Jitter, PWM | $PWM_{JIT}$ | $f_{PWM} \geq 2$ kHz, see Table 104 for LSB definition | –1 | – | 1 | LSB |
| | | $f_{PWM} < 2$ kHz, see Table 104 for LSB definition | –3 | – | 3 | LSB |
| PWM Duty Cycle | $D_{PWM}$ | | 2 | – | 98 | % |
| PWM Output Saturation Voltage | $V_{SAT(LOW)}$ | $R_{PULLUP} \geq 1.2$ kΩ | – | – | 0.40 | V |
| PWM Output Load Resistance | $R_{L(PULLUP)}$ | | 3.3 | – | – | kΩ |

[1] Based on receiver design.
[2] Tick times under 0.5 µs are available, but not guaranteed.
[3] Parameter not measured at final test. Determined by design and characterization.



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## POWER-UP AND POWER-DOWN SEQUENCES

As long as the supply voltage is below $V_{POR(RISE)}$, the sensor is held in reset. $V_{OUT}$ will be between GND and VCC. As the supply passes $V_{POR(RISE)}$, the sensor will leave the reset state and copy EEPROM values to the shadow registers. After the POR (Power-on reset) procedure is completed, the sensor will move to normal operation. If the supply is still below $V_{UVD(RISE)}$ at that point, the sensor will report undervoltage on the output as per error diagnostic configuration. If there is no error to be reported, the sensor will output data on the output pin. The first unfiltered data are available after $t_{PO}$. See Table 34 for $V_{UVD(RISE)}$ and $V_{UVD(FALL)}$ settings. See Table 35 for $V_{OVD(RISE)}$ and $V_{OVD(FALL)}$ options.

Note that, depending on the region, the output high or low level is decided by $R_L$, *out_err_resp_sel(ov/uv)*. These three levels can be defined independently of each other.

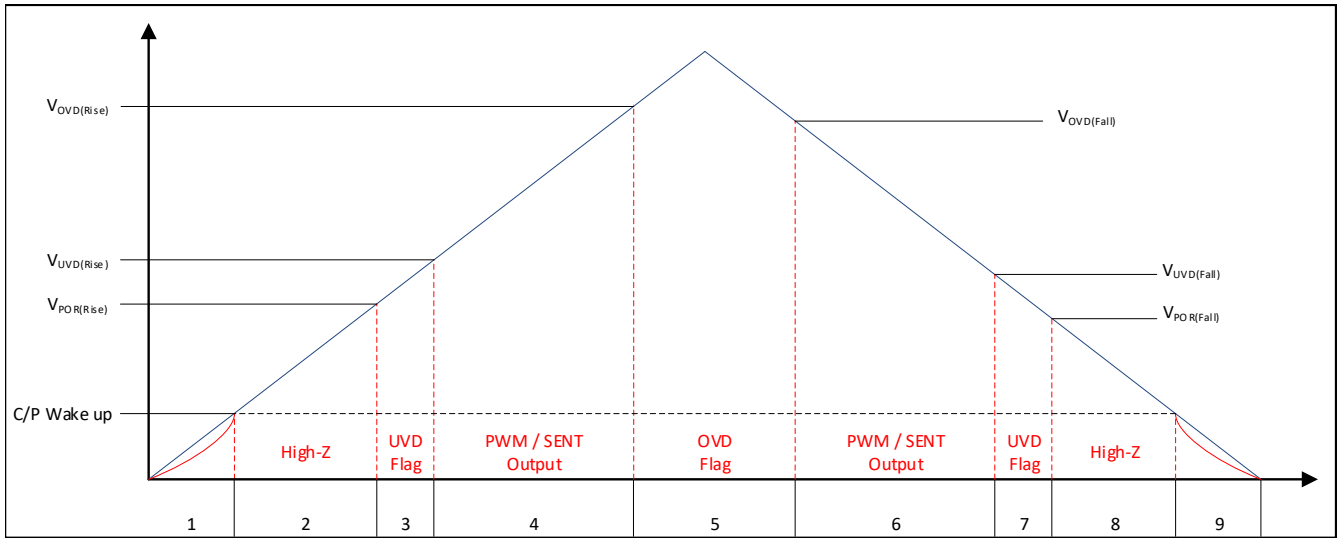



**Figure 3**

### Power-Up Time Specifications

| | |
|---|---|
| 1, 9 | Device is off. Output is determined by output stage and load circuit. |
| 2, 8 | Device is High-Z. Output voltage is based on load circuit. |
| 3, 7 | Device is in UVD. Output voltage is based on UVD error reporting settings. |
| 4, 6 | Device is active and in normal operation. |
| 5 | Device is in OVD. Output is based on OVD error reporting settings. |



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## FUNCTIONAL DESCRIPTION

The A31316 contains two independent signal paths. One of those are dedicated to alternate between the two sensing dimensions for the angle calculation. The second signal path is a complete copy of the time-shared signal path to provide a diagnostic check of the sensing channels to ensure accuracy for safety-critical applications. Each channel has dedicated Polarity, Sensitivity, and Offset correction that is available to the customer for end-of-line calibration. This allows the A31316 to be used in both rotary and linear position applications in any mounting orientation relative to the sensing magnet and to provide high accuracy and matching as the device and magnetic system changes over temperature.

The A31316 features an internal CORDIC calculation of angle from factory-selected pairs of detection axes (X, Y, and Z). The CORDIC calculation effective accuracy is 16 bits.

Equation 1:

$$\theta = \text{atan2}(\sin(\theta), \cos(\theta))$$

The output angle value is available in both SENT and PWM options. Alternatively, the two factory-selected channels of the X, Y, and Z channels are available to output in SENT. Along with the magnetic data, the SENT option provides access to additional device information such as temperature, error flag information, and customer identification register data. End-of-line angle calibration options are available in customer space to allow the device to be used in a wide number of contactless sensing applications.

### Typical Application Information

The A31316 has a high level of customer programmability to be used in a number of applications for either on- or off-axis rotary angle or linear position sensing. For on-axis rotary sensing, the on-chip ATAN2 provides an angle output that, combined with the configurable update rate, allows magnetic angular sensing at a wide range of system bandwidth requirements. To help account for errors associated with off axis mounting of the sensor, the individual Channel A and Channel B Sensitivity and Offset correction can be used to match the amplitude of the signals input to the ATAN2.

The A31316 can be used for slide-by applications, in which a one-dimensional position change of a target is to be measured. The angle output from the A31316 is related to the linear position of the magnetic target. With the available linearization on the A31316, stroke lengths greater than the length of the magnet can be realized.

### Temperature Output

The A31316 temperature sensor output that is used for temperature compensation within the device can be read from primary register temperature_16b [11:0], or in SENT in the extended data nibbles or SCN serial message.

**Table 1: Temperature Output Options**

| Temperature Reporting Method | Code Range | Temperature Range | Step Size | Conversion |
|---|---|---|---|---|
| Read of Register (temperature_16b) | –32,768 … 32,767 | –231.0°C … 281.0°C | 1/8°C | $T_A\,[°C] = \frac{\text{signed 16-bit temperature code}}{128} + 25$ |
| SENT Serial or Extended Nibble | 1 … 4088 | –230.9°C … 280.0 °C | 1/8°C | $T_A\,[°C] = \frac{\text{unsigned 12-bit temperature code} - 2048}{8} + 25$ |
| SENT 8-BIT Temperature Data | 1 … 255 | –229.0°C… 279.0 °C | 2°C | $T_A\,[°C] = (\text{unsigned 8-bit temperature code} - 128) \times 2 + 25$ |

SENT temperature sensor output corresponds to SAEJ2716 APRIL2016, chapter E.2.2.3, with the following function representation:

SENT Serial or Extended Nibble:
$X_1$ = –230.875°C = 42.275 K
$Y_1$ = 1

$X_2$ = 280.000°C = 553.150 K
$Y_2$ = 4088

SENT 8-Bit Data:
$X_1$ = –229.0°C = 44.150 K
$Y_1$ = 1

$X_2$ = 279.000°C = 552.150 K
$Y_2$ = 255



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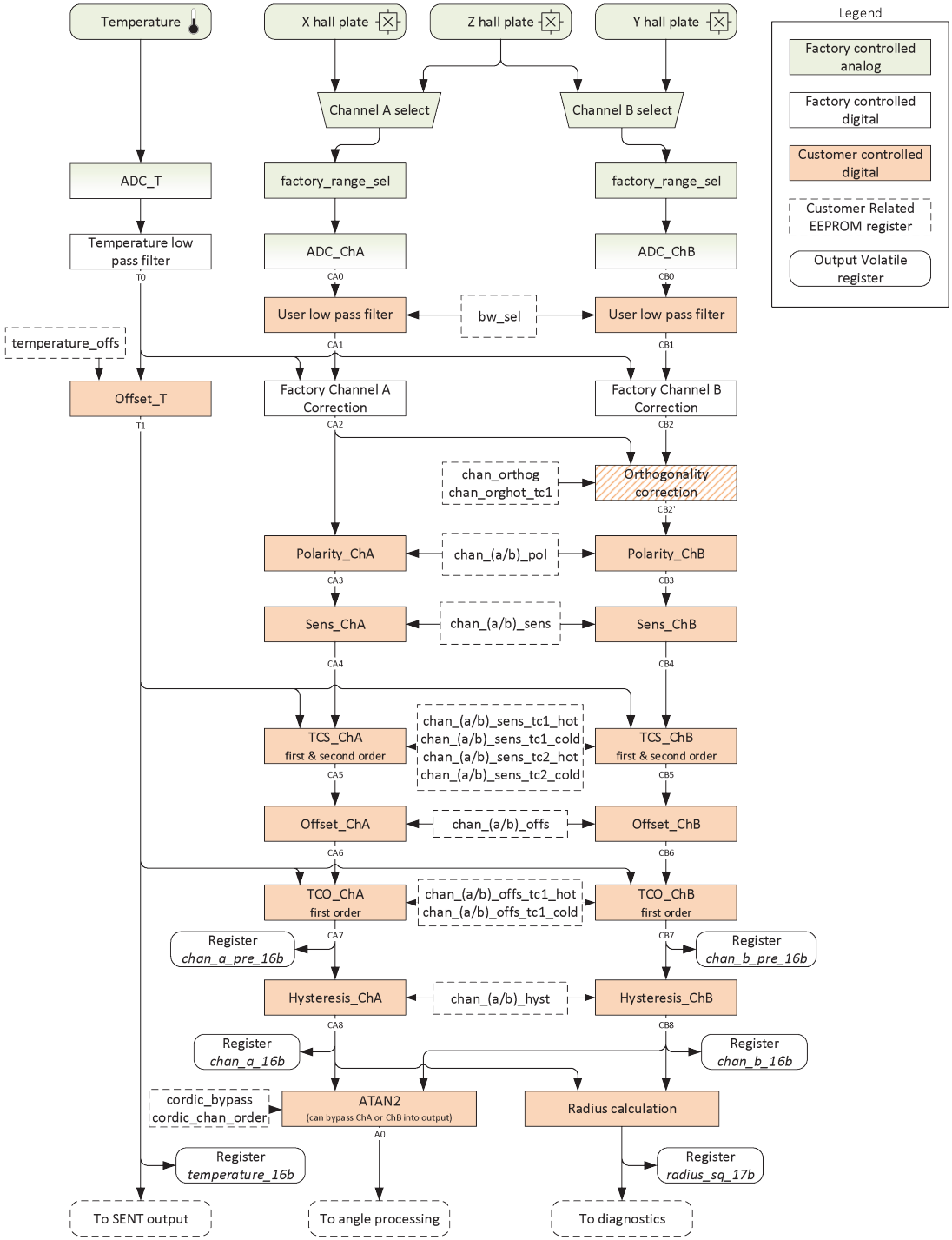



**Figure 4: 1D Signal Path Processing Flow**



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## Signal Path

The A31316 signal path contains two min sections. The first is two 1-D signal paths each reflecting the magnetic field in one direction as specified in the selection guide. The second section uses a CORDIC calculation to determine an angle from the 1-D signals. Both sections provide customer-accessible trim registers for end-of-line calibrations.

## 1-D Signal Path

### FACTORY CHANNEL A / CHANNEL B INPUT SELECTION

Selects the input to Channel A and Channel B. This is programmed at factory level. Use the selection guide to determine which axes are used.

### FACTORY RANGE SELECTION

Factory range selection sets the analog pre-amplifier. The A31316 front end settings are configured for a limited field range. To determine the field range, consult the selection guide.

### CUSTOMER CONTROLLABLE DATA PATH

The data path further processing is performed as by the equations below.

NOTE: If the segment processor correction components are changed by the customer, temperature performance may deviate from specification. The customer must take care in changing these components and assumes liability for temperature performance deviations that come about from the changes applied.

## Customer Trimming

### LOW-PASS FILTER

The user low pass filter allows a noise reduction without data update rate change using a combination of a CIC and IIR filter. The IIR filter is a third-order low pass filter.

Equation 2:

$$CA_1 = LPF(CA_0)$$
$$CB_1 = LPF(CB_0)$$

$$H(z) = \frac{1}{2^{k+1}} \cdot \frac{1 + z^{-1}}{1 - (1 - 2^{-k})z^{-1}}$$

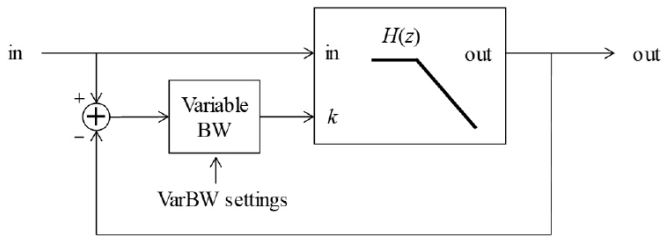



**Figure 5: Low-Pass Filter**

**Table 2: Selection of Customer Low-Pass Filter, EEPROM Parameter *bw_sel***

| bw_sel | 3 dB Frequency (Hz) | 90% Settling (ms) |
|---|---|---|
| 0 | 329.1 | 1.666 |
| 1 | 465.8 | 1.172 |
| 2 | 556 | 0.9925 |
| 3 | 700 | 0.763 |
| 4 | 1000 | 0.554 |
| 5 | 1482 | 0.396 |
| 6 | 2024 | 0.249 |
| 7 | Adaptive | 0.135 |

The adaptive filter has a selectable minimum and maximum bandwidth for increased customization. The minimum and maximum bandwidths are selected via the *bw_adap_min* and *bw_adap_max* registers respectively. The table below shows the corresponding bandwidths for each register. *bw_adap_min* is by default set to code 0 and *bw_adap_max* is by default set to code 7.

**Table 3: bw_adapt_(min/max) Frequencies**

| bw_adapt_(min/max) (LSB) | Frequency (Hz) |
|---|---|
| 0 | 38.9 |
| 1 | 77.8 |
| 2 | 156.3 |
| 3 | 314.8 |
| 4 | 638.7 |
| 5 | 1308.6 |
| 6 | 2672.1 |
| 7 | 4734.2 |

The overall filter response is given below.

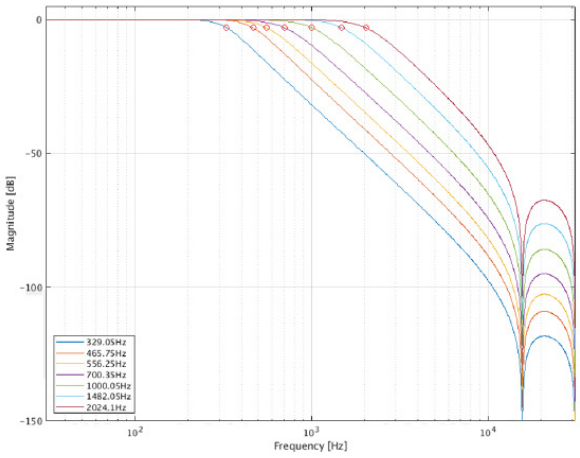



**Figure 6: Overall IIR filter Response Depending on the Selected Bandwidth**



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## SENSOR OUTPUT DURING LOW-PASS FILTER INITIALIZATION

After startup, the low pass filter takes some time to settle. It may be undesirable for the output values to show this settling behavior. For this reason, the parameter *power_on_delay* allows suppressing the sensor output for a configurable amount of time. If desired, the time that the output is suppressed should be set to a value compatible with the filter settling time. It is the user's responsibility to do this. The value is not automatically chosen by the sensor to be compatible with the filter bandwidth setting.

For SENT output, if

- if *sent_encoding_sel* = 1) and *sent_data_sel* = 0, 4, 7, or 15, an initialization code selected by parameter *sent_init_sel* will be transferred for the configured amount of time.
- In other cases, the data will be sent out with SCN[0] = 1 for the configured filter initialization time.

For PWM output, the POR error code will be sent out for the time selected by *power_on_delay*. This error code is represented by the values shown in Table 36. The error may be superseded by errors of higher priority as per Table 36.

The *power_on_delay* options are given in the following table.

**Table 4: Selection of output during low-pass filter startup, EEPROM Parameter *por_on_delay***

| por_on_delay (code) | SENT Additional Init Code Time (ms) / Additional POR Error Time (ms) | PWM POR state duration (ms) |
|---|---|---|
| 0 | 0.5 | 0.5 |
| 1 | 1.0 | 1.0 |
| 2 | 1.5 | 1.5 |
| 3 | 2.0 | 2.0 |
| 4 | 2.5 | 2.5 |
| 5 | 3.0 | 3.0 |
| 6 | 4.0 | 4.0 |
| 7 | none | 0.25 |

## FACTORY CORRECTION

The A31316 devices are factory-trimmed for the channels and field ranges noted in the selection guide. The trim provides a flat TC to all parameters and accuracy to the DS specifications for channel and angle.

$$CA_2 = Factory_{Correction}\ (CA_1)$$

$$CB_2 = Factory_{Correction}\ (CB_1)$$

## ORTHOGONALITY CORRECTION

A factory-trimmed orthogonality correction is implemented. This works by modeling the orthogonality error as a cross-sensitivity from Channel A into Channel B prior to CORDIC calculation.

Equation 3:

$$CB_2' = CB_2 + (Phase_{Corr} \times CA_2)$$

For information on how to adapt the orthogonality correction, contact Allegro MicroSystems.

## POLARITY, OFFSET, TCO, SENSITIVITY, TCS CALIBRATION

Polarity bits are provided for each channel to invert the direction of sensitivity of either or both axes. Polarity change is the first operation performed in the customer trim path. Because of this, it should be set first to ensure the offset is programmed properly.

The offset and sensitivity parameters can be used to help provide a linear output when using the device in any off-axis orientation. The angle output will be linear for well-matched input sensing vectors. When mounting off axis, one dimension often has offset and amplitude variation relative to the other. Using the *chan_(a/b)_offs* and *chan_(a/b)_sens* parameters can correct this system level mismatch, effectively providing a simple two parameter linearization method.

The offset and sensitivity parameters can be used to stabilize the sensor output over temperature. First and second order corrections, separated per channel and separated for temperature above and below 25°C, are provided for post-mounting offset and gain calibration.



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### POLARITY CORRECTION

Equation 4:

$$CA_3 = \begin{cases} CA_2 & \text{for} \quad chan_a_pol = 0 \\ -CA_2 & \text{for} \quad chan_a_pol = 1 \end{cases}$$
$$CB_3 = \begin{cases} CB_2 & \text{for} \quad chan_b_pol = 0 \\ -CB_2 & \text{for} \quad chan_b_pol = 1 \end{cases}$$

### SENSITIVITY ADJUSTMENT

Equation 5:

$CA_4 = CA_3 \times chan_a_sens$
$CB_4 = CB_3 \times chan_b_sens$

The range for *chan_(a/b)_sens* is [0 … 7.9995], with a resolution of $2^{-11}$ = 4.88e-04. The default value is 2048, resulting in a gain of 1.

### SENSITIVITY CORRECTION OVER TEMPERATURE

Equation 6:

$$CA_5 = \begin{cases} CA_4 \times (1 + chan_a_sens_tc1_cold \times (T_0 - 25°C) + chan_a_sens_tc2_cold \times (T_0 - 25°C)^2) & \text{Temperature} < 25°C \\ CA_4 \times (1 + chan_a_sens_tc1_hot \times (T_0 - 25°C) + chan_a_sens_tc2_hot \times (T_0 - 25°C)^2) & \text{Temperature} \geq 25°C \end{cases}$$
$$CB_5 = \begin{cases} CB_4 \times (1 + chan_b_sens_tc1_cold \times (T_0 - 25°C) + chan_b_sens_tc2_cold \times (T_0 - 25°C)^2) & \text{Temperature} < 25°C \\ CB_4 \times (1 + chan_b_sens_tc1_hot \times (T_0 - 25°C) + chan_b_sens_tc2_hot \times (T_0 - 25°C)^2) & \text{Temperature} \geq 25°C \end{cases}$$

The range for *chan_x_sens_tc1_cold* is [$-2^{-7}$ … ($2^{-7} - 2^{-17}$)] = –0.0078 … +0.0078 with a resolution of $2^{-17}$ = 7.63e–06[1/K]
The range for *chan_x_sens_tc1_hot* is [$-2^{-8}$ … ($2^{-8} - 2^{-18}$)] = –0.0039 … +0.0039 with a resolution of $2^{-18}$ = 3.81e–06[1/K]
The range for *chan_x_sens_tc2_cold* is [$-2^{-14}$ … ($2^{-14} - 2^{-23}$)] = –6.10e–05… +6.09e–05 with a resolution of $2^{-23}$ = 1.19e–07[1/K$^2$]
The range for *chan_x_sens_tc2_hot* is [$-2^{-16}$ … ($2^{-16} - 2^{-25}$)] = –1.53e–05… +1.52e–05 with a resolution of $2^{-25}$ = 2.98e–08[1/K$^2$]

### CUSTOMER OFFSET CORRECTION

Equation 7:

$CA_6 = CA_5 + chan_a_offs$
$CB_6 = CB_5 + chan_b_offs$

The range for *chan_b_offs* is –32768 … +32764 with a resolution of 4 LSB.

### CUSTOMER OFFSET CORRECTION OVER TEMPERATURE

Equation 8:

$$CA_7 = \begin{cases} CA_6 + chan_a_offs_tc1_cold \times (T_0 - 25°C) & \text{Temperature} < 25°C \\ CA_6 + chan_a_offs_tc1_hot \times (T_0 - 25°C) & \text{Temperature} \geq 25°C \end{cases}$$
$$CB_7 = \begin{cases} CB_6 + chan_b_offs_tc1_cold \times (T_0 - 25°C) & \text{Temperature} < 25°C \\ CB_6 + chan_b_offs_tc1_hot \times (T_0 - 25°C) & \text{Temperature} \geq 25°C \end{cases}$$

The range for *chan_x_offs_tc1_cold* is [–128 … +127.9375] LSB/K with a resolution of $2^{-4}$ = 0.0625 LSB/K
The range for *chan_x_offs_tc1_hot* is [–256 … +255.875] LSB/K with a resolution of $2^{-3}$ = 0.125 LSB/K



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## HYSTERESIS FILTER

Equation 9:

$CA_8 = Hysteresis_filter(CA_7)$
$CB_8 = Hysteresis_filter(CB_7)$

The hysteresis block limits change in the sensor output to remove noise from the channels. The hysteresis block can be disabled by setting the hysteresis window width to zero. The hysteresis block input as measured by the sensor is at the "head" of the hysteresis window. As long as the hysteresis input ($CA_7$/$CB_7$) advances in the same direction of rotation, the hysteresis output ($CA_8$/$CB_8$) will be unchanged, minimizing latency. If the hysteresis input ($CA_7$/$CB_7$) reverses direction, the hysteresis output is held static until the input data exit the hysteresis window in either direction. If the exit is in the opposite direction of movement as to where the "head" was, the head flips to the opposite end of the hysteresis window and that becomes the new reference direction. On sensor reset, the first value change is accepted as initial direction. The behavior of the hysteresis block is shown in Figure 6.

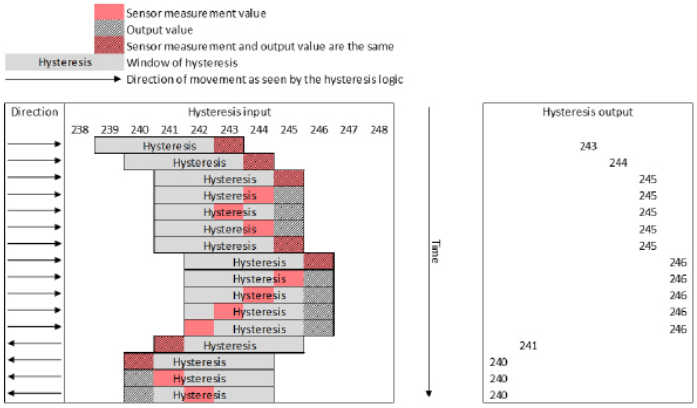



**Figure 7: Input and Output Example of Hysteresis Block**

The range for *chan_(a/b)_hyst* is [0 … 1023] LSB with a resolution of 1 LSB.

## DIRECT OUTPUT REGISTER

The Channel A and Channel B data can be read directly through the digital interface for customer trimming and in-application debugging purposes.

Equation 10:

$chan_a_16b[15:0] = CA_8$
$chan_b_16b[15:0] = CB_8$

## ATAN INPUT SELECTION

In order to provide the angle output from the 3D Hall elements, the two-input function "atan2" is used. It is internally implemented using the CORDIC algorithm. The sine and cosine inputs to the ATAN2 are user selectable based on the EEPROM parameter cordic_chan_order. The CORDIC algorithm will calculate the arctangent to provide the angle between the two input vectors. This angle is related to the linear position in slide-by long stroke applications. A bypass option is provided to route the CA or CB information directly to the next processing steps. This allows for use of the A31316 as a 1-D sensor. When bypassing the ATAN2 calculation, the most negative 1-D value (–32768) becomes an angle of 0° (value 0), a zero value of the 1-D channel becomes 180° (value 32768), and the most positive value of the 1-D channel becomes 359.99° (value 65535).

Equation 11:

$$A_0 = \begin{cases} \text{atan2}(B_8, C_8) & cordic_bypass = 0,\ cordic_chan_order = 0 \\ \text{atan2}(C_8, B_8) & cordic_bypass = 0,\ cordic_chan_order = 1 \\ B_8 + 32768 & cordic_bypass = 1,\ cordic_chan_order = 0 \\ C_8 + 32768 & cordic_bypass = 1,\ cordic_chan_order = 1 \end{cases}$$

Note: in the equation above, atan2(0,1) = 0°, atan2(1,0) = +90°, atan2(0,–1) = +180°, and atan2(–1,0) = +270°. This follows from the function definition of θ = atan2(sin(θ),cos(θ)) as it is implemented in MATLAB. Microsoft Excel has the input arguments in the opposite sequence.



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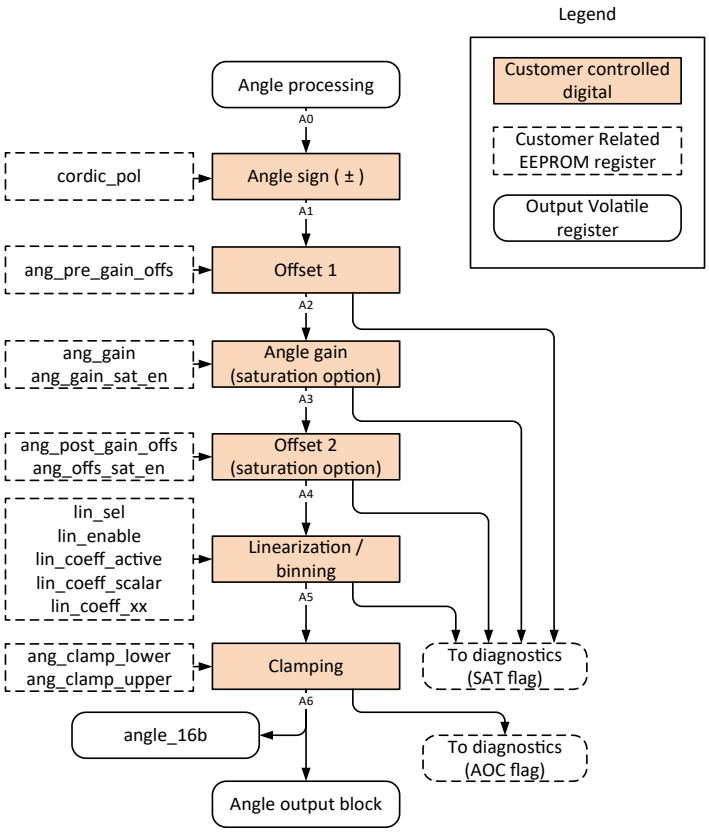



**Figure 8: Angle Signal Path Processing Flow**

## PRE-GAIN ANGLE OFFSET CORRECTION

A31316 contains a programmable zero angle point allowing the electrical zero angle to be adjusted from the magnetic angle to match mechanical orientations. This is provided in the form of an angle offset correction at the output of the angle averaging filter. This offset is a full-scale offset with a range of 0 to 360 degrees following Equation 12.

Equation 12:

$$A_1 = mod(A_0 + ang_pre_gain_offs, 360°)$$

The output of the pre-gain offset correction block, $A_2$ is always allowed to roll over from max output to min output as needed. It is possible to compare the output angle of this block to programmed limits using the parameters *ang_thresh_low and ang_thresh_high*, if *ang_thresh_en* = 1. These limits do not saturate the $A_2$ angle, but can be used to cause a saturation flag.

The range for *ang_pre_gain_offs* is [0 … 359.989013671875] ° with a resolution of 360 / $2^{15}$ = 0.010986328125.

The range for *ang_thresh_low* is [0 … 358.59375] ° with a resolution of 360 / $2^8$ = 1.40625°.

The range for *ang_thresh_high* is [0 … 358.59375] ° with a resolution of 360 / $2^8$ = 1.40625°.

See section “Saturation Flag (SAT)” regarding the possible diagnostics for this block.

## ANGLE GAIN CORRECTION

Following the initial angle offset correction, there is an angle gain block. This gain correction, defined by the EEPROM parameter *ang_gain*, allows inputs to be scaled to any desired output range. This can be to increase inputs as is short stroke rotary applications or slide by linear applications to provide the desired output range, or to reduce the inputs if a reduced range is desired for a full output range.

The range for *ang_gain* is [0 … 63.9990234375] with a resolution of $2^{-10}$ = 0.0009765625. Setting the gain to zero results in a zero output of the block and has no practical use.

If the gain is set to a value larger than 1.0x, some input values would result in an output angle larger than 360°. In this case, the output of the angle gain block, $A_3$, can either saturate to max code, or roll over, depending on the preference set by the EEPROM parameter *ang_gain_sat_en*.

If *ang_gain_sat_en* = 0, the output will roll over from 360° to restart from 0°.

If *ang_gain_sat_en* = 1 (saturation after gain enabled), and gain is set to >1, the output will saturate to 360° instead of rolling over. After that, there will be a point where the sensor’s output jumps from 360° to 0°. This point, measured in pre-gain angle $A_2$, is user configurable using the parameter *ang_sat_rollover*. This is displayed in Figure 8.

The range for *ang_sat_rollover* is [0 … 358.59375] ° with a step size of 360° / $2^8$ ≈ 1.40625°.

In most applications, it will be safest to put the output discontinuity of the chip is as far away as possible from the range that is being gained up. This is achieved by setting *ang_sat_rollover*=180°+(180°)/”*ang_gain*” . For example, with *ang_gain* set to 4x, the recommended value in degrees for *ang_sat_rollover* would be 225°. This is equal to a register value of *ang_sat_*



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*rollover*=round($2^8 \cdot (225°)/(360°)$)=160. The value for *ang_sat_rollover* must be larger than 360°/*ang_gain.*

The behavior is summarized by the following equations:

Equation 13:

If *ang_gain_sat_en* = 0:

$A_2 = mod(A_1 \times ang_gain, 360)$

Equation 14:

If *ang_gain_sat_en* = 1:

$$A_1 = \begin{cases} \text{ang_gain} \times A_1 & \text{for} \quad A_1 \le \left(\dfrac{360°}{\text{ang_gain}}\right) \\ 359.9945° & \text{for} \quad \left(\dfrac{360°}{\text{ang_gain}}\right) < A_1 \le \text{ang_sat_rollover} \\ 0° & \text{for} \quad A_1 > \text{ang_sat_rollover} \end{cases}$$

As an example, the output function for a setting of *ang_gain* = 4, *ang_gain_sat_en* = 1, and *ang_sat_rollover* = 225° is given in the figure below:

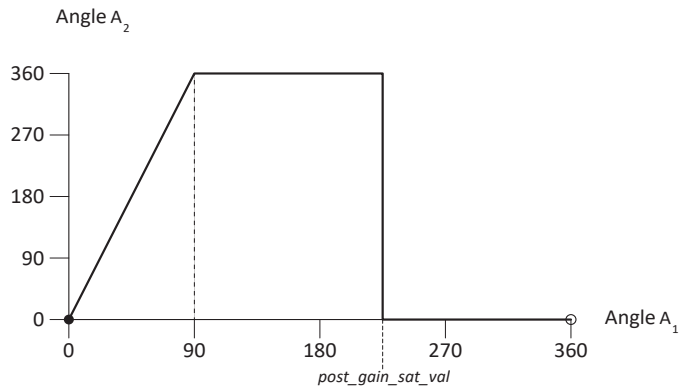



**Figure 9: Angle gain behavior over full rotation with gain = 4 and output clamping enabled**

As a second example, the output function for a setting of *ang_gain* = 3 and *ang_gain_sat_en* = 0 is given below:

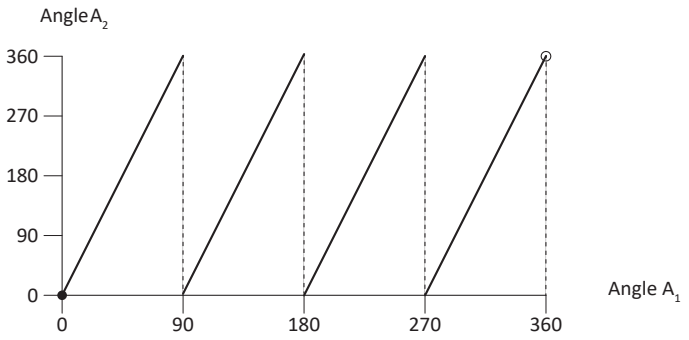



**Figure 10: Angle gain behavior over full rotation with gain = 3 and ang_gain_sat_en = 0**

See section “Saturation Flag (SAT)” regarding the possible diagnostics for this block.

## POST GAIN ANGLE OFFSET CORRECTION

After the Gain Block, there is an additional offset correction block to allow full flexibility of angle programming. The user can optionally saturate the output of the Post Gain Angle Offset block or allow to rollover using the EEPROM parameter *ang_offs_sat_en*.

Equation 15:

$$A_3 = \begin{cases} mod(A_2 + ang_post_gain_offs, 360) & \text{for } ang_offs_sat_en = 0 \\ \min(\max(A_2 + ang_post_gain_offs, 0), 359.9945) & \text{for } ang_offs_sat_en = 1 \end{cases}$$

The range for *ang_post_gain_offs* is [–360 … 359.9890137] ° with a step size of 720° / $2^{16}$ ≈ 0.010986328125°.

See section “Saturation Flag (SAT)” regarding the possible diagnostics for this block.



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## ANGLE SIGN (ROTATION DIRECTION)

The A31316 has a bit in EEPROM, *cordic_pol* designating the polarity of the angle reading of the device, determined by whether increasing output for clockwise or counterclockwise rotation. Since each channel can be inverted individually in the channel path, this setting must be combined with the channel polarity bits to determine which direction of rotation is considered positive.

Equation 16:

$$A_4 = \begin{cases} A_3 & \text{for} \quad cordic_pol = 0 \\ 360° - A_3 & \text{for} \quad cordic_pol = 1 \end{cases}$$

## LINEARIZATION AND BINNING

The A31316 contains two different means of producing an output based on any sensed angle waveform. These options are in the form of a segmented linearization, and a discretized output option called Binning mode. Each of these options allow for the use of up to 33 fixed points to quantize the angle output, or the ability to apply the segment endpoints at configurable sensed angle locations.

See section “Saturation Flag (SAT)” regarding the possible diagnostics for this block.

## LINEARIZATION / BINNING MODE SELECTION

The preferred mode is selected by the EEPROM parameter *lin_mode*, as shown in Table 9 and depicted in Figure 10.

**Table 5: Linearization / binning mode selection**

| lin_mode Code | Output Transfer Function Option |
|---|---|
| 0 | Fixed Segment Linearization |
| 1 | Fixed Segment Binning Mode |
| 2 | Variable Segment Linearization Mode |
| 3 | Variable Segment Binning Mode |

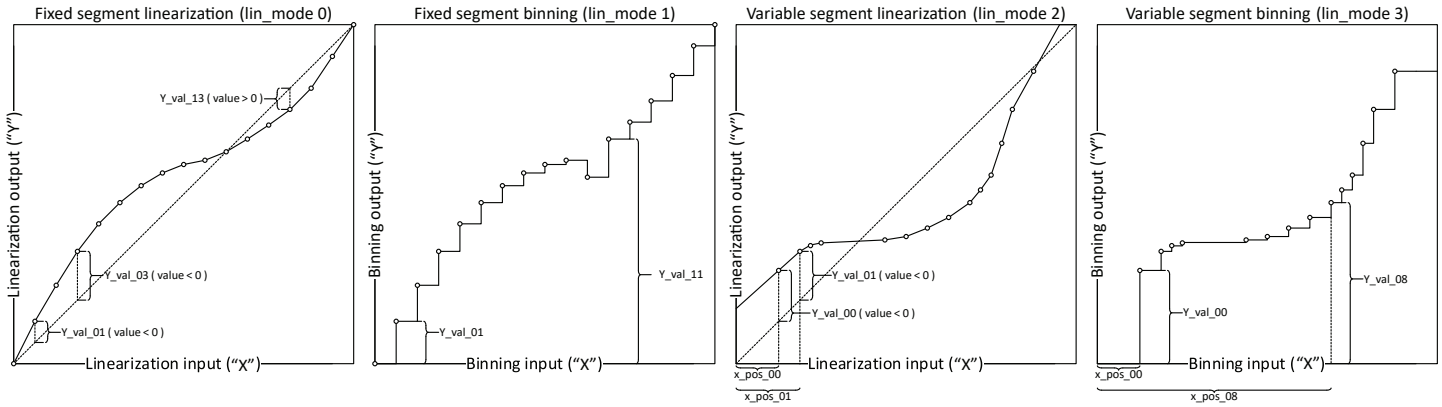



**Figure 11: Linearization and Binning Modes**



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## FIXED SEGMENT LINEARIZATION (LIN_MODE 0)

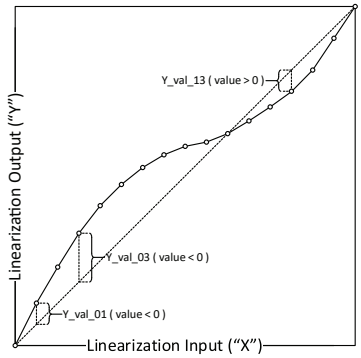



**Figure 12: Fixed-Segment Linearization**

In fixed-segment linearization mode, between 2 and 33 output correction points are equidistantly positioned between 0° and 360° input. The correction codes *Y_val_xx* are in signed 13-bit format and represent a correction using the format in the table below:

**Table 6: *Y_val_xx* range depending on *lin_coeff_scalar* setting**

| lin_coeff_ scalar | Range (°) | Value for code –4096 (°) | Value for code +4095 (°) | Step size (°) |
|---|---|---|---|---|
| 0 | ±45 | +45 | –44.99 | $90/2^{13} \approx 0.011$ |
| 1 | ±90 | +90 | –89.98 | $180/2^{13} \approx 0.022$ |
| 2 | ±180 | +180 | –179.96 | $360/2^{13} \approx 0.044$ |
| 3 | ±360 | +360 | –359.91 | $720/2^{13} \approx 0.088$ |

Most applications will have monotonically rising outputs. However, the sensor can support rising and falling outputs if needed.

If the result of the linearization is outside the 0–360° range, the value will be clipped to 0° or 360°. No overflow will happen in the linearization block. This means that for rotary applications, the 0° correction value and the 360° correction value must both be set to 0

## FIXED SEGMENT BINNING (LIN_MODE 1)

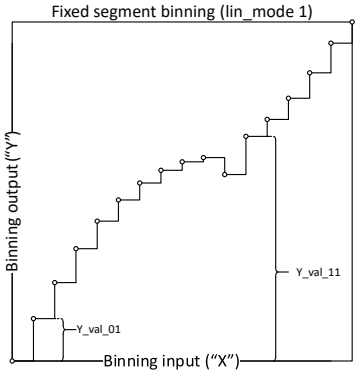



**Figure 13: Fixed-Segment Binning**

In fixed-segment binning mode, between 2 and 33 bins are equidistantly positioned between 0° and 360° input. The binning output codes *Y_val_xx* are in unsigned 13-bit format and represent an output value of 0° (*Y_val_xx* = 0) and 359.96° (*Y_val_xx* = 8191). Any value is mapped to the bin with a lower value than the input. The parameter *lin_coeff_scalar* has no meaning in binning mode. The *Y_val_xx* values do not need to be in any special order.



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## VARIABLE SEGMENT LINEARIZATION (LIN_MODE 2)

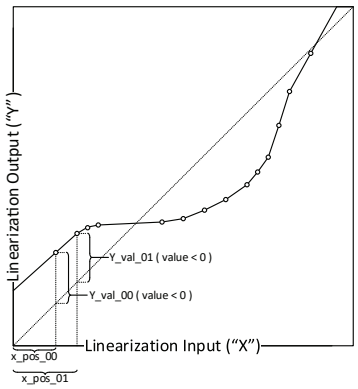



**Figure 14: Variable Segment Linearization**

In variable-segment linearization mode, between 2 and 22 output correction points are positioned at user-selected positions. The correction codes *Y_val_xx* are in signed 13-bit format and represent a correction using the format in the table below:

**Table 7: Y_val_xx range depending on lin_coeff_scalar setting**

| lin_coeff_ scalar | Range (°) | Value for code –4096 (°) | Value for code +4095 (°) | Step size (°) |
|---|---|---|---|---|
| 0 | ±45 | +45 | –44.99 | $90/2^{13} \approx 0.011$ |
| 1 | ±90 | +90 | –89.98 | $180/2^{13} \approx 0.022$ |
| 2 | ±180 | +180 | –179.96 | $360/2^{13} \approx 0.044$ |
| 3 | ±360 | +360 | –359.91 | $720/2^{13} \approx 0.088$ |

Most applications will have monotonically rising outputs. However, the sensor can support rising and falling outputs if needed.

The position codes *X_pos_xx* are in unsigned 6-bit format and represent positions of 0° (*X_pos_xx* = 0) to 354.375° (*X_pos_xx* = 63). The X values must be placed in a rising manner, so that the value of $X_pos(n+1) \geq X_pos(n)$.

If the result of the linearization is outside the 0–360° range, the value will be clipped to 0° or 360°. No overflow will happen in the linearization block. This means that for rotary applications, the 0° correction value and the 360° correction value must both be set to 0.

For input values below the angle defined by the *X_pos_00* value, the linearization function will extrapolate the slope set by the first two defined points. For input angles above the angle defined by the last *X_pos_xx* value, the linearization function will extrapolate the slope set by the last two defined points. For input angles between 354.375° and 360°, this will always happen, and there is no other way to control the behavior in this area than by making use of the extrapolation of the two previous points. The extrapolating behavior is shown in Figure 13 for both low and high input values

## VARIABLE SEGMENT BINNING (LIN_MODE 3)

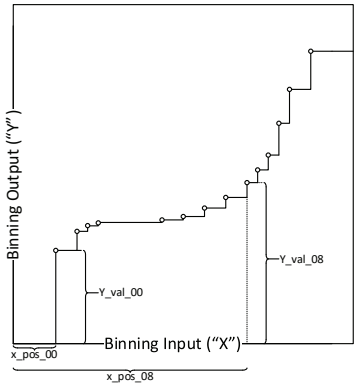



**Figure 15: Variable Segment Binning**

In variable-segment binning mode, between 2 and 21 bins are equidistantly positioned between 0° and 360° input. The binning output codes *Y_val_xx* are in unsigned 13-bit format and represent an output value of 0° (*Y_val_xx* = 0) and 359.96° (*Y_val_xx* = 8191). Any value is mapped to the bin as an input angle below that of the input, i.e. the bin that the output ends up in is the bin whose X value is "to the left" of the measured angle. The parameter *lin_coeff_scalar* has no meaning in binning mode.

The position codes *X_pos_xx* are in unsigned 6-bit format and represent positions between 0° (*X_pos_xx* = 0) and 354.375° (*X_pos_xx* = 63). The X values must be placed in a rising manner, so that the value of $X_pos_(n+1) \geq X_pos_(n)$.

If *X_pos_00* does not define a bin at position 0°, a bin with *X_pos* = 0°, *Y_val* = 0° will be automatically assumed.

## LINEARIZATION/BINNING PARAMETER STORAGE

The individual linearization/binning parameters are stored in the EEPROM parameters *lin_coeff_00 … lin_coeff_32*. Depending on the linearization/binning configuration, the contents of these memory locations have different meanings. All modes and EEPROM field contents are listed in Table 12. Parameters that are not used for linearization may be used otherwise. The parameters *lin_coeff_17 … lin_coeff_31* can be sent out through the SENT enhanced serial message for certain constants (see Table 20). If they are used in this manner, the parameter *coeff_active* must be set in such a way that these two usages do not interfere (see Table 13).



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**Table 8: Linearization/Binning parameter storage**

| EEPROM Coefficient | Fixed position linearization (lin_mode 0) | Fixed position binning (lin_mode 1) | Variable segment linearization (lin_mode 2) | Variable segment binning (lin_mode 3) | SENT emsg |
|---|---|---|---|---|---|
| | 12 11 10 9 8 7 6 5 4 3 2 1 0 | 12 11 10 9 8 7 6 5 4 3 2 1 0 | 12 11 10 9 8 7 6 5 4 3 2 1 0 | 12 11 10 9 8 7 6 5 4 3 2 1 0 | |
| lin_coeff_00 | Y_val_00 (signed 13 bit) | Y_val_00 (unsigned 13 bit) | X_pos_01 (uns. 6 bit) X_pos_00 (uns. 6 bit) | X_pos_01 (uns. 6 bit) X_pos_00 (uns. 6 bit) | |
| lin_coeff_01 | Y_val_01 (signed 13 bit) | Y_val_01 (unsigned 13 bit) | X_pos_03 (uns. 6 bit) X_pos_02 (uns. 6 bit) | X_pos_03 (uns. 6 bit) X_pos_02 (uns. 6 bit) | |
| lin_coeff_02 | Y_val_02 (signed 13 bit) | Y_val_02 (unsigned 13 bit) | X_pos_05 (uns. 6 bit) X_pos_04 (uns. 6 bit) | X_pos_05 (uns. 6 bit) X_pos_04 (uns. 6 bit) | |
| lin_coeff_03 | Y_val_03 (signed 13 bit) | Y_val_03 (unsigned 13 bit) | X_pos_07 (uns. 6 bit) X_pos_06 (uns. 6 bit) | X_pos_07 (uns. 6 bit) X_pos_06 (uns. 6 bit) | |
| lin_coeff_04 | Y_val_04 (signed 13 bit) | Y_val_04 (unsigned 13 bit) | X_pos_09 (uns. 6 bit) X_pos_08 (uns. 6 bit) | X_pos_09 (uns. 6 bit) X_pos_08 (uns. 6 bit) | |
| lin_coeff_05 | Y_val_05 (signed 13 bit) | Y_val_05 (unsigned 13 bit) | X_pos_11 (uns. 6 bit) X_pos_10 (uns. 6 bit) | X_pos_11 (uns. 6 bit) X_pos_10 (uns. 6 bit) | |
| lin_coeff_06 | Y_val_06 (signed 13 bit) | Y_val_06 (unsigned 13 bit) | X_pos_13 (uns. 6 bit) X_pos_12 (uns. 6 bit) | X_pos_13 (uns. 6 bit) X_pos_12 (uns. 6 bit) | |
| lin_coeff_07 | Y_val_07 (signed 13 bit) | Y_val_07 (unsigned 13 bit) | X_pos_15 (uns. 6 bit) X_pos_14 (uns. 6 bit) | X_pos_15 (uns. 6 bit) X_pos_14 (uns. 6 bit) | |
| lin_coeff_08 | Y_val_08 (signed 13 bit) | Y_val_08 (unsigned 13 bit) | X_pos_17 (uns. 6 bit) X_pos_16 (uns. 6 bit) | X_pos_17 (uns. 6 bit) X_pos_16 (uns. 6 bit) | |
| lin_coeff_09 | Y_val_09 (signed 13 bit) | Y_val_09 (unsigned 13 bit) | X_pos_19 (uns. 6 bit) X_pos_18 (uns. 6 bit) | X_pos_19 (uns. 6 bit) X_pos_18 (uns. 6 bit) | |
| lin_coeff_10 | Y_val_10 (signed 13 bit) | Y_val_10 (unsigned 13 bit) | X_pos_21 (uns. 6 bit) X_pos_20 (uns. 6 bit) | X_pos_20 (uns. 6 bit) | |
| lin_coeff_11 | Y_val_11 (signed 13 bit) | Y_val_11 (unsigned 13 bit) | Y_val_00 (signed 13 bit) | Y_val_00 (unsigned 13 bit) | |
| lin_coeff_12 | Y_val_12 (signed 13 bit) | Y_val_12 (unsigned 13 bit) | Y_val_01 (signed 13 bit) | Y_val_01 (unsigned 13 bit) | |
| lin_coeff_13 | Y_val_13 (signed 13 bit) | Y_val_13 (unsigned 13 bit) | Y_val_02 (signed 13 bit) | Y_val_02 (unsigned 13 bit) | |
| lin_coeff_14 | Y_val_14 (signed 13 bit) | Y_val_14 (unsigned 13 bit) | Y_val_03 (signed 13 bit) | Y_val_03 (unsigned 13 bit) | |
| lin_coeff_15 | Y_val_15 (signed 13 bit) | Y_val_15 (unsigned 13 bit) | Y_val_04 (signed 13 bit) | Y_val_04 (unsigned 13 bit) | |
| lin_coeff_16 | Y_val_16 (signed 13 bit) | Y_val_16 (unsigned 13 bit) | Y_val_05 (signed 13 bit) | Y_val_05 (unsigned 13 bit) | |
| lin_coeff_17 | Y_val_17 (signed 13 bit) | Y_val_17 (unsigned 13 bit) | Y_val_06 (signed 13 bit) | Y_val_06 (unsigned 13 bit) | $03 |
| lin_coeff_18 | Y_val_18 (signed 13 bit) | Y_val_18 (unsigned 13 bit) | Y_val_07 (signed 13 bit) | Y_val_07 (unsigned 13 bit) | $05 |
| lin_coeff_19 | Y_val_19 (signed 13 bit) | Y_val_19 (unsigned 13 bit) | Y_val_08 (signed 13 bit) | Y_val_08 (unsigned 13 bit) | $06 |
| lin_coeff_20 | Y_val_20 (signed 13 bit) | Y_val_20 (unsigned 13 bit) | Y_val_09 (signed 13 bit) | Y_val_09 (unsigned 13 bit) | $07 |
| lin_coeff_21 | Y_val_21 (signed 13 bit) | Y_val_21 (unsigned 13 bit) | Y_val_10 (signed 13 bit) | Y_val_10 (unsigned 13 bit) | $08 |
| lin_coeff_22 | Y_val_22 (signed 13 bit) | Y_val_22 (unsigned 13 bit) | Y_val_11 (signed 13 bit) | Y_val_11 (unsigned 13 bit) | $09 |
| lin_coeff_23 | Y_val_23 (signed 13 bit) | Y_val_23 (unsigned 13 bit) | Y_val_12 (signed 13 bit) | Y_val_12 (unsigned 13 bit) | $0A |
| lin_coeff_24 | Y_val_24 (signed 13 bit) | Y_val_24 (unsigned 13 bit) | Y_val_13 (signed 13 bit) | Y_val_13 (unsigned 13 bit) | $90 |
| lin_coeff_25 | Y_val_25 (signed 13 bit) | Y_val_25 (unsigned 13 bit) | Y_val_14 (signed 13 bit) | Y_val_14 (unsigned 13 bit) | $91 |
| lin_coeff_26 | Y_val_26 (signed 13 bit) | Y_val_26 (unsigned 13 bit) | Y_val_15 (signed 13 bit) | Y_val_15 (unsigned 13 bit) | $92 |
| lin_coeff_27 | Y_val_27 (signed 13 bit) | Y_val_27 (unsigned 13 bit) | Y_val_16 (signed 13 bit) | Y_val_16 (unsigned 13 bit) | $93 |
| lin_coeff_28 | Y_val_28 (signed 13 bit) | Y_val_28 (unsigned 13 bit) | Y_val_17 (signed 13 bit) | Y_val_17 (unsigned 13 bit) | $94 |
| lin_coeff_29 | Y_val_29 (signed 13 bit) | Y_val_29 (unsigned 13 bit) | Y_val_18 (signed 13 bit) | Y_val_18 (unsigned 13 bit) | $95 |
| lin_coeff_30 | Y_val_30 (signed 13 bit) | Y_val_30 (unsigned 13 bit) | Y_val_19 (signed 13 bit) | Y_val_19 (unsigned 13 bit) | $96 |
| lin_coeff_31 | Y_val_31 (signed 13 bit) | Y_val_31 (unsigned 13 bit) | Y_val_20 (signed 13 bit) | Y_val_20 (unsigned 13 bit) | $97 |
| lin_coeff_32 | Y_val_32 (signed 13 bit) | Y_val_32 (unsigned 13 bit) | Y_val_21 (signed 13 bit) | | |



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### NUMBER OF LINEARIZATION / BINNING POINTS

All modes have a configurable number of activated linearization/ binning points. The number of active points is selected with the parameter *coeff_active*:

**Table 9: Linearization / binning mode parameters used depending on *coeff_active***

| *coeff_active* setting | Number of Active Coefficients | | | |
|---|---|---|---|---|
| | ***lin_sel* 0** fixed segment linearization | ***lin_sel* 1** fixed segment binning | ***lin_sel* 2** variable segment linearization | ***lin_sel* 3** variable segment binning [2] |
| 0 | 33 | 32 | 2 | 1 [1] |
| 1 | 17 | 16 | 2 | 2 |
| 2 | 9 | 8 | 3 | 3 |
| 3 | 5 | 4 | 4 | 4 |
| 4 | 3 | 2 | 5 | 5 |
| 5 | 2 | 1 [1] | 6 | 6 |
| 6 | 2 | 1 [1] | 7 | 7 |
| 7 | 2 | 1 [1] | 8 | 8 |
| 8 | 2 | 1 [1] | 9 | 9 |
| 9 | 2 | 1 [1] | 10 | 10 |
| 10 | 2 | 1 [1] | 11 | 11 |
| 11 | 2 | 1 [1] | 12 | 12 |
| 12 | 2 | 1 [1] | 13 | 13 |
| 13 | 2 | 1 [1] | 14 | 14 |
| 14 | 2 | 1 [1] | 15 | 15 |
| 15 | 2 | 1 [1] | 16 | 16 |
| 16 | 2 | 1 [1] | 17 | 17 |
| 17 | 2 | 1 [1] | 18 | 18 |
| 18 | 2 | 1 [1] | 19 | 19 |
| 19 | 2 | 1 [1] | 20 | 20 |
| 20 | 2 | 1 [1] | 21 | 21 |
| 21...31 | 2 | 1 [1] | 22 | 21 |

[1] Single coefficient settings for binning mode serve no practical purpose. The output will always be equal to the set value.
[2] In lin_sel = 3, if X_pos_00 does not define a bin at position 0°, a bin with X_pos = 0°, Y_val = 0° will be automatically assumed.

### BINNING MODE HYSTERESIS

To prevent chattering around the transition threshold between the bins, the A31316 contains internal hysteresis control in binning mode. The *bin_hyst* parameter will establish the hysteresis in codes below the threshold, which the input into the binning block must pass before changing to the lower bin. This prevents expected noise and drift from changing the desired output bin for the designated output range. The binning hysteresis is controlled using the parameter *bin_hyst*. The default value of *bin_hyst* = 0 results in no hysteresis being applied.

The range for *bin_hyst* is [0… 11.162109375]° with a step size of 11.25° / $2^7$ = 0.087890625°.

## Output Clamps

The A31316 contains a digital clamp feature that can clamp the digital output range of the device. These high and low clamps are both programmable to the entire output range of the device. If the input to the clamp block exceeds the upper clamp value, the output is set to the upper clamp value. Similarly, if the input to the clamp block is less than the lower clamp value, the output is set to the lower clamp value. If high and low clamp value are equal, the output will equal the clamp value. This can be practical for testing purposes. If the low clamp value is set to a higher value than the high clamp value, the output will equal the low clamp number. This configuration has no practical use.

Equation 17:

$$A_6 = \max(ang_clamp_lower, \min(ang_clamp_upper, A_5))$$

The range for *ang_clamp_upper* is [0 … 65535] LSB with a step size of 1 LSB.

The range for *ang_clamp_lower* is [0 … 65535] LSB with a step size of 1 LSB.



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## OUTPUT PROTOCOLS

### PWM Output Mode

PWM involves converting the output value to a series of constant-frequency binary pulses, with the percentage of the high portion of the pulse varied in direct proportion to the digital angle.

The PWM output mode (*dig_out_sel* = 0) is configured by setting the carrier frequency and diagnostic reporting options in EEPROM. The slew rate of the edges may be adjusted using the EEPROM parameter *dig_out_pull_lim* and *dig_out_drive_sel*. See Digital output pin drive strength options for more information.

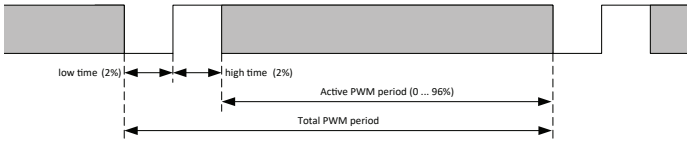



**Figure 16: PWM Frame Format**

**Table 10: PWM Carrier Frequency, EEPROM Parameter dig_out_data_rate**

| EEPROM Code | PWM Frequency (Hz) | Output Resolution (bit) |
|---|---|---|
| 0 or 16 (X0000) | 125 | 15 |
| 1 or 17 (X0001) | 167 | 15 |
| 2 or 18 (X0010) | 250 | 14 |
| 3 or 19 (X0011) | 333 | 14 |
| 4 or 20 (X0100) | 500 | 13 |
| 5 or 21 (X0101) | 667 | 13 |
| 6 or 22 (X0110) | 800 | 13 |
| 7 or 23 (X0111) | 1000 | 12 |
| 8 or 24 (X1000) | 1333 | 12 |
| 9 or 25 (X1001) | 1600 | 12 |
| 10 or 26 (X1010) | 2000 | 11 |
| 11 or 27 (X1011) | 2667 | 11 |
| 12 or 28 (X1100) | 4000 | 10 |
| 13 or 29 (X1101) | 5333 | 10 |
| 14 or 30 (X1110) | 8000 | 9 |
| 15 or 31 (X1111) | 16000 | 8 |

### PWM Sampling Time

The data for the PWM output is sampled at the beginning of each frame, as shown in Figure 176. In the figure, Data 0, 1, 3, 5, 7 and 8 are transmitted. Data 2, 4, 6 and 9 are discarded.

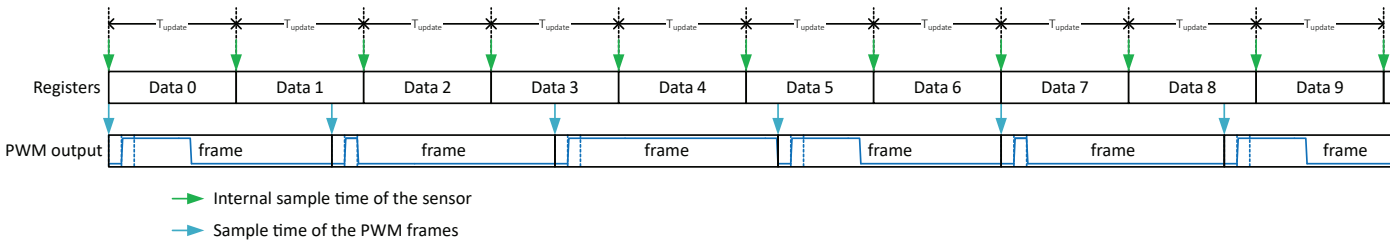



**Figure 17: PWM Frame Sampling Timing**



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## SENT Output Mode

The Single Edge Nibble Transmission (SENT) output mode converts the calculated angle to a binary value mapped to the Full Scale Output, FSO, range of 0 to 4095, as shown in Figure 17 (for a 12 bit output). This data is inserted into a binary pulse message, referred to as a frame that conforms to the SENT data transmission specification (SAEJ2716 APRIL2016). Certain parameters for configuration of the SENT messages can be set in EEPROM.

The SENT output mode is configured by setting the following parameters in EEPROM:

- SAE J2716 SENT with enhancement options (*dig_out_sel* = 1 (no pause pulse), *dig_out_sel* = 2 (pause pulse)).
- Additional configuration parameters in EEPROM.

## Message Structure

A SENT message is a series of nibbles. Each nibble is an ordered pair of a low-voltage interval followed by a high-voltage interval. The low interval is defined as 5 SENT ticks. The high interval contains information and is variable in duration to indicate the data payload of the nibble. The duration of a nibble is denominated in ticks. The period of a tick is set by *dig_out_data_rate* parameter. The duration of the nibble is the sum of the low-voltage interval plus the high-voltage interval. The slew rate of the falling edge may be adjusted using the EEPROM parameter *dig_out_pull_lim*.

The nibbles of a SENT message are arranged in the following required sequence (see Figure 187):

1. Synchronization and Calibration: flags the start of the SENT message.
2. Status and Communication: provides A31316 status.
3. Data: magnetic field and optional data.
4. CRC(Cyclical Redundancy Check): error checking.
5. Pause Pulse: sets timing relative to a constant message frame length. See section SENT output rate for the settings.

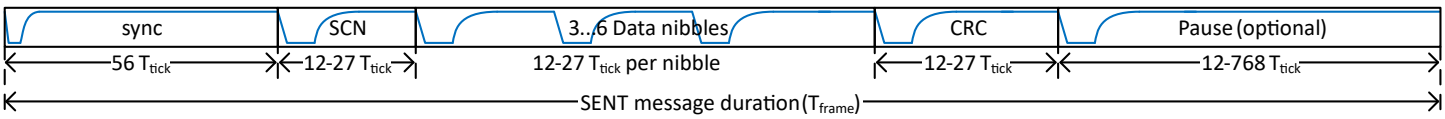



**Figure 18: General Format for SENT message**

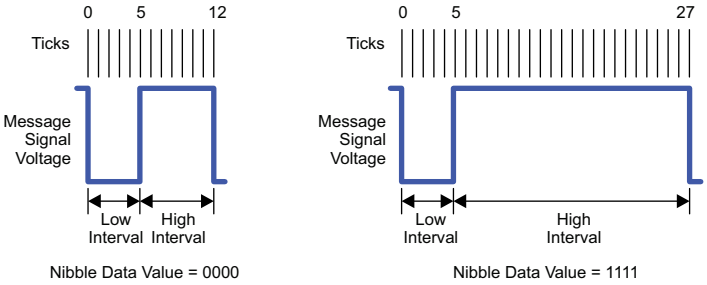



**Figure 19: General SENT Nibble Composition**

**Table 11: SENT Nibble composition and value**

| Quantity of Ticks | | | Binary (4-bit) Value | Decimal Equivalent Value |
|---|---|---|---|---|
| Low-Voltage Interval | High-Voltage Interval | Total | | |
| 5 | 7 | 12 | 0000 | 0 |
| 5 | 8 | 13 | 0001 | 1 |
| 5 | 9 | 14 | 0010 | 2 |
| ⋮ | ⋮ | ⋮ | ⋮ | ⋮ |
| 5 | 21 | 26 | 1110 | 14 |
| 5 | 22 | 27 | 1111 | 15 |



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## SENT Sampling Time

The SENT output data is sampled 33 ticks prior to the start of the SCN nibble. If beginning a new serial message, it is also composed at this time. This is detailed in Figure 19. In the figure, Data 1 and Data 5 are sent out. Others are discarded.

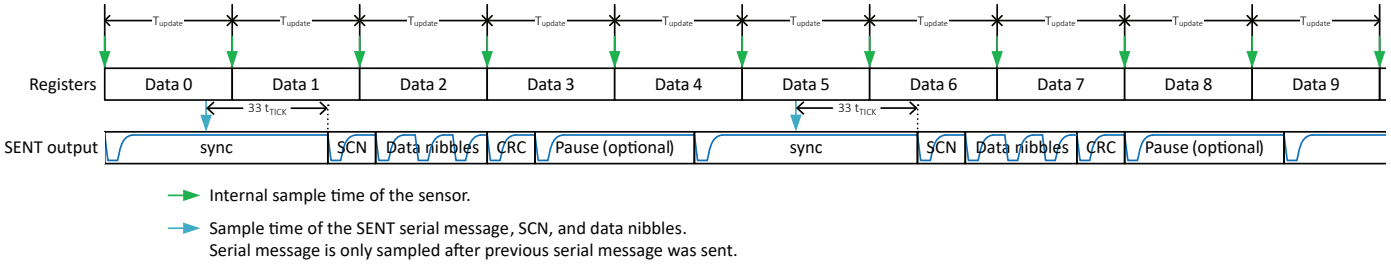



**Figure 20: SENT Frame Sample Timing**

## SENT Output Rate

The SENT output rate depends on the SENT mode. In regular SENT, the frame length is defined by the frame contents. Using SENT-Pause, the frame length is constant. The length of the frames can be selected. There are four options for the frame length settings. Using *sent_frame_rate* = 0, the shortest possible pause-pulse that can achieve a fixed frame duration is used, with the calculation shown in the table below. Using the options *sent_frame_rate* = 1, 2 or 3, a fixed frame rate, measured in ms rather than ticks, can be selected. Settings are detailed in Table 16.

**Table 12: SENT frame duration, depending on *sent_frame_rate***

| *sent_frame_rate* | Frame rate including pause pulse |
|---|---|
| 0 | 3 data nibbles: frame length 210 $t_{tick}$<br>4 data nibbles: frame length 228 $t_{tick}$<br>6 data nibbles: frame length 282 $t_{tick}$ |
| 1 | 0.5 ms |
| 2 | 1.0 ms |
| 3 | 2.0 ms |

The output behavior for correct frame rate configurations can be seen in Figure 210 below:

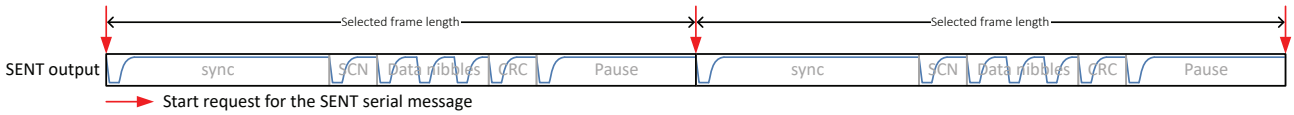



**Figure 21: SENT frame start depending on selected frame rate**

If the frame rate is configured to be so high that a message is not finished before the intended start of the next one, the start request is discarded. Such a setting is shown in Figure 221.

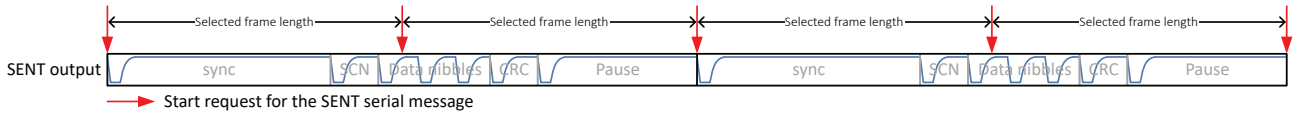



**Figure 22: SENT frame start depending on selected frame rate, with *sent_frame_rate* defining a too fast frame rate setting**



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## Optional SENT Slow Serial Output Protocol

SENT output supports an optional mode to transmit additional data. The slow serial mode enables transmission of additional data by encoding information in the Status and Communication (SCN) nibbles. The encoded data is captured over several transmissions and is then decoded to indicate additional serial message data. For more details on the serial message, refer to the SENT SAE J2716 APRIL2016 specification.

The slow serial mode is enabled when the EEPROM parameter *sent_emsg_dis* = 0. Following a reset, the first message transmitted is 0, following in order of the message ID until message 7, and then repeating. Table 19 and Table 20 identify the data sent with each message ID. The CRC for the Serial Message is derived from the Message ID and data.

**Table 13: SCN [3:2] Configuration Control**

| sent_emsg_dis | SCN Nibble bits [3:2] Contents |
|---|---|
| 0 | Serial Message |
| 1 | All Zeros |

The data in the serial message follows the table below:

**Table 14: Serial Message Format in SENT Status and Communication Nibble**

| received SCN nibble # | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SCN[3] | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 8-bit ID[7:4] | | | | 0 | 8-bit ID[3:0] | | | | 0 |
| SCN[2] | 6-bit CRC | | | | | | 12-bit data field | | | | | | | | | | | |

There are a number of codes available to be sent out in serial mode.

Some codes are based on sensor data, such as the following:

$01: Error and Status Codes

$23: Supplementary data channel #4,1 (Temperature data)

Other codes only send out constants, such as:

$03: Channel 1 / 2 Sensor type

$05: Manufacturer code

$06: Protocol standard revision

$07-0A: Fast Channel 1 Characteristic X1, X2, Y1, Y2

$29~2C: Sensor ID #1~4

$90~97: ASCII character OEM codes MESSAGE ID

Due to EEPROM sharing, the constant values are not compatible with all Linearization modes. The constant values are factory-programmed to EEPROM locations that are shared with for *lin_coeff_17* through *lin_coeff_31*. If using linearization in parallel with these constants, only *lin_coeff_00* through *lin_coeff_16* should be used. This means fixed position linearization and binning can be used with up to 17 points, and variable segment linearization and binning can be used with up to 6 points. See Table 8 for reference. For selecting how many coefficients are used, see Table 9 for the desired coeff_active setting.

If the *lin_coeff_xx* value that is assigned to a constant is changed, the new value will be output instead of the desired constant. For that reason, it is important to take caution when programming linearization coefficients, to ensure desired constant values are not overwritten.

Each message can be activated or deactivated using the *sent_emsg_sel* EEPROM bits. In this way, if the first constant(s) is(are) not required, their corresponding *lin_coeff_xx* value(s) can be used for linearization. The lowest $xx value used determines how many extra linearization coefficients can be used. If $03 is used, even if no other constants are reported, only 17 or 6 coefficients can be used for fixed or movable point respectively (e.g. if constant $03 and $05 are not reported, up to 19 fixed point coefficients or 8 movable point coefficients can be used).

Using the EEPROM setting *sent_serial_repeat_1* = 1, the message-ID $01 is repeated between any other messages. That means that if messages $01, $07, $08, $09, $0A are activated, transmission will be $01-$07-$01-$08-$01-$09-$01-$0A-$01-$07-$01-$08-….

The tables below give the serial output message numbers, the enable bits, the data source, and the byte contents.



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**Table 15: SENT Serial Output Message ID Contents for data registers**

| SENT serial message ID | Enable | Data source | Contents |
|---|---|---|---|
| $01 | sent_emsg_sel[0] | error register 0xA3[11:0] | Error and Status Codes |
| $23 | sent_emsg_sel[1] | temperature_16b[15:4] | Supplementary data channel #4,1 (Temperature data) |

**Table 16: SENT Serial Output Message ID Contents for constants**

| SENT serial message ID | Enable | Data source | Contents |
|---|---|---|---|
| $03 | sent_emsg_sel[2] | lin_coeff_17[11:0] | Channel 1 / 2 Sensor type |
| $05 | sent_emsg_sel[3] | lin_coeff_18[11:0] | Manufacturer code |
| $06 | sent_emsg_sel[4] | lin_coeff_19[11:0] | Protocol standard revision |
| $07 | sent_emsg_sel[5] | lin_coeff_20[11:0] | Fast Channel 1 Characteristic X1 |
| $08 | sent_emsg_sel[6] | lin_coeff_21[11:0] | Fast Channel 1 Characteristic X2 |
| $09 | sent_emsg_sel[7] | lin_coeff_22[11:0] | Fast Channel 1 Characteristic Y1 |
| $0A | sent_emsg_sel[8] | lin_coeff_23[11:0] | Fast Channel 1 Characteristic Y2 |
| $29 | sent_emsg_sel[9] | 0x0 & wafer_id[15:8] | Sensor ID #1 |
| $2A | sent_emsg_sel[10] | 0x0 & wafer_id[7:0] | Sensor ID #2 |
| $2B | sent_emsg_sel[11] | 0x0 & wafer_ypos[7:0] | Sensor ID #3 |
| $2C | sent_emsg_sel[12] | 0x0 & wafer_xpos[7:0] | Sensor ID #4 |
| $90 | sent_emsg_sel[13] | lin_coeff_24[11:0] | ASCII character OEM codes [1] |
| $91 | sent_emsg_sel[14] | lin_coeff_25[11:0] | ASCII character OEM codes [1] |
| $92 | sent_emsg_sel[15] | lin_coeff_26[11:0] | ASCII character OEM codes [1] |
| $93 | sent_emsg_sel[16] | lin_coeff_27[11:0] | ASCII character OEM codes [1] |
| $94 | sent_emsg_sel[17] | lin_coeff_28[11:0] | ASCII character OEM codes [1] |
| $95 | sent_emsg_sel[18] | lin_coeff_29[11:0] | ASCII character OEM codes [1] |
| $96 | sent_emsg_sel[19] | lin_coeff_30[11:0] | ASCII character OEM codes [1] |
| $97 | sent_emsg_sel[20] | lin_coeff_31[11:0] | ASCII character OEM codes [1] |

[1] Can be used to send two 6-bit ASCII characters in representation according to SAE J2716, APR2016, Table D.9-1.

## Data Nibble Format

When transmitting normal operation data, information about the measurement data is embedded in the first three or four data nibbles. Each data nibble consists of 4 bits with values ranging from 0 to 15. In order to present an output with the resolution of 12 or 16 bits, 3 or 4 data nibbles are required. The data nibble containing the MSB of the whole data section is sent first.

Three additional optional data nibbles can be associated with other parameters, by setting the EEPROM parameter: *sent_data_sel* as shown in Table 17.

- Counter – Each message frame has a serial number in each Counter nibble.
- Temperature – Temperature data from the A31316 internal temperature sensor.
- Diagnostics – Diagnostic flags can be sent as described in Table 32.
- Inverted nibble 1 – Nibble 1 contents (Data MSB) can be sent in one's complement.



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## SENT CRC

The SENT message contains a 4-bit CRC for data validity checks. The CRC polynomial is shown in Equation 18 with an initial seed of 0×5. By default, the CRC only includes the data nibbles of the SENT message with the Synchronization and SCN nibbles being ignored. With the EEPROM parameter *sent_crc_scn* = 1, the SCN nibble will be included in the CRC calculation.

Equation 18:

$$g(x) = x^4 + x^3 + x^2 + 1$$

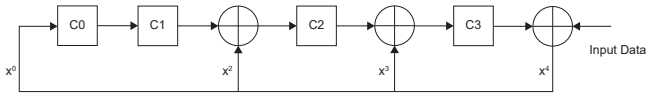



**Figure 23: SENT CRC Calculation**

## SENT Serial Message 6-Bit CRC

The SENT serial message contains a 6-bit CRC, based on the polynomial $x^6 + x^4 + x^3 + 1$.

The CRC checksum can be implemented via a bitwise exclusive OR with a 64-array lookup. The checksum is determined by reading 6-bit groups of the 24-bit message data in sequence, and then calculating the checksum with an extra zero value (augmentation by six 0-bits).

**Table 17: SENT Options Bit Contents EEPROM Parameter: *sent_data_sel***

| SENT Frame | *sent_data_sel* | Nibble 1 | | | | Nibble 2 | | | | Nibble 3 | | | | Nibble 4 | | | | Nibble 5 | | | | Nibble 6 | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 3 | 2 | 1 | 0 | 3 | 2 | 1 | 0 | 3 | 2 | 1 | 0 | 3 | 2 | 1 | 0 | 3 | 2 | 1 | 0 | 3 | 2 | 1 | 0 |
| H2 | 0 | 12 Bit Angle [11:0] [1] | | | | | | | | | | | | Not Used | | | | | | | | | | | |
| | 1 | 12 Bit Angle [11:0] | | | | | | | | | | | | 8-bit Temperature | | | | | | | | 4-Bit Message Counter | | | |
| | 2 | 12 Bit Angle [11:0] | | | | | | | | | | | | 8-bit diag_byte (See SENT Output Error Reporting Section) | | | | | | | | 4-Bit Message Counter | | | |
| | 3 | 12 Bit Angle [11:0] | | | | | | | | | | | | 12-Bit Message Counter | | | | | | | | | | | |
| H4 | 4 | 12 Bit Angle [11:0] [1] | | | | | | | | | | | | 8-bit Message Counter | | | | | | | | Inverted Nibble 1 | | | |
| | 5 | 12 Bit Angle [11:0] | | | | | | | | | | | | Ones Complement 12 Bit Angle ~[11:0] | | | | | | | | | | | |
| | 6 | 16-Bit Angle [15:0] | | | | | | | | | | | | | | | | Not Used | | | | | | | |
| H7 | 7 | 16-Bit Angle [15:0] [1] | | | | | | | | | | | | | | | | 8-bit Temp[3:0] [1] | | | | 8-bit Temp[7:4] [1] | | | |
| | 8 | 16-Bit Angle [15:0] | | | | | | | | | | | | | | | | 8-bit diag_byte (See Table 32) | | | | | | | |
| | 9 | 16-Bit Angle [15:0] | | | | | | | | | | | | | | | | 8-bit Message Counter | | | | | | | |
| | 10 | 12bit ChA data | | | | | | | | | | | | 12bit ChB data | | | | | | | | | | | |
| | 11 | ChA | ChB | 14-bit ChA, ChB (rotates each message) | | | | | | | | | | | | | | Not Used | | | | | | | |
| | 12 | ChA | ChB | 14-bit ChA, ChB (rotates each message) | | | | | | | | | | | | | | 8-bit Temperature | | | | | | | |
| | 13 | ChA | ChB | 14-bit ChA, ChB (rotates each message) | | | | | | | | | | | | | | 8-bit diag_byte (See SENT Output Error Reporting Section) | | | | | | | |
| | 14 | ChA | ChB | 14-bit ChA, ChB (rotates each message) | | | | | | | | | | | | | | 8-Bit Message Counter | | | | | | | |
| H1 | 15 | 12-Bit Angle [11:0] [1] | | | | | | | | | | | | 12-Bit Temp[3:0] [1] | | | | 12-Bit Temp[7:4] [1] | | | | 12-Bit Temp[11:8] [1] | | | |

[1] This value is subject to modification as per Table 20 based on setting *sent_encoding_sel*.



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**Table 18: SENT Tick Times, EEPROM Parameter dig_out_data_rate**

| EEPROM Code | SENT Tick Time (µs) |
|---|---|
| 0 (00000) | 3 |
| 1 (00001) | 0.25 |
| 2 (00010) | 0.375 |
| 3 (00011) | 0.5 |
| 4 (00100) | 0.625 |
| 5 (00101) | 0.75 |
| 6 (00110) | 0.875 |
| 7 (00111) | 1.0 |
| 8 (01000) | 1.125 |
| 9 (01001) | 1.25 |
| 10 (01010) | 1.375 |
| 11 (01011) | 1.5 |
| 12 (01100) | 1.625 |
| 13 (01101) | 1.75 |
| 14 (01110) | 1.875 |
| 15 (01111) | 2.0 |
| 16 (10000) | 2.125 |
| 17 (10001) | 2.25 |
| 18 (10010) | 2.375 |
| 19 (10011) | 2.5 |
| 20 (10100) | 2.625 |
| 21 (10101) | 2.75 |
| 22(10110) | 2.875 |
| 23 (10111) | 3.0 |
| 24 (11000) | 3.5 |
| 25 (11001) | 4.0 |
| 26 (11010) | 4.5 |
| 27 (11011) | 5.0 |
| 28 (11100) | 5.5 |
| 29 (11101) | 6.0 |
| 30 (11110) | 7.0 |
| 31 (11111) | 10.0 |



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**Table 19: SENT Message Frame Definitions**

| Section | Description |
|---|---|
| **Synchronization and Calibration** | |
| Function | Provide the external controller with a detectable start of the message frame. The large quantity of ticks distinguishes this section for ease of distinction by the external controller. |
| Syntax | Nibbles: 1<br>Quantity of ticks: 56<br>Quantity of bits: 1 |
| **Status and Communication** | |
| Function | Provides the external controller with the status of the A31316 and indicates the format and contents of the Data section. |
| Syntax | Nibbles: 1<br>Quantity of ticks: 12 to 27<br>Quantity of bits: 4<br>1:0 Device status<br>3:2 Message serial data protocol |
| **Data** | |
| Function | Provides the external controller with data selected by the *sent_data_sel* parameter. |
| Syntax | Nibbles: 3 to 6<br>Quantity of ticks: 12 to 27 (each nibble)<br>Quantity of bits: 4 (each nibble) |
| **CRC** | |
| Function | Provides the external controller with cyclic redundancy check (CRC) data for certain error detection routines applied to the Data nibbles and to the Status information. |
| Syntax | Nibbles: 1<br>Quantity of ticks: 12 to 27 (each nibble)<br>Quantity of bits: 4 |
| **Pause Pulse** | |
| Function | Additional time can be added at the end of a SENT message frame to ensure all message frames are of appropriate length and correlate to the internal update rate of the device. |
| Syntax | Nibbles: N/A<br>Quantity of ticks: Varies<br>Quantity of bits: N/A. |



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## Error Indicators / Specific Messages / Initialization Message in SENT Output Codes

If sent_data_sel is set to code 0, 4, 7, or 15, it is possible to output specific status information to the SENT data code by EEPROM setting sent_encoding_sel.

**Table 20: SENT error indicators / initialization message, if sent_encoding_sel = 1 and (sent_data_sel = 0, 4 , 7 or 15)**

| n-bit Data Value | 12-bit data value | SENT definition | Sensor mapping |
|---|---|---|---|
| Output is High Impedance, or High, or Low, depending on *err_resp_sel* | | | Sensor is in UVD mode (undervoltage detected) |
| Selectable (see SENT Initialization code selection) | Selectable (see SENT Initialization code selection) | Initialization | Sensor is not in UVD mode, AND<br>Sensor is initializing, no final data available yet |
| $2^n$–5 | 4091 | Sensor error indication | Sensor is not in UVD mode, AND<br>Sensor is not initializing, AND<br>any of the errors (UVD \| OVD \| SAT \| AOC) are set |
| $2^n$–6 | 4090 | Sensor functionality and processing error indication | Sensor is not in UVD mode, AND<br>Sensor is not initializing, AND<br>none of (OVD \| SAT \| AOC) are set, AND<br>any of the errors (SLF \| SRR \| ACF \| TSE \| POR) are set |

## SAE J2716 SENT

When configured Free Running Mode (SENT), *dig_out_sel* = 1, the SENT output transmits continuously, while in normal operating conditions with no extended pause pulse. When in *dig_out_sel* = 2, the SENT message frame rate is extended with a variable pause pulse to ensure a constant output rate. The pause pulse is limited to 768 tick times as defined by the SAEJ2716 APRIL2016 SENT standard.

## SENT Initialization Code Selection

According to the SAEJ2716, the output for initialization status must be 0. However, the A31316 permits the user to select other messages instead, which is adjuvant for standard compliance eschewal. The parameter *sent_init_sel* controls which code is used for initialization, if *sent_encoding_sel* = 1 and *sent_data_sel* is set to code 0, 4, 7, or 15.

**Table 21: SENT initialization code mapping selection when sent_encoding_sel = 1**

| sent_init_sel | n-bit Data Output for Initialization | 8-Bit Data Output for Initialization | 12-Bit Data Output for Initialization | 16-Bit Data Output for Initialization |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 1 | $2^n$ – 7 | 249 | 4089 | 65529 |
| 2 | $2^n$ – 4 | 252 | 4092 | 65532 |
| 3 | $2^n$ – 3 | 253 | 4093 | 65533 |
| 4 | $2^n$ – 2 | 254 | 4094 | 65534 |
| 5 | $2^n$ – 1 | 255 | 4095 | 65535 |
| 6 | 0 | 0 | 0 | 0 |
| 7 | 0 | 0 | 0 | 0 |



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## Output Pin Drive Strength Options

The A31316 provides configurable output drive strength. This can be done in open-drain and in push-pull mode.

### OUTPUT PIN FALL TIME SELECTION

The A31316 allows the user to change the fall time of the open-drain output digital SENT or PWM signal using the EEPROM parameter *dig_out_pull_lim*. This control is viewed as a discrete gradient from Faster to Slower with intermediate steps to provide desired pulse shaping to improve EMC emissions performance. The resulting fall time is heavily dependent on load capacitance. As reference, fall times for certain capacitance values are shown in Table 22.

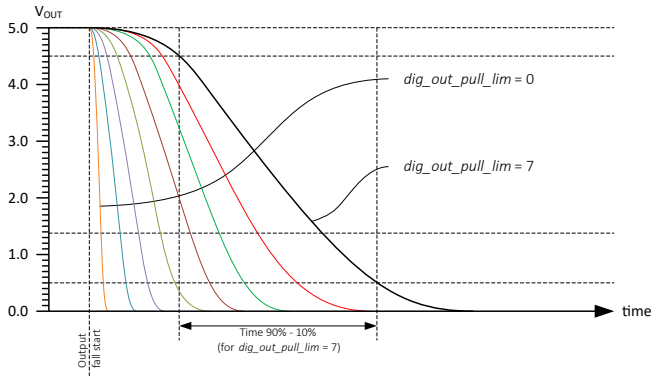



**Figure 24: Definition of output fall times and output delay (exemplary plot)**

**Table 22: Typical Output fall time for each dig_out_pull_lim**

| dig_out_pull_lim | Time 90% to 10% (µs) |
|---|---|
| | $C_L$ = 4.7 nF |
| | Pullup $R_L$ = 55 kΩ |
| 0 | 1.15 |
| 1 | 1.18 |
| 2 | 1.20 |
| 3 | 1.33 |
| 4 | 2.00 |
| 5 | 2.87 |
| 6 | 4.37 |
| 7 | 5.68 |



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### PUSH-PULL OUTPUT SETTING FOR SENT AND PWM RISING EDGE

In order to decrease the rise time for digital outputs, it is possible to enable a push-pull output. This is done by setting *dig_out_drive_sel* = 0. In such a configuration, a pull-up resistor is not necessary, but still recommended. The table below shows the digital output rise times, depending on the capacitive load.

**Table 23: Typical Output rise time if dig_out_drive_sel = 0**

| Time 10% to 90% (µs)<br>$C_{load}$ = 4.7 nF<br>Pullup $R_L$ = 55 kΩ |
|---|
| 0.38 |

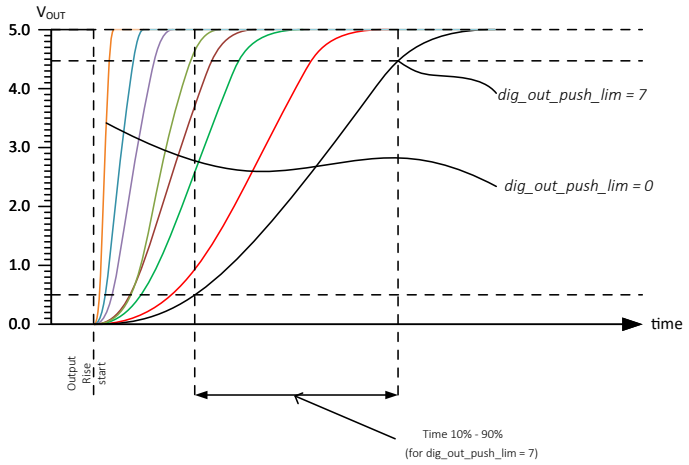



**Figure 25: Definition of output rise times and output delay (exemplary plot)**



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## PROGRAMMING PROTOCOL

The A31316 device generally uses a 3-wire programming interface where $V_{CC}$ can control the program enable signal, data is transmitted on the output pin, and all signals are referenced to ground. This 3-wire interface makes it possible to use multiple devices with shared $V_{CC}$ and ground lines. If $V_{CC}$ can be controlled by the host, this is the preferred method of communication. If $V_{CC}$ cannot be controlled by the host, initiating Manchester communication can be done through the output pin as well. See section Physical Layer for more information.

When performing a write to EEPROM transaction, the A31316 requires a delay of $t_w$ to store the data into the EEPROM. The device will respond with a low-to-high transition on the output pin to indicate the write to EEPROM sequence is complete.

### Physical Layer

The serial interface allows an external controller to read and write registers, including EEPROM, in the A31316 using a point-to-point command/acknowledge protocol when using any of the output protocols. The A31316 does not initiate communication; it only responds to commands from the external controller. Each transaction consists of a command from the controller. If the command is a write, there is an acknowledge pulse from the A31316 in the form of a low pulse following a successful write. If the command is a read, the A31316 responds by transmitting the requested data in a Read Acknowledge frame. It is the external controller's responsibility to avoid sending a Command Frame which overlaps a Read Acknowledge frame.

The serial interface uses a Manchester encoding based protocol per G.E. Thomas (0 = rising edge, 1 = falling edge), with address and data transmitted MSB first. Four commands are recognized by the A31316: Write Access Code, Write to Volatile Memory, Write to Non-Volatile Memory (EEPROM) and Read. One frame type, Read Acknowledge, is sent by the A31316 in response to a Read command.

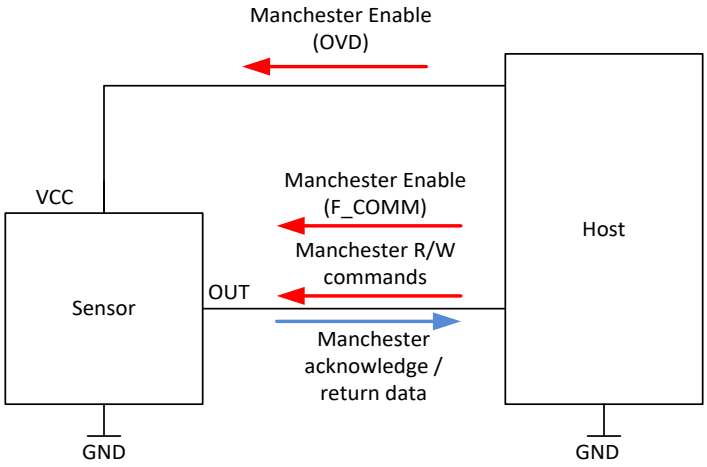



**Figure 26: Manchester Communication Block Diagram**

### Settings Controlling the Manchester Communication

It is possible to limit access to the device by programming certain options. These are detailed below.

**Table 24: manch_access_sel behavior**

| manch_ access_sel | Overvoltage Detection | Trigger | Description |
|---|---|---|---|
| 00 (default) | Enabled | Enabled | Communications is enabled by either option. |
| 01 | Enabled | Disabled | Communication is enabled only by overvoltage detection. |
| 10 | Disabled | Enabled | Communication is enabled only by external trigger on output line. |
| 11 | Disabled | Disabled | Communication is locked. |



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## SERIAL INTERFACE MESSAGE STRUCTURE

The general format of a command message frame is shown in Figure 27. Note that, in the Manchester coding used, a bit value of 1 is indicated by a falling edge within the bit boundary, and a bit value of zero is indicated by a rising edge within the bit boundary. The time period for the bit boundary is determined by the baud rate initiated by the external controller. The A31316 read acknowledge is transmitted at the same rate as the command message frame. The bits are described in Table 25.

For a Write Access command frame, the data consists of 16 bits. For a Read Request frame, the data bits are omitted. For a Read Acknowledge or Write frame, the data bits are defined as shown in Figure 27, where bit 0 is the LSB.

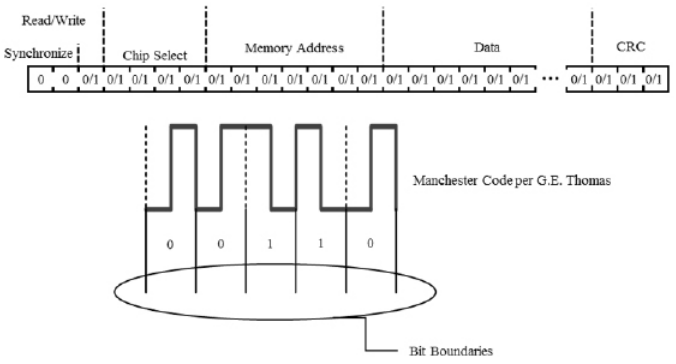



**Figure 27: Manchester Bit Stream Definition**

**Table 25: Manchester Bit Definition (host commands)**

| Quantity of Bits | Name | Values | Description |
|---|---|---|---|
| 2 | Synchronization | 00 | Used to identify the beginning of a Manchester command and communication bit time |
| 1 | Read / Write | 0 | [As required] Write operation |
| | | 1 | [As required] Read operation |
| 2 | Chip Select | – | Chip select for up to 2 dies connected in parallel: |
| | | 01 | [as required] device communication address 0 |
| | | 10 | [as required] device communication address 1 |
| | | 00 / 11 | [as required] Broadcast<br>00 can be used as default if only one device is connected |
| 8 | Address | Any | Register address for read or write |
| 32 (write command)<br>0 (read command) | Data | Any | 32 data bits (write command)<br>0 bits (read command) |
| 3 | CRC | Any | Bits to check the validity of frame. |



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During a read command, the device determines the baud rate from the sync bits and responds with a read response frame using the same baud rate detected. The baud rate during a write command is also automatically detected, but is only used for decoding, as the A31316 does not respond to write commands.

**Table 26: Manchester Bit Definition (device response)**

| Quantity of Bits | Name | Values | Description |
|---|---|---|---|
| 2 | Synchronization | 00 | Used to announce the beginning of a Manchester interface response |
| 32 | Data | Any | Read data |
| 3 | CRC | Any | Bits to check the validity of frame. |

The device memory contains non-volatile (EEPROM) and volatile registers which are accessible via the serial interface through Manchester communication modes. The memory address space is divided into Factory and Customer areas.

### MANCHESTER UNLOCKING – VIA OVD

1. At any time after POR, create an OVD condition. This sets the OUT in HIGH-Z state since PWM/SENT Output is turned off.
2. Send the correct access code.
3. Device is unlocked.
4. If *manch_en* bit was set LOW, the OVD condition can be removed and the device returned to PWM/SENT Mode with the device unlocked. OVD is needed for every Manchester Read/Write command.
5. If *manch_en* bit was set HIGH, the OVD condition can be removed, but the device will remain in communication mode. OVD is not needed for Manchester transactions until *manch_en* bit is set LOW through a Write Command. This action will lock the device back.

### MANCHESTER UNLOCKING – VIA TRIGGERING PULSE

1. At any time after POR, create the trigger condition by driving the output LOW for a specific amount of time depending on the PWM (minimum of 2 full PWM messages) or SENT Mode (minimum of 30 $t_{tick}$). Then release the line or drive it HIGH to create a 0→1 condition.
2. The device is in communication mode and a 300 µs timeout starts.
3. Write the correct access code before the 300 µs expires. Timing requirements stop once the first sync bit is detected.
4. If the code is wrong, aborted, or it was an incorrect transaction, the part goes back to PWM/SENT mode. Retrying by starting at step 1 is possible.
5. If the code is correct, the device is unlocked and manch_en bit is set to 1. The output is disabled, and the device remains unlocked until *manch_en* is written to 0 through a Manchester Write.

**Table 27: Unlock Code and Customer Access Codes**

| Command | Write address | Write data |
|---|---|---|
| Customer access code (Read access to factory) *manch_en* = 1 | 0x86 | 0xC2D8E67B |
| Customer access code (Read access to factory) *manch_en* = 0 | 0x86 | 0xC2D8E67A |

## Manchester Communication CRC

The serial interface uses a cyclic redundancy check (CRC) for data-bit error checking (synchronization bits are ignored during the check). The CRC algorithm is based on the following polynomial and the calculation is represented graphically in Figure 28. The trailing 3 bits of a message frame comprise the CRC token. The CRC is initialized at 111.

$$g(x) = x^3 + x + 1$$

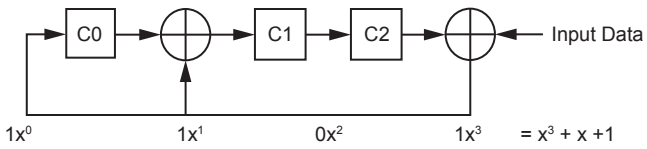



**Figure 28: Manchester CRC Implementation**

## EEPROM Lock

There are 3 different lock modes available in the A31316: EELOCK, WRLOCK, and FLOCK. Each of these are separate from access lock which requires a customer unlock code to control. EELOCK locks the EEPROM from external write access, while still allowing writes to shadow and volatile registers. The entirety of memory can still be read in this mode allowing for a level of customer lock, while maintaining debug support. WRLOCK prevents any write both EEPROM and volatile registers. Factory read support is maintained. This is not recommended for any output mode. The FLOCK mode locks out both reads and writes to EEPROM and all registers. This is will prevent any



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access by either customer or factory, removing available support options from the factory.

NOTE: When any of the EEPROM lock options are set, non-destructive factory debug support is limited.

**Table 28: Serial Communication Lockout Modes**

| mem_lock_sel[3:0] | Lock Mode | Description |
|---|---|---|
| 4'b0011 | EELOCK | EEPROM Lock: Prevents writes to EEPROM but all volatile registers including shadow can be written. All registers and EEPROM can be read normally. |
| 4'b0110 | WRLOCK | Write Lock: Prevents writing anything to either EEPROM or registers. Factory debug support is still available |
| 4'b1100 | FLOCK | Full Lock: Prevents writing and reading to any register in the device. |

## EEPROM Margin Checking

The A31316 contains a test mode, EEPROM Margining, to check the logic levels of the EEPROM bits. The EEPROM margining is accessible with customer access. The EEPROM margining is selectable to check all logic 1, logic 0, or both. The results of the test are reported back in EEPROM registers.

Note: A fail of the margin test does not force the output to a diagnostic state.

## Error Flag Registers

The different error flags available in the A31316 are stored in the primary memory space of register 0xA4. If the error conditions are removed, all the non-critical error flags are cleared on a read of this register, or after being sent out through the output protocols. The register contents can be seen in Table 29.

**Table 29: Error Registers**

| Address | NAME | Access | Bit | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31…13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0xA3 | error | RO | 0 | OFE | SPE | EUE | OVD | UVD | ESE | POR | SRR | SLF | SAT | TSE | AOC | ACF |

## Analog Check Failure (ACF)

To ensure proper operation of the internal regulators, a voltage check is done on the different reference sources for the analog and digital circuitry, as well as for the Hall element drivers. If any of these voltages deviate to where the accuracy of the part will be in question, the ACF flag will be set and the device will go into a state as defined in Table 32. If the voltages are detected to recover, a read of the device register or reporting through the output modes will clear the error flag so normal operation can resume. The ACF flag can be disabled by setting *acf_mask* bit in EEPROM.

## Angle Outside Clamp (AOC)

If the upper and lower clamps are set within the operating range of the device, the AOC flag can be set as shown in Table 32 to indicate the signal reaching this clamp value. If the signal moves back within the range defined *ang_clamp_high* and *ang_clamp_low* as described in the Output Clamps section, the AOC flag can be removed by a read of the device register or through reporting in the applicable output protocol. If the flag is not desired, the EEPROM bit *aoc_mask* can be set. The AOC error is updated with every angle update. However, the error may be suppressed for up to 16 $t_{update}$ based on the *fault_filt* EEPROM setting.

## Temperature Error (TSE)

The TSE flag is set if the temperature sensor output saturates high, which indicates the ambient temperature is greater than 175.138°C or if the measured temperature is less than −54.963°C. If any of these conditions occur the TSE flag will be set, and the device will go into a state as defined in Table 32. If the temperature is detected to recover, a read of the device register or reporting through the output modes will clear the error flag so normal operation can resume. The TSE flag can be disabled by setting *tse_mask* bit in EEPROM. The TSE error is detected every nominal 1.5 ms and reaches the output after latest 1.62 ms.

## Saturation Flag (SAT)

The Saturation Flag is provided to warn the user in case the magnetic signal is outside of the detectable range of the signal path. A saturation can occur:

- In the ADC and filters, which would indicate a front-end gain too large for the detected field, or
- A digital signal path saturation which would indicate a gain setting too large.

If either of these conditions occur, the SAT flag will be set as defined in Table 35. If the saturation condition is removed, the



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error flag can be cleared by a read of the device register, or through reporting in the applicable output protocol.

Overall, the SAT flag is constructed as follows:

- SAT can be caused by saturation at multiple points of the signal path. Each point is lumped in with a sub-flag which can be individually masked to customize the saturation detection flag. Provided in order of the signal path the individual sub-flags are: SAT_FILT, SAT_CHAN, SAT_COR, and SAT_LIN. Alternatively if no saturation detection is required, the entire SAT error can be masked by setting *sat_mask* = 1
  - □ SAT_FILT is set when saturation occurs in the ACD or low-pass filter. This sub-flag can be disabled by setting *sat_filt_mask* = 1. Possible causes are:
    - ◦ Too high of input field on the device.
    - ◦ A digital or analog error in the ADC or filter circuitry.
  - □ SAT_CHAN is saturation caused by channel A/B 1-D offset/gain corrections. This sub-flag can be disabled by setting *sat_chan_mask* = 1. Possible causes are:
    - ◦ Too high of an input field on the device.
    - ◦ A digital error in the factory or customer 1-D trims
    - ◦ Customer 1-D trim is set incorrectly for the input field used.
  - □ SAT_COR is set when saturation would occur within the angle offset and gain corrections. This sub-flag can be disabled by setting *sat_cor_mask* = 1. Possible causes are:
    - ◦ Output value of pre-gain offset is outside of the *ang_thresh_low / ang_thresh_high* limits. This check is only performed if *ang_thresh_en* bit is set.
    - ◦ Output value of angle gain is outside of the signal path range. This check is only performed if *ang_gain_sat_en* is set. Otherwise the output will rollover to a valid output.
    - ◦ Output value of the post-gain offset is outside of the signal path range. This check is only performed if the *ang_offs_sat_en* bit is set.
  - □ SAT_LIN is set when the output of linearization would cause saturation. This sub-flag can be disabled by s*at_lin_mask* = 1. Possible causes are:
    - ◦ Linearization correction applies a correction which results in a value beyond the range.

The SAT error is updated with every angle update. However, the error can be suppressed for up to 16 $t_{update}$ based on the f*ault_filt* EEPROM setting.

## Oscillator Frequency Error (OFE)

The A31316 contains a low frequency oscillator to act as a watchdog of the main oscillator. If these two oscillators deviate beyond comparison threshold (20%), the device will go into a state as defined in Table 32. This error is considered critical and cannot be cleared by any action besides a device reset (POR). To mask OFE errors, the *ofe_mask* bit can be set. It is not recommended to set this bit for normal operation but is provided for debugging purposes. The OFE error detection starts every 10 $t_{update}$.

## Signal Processing Logic Failure (SLF)

To help check the main signal path logic in the device during operation, a set of known inputs will periodically be run through key parts of the data path and compared to known outputs. This allows the user to have confidence in the accuracy of the digital signal path without need for running the LBIST which interrupts the device operation. Additionally, a watchdog checks that the output angle is updated at the expected delay after the input signals are available. In case of unexpected test outputs, or missed watchdog timer, the SLF flag will be set as shown in Table 32. If the error condition is removed the error flag can be cleared by a read of the device register or by reporting through the output modes so normal operation can resume. The SLF error is determined every 10 $t_{update}$.

## Signal Radius Out of Range (SRR)

The A31316 has an internal check on the two dimensions that are used to calculate angle (called sine and cosine) by calculating the radius and comparing to user defined diagnostic boundaries. These boundaries are set by the *magnetic_thresh_min* and *magnetic_thresh_max* EEPROM parameters. The condition for no error is calculated by the equation below:

Equation 19:

$$magnetic_thresh_min^2 < radius_sq_17b < magnetic_thresh_max^2$$

with

$$\text{radius_sq_17b} = \left(\left[\frac{chan_a_16b}{128}\right]\right)^2 + \left(\left[\frac{chan_b_16b}{128}\right]\right)^2$$

The brackets [*x*] denote the floor function, which rounds x down to the nearest integer. The current value of *radius_out_sq_17b* can be read directly from the appropriate register.

The SRR check helps ensure the accuracy of the ATAN2 by the assumption the magnitude of the two dimensions will remain



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constant over the complete rotation. This is only true in rotary applications. In the event the magnetic field is outside of the threshold boundaries *magnetic_thresh_min* and *magnetic_thresh_max*, the SRR flag will be set as shown in Table 32. If the error condition is removed, the error flag can be cleared by a read of the device register or reporting through the output modes so normal operation can resume. The SRR flag can be disabled by setting *srr_mask* bit in EEPROM. The SRR error is updated with every angle update. However, the error can be suppressed for up to 16 $t_{update}$ based on the *fault_filt* EEPROM setting.

## Power-On Reset (POR)

To indicate a Power-On Reset event occurred, the POR error flag will be set on startup. In the event of a reset, the filters and signal path will need time to settle and this error flag is set to help indicate this state in the event the reset was unintentional. This flag is reported as shown in Table 32. Once the first angle update is available, a read of the device register, or reporting through the output modes will clear the POR flag so normal operation can resume. The POR flag can be disabled by setting the *por_mask* bit in EEPROM.

The first output message (SENT) or first output cycle (PWM) will report the POR error, unless POR is masked.

POR error may be prolonged in PWM mode to suppress filter initialization showing on the output. Refer to Sensor Output During Low-Pass Filter Initialization section for more information

## EEPROM Multiple Bit Error (EUE) and EEPROM Single Bit Error (ESE)

The A31316 contains EEPROM with error checking and correction codes, ECC, that provide correction of any single EEPROM bit error without effecting device performance. The ECC also detects a multiple bit EEPROM errors and triggers an internal fault signal at which point the device will go into a state as defined in Table 32. An EEPROM multi-bit error is considered critical and cannot be cleared by any action besides a device reset (POR). The EEPROM error indication bits containing the single bit error is cleared after a read. A single bit error will not affect the device output as it will be corrected but it may indicate deteriorating performance of the EEPROM and should be monitored. The ESE flag can be disabled by setting the *ese_mask* bit in EEPROM. The EUE flag cannot be disabled. The EUE and ESE flags can only be set on EEPROM read, which occurs only at POR.

## Shadow Parity Error (SPE)

Upon power up of the A31316, the EEPROM parameters are loaded into fast access shadow registers for use in operation. These registers have a simple parity structure to ensure proper loading of the EEPROM parameters. If a parity error is detected, the SPE error flag is set and the device will go into a state as defined in Table 32. This error is considered critical and cannot be cleared by any action besides a device reset (POR). The SPE flag can be disabled by setting the *spe_mask* bit in EEPROM. The parity error is detected every 10 $t_{update}$.

## Undervoltage Detection (UVD)

The A31316 contains circuitry to detect a condition when the supply voltage drops below the specified limit. Hysteresis is designed into the circuit to prevent chattering around the threshold. This hysteresis is defined by $V_{UVD(RISE)} - V_{UVD(FALL)}$. As an example, initially $V_{CC}$ and OUT are within the normal operating range. If $V_{CC}$ drops below $V_{UVD(FALL)}$, OUT is forced to a state as defined in Table 32. When $V_{CC}$ returns above $V_{UVD(RISE)}$, OUT returns to its normal operating state after a read of the device register or once the error is reported through the output mode. If $V_{CC}$ drops below the internal reset level, $V_{POR(FALL)}$, the output is forced to a high impedance state. When $V_{CC}$ returns above the rising reset level, $V_{POR(RISE)}$, the output responds with the POR flag if enabled.

Undervoltage Detection is set to one of two configurable thresholds based on the EEPROM parameter *uvd_sel* as shown in Table 300 and Figure 298.

**Table 30: uvd_sel settings for $V_{UVD}$**

| uvd_sel | $V_{UVD(RISE)}$ | $V_{UVD(FALL)}$ |
|---|---|---|
| 0 | $V_{UVD(LOW, RISE)}$ | $V_{UVD(LOW, FALL)}$ |
| 1 | $V_{UVD(HIGH, RISE)}$ | $V_{UVD(HIGH, FALL)}$ |

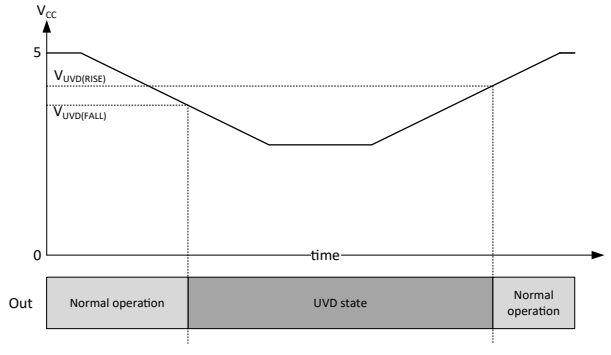



**Figure 29: $V_{CC}$ Low Threshold Levels**



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## Overvoltage Detection (OVD)

The A31316 contains circuitry to detect a condition when the supply voltage rises above the specified limit. Hysteresis is designed into the circuit to prevent chattering around the threshold. This hysteresis is defined by $V_{OVD(RISE)} - V_{OVD(FALL)}$. As an example, Initially, $V_{CC}$ and OUT are within the normal operating range. If $V_{CC}$ rises above $V_{OVD(RISE)}$, OUT is forced to a state as defined in Table 32. When $V_{CC}$ returns below $V_{OVD(FALL)}$, OUT returns to its normal operating state after a read of the device register or reporting through the output mode. If the device is in SENT/PWM or Analog output modes, and the EEPROM lock options are not set, the device will enter programming mode and the output will always be forced to a high impedance state when $V_{CC}$ increases above $V_{OVD(RISE)}$. The overvoltage detection is only enabled if the EEPROM lock options are set, otherwise the device will be in programming mode (Manchester Communication on the OUT Pin).

Overvoltage Detection is set to one of two configurable thresholds based on the EEPROM parameter ovd_sel as shown in Figure 3029 and Table 311.

**Table 31: ovd_sel settings for $V_{OVD}$**

| ovd_sel | $V_{OVD(RISE)}$ | $V_{UVD(FALL)}$ |
|---|---|---|
| 0 | $V_{OVD(HIGH, RISE)}$ | $V_{OVD(HIGH, FALL)}$ |
| 1 | $V_{OVD(LOW, RISE)}$ | $V_{OVD(LOW, FALL)}$ |

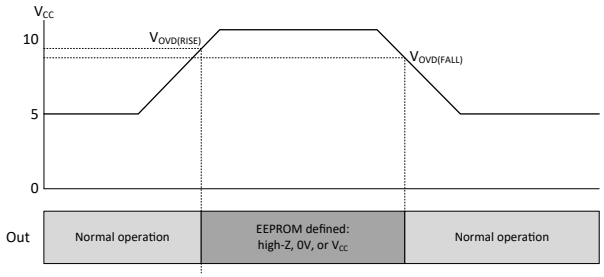



**Figure 30: OVD Threshold Levels**

## SENT Output Error Reporting

In SENT mode, there are four ways to report error flags; the SCN status bits [1:0], the slow serial message, and the option extended data options that include a rotating reporting of the error registers or going high impedance output state when any error condition occurs. The SCN status bits [1:0] are broken up based on whether they are more likely to be internal or external caused errors. When any error flag is set, these status bits will be set until a clear condition occurs. The clear condition can be a read of the err register, or a SENT message being sent out with the SCN bit set. The SENT message will clear the error flag from the err register. If either of the SCN status bits are set, the data should not be trusted as it indicates an error condition occurred since the previous SENT message was received. The bits are constructed as follows:

SCN[0] = SLF | SRR | ACF | TSE | POR (see chapter Sensor output during low-pass filter initialization for information on POR bit setting during filter initialization)

SCN[1] = UVD | OVD | SAT | AOC

The serial message requires successive SENT messages to be received. The Error flags that are sent in this method are taken from an internal register which is not cleared during normal conditions to allow normal operation for other interfaces. Once the error bits are sent out from the slow serial message, the register will be cleared.

The third reporting method is through the optional extended diagnostic nibbles in *sent_data_sel* options 2, 8, or 13. This method sends the *diag_byte* error flags in every SENT message. The error flags for this method are taken from an internal copy of the error registers to allow the error register to be cleared separately. The bits are sent out as shown in Table 32. Note that over voltage and under voltage are reported through the same bit.

If the specific error flags are not desired to be transmitted, the EEPROM parameter *dig_out_err_resp_sel* can be set to put the output in a high impedance state when an error condition occurs. If the error condition is removed, the output will return to normal operation. This option will prevent the device from transmitting any data through the SENT mode, but Manchester communications are still possible.

## PWM Output Error Reporting

When in PWM output mode, the error flags are reported by sending out a specific diagnostic message format. The format consists of setting the carrier frequency to half of the configured setting and sending a specific duty cycle as defined in Table 32. In the event of more than one error occurring, the higher priority message will be sent. If two error conditions occur and clear at the same time, only one error flag will be seen. Table 32 is listed in descending order in terms of priority.

If the specific error flags are not desired to be transmitted, the EEPROM parameter *dig_out_err_resp_sel* can be set to put the output in a high impedance state when an error condition occurs. If the error condition is removed, the output will return to normal operation. This option will prevent the device from transmitting any data through the PWM mode, but Manchester communica-



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tions are still possible. If using the half frequency error reporting with the trigger pulse Manchester method, the trigger must cover two full periods of the new frequency.

## Broken Wire Detection

The A31316 contains circuitry to detect a condition when the ground or supply connection is disconnected. If the GND connection is broken, the output will be at $V_{SAT(DIAG, HIGH)}$. If the $V_{CC}$ connection is broken, the output will be at $V_{SAT(DIAG, LOW)}$.

## Logic Built-In Self-Test (LBIST)

It is possible to test the logic of the sensor using a built-in self-test. This self-test runs quasi-random signals though a scan chain connection of the digital logic. A checksum is calculated by the sensor and compared to a known good checksum value.

The user can start the self-test by unlocking the part (see section Programming Protocol ) and writing ‘1’ to the *bist_start.* The self-test typically takes 200 ms to complete. No communication is possible while LBIST is running.

After LBIST is done:

- *lbist_status* will be set to ‘1’ regardless of the test result.
- *lbist_result* will be set to ‘1’ if the test was successful.
- The checksum can be read out be reading *lbist_result_signature*. This is not necessary to judge the test result. The correct checksum is 0x556E4F7D.



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**Table 32: Device Error Flag Responses**

| Error Flag | ERR Register (Bit) | Meaning | Analog / PWM Error Priority | SENT Response err_resp_sel = 0 | PWM Response err_resp_sel = 0 | SENT/PWM Response err_resp_sel = 1 |
|---|---|---|---|---|---|---|
| OFE | ERR[12] | Oscillator Frequency Error | 1 (highest) | High Impedance | High Impedance | High Impedance |
| EUE | ERR[10] | EEPROM Multiple Bit Error | 2 | High Impedance | High Impedance | High Impedance |
| SPE | ERR[11] | Shadow Parity Error | 3 | High Impedance | High Impedance | High Impedance |
| SLF | ERR[4] | Signal Processing Logic Failure | 5 | SCN[0] = 1<br>diag_byte[0] = 1 | ½ Frequency<br>10% Duty Cycle | High Impedance [*4] |
| SRR | ERR[5] | Signal Radius Out of Range | 6 | SCN[0] = 1<br>diag_byte[1] = 1 | ½ Frequency<br>20% Duty Cycle | High Impedance [*4] |
| ACF | ERR[0] | Voltage Check Failure | 7 | SCN[0] = 1<br>diag_byte[2] = 1 | ½ Frequency<br>30% Duty Cycle | High Impedance [*4] |
| TSE | ERR[2] | Temperature Error | 8 | SCN[0] = 1<br>diag_byte[3] = 1 | ½ Frequency<br>40% Duty Cycle | High Impedance [*4] |
| POR | ERR[6] | Power-On Reset | 9 | SCN[0] = 1 [*6]<br>diag_byte[4] = 1 | ½ Frequency<br>50% Duty Cycle [*6] | High Impedance [*4] |
| UVD | ERR[8] | Undervoltage Detection | 10 | High Impedance, or High, or Low, depending on err_resp_sel_uv<br>and<br>SENT reset [*2]<br>and<br>SCN[1] = 1 [*3]<br>and<br>diag_byte[5] = 1 [*5] | High Impedance, or High, or Low, depending on err_resp_sel_uv<br>and<br>½ Frequency<br>60% Duty Cycle [*3] | Same as with err_resp_sel = 0 |
| OVD [*1] | ERR[9] | Overvoltage Detection | 11 | SCN[1] = 1<br>diag_byte[5] = 1 | ½ Frequency<br>70% Duty Cycle | High Impedance [*4] |
| SAT | ERR[3] | Saturation Flag | 12 | SCN[1] = 1<br>diag_byte[6] = 1 | ½ Frequency<br>80% Duty Cycle | High Impedance [*4] |
| AOC | ERR[1] | Angle Outside Clamp | 13 | SCN[1] = 1<br>diag_byte[7] = 1 | ½ Frequency<br>90% Duty Cycle | High Impedance [*4] |
| ESE | ERR[7] | EEPROM Single Bit Error | 14 (lowest) | None | None | High Impedance [*4] |

[*1] OVD will cause the device to go High Impedance if *manch_access_sel* = 2'b0X.
[*2] SENT interface will restart after coming out of the UVD reporting, starting with message counter = 0 (if enabled) and the first serial message (if enabled).
[*3] At the first frame and potentially further frames transmitted after UVD condition is released, depending on *err_min* setting.
[*4] The error will be included in the next enhanced message to start after the current enhanced message finishes
[*5] At the first frame after UVD condition is released.
[*6] POR status on PWM output, and SCN[0] = 1 status can also be caused by filter initialization reporting. See Sensor output during low-pass filter initialization.



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## DIAGNOSTIC SETTING AND CLEARING

Diagnostic bits are set internally as soon as an error is detected and are sent out whenever the protocol allows it. In PWM, this is at the start of the next PWM cycle. In SENT, this is at the creation of the next SENT frame. For SENT serial messages, this is at the creation of the next serial message.

In both SENT and PWM mode, most errors are cleared when they no longer occur. There are a few errors which are considered critical, and will not clear themselves, these errors require a POR event before the device returns to normal operation. These errors are: OFE, EUE, and SPE.

All errors are guaranteed to output at least once. This means if an error condition occurs but is cleared before the next output reporting the error flag will still be reported. For example, if the angle exceeds the clamp value in the middle of a PWM period or SENT message but returns to a valid angle before the start of the next PWM period or SENT message, that next period or message will still report AOC error even though the angle is not currently outside of the clamp. This ensures that no error conditions are lost during the operation.

## MEMORY ACCESS

The A31316 utilizes a Primary-only memory structure to allow fast communication. The device uses EEPROM to permanently store configuration parameters for operation. EEPROM is user-programmable and permanently stores operation parameter values or customer information. The operation parameters are downloaded to shadow (volatile) memory at power-up. Shadow fields are initially loaded from corresponding fields in EEPROM, but can be overwritten, either by performing a write to the shadow addresses, or by reprogramming the corresponding EEPROM fields and power cycling the IC. Use of Shadow Memory is substantially faster than accessing EEPROM. In situations where many parameters need to be tested quickly, shadow memory is recommended for trying parameter values before permanently programming them into EEPROM. The shadow memory registers have the same format as the EEPROM and are accessed at extended addresses 0x40 higher than the equivalent EEPROM address. Unused bits in the EEPROM do not exist in the related shadow register and will return 0 when read. Shadow registers do not contain the ECC bits. All EEPROM and Shadow locations may be read after customer unlock.

The device does not answer Manchester reads commands from registers which do not exist, or which only contain “write-only” bits.

### Shadow Memory Read and Write Transactions

Shadow memory Read and Write transactions are identical to those for EEPROM. Instead of addressing to the EEPROM addresses, one must address to the Shadow addresses, which are located at an offset of 0x40 above the EEPROM.



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**Table 33: Register Description – Volatile**

| Volatile Address (hex) | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Volatile Address (hex) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x83 | | | | | | | | | | | | | | | | | | | ee_margin_loop | ee_margin_test_addr | | | | | | | ee_margin_test_addr_en | ee_margin_result | ee_margin_status | | ee_margin_min_dis | ee_margin_max_dis | ee_margin_start | 0x83 |
| 0x85 | | | | | | | | | | | | | | | | | | | | | | | | | | | lbist_result | lbist_status | | | | | 0x85 |
| 0x86 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | memory_access | | 0x86 |
| 0xA0 | | | | | | | | | | | | | | | | | | | | | | | | | march_en | | | | | | | lbist_start | 0xA0 |
| 0xA1 | lbist_result_signature | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 0xA1 |
| 0xA2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | software_reset | 0xA2 |
| 0xA3 | | | | | | | | | | | | | | | | | | | | ofe | spe | eue | ovd | uvd | ese | por | srr | slf | sat | tse | aoc | acf | 0xA3 |
| 0xA7 | temperature_16b | | | | | | | | | | | | | | | | | | angle_16b | | | | | | | | | | | | | | 0xA7 |
| 0xA8 | chan_b_16b | | | | | | | | | | | | | | | | | | chan_a_16b | | | | | | | | | | | | | | 0xA8 |
| 0xA9 | chan_b_pre_16b | | | | | | | | | | | | | | | | | | chan_a_pre_16b | | | | | | | | | | | | | | 0xA9 |
| 0xAA | | | | | | | | | | | | | | | | | radius_sq_17b | | | | | | | | | | | | | | | | 0xAA |

The table above shows the location of all useful volatile registers. Most volatile registers are read only and meant to provide information about the device's internal functions.

Other unmarked registers may contain data used for internal purposes, only registers useful for external interfacing are shown. When writing to volatile registers, all unlabeled bits should be set to '0'.

## Volatile 0x83

### EE_MARGIN_LOOP (BITS 13) R/W (READ AND WRITE)

If set, the margin testing will continuously test the register in *ee_margin_test_addr*.

### EE_MARGIN_TEST_ADDR (BITS 12:7) R/W

If the margin testing fails, this register contains the address of the register that failed. If multiple registers fail, this contains the address of the most recent failed register (highest register). If *ee_margin_test_addr_en* is set to '1', this address can be written to and used as the starting address for margin testing.

### EE_MARGIN_TEST_ADDR_EN (BIT 6) R/W

Determines if a custom starting address is used, or the default starting address is used.

- If *ee_margin_test_addr_en* = '0', Margin testing begins at address 0
- If *ee_margin_test_addr_en* = '1' Margin testing begins at the address contained in *ee_margin_test_addr*



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#### EE_MARGIN_RESULT (BIT 5) RO (READ ONLY)

Indicates which limit the margin failed. When the margin testing fails, this bit is set based on the fail condition.

- If *ee_margin_result* = '0', Lower margin failed
- If *ee_margin_result* = '1', Upper margin failed

#### EE_MARGIN_STATUS (BITS 4:3) RO

Indicates the current status of margin testing.

- If *ee_margin_status* = '00', Test has not been run
- If *ee_margin_status* = '01', Test has passed
- If *ee_margin_status* = '10', Test has failed
- If *ee_margin_status* = '11', Test is currently running

#### EE_MARGIN_MIN_DIS (BIT 2) R/W

Determines if the low margin testing will be performed or skipped.

- If *ee_margin_min_dis* = '0', Lower margin testing will be performed when margin testing is run.
- If *ee_margin_min_dis* = '1', Lower margin testing will not be performed when margin testing is run.

#### EE_MARGIN_MAX_DIS (BIT 1) R/W

Determines if the high margin testing will be performed or skipped.

- If *ee_margin_max_dis* = '0', Upper margin testing will be performed when margin testing is run.
- If *ee_margin_max_dis* = '1', Upper margin testing will not be performed when margin testing is run.

#### EE_MARGIN_START (BIT 0) R/W

Write to '1' to begin the margin testing. This bit self-clears when the margin testing finishes. If cleared during testing, the test will end prematurely.

### Volatile 0x85

#### LBIST_RESULT (BIT 5) RO

Indicates whether LBIST has passed or failed when run.

- If *lbist_result* = '0', LBIST test failed
- If *lbist_result* = '1', LBIST test passed

#### LBIST_STATUS (BIT 4) RO

Indicates when BIST test is finished.

- If *lbist_status* = '0', BIST is not finished or not started
- If *lbist_status* = '1', BIST has finished and lbist_result contains valid results.

### Volatile 0x86

#### MEMORY_ACCESS (BIT 1) RO

Set to '1' when access code is successfully sent.

### Volatile 0xA0

#### MANCH_EN (BIT 7) R/W

Disables the current device output and forces Manchester interface to be active.

- If *manch_en* = '0', Device is in normal operation mode and will output based on EEPROM settings
- If *manch_en* = '1', Device output is in High-Z mode, and Manchester is active and waiting for commands.

### Volatile 0xA1

#### LBIST_START (BITS 32:0) RO

Contains the calculated LBIST signature. This is internally compared against the expected value to determine if there are any internal logic failures.

### Volatile 0xA3

#### OFE (BIT: 12) RO

Indicates when the oscillator frequency error has occurred. This bit will NOT be asserted if the flag is masked.

#### SPE (BIT: 11) RO

Indicates when the shadow parity error has occurred. This bit will NOT be asserted if the flag is masked.

#### EUE (BIT: 10) RO

Indicates when the EEPROM uncorrectable error has occurred. This bit will NOT be asserted if the flag is masked.

#### OVCC (BIT: 9) RO

Indicates when the OVD error has occurred. This bit will NOT be asserted if the flag is masked.



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#### UVCC (BIT: 8) RO

Indicates when the UVD error has occurred. This bit will NOT be asserted if the flag is masked.

#### ESE (BIT: 7) RO

Indicates when the EEPROM single bit error has occurred. This bit will NOT be asserted if the flag is masked.

#### POR (BIT: 6) RO

Indicates when a power-on reset has occurred. This bit will NOT be asserted if the flag is masked.

#### SRR (BIT: 5) RO

Indicates when the signal radius is out of range. This bit will NOT be asserted if the flag is masked.

#### SLF (BIT: 4) RO

Indicates when an error is detected in the signal path logic. This bit will NOT be asserted if the flag is masked.

#### SAT (BIT: 3) RO

Indicates when saturation occurs within the signal path. This bit will NOT be asserted if the flag is masked.

#### TSE (BIT: 2) RO

Indicates when the temperature sensor is either in error our out of range. This bit will NOT be asserted if the flag is masked.

#### AOC (BIT: 1) RO

Indicates when the angle is outside of the clamped region. This bit will NOT be asserted if the flag is masked.

#### ACF (BIT: 0) RO

Indicates when a failure has occurred on the internal analog checks. This bit will NOT be asserted if the flag is masked.

### Volatile 0xA7

#### TEMPERATURE_16B (BITS: 31:16) RO

Contains the digital readout of the temperature sensor. This value is provided in 2's complement. Conversion to degrees can be done with the following equation:

$$Temperature\ [°C] = (temperature_16b) / 128 + 25°$$

#### ANGLE_16B (BITS: 15:0) RO

The calculated angle after all trimming and compensation. Conversion to degrees can be done with the following equation:

$$Angle\ [Deg] = angle_16b \times (360°)/2^{16}$$

### Volatile 0xA8

#### CHAN_B_16B (BITS: 31:16) RO

Final output of channel B after customer trimmed compensation. This value is directly input to the CORDIC calculation.

#### CHAN_A_16B (BITS: 15:0) RO

Final output of channel A after customer trimmed compensation. This value is directly input to the CORDIC calculation.

### Volatile 0xA9

#### CHAN_B_PRE_16B (BITS: 31:16) RO

Customer-trimmed output of channel B before the hysteresis filter.

#### CHAN_A_PRE_16B (BITS: 15:0) RO

Customer-trimmed output of channel A before the hysteresis filter.

### Volatile 0xAA

#### RADIUS_SQ_17B (BITS: 16:0) RO

The squared radius as calculated internally. This value is used to determine if the signal radius is out of range for the SSR flag.



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**Table 34: Register Description – EEPROM & Shadow**

| EEPROM Address (hex) | 31:26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | EEPROM Address (hex) | Shadow Address (hex) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x05 | ECC | | | dig_out_drive_sel | chan_b_hysteresis | | | | | | | | | | chan_a_hysteresis | | | | | | | | | | | | | 0x05 | 0x45 |
| 0x15 | ECC | | | | | | | | | | | spare_0x15 | | | | chan_orthog | | | | | | | | | | chan_b_dis | chan_a_dis | 0x15 | 0x55 |
| 0x16 | ECC | | | | | | | | | | ang_thresh_high | | | | | | | ang_thresh_low | | | | | | | | | ang_thresh_en | 0x16 | 0x56 |
| 0x17 | ECC | | | | | | | | | | | | chan_a_pol | chan_a_offs | | | | | | | | | | | | | | 0x17 | 0x57 |
| 0x18 | ECC | | | chan_a_offs_tc1_hot | | | | | | | | | | | | chan_a_offs_tc1_cold | | | | | | | | | | | | 0x18 | 0x58 |
| 0x19 | ECC | | | | | | | | | | | | | chan_a_sens | | | | | | | | | | | | | | 0x19 | 0x59 |
| 0x1A | ECC | | | | | chan_a_sens_tc1_hot | | | | | | | | | | | chan_a_sens_tc1_cold | | | | | | | | | | | 0x1A | 0x5A |
| 0x1B | ECC | | | | | | | chan_a_sens_tc2_hot | | | | | | | | | | chan_a_sens_tc2_cold | | | | | | | | | | 0x1B | 0x5B |
| 0x1C | ECC | | | | | | | | | | | | chan_b_pol | chan_b_offs | | | | | | | | | | | | | | 0x1C | 0x5C |
| 0x1D | ECC | | | chan_b_offs_tc1_hot | | | | | | | | | | | | chan_b_offs_tc1_cold | | | | | | | | | | | | 0x1D | 0x5D |
| 0x1E | ECC | | | | | | | | | | | | | chan_b_sens | | | | | | | | | | | | | | 0x1E | 0x5E |
| 0x1F | ECC | | | | | chan_b_sens_tc1_hot | | | | | | | | | | | chan_b_offs_tc1_hot | | | | | | | | | | | 0x1F | 0x5F |
| 0x20 | ECC | | temperature_offs | | | | | chan_b_sens_tc2_hot | | | | | | | | | | chan_b_sens_tc2_cold | | | | | | | | | | 0x20 | 0x60 |
| 0x21 | ECC | | | lin_coeff_0 | | | | | | | | | | | | spare_0x21 | | lin_coeff_active | | | | | lin_coeff_scalar | | lin_sel | lin_enable | 0x21 | 0x61 |
| – | ECC | | | – | | | | | | | | | | | | – | | | | | | | | | | | | – | – |
| 0x31 | ECC | | | lin_coeff_32 | | | | | | | | | | | | lin_coeff_31 | | | | | | | | | | | | 0x31 | 0x71 |
| 0x32 | ECC | | | | | | | | | | | | | | | | | | | | | | | | cordic_bypass | cordic_chan_order | cordic_pol | 0x32 | 0x72 |
| 0x33 | ECC | | | | bin_hyst | | | | | | | ang_gain | | | | | | | | | | | | | | | | 0x33 | 0x73 |
| 0x34 | ECC | | | | | ang_sat_rollover | | | | | ang_gain_sat_en | | | | | | | | | | | | | | | | ang_offs_sat_en | 0x34 | 0x74 |
| 0x35 | ECC | | | | | | | | | | | | | | | | | | | | | | | | | | | 0x35 | 0x75 |
| 0x36 | ECC | | | | | | | | | | | | | | | | | | | | | | | | | | | 0x36 | 0x76 |
| 0x37 | ECC | | | bw_adapt_max | | | bw_adapt_min | | | bw_sel | | | | | | | | | | | | | | | | | | 0x37 | 0x77 |

*Continued on next page...*



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**Table 34: Register Description – EEPROM and Shadow (continued)**

| EEPROM Address (hex) | 31:26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | EEPROM Address (hex) | Shadow Address (hex) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x38 | ECC | | | | | | power_on_delay | | | bw_adapt_delay | | | | | | | | | | bw_adapt_exp | | | | bw_adapt_frac | | | | 0x38 | 0x78 |
| 0x39 | ECC | | | sent_frame_rate | | sent_init_sel | | | sent_encoding_sel | sent_crc_sel | sent_emsg_dis | dig_out_pull_lim_dis | dig_out_pull_lim | | | dig_out_data_rate | | | | sent_data_sel | | | | dig_comm_id | dig_out_sel | | 0x39 | 0x79 |
| 0x3A | ECC | | | | | sent_emsg_err_repeat | sent_emsg_sel | | | | | | | | | | | | | | | | | | | | | 0x3A | 0x7A |
| 0x3B | ECC | enhanced_settings_unlock | dig_out_push_lim | | | dig_out_push_lim_sel | sat_chan_mask | sat_filt_mask | sat_cor_mask | sat_lin_mask | acf_fault_filt | | fault_filt | | | ovd_mask | uvd_mask | spe_mask | ese_mask | por_mask | srr_mask | slf_mask | ofe_mask | sat_mask | tse_mask | aoc_mask | acf_mask | 0x3B | 0x7B |
| 0x3C | ECC | | mem_lock_sel | | | manch_access_sel | test_mode_dis | ovd_sel | uvd_sel | spare_0x3c | | | | | | err_resp_sel_ov | | err_resp_sel | | err_resp_sel_uv | | err_hold_sel | | | dig_comm_input_high | dig_comm_input_low | 0x3C | 0x7C |
| 0x3D | ECC | spare_0x3d | | | | | | | | | | | | | | | | | | | | | | | | | | 0x3D | 0x7D |
| 0x3E | ECC | spare_0x3e | | | | | | | | | | | | | | | | | | | | | | | | | | 0x3E | 0x7E |
| 0x3F | ECC | spare_0x3f | | | | | | | | | | | | | | | | | | | | | | | | | | 0x3F | 0x7F |

The table above shows the location of all customer accessible EEPROM registers. Additionally, Shadow registers are mirrored in volatile space to allow quick access to the values during operating. All Shadow registers are located at an address 0x40 higher than the EEPROM register of which it is a copy. The Shadow registers are written with copies of the data from EEPROM at power up, and when an EEPROM write is performed. Values that are manually written to Shadow take effect immediately, and last until they are reset either by a changing the Shadow register itself, changing the EEPROM register, or power cycling the device. This allows quick testing of parameters with no risk of permanently changing the device performance. It also reduces the number of EEPROM writes required during testing which can improve test time, as EEPROM writes take longer than Shadow writes.

For all EEPROM and Shadow registers the first 6 most significant bits [31:26] are dedicated to ECC bits. These are used for internal testing to allow the device to correct single bit disturbances and detect double bit disturbances when copying EEPROM into Shadow. When performing an EEPROM/Shadow write there is no need to manually calculate the ECC bits. The ECC bits are ignored and replaced with the internally calculated values. During an EEPROM/Shadow read, the ECC bits will be transmitted along with the rest of the register data and may be ignored.



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## EEPROM 0x05 / Shadow 0x45

### DIG_OUT_DRIVE_SEL (BIT 23)

Selects the digital output driver mode.

- If *dig_out_drive_sel* = '0' the digital output driver functions as a push-pull output.
- If *dig_out_drive_sel* = '1' the digital output driver functions as an open-drain output.

### CHAN_B_HYST (BITS 22:13)

Selects the amount of hysteresis present on channel B of the 1-D signal path. This value directly selects the number of LSBs of hysteresis applied to each channel at a 1:1 ratio.

### CHAN_A_HYST (BITS 12:3)

Selects the amount of hysteresis present on channel A of the 1-D signal path. This value directly selects the number of LSBs of hysteresis applied to each channel at a 1:1 ratio.

## EEPROM 0x15 / Shadow 0x55

EEPROM 0x15 can be Factory or Customer accessible based on the bit *enhanced_settings_unlock*. When *enhanced_settings_unlock* = '0', EEPROM 0x15 is considered Factory space and cannot be written to at customer level. This can be used to prevent accidental changes to this value.

### SPARE_0X15 (BITS 15:11)

Spare bits that can be used as non-volatile storage within the device. This register has no effect on device performance.

### CHAN_ORTHOG (BITS 10:2)

*chan_orthog* determines the phase correction that is applied to channel B for the purposes of removing orthogonality error.

### CHAN_B_DIS (BIT 1)

Disables channel B when set.

- If *chan_b_dis* = '0', Channel B operates normally.
- If *chan_b_dis* = '1', Channel B is disabled.

### CHAN_A_DIS (BIT 0)

Disabled channel A when set.

- If *chan_a_dis* = '0', Channel A operates normally.
- If *chan_a_dis* = '1', Channel A is disabled.

## EEPROM 0x16 / Shadow 0x56

### ANG_THRESH_HIGH (BITS 16:9)

Sets a high angle saturation point before gain is applied to the channel. A diagnostic flag will trigger if the angle recorded is above the programmed value. *ang_thresh_high* can be set between 0 and 360 degrees with 1.41-degree steps. Since the value into the comparison is rolled over to 0–360, an *ang_thresh_high* value of 0 will always result in an error flag, and an *ang_thresh_high* value of 255 will never result in an error flag.

### ANG_THRESH_LOW (BITS 8:1)

Sets a low angle saturation point before gain is applied to the channel. A diagnostic flag will trigger if the angle recorded is below the programmed value. *ang_thresh_low* can be set between 0 and 360 degrees with 1.41 degree steps. Since the value into the comparison is rolled over to 0–360, an *ang_thresh_low* value of 0 will never result in an error flag, and an *ang_thresh_low* value of 255 will always result in an error flag.

| ANG_THRESH_LOW/HIGH | Degrees |
|---|---|
| 0 | 0 |
| x | x × 1.41 |
| 255 | 359.55 |

### ANG_THRESH_EN (BIT 0)

Enables the pre-gain saturation check.

- *ang_thresh_en* = '0', Angle saturation check is disabled.
- *ang_thresh_en* = '1', Angle value prior to gain block is checked against the programmed thresolds *ang_thresh_(low/high)* to set the saturation diagnostic flag.

## EEPROM 0x17 / Shadow 0x57

### CHAN_A_POL (BIT 14)

Changes the polarity of channel A when set.

- *chan_a_pol* = '0', Channel A follows axis definition.
- *chan_a_pol* = '1', Channel A polarity is inverted.

### CHAN_A_OFFS (BITS 13:0)

Customer offset trim at room temperature for channel A.

## EEPROM 0x18 / Shadow 0x58

### CHAN_A_OFFS_TC1_HOT (BITS 23:12)

Customer 1st order offset trim for room to hot slope of channel A.



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#### CHAN_A_OFFS_TC1_COLD (BITS 11:0)

Customer 1st order offset trim for room to cold slope of channel A.

### EEPROM 0x19 / Shadow 0x59

#### CHAN_A_SENS (BITS 13:0)

Customer sensitivity trim at room temperature for channel A.

### EEPROM 0x1A / Shadow 0x5A

#### CHAN_A_SENS_TC1_HOT (BITS 21:11)

Customer 1st order sensitivity trim for room to hot slope of channel A.

#### CHAN_A_SENS_TC1_COLD (BITS 10:0)

Customer 1st order sensitivity trim for room to cold slope of channel A.

### EEPROM 0x1B / Shadow 0x5B

#### CHAN_A_SENS_TC2_HOT (BITS 19:10)

Customer 2nd order sensitivity trim for room to hot slope of channel A.

#### CHAN_A_SENS_TC2_COLD (BITS 9:0)

Customer 2nd order sensitivity trim for room to cold slope of channel A.

### EEPROM 0x1C / Shadow 0x5C

#### CHAN_B_POL (BIT 14)

Changes the polarity of channel B when set.

- *chan_b_pol* = '0', Channel B follows axis definition.
- *chan_b_pol* = '1', Channel B polarity is inverted.

#### CHAN_B_OFFS (BITS 13:0)

Customer offset trim at room temperature for channel B.

### EEPROM 0x1D / Shadow 0x5D

#### CHAN_B_OFFS_TC1_HOT (BITS 23:12)

Customer 1st order offset trim for room to hot slope of channel B.

#### CHAN_B_OFFS_TC1_COLD (BITS 11:0)

Customer 1st order offset trim for room to cold slope of channel B.

### EEPROM 0x1E / Shadow 0x5E

#### CHAN_B_SENS (BITS 13:0)

Customer sensitivity trim at room temperature for channel B.

### EEPROM 0x1F / Shadow 0x5F

#### CHAN_B_SENS_TC1_HOT (BITS 21:11)

Customer 1st order sensitivity trim for room to hot slope of channel B.

#### CHAN_B_SENS_TC1_COLD (BITS 10:0)

Customer 1st order sensitivity trim for room to cold slope of channel B.

### EEPROM 0x20 / Shadow 0x60

#### TEMPERATURE_OFFS (BITS 24:20)

Customer temperature offset trim. Value is added to the temperature reported, represented in 2's complement format, step size is 0.5°C/LSB.

#### CHAN_B_SENS_TC2_HOT (BITS 21:11)

Customer 2nd order sensitivity trim for room to hot slope of channel B.

#### CHAN_B_SENS_TC2_COLD (BITS 10:0)

Customer 2nd order sensitivity trim for room to cold slope of channel B.

### EEPROM 0x21 / Shadow 0x61

#### LIN_COEFF_0 (BITS 25:13)

Linearization coefficient number 0. Functionality is based on linearization mode and scalar. See Linearization section for details.

#### SPARE_0X21 (BITS 12:10)

Spare bits that can be used as non-volatile storage within the device. This register has no effect on device performance.

#### LIN_COEFF_ACTIVE (BITS 9:5)

Determines the number of active linearization coefficients. See Linearization section for details.

#### LIN_COEFF_SCALAR (BITS 4:3)

Determines what scalar quantity is applied to the *lin_coeff_x* values. See Linearization section for details.



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### LIN_SEL (BITS 2:1)

Determines what function the linearization block performs on the signal path.

### LIN_ENABLE (BIT 0)

Enables the linearization block when set.

- If *lin_enable* = '0' linearization is disabled, and all related registers have no effect on device operation.
- If *lin_enable* = '1' linearization is enabled, and functions based on the linearization settings.

## EEPROM 0x22 / Shadow 0x62

### LIN_COEFF_2 (BITS 25:13)

Linearization coefficient number 2. Functionality is based on linearization mode and scalar. See Linearization section for details.

### LIN_COEFF_1 (BITS 12:0)

Linearization coefficient number 1. Functionality is based on linearization mode and scalar. See Linearization section for details.

## EEPROM 0x23 – 0x31 / Shadow 0x63 – 0x71

### LIN_COEFF_XX (BITS 25:13 & BITS 12:0)

The remaining linearization coefficients are stored in EEPROM registers 0x23 through 0x31. They follow the same pattern as EEPROM 0x22 with the higher coefficient value stored in bits 25:13 of the register, and the lower coefficient value stored in bits 12:0.

## EEPROM 0x32 / Shadow 0x72

### ANG_PRE_GAIN_OFFS (BITS 17:3)

The 2's complement value that is added to the digital angle prior to the gain stage of the short stroke block.

### CORDIC_BYPASS (BIT 2)

Bypasses the CORDIC angle calculation when set. The value that is passed through is based on the *cordic_chan_order* bit.

- If *cordic_bypass* = '0', device performs CORDIC angle calculation based on channel A and channel B data.
- If *cordic_bypass* = '1', no CORDIC calculation is performed, and the device passes through channel A or B directly through the rest of the signal path.

### CORDIC_CHAN_ORDER (BIT 1)

Determines the order of inputs to the CORDIC calculation or determines which channel to pass when *cordic_bypass* = '1'.

| CORDIC_BYPASS | CORDIC_CHAN_ORDER | Output of CORDIC |
|---|---|---|
| 0 | 0 | atan2(chanA, chanB) |
| 0 | 1 | atan2(chanB, chanA) |
| 1 | 0 | chanA+32768 |
| 1 | 1 | chanB+32768 |

### CORDIC_POL (BIT 0)

Inverts the polarity of the output of the CORDIC when set.

## EEPROM 0x33 / Shadow 0x73

### BIN_HYST (BITS 22:16)

Determines the amount of hysteresis for each bin when using binning mode of linearization.

### ANG_GAIN (BITS 15:0)

Determines the amount of that is applied to the signal within the short stroke block.

## EEPROM 0x34 / Shadow 0x74

### ANG_SAT_ROLLOVER (BITS 25:18)

Determines the saturation rollover point for the post gain signal value.

### ANG_GAIN_SAT_EN (BIT 17)

Determines the signal functionality in cases where the digital value exceeds the value set by the *ang_sat_rollover*.

- If *ang_gain_sat_en* = '0', the angle will 'rollover' back to 0.
- If *ang_gain_sat_en* = '1', the angle will saturate high or low based on the pre-gain angle and *ang_sat_rollover.*

### ANG_POST_GAIN_OFFS (BITS 16:1)

Offset value added to the digital signal after the gain of the short stroke block.

### ANG_OFFS_SAT_EN (BIT 0)

Enables the post gain saturation feature when set.

- If *ang_offs_sat_en* = '0' device will output the value after gain and offset, ignoring a*ng_sat_rollover.*
- If *ang_offs_sat_en* = '1' the device will either rollover or saturate the signal at the *ang_sat_rollover* based on the *ang_gain_sat_en* bit.

## EEPROM 0x35 / Shadow 0x75

### MAGNETIC_THRESH_MAX (BITS 17:10)

Sets the maximum magnetic magnitude threshold. All values



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above this set value will trigger an error flag.

### MAGNETIC_THRESH_MAX_EN (BIT 9)

Enables the maximum magnetic threshold checking when enabled.

- If *magnetic_thresh_max_en* = '0', *magnetic_thresh_max* is ignored.
- If *magnetic_thresh_max_en* = '1', magnetic magnitude is compared against *magnetic_thresh_max* and will trigger a flag if condition fails.

### MAGNETIC_THRESH_MIN (BITS 8:1)

Sets the minimum magnetic magnitude threshold. All values below this set value will trigger an error flag.

### MAGNETIC_THRESH_MIN_EN (BIT 0)

Enables the minimum magnetic threshold checking when enabled.

- If *magnetic_thresh_min_en* = '0', magnetic_thresh_min is ignored.
- If *magnetic_thresh_min_en* = '1', magnetic magnitude is compared against *magnetic_thresh_min* and will trigger a flag if condition fails.

## EEPROM 0x36 / Shadow 0x76

### CLAMP_LOWER (BITS 15:0)

Sets the low clamp value for the output of the digital signal path. All signals below this value will be limited to this value.

## EEPROM 0x37 / Shadow 0x77

### BW_ADAPT_MAX (BITS 24:22)

Sets the maximum bandwidth of the adaptive filter.

### BW_ADAPT_MIN (BITS 21:19)

Sets the minimum bandwidth of the adaptive filter.

### BW_SEL (BITS 18:16)

Determines which bandwidth settings to use for internal filtering.

| *bw_sel* | Bandwidth (Hz) |
|---|---|
| 0 | 329.1 |
| 1 | 465.8 |
| 2 | 556 |
| 3 | 700 |
| 4 | 1000 |
| 5 | 1482 |
| 6 | 2024 |
| 7 | Adaptive |

### CLAMP_UPPER (BITS 15:0)

Sets the upper clamp value for the output of the digital signal path. All signals above this value will be limited to this value.

## EEPROM 0x38 / Shadow 0x78

### POWER_ON_DELAY (BITS 20:18)

Selects the length of time for which the device will output the POR condition before beginning to transmit data. See Sensor Output During Low-Pass Filter Initialization section for more details.

| *power_on_delay* | Additional Delay (ms) |
|---|---|
| 0 | 0.5 |
| 1 | 1.0 |
| 2 | 1.5 |
| 3 | 2.0 |
| 4 | 2.5 |
| 5 | 3.0 |
| 6 | 4.0 |
| 7 | 0.0 |

### BW_ADAPT_DELAY (BITS 17:8)

Number of clock cycles at 8 MHz delay before the adaptive filter bandwidth decreases.

### BW_ADAPT_EXP (BITS 7:4)

Exponential gain of the feedforward adaptive filter loop.

### BW_ADAPT_FRACT (BITS3:0)

Fractional gain of the feedforward adaptive filter loop.



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## EEPROM 0x39 / Shadow 0x79

### SENT_FRAME_RATE (BITS 23:22)

Sets the frame rate when using paused SENT.

| *sent_frame_rate* | Frame Rate including pause pulse |
|---|---|
| 0 | 3 data nibbles: frame length 210 $t_{tick}$<br>4 data nibbles: frame length 228 $t_{tick}$<br>6 data nibbles: frame length 282 $t_{tick}$ |
| 1 | 0.5 ms |
| 2 | 1.0 ms |
| 3 | 2.0 ms |

### SENT_INIT_SEL (BITS 21:19)

Selects which data the SENT interface will transmit during the initialization time. If no initialization time is selected this register does nothing.

| *sent_init_sel* | n-bit data Output |
|---|---|
| 0 | 0 |
| 1 | $2^n - 7$ |
| 2 | $2^n - 4$ |
| 3 | $2^n - 3$ |
| 4 | $2^n - 2$ |
| 5 | $2^n - 1$ |
| 6 | 0 |
| 7 | 0 |

### SENT_ENCODING_SEL (BIT 18)

Selects SENT data mapping for SENT configurations 0, 4, 7, and 15.

- If *sent_encoding_sel* = '0', mapping is disabled, SENT will output the data as it appears in the registers.
- If *sent_encoding_sel* = '1', output SENT data is remapped per the table below.

| DATA Value | SENT Output |
|---|---|
| 0 | 1 |
| 1 through $2^{n-8}$ | Unchanged |
| >=$2^{n-8}$ | $2^{n-8}$ |
| SCN 1 Error flag | $2^{n-5}$ |
| SCN 2 Error flag | $2^{n-6}$ |
| Not Valid | 0 |

* n is the number of bits in the data of the SENT packet.

** Not valid refers to the period of time after power up before the SENT interface receives the first valid update from the signal path.

### SENT_CRC_SEL (BIT 17)

Includes the SCN nibble in the CRC calculations when set.

### SENT_EMSG_DIS (BIT 16)

Disables SENT serial message when set.

### DIG_OUT_PULL_LIM_DIS (BIT 15)

Disables slew rate control when set.

### DIG_OUT_PULL_LIM (BITS 14:12)

Selects the slew rate control for digital drivers.

### DIG_OUT_DATA_RATE (BITS 11:7)

Selects the tick time if using SENT interface, or the period when using the PWM interface.

### SENT_DATA_SEL (BITS 6:3)

Selects the SENT data configuration.

### DIG_COMM_ID (BIT 2)

Sets the device ID for Manchester communication protocol.

### DIG_OUT_SEL (1:0)

Selects the output mode for digital interface devices.

| *dig_out_sel* | Output Protocol |
|---|---|
| 0 | PWM |
| 1 | SENT |
| 2 | SENT with Pause Pulse |
| 3 | PWM |

## EEPROM 0x3A / Shadow 0x7A

### SENT_EMSG_ERR_REPEAT (BIT 21)

Enables SENT message repeat when set.

### SENT_EMSG_SEL (BITS 20:0)

Selects which EMSG messages will be sent.

## EEPROM 0x3B / Shadow 7B

### ENHANCED_SETTINGS_UNLOCK (BIT 25)

Enables write access to register 0x16 when set.

### SPARE_0X3B (BITS 24:23)

Spare bits that can be used as non-volatile storage within the device. This register has no effect on device performance.



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### DIG_OUT_PUSH_LIM (BITS 24:22)

Selects the digital output push driver current limit. Approximate current limits are provided below:

| *dig_out_push_lim* | Current Limit (mA) |
|---|---|
| 0 | 10 |
| 1 | 8.75 |
| 2 | 7.5 |
| 3 | 6.25 |
| 4 | 5 |
| 5 | 3.75 |
| 6 | 2.5 |
| 7 | 1.25 |

### DIG_OUT_PUSH_LIM_SEL (BIT 21)

Disables the digital push driver current limit.

- If *dig_out_push_lim_dis* = '0' current limit is set by *dig_out_push_lim* register.
- If *dig_out_push_lim_dis* = '1' current limit is ~20 mA

### SAT_COR_MASK (BIT 20)

Disables the channel level saturation sub-flag when set. This mask only effects the error flag reporting ability and does not change the effects of saturation on the signal path data.

### SAT_FILT_MASK (BIT 19)

Disables the filter level saturation sub-flag when set. This mask only effects the error flag reporting ability and does not change the effects of saturation on the signal path data.

### SAT_COR_MASK (BIT 18)

Disables the saturation correction error flag when set. This mask only affects the error flag reporting ability. It does not change the effect of the saturation on the signal path data.

### SAT_LIN_MASK (BIT 17)

Disables the saturation linearization error flag when set. This mask only affects the error flag reporting ability. It does not change the effect of the saturation on the signal path data.

### ACF_FAULT_FILT (BITS 16:15)

Filters the ACF fault condition, the error condition must be present for the number of cycles shown below before a fault flag is tripped.

| *acf_fault_filt* | Cycles |
|---|---|
| 0 | 0 |
| 1 | 2 |
| 2 | 4 |
| 3 | 8 |

### FAULT_FILT (BITS 14:12)

Filters the SAT, AOC, and SRR flags; each error condition must be present for the number of cycles shown below before their respective flag is tripped. Additionally, also sets the number of temperature updates for which the temperature sensor must be in error before a TSE flag is set

| *fault_filt* | SAT, AOC, SSR [Cycles] | TSE [Temperature Updates] |
|---|---|---|
| 0 | 0 | 1 |
| 1 | 2 | 2 |
| 2 | 4 | 4 |
| 3 | 8 | 8 |
| 4 | 16 | 16 |
| 5 | 32 | 2 |
| 6 | 64 | 4 |
| 7 | 128 | 8 |

### OVD_MASK (BIT 11)

Disables the overvoltage detection error flag when set.

### UVD_MASK (BIT 10)

Disables the undervoltage detection error flag when set.

### SPE_MASK (BIT 9)

Disables the signal path error flag when set.

### ESE_MASK (BIT 8)

Disables the EEPROM single bit error flag when set.

### POR_MASK (BIT 7)

Disables the power-on reset error flag when set.



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### SRR_MASK (BIT 6)

Disables the signal radius out of range error flag when set.

### SLF_MASK (BIT 5)

Disables the signal processing logic failure error flag when set.

### OFE_MASK (BIT 4)

Disables the oscillator frequency error flag when set.

### SAT_MASK (BIT 3)

Disables the saturation error flag when set.

### TSE_MASK (BIT 2)

Disables the temperature sensor error flag when set.

### AOC_MASK (BIT 1)

Disables the angle outside of clamp error flag when set.

### ACF_MASK (BIT 0)

Disables the analog check failure error flag when set.

## EEPROM 0x3C / Shadow 0x7C

### MEM_LOCK_SEL (BITS 24:21)

Prevents writes to EEPROM memory when set.

### MANCH_ACCESS_SEL (BITS 20:19)

Disables Manchester entry triggers.

| *manch_access_sel* | Manchester Entry Method |
|---|---|
| 00 | Manchester enabled by OVD or function pulses |
| 01 | Manchester enabled by OVD only |
| 10 | Manchester enabled by function pulses only |
| 11 | Manchester cannot be enabled |

* Note: Setting *manch_access_sel* = '11' prevents all further communication.

### TEST_MODE_DIS (BIT 18)

Disables internal test modes which affect the device output (Margin testing). In order to perform margin testing with this bit active, it must first be cleared in Shadow before margin testing can be run. This is provided to prevent single bit error in volatile space from causing an invalid output.

### OVD_SEL (BIT 17)

Selects which overvoltage value to use when determining if an overvoltage error occurred.

### UVD_SEL (BIT 16)

Selects which undervoltage value to use when determining if an undervoltage error occurred.

### SPARE_0X3C (BITS 15:12)

Spare bits that can be used as non-volatile storage within the device. This register has no effect on device performance.

### ERR_RESP_SEL_OV (BITS 11:10)

Selects how the device responds to overvoltage conditions when manch_access_sel = 2'b1X.

| *err_resp_sel_ov* | *manch_access_sel* | Output Response |
|---|---|---|
| XX | 0X | High-Z |
| 00 | 1X | Based on output prorotocol |
| 01 | 1X | High-Z |
| 10 | 1X | High* |
| 11 | 1X | LOW** |

### ERR_RESP_SEL (BITS 9:8)

Selects how the device responds to error flags.

| *err_resp_sel* | Output Response |
|---|---|
| 00 | Based on output protocol |
| 01 | High-Z |
| 10 | HIGH* |
| 11 | RESERVED |

### ERR_RESP_SEL_UV (BITS 7:6)

| *err_resp_sel_uv* | Output Response |
|---|---|
| 00 | High-Z |
| 01 | HIGH* |
| 10 | LOW** |
| 11 | High-Z |

* Device can only drive HIGH if *dig_out_drive_sel* = 0, otherwise output will be High-Z

** If manch_access_sel = 2'bX0 recovery from an error reported as LOW may be delayed by an additional Manchester code time-out length (300 uS)



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### ERR_HOLD_SEL (BITS 5:3)

Selects the number of updates the SENT and PWM interface report a UVD error condition for after returning to normal $V_{CC}$ levels.

| *err_hold_sel* | Digital UVD Reports |
|---|---|
| 0 | 1 |
| 1 | 2 |
| 2 | 4 |
| 3 | 8 |
| 4 | 16 |
| 5 | 32 |
| 6 | 64 |
| 7 | 128 |

### DIG_COMM_INPUT_HIGH (BIT 1)

Sets the threshold for the rising edge when determining Manchester data input.

### DIG_COMM_INPUT_LOW (BIT 0)

Sets the threshold for the falling edge when determining Manchester data input. Also determines the low threshold for overdriving the output to initiate Manchester interface when in digital modes.



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## PACKAGE OUTLINE DRAWING

**For Reference Only – Not for Tooling Use**

(Reference DWG-0000409, Rev. 2)
Dimensions in millimeters – NOT TO SCALE
Dimensions exclusive of mold flash, gate burs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

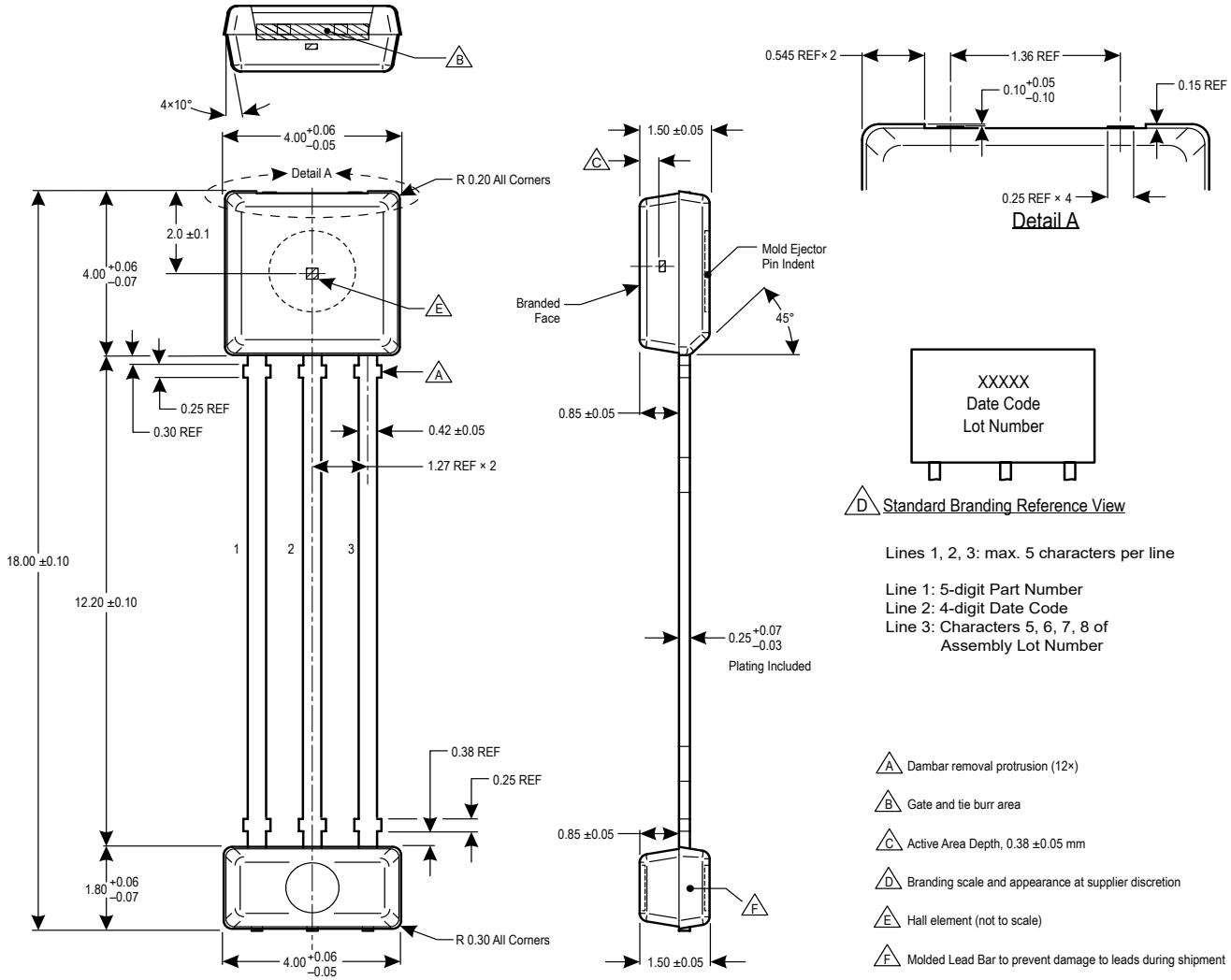



**Figure 31: 3-Pin SIP (Suffix UC)**



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## Revision History

| Number | Date | Description |
|---|---|---|
| – | September 14, 2022 | Initial release |
| 1 | November 3, 2022 | Updated Angle Drift TBD values (page 8) and Channel Drift values (page 9); removed TBD Angle Error rows (page 9) |
| 2 | November 29, 2022 | Updated Figure 8 (page 19), and Table 32 (page 45, error flag UVD SENT and PWM Response) |

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