A1338

Precision, Hall-Effect Angle Sensor IC with SPI, and SENT or PWM Outputs

FEATURES AND BENEFITS

- Contactless 0° to 360° angle sensor IC, for angular position and rotation direction measurement
  - □ Circular Vertical Hall (CVH) technology provides a single-channel sensor system, with air gap independence
- 12-bit resolution possible in Low RPM mode, 10-bit resolution in High RPM mode
- Angle Refresh Rate (output rate) configurable between 25 and 3200 µs through EEPROM programming
  - □ Capable of sensing magnetic rotational speeds up to 7600 rpm, and up to 30,000 rpm with reduced accuracy
- SPI (mode 3), and SENT (Single Edge Nibble Transmission) or PWM (Pulse-Width Modulation)*

Continued on the next page…

PACKAGES:

14-pin TSSOP (Suffix LE) **24-pin TSSOP (Suffix LE)**



Not to scale

Single SoC Dual Independent SoCs

DESCRIPTION

The A1338 is a 0° to 360° angle sensor IC that provides contactless high-resolution angular position information based on magnetic circular vertical Hall (CVH) technology. It has a system-on-chip (SoC) architecture that includes: a CVH front end, digital signal processing, digital SPI, and SENT or PWM outputs. It also includes on-chip EEPROM technology, capable of supporting up to 100 read/write cycles, for flexible end of line programming of calibration and configuration parameters. The A1338 is ideal for automotive applications requiring 0° to 360° angle measurements, such as electronic power steering (EPS), seatbelt motor position systems, rotary PRNDLs, and throttle systems.

The A1338 was designed with safety-critical application requirements in mind. It includes user-controlled on-chip logic built-in self-test (LBIST) and full signal path diagnostics to enable customers to determine if the IC is operating in a proper manner.

The A1338 supports a Low RPM mode for slower rate applications and a High RPM mode for high-speed applications. High RPM mode is for applications that require higher refresh rates to minimize error due to latency. Low RPM mode is for applications that require higher resolution operating at lower angular velocities.

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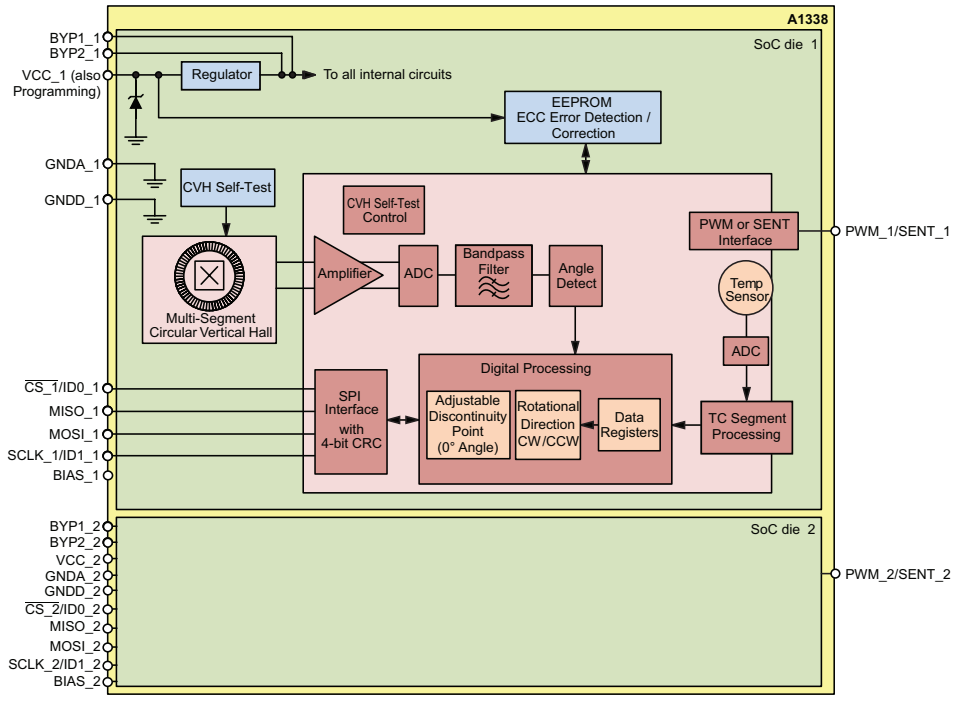


Figure 1: A1338 Magnetic Circuit and IC Diagram

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FEATURES AND BENEFITS (continued)

- □ SPI interface provides a robust communication protocol for fast angle readings*
- □ SENT output supports four modes: SAEJ2716 (JAN2010) and Allegro proprietary options of Triggered SENT (TSENT), Sequential SENT (SSENT), and Addressable SENT (ASENT)*
- □ Programmable via Manchester Encoding on the VCC line, reducing external wiring*
- □ SPI and SENT interfaces allows use of multiple independent sensors for applications requiring redundancy*

- Advanced diagnostics to support safety-critical applications, including:
  - □ On-chip, user-controlled logic built-in self-test (LBIST) and signal path diagnostics
  - □ 4-bit CRC on SPI messages
  - □ User-Programmable Missing Magnet Error flag for notifying controller of low magnetic field level
- Diagnostics are initiated over the SPI or SENT interface and can directly test proper operation of the IC in safety-critical applications
- EEPROM with Error Correction Control (ECC) configuration, sensor calibration including end-of line adjustments like programmable angle reference (0°) position and rotation direction (CW or CCW)
- Available in both single-die and dual-die configurations
  - □ Dual-die devices contain two independent die housed within a single package
- Absolute maximum V_{CC} of 26.5 V for increased robustness and direct connection to automotive vehicle battery

* See Selection Guide for more details.

DESCRIPTION (continued)

The A1338 is available in single-die 14-pin TSSOP and a dual-die 24-pin TSSOP. Both packages are lead (Pb) free with 100% matte-tin leadframe plating.

SELECTION GUIDE

Part Number	System Die	Output Protocols	Package	Packing [1]
A1338LLETR-DD-T	Dual	SPI and SENT	24-pin TSSOP	4000 pieces per 13-in. reel
A1338LLETR-P-DD-T	Dual	SPI and PWM	24-pin TSSOP	4000 pieces per 13-in. reel
A1338LLETR-T	Single	SPI and SENT	14-pin TSSOP	4000 pieces per 13-in. reel
A1338LLETR-P-T	Single	SPI and PWM	14-pin TSSOP	4000 pieces per 13-in. reel

[1] Contact Allegro™ for additional packing options.

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ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Forward Supply Voltage	V_{CC}	Not sampling angles	26.5	V
Reverse Supply Voltage	V_{RCC}	Not sampling angles	–18	V
All Other Pins Forward Voltage	V_{IN}		5.5	V
All Other Pins Reverse Voltage	V_R		0.5	V
Operating Ambient Temperature	T_A	L range	–40 to 150	°C
Maximum Junction Temperature	T_J(max)		165	°C
Storage Temperature	T_{stg}		–65 to 170	°C

THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

Characteristic	Symbol	Test Conditions [1]	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	LE-24 package	117	°C/W
		LE-14 package	82	°C/W

[1] Additional thermal information available on the Allegro website.

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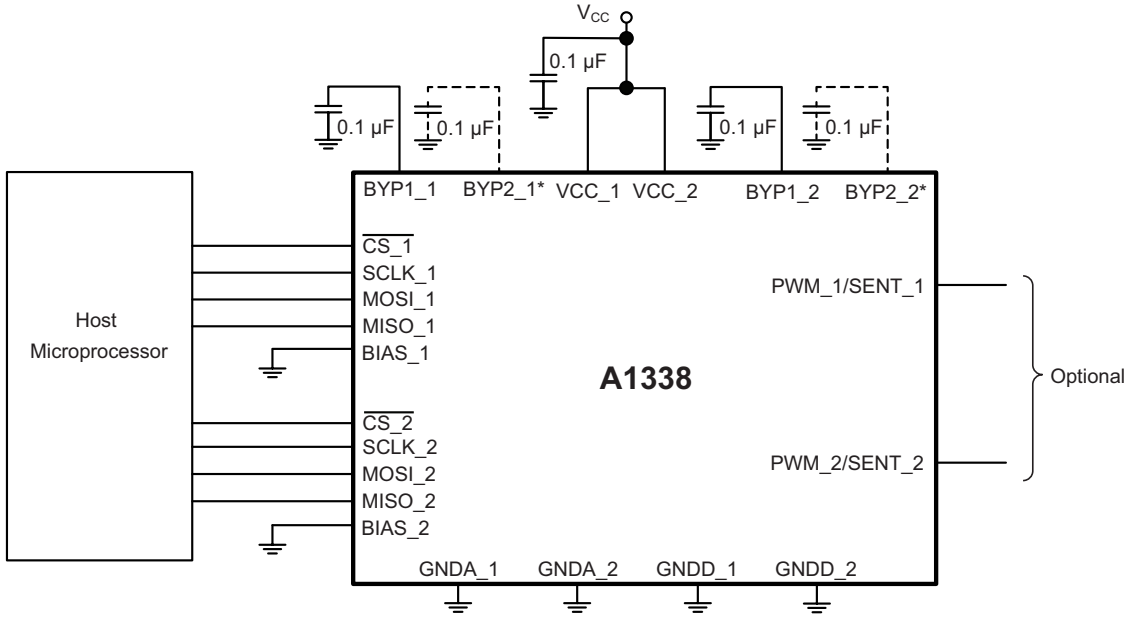


Figure 2: Typical A1338 Configuration Using SPI Interface

Either or both internal SoCs can be operated simultaneously.
(See "EMC Reduction" Section for application circuits that require a higher level of EMC immunity.)
* Secondary bypass capacitors only required when using Elevated SPI Output Voltage. Contact Allegro for availability.

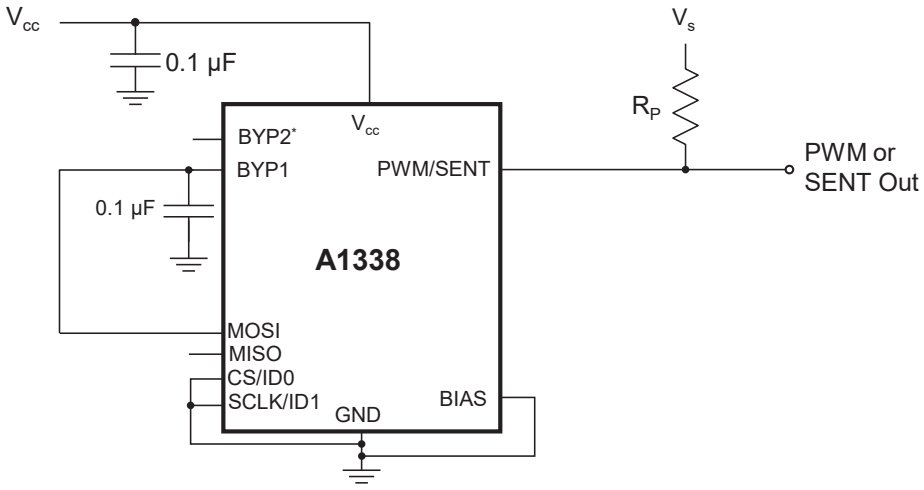


Figure 3: Typical A1338 Configuration Using PWM or SENT Output. ID Value of 00_2.

ID0/ID1 brought to BYP or GND to configure Manchester address.
When configuring an IC for address 00_2, MOSI should be tied to BYP.
* Secondary bypass capacitors only required when using Elevated SPI Output Voltage. Contact Allegro for availability.

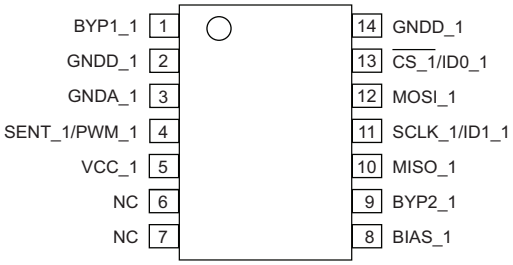
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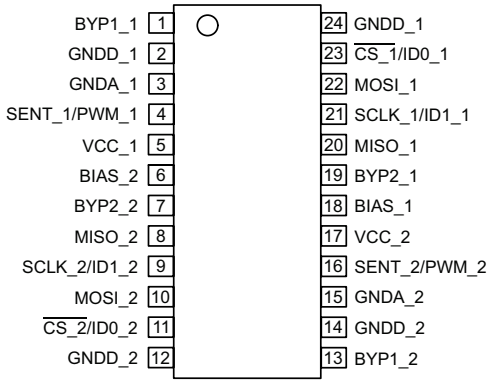
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PINOUT DIAGRAMS AND TERMINAL LIST



14-Pin TSSOP LE Package Pinouts



24-Pin TSSOP LE Package Pinouts

Terminal List Table

Pin Name	Pin Number		Function
	LE-14	LE-24	
BYP1_1	1	1	External Bypass Capacitor Terminal for Internal Regulator (die 1)
BYP2_1	9	19	External Bypass Capacitor Terminal for Internal Regulator (die 1)
BYP1_2	–	13	External Bypass Capacitor Terminal for Internal Regulator (die 2)
BYP2_2	–	7	External Bypass Capacitor Terminal for Internal Regulator (die 2)
$\overline{CS_1}$ /ID0_1	13	23	Option 1: SPI Chip Select Terminal, Active Low Input(die 1)
			Option 2: ID0 bit to indicate Slave Address for SSENT or ASENT communication modes only (die 1)
$\overline{CS_2}$ /ID0_2	–	11	Option 1: SPI Chip Select Terminal, Active Low Input(die 2)
			Option 2: ID0 bit to indicate Slave Address for SSENT or ASENT communication modes only (die 2)
GNDA_1	3	3	Device Analog Ground Terminal (die 1)
GNDA_2	–	15	Device Analog Ground Terminal (die 2)
GNDD_1	2, 14	2, 24	Device Digital Ground Terminal (die 1)
GNDD_2	–	12, 14	Device Digital Ground Terminal (die 2)
MISO_1	10	20	SPI Master Input/Slave Output (die 1)
MISO_2	–	8	SPI Master Input/Slave Output (die 2)
MOSI_1	12	22	SPI Master Output Slave Input (die 1)
MOSI_2	–	10	SPI Master Output Slave Input (die 2)
SLCK_1/ID1_1	11	21	Option 1: SPI Clock Terminal (die 1)
			Option 2: ID1 bit to indicate Slave Address for SSENT or ASENT communication modes only (die 1)
SCLK_2/ID1_2	–	9	Option 1: SPI Clock Terminal (die 2)
			Option 2: ID1 bit to indicate Slave Address for SSENT or ASENT communication modes only (die 2)
SENT_1/PWM_1	4	4	SENT Output (Die1); PWM Output (Die1); SENT for A1338LLETR-DD-T, A1338LLETR-T; PWM for A1338LLETR-P-DD-T, A1338LLETR-P-T
SENT_2/PWM_2	–	16	SENT Output (Die2); PWM Output (Die2); SENT for A1338LLETR-DD-T, A1338LLETR-T; PWM for A1338LLETR-P-DD-T, A1338LLETR-P-T
BIAS_1	8	18	Bias Connection; connect to ground or pull up to 3.3 V (die 1)
VCC_1	5	5	Power Supply (die 1); also used for EEPROM Programming
VCC_2	–	17	Power Supply (die 2); also used for EEPROM Programming
BIAS_2	–	6	Bias Connection; connect to ground or pull up to 3.3 V (die 2)
NC	6, 7	–	Not internally connected; tie to GNDD

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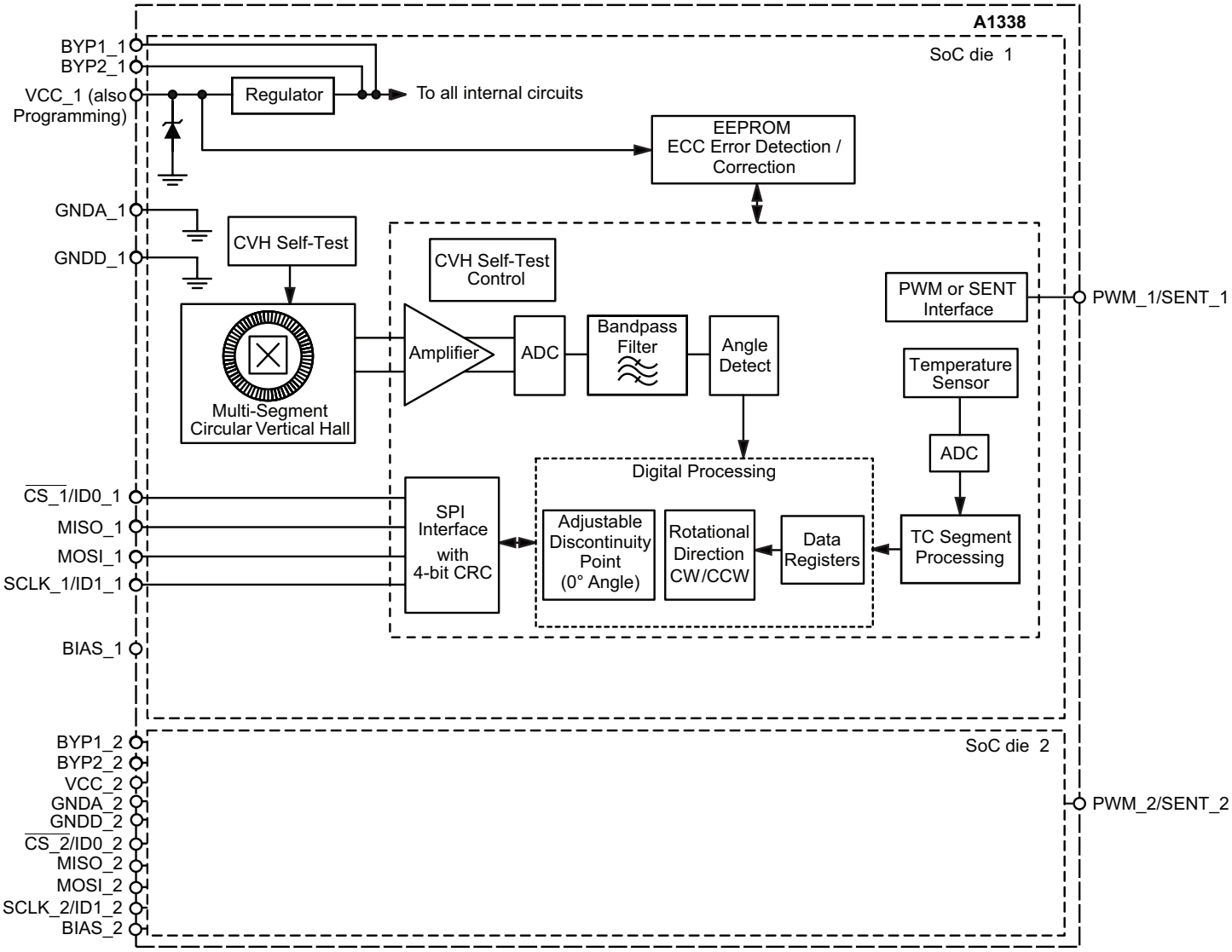


Figure 4: Functional Block Diagram

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OPERATING CHARACTERISTICS: Valid over the full operating voltage and ambient temperature ranges, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ. [1]	Max.	Unit [2]
ELECTRICAL CHARACTERISTICS						
Supply Voltage	V_{CC}		3.7	–	16	V
Supply Current	I_{CC}	Each die, T_A = 150°C	–	8.25	10	mA
Undervoltage Lockout Threshold Voltage [3]	V_{UVLOHI}	Maximum V_{CC}, dV/dt = 1V/ms, T_A = 25°C	–	–	3.6	V
	$V_{UVLOLOW}$	Maximum V_{CC}, dV/dt = 1V/ms, T_A = 25°C	2.9	–	–	V
VCC Low Flag Threshold [4]	V_{UVLOTH}		3.5	–	3.9	V
Supply Zener Clamp Voltage	V_{ZSUP}	I_{CC} = $I_{CC(AWAKE)}$ + 3 mA, T_A = 25°C	26.5	40	–	V
Reverse-Battery Current	I_{RCC}	V_{RCC} = –18 V, T_A = 25°C	–5	–	0	mA
Power-On Time [5]	t_{PO}		–	300	–	µs
Bypass1 Pin Output Voltage [6]	V_{BYP1}	T_A = 25°C, C_{BYP} = 0.1 µF	2.5	2.7	2.9	V
Bypass2 Pin Output Voltage [6] (Elevated SPI Output Mode)	V_{BYP2}	T_A = 25°C, C_{BYP2} = 0.1 µF; Contact Allegro for availability	2.9	3.1	3.3	V
SPI INTERFACE SPECIFICATIONS						
Digital Input High Voltage [7]	V_{IH}	MOSIx, SCLKx, $\overline{CS}$x pins	2.4	–	5.5	V
Digital Input Low Voltage [7]	V_{IL}	MOSIx, SCLKx, $\overline{CS}$x pins	–	–	0.5	V
CSx Pin Input Bias Current	I_{BIAS}	V_{CSx} = 3.3 V	–	15	–	µA
SPI Output High Level	V_{OH1}	MISOx pins, C_L = 20 pF, C_{BYP1} = 0.1 µF, C_{BYP2} grounded	2.5	2.7	2.9	V
SPI Output High Level (Elevated SPI Output Mode)	V_{OH2}	MISOx pins, C_L = 20 pF, C_{BYP1} = 0.1 µF, C_{BYP2} = 0.1 µF. Contact Allegro for availability.	2.9	3.1	3.3	V
SPI Output Low Voltage	V_{OL}	MISOx pins, C_L = 20 pF	–	0.3	–	V
SPI Clock Frequency [7]	f_{SCLK}	MISOx pins, C_L = 20 pF	0.1	–	10	MHz
SPI Clock Duty Cycle [7]	D_{fSCLK}	$SPICLK_{DC}$, 5 V compliant	40	–	60	%
SPI Frame Rate [7]	t_{SPI}	5 V compliant	5.8	–	588	kHz
Chip-Select to First SCLK Edge [7]	t_{CS}	Time from $\overline{CS}$x going low to SCLKx falling edge	50	–	–	ns
Data Output Valid Time [7]	t_{DAV}	Data output valid after SCLKx falling edge	–	–	40	ns
MOSI Setup Time [7]	t_{SU}	Input setup time before SCLKx rising edge	25	–	–	ns
MOSI Hold Time [7]	t_{HD}	Input hold time after SCLKx rising edge	40	–	–	ns
SCLK to CS Hold Time [7]	t_{CHD}	Hold SCLKx high time before $\overline{CS}$x rising edge	5	–	–	ns
Capacitive Load [7]	C_L	Loading on digital output (MISOx) pin with SPI Clock Frequency = 10 MHz	–	–	20	pF

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OPERATING CHARACTERISTICS (continued): Valid over the full operating voltage and ambient temperature ranges, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ. [1]	Max.	Unit [2]
PWM INTERFACE SPECIFICATIONS (A1338LLETR-P-DD-T and A1338LLETR-P-T variants only)						
PWM Carrier Frequency	f_{PWM}	PWM Frequency Code = 00	–	122	–	Hz
		PWM Frequency Code = 01	–	1.024	–	kHz
		PWM Frequency Code = 10	–	2.048	–	kHz
PWM Duty Cycle Minimum	$D_{PWM(min)}$		–	5	–	%
PWM Duty Cycle Maximum	$D_{PWM(max)}$		–	95	–	%
PWM Output Signal [8]	$V_{PWM(L)}$	5 kΩ ≤ R_{pullup} ≤ 50 kΩ	–	–	0.2	V
		2 kΩ ≤ R_{pullup} < 5 kΩ	–	–	0.4	V
	$V_{PWM(H)}$	Minimum R_{pullup} = 2 kΩ	0.9 × V_S	–	–	V
		Maximum R_{pullup} = 50 kΩ	0.7 × V_S	–	–	V
Maximum Sink Current	I_{LIMIT}	Output FET on, T_A = 25°C	–	30	–	mA
PWM Carrier Frequency Tolerance [7]	–	Deviation from expected f_{PWM}	–10	–	10	%
PWM Resolution	–	12-bit angle value		0.022	–	%DC/LSB
PWM Frequency Jitter	$f_{PWM(JITTER)}$	1σ, T_A = 25°C, f_{PWM} = 2 kHz		0.18	–	Hz
		1σ, T_A = 25°C, f_{PWM} = 1 kHz		0.11	–	Hz
		1σ, T_A = 25°C, f_{PWM} = 124 Hz		0.01	–	Hz
PWM Duty Cycle Jitter	$D_{PWM(JITTER)}$	3σ, 300 G, T_A = 25°C, no AVG		0.095	–	%DC
		3σ, 300 G, f_{PWM} = 2 kHz, AVG = 0x4 or greater		0.095	–	%DC
		3σ, 300 G, f_{PWM} = 1 kHz, AVG = 0x5 or greater		0.03	–	%DC
		3σ, 300 G, f_{PWM} = 124 Hz, AVG = 0x7		0.027	–	%DC
PWM Thermal Duty Cycle Drift [7]	$D_{PWM(THDRIFT)}$	Change in duty cycle from 25°C to 150°C; 300 G	–0.35	–	0.35	%DC
SENT PROTOCOL SPECIFICATIONS (A1338LLETR-DD-T and A1338LLETR-T variants only)						
SENT Message Duration	t_{CVHST}	Tick time = 3 µs	–	–	1	ms
Minimum Programmable SENT Message Duration	$t_{SENTMIN}$	Tick time = 0.5 µs, 3 data nibbles, SCN, and CRC, nibble length = 27 ticks	–	96	–	µs
SENT Output Signal [7]	$V_{SENT(L)}$	5 kΩ ≤ R_{pullup} ≤ 50 kΩ	–	–	0.2	V
		2 kΩ ≤ R_{pullup} < 5 kΩ	–	–	0.4	V
	$V_{SENT(H)}$	Minimum R_{pullup} = 2 kΩ	0.9 × V_S	–	–	V
		Maximum R_{pullup} = 50 kΩ	0.7 × V_S	–	–	V
SENT Output Trigger Signal	$V_{SENTtrig(L)}$		–	–	1.4	V
	$V_{SENTtrig(H)}$		2.8	–	–	V
Minimum Time Frame for SENT Trigger Signal	$t_{SENTMIN}$	Tick time = 0.5 µs, 3 data nibbles, SCN, and CRC, nibble length = 27 ticks	2	–	–	µs
Triggered Delay Time	t_{dSENT}	From end of trigger pulse to beginning of SENT message frame. TSENT (SENT_MODE 3 and SENT_MODE 4)	–	7	–	tick
Maximum Sink Current	I_{LIMIT}	Output FET on, T_A = 25°C	–	30	–	mA
DIAGNOSTIC SPECIFICATIONS						
CVH Self-Test Time	t_{UI_DIAG}		–	23	–	ms
Logic BIST Coverage vs. Time	$t_{LBISTXX}$	70% Coverage	–	10	–	ms

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OPERATING CHARACTERISTICS (continued): Valid over the full operating voltage and ambient temperature ranges, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ. [1]	Max.	Unit [2]
EEPROM PROGRAMMING PULSES						
Pulse High Time	$t_{PULSE(H)}$	Time above minimum pulse voltage	8	10	11	ms
Rise Time	t_r	10% to 90% of minimum pulse level	300	–	–	µs
Fall Time	t_f	10% to 90% of minimum pulse level	60	–	–	µs
Pulse Voltage	V_{PULSE}	Applied on VCC line	18	19	19.5	V
Separation Time	$t_{PULSE(f-r)}$	Timing between first pulse dropping below 6 V and 2nd pulse rising above 6 V	0.002	–	50	ms
MAGNETIC CHARACTERISTICS						
Magnetic Field	B	Range of input field	–	–	1500	G_{pp}
ANGLE CHARACTERISTICS						
Digital Output Word Length [8]	RES_{ANGLE}		–	12	–	bit
Effective Resolution [9]		B = 300 G, T_A = 25°C, ORATE = 0	–	11.59	–	bit
Angle Refresh Rate [10]	t_{ANG}	High RPM mode	–	25	–	µs
		Low RPM mode, AVG = 011 (varies with AVG mode, refer to the appendix *Programming Reference*)	–	200	–	µs
Response Time	$t_{RESPONSE}$	Low RPM mode (see Figure 4)	–	60	–	µs
Angle Error	ERR_{ANG}	T_A = 25°C, ideal magnet alignment, B = 300 G, target rpm = 0	–	0.5	–	degrees
		T_A = 150°C, ideal magnet alignment, B = 300 G, target rpm = 0	–1.3	–	1.3	degrees
Angle Noise	N_{ANG}	T_A = 25°C, B = 300 G, 3 sigma noise, no internal filtering	–	0.35	–	degrees
		T_A = 150°C, no internal filtering, B = 300 G, 3 sigma noise, target rpm = 0	–	0.55	–	degrees
Temperature Drift	$ANGLE_{DRIFT}$	T_A = 150°C, B = 300 G	–1.4	–	1.4	degrees
		T_A = –40°C, B = 300 G	–	±1	–	degrees
Angle Drift Over Lifetime	$ANGLE_{DRIFT-LIFE}$	B = 300 G, typical maximum drift observed after AEC-Q100 qualification testing	–	±0.5	–	degrees

[1] Typical data is at T_A = 25°C and V_{CC} = 5 V, and it is for design estimates only.
[2] 1 G (gauss) = 0.1 mT (millitesla).
[3] At power-on, a die will not respond to commands until V_{CC} rises above V_{UVLOHI}. After that, the die will perform and respond normally until V_{CC} drops below $V_{UVLOLOW}$.
[4] VCC Low Threshold Flag will be sent via the SPI interface as part of the angle measurement.
[5] During the power-on time period, the A1338 SPI transactions are not guaranteed.
[6] The output voltage and current specifications are to aid in PCB design. The pin is not intended to drive any external circuitry. The specifications indicate the peak capacitor charging and discharging currents to be expected during normal operation.
[7] Parameter is not guaranteed at final test. Determined by design.
[8] RES_{ANGLE} represents the number of bits of data available for reading from the die registers.
[9] Effective Resolution is calculated using the formula below:

$$log_2(360) - log_2\left(\frac{1}{n}\sum_{i=1}^{n}\sigma_i\right)$$

[10] The rate at which a new angle reading will be ready.

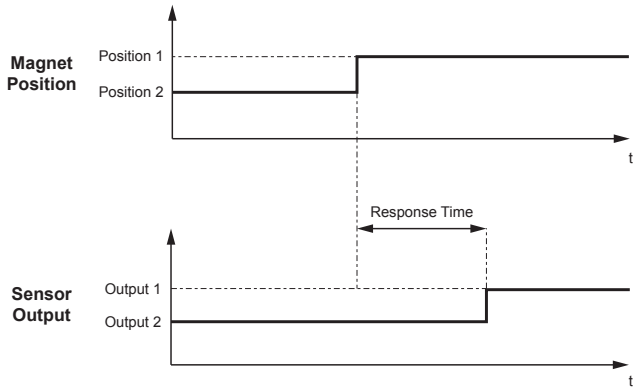


Figure 5: Definition of Response Time

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FUNCTIONAL DESCRIPTION

Overview

The A1338 is a rotary position Hall-sensor-based device. It incorporates up to two electrically independent Hall-based sensor dies in the same surface-mount package to provide solid-state consistency and reliability, and to support a wide variety of automotive applications. Each Hall-sensor-based die measures the direction of the magnetic field vector through 360° in the x-y plane (parallel to the branded face of the device) and computes an angle measurement based on the actual physical reading, as well as any internal configuration parameters that have been set by the user. The output of each die is used by the host microcontroller to provide a single channel of target data.

This device is an advanced, programmable system-on-chip (SoC). Each integrated circuit includes a circular vertical Hall (CVH) analog frontend, a high-speed sampling A-to-D converter, digital filtering, digital signal processing, and an SPI, SENT, or PWM output of the processed angle data.

Angle Measurement

The A1338 can monitor the angular position of a rotating magnet at speeds ranging from 0 to more than 7600 rpm. At lower rotational speeds, the A1338 is able to measure angle data with minimal angular latency between the actual magnet and sensor output. As the rpm increases, the angular latency between the magnet and sensor output also increases. Above 7600 rpm, the A1338 continues to provide angle data; however, the accuracy is proportionally reduced.

The A1338 can be configured to operate in two angular measurement modes of operation: Low RPM mode, and High RPM mode. Low RPM mode allows a programmable number of internal angle samples to be accumulated and averaged, providing greater resolution while reducing the update rate. This is suitable for lower rpm applications (0 to ≈500 rpm). For high-speed applications, the averaging function may be bypassed by operating in High RPM mode.

The actual update rate of Low RPM mode can be changed by setting the AVERAGING bits in the EEPROM (see the appendix *Programming Reference* for details). Table 1 describes the different levels of averaging available in Low RPM mode. A setting of 000_2 is equivalent to High RPM mode.

Table 1: Refresh Rate Based on Quantity of Samples Averaged

AVG [2:0]	Quantity of Samples Averaged	Refresh Rate (µs)
000	1	25
001	2	50
010	4	100
011	8	200
100	16	400
101	32	800
110	64	1600
111	128	3200

The A1338 has a typical output bandwidth of 40 kHz (25 µs refresh rate) in High RPM mode. In High RPM mode, a new angle measurement is available at the internal angle output register to be transmitted over the SPI/SENT or PWM output ports every 25 µs. There is a latency of 60 µs from when there is a change in the position of the target magnet field to when the new representative angle is updated in the internal angle output register. This latency effectively represents the age of the angle measurement.

Impact of High-Speed Sensing

Due to signal path latency, the angle information is delayed by $t_{RESPONSE}$. This delay equates to a greater angle value as the rotational velocity increases (i.e. a magnet rotating at 20,000 rpm traverses twice as much angular distance in a fixed time period as a magnet rotating at 10,000 rpm), and is referred to as angular lag.

The lag is directly proportional to rpm, and may be compensated for externally, if the velocity is known.

Angular lag can be expressed using the following equation:

$$Angle_Lag = (rpm \times 6) / (1^6 \times t_{RESPONSE}) \quad (1)$$

where rpm represents the rotational velocity of the magnet, Angle_lag is expressed in degrees, and $t_{RESPONSE}$ is in µs.

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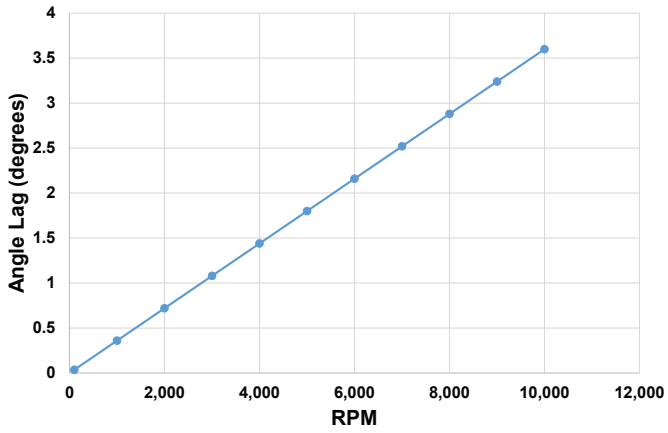


Figure 6: Angle Lag versus RPM, 60 µs Response Time

Angle Resolution and Representation

In addition to using the internal averaging of the sensor, angle resolution is also dependent on the intensity (B, in gauss) of the applied magnetic field from the target. At lower intensities, a reduced signal-to-noise ratio will cause one or two LSBs to change state randomly due to noise. These factors work together, so when High RPM mode is selected, the effective range of resolution is 8 to 10 bits (from lower to higher field intensities), and in Low RPM mode, the effective range is 11 to 12 bits, depending on field strength and AVG selection.

Regardless of the field intensity and mode selection, the transmission protocol and number formatting remains the same. The MSB is always transmitted first. The entire number should be read.

The Output Angle is always calculated at maximum resolution. To be more explicit, when reading the digital angle value:

$$Angle_{OUT} = 360\ (°) \times D[12:0] / (2^{13}) \qquad (2)$$

This formula is always true, regardless of the applied field intensity. What changes with the field and speed setting is how "quiet" the LSBs of the measurement data (D 12:*x*) will be.

It should be noted that the secondary die (E2) is rotated 180° relative to the primary die (E1). This results in a difference in measurement of approximately 180° between the two dies, given perfect alignment of each die to the target magnet.

This phenomenon can be counteracted by subtracting the offset using a microprocessor. Alternatively, the difference between the two dies can be compensated for using the EEPROM for setting the Reference Angle.

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Programing Modes

The EEPROM can be programmed through the dedicated SPI interface pins or via Manchester encoding on the VCC pin, allowing process coefficients to be entered and options selected. (Note: programming EEPROM also requires the VCC line to be pulsed, which could adversely affect other devices if powered from the same line). The EEPROM provides persistent storage at end of line for final parameters.

SPI System-Level Timing

The A1338 outputs a new angle measurement every t_{ANG} µs. In High RPM mode, the A1338 outputs a new angle measurement every t_{ANG} µs, with an effective resolution of 10 bits. There is, however, a latency of t_{LAT}, from when the rotating magnet is sampled by the CVH to when the sampled data has been completely transmitted over the SPI interface. Because an SPI interface Read command is not synchronous with the CVH timing, but instead is polled by the external host microcontroller, the latency can vary. For single back-to-back SPI transactions (first transaction is sending the Read register 0x0 command, second is retrieving the angle data) the following scenarios are possible:

- Worst case: 2 CVH cycle + 2 SPI cycles
- Best case: 1.5 SPI cycles; 2 µs, assuming a 10 MHz SPI clock

Power-Up

Upon applying power to the A1338, the device automatically runs through an initialization routine. The purpose of this initialization is to ensure that the device comes up in the same predictable operating condition every power cycle. This initialization routine takes a finite amount of time to complete, which is referred to as Power-On Time, t_{PO}.

The A1338 wakes up in a default state that sets all SPI registers to their default value. It is important to note that, regardless of the state of the device before a power cycle, the device will re-power with default values. For example, on every power-up, the device will power up in the mode set in the EEPROM bit RPM. The state of the EEPROM is unchanged.

PWM Output (“-P-” option)

The A1338LLETR-P-DD-T and A1338LLETR-P-T options provide a pulse-width-modulated output with duty cycle proportional to the measured angle. The PWM duty cycle ranges between 5% (corresponding to 0° angle) and 95% (corresponding to 360° angle). The 0% and 100% (Pulled Low and Pulled High) states are reserved for error condition notifications.

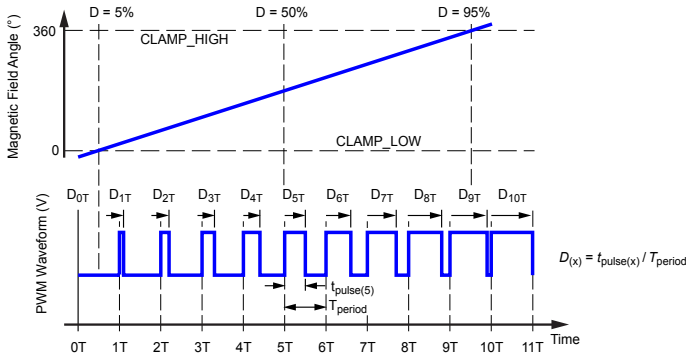


Figure 7: PWM mode outputs a duty-cycle-based waveform that can be read by the external controller as a cumulatively changing continuous voltage.

Within each cycle, the output is high for the first 5% of the period. The middle 90% of the period is a linear interpolation of the angle as samples at the beginning of the PWM period.

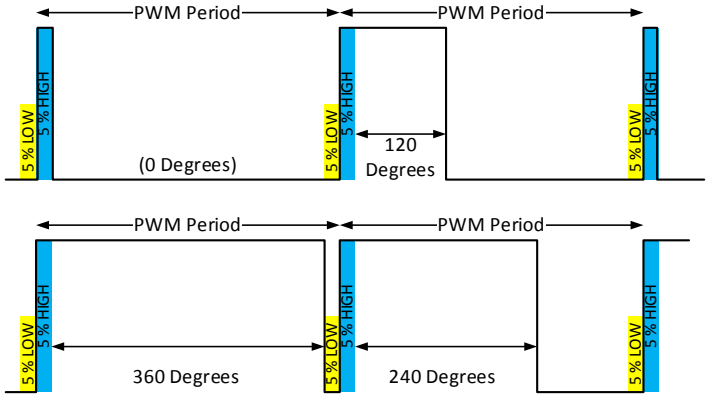


Figure 8: Pulse-Width Modulation (PWM) Examples

The angle is represented in 12-bit resolution and can never reach exactly 360°. The maximum duty cycle high period is:

$$\text{DutyCycleMax (\%)} = (4095 / 4096) \times 90 + 5 .$$

Error Reporting in PWM

The PWM output will tristate when any unmasked error is present (see ERR and ERR2 register descriptions). Error flags are masked via bits within EEPROM 0x1E.

By default, the BATD error mask is set in EEPROM for all PWM output ICs. This prevents the PWM output from tristating on power-on.

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MANCHESTER SERIAL INTERFACE

To facilitate addressable device programming when using the unidirectional SENT output mode with no need for additional wiring, the A1338 incorporates a serial interface on the VCC line. (Note: The A1338 may be programmed via the SPI interface, with additional wiring connections. For detailed information on part programming, refer to the A1338 programming manual). This interface allows an external controller to read and write registers in the A1338 EEPROM and volatile memory. The device uses a point-to-point communication protocol, based on Manchester encoding per G.E. Thomas (a rising edge indicates a 0 and a falling edge indicates a 1), with address and data transmitted MSB first. The addressable Manchester code implementation uses the logic states of the SA0 (SPI $\overline{CS}$ pin) / SA1 (SPI SCLK pin) to set address values for each die. In this way, individual communication with up to four A1338 dies is possible.

To prevent any undesired programming of the A1338, the serial interface can be disabled by setting the Disable Manchester bit (0x19 bit 18) to a 1. With this bit set, the A1338 will ignore any Manchester input on VCC.

Entering Manchester Communication Mode

Provided the Disable Manchester bit is not set in EEPROM, the A1338 continuously monitors the VCC line for valid Manchester commands. The part takes no action until a valid Manchester Access Code is received.

There are two special Manchester code commands used to activate or deactivate the serial interface and specify the output format used during Read operations:

1. **Manchester Access Code:** Enters Manchester Communication Mode; Manchester code output on the SENT pin.
2. **Manchester Exit Code:** Returns the SENT pin to normal (angle data) output format.

Once the Manchester Communication Mode is entered, the SENT output pin will cease providing angle data, interrupting any data transmission in progress.

Transaction Types

As shown in Figure 9, the A1338 receives all commands via the VCC pin, and responds to Read commands via the SENT pin. This implementation of Manchester encoding requires the communication pulses be within a high ($V_{MAN(H)}$) and low ($V_{MAN(L)}$) range of voltages on the VCC line. Writing to EEPROM is supported by two high-voltage pulses on the VCC line.

Each transaction is initiated by a command from the controller; the A1338 does not initiate any transactions. Two commands are recognized by the A1338: Write and Read.

Writing to EEPROM

When a Write command requires writing to non-volatile EEPROM, after the Write command, the controller must also send two *Programming pulses*, high-voltage strobes via the VCC pin. These strobes are detected internally, allowing the A1338 to boost the voltage on the EEPROM gates. Refer to the programming manual for specifics on sensor programming and protocol details.

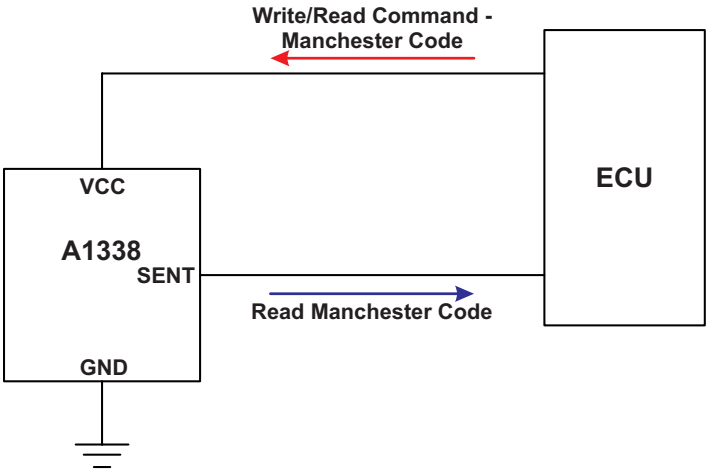


Figure 9: Top-Level Programming Interface

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Manchester Interface Reference

Table 2: Manchester Interface Protocol Characteristics [1]

Characteristics	Symbol	Note	Min.	Typ.	Max.	Unit
INPUT/OUTPUT SIGNAL TIMING						
Bit Rate		Defined by the input message bit rate sent from the external controller	4	–	50	kbps
Bit Time	t_{BIT}	Data bit pulse width at 4 kbps	243	250	257	µs
		Data bit pulse width at 100 kbps	9.5	10	10.5	µs
Bit Time Error	err_{TBIT}	Deviation in t_{BIT} during one command frame	–11	–	+11	%
Write Delay	$t_{WRITE(E)}$	Required delay from the end of the second EEPROM Program pulse to the leading edge of a following command frame	V_{CC} < 6.0 V	–	–	–
Read Delay	t_{START_READ}	Delay from the trailing edge of a Read command frame to the leading edge of the Read Acknowledge frame	¼ × t_{bit}	–	¾ × t_{bit}	µs
EEPROM PROGRAMMING PULSE						
EEPROM Programming Pulse Setup Time	$t_{sPULSE(E)}$	Delay from last bit cell of write command to start of EEPROM programming pulse	40	–	–	µs
Pulse High Time	$t_{PULSE(H)}$	Time above minimum pulse voltage	8	10	11	ms
Rise Time	t_r	10% to 90% of minimum pulse level	300	–	–	µs
Fall Time	t_f	10% to 90% of minimum pulse level	60	–	–	µs
Pulse Voltage	V_{PULSE}	Applied on VCC Line	18	19	19.5	V
Separation Time	$t_{PULSE(f-r)}$	Timing between first pulse dropping below 6 V and 2nd pulse rising above 6 V	0.002	–	50	ms
INPUT SIGNAL VOLTAGE						
Manchester Code High Voltage	$V_{MAN(H)}$	Applied to VCC line	7.8	–	–	V
Manchester Code Low Voltage	$V_{MAN(L)}$	Applied to VCC line	–	–	6.3	V
OUTPUT SIGNAL VOLTAGE (APPLIED ON SENT LINE)						
Manchester Code High Voltage	$V_{MAN(H)}$	Minimum R_{pullup} = 5 kΩ	0.9 × V_S	–	–	V
		Maximum R_{pullup} = 50 kΩ	0.7 × V_S	–	–	V
Manchester Code Low Voltage	$V_{MAN(L)}$	5 kΩ ≤ R_{pullup} ≤ 50 kΩ	–	–	0.2	V

[1] Determined by design.

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SENT Output Mode

(A1338LLETR-DD-T, A1338LLETR-T options)

The SENT output converts the measured magnetic field angle to a binary value mapped to the Full-Scale Output (FSO) range of 0 to 4095, shown in Figure 10. This data is inserted into a binary pulse message, referred to as a frame, that conforms to the SENT data transmission specification (SAEJ2716 JAN2010).

The SENT frame may be configured via EEPROM. The A1338 may operate in one of three broadly defined SENT modes (see the A1337/8 Programming Manual for details on SENT modes and settings).

- SAE J2716 SENT: Free-streaming SENT frame in accordance with industry specification.
- Triggered SENT (TSENT): User-defined sampling and retrieval.
- Shared SENT: Allows multiple devices to share a common SENT line. Devices may either be directly addressed (Addressable SENT or ASENT) or sequentially polled (Sequential SENT or SSENT).

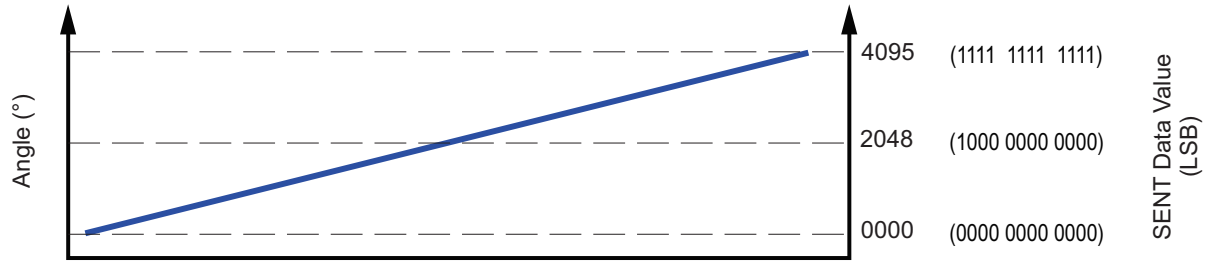


Figure 10: Angle is represented as a 12-bit digital value.

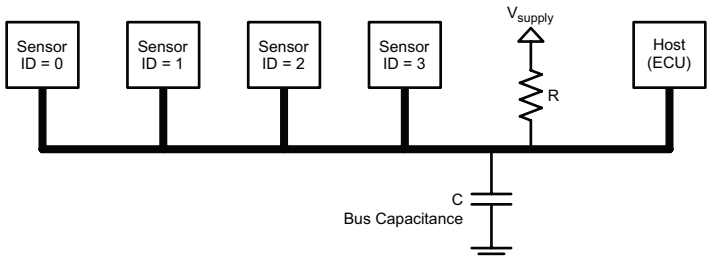


Figure 11: Allegro's proprietary SENT protocol allows multiple parts to share one common output bus.

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SENT MESSAGE STRUCTURE

Data within a SENT message frame is represented as a series of nibbles, with the following characteristics:

- Each nibble is an ordered pair of a low-voltage interval followed by a high-voltage interval.
- The low-voltage interval acts as the delimiting state which acts as a boundary between each nibble. The length of this low-voltage interval is fixed at 5 ticks.
- The high-voltage interval performs the job of the information state and is variable in duration in order to contain the data payload of the nibble.
- The slew rate of the falling edge may be adjusted using the C_SENT_DRIVE parameter.

The duration of a nibble is denominated in ticks. The period of a tick is set by the C_TICK_TIME parameter. The duration of the nibble is the sum of the low-voltage interval plus the high-voltage interval.

The parts of a SENT message are arranged in the following required sequence (see Figure 13):

1. **Synchronization and Calibration:** Flags the start of the SENT message.
2. **Status and Communication Nibble:** Provides A1338 status and the optional serial data determined by the setting of the SENT_SERIAL parameter.
3. **Data:** Angle information and optional data.
4. **CRC:** Error checking.
5. **Pause Pulse (optional):** Fill pulse between SENT message frames.

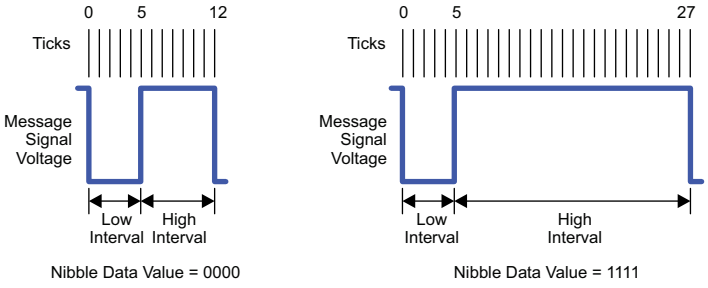


Figure 12: General Value Formation for SENT

0000 (left), 1111 (right)

Table 3: Nibble Composition and Value

Quantity of Ticks			Binary (4-bit) Value	Decimal Equivalent Value
Low-Voltage Interval	High-Voltage Interval	Total		
5	7	12	0000	0
5	8	13	0001	1
5	9	14	0002	2
⋮	⋮	⋮	⋮	⋮
5	21	26	1110	14
5	22	27	1111	15

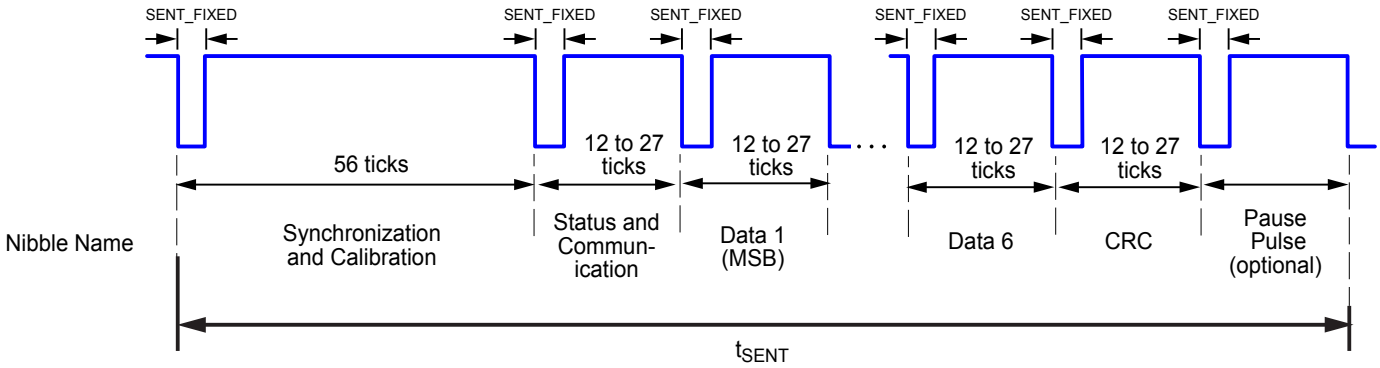


Figure 13: General Format for SENT Message Frame

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Table 4: EEPROM Registers Map Table with Defaults (Factory-Reserved Registers Not Shown) [1]

EADR	State	Bits																							
		23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x17	SENT_CFG	ZS	SS	SM	PO	IS	RES	SCN_MODE			DATA_MODE			SENT_MODE			TICK_TIME						SENT_DRIVE		
0x18	CUST_CFG1	RES			CIS	DA	MAXID		NS	FA	u_int_st		pw_up_st		MISSING_MAG_THRESHOLD										
0x19	CUST_CFG2	LOCK	RES	PWM_F		RES	MAND	SCRC	RPMD	AVERAGE			POL	ANGLE_OFFSET											
0x1E	ERM	RES									MAN2	MAN	UV	LBST	CVHST	GOVF	AH	AL	EU	ES	TR	TRNO	IE	MAGM	BATD
0x1F	CUST2	CUST_EEP																							

[1] For more details, see Programming Manual.

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Diagnostics

The A1338 was designed with ISO 26262:2011 requirements in mind and supports a number of on-chip self diagnostics to enable the host microcontroller to assess the operational status of each die. For example, each die can be user-configured for logic built-in self-test (LBIST) evaluation to ensure the digital circuits are operational. Upon completion of an LBIST operation, the A1338 will set a pass/fail LBIST status flag in the device error (ERR) register.

Each A1338 die also supports several diagnostic features and status flags, accessible via a SPI read of the ERR register, to let the user know if any issues are present with the A1338 or associated magnetic system, as shown in Table 5.

In addition, each die on the A1338 supports an on-chip user-initiated diagnostic (CVH Self-Test) mode that tests the entire signal path, including the front end CVH sensing circuitry.

USER-INITIATED DIAGNOSTICS

Each die on the A1338 can independently be controlled by a microcontroller to enter its CVH Self-Test mode via SPI or SENT.

When a CVH Self-Test mode operation is requested by the microcontroller, the respective die initiates a test mode sequence whereby it sequentially applies an internal constant bias current to every contact element in the CVH ring. As each element in the CVH ring is sequentially biased, an angle measurement is calculated.

The time to complete one revolution around the CVH ring and calculate and store incremental angle measurements is t_{CVHST}.

Table 5: Diagnostic Capabilities

Diagnostic/ Protection	Description	Output State
Loss of V_{CC}	Determine if battery power was lost.	BATD Error flag is set; see ERR register table.
Reverse V_{CC} Condition	Current Limiting (VCCx pin).	Output Below GND.
MISO/SENT/PWM Short to VCC	Current Limiting (MISOx pin).	MISO/SENT/PWM Line: Pulled up to V-pullup. Should not be tied to VCC if V_{CC} > 5.5 V.
MISO/SENT/PWM Short to Ground	Current Limiting (MISOx pin).	MISO/SENT/PWM Line: Pulled up to GND.
Logic Built-In Self-Test (LBIST)	70% coverage for 10 ms BIST of all digital circuitry.	Error Flags set in SPI message when errors are detected; see ERR2 Register table.
Signal Path Diagnostics	User controlled advanced CVH and full signal path diagnostics.	Error Flags set in SPI message when errors are detected; see ERR2 Register table.
Internal Error	Monitors digital logic for proper function.	IERR Error flag is set; see ERR Register table.
Missing Magnet	Monitors magnet field level in case of mechanical failure.	MAGM Error flag is set; see ERR Register table.
EEPROM Error Detection and Correction	Detection of single and dual bit error, and correction of single bit error.	Error flags set in SPI message when errors are detected or corrected; see ERR Register table.
V_{CC} Low Flag	Asserted when $V_{CC} < V_{UVLOTH}$.	Bit 2 of SPI Output on MISO is set high. See Programming manual for more details.
Temperature Out of Range	Die temperature has exceeded acceptable range.	See ERR Register table for more details.
Redundancy	Dual-die version of the A1338 provides redundant sensors in the same package.	

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SERIAL INTERFACE STRUCTURE

The serial interface contains the Primary Serial Interface (PSI) registers and the restricted Extended Addressing registers. The PSI fields are used by the host for routine communication with the A1338, such as retrieving current angle and turns count, error, and status data, and managing certain configuration settings. For information on extended addressing and EEPROM access, see the A1338 programming manual.

Table 6: Primary Serial Interface Registers (Reserved Registers Not Shown)

Address (Hex)	Name (Symbol)	Usage
0x00	Angle Output (ANG)	Read out current angle (Note: 12-bit Angle Output located MSB first, in bits12:1; Bit0 is always '0')
0x04	Error (ERR1)	Read out error flags
0x05	Error (ERR2)	Read out error flags
0x08	Control (CTRL)	Read or write configuration commands
0x0F	Key Code (KEY)	Write the Key Code to enable access to Extended Addressing registers

Table 7: Primary Serial Interface Registers Bits Map (Reserved Registers Not Shown)

Serial Address	Register Symbol	Addressed Byte (MSB)												
		12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	ANG	ANGLE OUTPUT (12:1)												0
0x04	ERR	–	–	–	–	–	–	EEP2	EEP1	TMP	RES	IERR	MAGM	BATD
0X05	ERR2	–	–	–	–	–	–	MANER	RES3	LBIST	CVHST	RES2	RES1	RES0
0x08	CTRL	–	–	–	–	–	–	–	–	STS	TRST	RPM	TEN	ERST
0x0F	KEY	–	–	–	–	–	KEY_CODE							

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ANG (Angle Output) Register
Address: 0x00

Address	0x00												
Bit	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ANGLE_OUTPUT												–
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R
Value	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0

Stores data on current angle reading.

ANGLE_OUTPUT [12:1] Current Angle

Most recent angle reading. Value is unsigned, stored in bits 12:1 (bit 0 defaults to 0). As the target turns, the angle value increases or decreases according to the rotational polarity setting in EEPROM (CUST_CFG2 register, POL bit).

Bit	Value	Description
12:1	0/1	Current angle reading.

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ERR (Error) Register
Address: 0x04

Address	0x04												
Bit	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	–	–	–	–	–	–	EEP2	EEP1	TMP	RES	IERR	MAGM	BATD
R/W	–	–	–	–	–	–	R	R	R	R	R	R	R
Value	X	X	X	X	X	X	0/1	0/1	0/1	0/1	0/1	0/1	0/1
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1

Error register. Indicates various current error conditions. When set, can only be cleared via the CTRL register ERST field, hard reset, or power-on reset (see BATD for exception). If any of the error bits are asserted, the error flag on the serial interface will be asserted. Masking an error bit will prevent the bit from asserting the serial interface error flag, but the error bit may still be asserted in this register.

EEP2 [6] EEPROM Error Flag 2

Uncorrectable dual-bit EEPROM error flag.

Bit	Value	Description
6	0	Error condition not present.
	1	Error condition present.

EEP1 [5] EEPROM Error Flag 1

Corrected single-bit EEPROM error flag.

Bit	Value	Description
5	0	Error condition not present.
	1	Error condition present.

TMP [4] Temperature Out of Range

This bit indicates an error condition when the die temperature has exceeded the acceptable range.

Bit	Value	Description
4	0	Error condition not present.
	1	Error condition present.

RES [3] Reserved

IERR [2] Internal Error

This bit is set to 1 if an internal logic error condition has been detected. When this bit is set to 1, a general reset is recommended.

Bit	Value	Description
2	0	No digital logic timer error has been detected.
	1	Digital logic timer error has been detected.

MAGM [1] Target Magnet Loss

Monitors target magnet field level to detect field loss due to mechanical failure in the application. Missing Magnet Field Threshold can be customer programmed by writing to EEPROM Address 0x18, Bits 10:0 (MISSING_MAG_THRESHOLD). Allegro programs this to a default value of 100 G, but the customer can readjust this field if they prefer.

Bit	Value	Description
1	0	Error condition not present.
	1	Error condition present.

BATD [0] Power Supply Loss

Indicates if battery power (VCC supply) was lost. By default also indicates at expected low power events: start-up, power-on reset, and after exiting Transport mode. Before commencing normal operation, must be set to 0 by asserting the ERST bit of the CTRL register (unless field is masked in EEPROM by ERM register BATD field).

Bit	Value	Description
0	0	Error condition not present.
	1	Error condition present.

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ERR2 (Error2) Register
Address: 0x05

Address	0x05												
Bit	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	–	–	–	–	–	–	MANER	RES3	LBIST	CVHST	RES2	RES1	RES0
R/W	–	–	–	–	–	–	R	–	R	R	–	R	R
Value	X	X	X	X	X	X	0/1	–	0/1	0/1	–	0/1	0/1
Reset	0	0	0	0	0	0	0	–	0	0	–	0	1

Error register. Indicates various current error conditions. When set, can only be cleared via the CTRL register ERST field, hard reset, or power-on reset (see BATD for exception). If any of the error bits are asserted, the error flag on the serial interface will be asserted. Masking an error bit will prevent the bit from asserting the serial interface error flag, but the error bit may still be asserted in this register.

MANER [6] Manchester/SENT Error Flag

Indicates Manchester/SENT Error.

Bit	Value	Description
6	0	Error condition not present.
	1	Error condition present.

RES3 [5] Factory Reserved Bit

LBIST [4] LBIST Error Flag

This bit indicates that the Logic Built-In Self-Test (LBIST) failed.

Bit	Value	Description
4	0	Error condition not present.
	1	Error condition present.

CVHST [3] Circular Vertical Hall Self-Test

This bit indicates that the CVH Built-In Self-Test (CVHST) failed.

Bit	Value	Description
3	0	Error condition not present.
	1	Error condition present.

RES2 [2] Factory Reserved Bit

RES1 [1] Factory Reserved Bit

RES0 [0] Factory Reserved Bit

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CTRL (Control) Register

Address: 0x08

Address	0x08							
Bit	7	6	5	4	3	2	1	0
Name	–	–	–	STST	RES1	RPM	RES0	ERST
R/W	–	–	–	RW1C	–	R/W	R/W	RW1C
Value	X	X	X	X	X	0/1	0/1	0/1
Reset	0	0	0	0	0	0	0	0

Initialization and operation configuration control command settings.
RW1C: When a 1 is written to the field, the command is immediately executed, and the value returns to zero. When Reading the field, this type of field will always read back 0.

STS [4] Self-Test Start

Commands the A1338 to begin Self-Test(s).

Which self-test is run, is determined by the U_INIT_ST field within EEPROM. There are two self-tests:

1. Logic Built-In Self-Test (LBIST): Verifies digital gate integrity. This is a modified version of digital scan testing. Requires approximately 10 ms to run during which time no angle readings can take place

2. CVH Self-Test: Test of the front end transducer and signal path. Requires approximately 40 ms to compete, during which time angle readings are not available.

Bit	Value	Description
4	0	Does not trigger Self-Test.
	1	Self-Test is triggered based on pre-selected options in the “U_INIT_ST” field of EEPROM.

RES1 [3] Reserved

RPM [2] RPM Operating Mode (see Programming Manual)

This field is populated on power-up by the EEPROM field RPMD. This field can be written during operation to temporarily override the EEPROM. On the next power cycle, this field will reset to the value determined by the EEPROM field RPMD. This bit must be a ‘1’ to enable internal averaging.

Bit	Value	Description
2	0	Internal Averaging not allowed.
	1	Internal Averaging allowed.

RES0 [1] Reserved

ERST [0] Error Flags Reset

A feature to clear the values in the ERR register (0x04).

Bit	Value	Description
0	0	ERR register not cleared.
	1	ERR register cleared.

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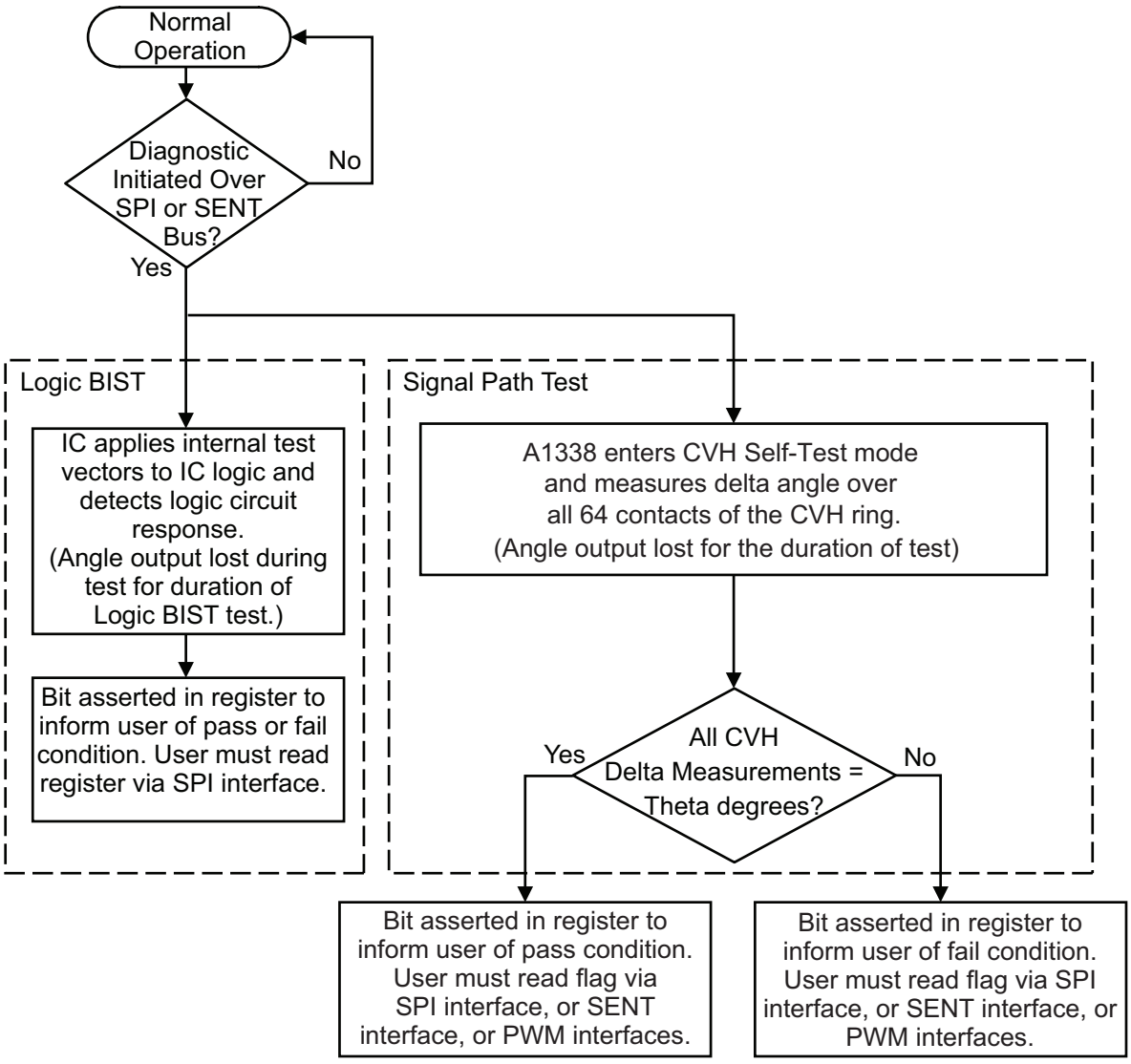


Figure 14: User-Interface Diagnostic Diagram

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APPLICATION INFORMATION

Serial Interface Description

The A1338 features SPI, SENT, and PWM interfaces. The following figures show some typical application circuits for using the A1338 with these interfaces.

Calculating Target Zero-Degree Angle

When shipped from the factory, the default angle value when oriented as shown in Figure 15, is approximately 21° (201° on the second die). In some cases, the end user may want to program an angle offset in the A1338 to compensate for variation in magnetic assemblies, or for applications where absolute system level readings are required.

The internal algorithm for computing the output angle is as follows:

$$Angle_{OUT} = Angle_{RAW} - Reference\ Angle\ . \quad (3)$$

The procedure to "zero out" the A1338 is quite simple. During final application calibration and programming, position the magnet above the A1338 in the required zero-degree position, and read the angle from the A1338 using the SPI interface ($Angle_{OUT}$). From this angle, the Reference Angle required to program the A1338 can be computed as follows:

$$Reference\ Angle = Angle_{OUT}\ . \quad (4)$$

Bypass Pins Usage

The bypass pins are required for proper operation of the device. A 0.1 µF capacitor should be placed in very close proximity to each of the bypass pins.

When using the SPI communication protocol, the A1338 has the ability to support host microcontroller inputs with Voltage Input High (V_{IH}) thresholds of 2 V (minimum). This option only requires BYP1 to be populated with a 0.1 µF capacitor.

By using an optional second bypass capacitor on the BYP2 pins, the A1338 can also support host microcontroller inputs with Voltage Input High (V_{IH}) thresholds of 2.5 V (minimum). This option requires that both BYP1 and BYP2 pins be populated with 0.1 µF

Target alignment for default angle setting
• Target rotation axis intersects primary die
  • Sets primary die 21° default point
  • Sets secondary die 201° default point
(Example shows element E1 as primary die element E2 as secondary die)

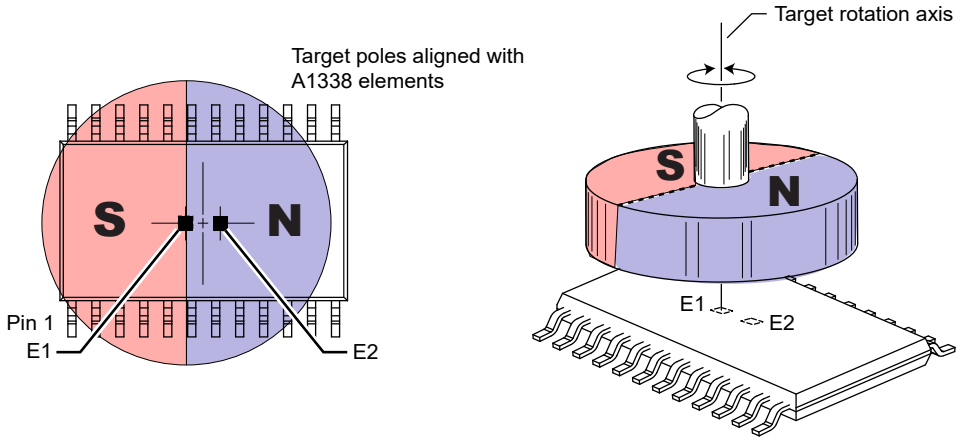


Figure 15: Orientation of Magnet Relative to Primary and Secondary Die

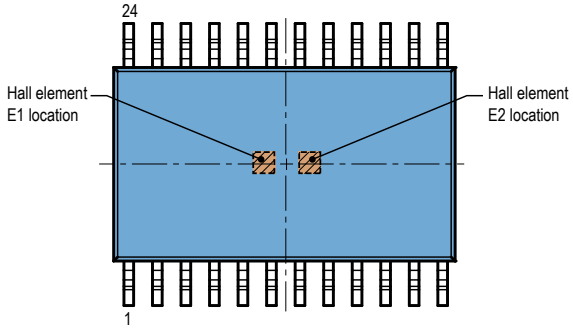


Figure 16: Hall Element Located Off-Center within the Device Body

(refer to the Package Outline Drawing for reference dimensions)

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capacitors, and that the appropriate EEPROM configuration bit be enabled. Contact Allegro for availability of parts with elevated SPI output levels.

The bypass pins are not intended to be used to source external components. To assist with PCB layout, see the Operating Characteristics table for output voltage and current requirements.

Changing Sampling Modes

The A1338 features a High RPM sampling mode and a Low RPM sampling mode. The default power-on state of the A1338 is loaded from EEPROM. To configure the A1338 to Low RPM mode, set the Operating mode to Low RPM mode by writing a logic 1 to bit 2 (RPM) of the configuration commands (CTRL) register, via the SPI interface.

Magnetic Target Requirements

The A1338 is designed to operate with magnets constructed with a variety of magnetic materials, cylindrical geometries, and field strengths, as shown in Table 8. Contact Allegro for more detailed information on magnet selection and theoretical error.

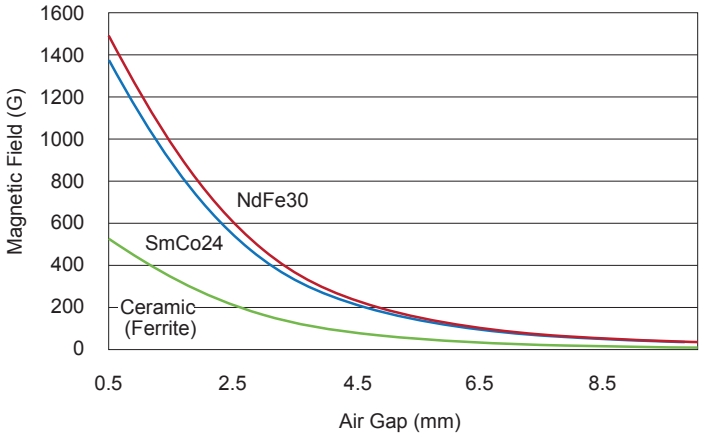
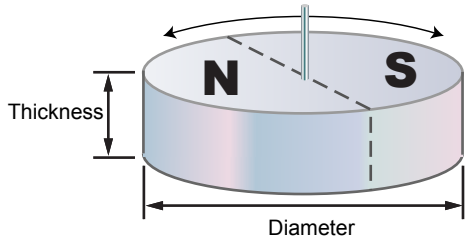


Figure 17: Magnetic Field versus Air Gap for a magnet 6 mm in diameter and 2.5 mm thick.

Allegro can provide similar curves for customer application magnets upon request. Larger magnets are recommended for applications that require optimized accuracy performance.

Table 8: Target Magnet Parameters

Magnetic Material	Diameter (mm)	Thickness (mm)
Neodymium (bonded)	15	4
Neodymium (sintered)*	10	2.5
Neodymium (sintered)	8	3
Neodymium / SmCo	6	2.5



*A sintered Neodymium magnet with 10 mm (or greater) diameter and 2.5 mm thickness is the recommended magnet for redundant applications.

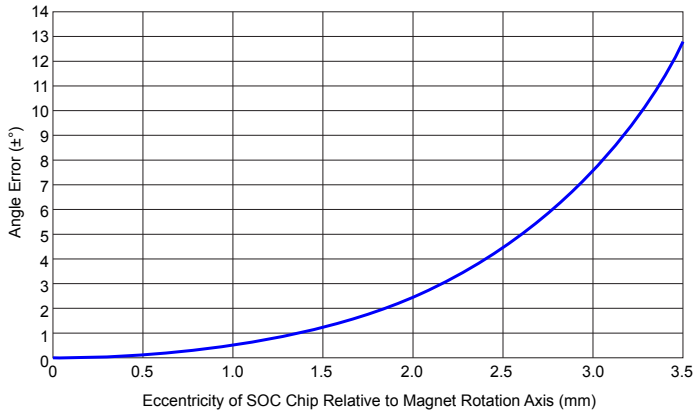


Figure 18: Angle Error versus Eccentricity

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Redundant Applications and Alignment Error

The A1338 is designed to be used in redundant, on-axis applications with a single magnet spinning over the two separate dies that are mounted side-by-side in the same package. One challenge with this configuration is correctly lining up the magnet with the device package, so it is important to be aware of the physical separation of the two dies.

Figure 19 illustrates the behavior of alignment error when using a Ø10 mm × 2.5 mm Neodymium magnet that is located 2.7 mm above the branded face of the package. The curve shows the relationship between absolute angle error present on the output of the die versus eccentricity of the die relative to the rotation axis of the magnet. The curve is the same for both dies in the package.

The curve provides guidance to determine what the optimal magnet placement should be for a given application. For example, given that the maximum spacing between the two dies is 1 mm, if the center of the magnet rotation is placed at the midpoint between the two dies, each die will have a maximum eccentricity of 0.5 mm.

For applications with reduced accuracy requirements, considering one die the primary and the other die the secondary, the magnet axis of rotation could be positioned directly above the primary die, and thus offset 1 mm from the secondary die, yielding zero alignment error on the primary die, and approximately ±1° of error on the secondary die, relative to the primary die, due to geometric mismatch.

System Timing and Error

The A1338 is a digital system, and therefore takes angle samples at a fixed sampling rate. When using a sensing device with a fixed sampling rate to sample a continuously moving target, there will be error introduced that can be simply calculated with the sampling rate of the device and the speed at which the magnetic signal is changing. In the case of the A1338, the input signal is rotating at various speeds, and the sampling rate of the A1338 is fixed at ANG. The calculation would be:

$$ANG\ (\mu s) \times angular\ velocity\ (^\circ/\mu s)\ . \qquad (5)$$

So the faster the magnetic object is spinning, the further behind in angle the output signal will seem for a fixed sampling rate.

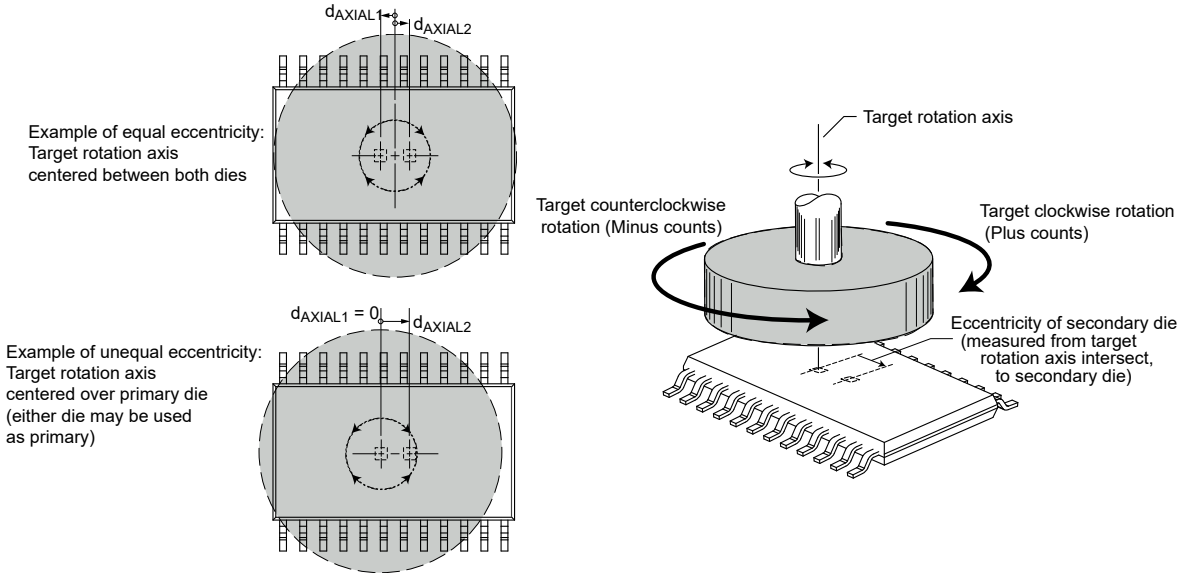


Figure 19: Demonstration of Magnet to Sensing Element Eccentricity

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CHARACTERISTIC PERFORMANCE DATA

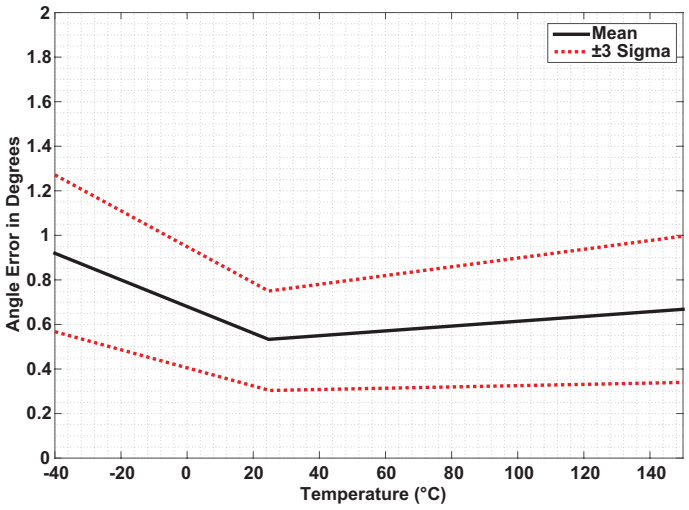


Figure 20: Angle Error over Temperature (300 G)

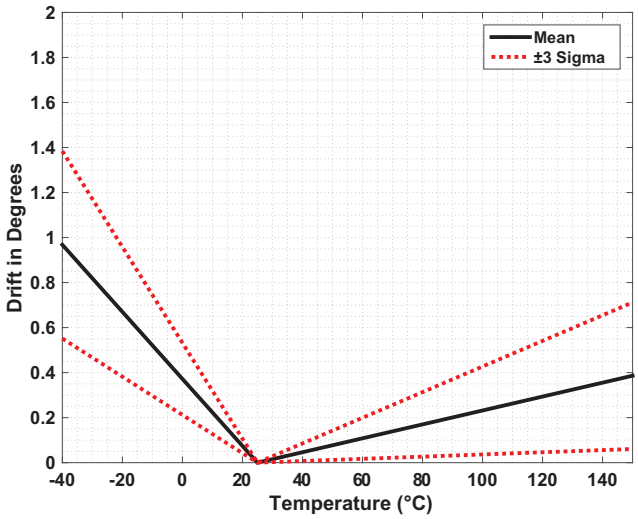


Figure 21: Angle Drift Relative to 25°C (300 G)

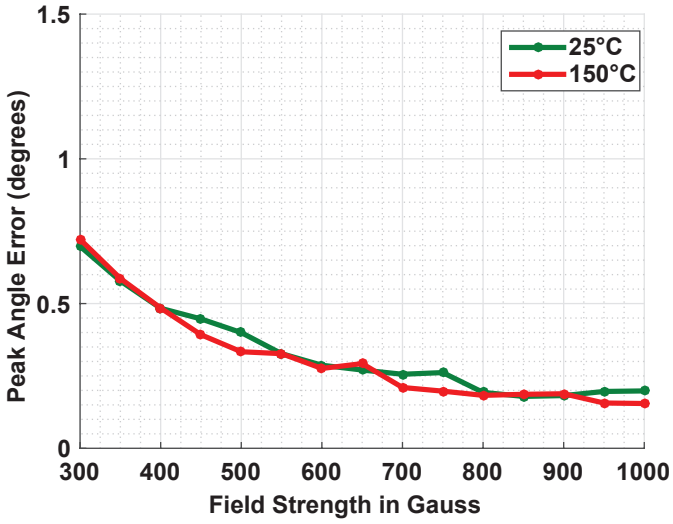


Figure 22: Angle Error over Field Strength

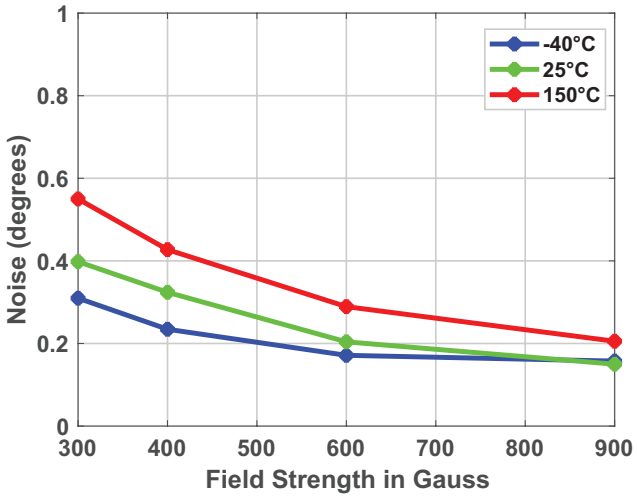


Figure 23: Typical Three Sigma Angle Noise Over Field Strength

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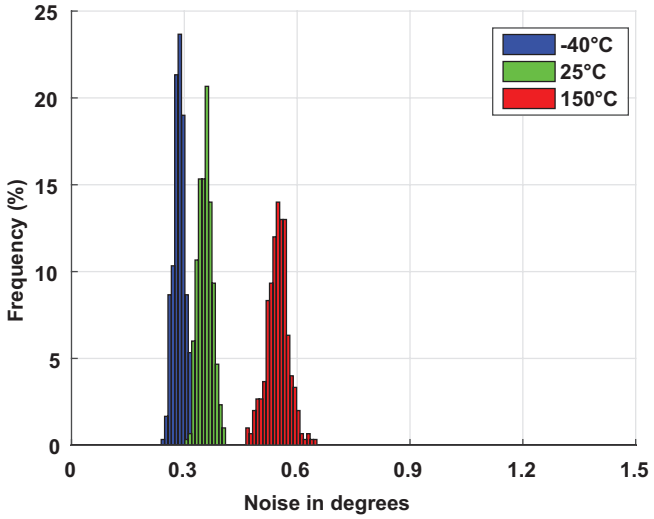


Figure 24: Noise Distribution over Temperature (3 σ, 300 G)

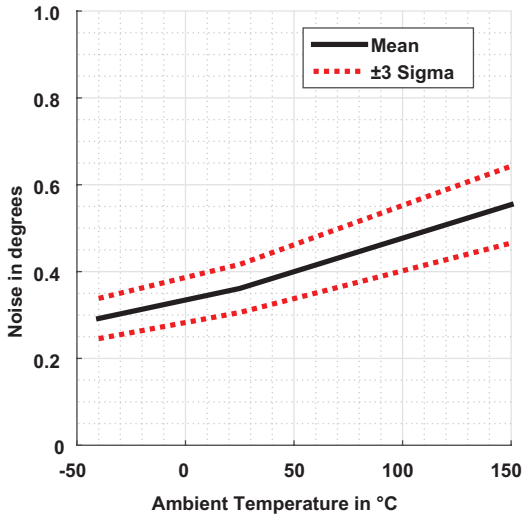


Figure 25: Noise Performance over Temperature (3 σ, 300 G)

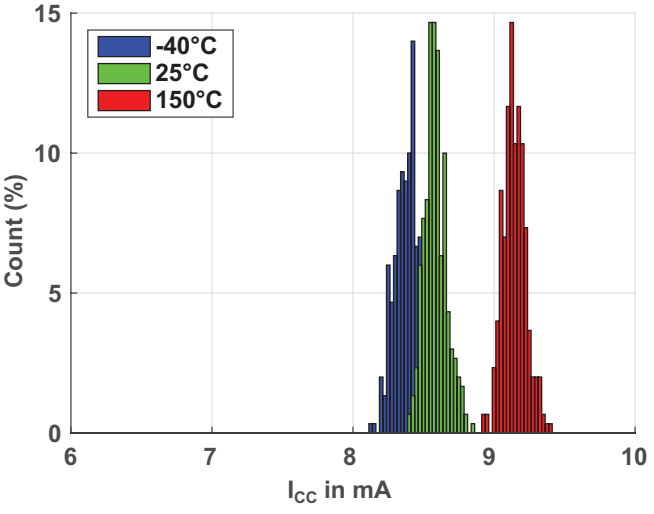


Figure 26: I_{CC} Distribution over Temperature (I_{CC} per die, V_{CC} = 3.7 V)

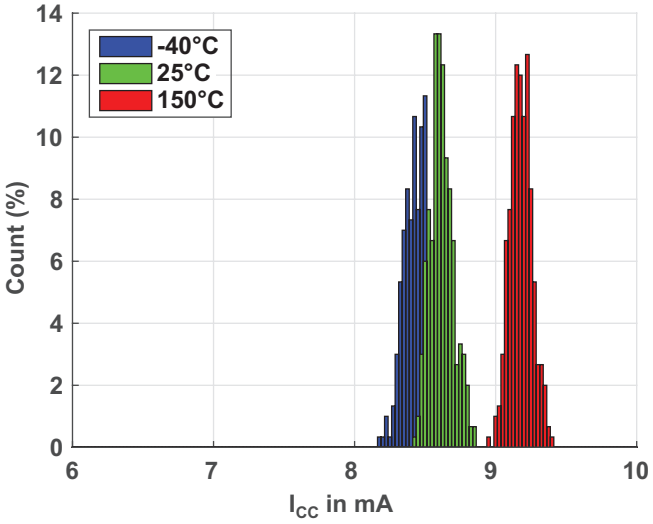


Figure 27: I_{CC} Distribution over Temperature (I_{CC} per die, V_{CC} = 16 V)

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EMC Reduction

For applications with stringent EMC requirements, a 100 Ω resistance should be added to the supply for the device in order to suppress noise. A recommended circuit is shown in Figure 28.

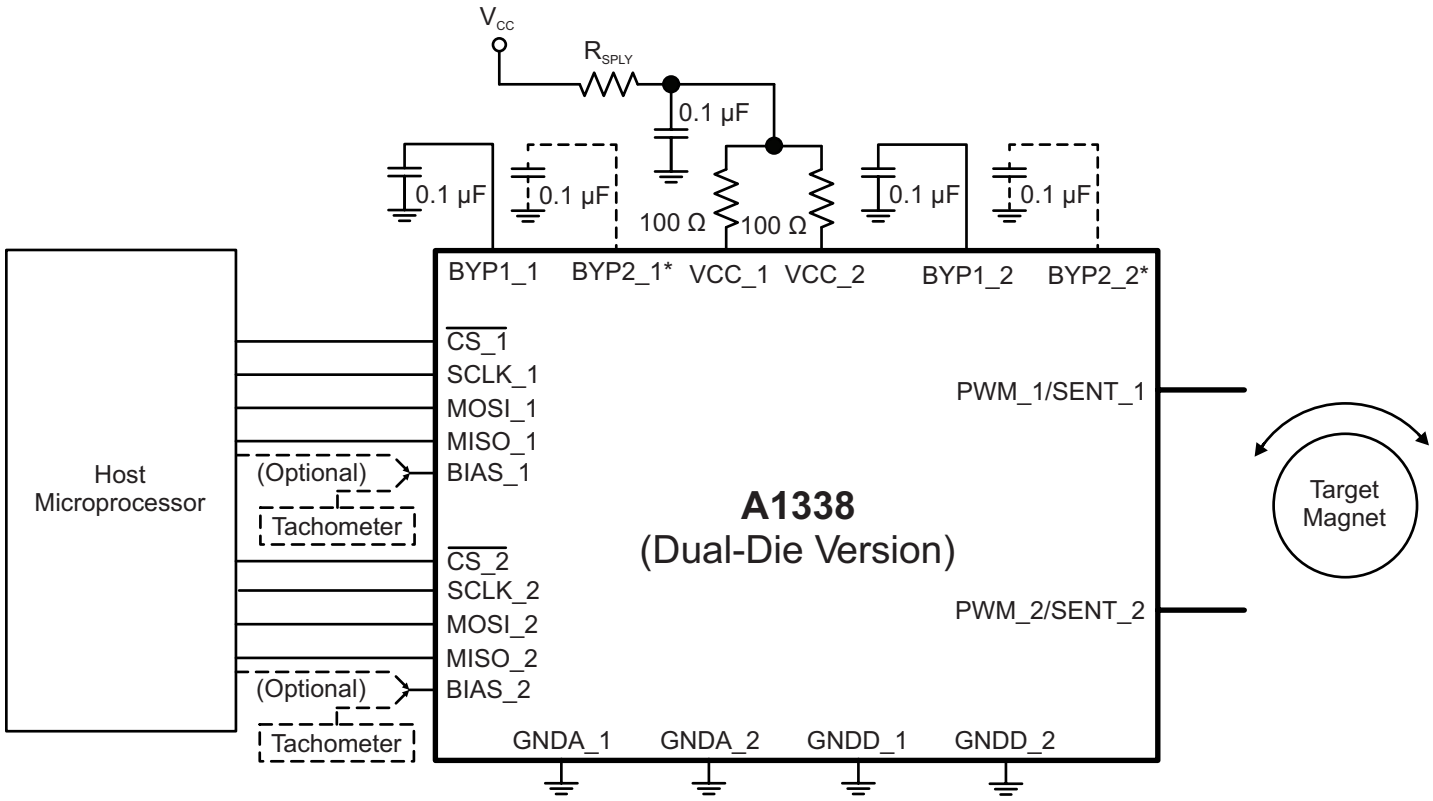


Figure 28: Typical application diagram (dual-die version) with EMC suppression resistor, R_{SPLY}, on supply line.
*Secondary bypass capacitors only required when using Elevated SPI Output Voltage. Contact Allegro for availability.

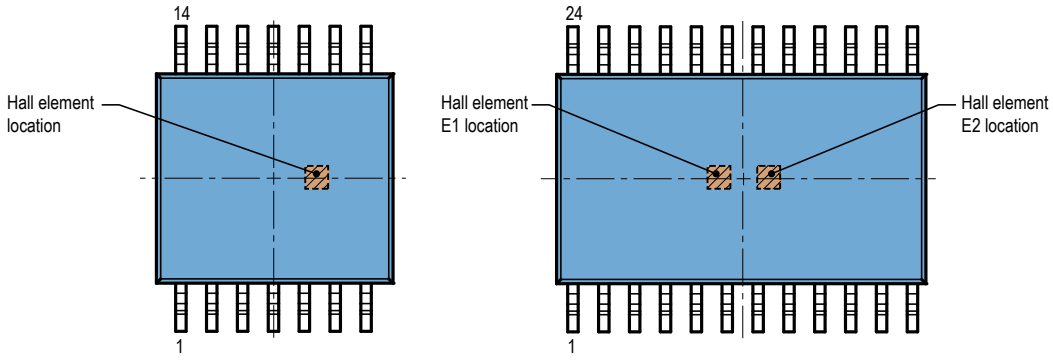


Figure 29: Hall element located off-center within the device body; refer to the Package Outline Drawing for reference dimensions

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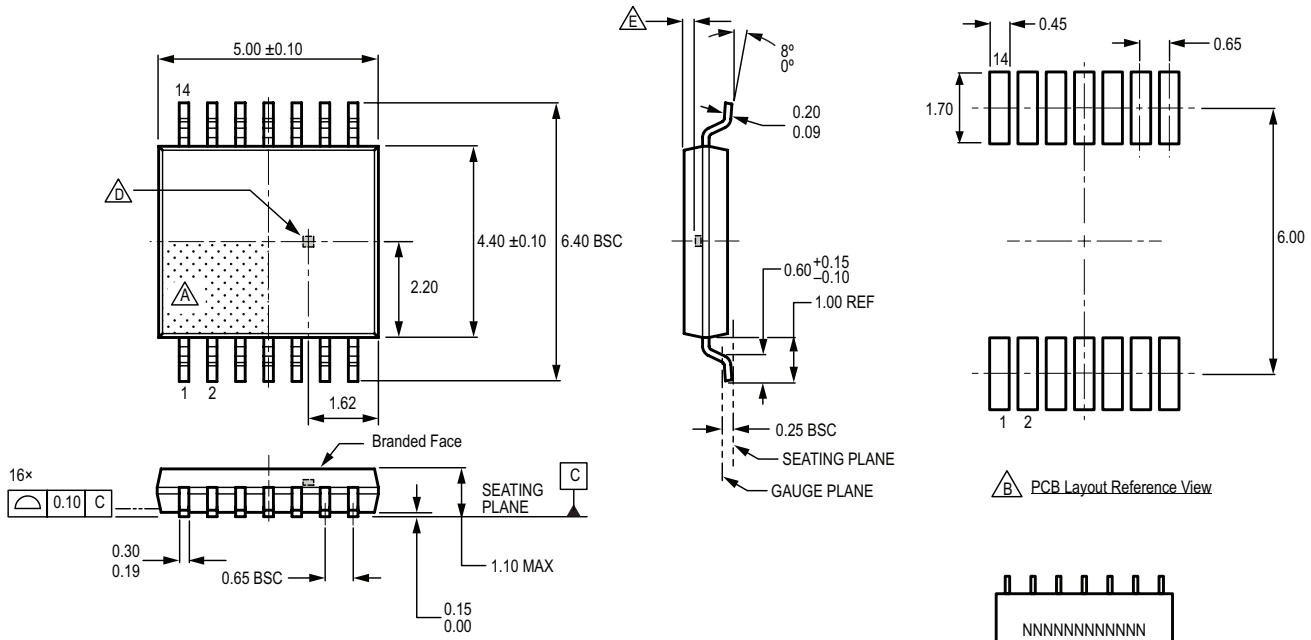
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PACKAGE OUTLINE DRAWINGS

For Reference Only – Not for Tooling Use

(Reference Allegro DWG-0000381, Rev. 1)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown



A Terminal #1 mark area

B Reference land pattern layout (reference IPC7351 TSOP65P640X120-14M); All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

C Branding scale and appearance at supplier discretion

D Hall element, not to scale

E Active Area Depth 0.36 mm REF

C Standard Branding Reference View

N = Device part number
= Supplier emblem
Y = Last two digits of year of manufacture
W = Week of manufacture
L = Lot number

Figure 30: Package LE, 14-Pin TSSOP

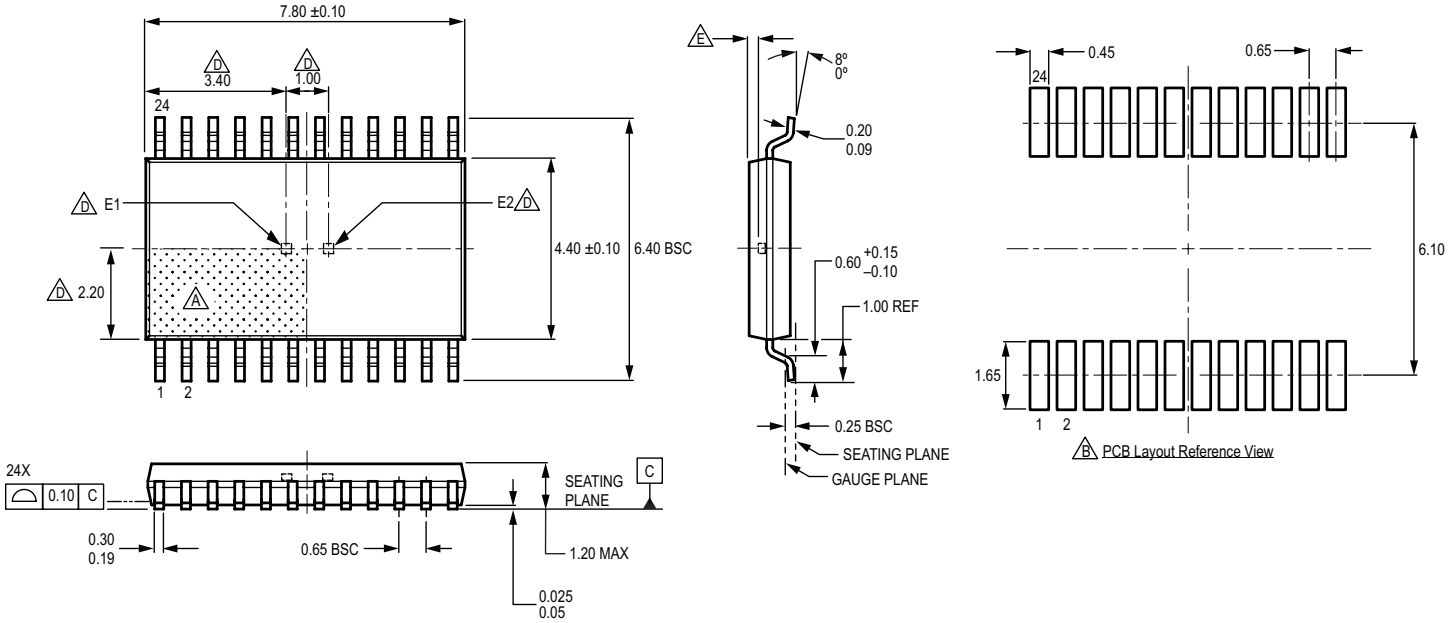
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(Reference Allegro DWG-0000381, Rev. 1)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown



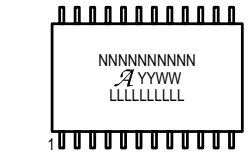
A Terminal #1 mark area

B Reference land pattern layout (reference IPC7351 TSOP65P640X120-25M); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

C Branding scale and appearance at supplier discretion

D Hall elements (E1, E2), corresponding to respective die; not to scale

E Active Area Depth 0.36 mm REF



C Standard Branding Reference View

N = Device part number
A = Supplier emblem
Y = Last two digits of year of manufacture
W = Week of manufacture
L = Lot number

Figure 31: Package LE, 24-Pin TSSOP

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Revision History

Number	Date	Description
–	November 18, 2016	Initial release
1	July 13, 2017	Updated MOSI_1/SCLK_1/ID1_1 and MOSI_2/SCLK_2/ID1_2 pinouts, WAKEx Input Specifications, PWM Output Signal, SENT Output Signal, Figure 12, 13, and 16.
2	January 25, 2018	Updated Typical Application Diagram (page 4); Bypass2 Pin Output Voltage characteristic and test conditions (page 7); PWM Carrier Frequency test conditions, Sent Output Signal maximum value, Logical BIST Coverage versus Time (page 8); Effective Resolution typical value, footnotes 8-15 (page 9); Overview, Angle Measurement sections (page 10-11); Manchester Code Low Voltage maximum value (page 14); Table 4 (page 17); Table 5 (page 18); ERR Register Address table and bit 3 detail (page 19); CTRL Register, STS Self-Test Start (page 21); Calculating Target Zero-Degree Angle (page 23); and Figure 22 (page 28).
3	April 4, 2018	Updated PWM Interface Specifications (page 8); PWM Output section (page 12); EEPROM Registers Map Table (page 17); Serial Interface Structure (pages 19-23); Figures 18 and 20 (pages 28-29).
4	January 25, 2019	Minor editorial updates
5	March 6, 2020	Minor editorial updates
7	January 15, 2021	Updated Typical Applications (page 4), MOSI Hold Time value (page 7), Figure 11 (page 15), Table 4 (page 17), and Package Outline Drawing reference numbers (pages 31-32).

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