25AA1024

1 Mbit SPI Bus Serial EEPROM

Device Selection Table

Part Number	Vcc Range	Page Size	Temp. Ranges	Packages
25AA1024	1.8-5.5V	256 Byte	I	P, SM, MF

Features

- 20 MHz Maximum Clock Speed
- Byte and Page-level Write Operations:
  - 256 byte page
  - 6 ms maximum write cycle time
  - No page or sector erase required
- Low-Power CMOS Technology:
  - Maximum Write current: 7 mA at 5.5V
  - Maximum Read current: 10 mA at 5.5V, 20 MHz
  - Standby current: 1 µA at 2.5V, 85°C (Deep Power-down)
- Electronic Signature for Device ID
- Self-Timed Erase and Write Cycles:
  - Page Erase (6 ms maximum)
  - Sector Erase (10 ms maximum)
  - Chip Erase (10 ms maximum)
- Sector Write Protection (32K byte/sector):
  - Protect none, 1/4, 1/2 or all of array
- Built-in Write Protection:
  - Power-on/off data protection circuitry
  - Write enable latch
  - Write-protect pin
- High Reliability:
  - Endurance: 1M erase/write cycles
  - Data Retention: >200 years
  - ESD Protection: 4000V
- Temperature Ranges Supported:
  - Industrial (I):-40°C to +85°C
- RoHS Compliant

Pin Function Table

Name	Function
$\overline{CS}$	Chip Select Input
SO	Serial Data Output
$\overline{WP}$	Write-Protect
Vss	Ground
SI	Serial Data Input
SCK	Serial Clock Input
$\overline{HOLD}$	Hold Input
Vcc	Supply Voltage

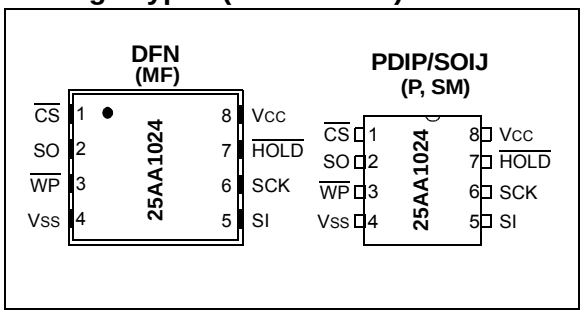
Description

The Microchip Technology Inc. 25AA1024 is a 1024 Kbit serial EEPROM memory with byte-level and page-level serial EEPROM functions. It also features Page, Sector and Chip erase functions typically associated with Flash-based products. These functions are not required for byte or page write operations. The memory is accessed via a simple Serial Peripheral Interface (SPI) compatible serial bus. The bus signals required are a clock input (SCK) plus separate data in (SI) and data out (SO) lines. Access to the device is controlled by a Chip Select ($\overline{CS}$) input.

Communication to the device can be paused via the hold pin ($\overline{HOLD}$). While the device is paused, transitions on its inputs will be ignored, with the exception of Chip Select, allowing the host to service higher priority interrupts.

The 25AA1024 is available in standard packages including 8-lead PDIP and SOIJ, and advanced 8-lead DFN package. All devices are RoHS compliant.

Package Types (not to scale)



深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com
微信扫码咨询客服

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (†)

VCC.....6.5V

All inputs and outputs w.r.t. VSS ..... -0.6V to VCC +1.0V

Storage temperature .....-65°C to 150°C

Ambient temperature under bias.....-40°C to 125°C

ESD protection on all pins.....4 kV

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for an extended period of time may affect device reliability.

TABLE 1-1: DC CHARACTERISTICS

DC CHARACTERISTICS			Industrial (I)*: TA = 0°C to +85°C VCC = 1.8V to 5.5V Industrial (I): TA = -40°C to +85°C VCC = 2.0V to 5.5V * Limited industrial temperature range.			
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Max.**	**Units**	**Test Conditions**
D001	VIH1	High-level Input Voltage	0.7 VCC	VCC +1	V	
D002	VIL1	Low-level Input Voltage	-0.3	0.3 VCC	V	VCC ≥ 2.7V
D003	VIL2		-0.3	0.2 VCC	V	VCC < 2.7V
D004	VOL	Low-level Output Voltage	—	0.4	V	IOL = 2.1 mA
D005	VOL		—	0.2	V	IOL = 1.0 mA, VCC < 2.5V
D006	VOH	High-level Output Voltage	VCC -0.2	—	V	IOH = -400 µA
D007	ILI	Input Leakage Current	—	±1	µA	$\overline{CS}$ = VCC, VIN = VSS or VCC
D008	ILO	Output Leakage Current	—	±1	µA	$\overline{CS}$ = VCC, VOUT = VSS or VCC
D009	CINT	Internal Capacitance (all inputs and outputs)	—	7	pF	TA = 25°C, CLK = 1.0 MHz, VCC = 5.0V **(Note)**
D010	ICCREAD	Operating Current	—	10	mA	VCC = 5.5V; FCLK = 20.0 MHz; SO = Open
			—	5	mA	VCC = 2.5V; FCLK = 10.0 MHz; SO = Open
D011	ICCWRITE		—	7	mA	VCC = 5.5V
			—	5	mA	VCC = 2.5V
D012	ICCS	Standby Current	—	12	µA	$\overline{CS}$ = VCC = 5.5V, Inputs tied to VCC or VSS, 85°C
D013	ICCSPD	Deep Power-down Current	—	1	µA	$\overline{CS}$ = VCC = 2.5V, Inputs tied to VCC or VSS, 85°C

Note: This parameter is periodically sampled and not 100% tested.

© 2007-2015 Microchip Technology Inc.
深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

TABLE 1-2: AC CHARACTERISTICS

AC CHARACTERISTICS			Industrial (I)*: TA = 0°C to +85°C VCC = 1.8V to 5.5V Industrial (I): TA = -40°C to +85°C VCC = 2.0V to 5.5V *Limited industrial temperature range.			
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Max.**	**Units**	**Conditions**
1	FCLK	Clock Frequency	—	20	MHz	4.5 ≤ VCC ≤ 5.5
			—	10	MHz	2.5 ≤ VCC < 4.5
			—	2	MHz	2.0 ≤ VCC < 2.5 1.8 ≤ VCC < 2.0, 0°C to +85°C
2	TCSS	$\overline{CS}$ Setup Time	25	—	ns	4.5 ≤ VCC ≤ 5.5
			50	—	ns	2.5 ≤ VCC < 4.5
			250	—	ns	2.0 ≤ VCC < 2.5 1.8 ≤ VCC < 2.0, 0°C to +85°C
3	TCSH	$\overline{CS}$ Hold Time	50	—	ns	4.5 ≤ VCC ≤ 5.5
			100	—	ns	2.5 ≤ VCC < 4.5
			500	—	ns	2.0 ≤ VCC < 2.5 1.8 ≤ VCC < 2.0, 0°C to +85°C (**Note 3**)
4	TCSD	$\overline{CS}$ Disable Time	50	—	ns	
5	TSU	Data Setup Time	5	—	ns	4.5 ≤ VCC ≤ 5.5
			10	—	ns	2.5 ≤ VCC < 4.5
			50	—	ns	2.0 ≤ VCC < 2.5 1.8 ≤ VCC < 2.0, 0°C to +85°C
6	THD	Data Hold Time	10	—	ns	4.5 ≤ VCC ≤ 5.5
			20	—	ns	2.5 ≤ VCC < 4.5
			100	—	ns	2.0 ≤ VCC < 2.5 1.8 ≤ VCC < 2.0, 0°C to +85°C
7	TR	CLK Rise Time	—	20	ns	(**Note 1**)
8	TF	CLK Fall Time	—	20	ns	(**Note 1**)
9	THI	Clock High Time	25	—		4.5 ≤ VCC ≤ 5.5
			50	—	ns	2.5 ≤ VCC < 4.5
			250	—	ns	2.0 ≤ VCC < 2.5 1.8 ≤ VCC < 2.0, 0°C to +85°C
10	TLO	Clock Low Time	25	—	ns	4.5 ≤ VCC ≤ 5.5
			50	—	ns	2.5 ≤ VCC < 4.5
			250	—	ns	2.0 ≤ VCC < 2.5 1.8 ≤ VCC < 2.0, 0°C to +85°C
11	TCLD	Clock Delay Time	50	—	ns	
12	TCLE	Clock Enable Time	50	—	ns	
13	TV	Output Valid from Clock Low	—	25	ns	4.5 ≤ VCC ≤ 5.5
			—	50	ns	2.5 ≤ VCC < 4.5
			—	250	ns	2.0 ≤ VCC < 2.5 1.8 ≤ VCC < 2.0, 0°C to +85°C

Note 1: This parameter is periodically sampled and not 100% tested.

2: This parameter is not tested but established by characterization and qualification. For endurance estimates in a specific application, please consult the Total Endurance™ Model which can be obtained from Microchip's web site at www.microchip.com.

3: Includes THI time.

深圳市满度科技有限公司 Tel:150-1290-5940
Web:www.manduic.com Email:sales@manduic.com

TABLE 1-2: AC CHARACTERISTICS (CONTINUED)

AC CHARACTERISTICS			Industrial (I)*: TA = 0°C to +85°C VCC = 1.8V to 5.5V Industrial (I): TA = -40°C to +85°C VCC = 2.0V to 5.5V *Limited industrial temperature range.			
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Max.**	**Units**	**Conditions**
14	THO	Output Hold Time	0	—	ns	(**Note 1**)
15	TDIS	Output Disable Time	—	25	ns	4.5 ≤ VCC ≤ 5.5
			—	50	ns	2.5 ≤ VCC < 4.5
			—	250	ns	2.0 ≤ VCC < 2.5 1.8 ≤ VCC < 2.0, 0°C to +85°C **(Note 1)**
16	THS	$\overline{HOLD}$ Setup Time	10	—	ns	4.5 ≤ VCC ≤ 5.5
			20	—	ns	2.5 ≤ VCC < 4.5
			100	—	ns	2.0 ≤ VCC < 2.5 1.8 ≤ VCC < 2.0, 0°C to +85°C
17	THH	$\overline{HOLD}$ Hold Time	10	—	ns	4.5 ≤ VCC ≤ 5.5
			20	—	ns	2.5 ≤ VCC < 4.5
			100	—	ns	2.0 ≤ VCC < 2.5 1.8 ≤ VCC < 2.0, 0°C to +85°C
18	THZ	$\overline{HOLD}$ Low to Output High Z	15	—	ns	4.5 ≤ VCC ≤ 5.5
			30	—	ns	2.5 ≤ VCC < 4.5
			150	—	ns	2.0 ≤ VCC < 2.5 1.8 ≤ VCC < 2.0, 0°C to +85°C (**Note 1**)
19	THV	$\overline{HOLD}$ High to Output Valid	15	—	ns	4.5 ≤ VCC ≤ 5.5
			30	—	ns	2.5 ≤ VCC < 4.5
			150	—	ns	2.0 ≤ VCC < 2.5 1.8 ≤ VCC < 2.0, 0°C to +85°C
20	TREL	$\overline{CS}$ High to Standby mode	—	100	µs	VCC = 1.8V to 5.5V
21	TPD	$\overline{CS}$ High to Deep Power-down	—	100	µs	VCC = 1.8V to 5.5V
22	TCE	Chip Erase Cycle Time	—	10	ms	VCC = 1.8V to 5.5V
23	TSE	Sector Erase Cycle Time	—	10	ms	VCC = 1.8V to 5.5V
24	TWC	Internal Write Cycle Time	—	6	ms	Byte or Page mode and Page Erase
25	—	Endurance	1M	—	E/W cycles	Page mode, 25°C, 5.5V (**Note 2**)

Note 1: This parameter is periodically sampled and not 100% tested.

2: This parameter is not tested but established by characterization and qualification. For endurance estimates in a specific application, please consult the Total Endurance™ Model which can be obtained from Microchip's web site at www.microchip.com.

3: Includes THI time.

© 2007-2015 Microchip Technology Inc.
深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

TABLE 1-3: AC TEST CONDITIONS

AC Waveform	
V_{LO} = 0.2V	—
V_{HI} = V_{CC} - 0.2V	**(Note 1)**
V_{HI} = 4.0V	**(Note 2)**
C_L = 30 pF	—
Timing Measurement Reference Level	
Input	0.5 V_{CC}
Output	0.5 V_{CC}

Note 1: For $V_{CC} \leq 4.0V$

2: For $V_{CC} > 4.0V$

FIGURE 1-1: HOLD TIMING

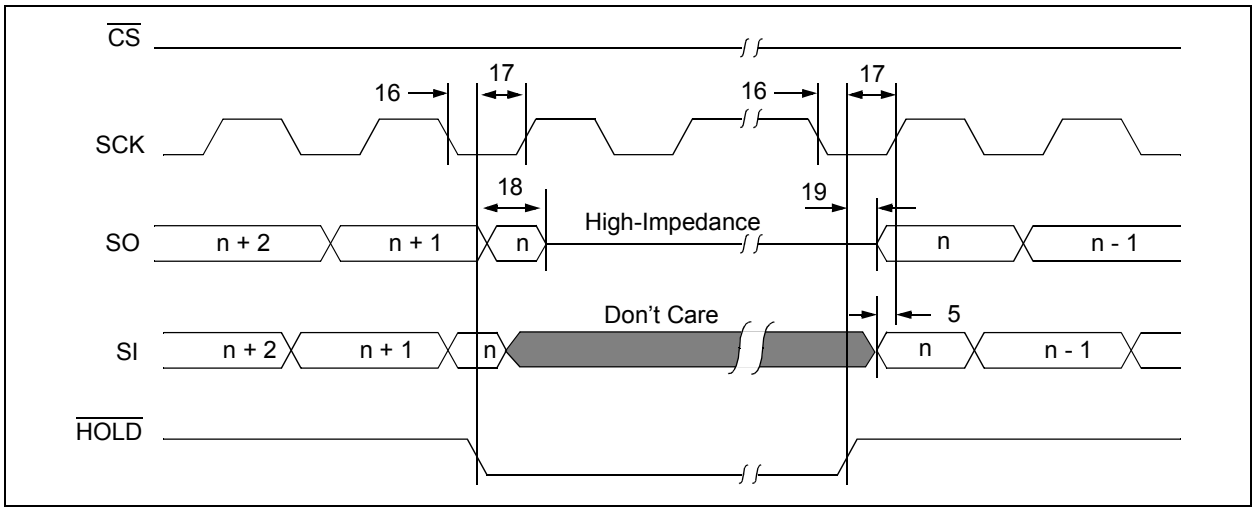
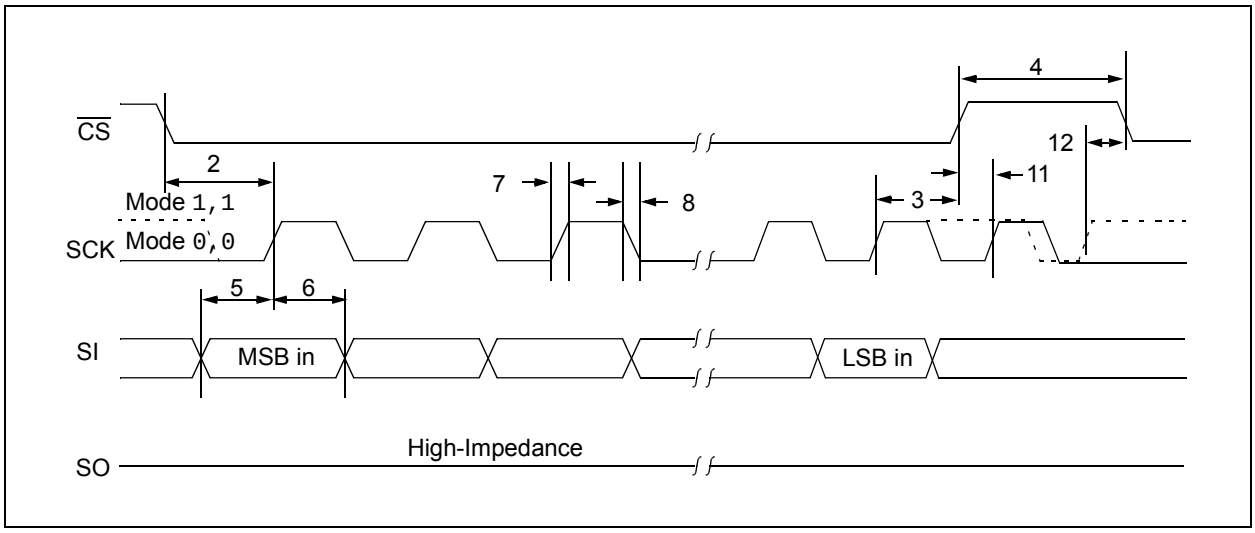
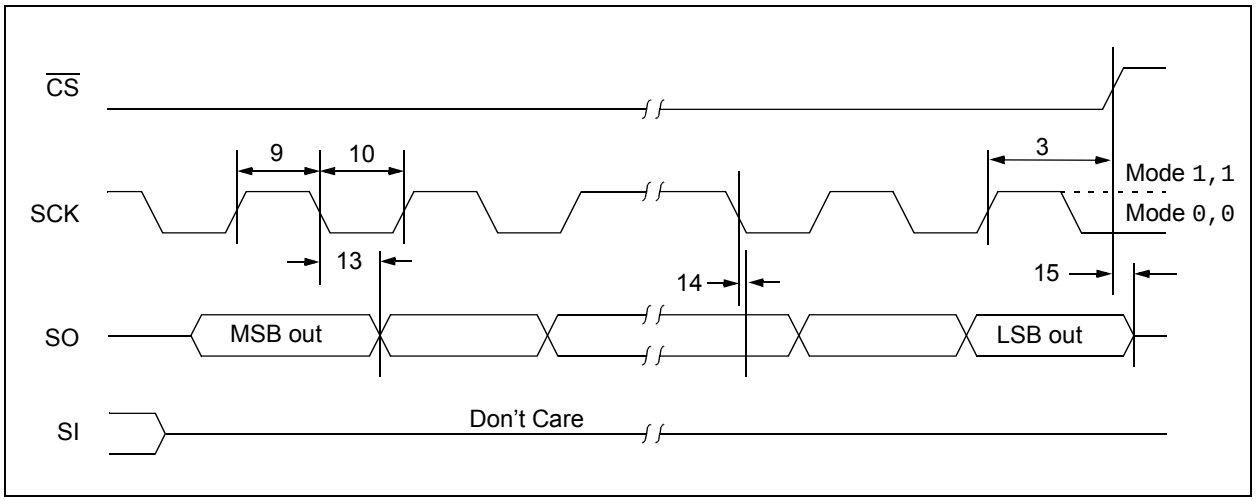


FIGURE 1-2: SERIAL INPUT TIMING



深圳市满度科技有限公司 Tel:150-1290-5940
Web:www.manduic.com Email:sales@manduic.com

FIGURE 1-3: SERIAL OUTPUT TIMING



© 2007-2015 Microchip Technology Inc.
深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

2.0 FUNCTIONAL DESCRIPTION

2.1 Principles of Operation

The 25AA1024 is a 131,072 byte Serial EEPROM designed to interface directly with the Serial Peripheral Interface (SPI) port of many of today's popular microcontroller families, including Microchip's PIC® microcontrollers. It may also interface with microcontrollers that do not have a built-in SPI port by using discrete I/O lines programmed properly in firmware to match the SPI protocol.

The 25AA1024 contains an 8-bit instruction register. The device is accessed via the SI pin, with data being clocked in on the rising edge of SCK. The $\overline{CS}$ pin must be low and the $\overline{HOLD}$ pin must be high for the entire operation.

Table 2-1 contains a list of the possible instruction bytes and format for device operation. All instructions, addresses and data are transferred MSB first, LSB last.

Data (SI) is sampled on the first rising edge of SCK after $\overline{CS}$ goes low. If the clock line is shared with other peripheral devices on the SPI bus, the user can assert the $\overline{HOLD}$ input and place the 25AA1024 in 'HOLD' mode. After releasing the $\overline{HOLD}$ pin, operation will resume from the point when the $\overline{HOLD}$ was asserted.

BLOCK DIAGRAM

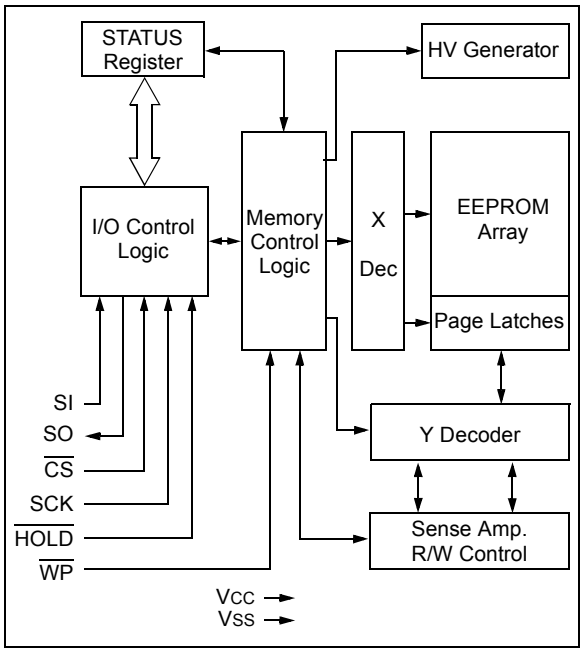


TABLE 2-1: INSTRUCTION SET

Instruction Name	Instruction Format	Description
READ	0000 0011	Read data from memory array beginning at selected address
WRITE	0000 0010	Write data to memory array beginning at selected address
WREN	0000 0110	Set the write enable latch (enable write operations)
WRDI	0000 0100	Reset the write enable latch (disable write operations)
RDSR	0000 0101	Read STATUS register
WRSR	0000 0001	Write STATUS register
PE	0100 0010	Page Erase – erase one page in memory array
SE	1101 1000	Sector Erase – erase one sector in memory array
CE	1100 0111	Chip Erase – erase all sectors in memory array
RDID	1010 1011	Release from Deep Power-down and Read Electronic Signature
DPD	1011 1001	Deep Power-Down mode

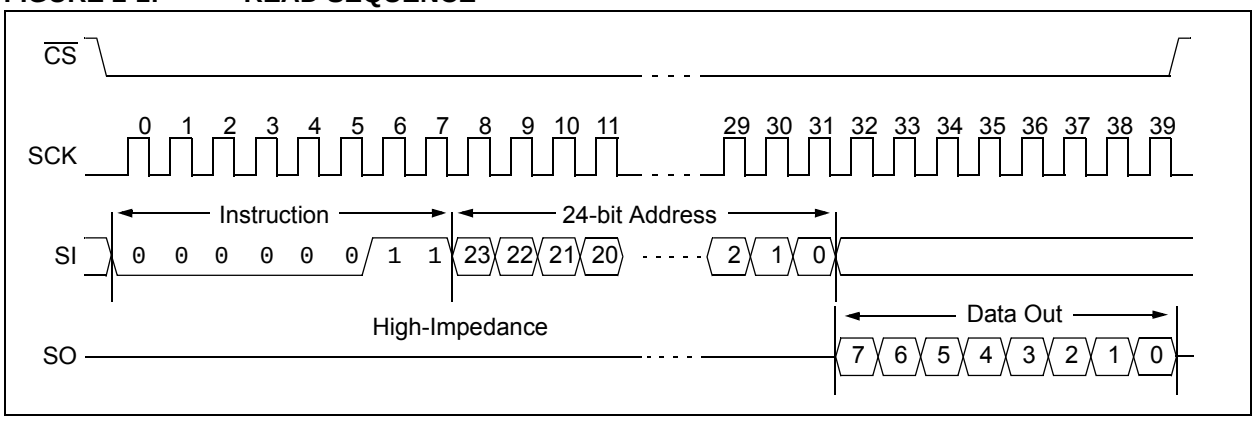
深圳市满度科技有限公司 Tel:150-1290-5940
Web:www.manduic.com Email:sales@manduic.com

Read Sequence

The device is selected by pulling $\overline{CS}$ low. The 8-bit READ instruction is transmitted to the 25AA1024 followed by the 24-bit address, with seven MSBs of the address being “don’t care” bits. After the correct READ instruction and address are sent, the data stored in the memory at the selected address is shifted out on the SO pin.

The data stored in the memory at the next address can be read sequentially by continuing to provide clock pulses. The internal Address Pointer is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached (1FFFFh), the address counter rolls over to address, 00000h, allowing the read cycle to be continued indefinitely. The read operation is terminated by raising the $\overline{CS}$ pin (Figure 2-1).

FIGURE 2-1: READ SEQUENCE



© 2007-2015 Microchip Technology Inc.
深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

2.2 Write Sequence

Prior to any attempt to write data to the 25AA1024, the write enable latch must be set by issuing the WREN instruction (Figure 2-4). This is done by setting $\overline{CS}$ low and then clocking out the proper instruction into the 25AA1024. After all eight bits of the instruction are transmitted, the $\overline{CS}$ must be brought high to set the write enable latch. If the write operation is initiated immediately after the WREN instruction without $\overline{CS}$ being brought high, the data will not be written to the array because the write enable latch will not have been properly set.

A write sequence includes an automatic, self-timed erase cycle. It is not required to erase any portion of the memory prior to issuing a Write command.

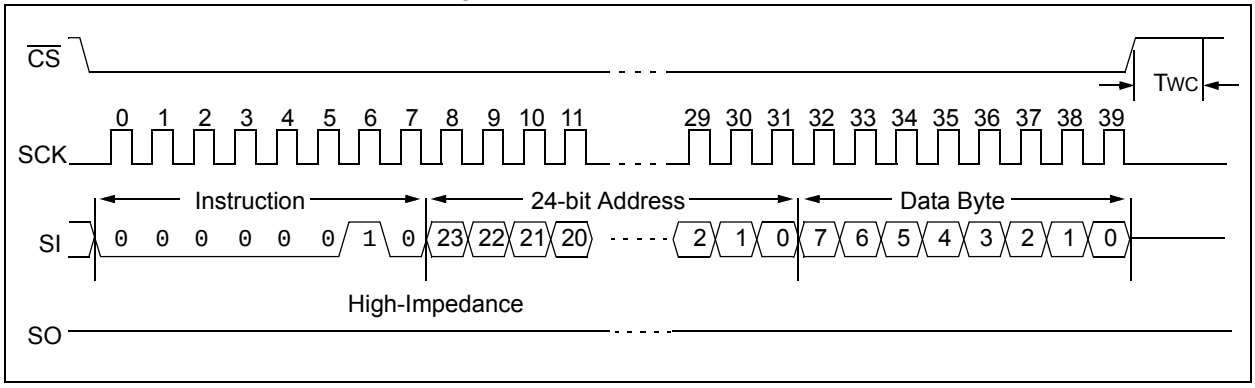
Once the write enable latch is set, the user may proceed by setting the $\overline{CS}$ low, issuing a WRITE instruction, followed by the 24-bit address, with seven MSBs of the address being "don't care" bits, and then the data to be written. Up to 256 bytes of data can be sent to the device before a write cycle is necessary. The only restriction is that all of the bytes must reside in the same page.

Note:	When doing a write of less than 256 bytes the data in the rest of the page is refreshed along with the data bytes being written. This will force the entire page to endure a write cycle, for this reason endurance is specified per page.

Note:	Page write operations are limited to writing bytes within a single physical page, **regardless** of the number of bytes actually being written. Physical page boundaries start at addresses that are integer multiples of the page buffer size (or 'page size'), and end at addresses that are integer multiples of page size – 1. If a Page Write command attempts to write across a physical page boundary, the result is that the data wraps around to the beginning of the current page (overwriting data previously stored there), instead of being written to the next page as might be expected. It is therefore necessary for the application software to prevent page write operations that would attempt to cross a page boundary.

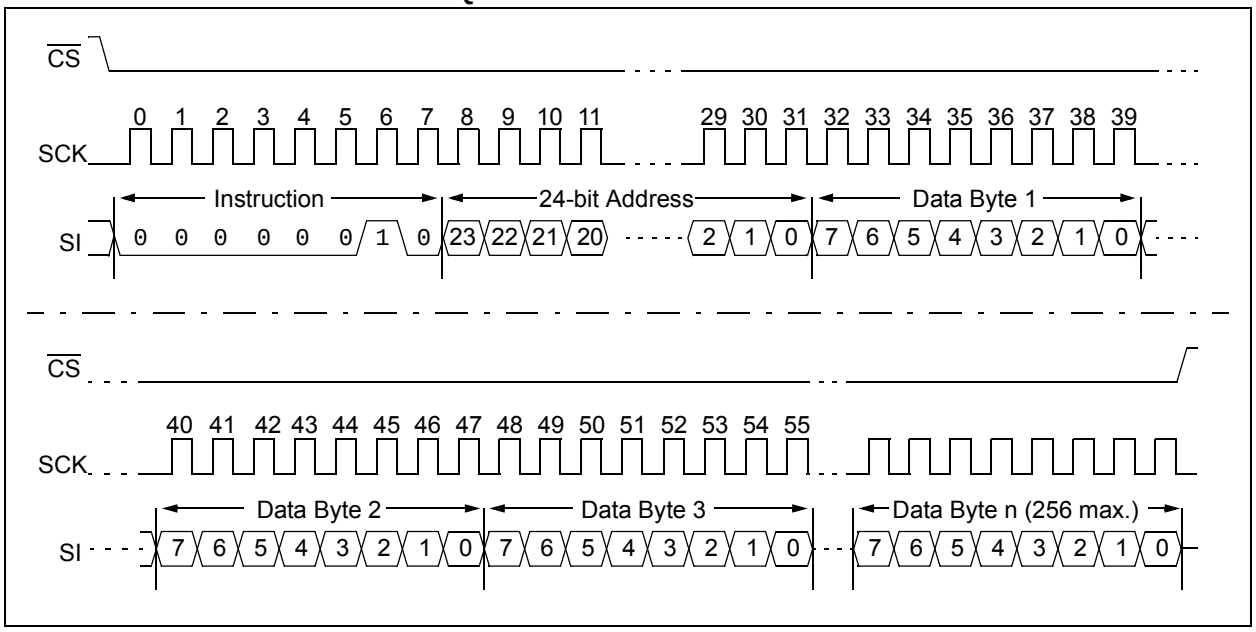
For the data to be actually written to the array, the $\overline{CS}$ must be brought high after the Least Significant bit (D0) of the n^{th} data byte has been clocked in. If $\overline{CS}$ is brought high at any other time, the write operation will not be completed. Refer to Figure 2-2 and Figure 2-3 for more detailed illustrations on the byte write sequence and the page write sequence, respectively. While the write is in progress, the STATUS register may be read to check the status of the WPEN, WIP, WEL, BP1 and BP0 bits (Figure 2-6). A read attempt of a memory array location will not be possible during a write cycle. When the write cycle is completed, the write enable latch is reset.

FIGURE 2-2: BYTE WRITE SEQUENCE



深圳市满度科技有限公司 Tel:150-1290-5940
Web:www.manduic.com Email:sales@manduic.com

FIGURE 2-3: PAGE WRITE SEQUENCE



© 2007-2015 Microchip Technology Inc.
深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

2.3 Write Enable (WREN) and Write Disable (WRDI)

The 25AA1024 contains a write enable latch. See Table 2-4 for the Write-Protect Functionality Matrix. This latch must be set before any write operation will be completed internally. The WREN instruction will set the latch, and the WRDI will reset the latch.

The following is a list of conditions under which the write enable latch will be reset:

- Power-up
- WRDI instruction successfully executed
- WRSR instruction successfully executed
- WRITE instruction successfully executed
- PE instruction successfully executed
- SE instruction successfully executed
- CE instruction successfully executed

FIGURE 2-4: WRITE ENABLE SEQUENCE (WREN)

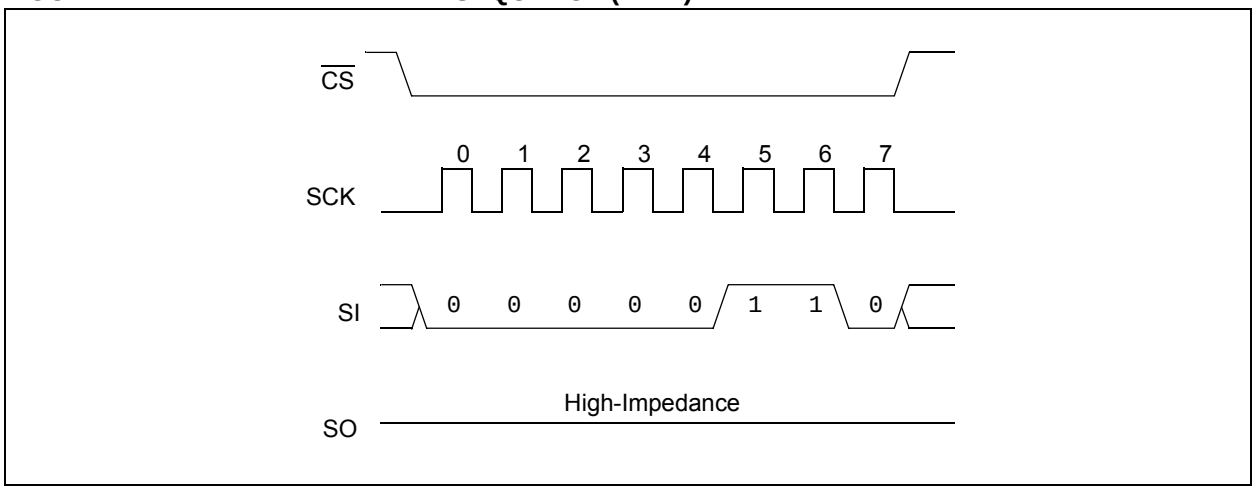
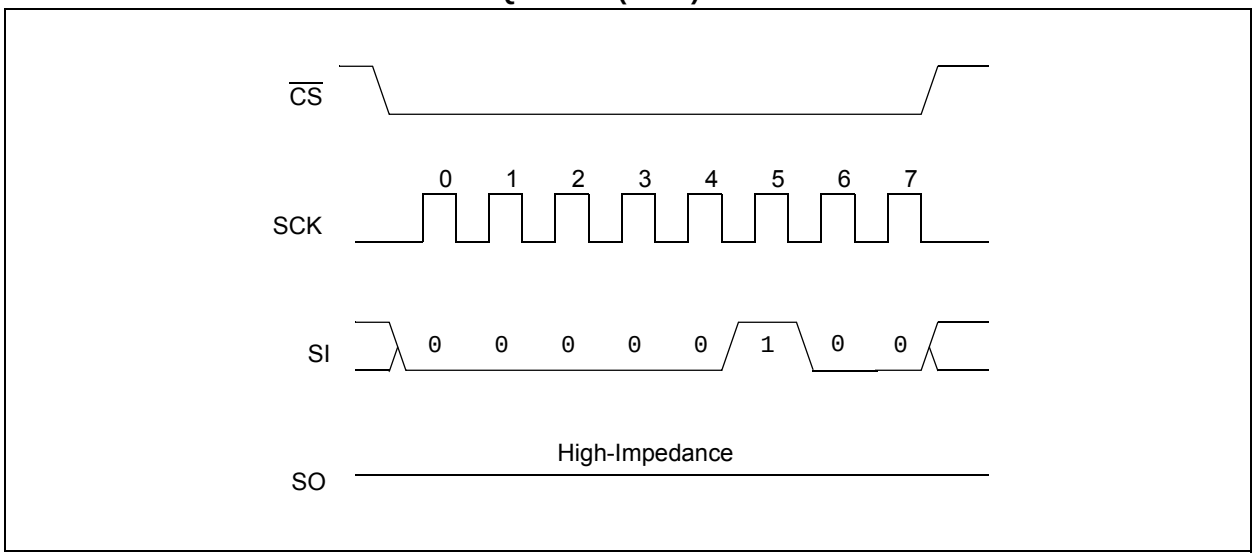


FIGURE 2-5: WRITE DISABLE SEQUENCE (WRDI)



深圳市满度科技有限公司 Tel:150-1290-5940
Web:www.manduic.com Email:sales@manduic.com

2.4 Read Status Register Instruction (RDSR)

The Read Status Register instruction (RDSR) provides access to the STATUS register. The STATUS register may be read at any time, even during a write cycle. The STATUS register is formatted as follows:

TABLE 2-2: STATUS REGISTER

7	6	5	4	3	2	1	0
W/R	–	–	–	W/R	W/R	R	R
WPEN	X	X	X	BP1	BP0	WEL	WIP
W/R = writable/readable. R = read-only.							

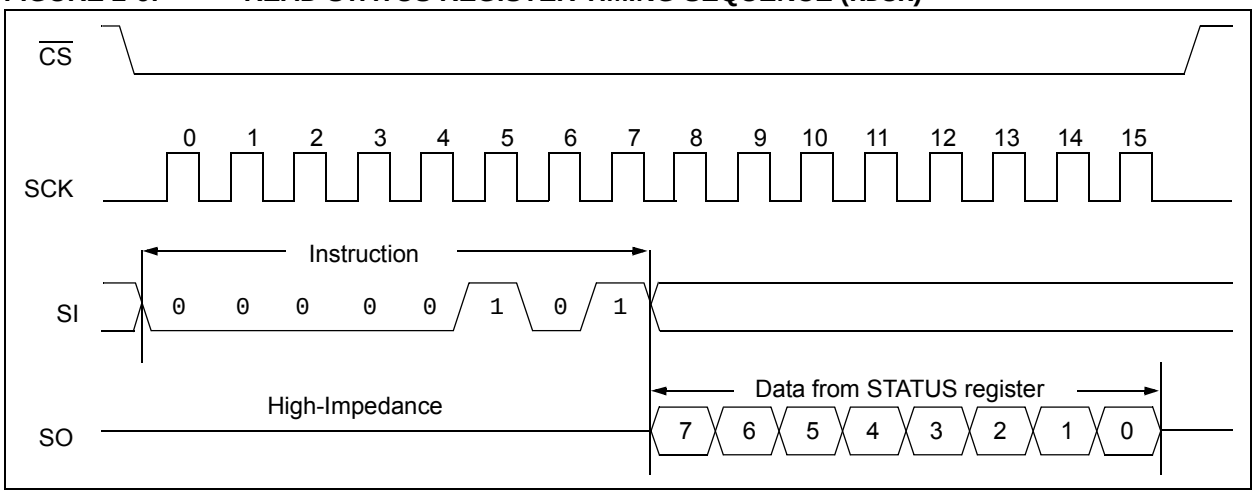
The **Write-In-Process (WIP)** bit indicates whether the 25AA1024 is busy with a write operation. When set to a '1', a write is in progress, when set to a '0', no write is in progress. This bit is read-only.

The **Write Enable Latch (WEL)** bit indicates the status of the write enable latch and is read-only. When set to a '1', the latch allows writes to the array, when set to a '0', the latch prohibits writes to the array. The state of this bit can always be updated via the WREN or WRDI commands regardless of the state of write protection on the STATUS register. These commands are shown in Figure 2-4 and Figure 2-5.

The **Block Protection (BP0 and BP1)** bits indicate which blocks are currently write-protected. These bits are set by the user issuing the WRSR instruction. These bits are nonvolatile and are shown in Table 2-3.

See Figure 2-6 for the RDSR timing sequence.

FIGURE 2-6: READ STATUS REGISTER TIMING SEQUENCE (RDSR)



© 2007-2015 Microchip Technology Inc.
深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

2.5 Write Status Register Instruction (WRSR)

The Write Status Register instruction (WRSR) allows the user to write to the nonvolatile bits in the STATUS register, as shown in Table 2-2. The user is able to select one of four levels of protection for the array by writing to the appropriate bits in the STATUS register. The array is divided up into four segments. The user has the ability to write-protect none, one, two, or all four of the segments of the array. The partitioning is controlled, as shown in Table 2-3.

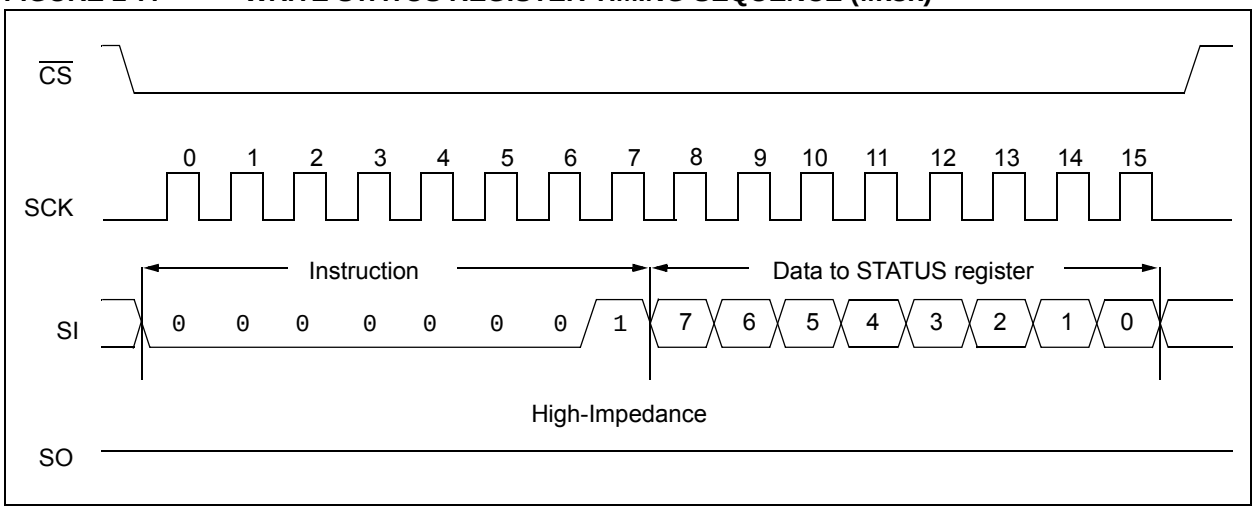
The Write-Protect Enable (WPEN) bit is a nonvolatile bit that is available as an enable bit for the $\overline{WP}$ pin. The Write-Protect ($\overline{WP}$) pin and the Write-Protect Enable (WPEN) bit in the STATUS register control the programmable hardware write-protect feature. Hardware write protection is enabled when the $\overline{WP}$ pin is low and the WPEN bit is high. Hardware write protection is disabled when either the $\overline{WP}$ pin is high or the WPEN bit is low. When the chip is hardware write-protected, only writes to nonvolatile bits in the STATUS register are disabled. See Table 2-4 for a matrix of functionality on the WPEN bit.

See Figure 2-7 for the WRSR timing sequence.

TABLE 2-3: ARRAY PROTECTION

BP1	BP0	Array Addresses Write-Protected	Array Addresses Unprotected
0	0	none	All (Sectors 0, 1, 2 & 3) (00000h-1FFFFh)
0	1	Upper 1/4 (Sector 3) (18000h-1FFFFh)	Lower 3/4 (Sectors 0, 1 & 2) (00000h-17FFFh)
1	0	Upper 1/2 (Sectors 2 & 3) (10000h-1FFFFh)	Lower 1/2 (Sectors 0 & 1) (00000h-0FFFFh)
1	1	All (Sectors 0, 1, 2 & 3) (00000h-1FFFFh)	none

FIGURE 2-7: WRITE STATUS REGISTER TIMING SEQUENCE (WRSR)



深圳市满度科技有限公司 Tel:150-1290-5940
Web:www.manduic.com Email:sales@manduic.com

2.6 Data Protection

The following protection has been implemented to prevent inadvertent writes to the array:

- The write enable latch is reset on power-up
- A write enable instruction must be issued to set the write enable latch
- After a byte write, page write or STATUS register write, the write enable latch is reset
- $\overline{CS}$ must be set high after the proper number of clock cycles to start an internal write cycle
- Access to the array during an internal write cycle is ignored and programming is continued

2.7 Power-On State

The 25AA1024 powers on in the following state:

- The device is in low-power Standby mode ($\overline{CS}$ = 1)
- The write enable latch is reset
- SO is in high-impedance state
- A high-to-low-level transition on $\overline{CS}$ is required to enter active state

TABLE 2-4: WRITE-PROTECT FUNCTIONALITY MATRIX

WEL (SR bit 1)	WPEN (SR bit 7)	$\overline{WP}$ (pin 3)	Protected Blocks	Unprotected Blocks	STATUS Register
0	x	x	Protected	Protected	Protected
1	0	x	Protected	Writable	Writable
1	1	0 (low)	Protected	Writable	Protected
1	1	1 (high)	Protected	Writable	Writable

x = don't care

© 2007-2015 Microchip Technology Inc.
深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

2.8 PAGE ERASE

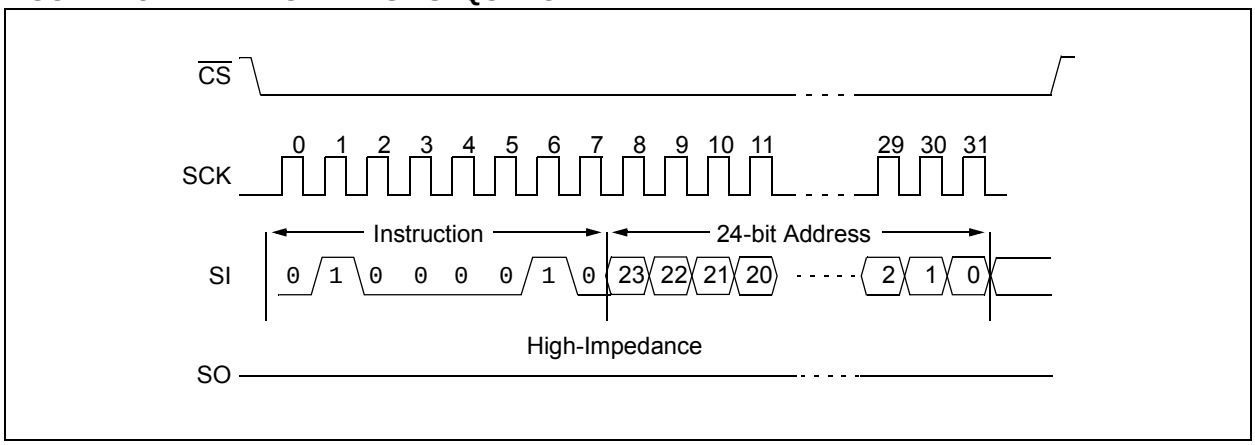
The Page Erase function will erase all bits (FFh) inside the given page. A Write Enable (WREN) instruction must be given prior to attempting a Page Erase. This is done by setting $\overline{CS}$ low and then clocking out the proper instruction into the 25AA1024. After all eight bits of the instruction are transmitted, the $\overline{CS}$ must be brought high to set the write enable latch.

The Page Erase function is entered by driving $\overline{CS}$ low, followed by the instruction code (Figure 2-8), and three address bytes. Any address inside the page to be erased is a valid address.

$\overline{CS}$ must then be driven high after the last bit if the address or the Page Erase will not execute. Once the $\overline{CS}$ is driven high, the self-timed Page Erase cycle is started. The WIP bit in the STATUS register can be read to determine when the Page Erase cycle is complete.

If a Page Erase function is given to an address that has been protected by the Block Protect bits (BP0, BP1) then the sequence will be aborted and no erase will occur.

FIGURE 2-8: PAGE ERASE SEQUENCE



深圳市满度科技有限公司 Tel:150-1290-5940
Web:www.manduic.com Email:sales@manduic.com

2.9 SECTOR ERASE

The Sector Erase function will erase all bits (FFh) inside the given sector. A Write Enable (WREN) instruction must be given prior to executing a Sector Erase. This is done by setting $\overline{CS}$ low and then clocking out the proper instruction into the 25AA1024. After all eight bits of the instruction are transmitted, the $\overline{CS}$ must be brought high to set the write enable latch.

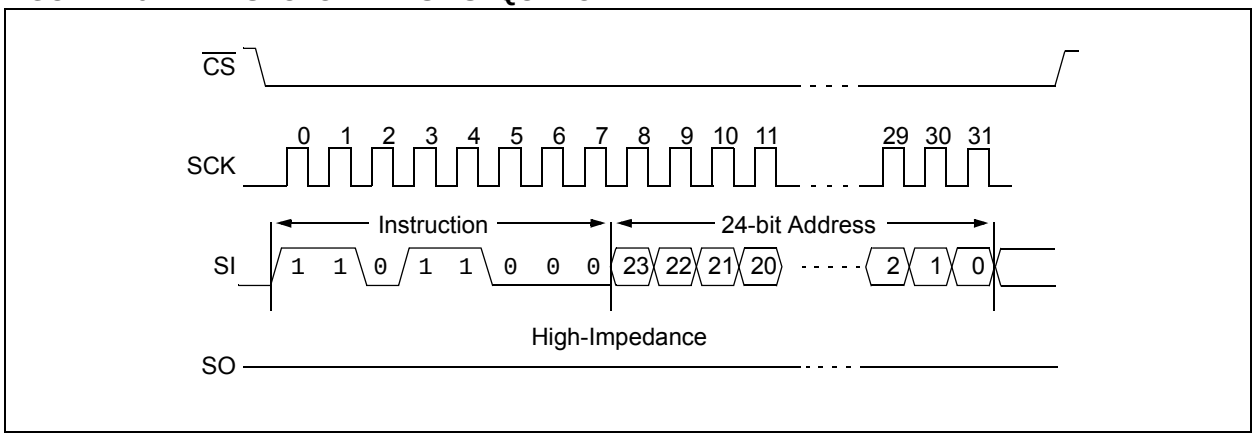
The Sector Erase function is entered by driving $\overline{CS}$ low, followed by the instruction code (Figure 2-9), and three address bytes. Any address inside the sector to be erased is a valid address.

$\overline{CS}$ must then be driven high after the last bit if the address or the Sector Erase will not execute. Once the $\overline{CS}$ is driven high, the self-timed Sector Erase cycle is started. The WIP bit in the STATUS register can be read to determine when the Sector Erase cycle is complete.

If a SECTOR ERASE instruction is given to an address that has been protected by the Block Protect bits (BP0, BP1) then the sequence will be aborted and no erase will occur.

See Table 2-3 for Sector Addressing.

FIGURE 2-9: SECTOR ERASE SEQUENCE



© 2007-2015 Microchip Technology Inc.
深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

2.10 CHIP ERASE

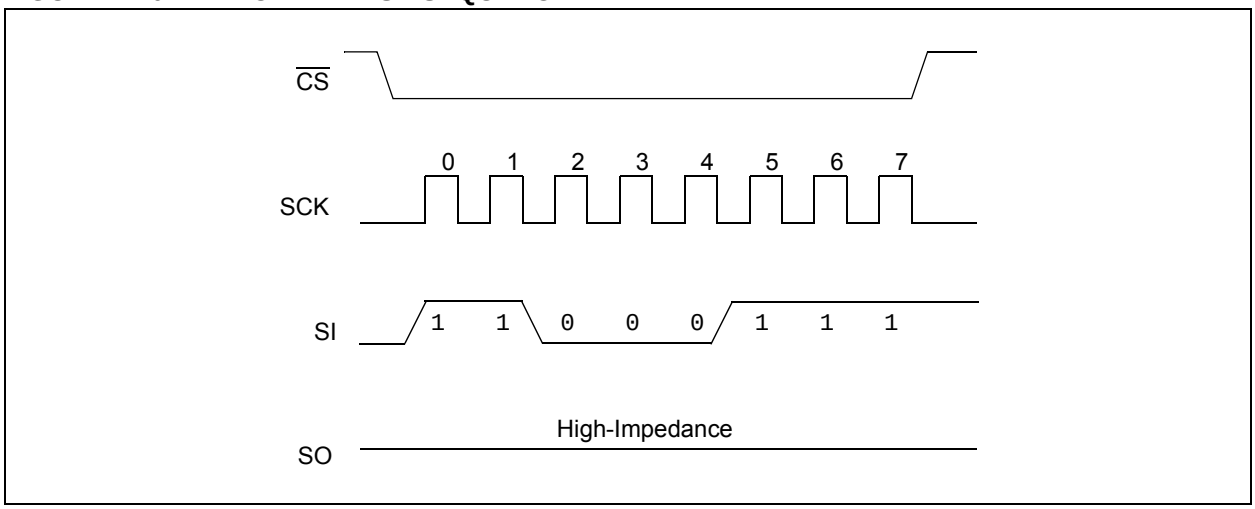
The Chip Erase function will erase all bits (FFh) in the array. A Write Enable (WREN) instruction must be given prior to executing a Chip Erase. This is done by setting $\overline{CS}$ low and then clocking out the proper instruction into the 25AA1024. After all eight bits of the instruction are transmitted, the $\overline{CS}$ must be brought high to set the write enable latch.

The Chip Erase function is entered by driving the $\overline{CS}$ low, followed by the instruction code (Figure 2-10) onto the SI line.

The $\overline{CS}$ pin must be driven high after the eighth bit of the instruction code has been given or the Chip Erase function will not be executed. Once the $\overline{CS}$ pin is driven high, the self-timed Chip Erase function begins. While the device is executing the Chip Erase function the WIP bit in the STATUS register can be read to determine when the Chip Erase function is complete.

The Chip Erase function is ignored if either of the Block Protect bits (BP0, BP1) are not 0, meaning ¼, ½, or all of the array is protected.

FIGURE 2-10: CHIP ERASE SEQUENCE



深圳市满度科技有限公司 Tel:150-1290-5940
Web:www.manduic.com Email:sales@manduic.com

2.11 DEEP POWER-DOWN MODE

Deep Power-Down mode of the 25AA1024 is its lowest power consumption state. The device will not respond to any of the Read or Write commands while in Deep Power-Down mode, and therefore it can be used as an additional software write protection feature.

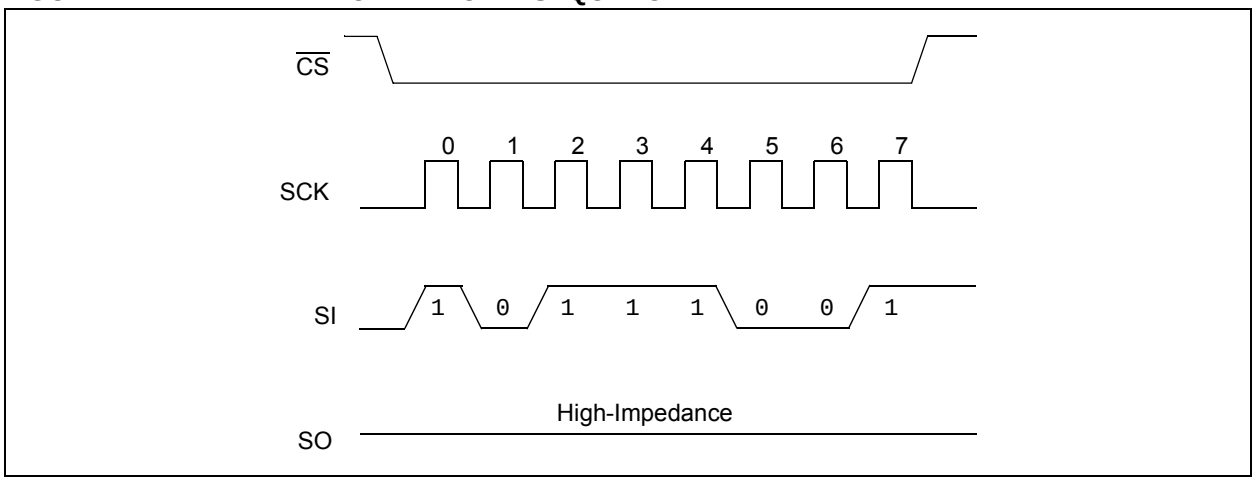
The Deep Power-Down mode is entered by driving $\overline{CS}$ low, followed by the instruction code (Figure 2-11) onto the SI line, followed by driving $\overline{CS}$ high.

If the $\overline{CS}$ pin is not driven high after the eighth bit of the instruction code has been given, the device will not execute Deep Power-down. Once the $\overline{CS}$ line is driven high, there is a delay (TDP) before the current settles to its lowest consumption.

All instructions given during Deep Power-Down mode are ignored except the Read Electronic Signature Command (RDID). The RDID command will release the device from Deep Power-down and outputs the electronic signature on the SO pin, and then returns the device to Standby mode after delay (TREL).

Deep Power-Down mode automatically releases at device power-down. Once power is restored to the device, it will power-up in the Standby mode.

FIGURE 2-11: DEEP POWER-DOWN SEQUENCE



© 2007-2015 Microchip Technology Inc.
深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

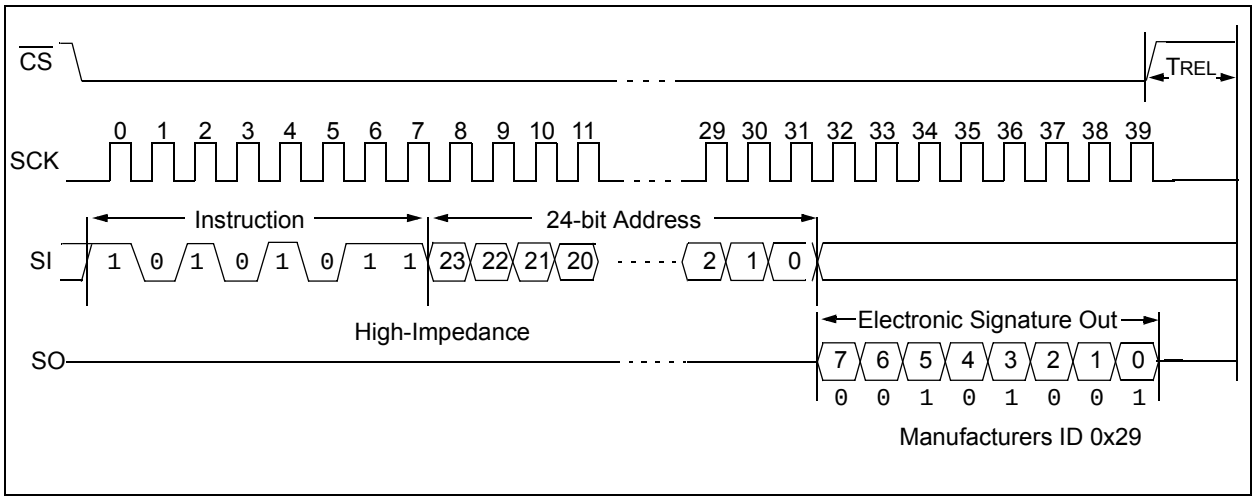
2.12 RELEASE FROM DEEP POWER-DOWN AND READ ELECTRONIC SIGNATURE

Once the device has entered Deep Power-Down mode, all instructions are ignored except the release from Deep Power-down and Read Electronic Signature command. This command can also be used when the device is not in Deep Power-down, to read the electronic signature out on the SO pin unless another command is being executed such as Erase, Program or Write STATUS register.

Release from Deep Power-Down mode and Read Electronic Signature is entered by driving $\overline{CS}$ low, followed by the RDID instruction code (Figure 2-12) and then a dummy address of 24 bits (A23-A0). After the last bit of the dummy address is clocked in, the 8-bit electronic signature is clocked out on the SO pin.

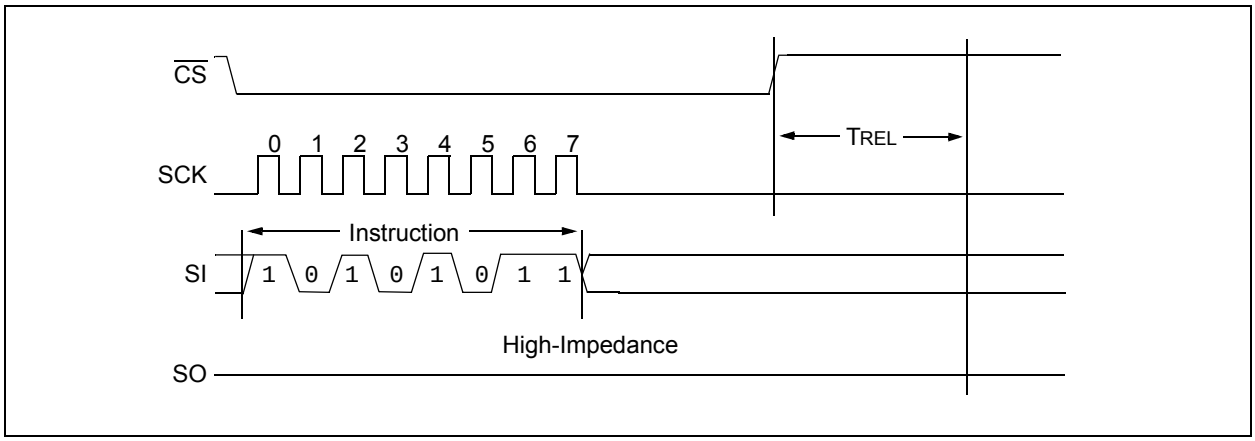
After the signature has been read out at least once, the sequence can be terminated by driving $\overline{CS}$ high. After a delay of TREL, the device will then return to Standby mode and will wait to be selected so it can be given new instructions. If additional clock cycles are sent after the electronic signature has been read once, it will continue to output the signature on the SO line until the sequence is terminated.

FIGURE 2-12: RELEASE FROM DEEP POWER-DOWN AND READ ELECTRONIC SIGNATURE



Driving $\overline{CS}$ high after the 8-bit RDID command, but before the electronic signature has been transmitted, will still ensure the device will be taken out of Deep Power-Down mode, as shown in Figure 2-13.

FIGURE 2-13: RELEASE FROM DEEP POWER-DOWN AND READ ELECTRONIC SIGNATURE



深圳市满度科技有限公司 Tel:150-1290-5940
Web:www.manduic.com Email:sales@manduic.com

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Name	Pin Number	Function
$\overline{CS}$	1	Chip Select Input
SO	2	Serial Data Output
$\overline{WP}$	3	Write-Protect Pin
VSS	4	Ground
SI	5	Serial Data Input
SCK	6	Serial Clock Input
$\overline{HOLD}$	7	Hold Input
VCC	8	Supply Voltage

3.1 Chip Select ($\overline{CS}$)

A low level on this pin selects the device. A high level deselects the device and forces it into Standby mode. However, a programming cycle which is already initiated or in progress will be completed, regardless of the $\overline{CS}$ input signal. If $\overline{CS}$ is brought high during a program cycle, the device will go into Standby mode as soon as the programming cycle is complete. When the device is deselected, SO goes to the high-impedance state, allowing multiple parts to share the same SPI bus. A low-to-high transition on $\overline{CS}$ after a valid write sequence initiates an internal write cycle. After power-up, a low level on $\overline{CS}$ is required prior to any sequence being initiated.

3.2 Serial Output (SO)

The SO pin is used to transfer data out of the 25AA1024. During a read cycle, data is shifted out on this pin after the falling edge of the serial clock.

3.3 Write-Protect ($\overline{WP}$)

This pin is used in conjunction with the WPEN bit in the STATUS register to prohibit writes to the nonvolatile bits in the STATUS register. When $\overline{WP}$ is low and WPEN is high, writing to the nonvolatile bits in the STATUS register is disabled. All other operations function normally. When $\overline{WP}$ is high, all functions, including writes to the nonvolatile bits in the STATUS register, operate normally. If the WPEN bit is set, $\overline{WP}$ low during a STATUS register write sequence will disable writing to the STATUS register. If an internal write cycle has already begun, $\overline{WP}$ going low will have no effect on the write.

The $\overline{WP}$ pin function is blocked when the WPEN bit in the STATUS register is low. This allows the user to install the 25AA1024 in a system with $\overline{WP}$ pin grounded and still be able to write to the STATUS register. The $\overline{WP}$ pin functions will be enabled when the WPEN bit is set high.

3.4 Serial Input (SI)

The SI pin is used to transfer data into the device. It receives instructions, addresses and data. Data is latched on the rising edge of the serial clock.

3.5 Serial Clock (SCK)

The SCK is used to synchronize the communication between a master and the 25AA1024. Instructions, addresses or data present on the SI pin are latched on the rising edge of the clock input, while data on the SO pin is updated after the falling edge of the clock input.

3.6 Hold ($\overline{HOLD}$)

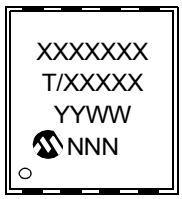
The $\overline{HOLD}$ pin is used to suspend transmission to the 25AA1024 while in the middle of a serial sequence without having to retransmit the entire sequence again. It must be held high any time this function is not being used. Once the device is selected and a serial sequence is underway, the $\overline{HOLD}$ pin may be pulled low to pause further serial communication without resetting the serial sequence. The $\overline{HOLD}$ pin must be brought low while SCK is low, otherwise the $\overline{HOLD}$ function will not be invoked until the next SCK high-to-low transition. The 25AA1024 must remain selected during this sequence. The SI, SCK and SO pins are in a high-impedance state during the time the device is paused and transitions on these pins will be ignored. To resume serial communication, $\overline{HOLD}$ must be brought high while the SCK pin is low, otherwise serial communication will not resume. Pulling the $\overline{HOLD}$ line low at any time will tri-state the SO line.

© 2007-2015 Microchip Technology Inc.
深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

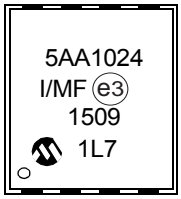
4.0 PACKAGING INFORMATION

4.1 Package Marking Information

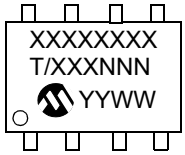
8-Lead DFN



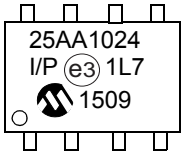
Example:



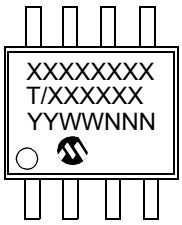
8-Lead PDIP



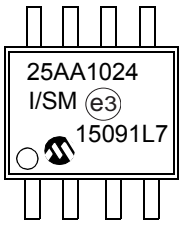
Example:



8-Lead SOIJ



Example:



Legend:	XX...X	Part number or part number code
	T	Temperature (I, E)
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code (2 characters for small packages)
	(e3)	JEDEC® designator for Matte Tin (Sn)

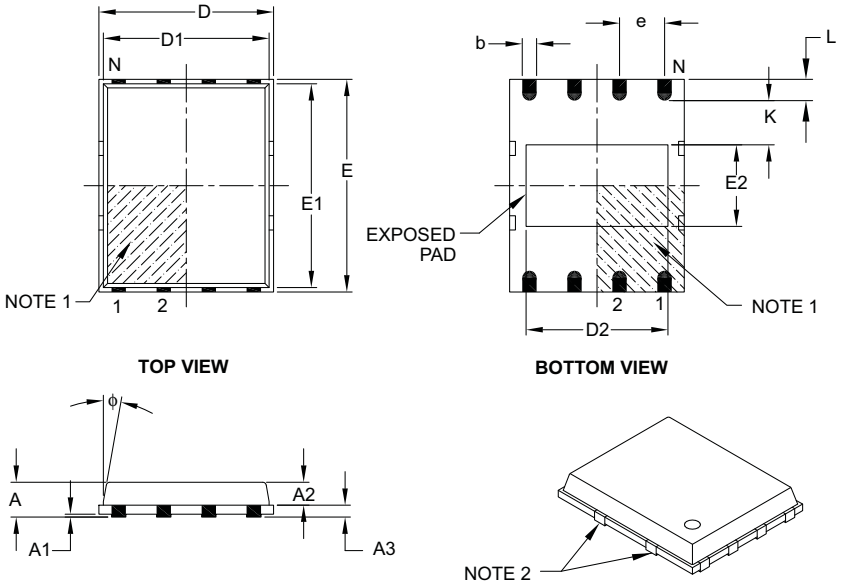
Note: For very small packages with no room for the JEDEC® designator (e3), the marking will only appear on the outer carton or reel label.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

深圳市满度科技有限公司 Tel:150-1290-5940
Web:www.manduic.com Email:sales@manduic.com

8-Lead Plastic Dual Flat, No Lead Package (MF) – 6x5 mm Body [DFN-S] PUNCH SINGULATED

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	–	0.85	1.00
Molded Package Thickness	A2	–	0.65	0.80
Standoff	A1	0.00	0.01	0.05
Base Thickness	A3		0.20 REF	
Overall Length	D		4.92 BSC	
Molded Package Length	D1		4.67 BSC	
Exposed Pad Length	D2	3.85	4.00	4.15
Overall Width	E		5.99 BSC	
Molded Package Width	E1		5.74 BSC	
Exposed Pad Width	E2	2.16	2.31	2.46
Contact Width	b	0.35	0.40	0.47
Contact Length	L	0.50	0.60	0.75
Contact-to-Exposed Pad	K	0.20	–	–
Model Draft Angle Top	ϕ	–	–	12°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Dimensioning and tolerancing per ASME Y14.5M.

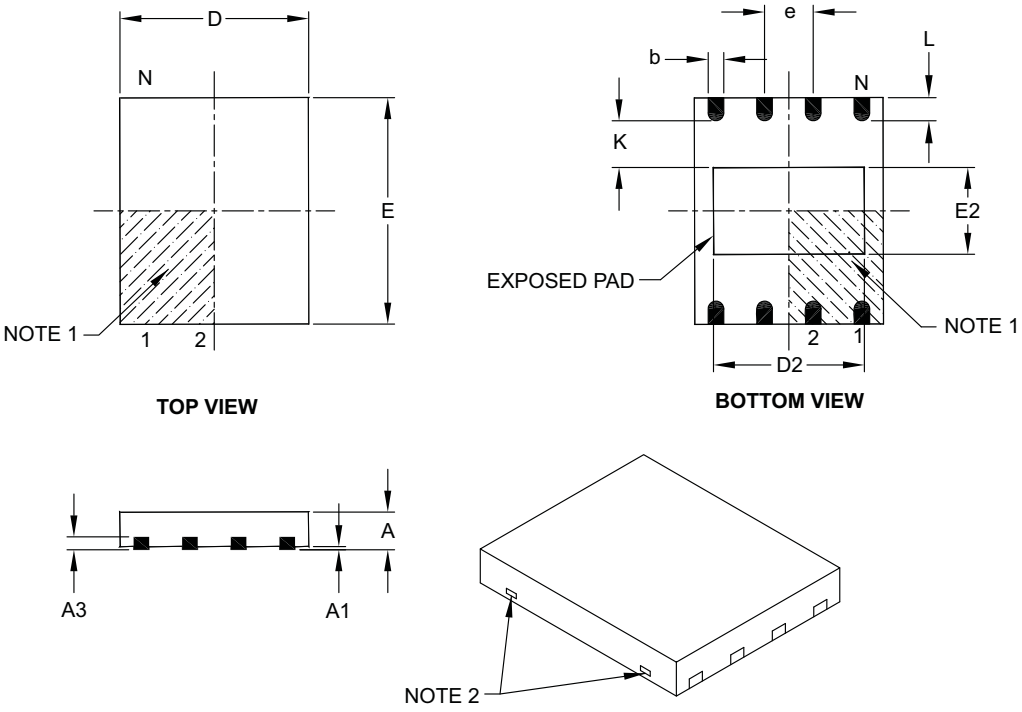
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-113B

© 2007-2015 Microchip Technology Inc.
深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

8-Lead Plastic Dual Flat, No Lead Package (MF) – 6x5 mm Body [DFN-S]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	0.80	0.85	1.00
Standoff	A1	0.00	0.01	0.05
Contact Thickness	A3		0.20 REF	
Overall Length	D		5.00 BSC	
Overall Width	E		6.00 BSC	
Exposed Pad Length	D2	3.90	4.00	4.10
Exposed Pad Width	E2	2.20	2.30	2.40
Contact Width	b	0.35	0.40	0.48
Contact Length	L	0.50	0.60	0.75
Contact-to-Exposed Pad	K	0.20	–	–

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated.
4. Dimensioning and tolerancing per ASME Y14.5M.

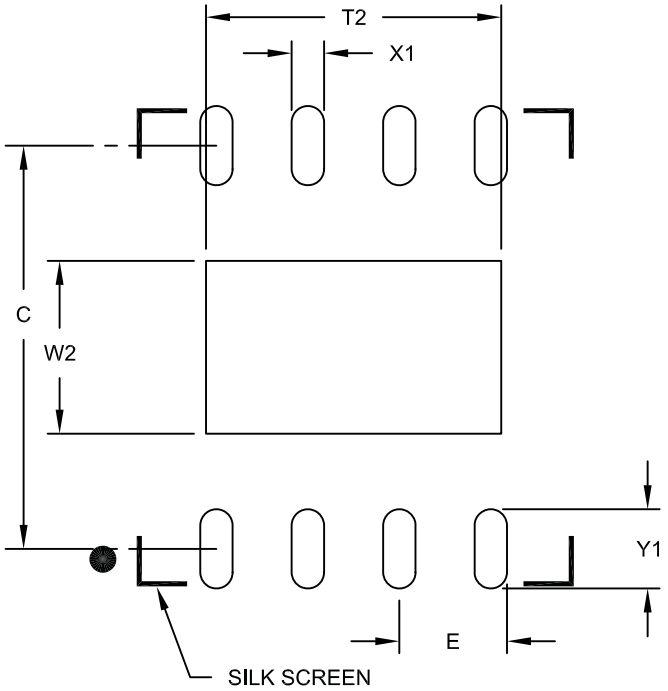
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-122B

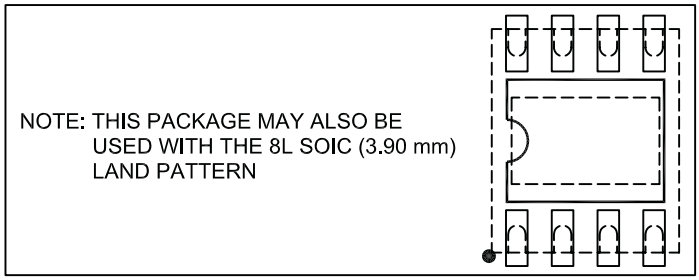
深圳市满度科技有限公司 Tel:150-1290-5940
Web:www.manduic.com Email:sales@manduic.com

8-Lead Plastic Dual Flat, No Lead Package (MF) - 6x5 mm Body [DFN-S]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Optional Center Pad Width	W2			2.40
Optional Center Pad Length	T2			4.10
Contact Pad Spacing	C		5.60	
Contact Pad Width (X8)	X1			0.45
Contact Pad Length (X8)	Y1			1.10

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

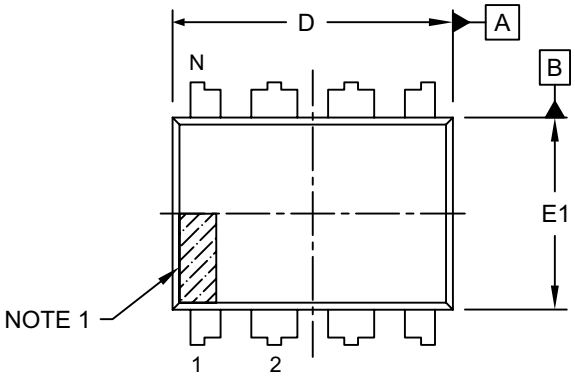
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2122A

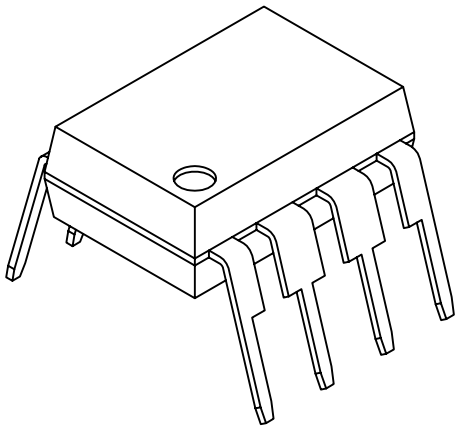
© 2007-2015 Microchip Technology Inc.
深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

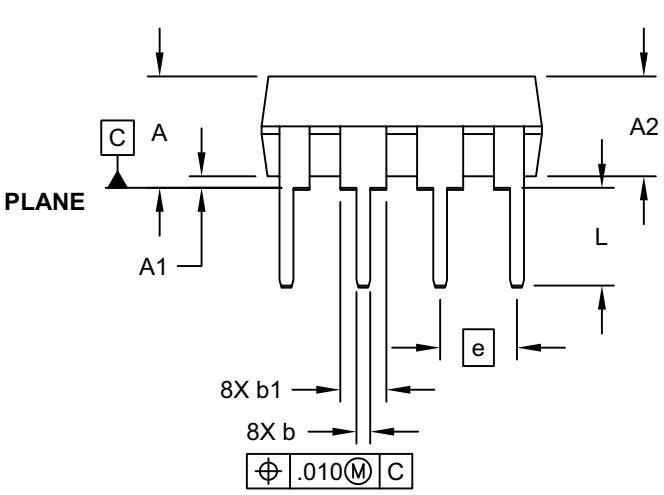
8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

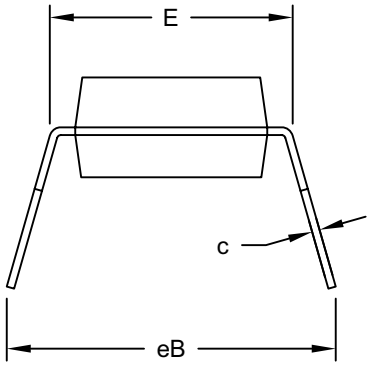


TOP VIEW





SIDE VIEW



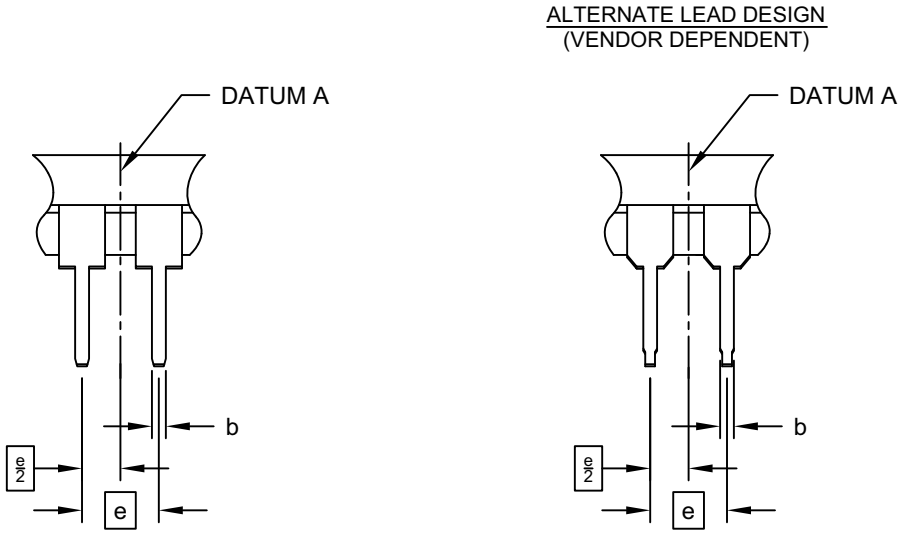
END VIEW

Microchip Technology Drawing No. C04-018D Sheet 1 of 2

深圳市满度科技有限公司 Tel:150-1290-5940
Web:www.manduic.com Email:sales@manduic.com

8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		.100 BSC	
Top to Seating Plane	A	-	-	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	-	-
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.348	.365	.400
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	-	-	.430

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M

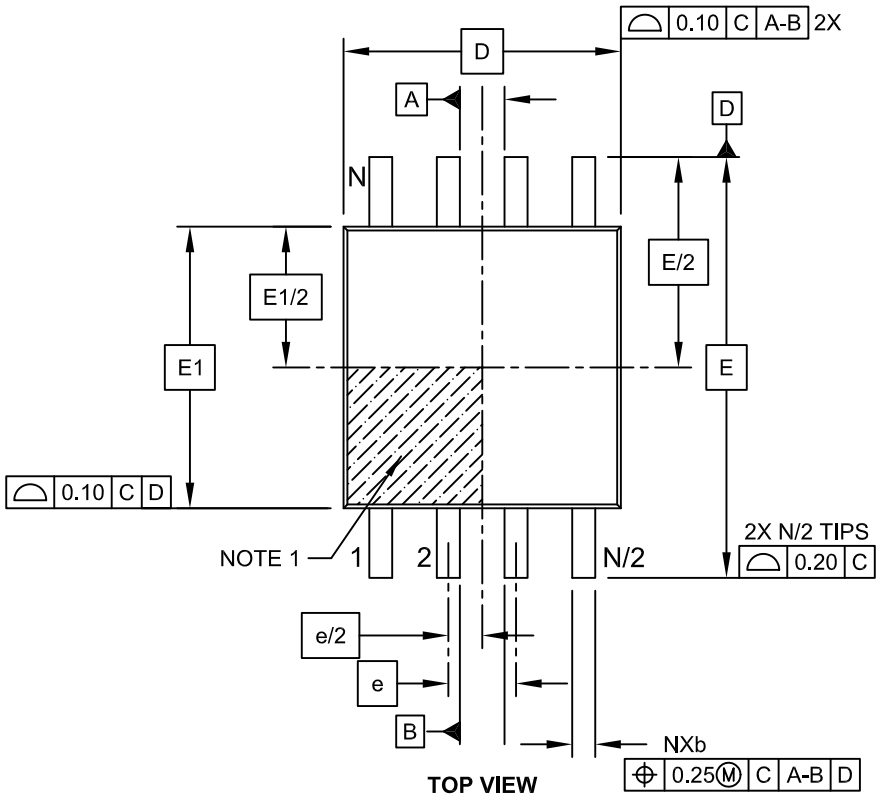
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

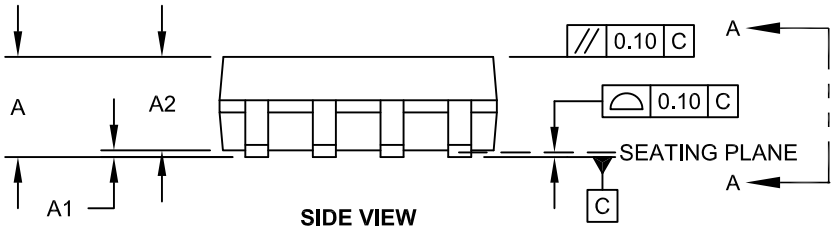
Microchip Technology Drawing No. C04-018D Sheet 2 of 2

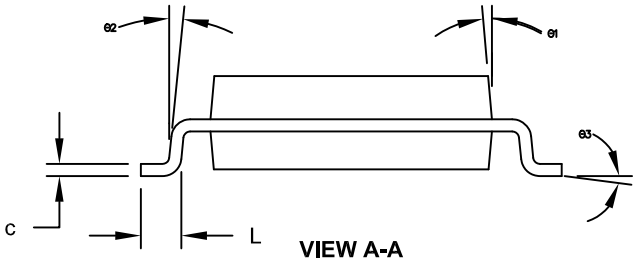
© 2007-2015 Microchip Technology Inc.
深圳市满度科技有限公司
Tel:150-1290-5940
Web:www.manduic.com
Email:sales@manduic.com

8-Lead Plastic Small Outline (SM) - Medium, 5.28 mm Body [SOIJ]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





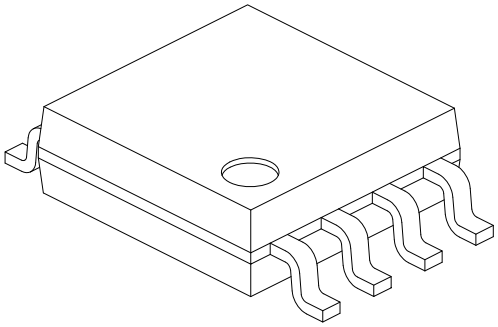


Microchip Technology Drawing C04-056C Sheet 1 of 2

深圳市满度科技有限公司 Tel:150-1290-5940
Web:www.manduic.com Email:sales@manduic.com

8-Lead Plastic Small Outline (SM) - Medium, 5.28 mm Body [SOIJ]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	1.77	-	2.03
Standoff §	A1	0.05		0.25
Molded Package Thickness	A2	1.75	-	1.98
Overall Width	E		7.94 BSC	
Molded Package Width	E1		5.25 BSC	
Overall Length	D		5.26 BSC	
Foot Length	L	0.51	-	0.76
Lead Thickness	c	0.15	-	0.25
Lead Width	b	0.36	-	0.51
Mold Draft Angle	Θ1	-	-	15°
Lead Angle	Θ2	0°	-	8°
Foot Angle	Θ3	0°	-	8°

Notes:

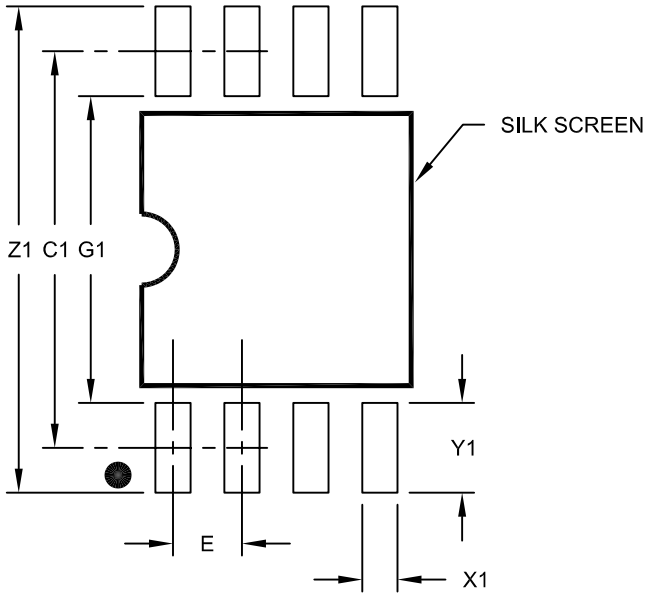
1. SOIJ, JEITA/EIAJ Standard, Formerly called SOIC
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.

Microchip Technology Drawing No. C04-056C Sheet 2 of 2

© 2007-2015 Microchip Technology Inc.
深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

8-Lead Plastic Small Outline (SM) - Medium, 5.28 mm Body [SOIJ]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Overall Width	Z1			9.00
Contact Pad Spacing	C1		7.30	
Contact Pad Width (X8)	X1			0.65
Contact Pad Length (X8)	Y1			1.70
Distance Between Pads	G1	5.60		
Distance Between Pads	G	0.62		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2056C

深圳市满度科技有限公司 Tel:150-1290-5940
Web:www.manduic.com Email:sales@manduic.com

APPENDIX A: REVISION HISTORY

Revision C (02/2007)

Revised Features Section (Self-timed Erase and Write Cycles); Revised Table 1-1 (parameters D012 and D13); Table 1-2 (parameters 20-24); Revised Package Marking Information; Replaced Package Drawings; Revised Product ID System Section (SM package); Changed PICmicro to PIC.

Revision D (07/2007)

Revised Features; Revised Tables 1-1 and 1-2 (added Industrial temp. and revised parameters 22-23); Replaced Package Drawings (Rev. AP); Revised Product ID System; Changed Flash to EEPROM.

Revision E (10/2007)

Removed 25LC1024 part number; New data sheet created for 25LC1024 (DS22064); Revised Tables; Updates throughout.

Revision F (05/2008)

Modified parameter D006 in Table 1-1; Revised Package Marking Information; Replaced Package Drawings.

Revision G (01/2010)

Added 8-Lead (MF) DFN-S Land Pattern; Replaced 8-Lead (SM) SOIJ Land Pattern.

Revision H (05/2010)

Revised Table 1-2, Param. No 25 Conditions; Revised Section 2.2; Added note.

Revision J (04/2015)

Corrected Features section; Revised Table 1-2, updated ‘Conditions’; Revised Figure 2-12, added parameter TREL; Revised Section 2-12, clarified condition for existing Deep Power-Down mode.

© 2007-2015 Microchip Technology Inc.
深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

THE MICROCHIP WEB SITE

Microchip provides online support via our web site at www.microchip.com. This web site is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the web site contains the following information:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQ), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

CUSTOMER CHANGE NOTIFICATION SERVICE

Microchip's customer notification service helps keep customers current on Microchip products. Subscribers will receive e-mail notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, access the Microchip web site at www.microchip.com. Under "Support", click on "Customer Change Notification" and follow the registration instructions.

CUSTOMER SUPPORT

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support

Customers should contact their distributor, representative or Field Application Engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

Technical support is available through the web site at: http://www.microchip.com/support

深圳市满度科技有限公司 Tel:150-1290-5940
Web:www.manduic.com Email:sales@manduic.com

NOTES:

© 2007-2015 Microchip Technology Inc.
深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	[X](1)	X	/XX
Device	Tape and Reel Option	Temperature Range	Package

Device:	25AA1024		1 Mbit, 1.8V, 256-Byte Page SPI Serial EEPROM
Tape & Reel Option:	Blank T	= =	Standard packaging (tube) Tape & Reel
Temperature Range:	I	=	-40°C to+85°C
Package:	MF P SM	= = =	Micro Lead Frame (6 x 5 mm body), 8-lead Plastic DIP (300 mil body), 8-lead Plastic SOIJ (5.28 mm), 8-lead

Examples:

a) 25AA1024T-I/SM = 1 Mbit, 1.8V Serial EEPROM, Industrial temp., Tape & Reel, SOIJ package

b) 25AA1024T-I/MF = 1 Mbit, 1.8V Serial EEPROM, Industrial temp., Tape & Reel, DFN package

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

深圳市满度科技有限公司 Tel:150-1290-5940
Web:www.manduic.com Email:sales@manduic.com

NOTES:

© 2007-2015 Microchip Technology Inc.
深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE**.** Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights.

Trademarks

The Microchip name and logo, the Microchip logo, dsPIC, FlashFlex, flexPWR, JukeBlox, KEELOQ, KEELOQ logo, Kleer, LANCheck, MediaLB, MOST, MOST logo, MPLAB, OptoLyzer, PIC, PICSTART, PIC^{32} logo, RightTouch, SpyNIC, SST, SST Logo, SuperFlash and UNI/O are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

The Embedded Control Solutions Company and mTouch are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Analog-for-the-Digital Age, BodyCom, chipKIT, chipKIT logo, CodeGuard, dsPICDEM, dsPICDEM.net, ECAN, In-Circuit Serial Programming, ICSP, Inter-Chip Connectivity, KleerNet, KleerNet logo, MiWi, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, MultiTRAK, NetDetach, Omniscient Code Generation, PICDEM, PICDEM.net, PICkit, PICtail, RightTouch logo, REAL ICE, SQI, Serial Quad I/O, Total Endurance, TSHARC, USBCheck, VariSense, ViewSpan, WiperLock, Wireless DNA, and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

Silicon Storage Technology is a registered trademark of Microchip Technology Inc. in other countries.

GestIC is a registered trademarks of Microchip Technology Germany II GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 2007-2015, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

ISBN: 978-1-63277-265-7

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
═ ISO/TS 16949 ═

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

深圳市满度科技有限公司 Tel:150-1290-5940
Web:www.manduic.com Email:sales@manduic.com

Worldwide Sales and Service

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
http://www.microchip.com/support
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Austin, TX
Tel: 512-257-3370

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Cleveland
Independence, OH
Tel: 216-447-0464
Fax: 216-447-0643

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Novi, MI
Tel: 248-848-4000

Houston, TX
Tel: 281-894-5983

Indianapolis
Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608

New York, NY
Tel: 631-435-6000

San Jose, CA
Tel: 408-735-9110

Canada - Toronto
Tel: 905-673-0699
Fax: 905-673-6509

ASIA/PACIFIC

Asia Pacific Office
Suites 3707-14, 37th Floor
Tower 6, The Gateway
Harbour City, Kowloon
Hong Kong
Tel: 852-2943-5100
Fax: 852-2401-3431

Australia - Sydney
Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing
Tel: 86-10-8569-7000
Fax: 86-10-8528-2104

China - Chengdu
Tel: 86-28-8665-5511
Fax: 86-28-8665-7889

China - Chongqing
Tel: 86-23-8980-9588
Fax: 86-23-8980-9500

China - Dongguan
Tel: 86-769-8702-9880

China - Hangzhou
Tel: 86-571-8792-8115
Fax: 86-571-8792-8116

China - Hong Kong SAR
Tel: 852-2943-5100
Fax: 852-2401-3431

China - Nanjing
Tel: 86-25-8473-2460
Fax: 86-25-8473-2470

China - Qingdao
Tel: 86-532-8502-7355
Fax: 86-532-8502-7205

China - Shanghai
Tel: 86-21-5407-5533
Fax: 86-21-5407-5066

China - Shenyang
Tel: 86-24-2334-2829
Fax: 86-24-2334-2393

China - Shenzhen
Tel: 86-755-8864-2200
Fax: 86-755-8203-1760

China - Wuhan
Tel: 86-27-5980-5300
Fax: 86-27-5980-5118

China - Xian
Tel: 86-29-8833-7252
Fax: 86-29-8833-7256

ASIA/PACIFIC

China - Xiamen
Tel: 86-592-2388138
Fax: 86-592-2388130

China - Zhuhai
Tel: 86-756-3210040
Fax: 86-756-3210049

India - Bangalore
Tel: 91-80-3090-4444
Fax: 91-80-3090-4123

India - New Delhi
Tel: 91-11-4160-8631
Fax: 91-11-4160-8632

India - Pune
Tel: 91-20-3019-1500

Japan - Osaka
Tel: 81-6-6152-7160
Fax: 81-6-6152-9310

Japan - Tokyo
Tel: 81-3-6880- 3770
Fax: 81-3-6880-3771

Korea - Daegu
Tel: 82-53-744-4301
Fax: 82-53-744-4302

Korea - Seoul
Tel: 82-2-554-7200
Fax: 82-2-558-5932 or
82-2-558-5934

Malaysia - Kuala Lumpur
Tel: 60-3-6201-9857
Fax: 60-3-6201-9859

Malaysia - Penang
Tel: 60-4-227-8870
Fax: 60-4-227-4068

Philippines - Manila
Tel: 63-2-634-9065
Fax: 63-2-634-9069

Singapore
Tel: 65-6334-8870
Fax: 65-6334-8850

Taiwan - Hsin Chu
Tel: 886-3-5778-366
Fax: 886-3-5770-955

Taiwan - Kaohsiung
Tel: 886-7-213-7828

Taiwan - Taipei
Tel: 886-2-2508-8600
Fax: 886-2-2508-0102

Thailand - Bangkok
Tel: 66-2-694-1351
Fax: 66-2-694-1350

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4450-2828
Fax: 45-4485-2829

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Dusseldorf
Tel: 49-2129-3766400

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Germany - Pforzheim
Tel: 49-7231-424750

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Italy - Venice
Tel: 39-049-7625286

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Poland - Warsaw
Tel: 48-22-3325737

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

Sweden - Stockholm
Tel: 46-8-5090-4654

UK - Wokingham
Tel: 44-118-921-5800
Fax: 44-118-921-5820

01/27/15

© 2007-2015 Microchip Technology Inc.
深圳市满度科技有限公司 Tel:150-1290-5940
Web:www.manduic.com Email:sales@manduic.com