24AA64/24LC64

64K I²C™ Serial EEPROM

Device Selection Table

Part Number	Vcc Range	Max Clock Frequency	Temp Ranges
24AA64	1.8-5.5	400 kHz(1)	I
24LC64	2.5-5.5	400 kHz	I, E

Note 1: 100 kHz for Vcc <2.5V

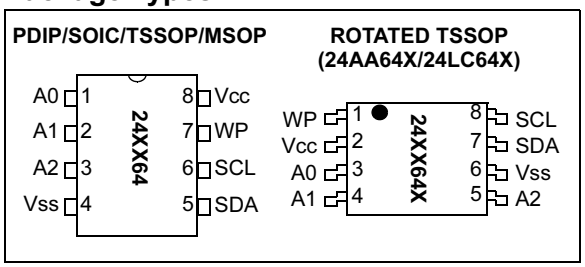
Features

- Single supply with operation down to 1.8V
- Low power CMOS technology
  - 1 mA active current typical
  - 1 µA standby current (max.) (I-temp)
- Organized as 8 blocks of 8K bit (64K bit)
- 2-wire serial interface bus, I²C™ compatible
- Cascadable for up to eight devices
- Schmitt Trigger inputs for noise suppression
- Output slope control to eliminate ground bounce
- 100 kHz (24AA64) and 400 kHz (24LC64) compatibility
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 32 bytes
- 2 ms typical write cycle time for page-write
- Hardware write protect for entire memory
- Can be operated as a serial ROM
- Factory programming (QTP) available
- ESD protection > 4,000V
- 1,000,000 erase/write cycles
- Data retention > 200 years
- 8-lead PDIP, SOIC, TSSOP, and MSOP package
- Available temperature ranges:
  - Industrial (I): -40°C to +85°C
  - Automotive (E): -40°C to +125°C

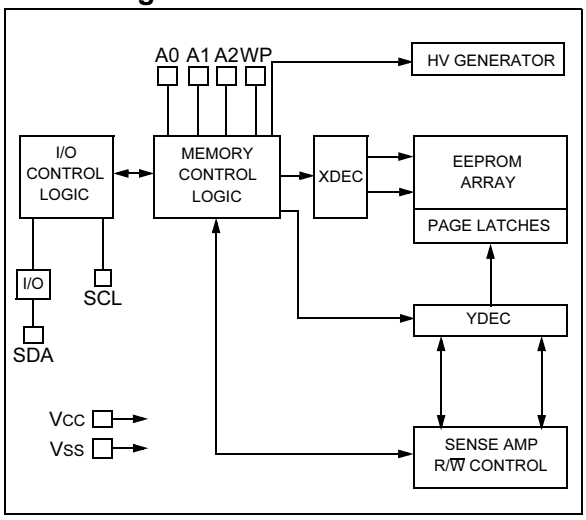
Description

The Microchip Technology Inc. 24AA64/24LC64 (24XX64*) is a 64 Kbit Electrically Erasable PROM. The device is organized as eight blocks of 1K x 8-bit memory with a 2-wire serial interface. Low voltage design permits operation down to 1.8V with standby and active currents of only 1 µA and 1 mA respectively. It has been developed for advanced, low power applications such as personal communications or data acquisition. The 24XX64 also has a page-write capability for up to 32 bytes of data. Functional address lines allow up to eight devices on the same bus, for up to 512 Kbits address space. The 24XX64 is available in the standard 8-pin PDIP, surface mount SOIC, TSSOP and MSOP packages.

Package Types



Block Diagram



*24XX64 is used in this document as a generic part number for the 24AA64/24LC64 devices.

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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

VCC.....6.5V

All inputs and outputs w.r.t. VSS ..... -0.3V to VCC +1.0V

Storage temperature .....-65°C to +150°C

Ambient temp. with power applied .....-40°C to +125°C

ESD protection on all pins .....≥ 4 kV

† NOTICE: Stresses above those listed under “Maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

1.1 DC Characteristics

DC CHARACTERISTICS			VCC = +1.8V to +5.5V Industrial (I): TAMB = -40°C to +85°C Automotive (E): TAMB = -40°C to +125°C				
Param. No.	**Sym**	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
D1	VIH	**WP, SCL and SDA pins**	—	—	—	—	—
D2	—	High level input voltage	0.7 VCC	—	—	V	—
D3	VIL	Low level input voltage	—	—	0.3 VCC	V	—
D4	VHYS	Hysteresis of Schmitt Trigger inputs	0.05 VCC	—	—	V	**(Note 1)**
D5	VOL	Low level output voltage	—	—	0.40	V	IOL = 3.0 mA, VCC = 2.5V
D6	ILI	**Input leakage current**	—	—	±10	µA	VIN =.1V to VCC
D7	ILO	**Output leakage current**	—	—	±10	µA	VOUT =.1V to VCC
D8	CIN, COUT	Pin capacitance (all inputs/outputs)	—	—	10	pF	VCC = 5.0V **(Note 1)** TAMB = 25°C, FCLK = 1 MHz
D9	ICC write	**Operating current**	—	0.1	3	mA	VCC = 5.5V, SCL = 400 kHz
D10	ICC read		—	0.05	1	mA	—
D11	ICCS	**Standby current**	— —	.01 —	1 5	µA µA	Industrial Automotive SDA = SCL = VCC WP = VSS

Note 1: This parameter is periodically sampled and not 100% tested.

2: Typical measurements taken at room temperature.

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1.2 AC Characteristics

AC CHARACTERISTICS			V_{CC} = +1.8V to +5.5V Industrial (I): T_{AMB} = -40°C to +85°C Automotive (E): T_{AMB} = -40°C to +125°C			
Param. No.	**Sym**	**Characteristic**	**Min**	**Max**	**Units**	**Conditions**
1	F_{CLK}	Clock frequency	— —	400 100	kHz	2.5V ≤ V_{CC} ≤ 5.5V 1.8V ≤ V_{CC} < 2.5V (24AA64)
2	T_{HIGH}	Clock high time	600 4000	— —	ns	2.5V ≤ V_{CC} ≤ 5.5V 1.8V ≤ V_{CC} < 2.5V (24AA64)
3	T_{LOW}	Clock low time	1300 4700	— —	ns	2.5V ≤ V_{CC} ≤ 5.5V 1.8V ≤ V_{CC} < 2.5V (24AA64)
4	T_R	SDA and SCL rise time **(Note 1)**	— —	300 1000	ns	2.5V ≤ V_{CC} ≤ 5.5V 1.8V ≤ V_{CC} < 2.5V (24AA64)
5	T_F	SDA and SCL fall time	—	300	ns	**(Note 1)**
6	$T_{HD:STA}$	START condition hold time	600 4000	— —	ns	2.5V ≤ V_{CC} ≤ 5.5V 1.8V ≤ V_{CC} < 2.5V (24AA64)
7	$T_{SU:STA}$	START condition setup time	600 4700	— —	ns	2.5V ≤ V_{CC} ≤ 5.5V 1.8V ≤ V_{CC} < 2.5V (24AA64)
8	$T_{HD:DAT}$	Data input hold time	0	—	ns	**(Note 2)**
9	$T_{SU:DAT}$	Data input setup time	100 250	— —	ns	2.5V ≤ V_{CC} ≤ 5.5V 1.8V ≤ V_{CC} < 2.5V (24AA64)
10	$T_{SU:STO}$	STOP condition setup time	600 4000	— —	ns	2.5V ≤ V_{CC} ≤ 5.5V 1.8V ≤ V_{CC} < 2.5V (24AA64)
11	T_{AA}	Output valid from clock **(Note 2)**	— —	900 3500	ns	2.5V ≤ V_{CC} ≤ 5.5V 1.8V ≤ V_{CC} < 2.5V (24AA64)
12	T_{BUF}	Bus free time: Time the bus must be free before a new transmission can start	1300 4700	— —	ns	2.5V ≤ V_{CC} ≤ 5.5V 1.8V ≤ V_{CC} < 2.5V (24AA64)
13	T_{OF}	Output fall time from V_{IH} minimum to V_{IL} maximum	20+0.1C_B —	250 250	ns	2.5V ≤ V_{CC} ≤ 5.5V 1.8V ≤ V_{CC} ≤ 2.5V (24AA64)
14	T_{SP}	Input filter spike suppression (SDA and SCL pins)	—	50	ns	**(Notes 1 and 3)**
15	T_{WC}	Write cycle time (byte or page)	—	5	ms	—
16	—	Endurance	1M	—	cycles	25°C, V_{CC} = 5.0V, Block Mode **(Note 4)**

Note 1: Not 100% tested. C_B = total capacitance of one bus line in pF.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

3: The combined T_{SP} and V_{HYS} specifications are due to new Schmitt Trigger inputs which provide improved noise spike suppression. This eliminates the need for a T_I specification for standard operation.

4: This parameter is not tested but ensured by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on Microchip's website: www.microchip.com.

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FIGURE 1-1: BUS TIMING DATA

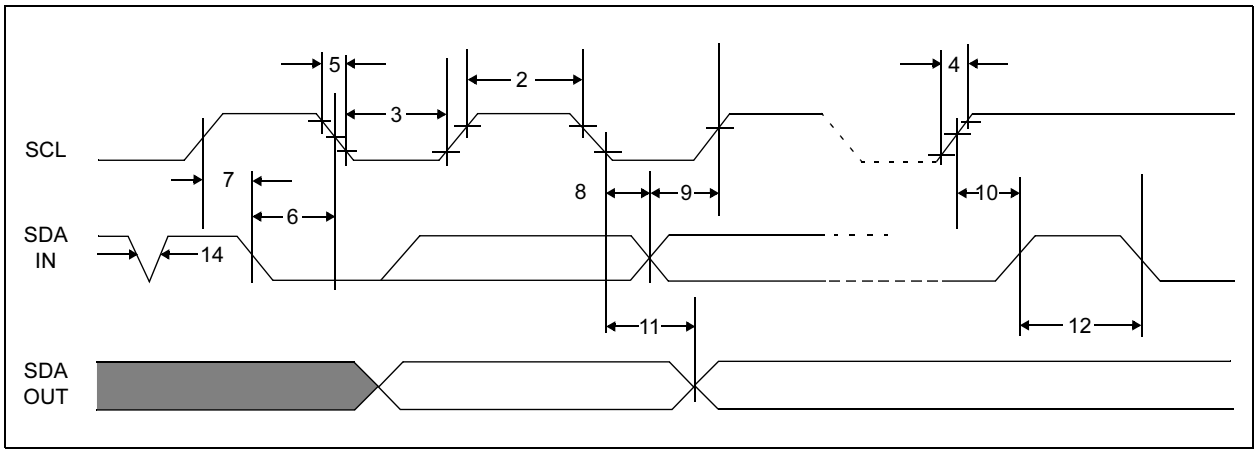
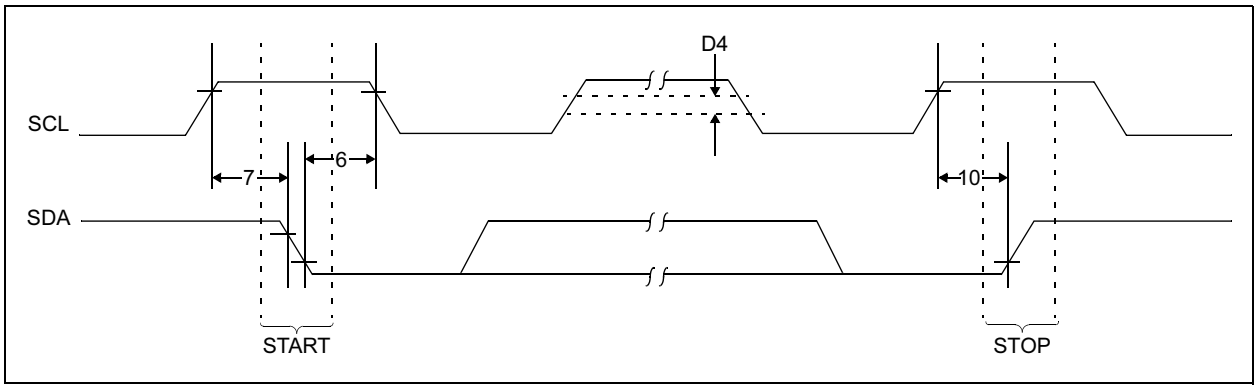


FIGURE 1-2: BUS TIMING START/STOP



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2.0 FUNCTIONAL DESCRIPTION

The 24XX64 supports a bi-directional 2-wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access and generates the START and STOP conditions, while the 24XX64 works as slave. Both master and slave can operate as transmitter or receiver, but the master device determines which mode is activated.

3.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (Figure 3-1).

3.1 Bus not Busy (A)

Both data and clock lines remain HIGH.

3.2 Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

3.3 Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

3.4 Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited, although only the last sixteen will be stored when doing a write operation. When an overwrite does occur it will replace data in a first-in first-out (FIFO) fashion.

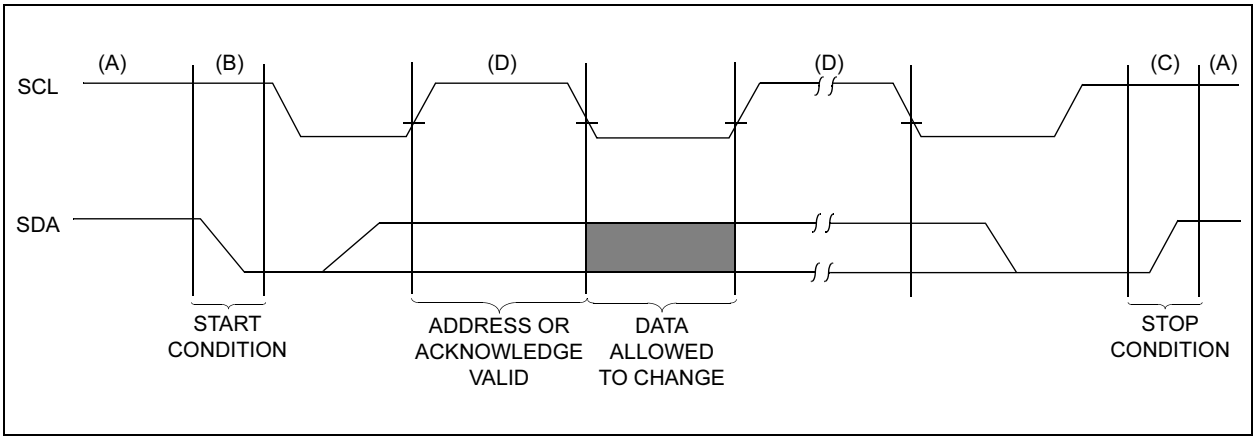
3.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this Acknowledge bit.

Note:	The 24XX64 does not generate any Acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges, has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. During reads, a master must signal an end of data to the slave by not generating an Acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave (24XX64) will leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 3-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS



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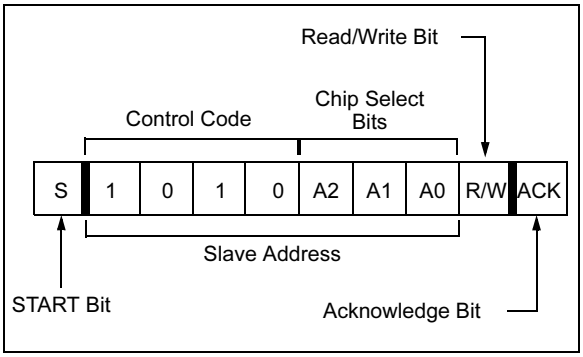
3.6 Device Addressing

A control byte is the first byte received following the START condition from the master device (Figure 3-2). The control byte consists of a four bit control code; for the 24XX64 this is set as 1010 binary for read and write operations. The next three bits of the control byte are the chip select bits (A2, A1, A0). The chip select bits allow the use of up to eight 24XX64 devices on the same bus and are used to select which device is accessed. The chip select bits in the control byte must correspond to the logic levels on the corresponding A2, A1, and A0 pins for the device to respond. These bits are in effect the three Most Significant bits of the word address.

The last bit of the control byte defines the operation to be performed. When set to a one a read operation is selected, and when set to a zero a write operation is selected. The next two bytes received define the address of the first data byte (Figure 3-3). Because only A12...A0 are used, the upper three address bits are don't care bits. The upper address bits are transferred first, followed by the less significant bits.

Following the START condition, the 24XX64 monitors the SDA bus checking the device type identifier being transmitted. Upon receiving a 1010 code and appropriate device select bits, the slave device outputs an Acknowledge signal on the SDA line. Depending on the state of the R/$\overline{W}$ bit, the 24XX64 will select a read or write operation.

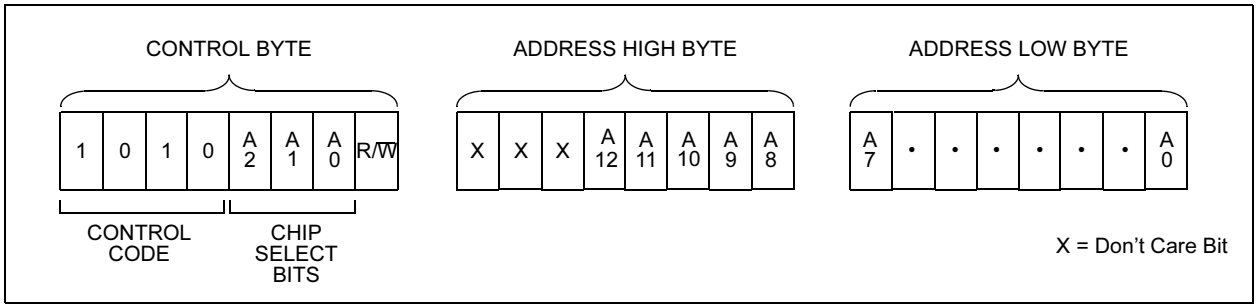
FIGURE 3-2: CONTROL BYTE FORMAT



3.7 Contiguous Addressing Across Multiple Devices

The chip select bits A2, A1, A0 can be used to expand the contiguous address space for up to 512K bits by adding up to eight 24XX64's on the same bus. In this case, software can use A0 of the control byte as address bit A13, A1 as address bit A14, and A2 as address bit A15. It is not possible to sequentially read across device boundaries.

FIGURE 3-3: ADDRESS SEQUENCE BIT ASSIGNMENTS



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4.0 WRITE OPERATIONS

4.1 Byte Write

Following the START condition from the master, the control code (four bits), the chip select (three bits), and the R/$\overline{W}$ bit (which is a logic low) are clocked onto the bus by the master transmitter. This indicates to the addressed slave receiver that the address high byte will follow after it has generated an Acknowledge bit during the ninth clock cycle. Therefore, the next byte transmitted by the master is the high-order byte of the word address and will be written into the address pointer of the 24XX64. The next byte is the Least Significant Address Byte. After receiving another Acknowledge signal from the 24XX64 the master device will transmit the data word to be written into the addressed memory location. The 24XX64 acknowledges again and the master generates a STOP condition. This initiates the internal write cycle, and during this time the 24XX64 will not generate Acknowledge signals (Figure 4-1). If an attempt is made to write to the array with the WP pin held high, the device will acknowledge the command but no write cycle will occur, no data will be written and the device will immediately accept a new command. After a byte write command, the internal address counter will point to the address location following the one that was just written.

4.2 Page Write

The write control byte, word address and the first data byte are transmitted to the 24XX64 in the same way as in a byte write. But instead of generating a STOP condition, the master transmits up to 31 additional bytes which are temporarily stored in the on-chip page buffer and will be written into memory after the master has transmitted a STOP condition. After receipt of each word, the five lower address pointer bits are internally incremented by one. If the master should transmit more than 32 bytes prior to generating the STOP condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the STOP condition is received, an internal write cycle will begin (Figure 4-2). If an attempt is made to write to the array with the WP pin held high, the device will acknowledge the command but no write cycle will occur, no data will be written and the device will immediately accept a new command.

Note: Page write operations are limited to writing bytes within a single physical page, **regardless** of the number of bytes actually being written. Physical page boundaries start at addresses that are integer multiples of the page buffer size (or 'page size') and end at addresses that are integer multiples of [page size - 1]. If a page write command attempts to write across a physical page boundary, the result is that the data wraps around to the beginning of the current page (overwriting data previously stored there), instead of being written to the next page as might be expected. It is therefore necessary for the application software to prevent page write operations that would attempt to cross a page boundary.

4.3 Write Protection

The WP pin allows the user to write protect the entire array (0000-1FFF) when the pin is tied to VCC. If tied to VSS or left floating, the write protection is disabled. The WP pin is sampled at the STOP bit for every write command (Figure 3-1) Toggling the WP pin after the STOP bit will have no effect on the execution of the write cycle.

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FIGURE 4-1: BYTE WRITE

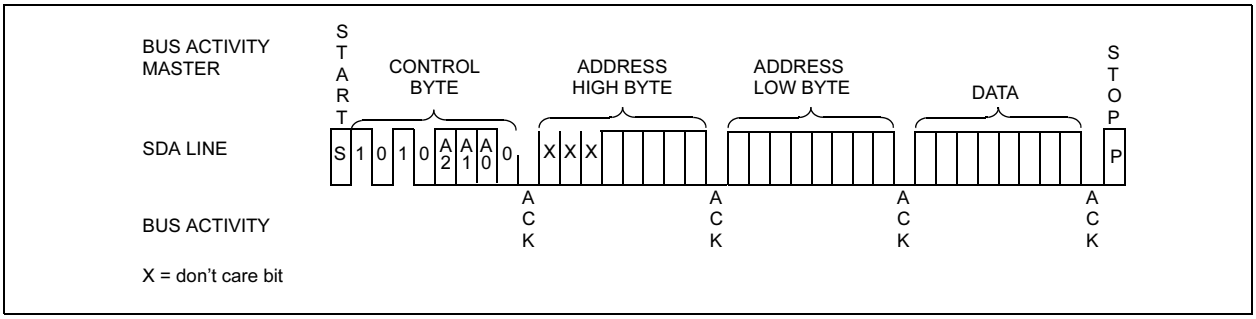
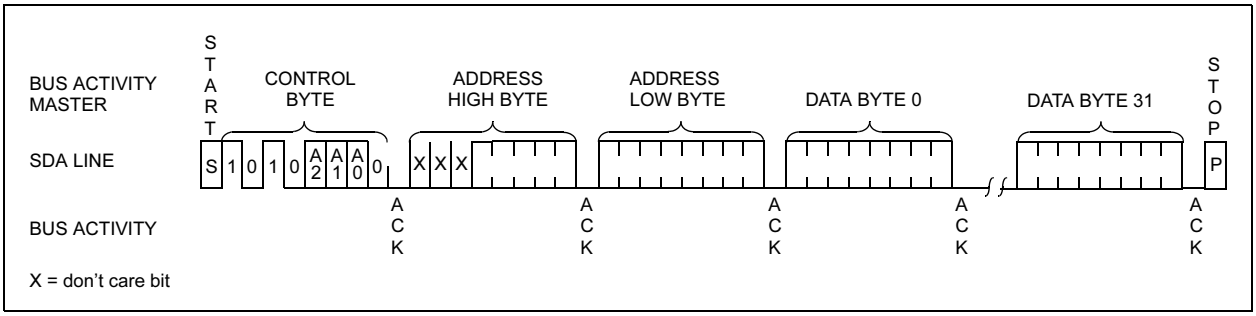


FIGURE 4-2: PAGE WRITE

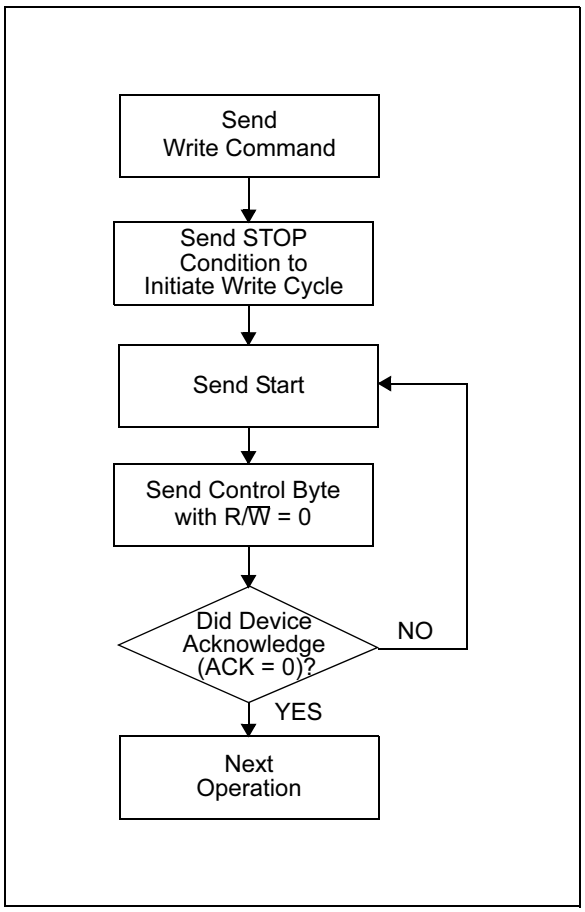


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5.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the STOP condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a START condition followed by the control byte for a write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, then no ACK will be returned. If no ACK is returned, then the START bit and control byte must be re-sent. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 5-1 for flow diagram.

FIGURE 5-1: ACKNOWLEDGE POLLING FLOW



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6.0 READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the control byte is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

6.1 Current Address Read

The 24XX64 contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous read access was to address n (n is any legal address), the next current address read operation would access data from address n + 1.

Upon receipt of the control byte with R/$\overline{W}$ bit set to one, the 24XX64 issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a STOP condition and the 24XX64 discontinues transmission (Figure 6-1).

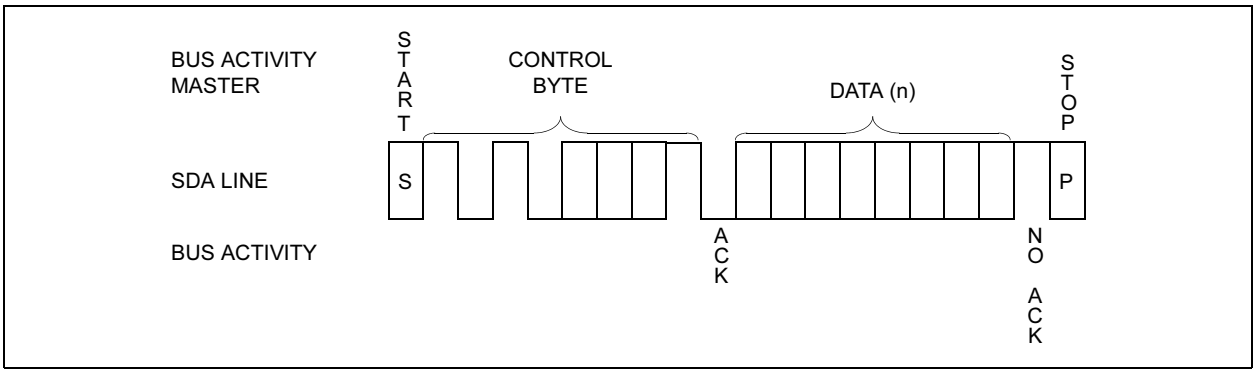
6.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24XX64 as part of a write operation (R/$\overline{W}$ bit set to 0). After the word address is sent, the master generates a START condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/$\overline{W}$ bit set to a one. The 24XX64 will then issue an acknowledge and transmit the 8-bit data word. The master will not acknowledge the transfer but does generate a STOP condition which causes the 24XX64 to discontinue transmission (Figure 6-2). After a random read command, the internal address counter will point to the address location following the one that was just read.

6.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24XX64 transmits the first data byte, the master issues an acknowledge as opposed to the STOP condition used in a random read. This acknowledge directs the 24XX64 to transmit the next sequentially addressed 8-bit word (Figure 6-3). Following the final byte transmitted to the master, the master will NOT generate an acknowledge but will generate a STOP condition. To provide sequential reads the 24XX64 contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation. The internal address pointer will automatically roll over from address 1FFF to address 0000 if the master acknowledges the byte received from the array address 1FFF.

FIGURE 6-1: CURRENT ADDRESS READ



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FIGURE 6-2: RANDOM READ

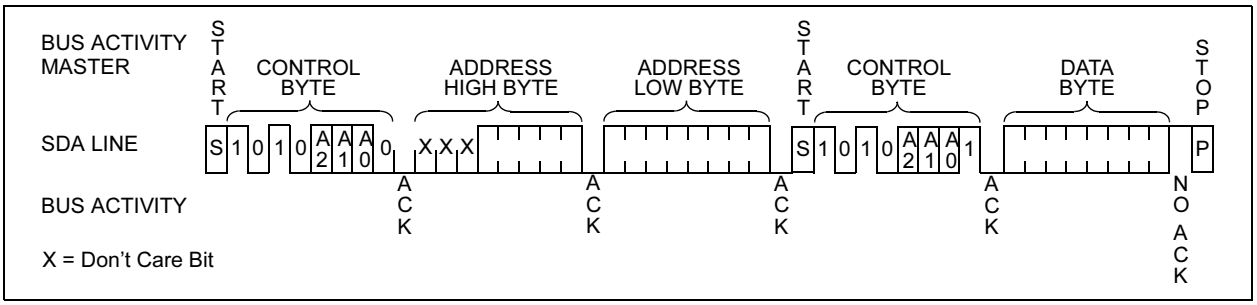
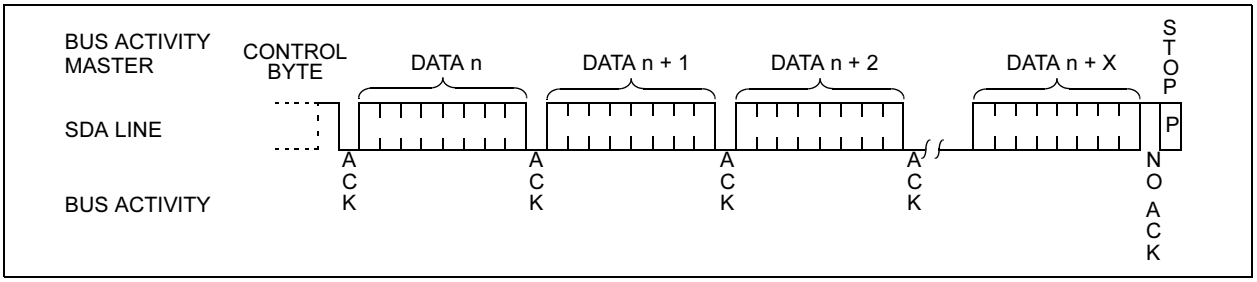


FIGURE 6-3: SEQUENTIAL READ



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7.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 7-1.

TABLE 7-1: PIN FUNCTION TABLE

Name	PDIP	SOIC	TSSOP	MSOP	ROTATED TSSOP	Description
A0	1	1	1	1	3	Chip Address Input
A1	2	2	2	2	4	Chip Address Input
A2	3	3	3	3	5	Chip Address Input
VSS	4	4	4	4	6	Ground
SDA	5	5	5	5	7	Serial Address/Data I/O
SCL	6	6	6	6	8	Serial Clock
WP	7	7	7	7	1	Write Protect Input
VCC	8	8	8	8	2	+1.8V to 5.5V Power Supply

7.1 A0, A1, A2 Chip Address Inputs

The A0, A1, A2 inputs are used by the 24XX64 for multiple device operation. The levels on these inputs are compared with the corresponding bits in the slave address. The chip is selected if the compare is true.

Up to eight devices may be connected to the same bus by using different chip select bit combinations. These inputs must be connected to either VCC or VSS.

7.2 Serial Data (SDA)

This is a bi-directional pin used to transfer addresses and data into and data out of the device. It is an open-drain terminal, therefore, the SDA bus requires a pull-up resistor to VCC (typical 10 kΩ for 100 kHz, 2 kΩ for 400 kHz)

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

7.3 Serial Clock (SCL)

This input is used to synchronize the data transfer from and to the device.

7.4 Write Protect (WP)

This pin can be connected to either VSS, VCC or left floating. An internal pull-down resistor on this pin will keep the device in the unprotected state if left floating. If tied to VSS or left floating, normal memory operation is enabled (read/write the entire memory 0000-1FFF).

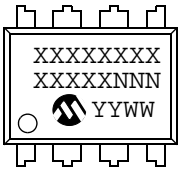
If tied to VCC, WRITE operations are inhibited. Read operations are not affected.

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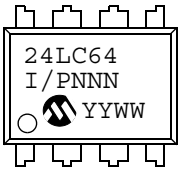
8.0 PACKAGING INFORMATION

8.1 Package Marking Information

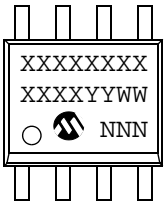
8-Lead PDIP (300 mil)



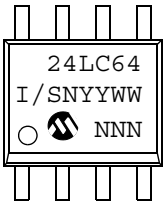
Example:



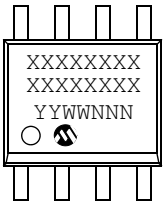
8-Lead SOIC (150 mil)



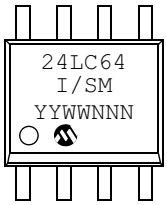
Example:



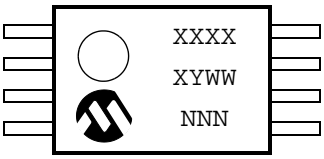
8-Lead SOIC (208 mil)



Example:

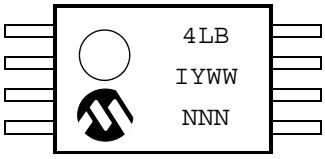


8-Lead TSSOP

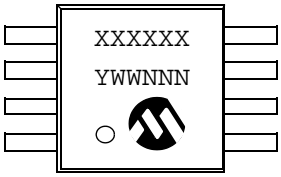


Rotated TSSOP marking will be "4LBX"

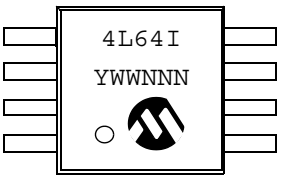
Example:



8-Lead MSOP



Example:



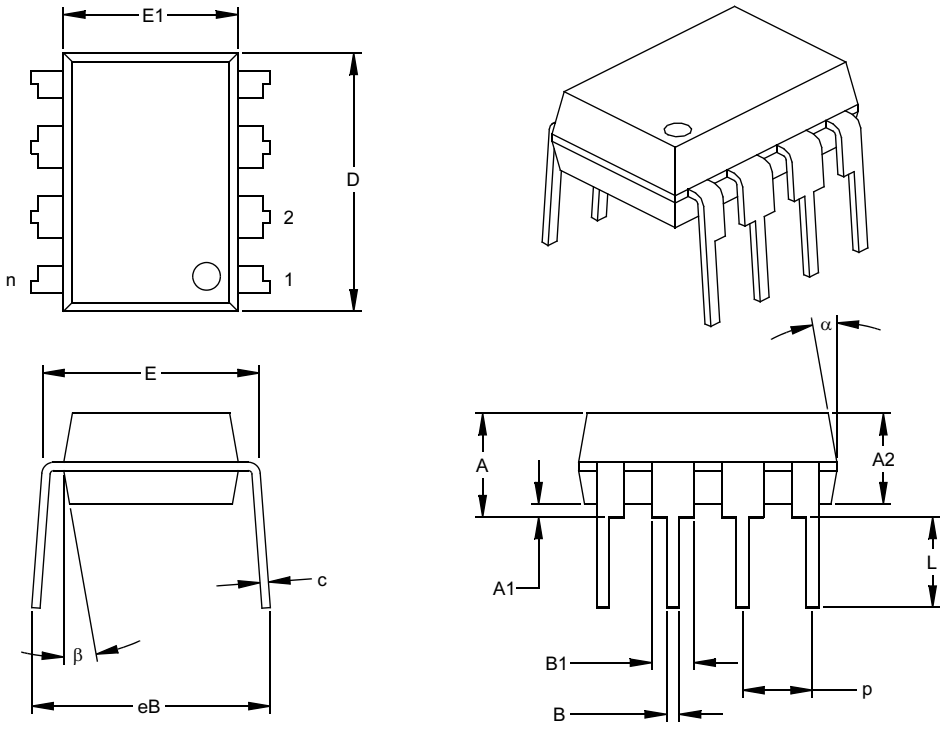
Legend:	XX...X	Customer specific information*
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

* Standard OTP marking consists of Microchip part number, year code, week code, and traceability code.

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8-Lead Plastic Dual In-line (P) – 300 mil (PDIP)



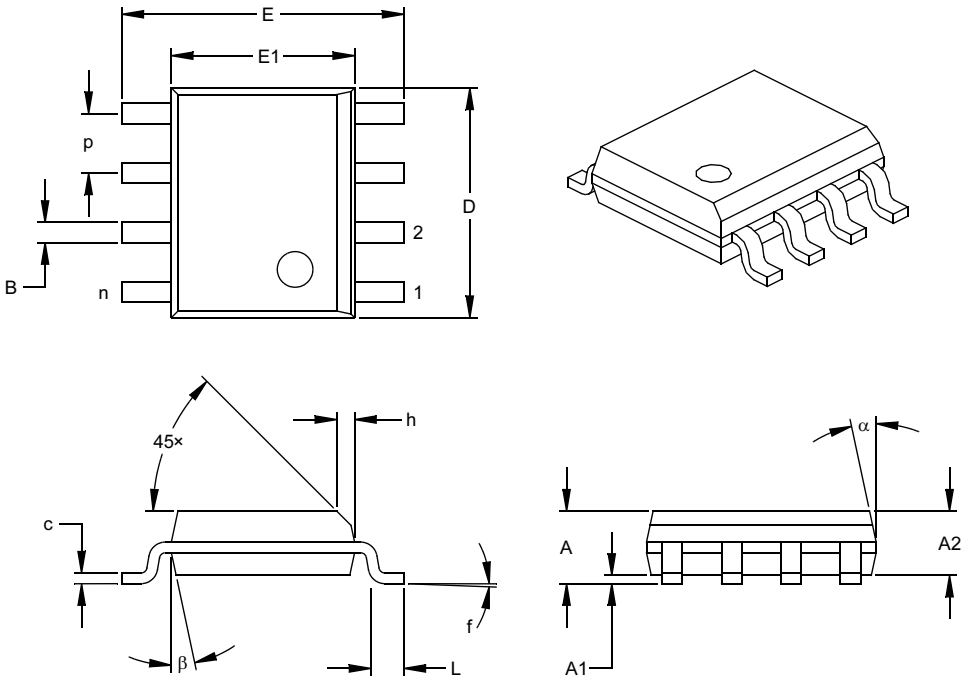
Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.360	.373	.385	9.14	9.46	9.78
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-018

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8-Lead Plastic Small Outline (SN) – Narrow, 150 mil (SOIC)



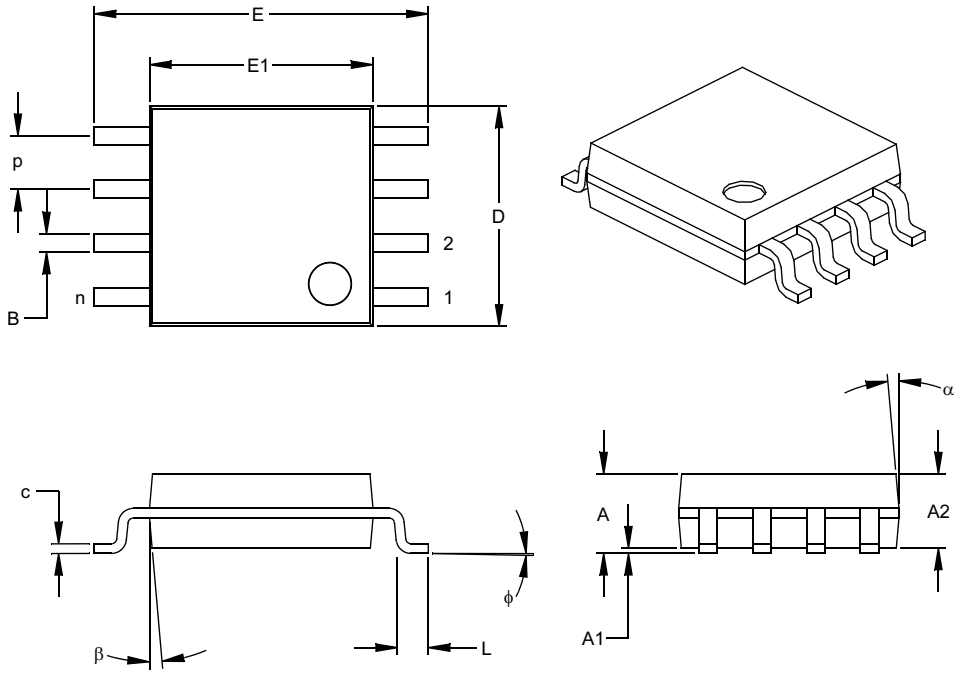
Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.019	.025	.030	0.48	0.62	0.76
Foot Angle	f	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.013	.017	.020	0.33	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-012
Drawing No. C04-057

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8-Lead Plastic Small Outline (SM) – Medium, 208 mil (SOIC)



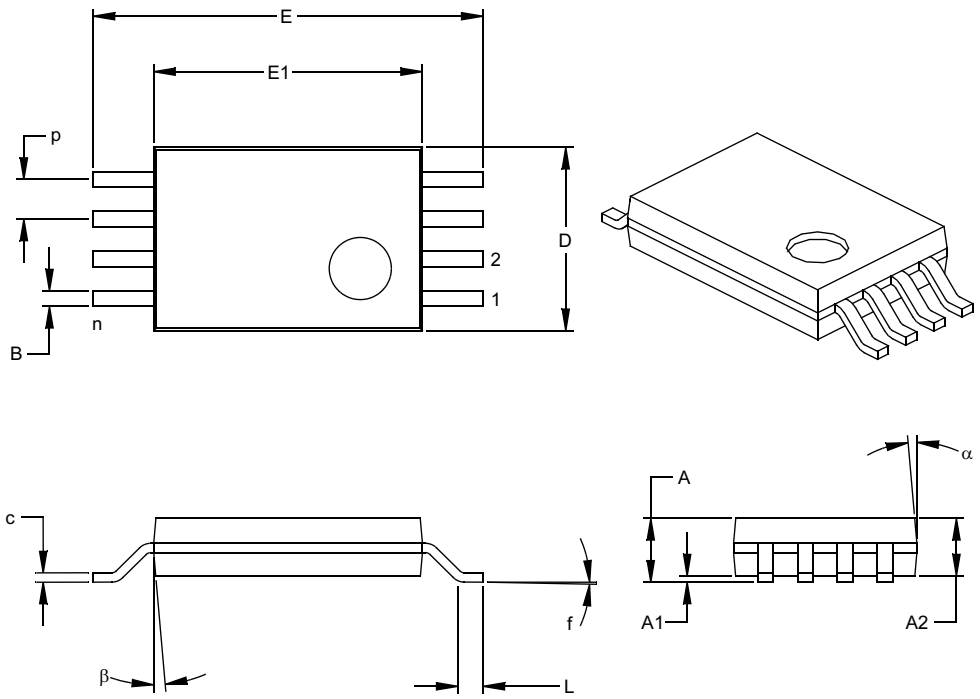
Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.070	.075	.080	1.78	1.97	2.03
Molded Package Thickness	A2	.069	.074	.078	1.75	1.88	1.98
Standoff §	A1	.002	.005	.010	0.05	0.13	0.25
Overall Width	E	.300	.313	.325	7.62	7.95	8.26
Molded Package Width	E1	.201	.208	.212	5.11	5.28	5.38
Overall Length	D	.202	.205	.210	5.13	5.21	5.33
Foot Length	L	.020	.025	.030	0.51	0.64	0.76
Foot Angle	ϕ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.014	.017	.020	0.36	0.43	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
Drawing No. C04-056

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8-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm (TSSOP)



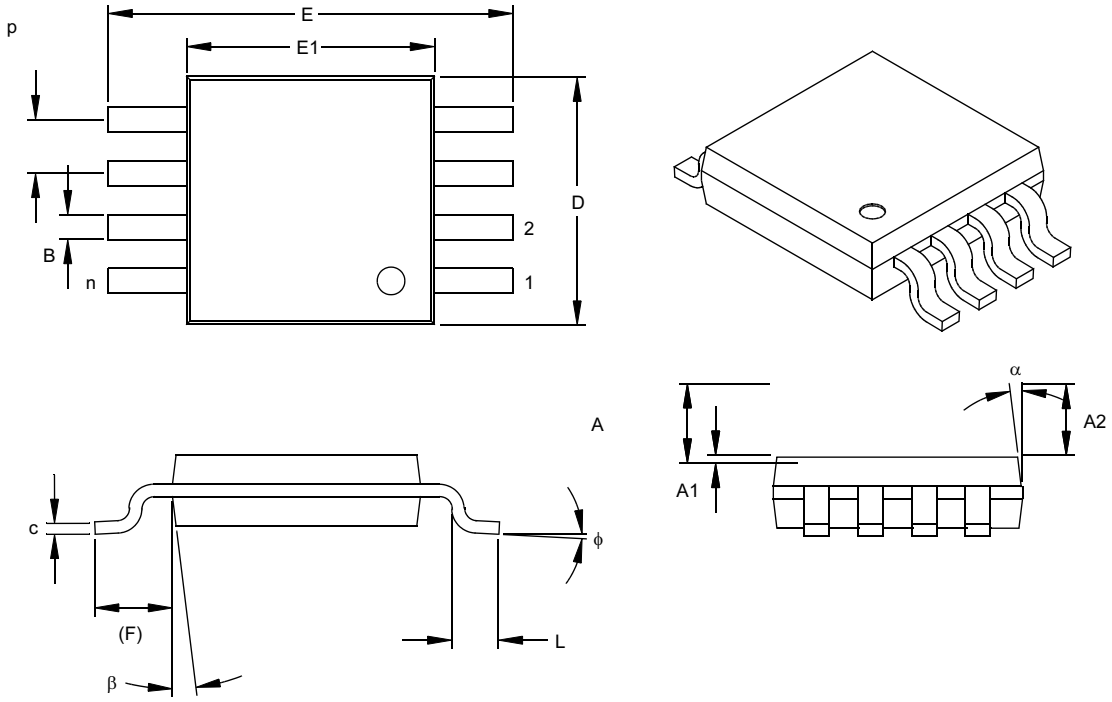
Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.026			0.65	
Overall Height	A			.043			1.10
Molded Package Thickness	A2	.033	.035	.037	0.85	0.90	0.95
Standoff §	A1	.002	.004	.006	0.05	0.10	0.15
Overall Width	E	.246	.251	.256	6.25	6.38	6.50
Molded Package Width	E1	.169	.173	.177	4.30	4.40	4.50
Molded Package Length	D	.114	.118	.122	2.90	3.00	3.10
Foot Length	L	.020	.024	.028	0.50	0.60	0.70
Foot Angle	f	0	4	8	0	4	8
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B	.007	.010	.012	0.19	0.25	0.30
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005” (0.127mm) per side.
JEDEC Equivalent: MO-153
Drawing No. C04-086

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8-Lead Plastic Micro Small Outline Package (MS) (MSOP)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8				8
Pitch	p		.026			0.65	
Overall Height	A			.044			1.18
Molded Package Thickness	A2	.030	.034	.038	0.76	0.86	0.97
Standoff §	A1	.002		.006	0.05		0.15
Overall Width	E	.184	.193	.200	4.67	4.90	.5.08
Molded Package Width	E1	.114	.118	.122	2.90	3.00	3.10
Overall Length	D	.114	.118	.122	2.90	3.00	3.10
Foot Length	L	.016	.022	.028	0.40	0.55	0.70
Footprint (Reference)	F	.035	.037	.039	0.90	0.95	1.00
Foot Angle	ϕ	0		6	0		6
Lead Thickness	c	.004	.006	.008	0.10	0.15	0.20
Lead Width	B	.010	.012	.016	0.25	0.30	0.40
Mold Draft Angle Top	α		7			7	
Mold Draft Angle Bottom	β		7			7	

*Controlling Parameter
§ Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

Drawing No. C04-111

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2. How does this document meet your hardware and software development needs?

3. Do you find the organization of this document easy to follow? If not, why?

4. What additions to the document do you think would enhance the structure and subject?

5. What deletions from the document could be made without affecting the overall usefulness?

6. Is there any incorrect or misleading information (what and where)?

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX
Device	Temperature Range	Package

Device:	24AA64:	1.8V, 64 Kbit I^2C Serial EEPROM
	24AA64T:	1.8V, 64 Kbit I^2C Serial EEPROM (Tape and Reel)
	24AA64X	1.8V, 64 Kbit I^2C Serial EEPROM in alternate pinout (ST only)
	24AA64XT	1.8V, 64 Kbit I^2C Serial EEPROM in alternate pinout (ST only)
	24LC64:	2.5V, 64 Kbit I^2C Serial EEPROM
	24LC64T:	2.5V, 64 Kbit I^2C Serial EEPROM (Tape and Reel)
	24LC64X	2.5V, 64 Kbit I^2C Serial EEPROM in alternate pinout (ST only)
	24LC64XT	2.5V, 64 Kbit I^2C Serial EEPROM in alternate pinout (ST only)
Temperature Range:	I =	-40°C to +85°C
	E =	-40°C to +125°C
Package:	P =	Plastic DIP (300 mil body), 8-lead
	SN =	Plastic SOIC (150 mil body), 8-lead
	SM =	Plastic SOIC (208 mil body), 8-lead
	ST =	Plastic TSSOP (4.4 mm), 8-lead
	MS =	Plastic Micro Small Outline (MSOP), 8-lead

Examples:

a) 24AA64-I/P: Industrial Temperature, PDIP package
b) 24AA64-I/SN: Industrial Temperature, SOIC package
c) 24AA64-I/SM: Industrial Temperature, SOIC (208 mil) package
d) 24AA64X-I/ST: Industrial Temperature, Rotated TSSOP package
e) 24AA64-I/ST: Industrial Temperature, TSSOP package

a) 24LC64-I/P: Industrial Temperature, PDIP package
b) 24LC64-E/SN: Extended Temperature, SOIC package
c) 24LC64-E/SM: Extended Temperature, SOIC (208 mil) package
d) 24LC64X-I/ST : Extended Temperature, Rotated TSSOP package
e) 24LC64-I/ST: Industrial Temperature, TSSOP package

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