16K-128K I²C Serial EEPROM with Software Write Protection Family Data Sheet

Device Selection Table

Part Number	Density	Page Size	Vcc Range	Package	Temp. Ranges
24CW16X	16-Kbit	32-byte	1.6-5.5	SN, OT, ST, MUY	I
24CW32X	32-Kbit	32-byte	1.6-5.5	SN, OT, ST, MUY	I
24CW64X	64-Kbit	32-byte	1.6-5.5	SN, OT, ST, MUY, CS0, CS1	I
24CW128X	128-Kbit	32-byte	1.6-5.5	SN, OT, ST, MUY, CS0, CS1	I

Note: 'X' in the part number refers to the preset hardware slave address. Refer to Table 3-2 for additional information.

Features

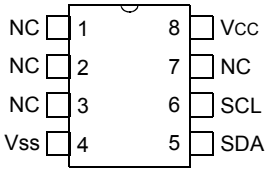
- 16/32/64/128-Kbit EEPROM:
  - Internally organized as one 2048/4096/8192/16384 x 8 bit block
  - Byte or page writes up to 32 bytes
  - Byte or sequential reads within a block
  - Self-timed write cycle (5 ms maximum)
- High-Speed I²C Interface:
  - Industry standard: 1 MHz, 400 kHz and 100 kHz
  - Output slope control to eliminate ground bounce
  - Schmitt trigger inputs for noise suppression
- Programmable Hardware Slave Address Bits:
  - Configurable via the Hardware Address Register (HAR)
- Versatile Data Protection Options:
  - Software write protection via the Write Protection Register (WPR)
- Operating Voltage Range of 1.6V to 5.5V
- Low-Power CMOS Technology:
  - Write current: 1.0 mA maximum at 5.5V
  - Read current: 1.0 mA maximum at 5.5V, 1 MHz
  - Standby Current: 1 µA at 5.5V
- High Reliability:
  - More than one million erase/write cycles
  - Data retention: >200 years
  - ESD protection: >4000V
- RoHS Compliant

Packages

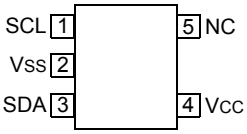
- 8-Lead SOIC, 8-Lead TSSOP, 8-Pad UDFN, 5-Lead SOT-23 and Two 4-Ball CSP options

Package Types (not to scale)

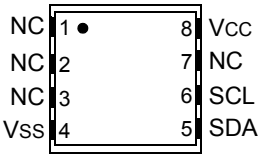
8-Lead SOIC/TSSOP
(Top View)



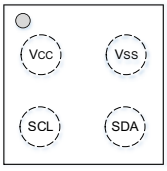
5-Lead SOT23
(Top View)



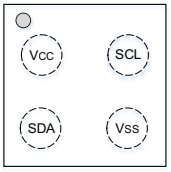
8-Pad UDFN
(Top View)



4-Ball CSP (CS0)(1)
(Top View)



4-Ball CSP (CS1)(2)
(Top View)



Note 1: CS0 CSP ball pitch is 0.4x0.4 mm.
2: CS1 CSP ball pitch is 0.5x0.4 mm.

Pin Function Table

Name	Function
Vss	Ground
SDA	Serial Data Pin
SCL	Serial Clock Input
Vcc	Supply Voltage

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Description

The 24CW16X/24CW32X/24CW64X/24CW128X (24CW Series) devices provide 16-128 Kbits of Serial EEPROM utilizing an I^2C (2-wire) serial interface. The 24CW Series is organized as 2048/4096/8192/16384 bytes of 8 bits each (2-16 Kbytes). The 24CW Series is optimized for use in consumer and industrial applications, where reliable and dependable nonvolatile memory storage is essential. The 24CW Series allows up to eight devices to share a common I^2C (2-wire) bus and is capable of operation across a broad voltage range (1.6V to 5.5V).

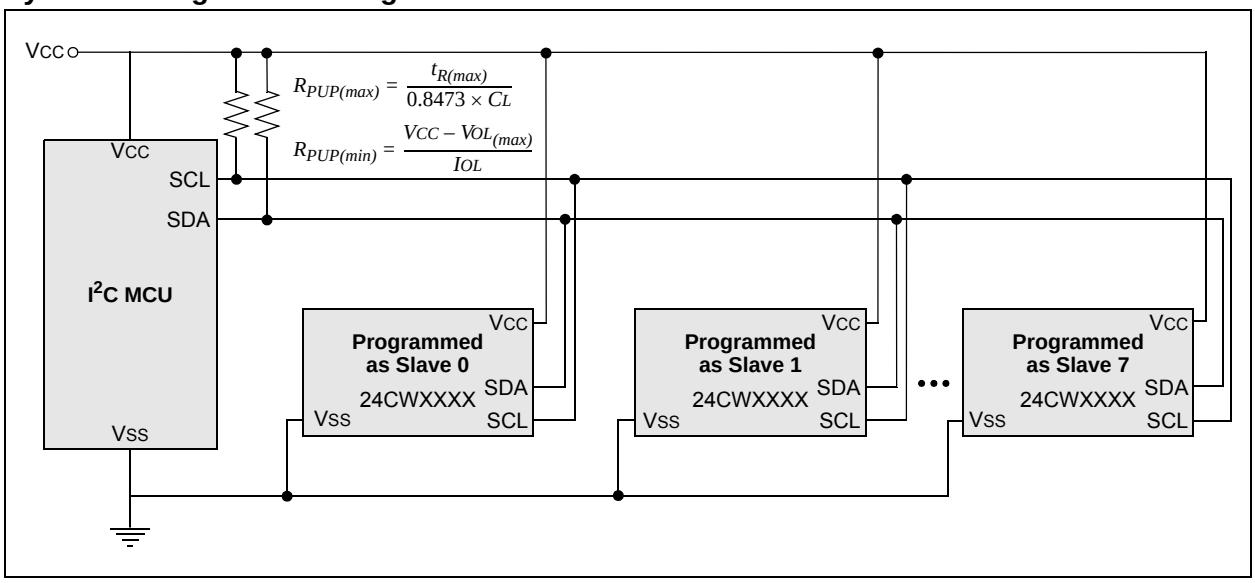
The 24CW Series contains a pair of programmable Configuration registers which allow certain device behaviors to be modified. These registers are the Write Protection Register and the Hardware Address Register.

The Write Protection Register (WPR) controls the valid address ranges of the EEPROM array that can be written. This allows the user to select the write protection behavior to be configured for software write protection.

The Hardware Address Register (HAR) controls the three hardware slave address bits. These bits determine which device addresses the 24CW Series will Acknowledge. Because the 24CW Series is a 4-pin device, the cascadable feature is controlled by the HAR.

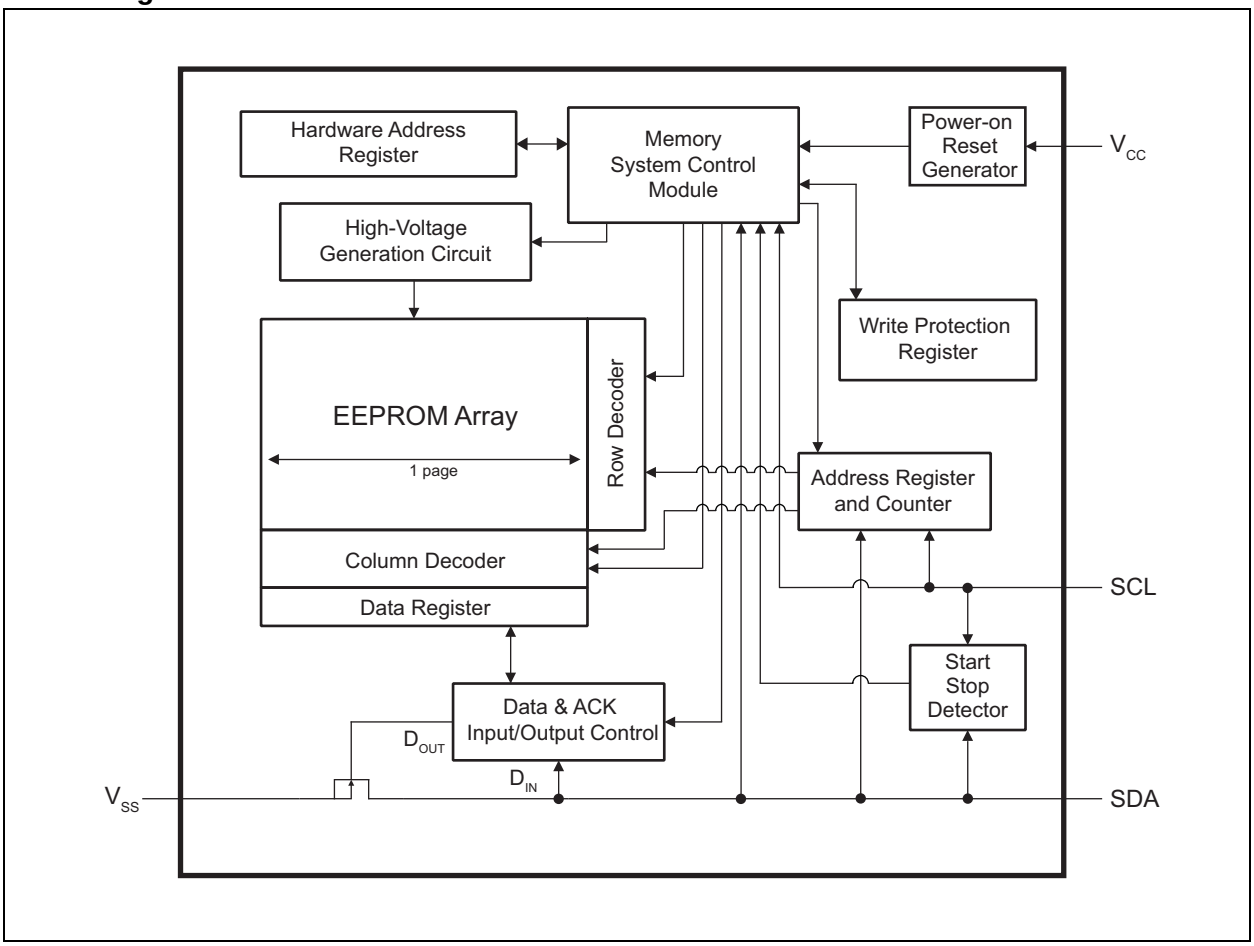
Once the desired software write protection and hardware slave address bits are set, these Configuration registers can be permanently locked, thereby preventing any further changes to the device operation.

System Configuration Using Serial EEPROMs



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Block Diagram



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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings(†)

VCC.....6.5V

All inputs and outputs w.r.t. VSS ..... -0.6V to 6.5V

Storage temperature .....-65°C to +150°C

Ambient temperature under bias.....-40°C to +85°C

ESD protection on all pins.....>4 kV

† **NOTICE:** Stresses above those listed under 'Maximum ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for an extended period of time may affect device reliability.

TABLE 1-1: DC CHARACTERISTICS

DC CHARACTERISTICS			**Electrical Characteristics:** Industrial (I): VCC = 1.6V to 5.5V TA = -40°C to +85°C			
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Max.**	**Units**	**Test Conditions**
D1	VIH	High-Level Input Voltage	VCC x 0.7	VCC + 0.5	V	
D2	VIL	Low-Level Input Voltage	-0.6	VCC x 0.3	V	
D3	VOL	Low-Level Output Voltage	—	0.4	V	IOL = 2.1 mA, VCC = 3.0V
			—	0.2	V	IOL = 0.15 mA, VCC = 1.8V
D4	ILI	Input Leakage Current	—	±1	µA	VIN = VSS or VCC
D5	ILO	Output Leakage Current	—	±1	µA	VOUT = VSS or VCC
D6	CINT	Internal Capacitance (all inputs and outputs)	—	7	pF	TAMB = +25°C, FCLK = 1 MHz, VCC = 5.5V **(Note 1)**
D7	ICCREAD	Operating Current	—	0.3	mA	VCC = 1.8V, FCLK = 400 kHz
			—	1	mA	VCC = 5.5V, FCLK = 1 MHz
D8	ICCWRITE	Operating Current	—	1	mA	VCC = 5.5V, FCLK = 1 MHz
D9	ICCS	Standby Current	—	0.5	µA	SCL = SDA = VCC = 1.8V
			—	1.0	µA	SCL = SDA = VCC = 5.5V

Note 1: This parameter is not tested, but is ensured by characterization.

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TABLE 1-2: AC CHARACTERISTICS

AC CHARACTERISTICS			Electrical Characteristics: Industrial (I): VCC = 1.6V to 5.5V TA = -40°C to +85°C:			
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Max.**	**Units**	**Conditions**
1	FCLK	Clock Frequency	—	1000	kHz	1.6V ≤ VCC ≤ 5.5V
2	THIGH	Clock High Time	260	—	ns	1.6V ≤ VCC ≤ 5.5V
3	TLOW	Clock Low Time	500	—	ns	1.6V ≤ VCC ≤ 5.5V
4	TR	SDA and SCL Rise Time	—	1000	ns	1.6V ≤ VCC ≤ 5.5V **(Note 1)**
5	TF	SDA and SCL Fall Time	—	300	ns	1.6V ≤ VCC ≤ 5.5V **(Note 1)**
6	THD:STA	Start Condition Hold Time	260	—	ns	1.6V ≤ VCC ≤ 5.5V
7	TSU:STA	Start Condition Setup Time	260	—	ns	1.6V ≤ VCC ≤ 5.5V
8	THD:DAT	Data Input Hold Time	0	—	ns	**(Note 2)**
9	TSU:DAT	Data Input Setup Time	50	—	ns	1.6V ≤ VCC ≤ 5.5V
10	TSU:STO	Stop Condition Setup Time	260	—	ns	1.6V ≤ VCC ≤ 5.5V
11	TAA	Output Valid from Clock	—	450	ns	1.6V ≤ VCC ≤ 5.5V
12	TBUF	Bus Free Time: Bus Time must be Free before a New Transmission can Start	500	—	ns	1.6V ≤ VCC ≤ 5.5V
13	TSP	Input Filter Spike Suppression (SDA and SCL pins)	—	50	ns	**(Note 3)**
14	TWC	Write Cycle Time (byte or page)	—	5	ms	

Note 1: The rise/fall times must be less than the specified maximums in order to achieve the maximum clock frequencies specified for FCLK. Please refer to the I^2C specification for applicable timings.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.

3: Not 100% tested. CB = total capacitance of one bus line in pF.

FIGURE 1-1: BUS TIMING DATA

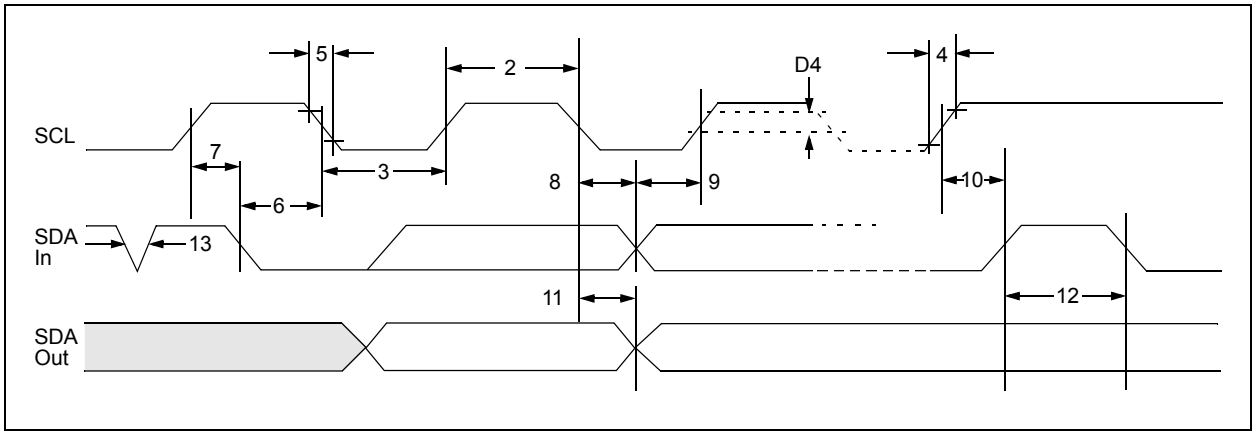


TABLE 1-3: EEPROM CELL PERFORMANCE CHARACTERISTICS

Operation	Test Condition	Min.	Max.	Units
Write Endurance(1)	TA = 25°C, 1.6V ≤ VCC ≤ 5.5V	1,000,000	—	Write Cycles
Data Retention(1)	TA = 55°C	200	—	Years

Note 1: Performance is determined through characterization and the qualification process.

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1.1 Power-up Requirements and Reset Behavior

During a power-up sequence, the VCC supplied to the 24CW Series should monotonically rise from VSS to the minimum VCC level, as specified in Table 1-1, with a slew rate no faster than 0.1V/µs.

1.1.1 DEVICE RESET

To prevent write operations or other spurious events from happening during a power-up sequence, the 24CW Series includes a Power-on Reset (POR) circuit. Upon power-up, the device will not respond to any commands until the VCC level crosses the internal voltage threshold (VPOR) that brings the device out of Reset and into Standby mode.

The system designer must ensure that instructions are not sent to the device until the VCC supply has reached a stable value greater than, or equal to, the minimum VCC level. Additionally, once the VCC is greater than, or equal to, the minimum VCC level, the master must wait at least TPUP before sending the first command to the device. See Table 1-4 for the values associated with these power-up parameters.

If an event occurs in the system where the VCC level supplied to the 24CW Series drops below the maximum VPOR level specified, it is recommended that a full-power cycle sequence be performed by first driving the VCC pin to VSS, waiting at least the minimum TPOFF time and then perform a new power-up sequence in compliance with the requirements defined in **Section 1.1 "Power-up Requirements and Reset Behavior"**.

TABLE 1-4: POWER-UP CONDITIONS

Symbol	Parameter	Min.	Max.	Units
TPUP	Time Required after VCC is Stable before the Device can Accept Commands	100	—	µs
VPOR	Power-on Reset Threshold Voltage	—	1.5	V
TPOFF	Minimum Time at VCC = 0V between Power Cycles	1	—	ms

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2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Name	8-Lead SOIC	8-Lead TSSOP	5-Lead SOT23	8-Lead UDFN(1)	4-Ball CSP (CS0)(2)	4-Ball CSP (CS1)(3)	Function
NC	1	1	—	1	—	—	No Connect
NC	2	2	—	2	—	—	No Connect
NC	3	3	—	3	—	—	No Connect
VSS	4	4	2	4	A2	B2	Ground
SDA	5	5	3	5	B2	B1	Serial Data
SCL	6	6	1	6	B1	A2	Serial Clock
NC	7	7	5	7	—	—	No Connect
VCC	8	8	4	8	A1	A1	Device Power Supply

Note 1: The exposed pad on this package can be connected to VSS or left floating.

2: CS0 CSP ball pitch is 0.4x0.4 mm.

3: CS1 CSP ball pitch is 0.5x0.4 mm.

2.1 Serial Data (SDA)

This is a bidirectional pin used to transfer addresses and data into and out of the device. It is an open-drain terminal, therefore, the SDA bus requires a pull-up resistor to VCC (typical 10 kΩ for 100 kHz and 2 kΩ for 400 kHz and 1 MHz).

For normal data transfer, SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the Start and Stop conditions.

2.2 Serial Clock (SCL)

This input is used to synchronize the data transfer from and to the device.

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3.0 MEMORY ORGANIZATION

3.1 EEPROM Organization

The 24CW Series is internally organized as 64/128/256/512 pages of 32 bytes each, depending on the density.

3.2 Device Configuration Registers

The 24CW Series contains two Configuration registers that modulate device operation and/or report on the current status of the device. These registers are:

- Write Protection Register (WPR)
- Hardware Address Register (HAR)

Once the device behavior is set as desired, the Configuration registers can be permanently locked (or set to read-only), thereby preventing any subsequent changes.

3.2.1 WRITE PROTECTION REGISTER

The Write Protection Register (WPR) allows for modification of the device write protection behavior. Refer to **Section 8.2 "Write Protection Register"** for additional information of the WPR.

3.2.2 HARDWARE ADDRESS REGISTER

The Hardware Address Register (HAR) allows for modification of the hardware slave address bits in the device address byte that the device will Acknowledge. Refer to **Section 8.3 "Hardware Address Register"** for additional information on the HAR.

3.3 Device Addressing

Communication with the 24CW Series begins with an 8-bit device address byte, comprised of a 7-bit slave address and a Read/Write Select (R/$\overline{W}$) bit. Since multiple slave devices can reside on the serial bus, each slave device must have its own unique device address, programmed in the HAR, so that the master can access each device independently.

The 7-bit slave address is constructed using two groups of bits. The first four bits contain the Device Type Identifier, followed by three bits containing the hardware slave address bits.

The 24CW Series will respond to only specific Device Type Identifiers, as shown in **Section 3.3.1 "Valid Device Address Byte Inputs"**.

The 3-bit hardware slave address is comprised of bits A2, A1 and A0. These bits can be used to expand the address space by allowing up to eight devices with the same Device Type Identifiers on the bus. These hardware slave address bits must correlate with the values programmed in the HAR.

The device will respond to all valid device address byte combinations that it receives.

3.3.1 VALID DEVICE ADDRESS BYTE INPUTS

The 24CW Series will respond to the Device Type Identifiers, as shown in Table 3-1.

3.3.1.1 Preset Slave Addresses

The 24CW Series is preset with a specific slave address. The preset slave address bits are embedded in the base part number, as shown in Table 3-2.

TABLE 3-1: TABLE OF VALID DEVICE ADDRESS BYTES

Access Region	Device Type Identifier				Hardware Slave Address			Read/Write Select
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EEPROM	1	0	1	0	A2	A1	A0	R/$\overline{W}$
Configuration Registers	1	0	1	0	A2	A1	A0	R/$\overline{W}$

Note: The access region is selected according to bit 7 of the first word address byte. Refer to **Section 3.3.2 "Word Address Bytes"** for additional information.

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TABLE 3-2: DEVICE PRESET SLAVE ADDRESS

Part Number Series 24CWXXXX	Hardware Slave Address Bits		
	A2	A1	A0
24CWXXX**0**(1)	0	0	0
24CWXXX**1**(1,2)	0	0	1
24CWXXX**2**(1,2)	0	1	0
24CWXXX**3**(1,2)	0	1	1
24CWXXX**4**(1,2)	1	0	0
24CWXXX**5**(1,2)	1	0	1
24CWXXX**6**(1,2)	1	1	0
24CWXXX**7**(1,2)	1	1	1

Note 1: 'XXX' in the part number varies depending on the density.

2: Contact your local sales representative for hardware slave address availability.

3.3.1.2 Read/Write Select Bit

The eighth bit (bit 0) of the device address byte is the Read/Write Select (R/$\overline{W}$) bit. A read operation is initiated if this bit is a logic '1' and a write operation is initiated if this bit is a logic '0'.

Upon the successful comparison of the device address byte, the 24CW Series will respond. If a valid comparison is not made, the device will not respond and return to a standby state.

3.3.2 WORD ADDRESS BYTES

Two 8-bit word address bytes are transmitted to the device immediately following the device address byte.

The first word address byte contains the Most Significant bits (MSbs) of the memory array word address to specify which location in the EEPROM to start reading or writing. Note that the number of word address bits depends on the density. Refer to Table 3-3 for details.

When accessing the memory array, it is required that bit 7 of the word address byte be set to a logic '0'. When accessing the Configuration registers, it is required that bit 7 of the first word address byte be set to a logic '1'. Refer to Table 3-3 for details.

Next, the second word address byte is sent to the device which provides the remaining eight bits of the word address (A7 through A0). Refer to Table 3-4 for details.

TABLE 3-3: FIRST WORD ADDRESS BYTE

Memory Region	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
16-Kbit EEPROM	0	x	x	x	x	A10	A9	A8
32-Kbit EEPROM	0	x	x	x	A11	A10	A9	A8
64-Kbit EEPROM	0	x	x	A12	A11	A10	A9	A8
128-Kbit EEPROM	0	x	A13	A12	A11	A10	A9	A8
Configuration Registers	1	x	x	x	x	x	x	x

TABLE 3-4: SECOND WORD ADDRESS BYTE

Memory Region	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
16-Kbit EEPROM	A7	A6	A5	A4	A3	A2	A1	A0
32-Kbit EEPROM	A7	A6	A5	A4	A3	A2	A1	A0
64-Kbit EEPROM	A7	A6	A5	A4	A3	A2	A1	A0
128-Kbit EEPROM	A7	A6	A5	A4	A3	A2	A1	A0
Configuration Registers(1)	x	x	x	x	x	x	x	x

Note 1: When accessing the Configuration registers, the second word address byte must be transmitted to the device despite containing only don't care values.

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4.0 FUNCTIONAL DESCRIPTION

The 24CW Series supports a bidirectional 2-wire bus and data transmission protocol. A device that sends data onto the bus is defined as a transmitter and a device receiving data as a receiver. The bus must be controlled by a master which generates the Serial Clock (SCL), controls the bus access and generates the Start and Stop conditions, while the 24CW Series works as a slave. Both master and slave can operate as a transmitter or receiver, but the master determines which mode is activated.

5.0 BUS CHARACTERISTICS

The following bus protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line, while the clock line is high, will be interpreted as a Start or Stop condition.

Accordingly, the following bus conditions have been defined (Figure 5-1).

5.1 Bus Not Busy (A)

Both data and clock lines remain high.

5.2 Start Data Transfer (B)

A high-to-low transition of the SDA line while the clock (SCL) is high determines a Start condition. All commands must be preceded by a Start condition.

5.3 Stop Data Transfer (C)

A low-to-high transition of the SDA line while the clock (SCL) is high determines a Stop condition. All operations must end with a Stop condition.

5.4 Data Valid (D)

The state of the data line represents valid data when, after a Start condition, the data line is stable for the duration of the high period of the clock signal.

The data on the line must be changed during the low period of the clock signal. There is one bit of data per clock pulse.

Each data transfer is initiated with a Start condition and terminated with a Stop condition. The number of the data bytes transferred between the Start and Stop conditions is determined by the master.

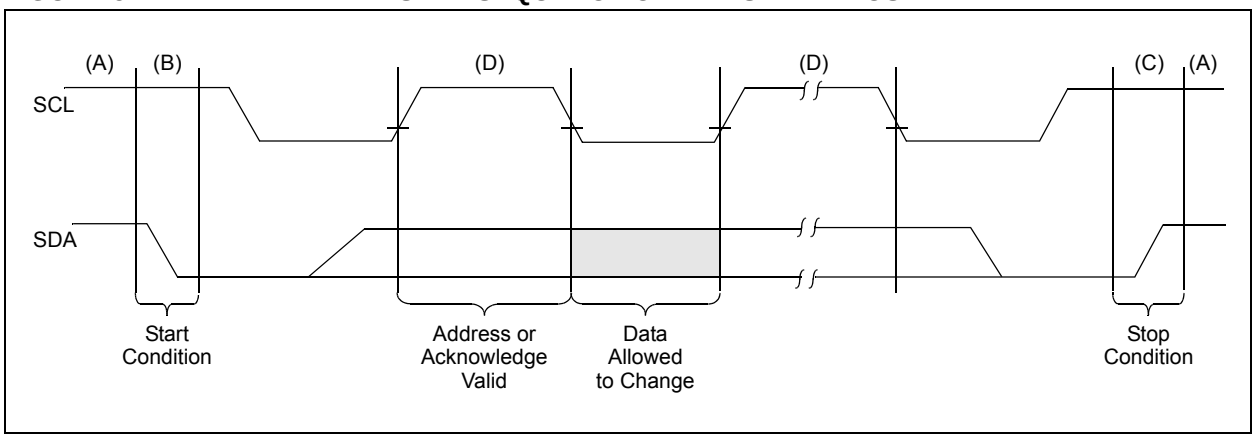
5.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an Acknowledge signal after the reception of each byte. The master must generate an extra clock pulse, which is associated with this Acknowledge bit. See Figure 5-2 for Acknowledge timing.

Note:	The 24CW Series does not generate any Acknowledge bits if an internal programming cycle is in progress.

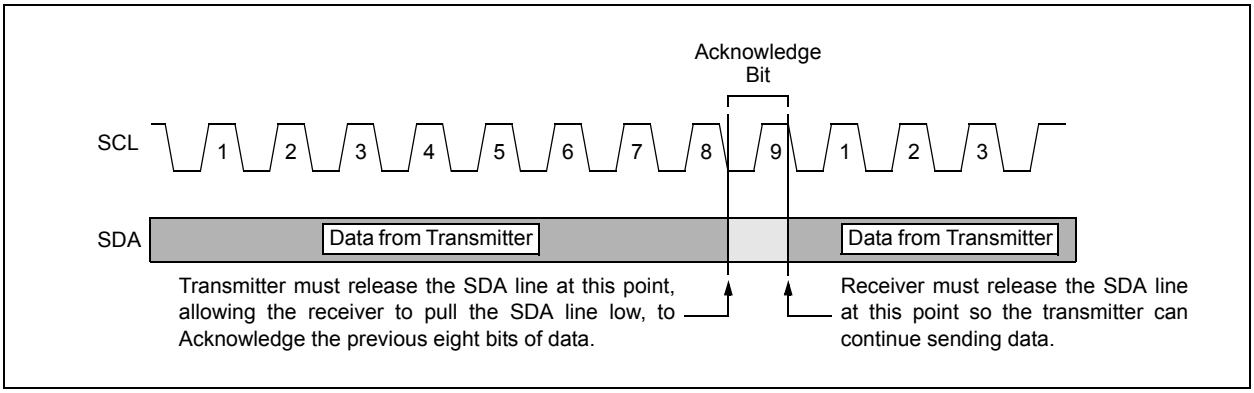
A device that Acknowledges must pull down the SDA line during the Acknowledge clock pulse, in such a way, that the SDA line is stable low during the high period of the Acknowledge related clock pulse. Of course, setup and hold times must be taken into account. During read operations, the master must signal an end of data to the slave by NOT generating an Acknowledge (NACK) bit on the last byte that has been clocked out of the slave. In this case, the slave (24CW Series) will leave the data line high to enable the master to generate the Stop condition.

FIGURE 5-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS



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FIGURE 5-2: ACKNOWLEDGE TIMING



5.6 Standby Mode

The 24CW Series features a low-power Standby mode which is enabled when any one of the following occurs:

- A valid power-up sequence is performed (see **Section 1.1 "Power-up Requirements and Reset Behavior"**).
- A Stop condition is received by the device unless it initiates an internal write cycle (see **Section 6.0 "Write Operations"**).
- At the completion of an internal write cycle (see **Section 6.0 "Write Operations"**).
- An unsuccessful match of the Device Type Identifier or hardware slave address in the device address byte occurs (see **Section 3.3 "Device Addressing"**).
- The master does not Acknowledge the receipt of data read out from the device; instead, it sends a NACK response.(see **Section 7.0 "Read Operations"**).

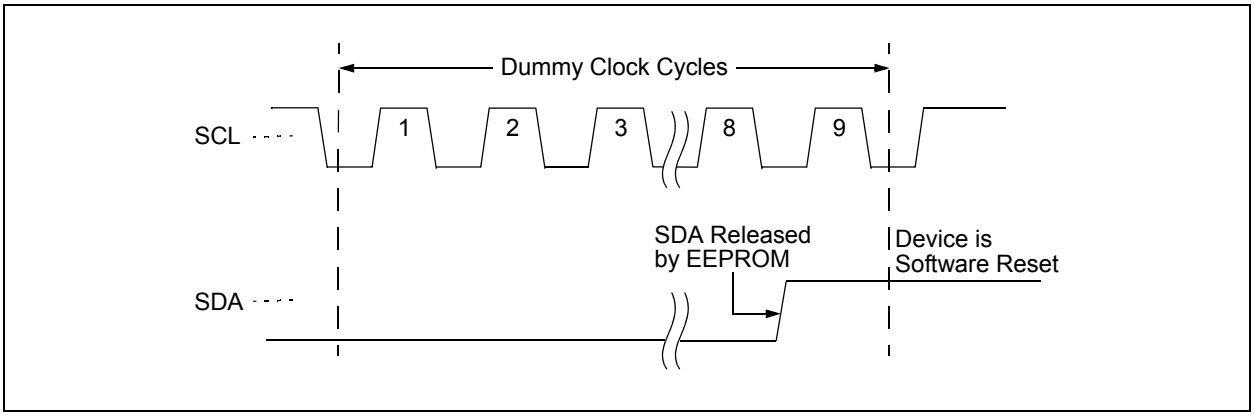
5.7 Software Reset

After an interruption in protocol, power loss or system Reset, any 2-wire device can be protocol reset by clocking SCL until SDA is released by the EEPROM and goes high. The number of clock cycles until SDA is released by the EEPROM will vary. The Software Reset sequence should not take more than nine dummy clock cycles. Note that the Software Reset sequence will not interrupt the internal write cycle and only resets the I^2C interface.

Once the Software Reset sequence is complete, new protocol can be sent to the device by sending a Start condition, followed by the protocol. Figure 5-3 illustrates the Software Reset sequence.

In the event that the device is still non-responsive, or remains active on the SDA bus, a power cycle must be used to reset the device (see **Section 1.1.1 "Device Reset"**).

FIGURE 5-3: SOFTWARE RESET



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6.0 WRITE OPERATIONS

All write operations for the 24CW Series begin with the master sending a Start condition, followed by a device address byte with the R/$\overline{W}$ bit set to a logic '0', and then by the word address bytes. The data value(s) to be written to the device immediately follows the word address bytes.

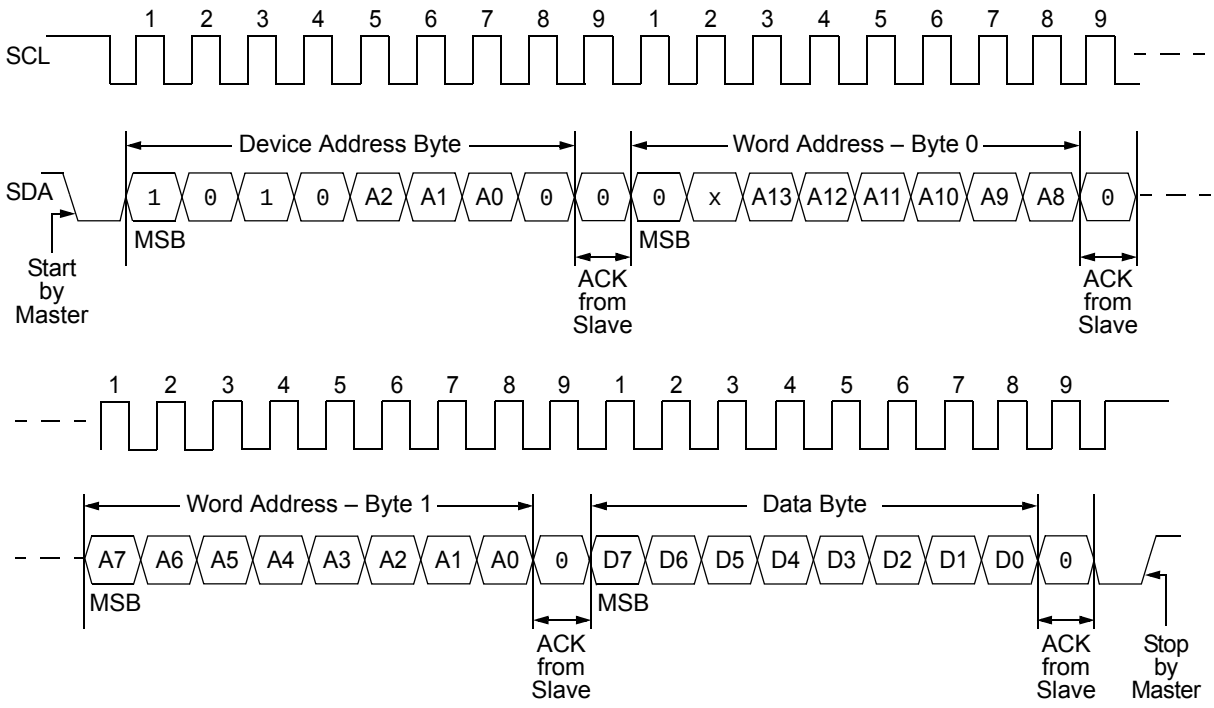
6.1 Byte Write

The 24CW Series supports the writing of a single 8-bit byte. Selecting a data byte in the 24CW Series requires a two-byte word address with the MSb set to a logic '0'. Note that some word address bits are ignored and the number of ignored bits depends on the device density.

Upon receipt of the proper device address and word address bytes, the EEPROM will send an Acknowledge. The device will then be ready to receive the first 8-bit data byte. Following the receipt of the data byte, the EEPROM will respond with an Acknowledge. The addressing device, such as a master, must then terminate the write operation with a Stop condition. At that time, the EEPROM will enter an internally self-timed write cycle, which will be completed within TWC, while the data byte is being programmed into the nonvolatile EEPROM. All inputs are disabled during this write cycle and the EEPROM will not respond until the write operation is complete.

If an attempt is made to write to a write-protected portion of the array, no data will be written and the device will immediately accept a new command.

FIGURE 6-1: BYTE WRITE



Note 1: The A13, A12 and A11 word address bits are don't care bits on the 24CW16X.

2: The A13 and A12 word address bits are don't care bits on the 24CW32X.

3: The A13 word address bit is a don't care bit on the 24CW64X.

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6.2 Page Write

A page write operation allows up to 32 bytes to be written in the same write cycle, provided all bytes are in the same page of the memory array. Partial page writes of less than 32 bytes are also allowed.

A page write is initiated the same way as a byte write, but the master does not send a Stop condition after the first data byte is clocked in. Instead, after the EEPROM Acknowledges receipt of the first data byte, the master can transmit up to 31 additional data bytes. The EEPROM will respond with an ACK after each data byte is received.

Once all data to be written has been sent to the device, the master must issue a Stop condition (see Figure 6-2). Once the Stop condition is received, an internal write cycle will begin.

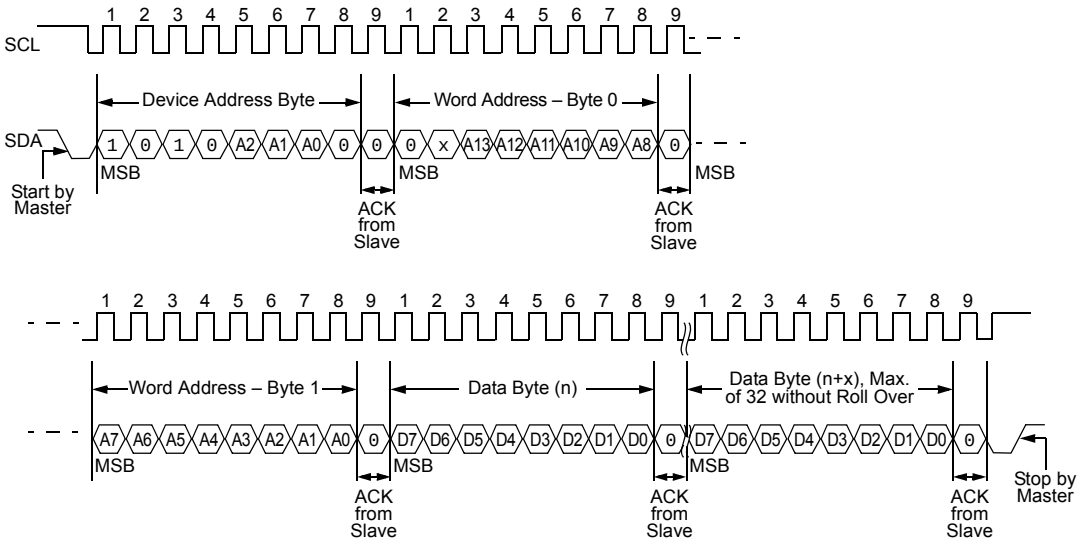
If an attempt is made to write to a write-protected portion of the array, no data will be written and the device will immediately accept a new command.

The lower five bits of the word address are internally incremented following the receipt of each data byte. The higher order address bits are not incremented and retain the memory page location.

When the incremented word address reaches the page boundary, the address counter will roll over to the beginning of the same page.

Note:	Page write operations are limited to writing bytes within a single physical page, **regardless** of the number of bytes actually being written. Physical page boundaries start at addresses that are integer multiples of the page buffer size (or 'page size') and end at the addresses that are integer multiples of [page size – 1]. If a page write operation attempts to write across a physical page boundary, the result is that the data wraps around to the beginning of the current page (overwriting data previously stored there), instead of being written to the next page as might be expected. It is therefore necessary for the application software to prevent page write operations that would attempt to cross a page boundary.

FIGURE 6-2: PAGE WRITE



Note 1: The A13, A12 and A11 word address bits are don't care bits on the 24CW16X.

2: The A13 and A12 word address bits are don't care bits on the 24CW32X.

3: The A13 word address bit is a don't care bit on the 24CW64X.

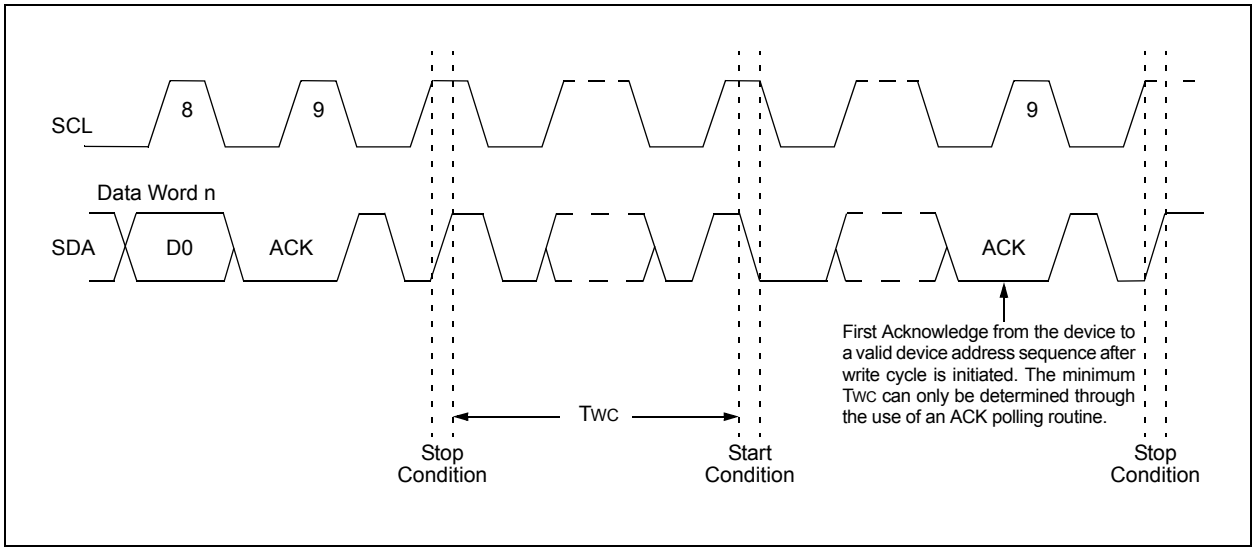
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6.3 Write Cycle Timing

The length of the self-timed write cycle, or TWC, is defined as the amount of time from the Stop condition that begins the internal write operation, to the Start condition of the first device address byte sent to the 24CW Series that it subsequently responds to with an ACK (see Figure 6-3).

During the internally self-timed write cycle, any attempts to read from, or write to, the memory array will not be processed.

FIGURE 6-3: WRITE CYCLE TIMING



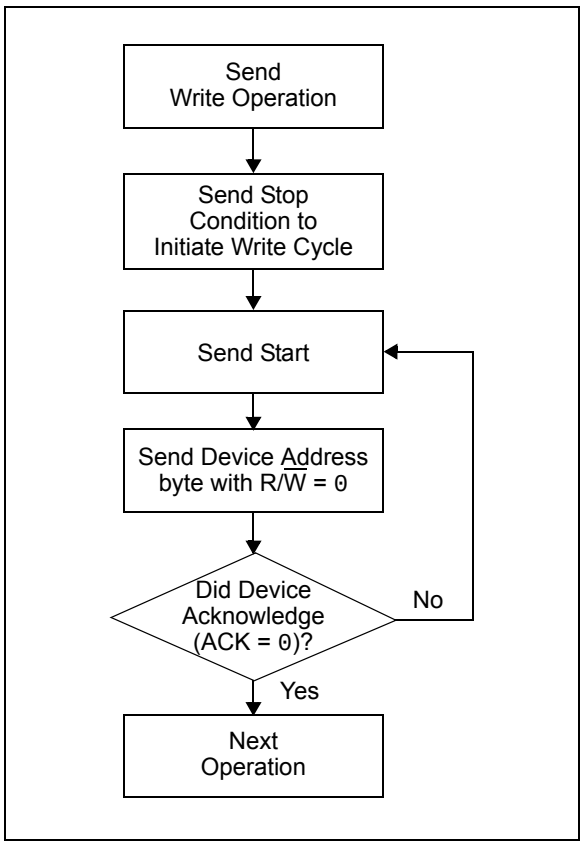
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6.4 Acknowledge Polling

Since the device will not Acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the Stop condition for a write operation has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a Start condition, followed by the device address byte for a write operation (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, then a NACK will be returned. If a NACK is returned, then the Start bit and device address byte must be resent. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write operation. See Figure 6-4 for the flow diagram.

Note:	If the user is polling after writing to the Hardware Address Register (HAR), the user must send the new hardware slave address to determine whether the write cycle is complete. If the 24CW Series doesn't ACK the new hardware slave address after the maximum write cycle time (T_{WC}), the write to the HAR was not successful.

FIGURE 6-4: ACKNOWLEDGE POLLING FLOW



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6.5 Write Protection

The 24CW Series write protection is controlled via the Write Protection Register (WPR). The 24CW Series is segmented into four different memory zones, which allows the user to select which of the zones will be software write-protected. The protection behavior can be made permanent by locking the Configuration registers. For additional information on the Write Protection Register, see **Section 8.2 "Write Protection Register"**.

TABLE 6-1: 24CW SERIES SOFTWARE WRITE PROTECTION

Protection Level	Protected Address Range			
	24CW16X	24CW32X	24CW64X	24CW128X
Upper 1/4	0600h-07FFh	0C00h-0FFFh	1800h-1FFFh	3000h-3FFFh
Upper 1/2	0400h-07FFh	0800h-0FFFh	1000h-1FFFh	2000h-3FFFh
Upper 3/4	0200h-07FFh	0400h-0FFFh	0800h-1FFFh	1000h-3FFFh
Entire Array	0000h-07FFh	0000h-0FFFh	0000h-1FFFh	0000h-3FFFh

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7.0 READ OPERATIONS

Read operations are initiated the same way as write operations, with the exception that the Read/Write Select (R/$\overline{W}$) bit in the device address byte must be a logic '1'. There are three read operations:

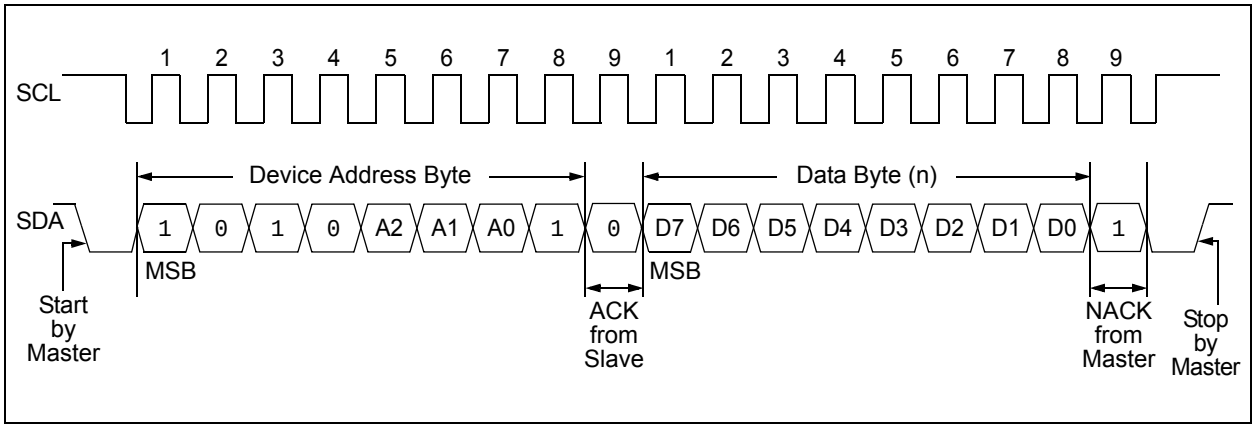
- Current Address Read
- Random Address Read
- Sequential Read

7.1 Current Address Read

The 24CW Series contains an internal Address Pointer that maintains the word address of the last byte accessed, internally incremented by one. Therefore, if the previous read access was to address 'n' (n is any legal address), the next current address read operation would access data from address n+1.

A current address read operation will output data according to the location of the internal Address Pointer. This is initiated with a Start condition, followed by a valid device address byte with the R/$\overline{W}$ bit set to logic '1'. The device will ACK this sequence and the current address data byte is serially clocked out on the SDA line. All types of read operations will be terminated if the master does not respond with an ACK (it NACKs) during the ninth clock cycle, which will force the device into Standby mode. After the NACK response, the master may send a Stop condition to complete the protocol or it can send a Start condition to begin the next sequence.

FIGURE 7-1: CURRENT ADDRESS READ

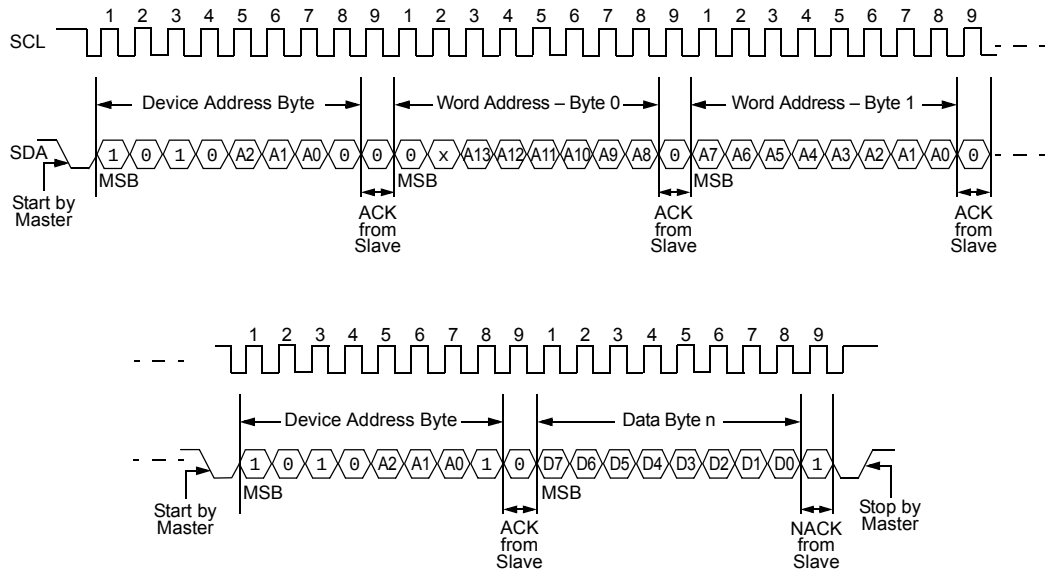


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7.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address, with the MSb set to logic '0', to the 24CW Series as part of a write operation (R/$\overline{W}$ bit set to '0'). After the word address is sent, the master generates a Start condition following the Acknowledge. This terminates the write operation, but not before the internal Address Pointer is set. Then, the master issues the device address byte again, but with the R/$\overline{W}$ bit set to a '1'. The 24CW Series will then issue an Acknowledge and transmit the 8-bit data byte. The master will not Acknowledge the transfer, but does generate a Stop condition which causes the 24CW Series to discontinue transmission (Figure 7-2). After a random read operation, the internal Address Pointer will point to the last word address location, incremented by one.

FIGURE 7-2: RANDOM READ



Note 1: The A13, A12 and A11 word address bits are don't care bits on the 24CW16X.
2: The A13, A12 word address bits are don't care bits on the 24CW32X.
3: The A13 word address bit is a don't care bit on the 24CW64X.

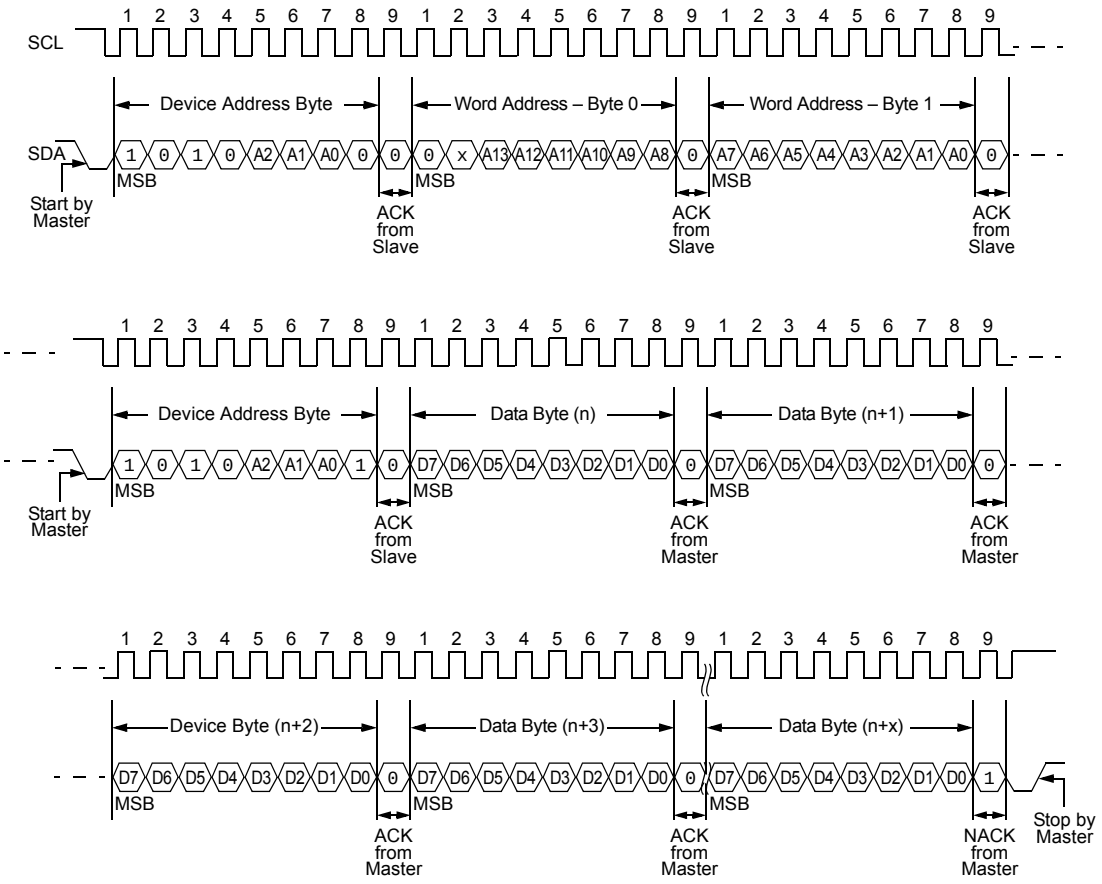
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7.3 Sequential Read

A sequential read is initiated by either a current address read or a random read. After the master receives a data byte, the master responds with an Acknowledge. As long as the EEPROM receives an ACK, it will continue to increment the word address and serially clock out the sequential data byte. When the maximum memory address is reached, the internal Address Pointer will automatically roll over from the end of the array to word address, 0000h, if the master Acknowledges the byte received from the end of the array.

All types of read operations will be terminated if the master does not respond with an ACK (it NACKs) during the ninth clock cycle, which will force the device into Standby mode. After the NACK response, the master may send a Stop condition to complete the protocol or it can send a Start condition to begin the next sequence.

FIGURE 7-3: SEQUENTIAL READ



Note 1: The A13, A12 and A11 word address bits are don't care bits on the 24CW16X.

2: The A13 and A12 word address bit are don't care bits on the 24CW32X.

3: The A13 word address bit is a don't care bit on the 24CW64X.

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8.0 CONFIGURATION REGISTERS

The 24CW Series device contains a pair of 8-bit Configuration registers which control software write protection and the hardware slave address.

The Configuration registers are accessed sequentially as Byte 0 and Byte 1, as shown in Table 8-1.

If desired, the Configuration registers can be locked so that the registers are set to read-only and can no longer be modified. This makes the current software write protection and hardware slave address scheme permanent.

TABLE 8-1: CONFIGURATION REGISTERS

Memory Region	Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Write Protection Register	0	—	WRTE	CCLK	—	WPRE	WPB1	WPB0	CRLB
Hardware Address Register	1	—	HWRE	A0CK	—	—	A2	A1	A0

8.1 Accessing the Configuration Registers

The value of the Configuration registers can be determined by executing a random read sequence, as shown in **Section 8.5 "Reading the Configuration Registers"**. Changing the value of the Configuration registers is accomplished with a byte write sequence with the requirements outlined in **Section 8.4 "Writing to the Configuration Registers"**.

Accessing these registers requires the use of '1010b' (Ah) as the Device Type Identifier in the device address byte. Following the Device Type Identifier is the hardware slave address bits for which the values are determined by what is currently programmed in the HAR (see **Section 8.3 "Hardware Address Register"**). Finally, bit 0 is the Read/Write Select (R/W) bit, where a logic '1' is used for reading and logic '0' is used for writing. See Table 3-1 for additional information.

Note: The hardware slave address bit values are initially factory preset but can be changed by the user. These bit values must match the current device configuration to receive an Acknowledge.

When accessing the Configuration registers, the word address must be sent to the device. All bits in the word address are ignored, except for the MSb which must be set to logic '1'. Refer to Table 3-3 and Table 3-4 for additional information.

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8.2 Write Protection Register

The Write Protection Register (WPR) is Byte 0 of the sequential Configuration registers. The Write Protection Register format can be seen in Register 8-1.

REGISTER 8-1: WRITE PROTECTION REGISTER – BYTE 0

U-0	W-0	W-0	U-0	R/W	R/W	R/W	R/W
—	WRTE	CCLK	—	WPRE	WPB1	WPB0	CRLB
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **Unimplemented:** Read as '0'

bit 6 **WRTE:** Configuration Registers Write bit
1 = Configuration registers are writable
0 = Configuration register writes are ignored

bit 5 **CCLK:** Configuration Registers Check Lock bit
Must match the CRLB bit when writing to the Configuration registers.

bit 4 **Unimplemented:** Read as '0'

bit 3 **WPRE:** Write Protection Register Enable bit
1 = Write protection is set by the WPB<1:0> bits
0 = No software write protection is enabled **(Default)**

bit 2-1 **WPB<1:0>:** Write-Protect Block bits
If WPRE = 1:
11 = Entire EEPROM is write-protected
10 = Upper 3/4 of EEPROM is write-protected
01 = Upper 1/2 of EEPROM is write-protected
00 = Upper 1/4 of EEPROM is write-protected
If WPRE = 0:
Unused (**Default**).

bit 0 **CRLB:** Configuration Registers Lock bit
1 = Configuration registers will become permanently locked
0 = Configuration registers can be written to **(Default)**

Configuration Registers Write bit (WRTE): This bit must be set to a logic '1' in order to write to the Configuration registers. Failure to set the WRTE bit to a logic '1' will cause the device to ignore the write operation. When reading the WPR, the WRTE bit will always read as logic '0'.

Configuration Registers Check Lock bit (CCLK): This bit must match the CRLB bit when writing the Configuration registers. If the CCLK bit does not match the CRLB, the device will ignore the write operation. When reading the WPR, the CCLK bit will always read as logic '0'.

Write Protection Register Enable bit (WPRE): This bit is used to enable or disable the device software write protection feature. A logic '0' will disable the software write protection feature and a logic '1' will enable software write protection.

Write-Protect Block bits (WPB<1:0>): These bits allow four levels of protection for the memory array, provided that the WPRE bit is set to a logic '1'. If the WPRE bit is a logic '0', the state of the WPB<1:0> bits has no impact on device protection. The protected address ranges can be found in Table 8-2.

Configuration Registers Lock bit (CRLB): This bit is used to permanently lock the current state of the WPR and HAR. A logic '0' indicates that these registers can be modified, whereas a logic '1' indicates that the WPR and HAR have been locked and can no longer be modified. To safeguard against accidental locking of these registers, the CCLK bit must match the CRLB bit sent to the device. If these bits do not match, the device will ignore the write operation.

Note: The Configuration registers cannot be unlocked once they are locked.

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8.2.1 SOFTWARE WRITE PROTECTION

The EEPROM array in the 24CW Series will be protected from writing in accordance with the WPB<1:0> bits value as long as the WPRE bit is set to logic '1'. If the WPRE bit is set to logic '0', the WPB<1:0> bits are ignored and no portion of the EEPROM array will be protected. The combination of these three bits creates five possible levels of protection for the device, as seen in Table 8-2.

TABLE 8-2: PROTECTED ADDRESS RANGE

Protection Level	WPRE	WPB1	WPB0	Protected Address Range			
				24CW16X	24CW32X	24CW64X	24CW128X
None	0	x	x	None	None	None	None
Upper 1/4	1	0	0	0600h-07FFh	0C00h-0FFFh	1800h-1FFFh	3000h-3FFFh
Upper 1/2	1	0	1	0400h-07FFh	0800h-0FFFh	1000h-1FFFh	2000h-3FFFh
Upper 3/4	1	1	0	0200h-07FFh	0400h-0FFFh	0800h-1FFFh	1000h-3FFFh
Entire Array	1	1	1	0000h-07FFh	0000h-0FFFh	0000h-1FFFh	0000h-3FFFh

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8.3 Hardware Address Register

The Hardware Address Register (HAR) is Byte 1 of the sequential Configuration registers. The Hardware Address Register format can be seen in Register 8-2.

REGISTER 8-2: HARDWARE ADDRESS REGISTER – BYTE 1

U-0	W-0	W-0	U-0	U-0	R/W	R/W	R/W
—	HWRE	A0CK	—	—	A2	A1	A0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **Unimplemented:** Read as '0'

bit 6 **HWRE:** HAR Write Enable bit
1 = Configuration registers are writable
0 = Configuration register writes are ignored

bit 5 **A0CK:** Hardware Slave Address Check A0 bit
Must match A0 bit when writing the Configuration registers.

bit 4-3 **Unimplemented:** Read as '0'

bit 2 **A2:** Hardware Slave Address A2 bit
1 = Hardware slave address bit A2 is set to a logic '1'
0 = Hardware slave address bit A2 is set to a logic '0'

bit 1 **A1:** Hardware Slave Address A1 bit
1 = Hardware slave address bit A1 is set to a logic '1'
0 = Hardware slave address bit A1 is set to a logic '0'

bit 0 **A0:** Hardware Slave Address A0 bit
1 = Hardware slave address bit A0 is set to a logic '1'
0 = Hardware slave address bit A0 is set to a logic '0'

HAR Write Enable bit (HWRE): When writing to the HAR, this bit must be set to a logic '1'. Failure to set the HWRE bit to a logic '1' will cause the device to ignore the write operation. When reading the HAR, the HWRE bit will always read as logic '0'.

Hardware Slave Address Check A0 bit (A0CK): This bit must match the A0 bit when writing to the Configuration registers. If the A0CK bit does not match the A0 bit, the device will ignore the write operation. When reading the HAR, the A0CK bit will always read as logic '0'.

Hardware Slave Address bits (A2, A1, A0): The 3-bit hardware slave address is contained in bits A2, A1 and A0 of the HAR. These bits control the valid values in bit 3 through bit 1 (A2, A1, A0) of the device address byte. Details of the device address byte are found in **Section 3.3 "Device Addressing"**.

Note: If multiple 24CW Series devices are on the same bus, each device must have unique hardware slave addresses to be accessed individually, including programming the HAR. Different preset hardware slave addresses are available. Contact your local sales representative for details.

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8.4 Writing to the Configuration Registers

When writing to the Configuration registers, a byte write sequence must be sent to the device (see **Section 6.1 "Byte Write"** for additional information). The MSb of the word address must be set to logic '1' in order to write to the Configuration registers.

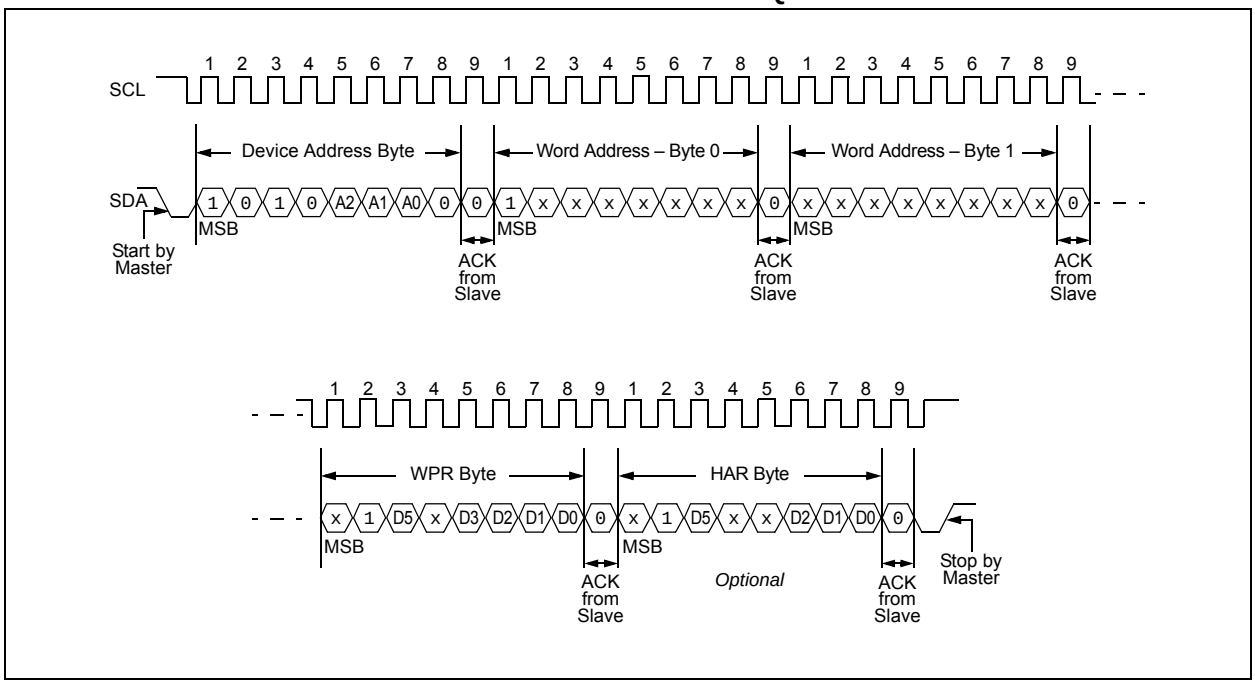
A valid WPR byte must be provided when writing to the Configuration registers. If the WPR byte is invalid, the operation will abort, the EEPROM will not Acknowledge any data bytes and the device will not execute the internal write cycle. Refer to **Section 8.2 "Write Protection Register"** for valid WPR byte values.

After sending a valid WPR byte, the HAR byte can optionally be sent. If the HAR byte is invalid, the operation will abort, the EEPROM will not Acknowledge any data bytes and the device will not execute the internal write cycle. Refer to **Section 8.3 "Hardware Address Register"** for valid HAR byte values.

Sending more than the WPR and HAR bytes to the 24CW Series will cause the write cycle to abort and the contents of the WPR and HAR will not be changed.

Note:	If a polling routine has been implemented and the user writes new data values to the HAR, the user must send the new hardware slave address for the device to Acknowledge.

FIGURE 8-1: CONFIGURATION REGISTERS WRITE SEQUENCE



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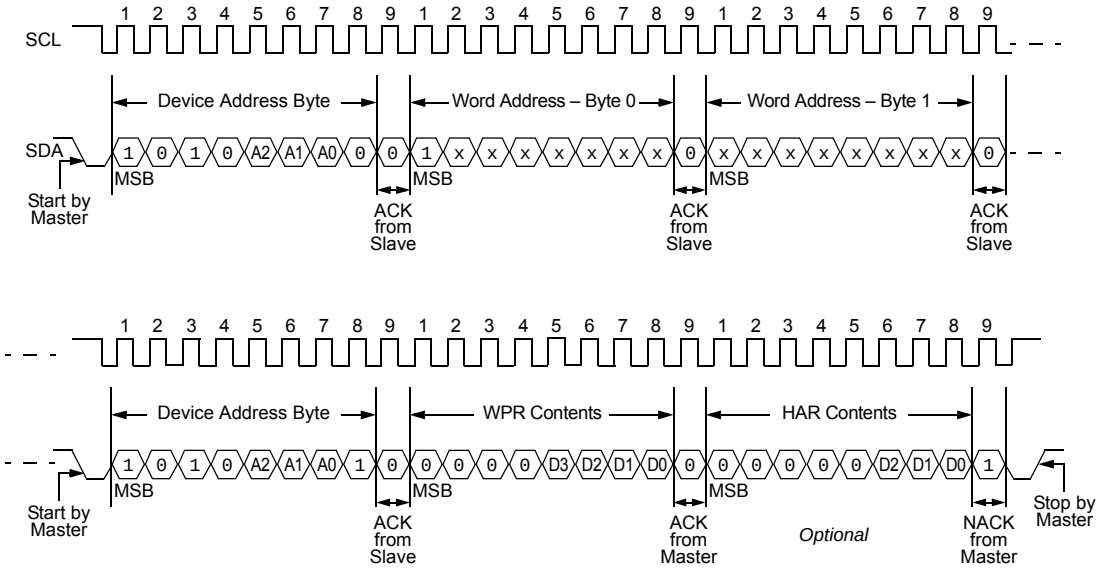
8.5 Reading the Configuration Registers

When reading the Configuration registers, a random read sequence must be sent to the device (see **Section 7.2 "Random Read"** for additional information). The MSb of the word address must be set to logic '1' in order to read the Configuration registers.

It is not possible to read the contents of the Configuration registers with a current address read sequence. Due to the sequential nature of the Configuration registers, it is not possible to read only the HAR contents.

Note: The 24CW Series will automatically roll over from the HAR (Byte 1) back to the WPR (Byte 0) if the master continues to Acknowledge the data bytes during the read operation.

FIGURE 8-2: CONFIGURATION REGISTERS READ SEQUENCE



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8.6 Locking the Configuration Registers

The locking mechanism of the Configuration registers is controlled through the CLRB bit found in the WPR byte.

When locking the Configuration registers, a byte write sequence must be sent to the device (see **Section 6.1 "Byte Write"** for additional information). The MSb of the word address must be set to logic '1' in order to write to the Configuration registers.

Note:	The Configuration registers cannot be unlocked once they are locked.

A valid WPR byte with the CCLK and CRLB bits set to a logic '1' must be provided when locking the Configuration registers. If the WPR byte is invalid, the operation will abort, the EEPROM will not Acknowledge any data bytes and the device will not execute the internal write cycle. Refer to **Section 8.2 "Write Protection Register"** for valid WPR byte values.

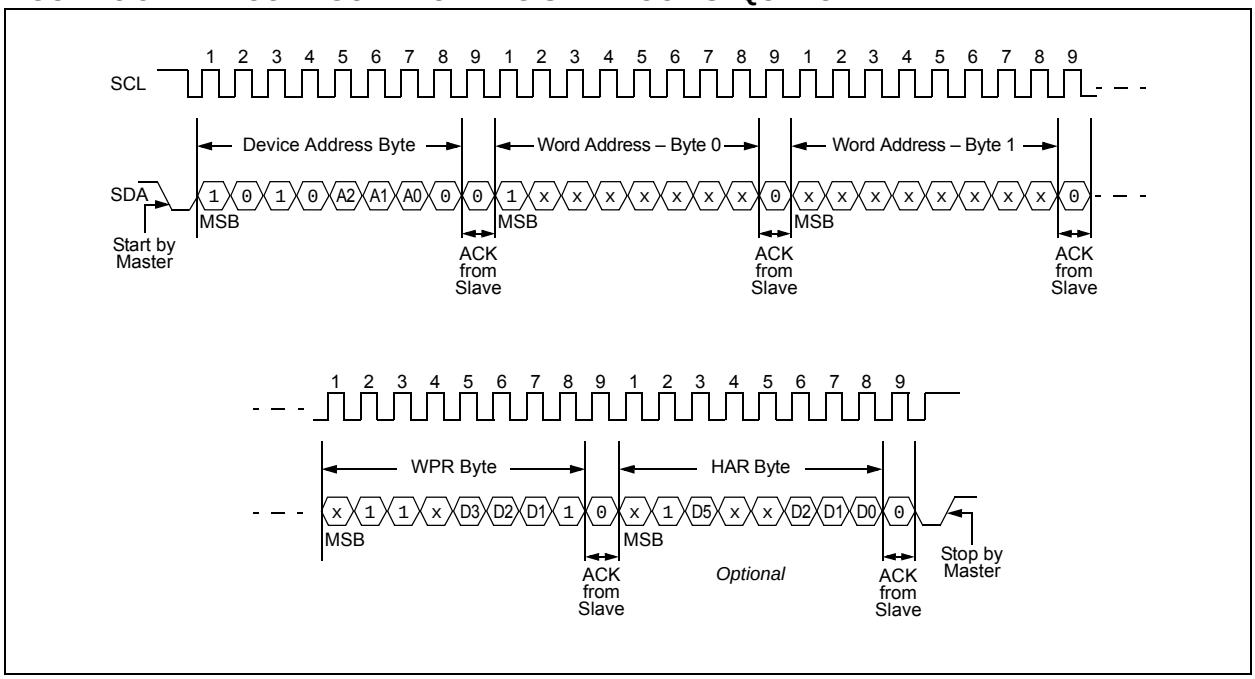
After sending a valid WPR byte, the HAR byte can optionally be sent. If the HAR byte is invalid, the operation will abort, the EEPROM will not Acknowledge any data bytes and the device will not execute the internal write cycle. Refer to **Section 8.3 "Hardware Address Register"** for valid HAR byte values.

It is possible to send only the WPR byte and lock the Configuration registers by omitting the HAR byte and sending a Stop condition after the WPR byte.

Note:	If the HAR byte is omitted, the hardware slave address will be locked with its current values.

Sending more than the WPR and HAR bytes to the 24CW Series will cause the write cycle to abort and the contents of the WPR and HAR will not be changed.

FIGURE 8-3: CONFIGURATION REGISTER LOCK SEQUENCE



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9.0 DEVICE DEFAULT CONDITION

The 24CW Series is delivered with the EEPROM array set to logic ‘1’, resulting in FFh data in all locations of the EEPROM memory array.

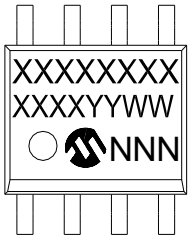
The Write Protection Register (WPR) is set to 00h and the Hardware Address Register (HAR) is preset in accordance with the ordering code selected. For factory preset hardware slave address bits, other than ‘000b’, contact your local sales representative.

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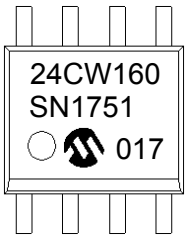
10.0 PACKAGING INFORMATION

10.1 Package Marking Information

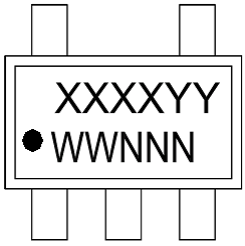
8-Lead 3.9 mm SOIC



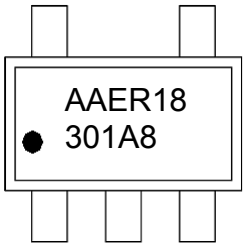
Example



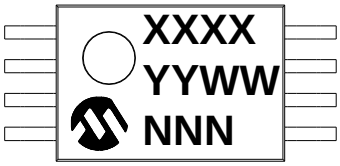
5-Lead SOT-23



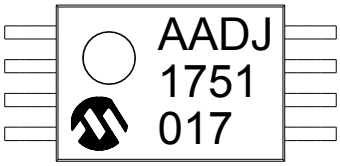
Example



8-Lead 4.4 mm TSSOP



Example



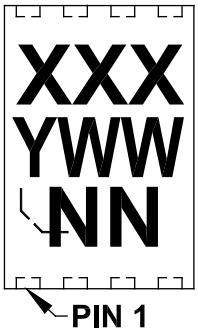
Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	*****	These packages are RoHs compliant. The JEDEC designator can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

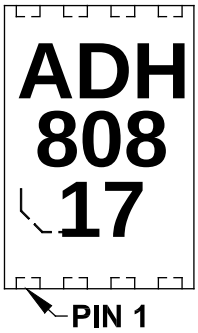
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Package Marking Information (Continued)

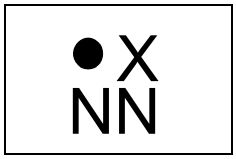
8-Lead 2x3 mm UDFN



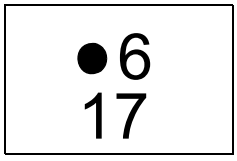
Example



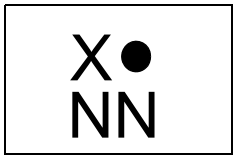
4-Ball 0.4x0.4 mm CSP (CS0)



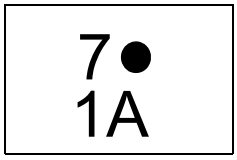
Example



4-Ball 0.5x0.4 mm CSP (CS1)



Example



Part Number	1st Line Marking Codes					
	SOIC	SOT-23	TSSOP	UDFN	CSP (CS0)(1)	CSP (CS1)(2)
24CW16 Series	24CW160	AAEN	AADJ	ADG	—	—
24CW32 Series	24CW320	AAEP	AADK	ADH	—	—
24CW64 Series	24CW640	AAEQ	AADL	ADJ	● 6	6 ●
24CW128 Series	24CW1280	AAER	AADM	ADK	● 7	7 ●

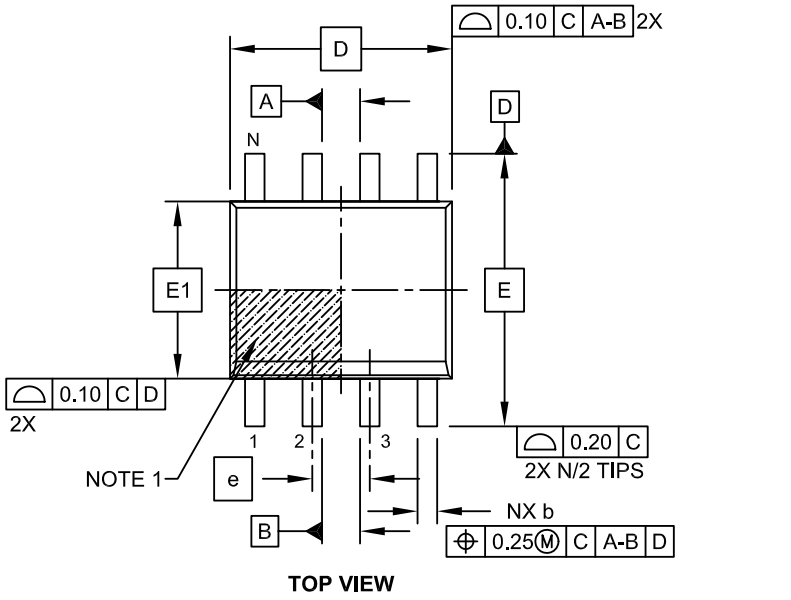
Note 1: CS0 CSP ball pitch is 0.4x0.4 mm.

2: CS1 CSP ball pitch is 0.5x0.4 mm.

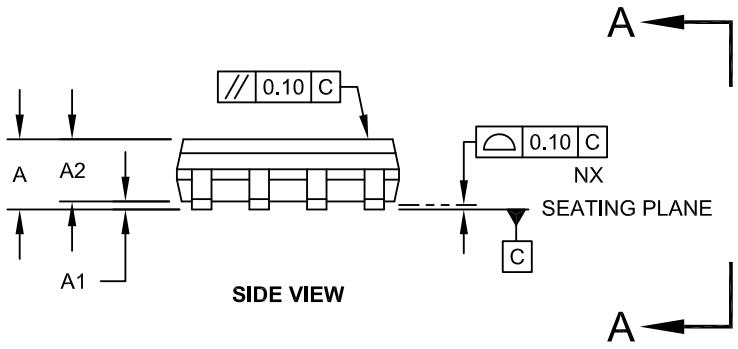
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Web:www.manduic.com Email:sales@manduic.com

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

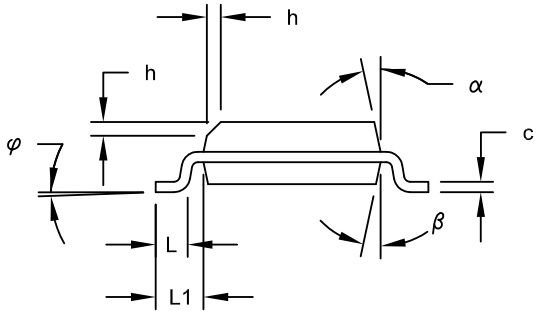
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW



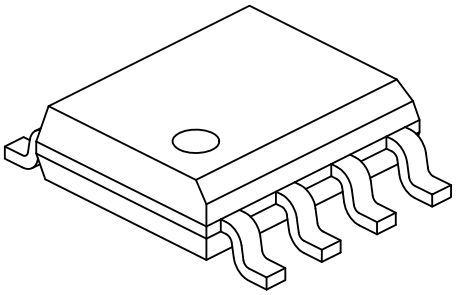
VIEW A-A

Microchip Technology Drawing No. C04-057C Sheet 1 of 2

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8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1		1.04 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.17	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

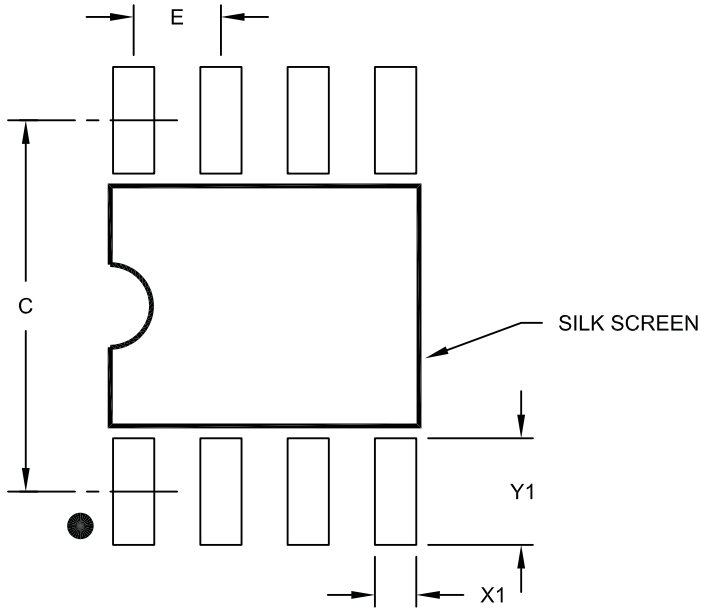
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-057C Sheet 2 of 2

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8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

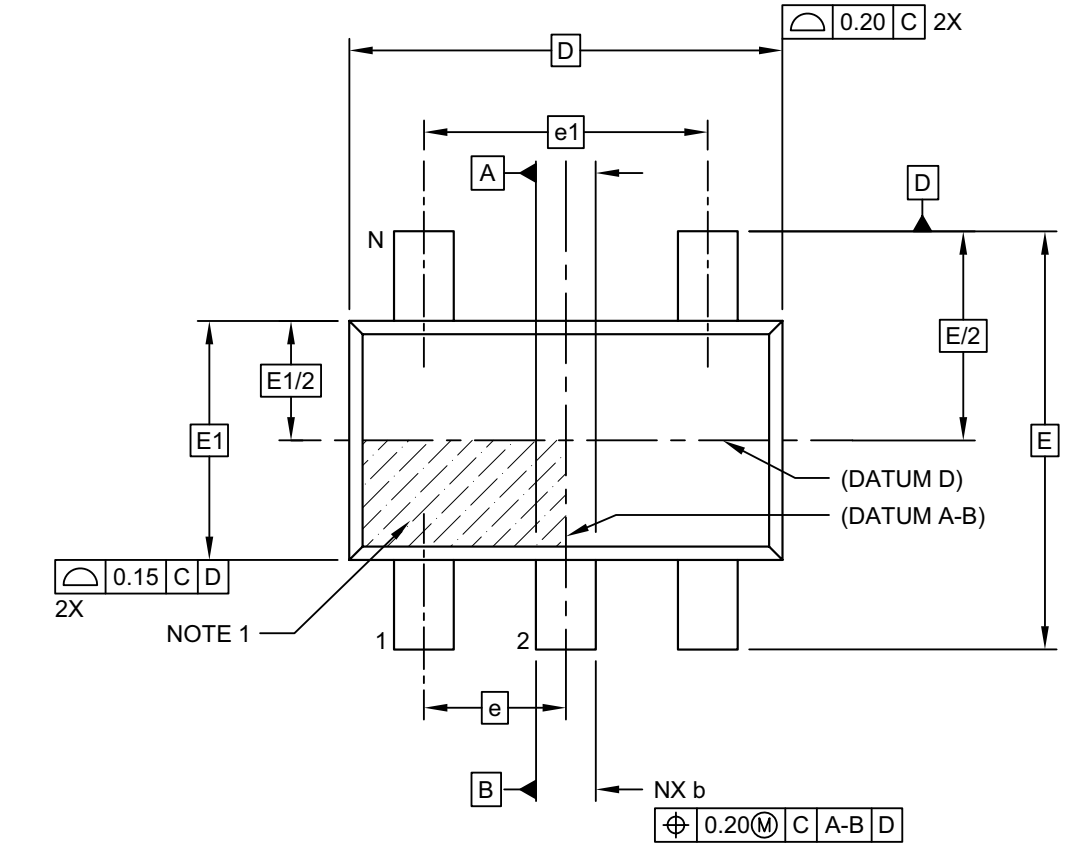
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

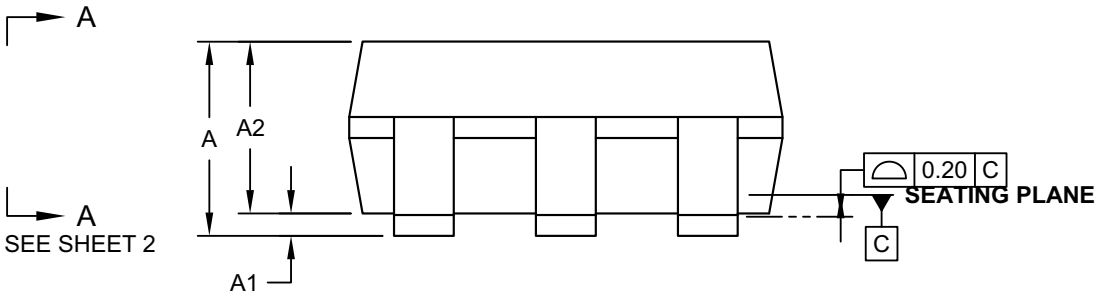
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Web:www.manduic.com Email:sales@manduic.com

5-Lead Plastic Small Outline Transistor (OT) [SOT23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



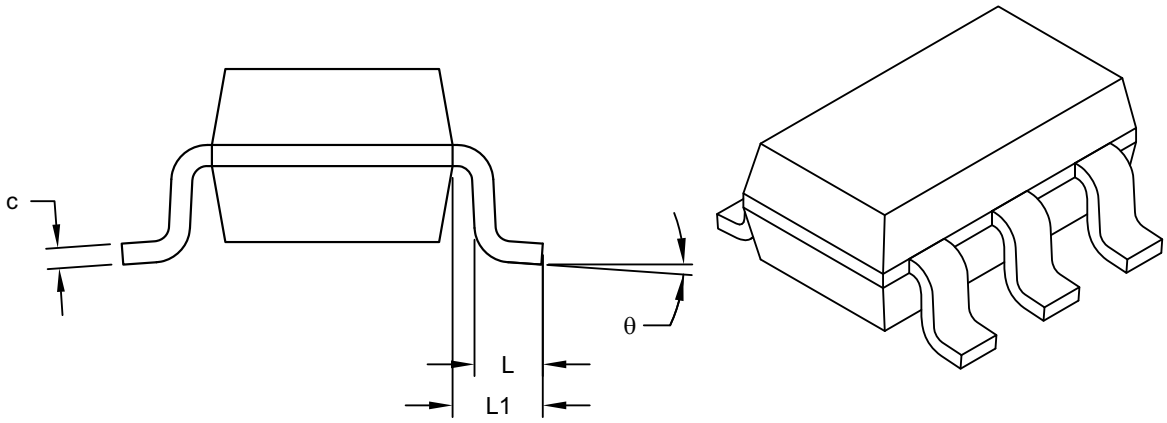
SIDE VIEW

Microchip Technology Drawing C04-028D [OT] Sheet 1 of 2

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5-Lead Plastic Small Outline Transistor (OT) [SOT23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



VIEW A-A
SHEET 1

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		6	
Pitch	e		0.95 BSC	
Outside lead pitch	e1		1.90 BSC	
Overall Height	A	0.90	-	1.45
Molded Package Thickness	A2	0.89	-	1.30
Standoff	A1	-	-	0.15
Overall Width	E		2.80 BSC	
Molded Package Width	E1		1.60 BSC	
Overall Length	D		2.90 BSC	
Foot Length	L	0.30	-	0.60
Footprint	L1		0.60 REF	
Foot Angle	ϕ	0°	-	10°
Lead Thickness	c	0.08	-	0.26
Lead Width	b	0.20	-	0.51

Notes:

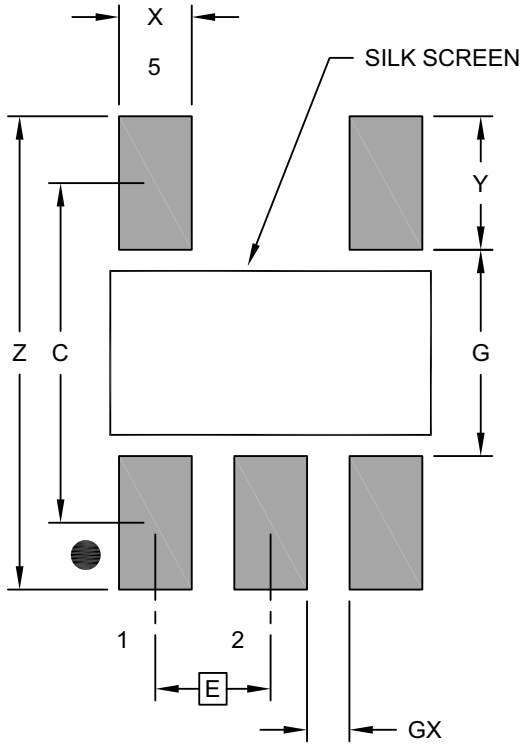
1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-091D [OT] Sheet 2 of 2

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5-Lead Plastic Small Outline Transistor (OT) [SOT23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.95 BSC	
Contact Pad Spacing	C		2.80	
Contact Pad Width (X5)	X			0.60
Contact Pad Length (X5)	Y			1.10
Distance Between Pads	G	1.70		
Distance Between Pads	GX	0.35		
Overall Width	Z			3.90

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

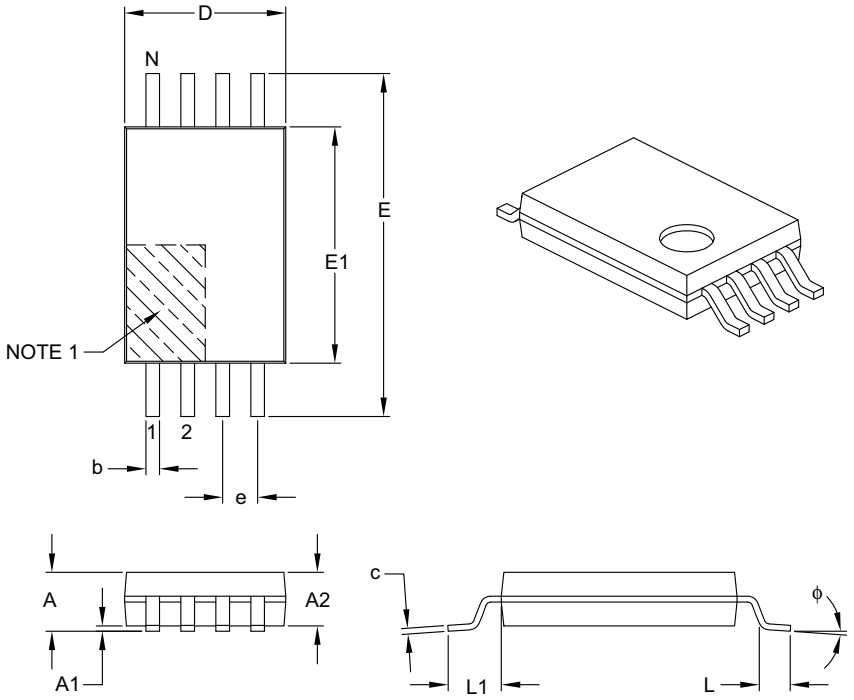
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2091A [OT]

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8-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.80	1.00	1.05
Standoff	A1	0.05	–	0.15
Overall Width	E		6.40 BSC	
Molded Package Width	E1	4.30	4.40	4.50
Molded Package Length	D	2.90	3.00	3.10
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	ϕ	0°	–	8°
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.19	–	0.30

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

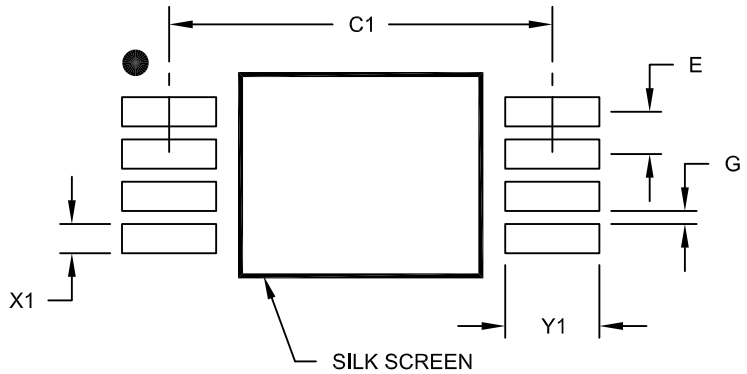
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-086B

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8-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C1		5.90	
Contact Pad Width (X8)	X1			0.45
Contact Pad Length (X8)	Y1			1.45
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

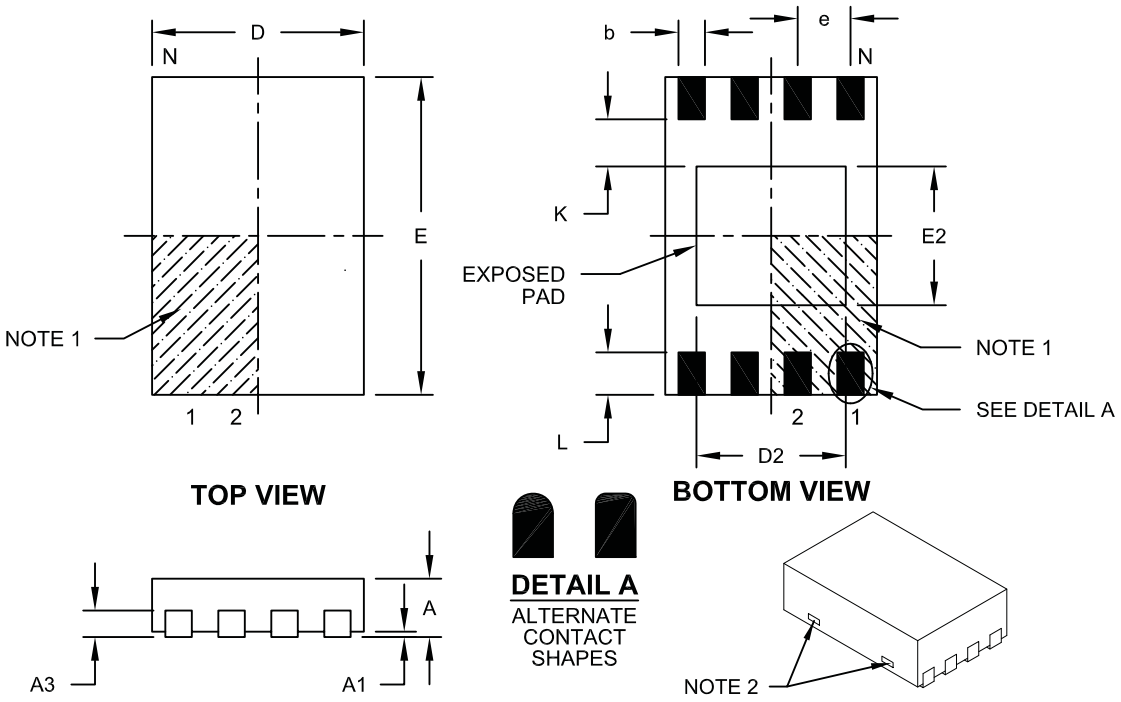
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2086A

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8-Lead Plastic Dual Flat, No Lead Package (MU) – 2x3x0.5 mm Body [UDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.50 BSC	
Overall Height	A	0.45	0.50	0.55
Standoff	A1			0.07
Contact Thickness	A3		0.127 REF	
Overall Length	D	1.95	2.00	2.05
Overall Width	E	2.95	3.00	3.05
Exposed Pad Length	D2	1.30	1.40	1.50
Exposed Pad Width	E2	1.20	1.30	1.40
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.25	0.30	0.35
Contact-to-Exposed Pad	K		0.55 REF	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated
4. Dimensioning and tolerancing per ASME Y14.5M

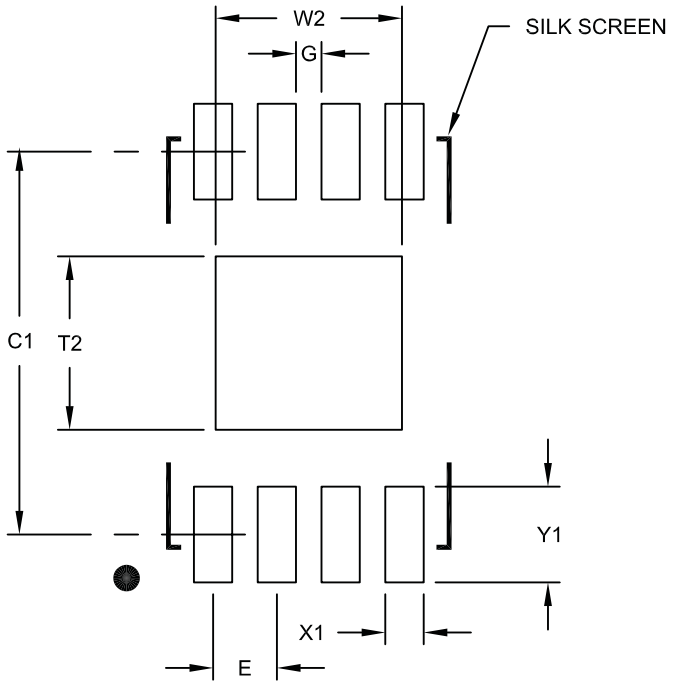
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-136B

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8-Lead Plastic Dual Flat, No Lead Package (MU) – 2x3x0.5 mm Body [UDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	W2			1.46
Optional Center Pad Length	T2			1.36
Contact Pad Spacing	C1		3.00	
Contact Pad Width (X8)	X1			0.30
Contact Pad Length (X8)	Y1			0.75
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

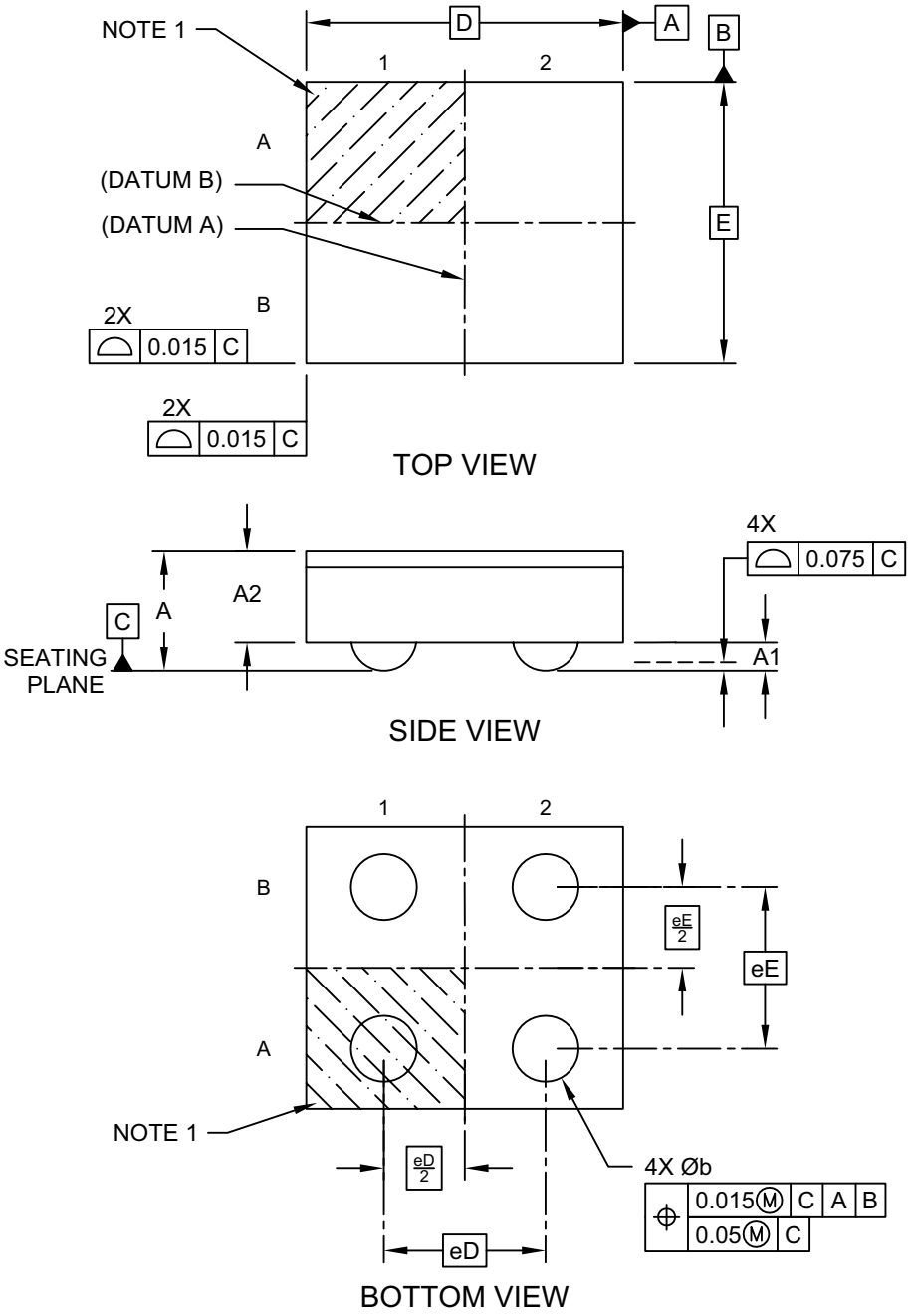
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2136A

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4-Ball Wafer Level Chip Scale Package (CS) - 0.4x0.4 mm Ball Pitch [CSP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

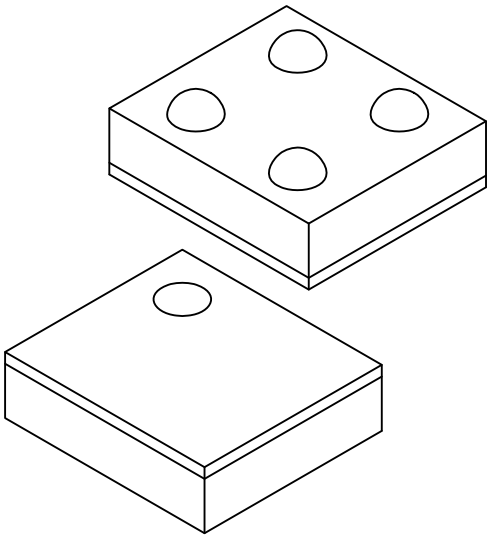


Microchip Technology Drawing C04-6047 Rev. B Sheet 1 of 2

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4-Ball Wafer Level Chip Scale Package (CS) - 0.4x0.4 mm Ball Pitch [CSP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		4	
Bump Pitch	eD		0.40 BSC	
Bump Pitch	eE		0.40 BSC	
Overall Height	A	0.260	0.295	0.330
Standoff	A1	-	0.070	-
Die Height	A2	-	0.225	-
Overall Length	D		Contact Microchip for details	
Overall Width	E		Contact Microchip for details	
Terminal Width	b		0.163 TYP	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

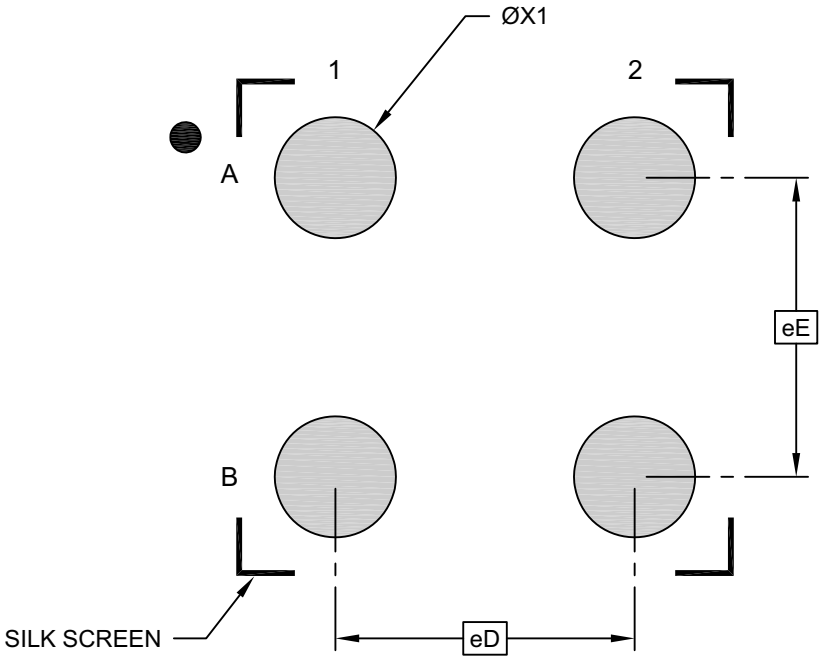
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-6047 Rev. B Sheet 2 of 2

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4-Ball Wafer Level Chip Scale Package (CS) - 0.4x0.4 mm Ball Pitch [CSP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	eD		0.40 BSC	
Contact Pitch	eE		0.40 BSC	
Contact Diameter	ØX1		0.163	

Notes:

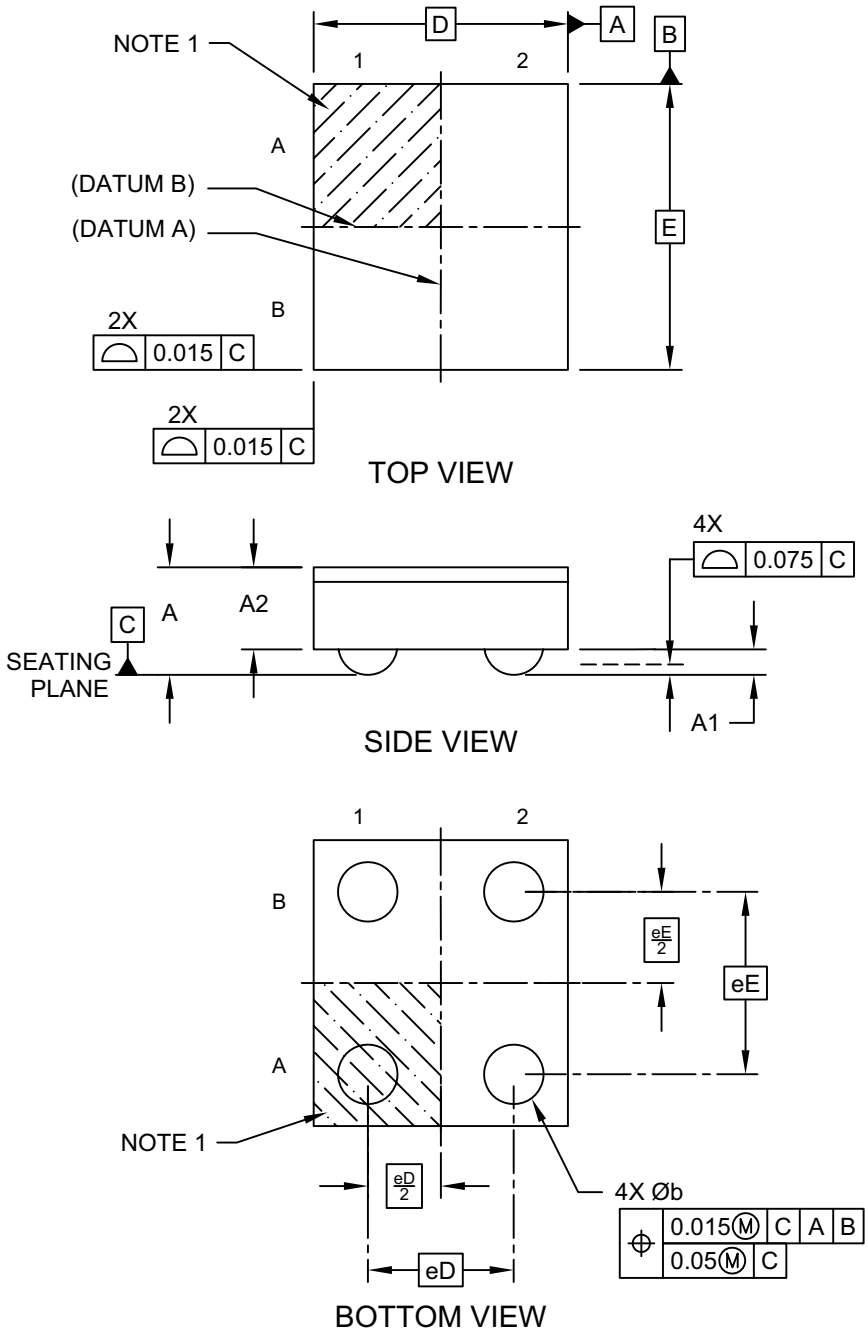
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-8047 Rev. B

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4-Ball Wafer Level Chip Scale Package (CS) - 0.4x0.5 mm Ball Pitch [CSP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

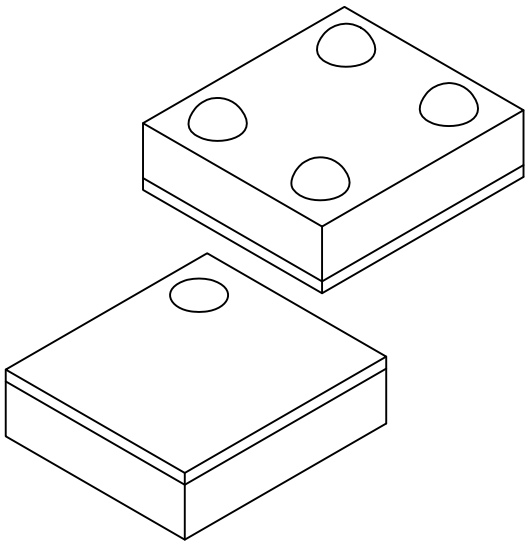


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4-Ball Wafer Level Chip Scale Package (CS) - 0.4x0.5 mm Ball Pitch [CSP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N	4		
Bump Pitch	eD	0.40 BSC		
Bump Pitch	eE	0.50 BSC		
Overall Height	A	0.260	0.295	0.330
Standoff	A1	-	0.070	-
Die Height	A2	-	0.225	-
Overall Length	D	Contact Microchip for details		
Overall Width	E	Contact Microchip for details		
Terminal Width	b	0.163 TYP		

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

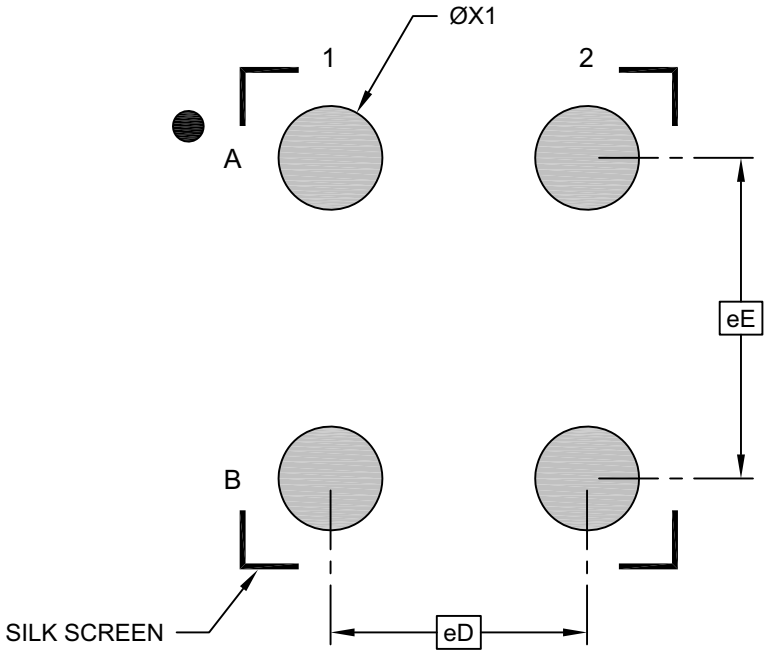
   REF: Reference Dimension, usually without tolerance, for information purposes only.

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4-Ball Wafer Level Chip Scale Package (CS) - 0.4x0.5 mm Ball Pitch [CSP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	eD		0.40 BSC	
Contact Pitch	eE		0.50 BSC	
Contact Diameter	ØX1		0.163	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

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APPENDIX A: REVISION HISTORY

Revision A (10/2017)

Initial release of this document.

Revision B (07/2018)

Added the 24CW128X device; Updated the CSP package drawings; Changed the 8-pad UDFN package code from MU to MUY; Added Data Retention test conditions; Removed Preliminary status.

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PRODUCT IDENTIFICATION SYSTEM

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PART NO.	X[1]	[X][1]	X	/XX
Device	Slave Address	Tape and Reel Option	Temperature Range	Package

Device:	24CW16	= 16-Kbit I^2C Compatible Serial EEPROM with Software Write Protection
	24CW32	= 32-Kbit I^2C Compatible Serial EEPROM with Software Write Protection
	24CW64	= 64-Kbit I^2C Compatible Serial EEPROM with Software Write Protection
	24CW128	= 128-Kbit I^2C Compatible Serial EEPROM with Software Write Protection
Slave Address:[1]	0	= Hardware Slave Address '000b'
	1	= Hardware Slave Address '001b'
	2	= Hardware Slave Address '010b'
	3	= Hardware Slave Address '011b'
	4	= Hardware Slave Address '100b'
	5	= Hardware Slave Address '101b'
	6	= Hardware Slave Address '110b'
	7	= Hardware Slave Address '111b'
Tape and Reel Option:	Blank	= Standard Packaging (tube or tray)
	T	= Tape and Reel[1]
Temperature Range:	I	= -40°C to +85°C (Industrial)
Package:	SN	= 8-Lead Plastic Small Outline – Narrow, 3.90 mm Body
	OT	= 5-Lead Plastic Small Outline Transistor
	ST	= 8-Lead Plastic Thin Shrink Small Outline – 4.4 mm Body
	MUY	= 8-Lead Plastic Dual Flat, No Lead Package – 2x3x0.5 mm
	CS0668	= 4-Ball Extremely Thin Fine Pitch Wafer Level Chip Scale Package – 0.4x0.4 mm Pitch
	CS1668	= 4-Ball Extremely Thin Fine Pitch Wafer Level Chip Scale Package – 0.5x0.4 mm Pitch

Examples:

a) 24CW160-I/SN = 16-Kbit, Slave Address 0, Industrial Temp., SOIC Package.

b) 24CW320T-I/SN = 32-Kbit, Slave Address 0, Tape and Reel, Industrial Temp., SOIC Package.

c) 24CW640-I/SN = 64-Kbit, Slave Address 0, Industrial Temp., SOIC Package.

d) 24CW1280T-I/SN = 128-Kbit, Slave Address 0, Tape and Reel, Industrial Temp., SOIC Package.

e) 24CW320-I/ST = 32-Kbit, Slave Address 0, Industrial Temp., TSSOP Package.

f) 24CW640T-I/ST = 64-Kbit, Slave Address 0, Tape and Reel, Industrial Temp., TSSOP Package.

g) 24CW160T-I/OT = 16-Kbit, Slave Address 0, Tape and Reel, Industrial Temp., SOT-23 Package.

h) 24CW320T-I/OT = 32-Kbit, Slave Address 0, Tape and Reel, Industrial Temp., SOT-23 Package.

i) 24CW1280T-I/OT = 128-Kbit, Slave Address 0, Tape and Reel, Industrial Temp., SOT-23 Package.

j) 24CW320T-I/MUY = 32-Kbit, Slave Address 0, Tape and Reel, Industrial Temp., UDFN Package.

k) 24CW640T-I/MUY = 64-Kbit, Slave Address 0, Tape and Reel, Industrial Temp., UDFN Package.

l) 24CW640T-I/CS0668 = 64-Kbit, Slave Address 0, Tape and Reel, Industrial Temp., CS0 Package.

m) 24CW640T-I/CS1668 = 64-Kbit, Slave Address 0, Tape and Reel, Industrial Temp., CS1 Package.

n) 24CW1280T-I/CS0668 = 128-Kbit, Slave Address 0, Tape and Reel, Industrial Temp., CS0 Package.

o) 24CW1280T-I/CS1668 = 128-Kbit, Slave Address 0, Tape and Reel, Industrial Temp., CS1 Package.

Note 1: Slave Address and Tape and Reel identifiers only appear in the catalog part number description. These identifiers are used for ordering purposes and are not printed on the device package. Check with your Microchip Sales Office for availability.

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