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Product Specification

XBLW 24C02

Two-Wire Serial EEPROM 2K(8-bit wide)

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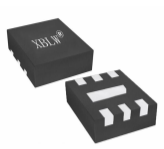


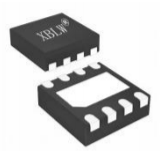
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Description

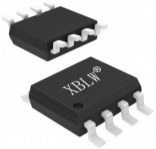
The 24C02 is 2048 bits of serial Electrical Erasable and Programmable Read Only Memory, Commonly known as EEPROM.They are organized as 25 6 words of 8 bits (1 byte) each.The devices are fabricated with proprietary advanced CMOS process for low power and low voltage applications. These devices are available in standard 8-lead DIP, 8-lead SOP, 8-lead MSOP, 8-lead TSSOP, 8-lead DFN,6-lead DFN and 5-lead SOT-23 packages. A standard 2 wire serial interface is used to address all read and write functions. Our extended V_{CC} range (1.8V to 5.5V) devices enables wide spectrum of applications.















Feature

- Low voltage and low power operations:
  24C02: VCC = 1 . 8V to 5 . 5V, Industrial temperature range (-40°C to 85°C) .
  24C02: With 3 bits device address, the devices are suitable for all application.(For use of 5 pins package, the device address A2,A1,and A0 bits must be set to zero)
- 16 bytes page write mode.
- Partial page write operation allowed.
- Internally organized: 256 × 8 (2K).
- Standard 2- wire bi-directional serial interface.
- Schmitt trigger, filtered inputs for noise protection.
- Self-timed programming cycle (5 ms maximum) .
- 1 MHz (2.5-5V), 400 kHz (1.8V) Compatibility.
- Automatic erase before write operation.
- Write protect pin for hardware data protection.
- High reliability: typically 1,000,000 cycles endurance.
- 100 years data retention.
- Standard 8-pin DIP/SOP/MSOP/TSSOP/DFN,6-pin DFN and 5-pin SOT-23 Pb-free packages .

Ordering Information

Product Model	Package Type	Marking	Packing	Packing Qty
XBLW 24C02S	SOT23-5	24C02S	Tape	3000Pcs/Reel
XBLW 24C02N	DIP-8	24C02N	Tube	2000Pcs/Box
XBLW 24C02BN	SOP-8	24C02BN	Tape	4000Pcs/Reel
XBLW 24C02MN	MSOP-8	02MN	Tape	5000Pcs/Reel
XBLW 24C02TN	TSSOP-8	02TN	Tape	5000Pcs/Reel
XBLW 24C02DN	DFN-8	02D8	Tape	5000Pcs/Reel
XBLW 24C02D6	DFN-6	02D6	Tape	4000Pcs/Reel

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PIN CONFIGURATION

Pin Name	Pin Function
A2 , A1, A0	Device Address Inputs
SDA	Serial Data Input / Open Drain Output
SCL	Serial Clock Input
WP	Write Protect
Vcc	Power Supply
GND	Ground
NC	No- Connect

Table 1

All these packaging types come in conventional or Pb- free certified.

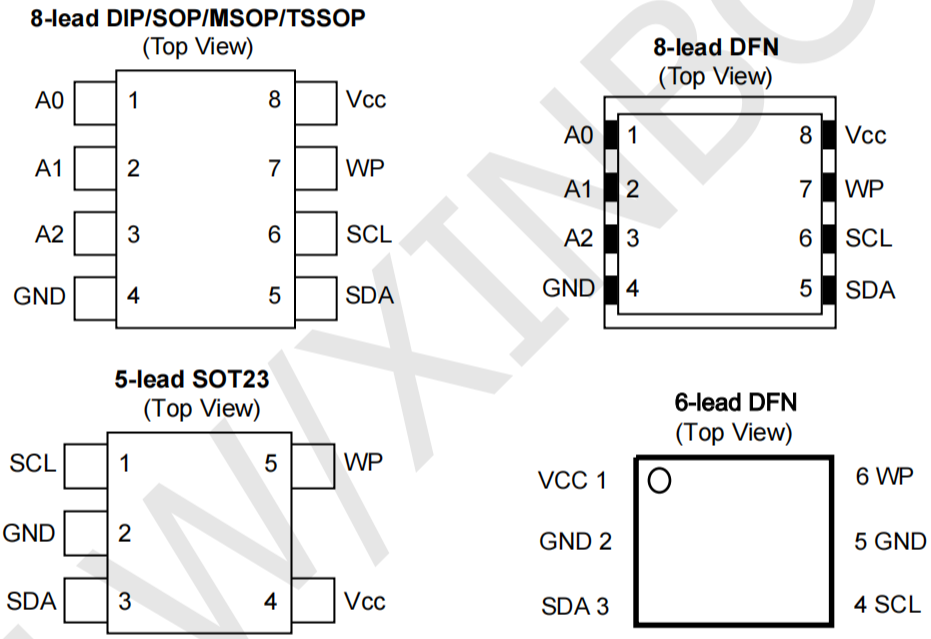


Figure 1: Package types

ABSOLUTE MAXIMUM RATINGS

Parameter	Parameter value	Unit
Industrial operating temperature	-40~+85	℃
Storage temperature	-50~+125	℃
Maximum voltage	8	V
ESD protection on all pins	＞2000	V
Input voltage on any pin relative to ground ： -0.3V to VCC + 0.3V		

* Stresses exceed those listed under "Absolute Maximum Rating"may cause permanent damage to the device.Functional operation of the device at conditions beyond those listed in the specification is not guaranteed.Prolonged exposure to extreme conditions may affect device reliability or functionality.

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Block Diagram

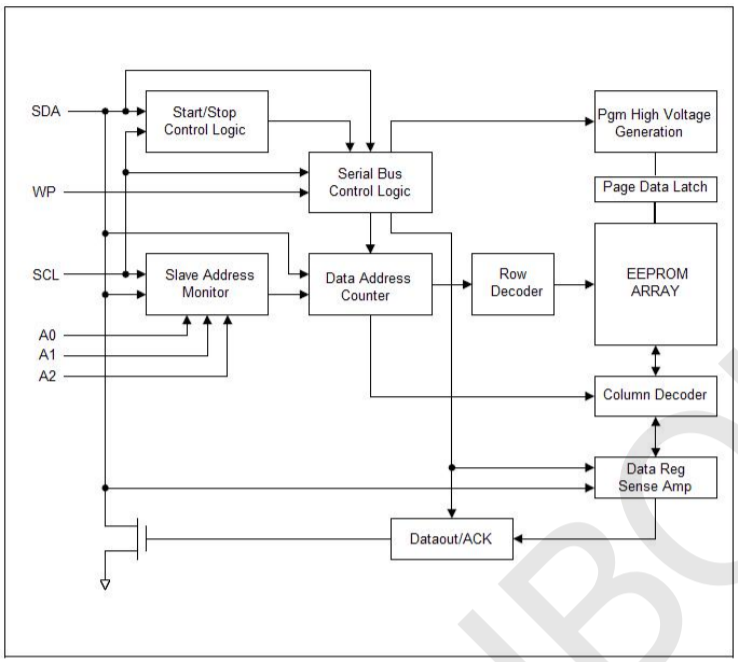


Figure 2: Block Diagram

PIN DESCRIPTIONS

(A) SERIAL CLOCK (SCL)

The rising edge of this SCL input is to latch data into the EEPROM device while the falling edge of this clock is to clock data out of the EEPROM device.

(B) SERIAL DATA LINE (SDA)

SDA data line is a bi-directional signal for the serial devices. It is an open drain output signal and can be wired OR with other open-drain output devices.

(C) DEVICE / CHIP SELECT ADDRESSES (A2, A1, A0)

These are the chip select input signals for the serial EEPROM devices. Typically, these signals are hardwired to either V_{IH} or V_{IL}. If left unconnected, they are internally recognized as V_{IL}. However, due to capacitive coupling that may appear in customer applications, recommends always connecting the address pins to a known state. When using a pull-up or pull-down resistor, recommends using 10kΩ or less.

(D) WRITE PROTECT (WP)

The 24C02 devices have a WP pin to protect the whole EEPROM array from programming. Programming operations are allowed if WP pin is left un-connected or input to V_{IL}. Conversely all programming functions are disabled if WP pin is connected to V_{IH} or V_{CC}. Read operations is not affected by the WP pin's input level. If left unconnected, it is internally recognized as V_{IL}. However, due to capacitive coupling that may appear in customer applications, recommends always connecting the WP pin to a known state. When using a pull-up or pull-down resistor, recommends using 10kΩ or less.

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MEMORY ORGANIZATION

The 24C02 devices have 16 pages. Since each page has 16 bytes, random word addressing to 24C02 willrequire 8 bits data word addresses.

DEVICE OPERATION

(A) SERIAL CLOCK AND DATA TRANSITIONS

The SDA pin is typically pulled to high by an external resistor. Data is allowed to change only when Serial clock SCL is at V_{IL}. Any SDA signal transition may interpret as either a START or STOP condition as described below.

(B) START CONDITION

With SCL ≥ V_{IH}, a SDA transition from high to low is interpreted as a START condition. All valid commands must begin with a START condition.

(C) STOP CONDITION

With SCL ≥ V_{IH}, a SDA transition from low to high is interpreted as a STOP condition. All valid read or write commands end with a STOP condition. The device goes into the STANDBY mode if it is after a read command.A STOP condition after page or byte write command will trigger the chip into the STANDBY mode after the self timed internal programming finish.

(D) ACKNOWLEDGE

The 2-wire protocol transmits address and data to and from the EEPROM in 8 bit words. The EEPROM acknowledges the data or address by outputting a "0" after receiving each word. The ACKNOWLEDGE signal occurs on the 9^{th} serial clock after each word.

(E) STANDBY MODE

The EEPROM goes into low power STANDBY mode after a fresh power up, after receiving a STOP bit in read mode, or after completing a self-time internal programming operation.

(F) SOFT RESET

After an interruption in protocol power loss or system reset, any two-wire part can be reset by following these steps:

1. Creat a START condition,
2. Clock eighteen data bits “ 1”,
3. Creat a start condition as SDA is high

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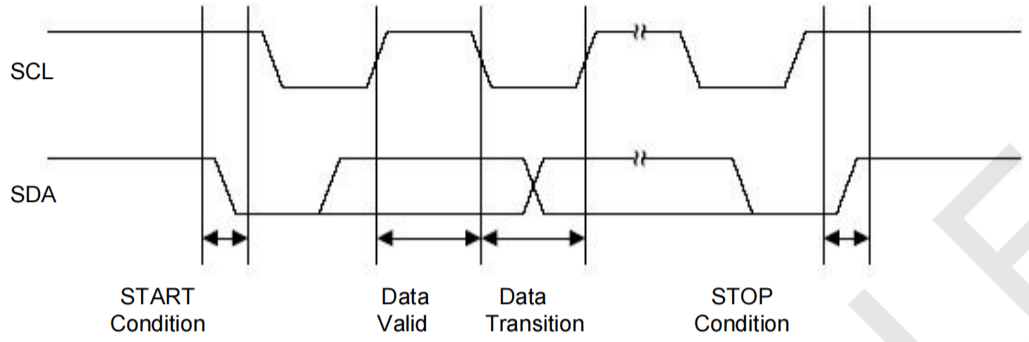


Figure 3: Timing diagram for START and STOP conditions

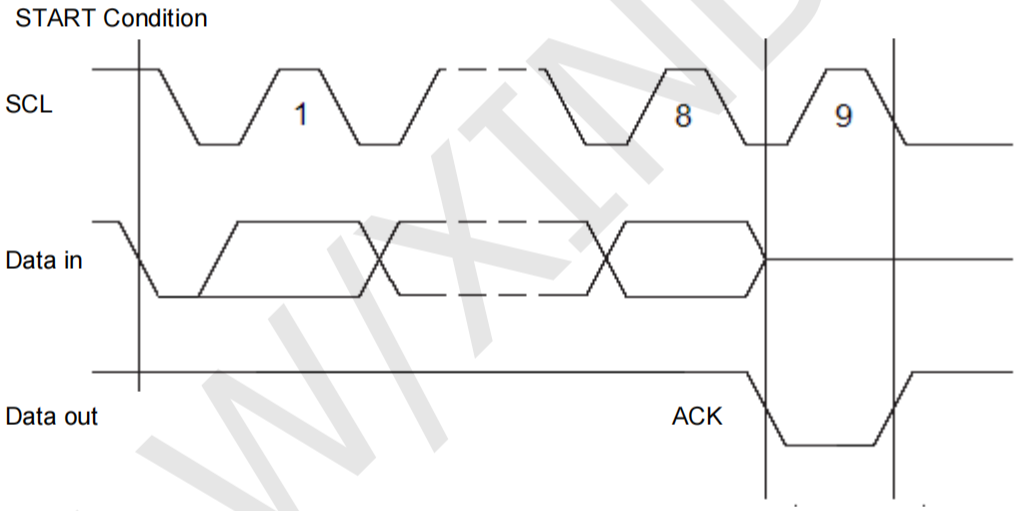


Figure 4: Timing diagram for output ACKNOWLEDGE

DEVICE ADDRESSING

The 2-wire serial bus protocol mandates an 8 bits device address word after a START bit condition to invoke valid read or write command. The first four most significant bits of the device address must be 1010, which is common to all serial EEPROM devices. The next three bits are device address bits. These three device address bits (5^{th} , 6^{th} and 7^{th}) are to match with the external chip select/address pin states. If a match is made, the EEPROM device outputs an ACKNOWLEDGE signal after the 8^{th} read/write bit, otherwise the chip will go into STANDBY mode.

The last or 8^{th} bit is a read/write command bit. If the 8^{th} bit is at VIH then the chip goes into read mode. If a "0" is detected, the device enters programming mode.

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WRITE OPERATIONS

(A) BYTE WRITE

A byte write operation starts when a micro-controller sends a START bit condition, follows by a proper EEPROM device address and then a write command. If the device address bits match the chip select address, the EEPROM device will acknowledge at the 9th clock cycle. The micro-controller will then send the rest of the lower 8 bits word address. At the 18th cycle, the EEPROM will acknowledge the 8-bit address word. The micro-controller will then transmit the 8 bit data. Following an ACKNOWLDEGE signal from the EEPROM at the 27th clock cycle, the micro-controller will issue a STOP bit. After receiving the STOP bit, the EEPROM will go into a self- timed programming mode during which all external inputs will be disabled. After a programming time of T_{WC}, the byte programming will finish and the EEPROM device will return to the STANDBY mode.

(B) PAGE WRITE

A page write is similar to a byte write with the exception that one to sixteen bytes can be programmed along the same page or memory row. All 24C02 are organized to have 16 bytes per memory row or page.

With the same write command as the byte write, the micro-controller does not issue a STOP bit after sending the 1st byte data and receiving the ACKNOWLEDGE signal from the EEPROM on the 27th clock cycle. Instead it sends out a second 8-bit data word, with the EEPROM acknowledging at the 36th cycle. This data sending and EEPROM acknowledging cycle repeats until the micro-controller sends a STOP bit after the n × 9th clock cycle. After which the EEPROM device will go into a self-timed partial or full page programming mode. After the page programming completes after a time of T_{WC}, the devices will return to the STANDBY mode.

The least significant 4 bits of the word address (column address) increments internally by one after receiving each data word. The rest of the word address bits (row address) do not change internally, but pointing to a specific memory row or page to be programmed. The first page write data word can be of any column address. Up to 16 data words can be loaded into a page. If more then 16 data words are loaded, the 17th data word will be loaded to the 1st

(C) ACKNOWLEDGE POLLING

ACKNOWLEDGE polling may be used to poll the programming status during a self-timed internal rogramming. By issuing a valid read or write address command, the EEPROM will not acknowledge at the 9th clock cycle if the device is still in the self-timed programming mode. However, if the programming completes and the chip has returned to the STANDBY mode, the device will return a valid ACKNOWLEDGE signal at the 9th clock cycle.

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READ OPERATIONS

The read command is similar to the write command except the 8th read/write bit in address word is set to "1". The three read operation modes are described as follows:

(A) CURRENT ADDRESS READ

The EEPROM internal address word counter maintains the last read or write address plus one if the power supply to the device has not been cut off. To initiate a current address read operation, the micro-controller issues a START bit and a valid device address word with the read/write bit (8th) set to "1". The EEPROM will response with an ACKNOWLEDGE signal on the 9th serial clock cycle. An 8-bit data word will then be serially clocked out. The internal address word counter will then automatically increase by one. For current address read the micro-controller will not issue an ACKNOWLEDGE signal on the 18th clock cycle. The micro-controller issues a valid STOP bit after the 18th clock cycle to terminate the read operation. The device then returns to STANDBY mode.

(B) SEQUENTIAL READ

The sequential read is very similar to current address read. The micro-controller issues a START bit and a valid device address word with read/write bit (8th) set to "1". The EEPROM will response with an ACKNOWLEDGE signal on the 9th serial clock cycle. An 8-bit data word will then be serially clocked out. Meanwhile the internally address word counter will then automatically increase by one. Unlike current address read, the micro-controller sends an ACKNOWLEDGE signal on the 18th clock cycle signaling the EEPROM device that it wants another byte of data. Upon receiving the ACKNOWLEDGE signal, the EEPROM will serially clocked out an 8-bit data word based on the incremented internal address counter. If the micro-controller needs another data, it sends out an ACKNOWLEDGE signal on the 27th clock cycle. Another 8-bit data word will then be serially clocked out. This sequential read continues as long as the micro-controller sends an ACKNOWLEDGE signal after receiving a new data word. When the internal address counter reaches its maximum valid address, it rolls over to the beginning of the memory array address.

Similar to current address read, the micro-controller can terminate the sequential read by not acknowledging the last data word received, but sending a STOP bit afterwards instead.

(C) RANDOM READ

Random read is a two-steps process. The first step is to initialize the internal address counter with a target read address using a "dummy write" instruction. The second step is a current address read. To initialize the internal address counter with a target read address, the micro-controller issues a START bit first, follows by a valid device address with the read/write bit (8th) set to "0". The EEPROM will then acknowledge. The micro-controller will then send the address word. Again the EEPROM will acknowledge. Instead of sending a valid written data to the EEPROM, the micro- controller performs a current address read instruction to read the data. Note that once a START bit is issued, the EEPROM will reset the internal programming process and continue to execute the new instruction - which is to read the current address.

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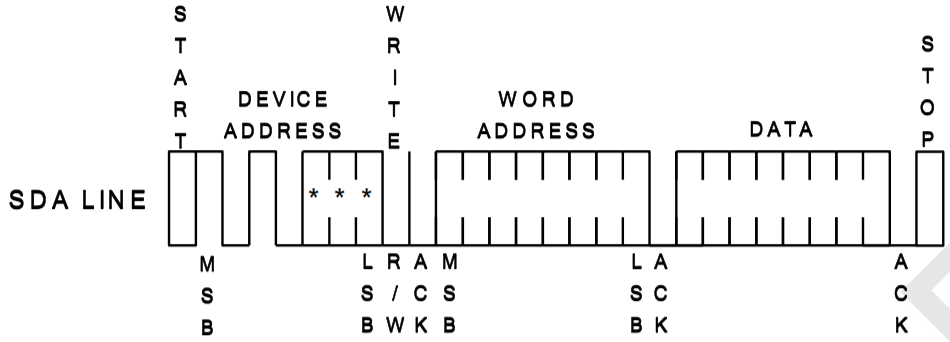


Figure 5: Byte Write

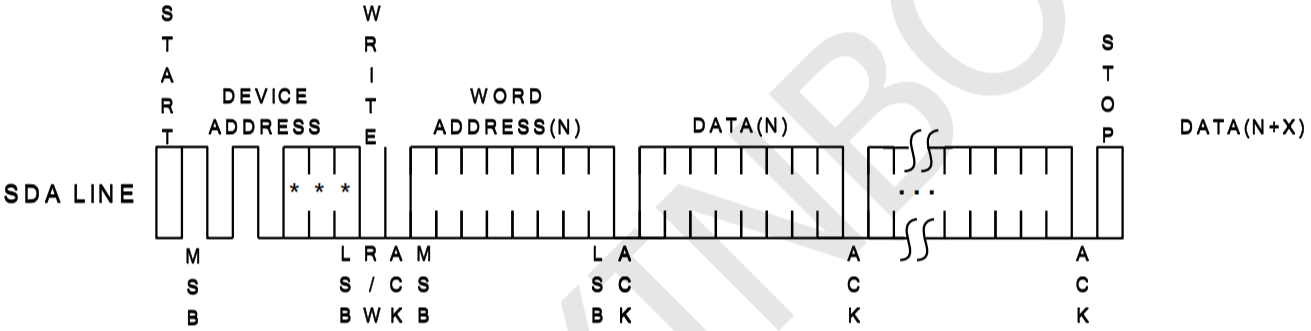


Figure 6: Page Write

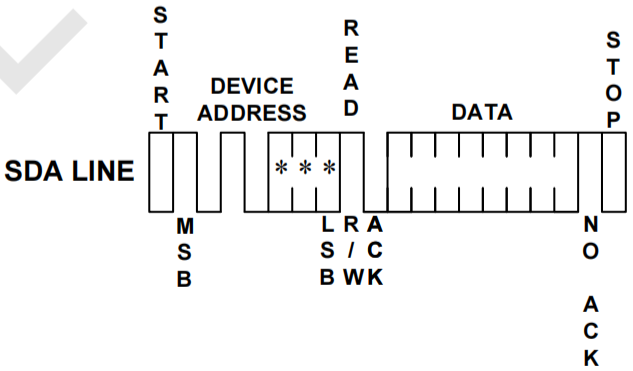


Figure 7: Current Address Read

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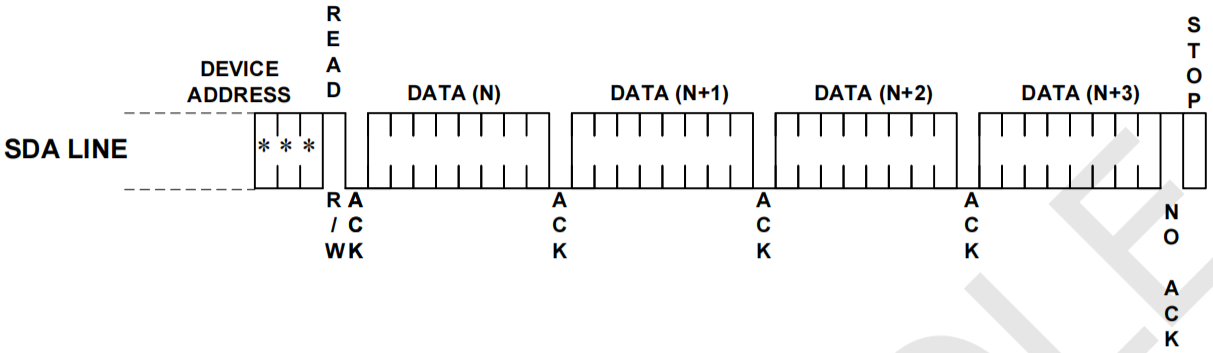


Figure 8: Sequential Read

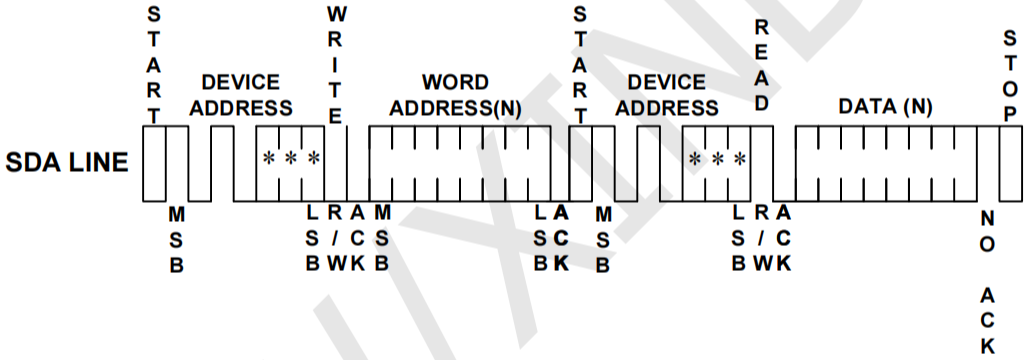


Figure 9: Random Read

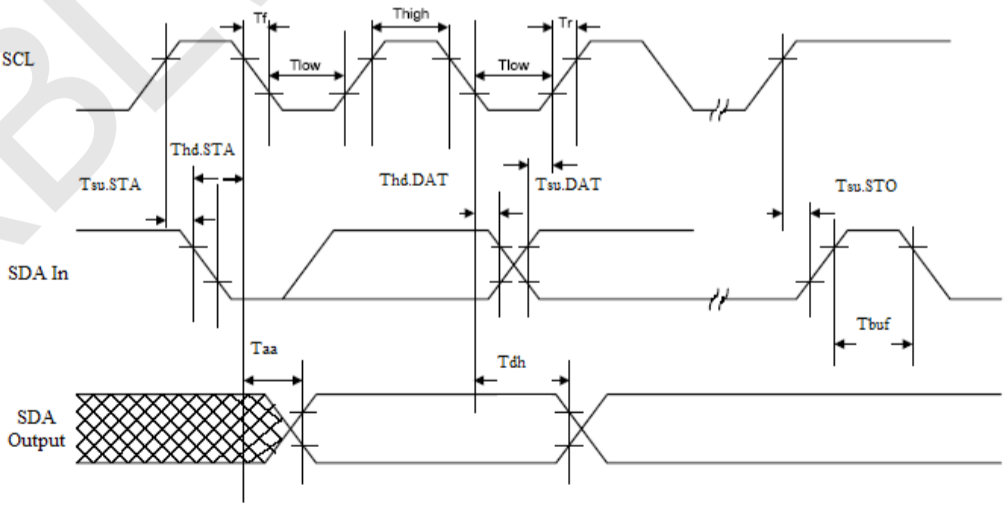


Figure 10: SCL and SDA Bus Timing

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Electrical Specifications

(A) Power-Up Requirements

During a power-up sequence, the V_{CC} supplied to the device should monotonically rise from GND to the minimum V_{CC} level, with a slew rate no faster than 0.05 V/μs and no slower then 0. 1 V/ms. A decoupling cap should be connected to the VCC PAD which is no smaller than 10nF.

(B) Device Reset

To prevent inadvertent write operations or any other spurious events from occurring during a power-up sequence, this device includes a Power-on Reset (POR) circuit. Upon power-up, the device will not respond to any commands until the V_{CC} level crosses the internal voltage threshold (V_{POR}) that brings the device out of Reset and into Standby mode. The system designer must ensure the instructions are not sent to the device until the V_{CC} supply has reached a stable value greater than or equal to the minimum V_{CC} level.

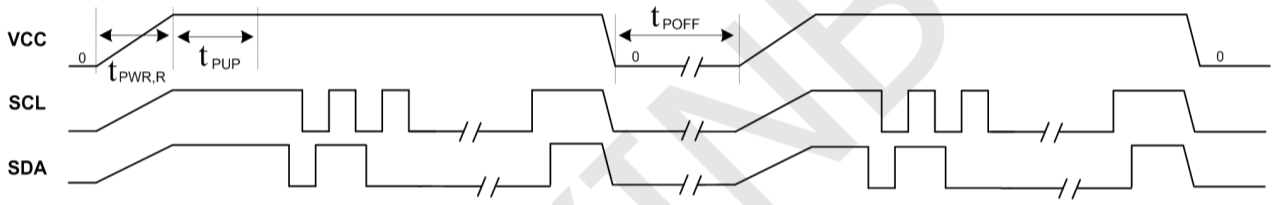


Figure 11: Power on and Power down

If an event occurs in the system where the V_{CC} level supplied to the device drops below the maximum V_{POR} level specified, it is recommended that a full power cycle sequence be performed by first driving the V_{CC} pin to GND, waiting at least the minimum t_{POFF} time and then performing a new power-up sequence in compliance with the requirements defined in this section.

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AC CHARACTERISTICS

Symbol	Parameter	1.8 V		2.5V-5.5 V		Unit
		Min	Max	Min	Max	
f_{SCL}	Clock frequency, SCL		400		1000	kHz
t_{LOW}	Clock pulse width low	1.3		0.4		μs
t_{HIGH}	Clock pulse width high	0.6		0.4		μs
t_I	Noise suppression time(1)		50		50	ns
t_{AA}	Clock low to data out valid	0.2	0.9	0.2	0.55	μs
t_{BUF}	Time the bus must be free before a new transmission can start(1)	1.3		0.5		μs
$t_{HD.STA}$	START hold time	0.6		0.25		μs
$t_{SU.STA}$	START set-up time	0.6		0.25		μs
$t_{HD.DAT}$	Data in hold time	0		0		μs
$t_{SU.DAT}$	Data in set-up time	100		100		ns
t_R	Input rise time(1)		0.3		0.3	μs
t_F	Input fall time(1)		300		100	ns
$t_{SU.STO}$	STOP set-up time	0.6		0.25		μs
t_{DH}	Date out hold time	50		50		ns
$t_{PWR,R}$(1)	Vcc slew rate at power up	0.1	50	0.1	50	V/ms
t_{PUP}(1)	Time required after VCC is stable before the device can accept commands	100		100		μs
t_{POFF}(1)	Minimum time at Vcc=0V between power cycles	500		500		ms
t_{WR}	Write cycle time		5		5	ms
Endurance(1)	25ºC, Page Mode, 3.3V	1,000,000				Write Cycles

Notes: 1. This Parameter is expected by characterization but is not fully screened by test.

2. AC Measurement conditions:

R_L (Connects to Vcc): 1.3KΩ

Input Pulse Voltages: 0.3Vcc to 0.7Vcc

Input and output timing reference Voltages: 0.5Vcc

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DC CHARACTERISTICS

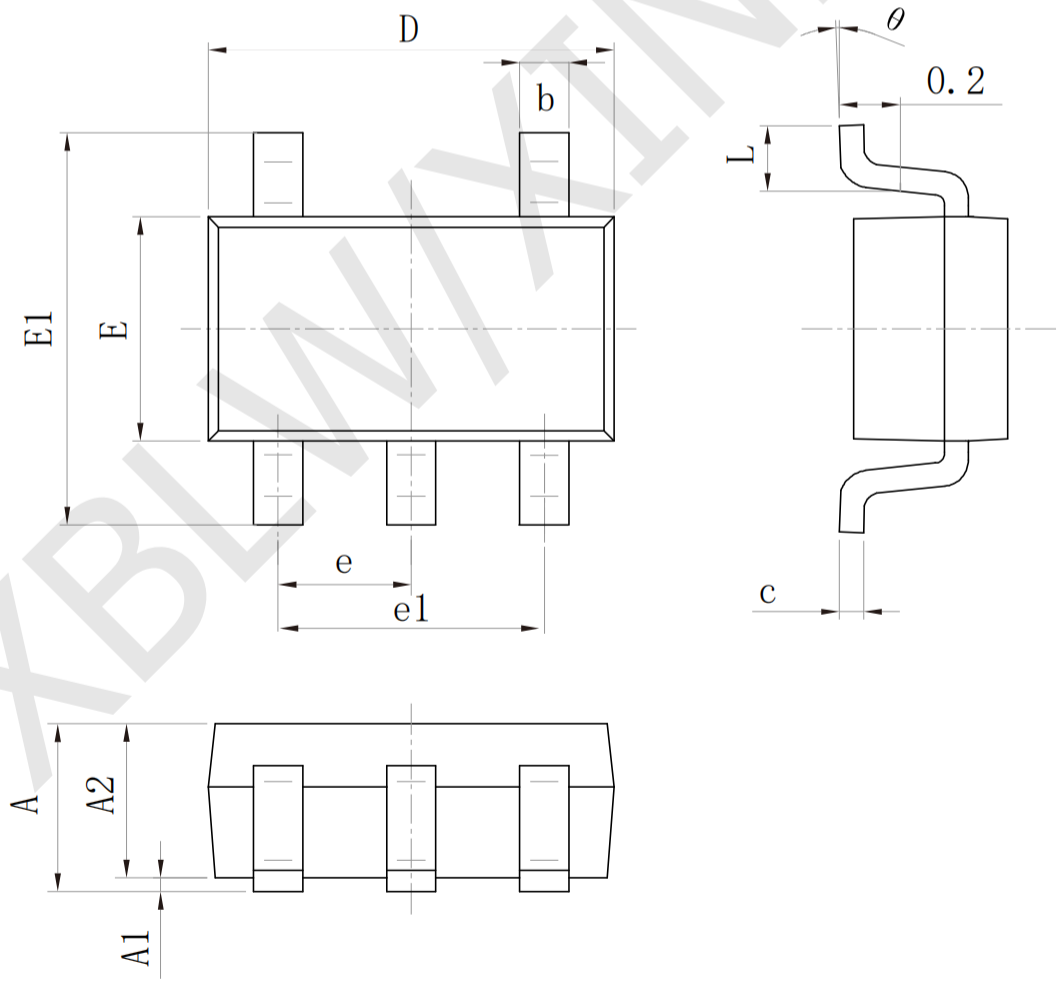
Symbol	Parameter	Test Conditions	Min	Typical	Max	Units
V_{CC1}	Power supply Vcc		1.8		5.5	V
I_{CC1}	Supply read current	Vcc @ 5.0VSCL = 400 kHz		0.5	1.0	mA
I_{CC2}	Supply write current	Vcc @ 5.0V SCL=400 kHz		2.0	3.0	mA
I_{SB1}	Supply current	Vcc @ 1.8V,Vin = Vcc or Vss		<1.0		μA
I_{SB2}	Supply current	Vcc @ 2.5V,Vin = Vcc or Vss		<1.0		μA
I_{SB3}	Supply current	Vcc @ 5.0V,Vin = Vcc or Vss		<1.0		μA
I_{IL}	Input leakage current	Vin = Vcc or Vss			3.0	μA
I_{LO}	Output leakage current	ViN = Vcc or Vss			3.0	μA
V_{IL}	Input low level		-0.6		Vcc× 0.3	V
V_{IH}	Input high level		Vcc × 0.7		Vcc + 0.5	V
V_{OL1}	Output low level	Vcc @ 1.8V,IoL =0. 15 mA			0.2	V
V_{OL2}	Output low level	Vcc @3.0V,IoL =2. 1 mA			0.4	V

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Package Information

- SOT23-5

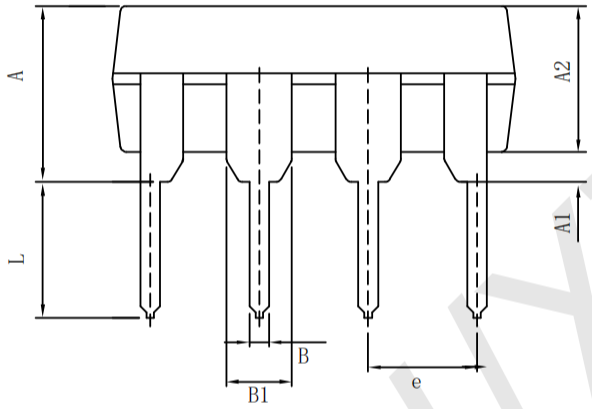
SIZE / SYMBOL	Dimensions In Millimeters		SIZE / SYMBOL	Dimensions In Inches	
	MIN(mm)	MAX(mm)		MIN(in)	MAX(in)
A	1.050	1.250	A	0.041	0.049
A1	0.000	0.100	A1	0.000	0.004
A2	1.050	1.150	A2	0.041	0.045
b	0.300	0.500	b	0.012	0.020
c	0.100	0.200	c	0.004	0.008
D	2.820	3.020	D	0.111	0.119
E	1.500	1.700	E	0.059	0.067
E1	2.650	2.950	E1	0.104	0.116
e	0.95(BSC)		e	0.037(BSC)	
e1	1.800	2.000	e1	0.071	0.079
L	0.300	0.600	L	0.012	0.024
θ	0°	8°	θ	0°	8°

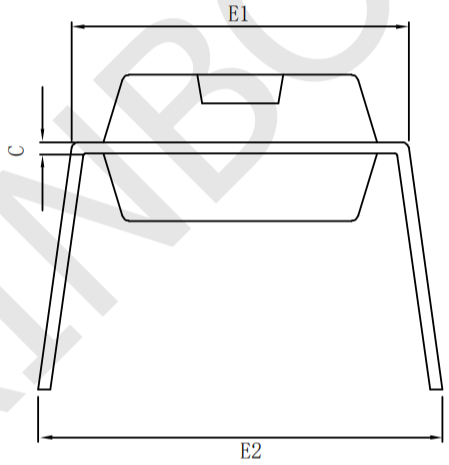


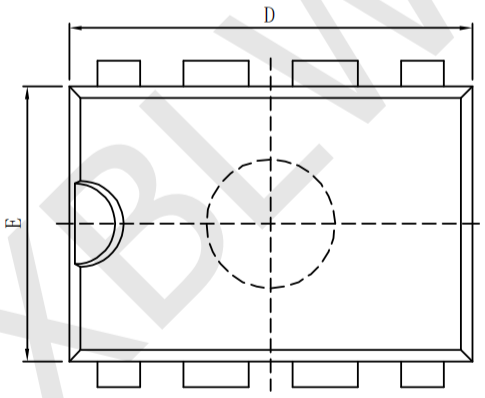
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• DIP-8

Size / Symbol	Dimensions In Millimeters		Size / Symbol	Dimensions In Inches	
	Min(mm)	Max(mm)		Min(in)	Max(in)
A	3.710	4.310	A	0.146	0.170
A1	0.510		A1	0.020	
A2	3.200	3.600	A2	0.126	0.142
B	0.380	0.570	B	0.015	0.022
B1	1.524(BSC)		B1	0.060(BSC)	
C	0.204	0.360	C	0.008	0.014
D	9.000	9.400	D	0.354	0.370
E	6.200	6.600	E	0.244	0.260
E1	7.320	7.920	E1	0.288	0.312
e	2.540(BSC)		e	0.100(BSC)	
L	3.000	3.600	L	0.118	0.142
E2	8.400	9.000	E2	0.331	0.354



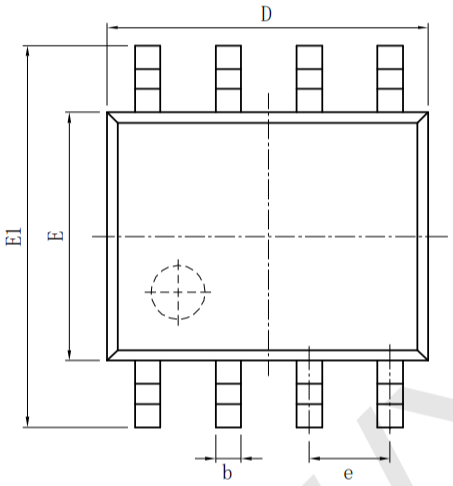


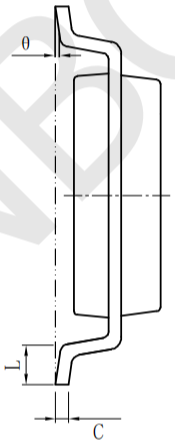


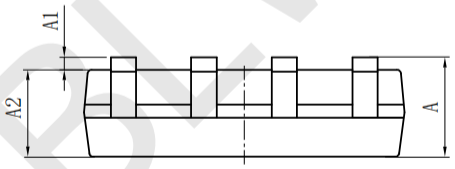
XBLW / XINBOLE

• SOP-8

Size / Symbol	Dimensions In Millimeters		Size / Symbol	Dimensions In Inches	
	Min(mm)	Max(mm)		Min(in)	Max(in)
A	1.350	1.750	A	0.053	0.069
A1	0.100	0.250	A1	0.004	0.010
A2	1.350	1.550	A2	0.053	0.061
b	0.330	0.510	b	0.013	0.020
c	0.170	0.250	c	0.006	0.010
D	4.700	5.100	D	0.185	0.200
E	3.800	4.000	E	0.150	0.157
E1	5.800	6.200	E1	0.228	0.224
e	1.270(BSC)		e	0.050(BSC)	
L	0.400	1.270	L	0.016	0.050
θ	0°	8°	θ	0°	8°



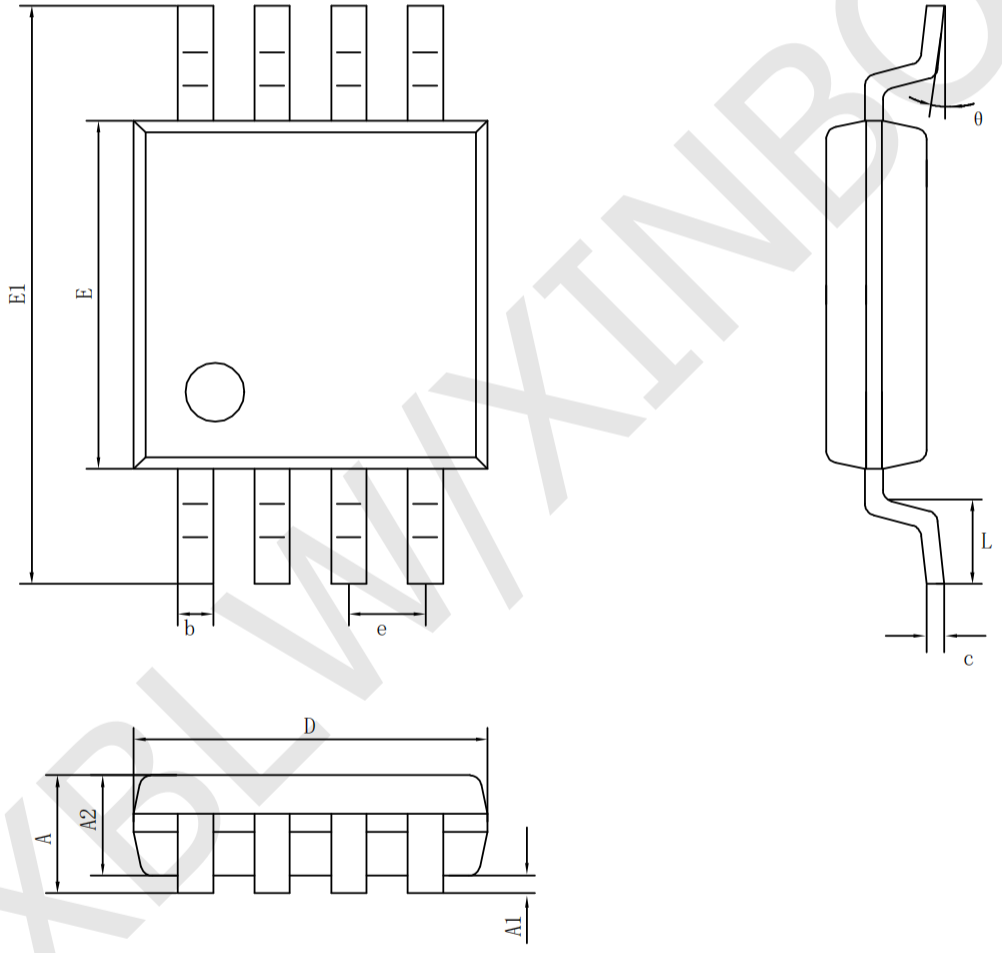




XBLW/XINBOLE

· MSOP-8

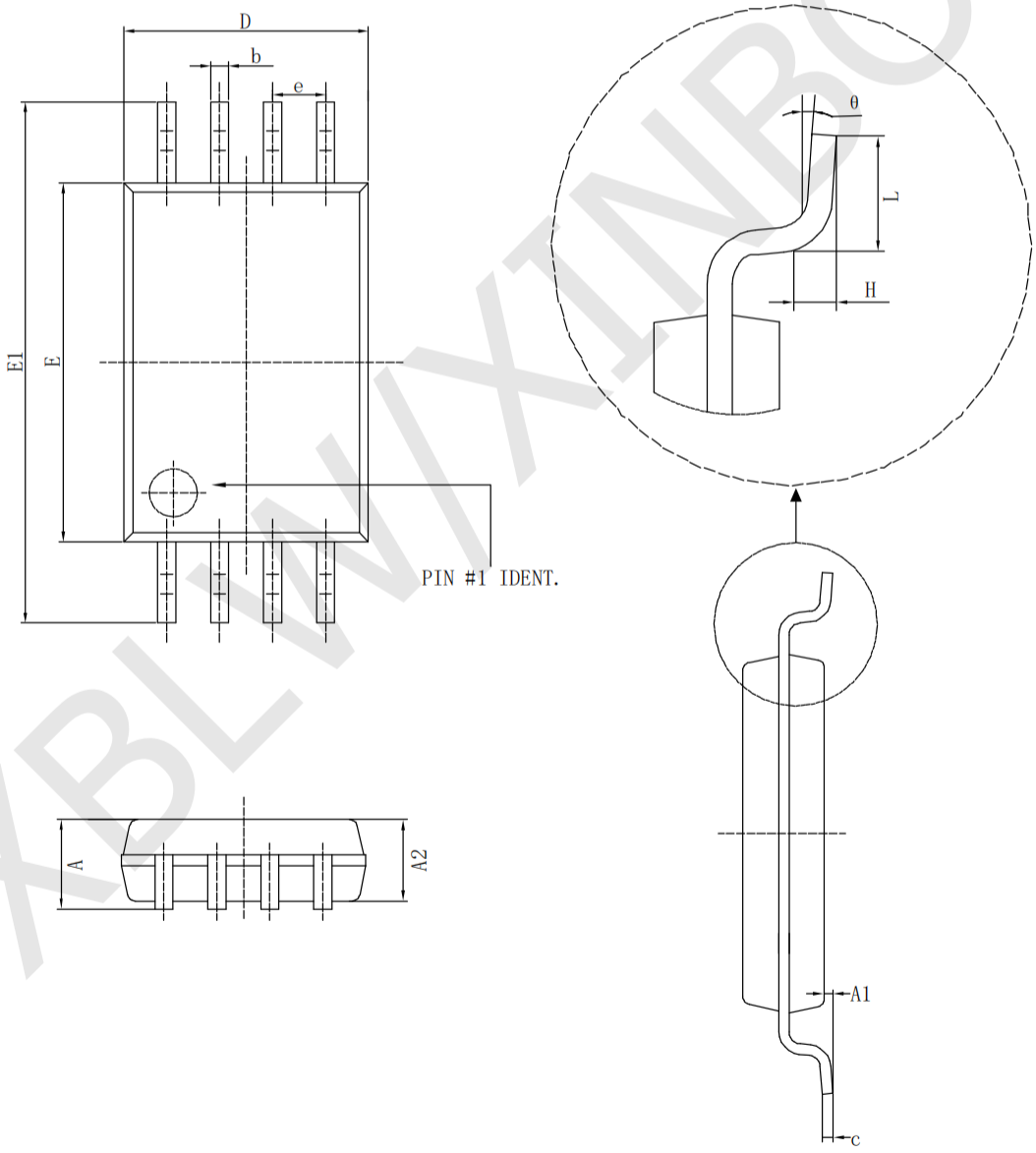
Size / Symbol	Dimensions In Millimeters		Size / Symbol	Dimensions In Inches	
	Min(mm)	Max(mm)		Min(in)	Max(in)
A	0.820	1.100	A	0.320	0.043
A1	0.020	0.150	A1	0.001	0.006
A2	0.750	0.950	A2	0.030	0.037
b	0.250	0.380	b	0.010	0.015
c	0.090	0.230	c	0.004	0.009
D	2.900	3.100	D	0.114	0.122
e	0.65 (BSC)		e	0.026(BSC)	
E	2.900	3.100	E	0.114	0.122
E1	4.750	5.050	E1	0.187	0.199
L	0.400	0.800	L	0.016	0.031
θ	0°	6°	θ	0°	6°



XBLW/XINBOLE

· TSSOP-8

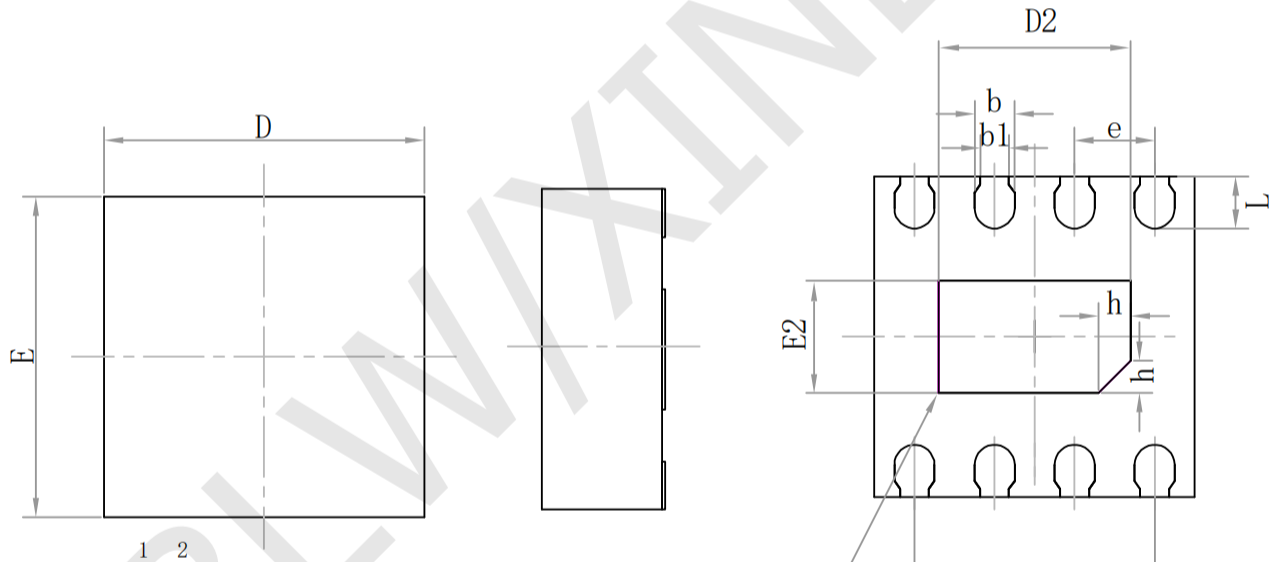
Size / Symbol	Dimensions In Millimeters Min(mm)	Max(mm)	Size / Symbol	Dimensions In Inches Min(in)	Max(in)
D	2.900	3.100	D	0.114	0.122
E	4.300	4.500	E	0.169	0.177
b	0.190	0.300	b	0.007	0.012
c	0.090	0.200	c	0.004	0.008
E1	6.250	6.550	E1	0.246	0.258
A		1.100	A		0.043
A2	0.800	1.000	A2	0.031	0.039
A1	0.020	0.150	A1	0.001	0.006
e	0.65(BSC)		e	0.026(BSC)	
L	0.500	0.700	L	0.020	0.028
H	0.25(TYP)		H	0.01(TYP)	
θ	1°	7°	θ	1°	7°

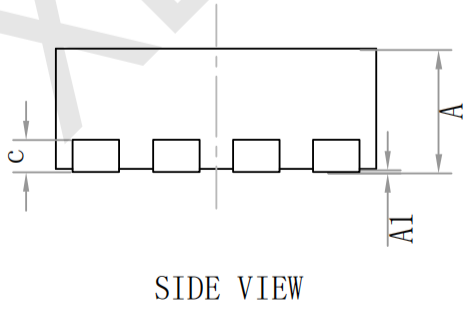


XBLW/XINBOLE

· DFN-8

Size / Symbol	Dimensions In Millimeters		Size / Symbol	Dimensions In Inches	
	Min(mm)	Max(mm)		Min(in)	Max(in)
A	0.450	0.550	A	0.017	0.021
A1	0.000	0.050	A1	0.000	0.002
b	0.180	0.300	b	0.007	0.039
b1	0.160(REF)		b1	0.006(REF)	
c	0.100	0.200	c	0.004	0.008
D	1.900	2.100	D	0.075	0.083
D2	1.400	1.600	D2	0.055	0.062
e	0.500(BSC)		e	0.020(BSC)	
Nd	1.500(BSC)		Nd	0.059(BSC)	
E	2.900	3.100	E	0.114	0.122
E2	1.500	1.700	E2	0.059	0.067
L	0.300	0.500	L	0.012	0.020
h	0.200	0.300	h	0.066	0.120

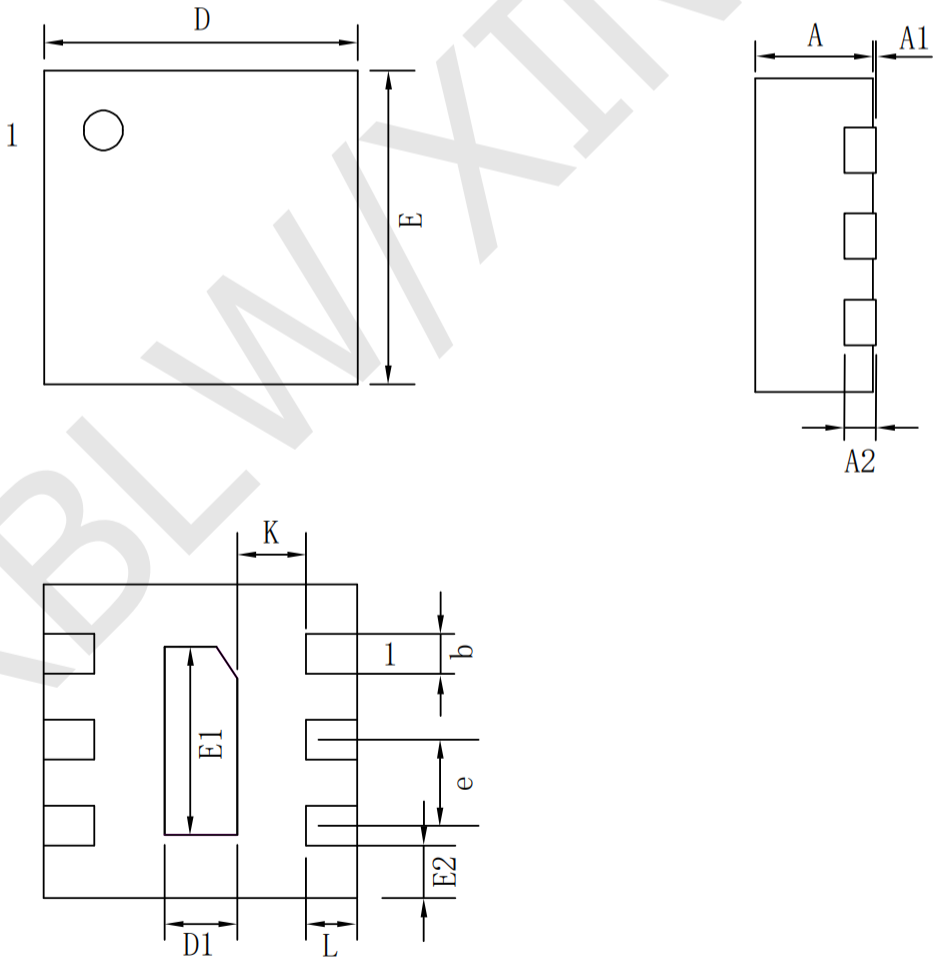




XBLW/XINBOLE

· DFN-6

Size / Symbol	Dimensions In Millimeters			Size / Symbol	Dimensions In Inches		
	Min(mm)	Nom(mm)	Max(mm)		Min(in)	Nom(in)	Max(in)
A	0.450	0.500	0.550	A	0.018	0.020	0.022
	0.500	0.550	0.600		0.020	0.022	0.024
	0.700	0.750	0.800		0.028	0.030	0.031
A1	0.000		0.050	A1	0.000		0.002
A2		0.203(TIY)		A2		0.008(TIY)	
b	0.170	0.220	0.270	b	0.007	0.009	0.011
D	1.450	1.500	1.550	D	0.057	0.059	0.061
D1	0.350	0.400	0.450	D1	0.014	0.016	0.018
E	1.450	1.500	1.550	E	0.057	0.059	0.061
E1	0.950	1.000	1.050	E1	0.037	0.039	0.041
E2		0.170(TYP)		E2		0.007(TYP)	
e		0.470(BSC)		e		0.019(BSC)	
K		0.300(BSC)		K		0.012(BSC)	
L	0.200	0.250	0.300	L	0.008	0.010	0.012



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